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Developing High-Performance, Low-Power Audio/Voice Subsystems Using Customizable DSP Blocks and Audio Interface IP

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As applications such as mobile gaming and voice triggering grow in popularity, audio/voice subsystems are becoming more important in many mobile system-on-chip (SoC) designs. Subsystem requirements have evolved to address multiple demands: high-performance, high-resolution audio stream processing, and always-on, low-power voice trigger and recognition. This white paper describes how customizable digital signal processing (DSP) and audio/voice subsystem solution intellectual property (IP) blocks can be used to cost-effectively and efficiently develop and deliver high-performance audio/voice products.

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Introduction

The emergence of smartphones and tablets over the last decade has driven innovation and created an increasing need for high-performance audio and video applications for personalization and consumer appeal. Emerging applications such as mobile gaming and voice trigger and recognition are changing the requirements of audio/voice subsystem performance. Today's developers are challenged by a growing demand for high-performance, high-resolution multi-channel audio stream processing combined with the demand for always-on voice trigger and speech recognition intelligence at extremely low power.

Designing an audio/voice subsystem that meets these growing demands requires advanced digital signal processing (DSP) technology and a well-architected system solution. Industry-leading, highly customizable DSP and audio/voice subsystem solution intellectual property (IP) blocks are a cost-effective way to deliver high-performance audio/voice products that meet time-to-market goals.

Mobile Audio/Voice Subsystems

In the mobile audio subsystem shown in Figure 1, an audio DSP core handles the main audio data processing, including stream encoding/decoding to different compression standards, sample rate conversion, pre- and post-processing, noise suppression, voice trigger/speech recognition, etc. If the audio DSP core is integrated into the application processor system on chip (SoC), the DSP core will be an offload processor on the SoC bus hierarchy with access to the SoC's main memory system. If the DSP is not integrated, a dedicated bus interface connects the application processor SoC to the stand-alone DSP. A shared or point-to-point digital bus interface connects audio peripherals such as the microphones (MICs) and speakers to the DSP core. The audio peripheral ICs contain the analog components, such as digital-to-

analog converter (DAC)/analog-to-digital converter (ADC), analog filters, and amplifiers. In addition to connecting the audio peripherals, audio interfaces may need to connect to the cellular baseband or WiFi/BT/FM radio combo devices to support voice calls in smartphones and Bluetooth audio or audio stream from FM radio.

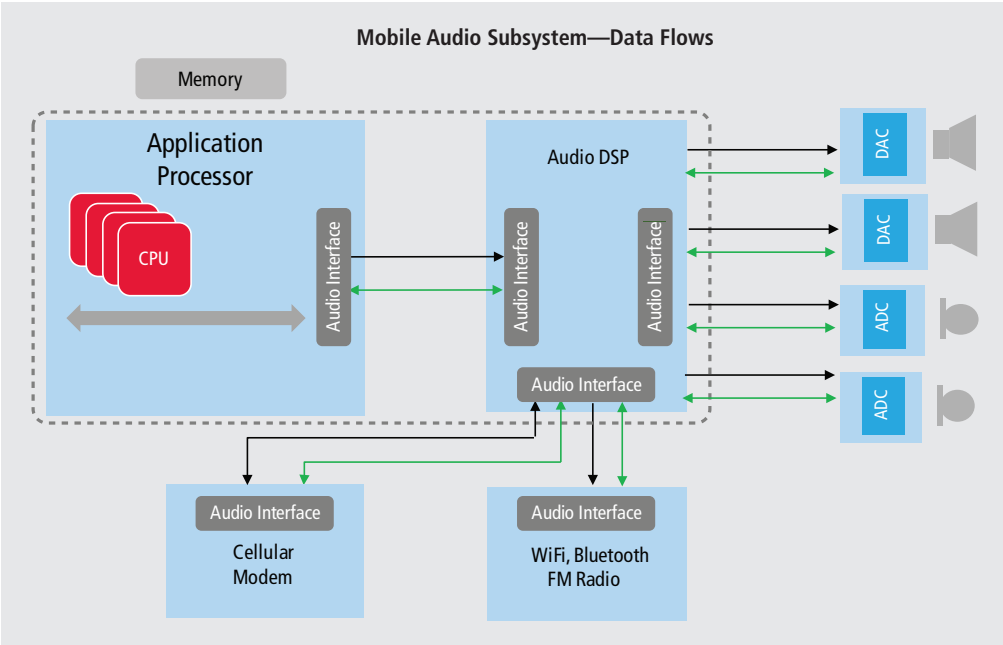

Figure 1. Representative Mobile Audio/Voice Subsystem

Audio Data Processing—High Performance, Low Power

The demand for high-performance DSP is driven by both voice and audio processing needs. Voice processing requirements such as wideband (AMR-WB) and super wideband voice codecs to support high-performance voice over IP (VoIP) and improved noise suppression and noise-dependent volume control pre-processing are raising the audio DSP processing complexity by a factor of 2X to 4X. On the audio side, the codec complexity peaked with the introduction of multi-channel lossless versions, such as Dolby TrueHD, MS10, and MS11, and DTS Master Audio, M6, and M8. This demand has sparked significant innovation in post-processing as shown in Table 1. The demand for high performance is also driving audio DSPs to have more parallel, higher precision multiply-accumulators (MACs).

Volume Leveling	Dialog Clarity	Volume Boost	Spatial Expansion	Bass and Treble Boost	Equalization	3D Audio
• Dolby Volume • DTS TruVolume • Audyssey Dynamic Volume	• DTS TruDialog • Dolby DS1	• DTS Boost • Dolby DS1 • Audyssey Volume Extension	• DTS TruSurround HD • DTS Envelo	• DTS TruBass • QSizzle and QRumble	• DTS TruEQ • Audyssey EQ	• Dolby ATMOS • DTS MDA

Table 1. Audio Post-Processing

While the demand for performance is increasing, the demand for a lower power profile is also increasing from two perspectives:

- With battery life restrictions of mobile devices, the system power profile for high-end audio applications like mobile gaming or professional-grade audio playback cannot keep increasing linearly with the data-processing performance
- The audio system needs to be always on in new applications such as voice trigger or speech recognition

Both perspectives require the DSP architecture to be extremely scalable and efficient. DSP architectures with scalable instruction set extensions, configurable memory and I/O partitions, and advanced power management features are the best to address both the high-performance and the low-power demands.

Audio Transport Efficiency

To reduce the power profile and support low-power applications like voice trigger, the efficiency of audio data transport also needs to be considered in addition to the power efficiency of the audio DSP. Two optimization points can help reduce the power of audio transport.

The first optimization point is to change the audio data transport model from a system memory-based model to a DSP-tunneled model. A system memory-based model places the audio data pre- and post-DSP processing into system memory across the SoC bus hierarchy. This model requires the system memory and SoC bus hierarchy to be always powered during the audio data processing. In this model, audio data traverses the SoC bus hierarchy multiple times. Data access through the high-frequency SoC bus hierarchy and system memory consumes significant power and prevents efficient support of always-on applications. In the DSP tunneled model, the audio data processing and transmit/receive through the audio interface are localized to the DSP processor with dedicated local memory and highly efficient FIFO-style interfaces. The local system is clocked at much lower frequency and the power consumption of the subsystem is significantly reduced.

The second optimization point is to use new audio interface standards that are designed to support multiple audio peripheral devices with low I/O pin count and power efficiency. Recently, the MIPI Alliance has established two new audio interface standards to optimize audio subsystem connectivity: Slimbus targets the connectivity between the application processor and the standalone DSP codec, and Soundwire targets many audio devices, including DSP codec and audio peripheral devices. The Soundwire standard can be scaled up to support multiple data lanes to transport wide PCM audio samples between the application processor and the DSP codec, and can also be optimized to support the transport of narrow PDM samples to MICs and speakers on a single data lane. The Soundwire standard defines a modified NRZI data encoding and double data rate for data transmission to minimize active driving and switching of the bus wire load. In addition, the standard contains a well-defined clock rate changing scheme and clock stop protocol to further minimize power consumption in always-on applications. The audio subsystem optimized by the Soundwire standard is shown in Figure 2.

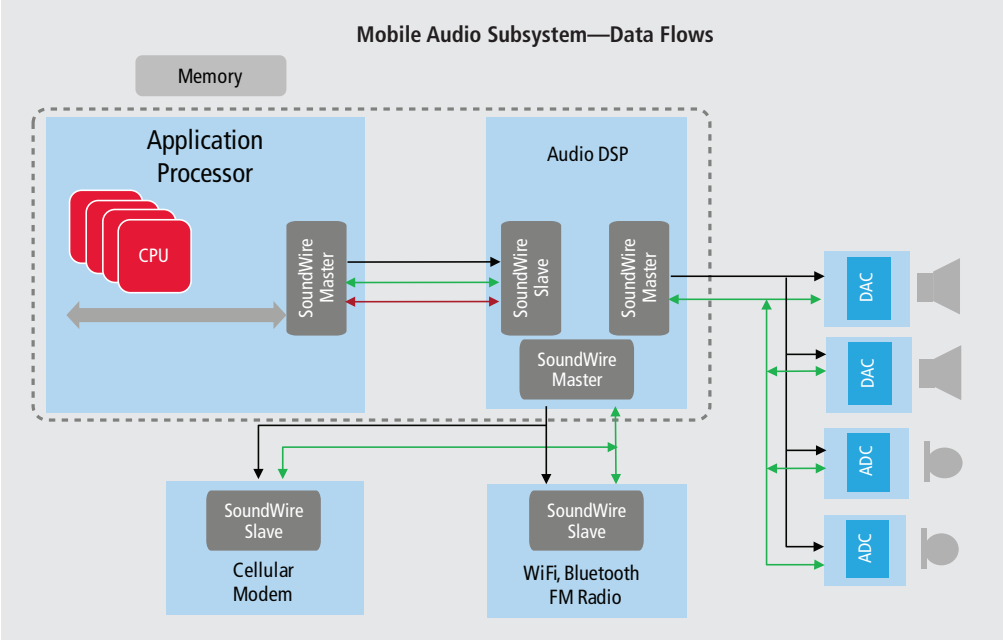

Figure 2. Soundwire-Based Audio Subsystem Optimization

Broad Portfolio of Configurable, Silicon-Proven IP

Cadence offers a broad, silicon-proven IP portfolio covering a variety of capabilities to support audio subsystem development, including audio DSP processor IP blocks and a variety of audio interface IP blocks. The IP cores are highly configurable and scalable, and they provide the flexibility to support customization.

Audio DSP IP

Cadence's Tensilica® Xtensa® processor family offers highly customizable processor cores with built-in architecture support for high-efficiency instruction set architecture (ISA) extensions. Cadence Tensilica HiFi processors—industry-leading audio DSP processors—use the flexible Tensilica Instruction Extensions (TIE) in several highly optimized products targeting mobile, consumer, and automotive audio applications with different power/performance requirements:

- HiFi Mini—Optimized for voice trigger and recognition
- HiFi EP—Optimized for consumer electronics, Blu-ray players, digital television, etc.
- HiFi 2—Cost-optimized for mobile audio and voice applications
- HiFi 3—Optimized for high-performance audio in-home or mobile entertainment

Audio Interface IP

Cadence offers a variety of audio interface IP cores that enable complete audio subsystem design. Mature audio interface IP cores that have been licensed to many customers include the I2S master/slave controller, S/PDIF controller, and MIPI Slimbus manager/device controller. Most recently, Cadence is leading the definition and development of the MIPI Soundwire standard. The Soundwire master/slave controller IP is under development and will become available after the standard is finalized.

Summary

As mobile and consumer devices evolve, their audio subsystems require even higher performance and lower power. Emerging applications such as voice trigger and recognition and mobile gaming increase audio processing complexity even further. These applications require audio subsystem designers to deliver always-on features at very low power and extremely high-quality audio effects for multiple audio channels. Cadence's industry-leading audio DSP processor IP cores and audio interface IP cores offer high-performing products enabling customers to build optimized audio subsystems with the ideal balance of functionality and low power consumption.

For Further Information

To learn more about Cadence's Tensilica Xtensa processor family, please visit http://ip.cadence.com/ipportfolio/tensilica-ip/xtensa-customizable.

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