# JPEG Image Compression with 2D DCT

2019170993 김두현

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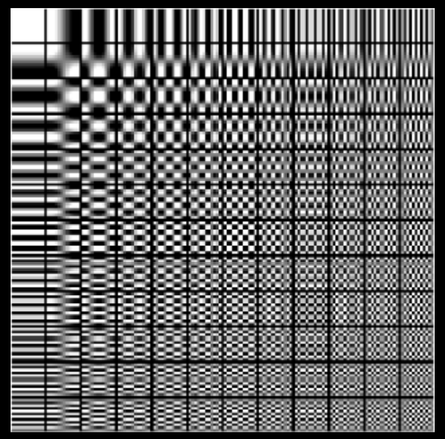
# DCT Algorithm

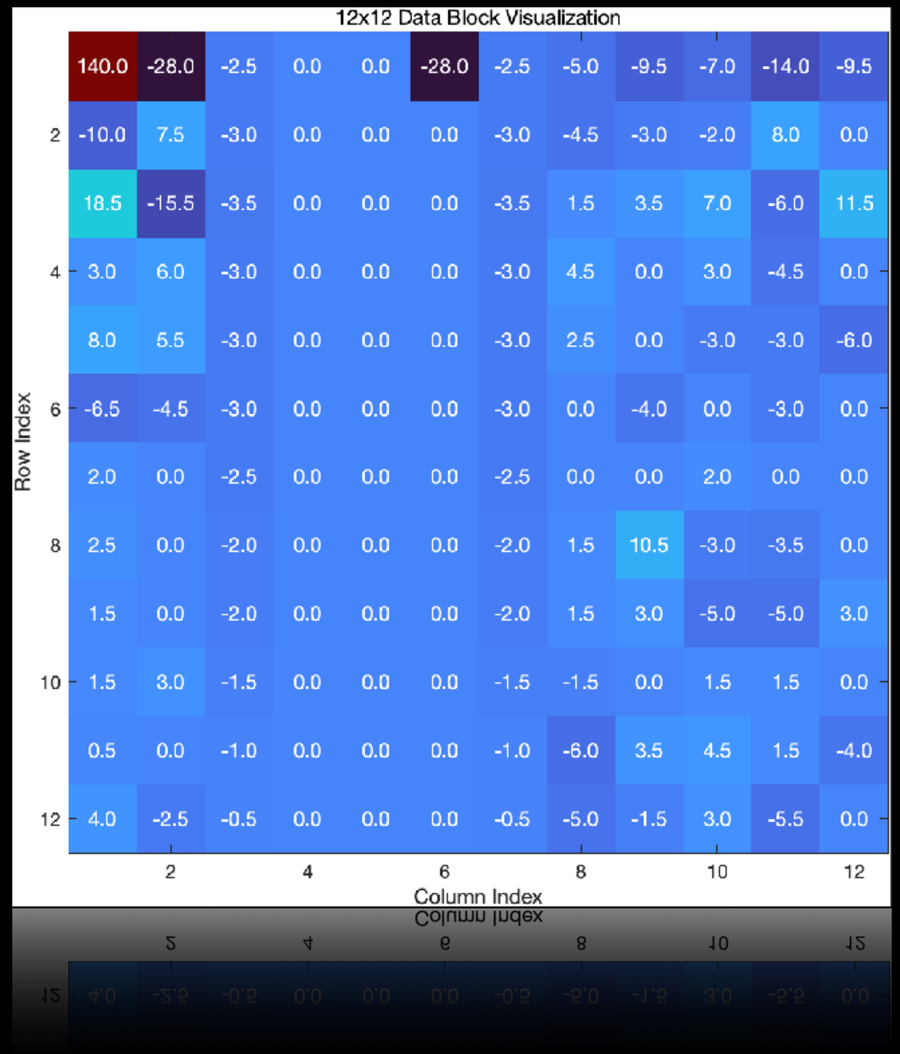
## JPEG

+



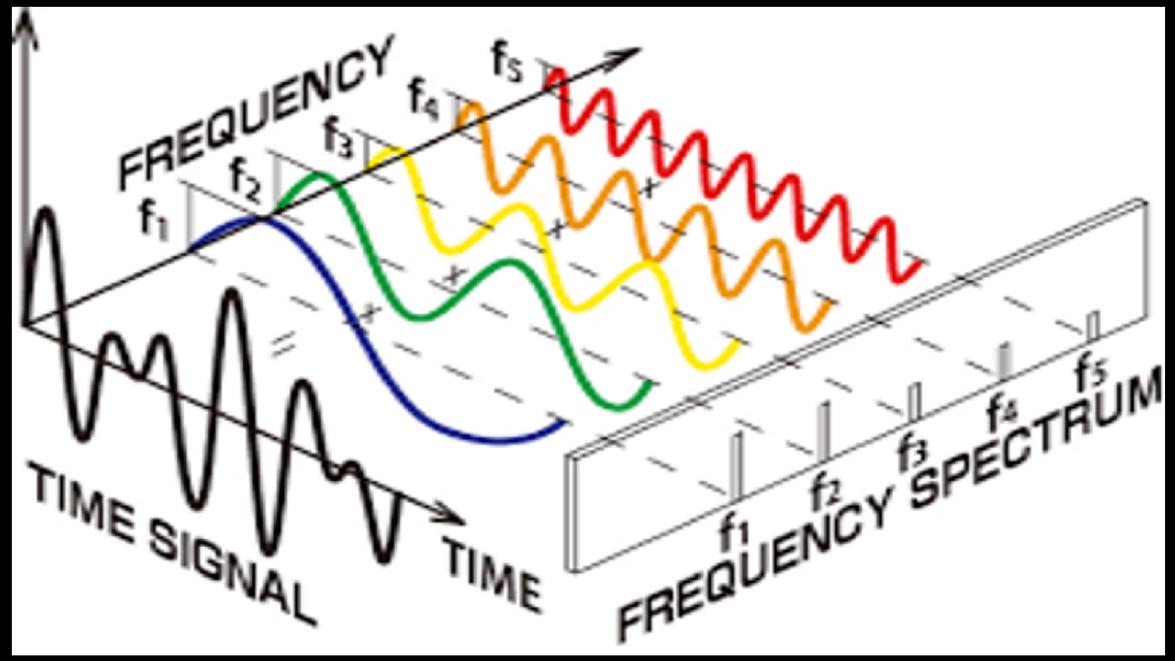
Frequency Domain

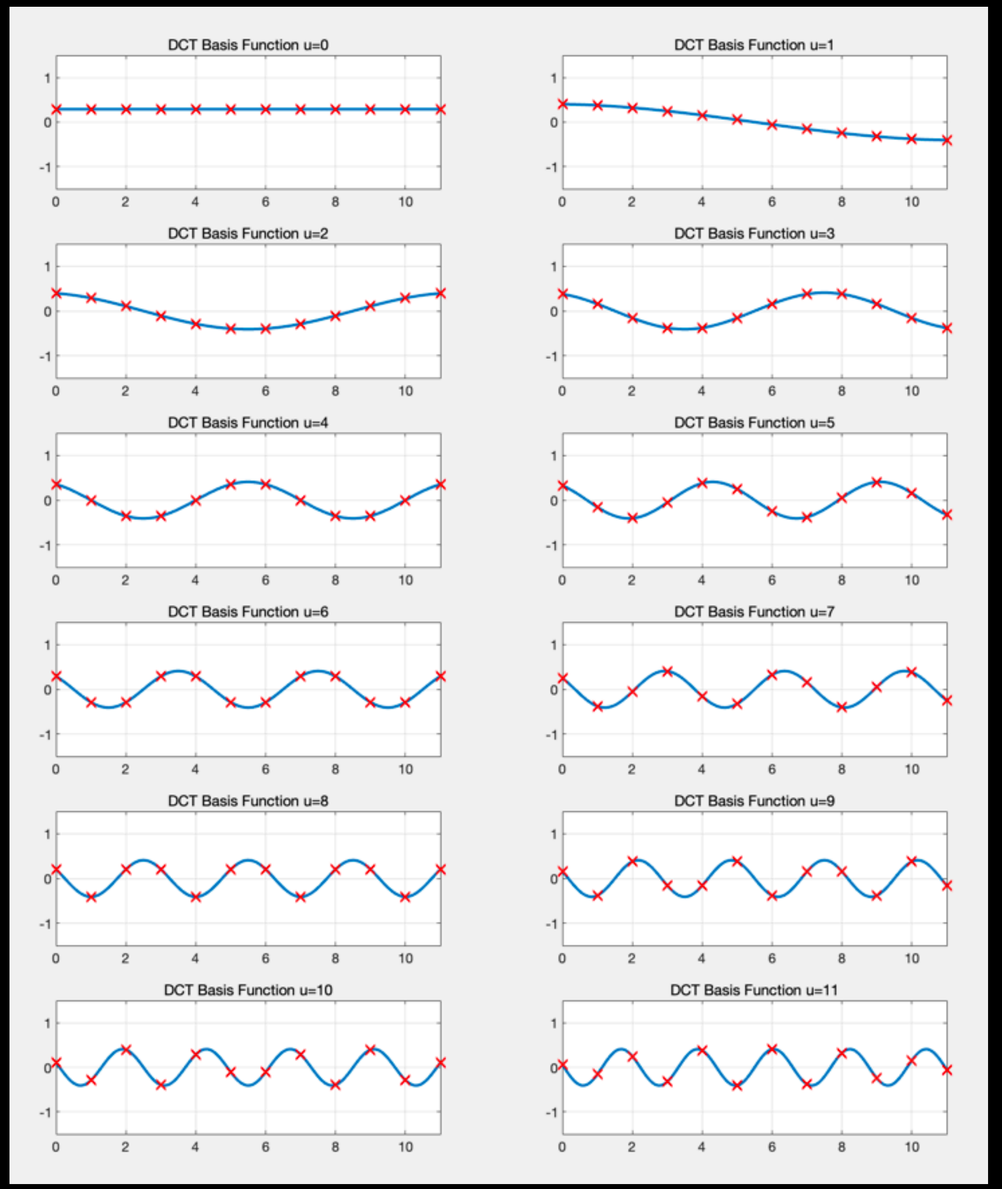
2D-DCT output



# DCT Algorithm

## Basis function

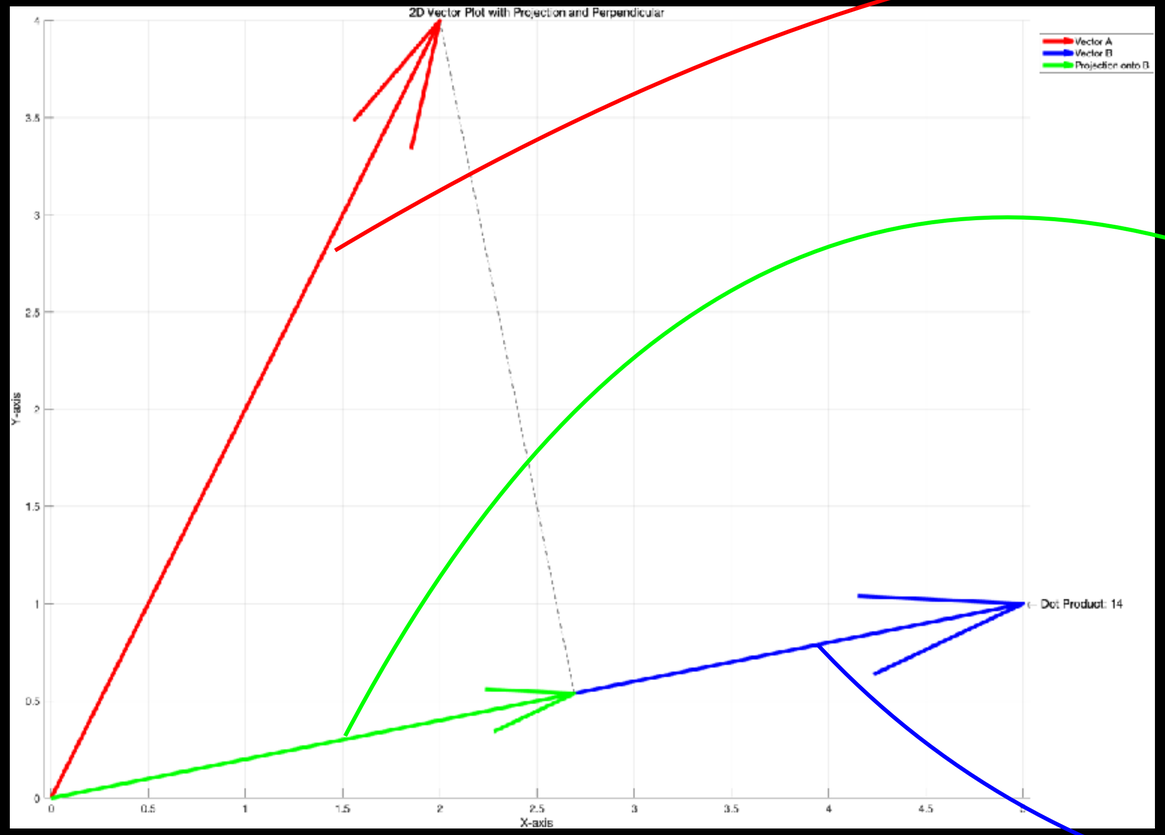


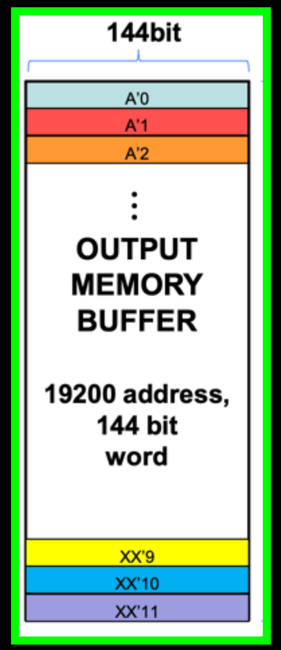




12x12 DCT Basis Function

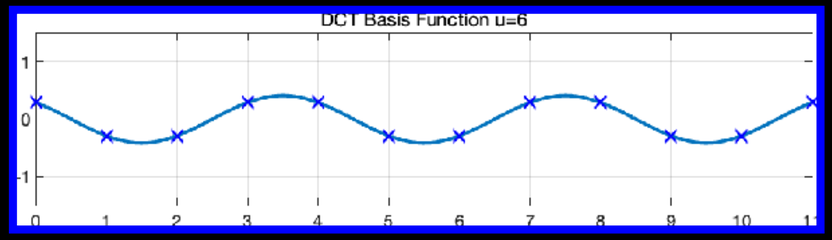
# DCT Algorithm

## Dot product between Cosine and Image Signal







# Basic Structure

## Ver 1.

8 bit

1D -DCT
(row-wise)

22 bit

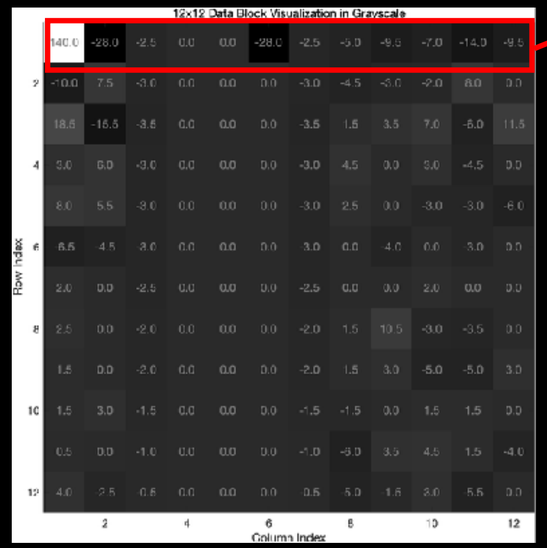
Transpose
Memory

22 bit

1D -DCT
(column-wise)

- Coefficient Multiplying
- No quantization
- TP MEM x 4

36 bit



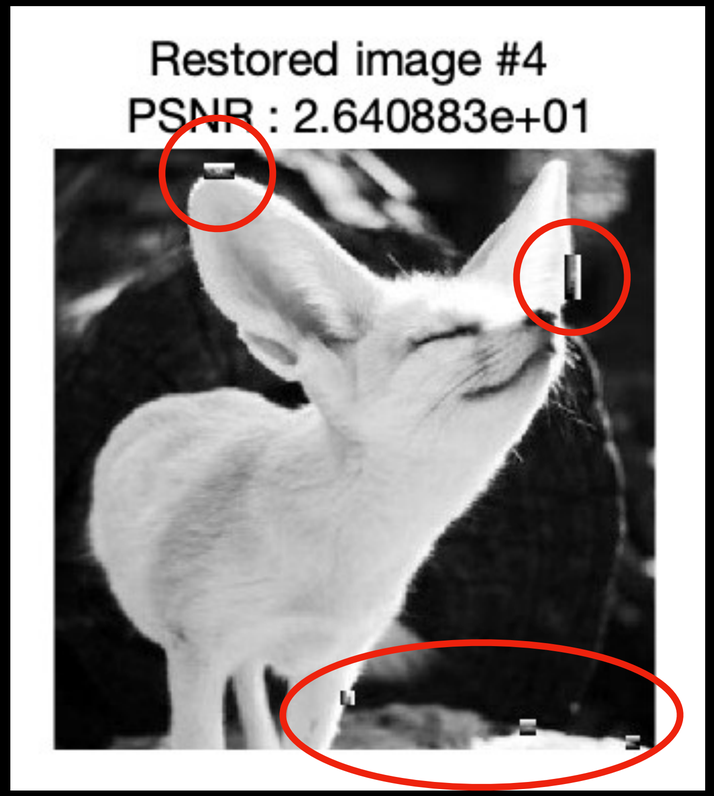

In TP_MEM

12 bit

Output
Memory

# Overflow fixed

## Ver 2.




`overflow_chcker`

Glitching Effect는 해당 bit의 연산의 최종 결과값의 signed bit을
마지막 12bit quantization을 할 때 포함지 못하여 발생한다.

↓

(Solution)
연산 중간 과정에서 signed bit (MSB) 을 기억하고,
마지막 12bit quantization 과정에 overflow 여부를 확인

↓

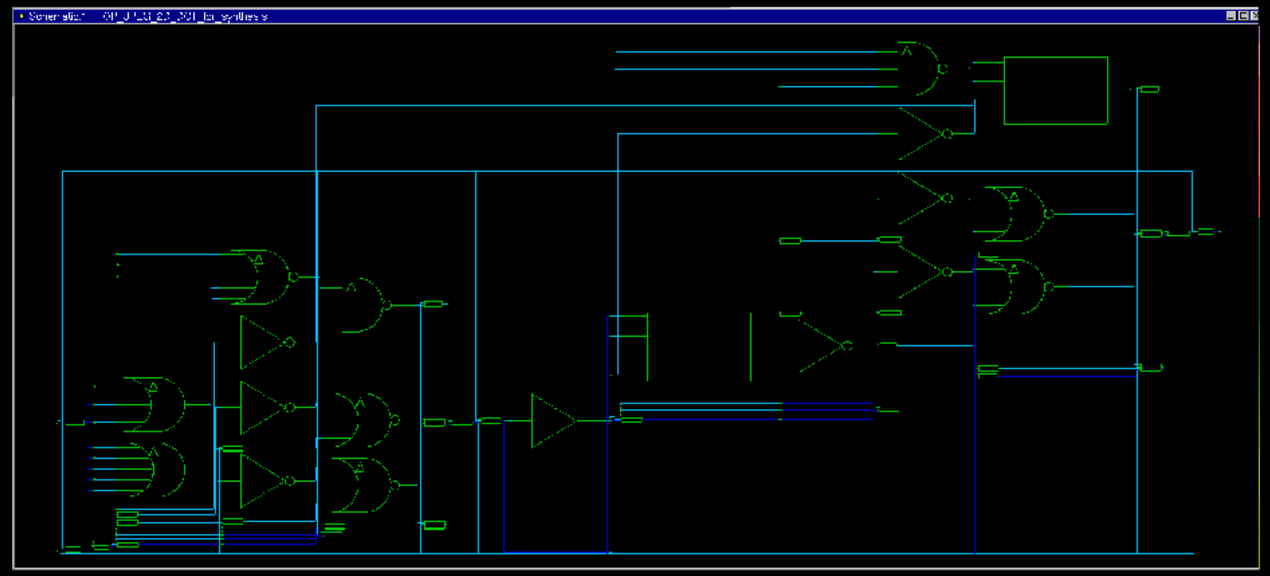
Overflow 시, 12’b0111_1111_1111 으로 처리
Underflow 시,  12’b1000_0000_000 으로 처리

# Overflow fixed

## PSNR

# Overflow fixed

## Synthesis Results



Combinational area: 4659445.898502
Noncombinational area: 2313652.221420
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 6973098.000000

Cell Internal Power = 122.5510 mW (86%)
Net Switching Power = 19.7006 mW (14%)

---

Total Dynamic Power = 142.2516 mW (100%)

# Overflow fixed

## Synthesis Results

Total cell area: 6973098.000000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 900605 |
| DCT_second_stage | 3227965 |
| tp_memory_1_top | 818188 |
| tp_memory_1_down | 818453 |
| tp_memory_2_top | 457796 |
| tp_memory_2_down | 456153 |

# Coefficient Quantized

## Basic Ver 1.

8 bit

1D -DCT
(row-wise)

22 bit

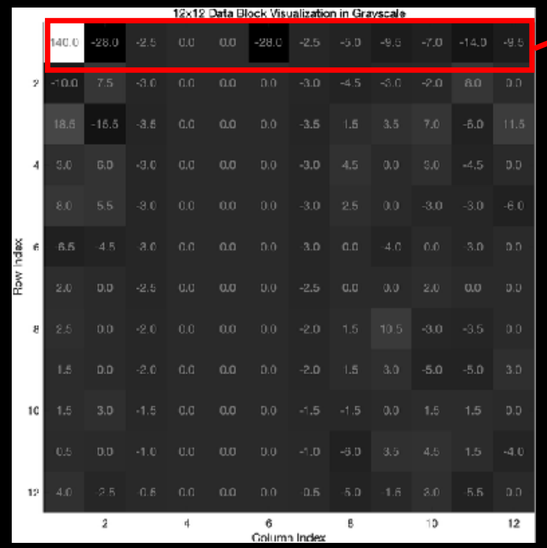
Transpose
Memory

22 bit

1D -DCT
(column-wise)

- Coefficient Multiplying
- No quantization
- TP MEM x 4

36 bit




12 bit

Output
Memory

# Coefficient Quantized

## Ver 3.

Matlab에서 확인 결과,

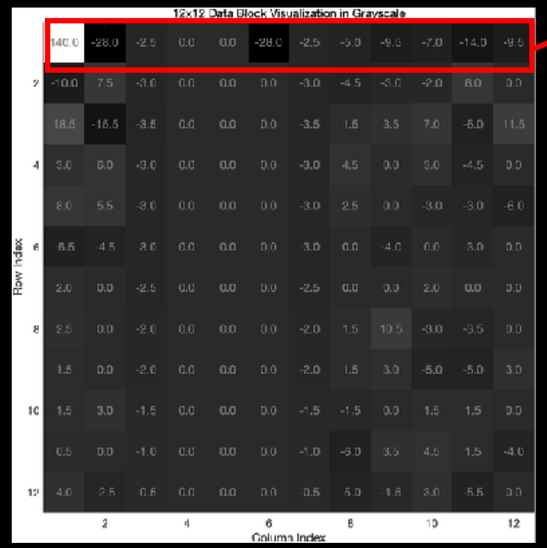
C_quantization_bit = 8;
Result_1D_DCT_quantization_bit = 9;

가 PNSR >= 30 을 보존하는 마지노선으로 판단

8 bit → 1D -DCT (row-wise) → 9 bit → 12bit → Transpose Memory → 12 bit → 1D -DCT (column-wise)

- Coefficient Multiplying
- No quantization
- TP MEM x 4

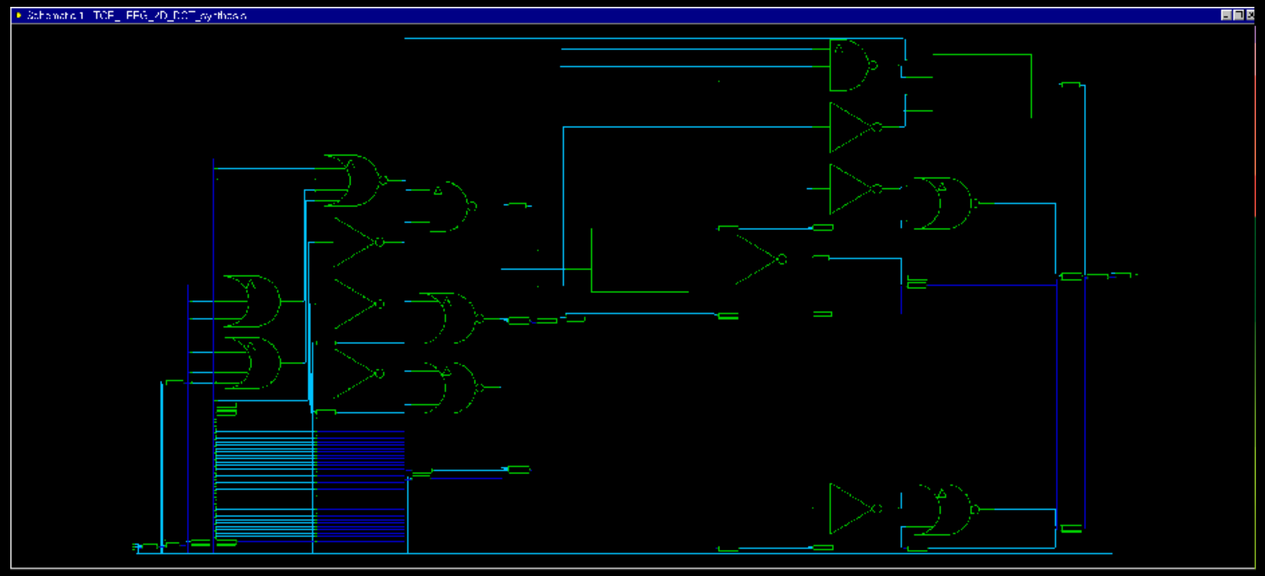
24 bit →




→ 12 bit → Output Memory

# Coefficient Quantized

## Synthesis Results



Combinational area: 2096874.500732
Noncombinational area: 1632597.973465
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 3729472.500000

Cell Internal Power = 83.2862 mW (88%)
Net Switching Power = 11.6557 mW (12%)

---

Total Dynamic Power = 94.9419 mW (100%)

# Coefficient Quantized

## Synthesis Results

Total cell area: 6973098.000000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 575021 |
| DCT_second_stage | 1115634 |
| tp_memory_1_top | 455556 |
| tp_memory_1_down | 454262 |
| tp_memory_2_top | 458260 |
| tp_memory_2_down | 456551 |

# Coefficient Symmetric Properties

## Ver 4.

Input을 변형하고,
최대한 적은 ASU (Adder Shift Unit) 을 활용

→ ASU 총 6개

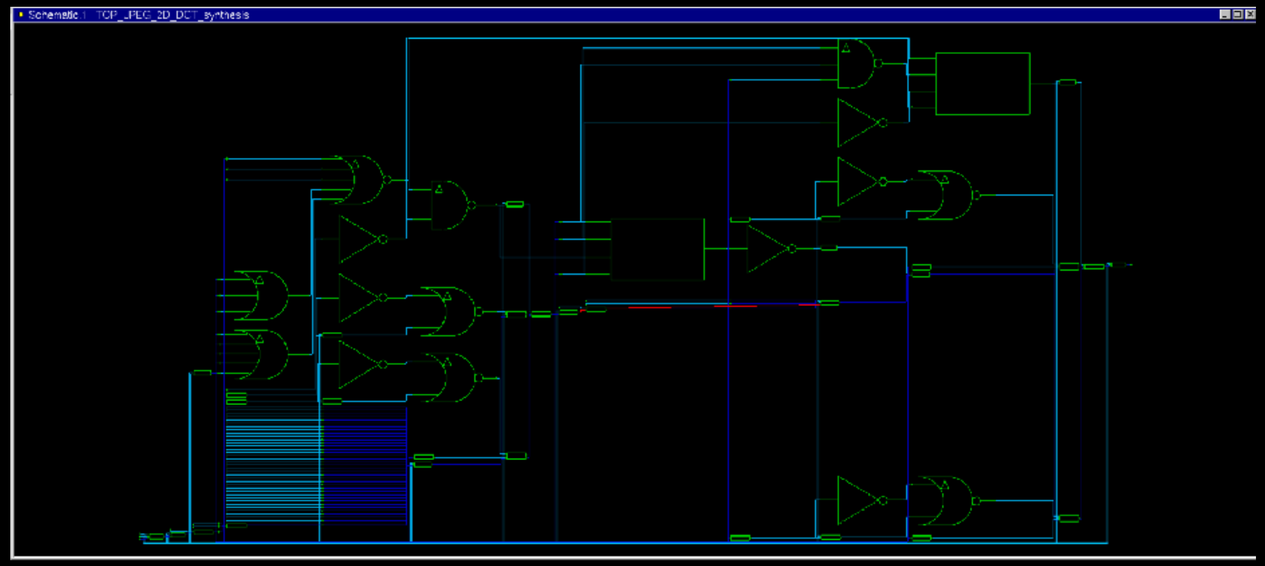
```
assign out0 = c6 * (a1+a2+a3+a4+a5+a6);  1)
assign out2 = c2*b1 + c6*b2 + c10*b3; 3)
assign out4 = c4*(e1-e3) + c12*e2; 5)
assign out6 = c6 * (a1 - a2 - a3 + a4 + a5 - a6); 1)
assign out8 = c8*(e1+e3) - c0*e2; 6)
assign out10 = c10*b1 - c6*b2 + c2*b3; 3)

assign out1 = c1*v1 + c3*v2 + c5*v3 + c7*v4 + c9*v5 + c11*v6; 2)
assign out3 = c3*d1 + c9*d2; 4)
assign out5 = c5*v1 - c9*v2 - c1*v3 - c11*v4 + c3*v5 + c7*v6; 2)
assign out7 = c7*v1 - c3*v2 - c11*v3 + c1*v4 - c9*v5 - c5*v6; 2)
assign out9 = c9*d1 - c3*d2; 4)
assign out11 = c11*v1 - c9*v2 + c7*v3 - c5*v4 + c3*v5 - c1*v6; 2)
```

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1) | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ | $C_6$ |
| 2) | $C_1$ | $C_3$ | $C_5$ | $C_7$ | $C_9$ | $C_{11}$ | $-C_{11}$ | $-C_9$ | $-C_7$ | $-C_5$ | $-C_3$ | $-C_1$ |
| 3) | $C_2$ | $C_6$ | $C_{10}$ | $-C_{10}$ | $-C_6$ | $-C_2$ | $-C_2$ | $-C_6$ | $-C_{10}$ | $C_{10}$ | $C_6$ | $C_2$ |
| 4) | $C_3$ | $C_9$ | $-C_9$ | $-C_3$ | $-C_3$ | $-C_9$ | $C_9$ | $C_3$ | $C_3$ | $C_9$ | $-C_9$ | $-C_3$ |
| 5) | $C_4$ | $C_{12}$ | $-C_4$ | $-C_4$ | $C_{12}$ | $C_4$ | $C_4$ | $C_{12}$ | $-C_4$ | $-C_4$ | $C_{12}$ | $C_4$ |
| | $C_5$ | $-C_9$ | $-C_1$ | $-C_{11}$ | $C_3$ | $C_7$ | $-C_7$ | $-C_3$ | $C_{11}$ | $C_1$ | $C_9$ | $-C_5$ |
| | $C_6$ | $-C_6$ | $-C_6$ | $C_6$ | $C_6$ | $-C_6$ | $-C_6$ | $C_6$ | $C_6$ | $-C_6$ | $-C_6$ | $C_6$ |
| | $C_7$ | $-C_3$ | $-C_{11}$ | $C_1$ | $-C_9$ | $-C_5$ | $C_5$ | $C_9$ | $-C_1$ | $C_{11}$ | $C_3$ | $-C_7$ |
| 6) | $C_8$ | $-C_0$ | $C_8$ | $C_8$ | $-C_0$ | $C_8$ | $C_8$ | $-C_0$ | $C_8$ | $C_8$ | $-C_0$ | $C_8$ |
| | $C_9$ | $-C_3$ | $C_3$ | $-C_9$ | $-C_9$ | $C_3$ | $-C_3$ | $C_9$ | $C_9$ | $-C_3$ | $C_3$ | $-C_9$ |
| | $C_{10}$ | $-C_6$ | $C_2$ | $-C_2$ | $C_6$ | $-C_{10}$ | $-C_{10}$ | $C_6$ | $-C_2$ | $C_2$ | $-C_6$ | $C_{10}$ |
| | $C_{11}$ | $-C_9$ | $C_7$ | $-C_5$ | $C_3$ | $-C_1$ | $C_1$ | $-C_3$ | $C_5$ | $-C_7$ | $C_9$ | $-C_{11}$ |

# Coefficient Symmetric Properties

## Synthesis Results




Combinational area: 1152142.132706
Noncombinational area: 1632664.324524
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 2784806.500000

Cell Internal Power = 74.0896 mW (91%)
Net Switching Power = 7.4053 mW (9%)

---

Total Dynamic Power = 81.4949 mW (100%)

# Coefficient Symmetric Properties

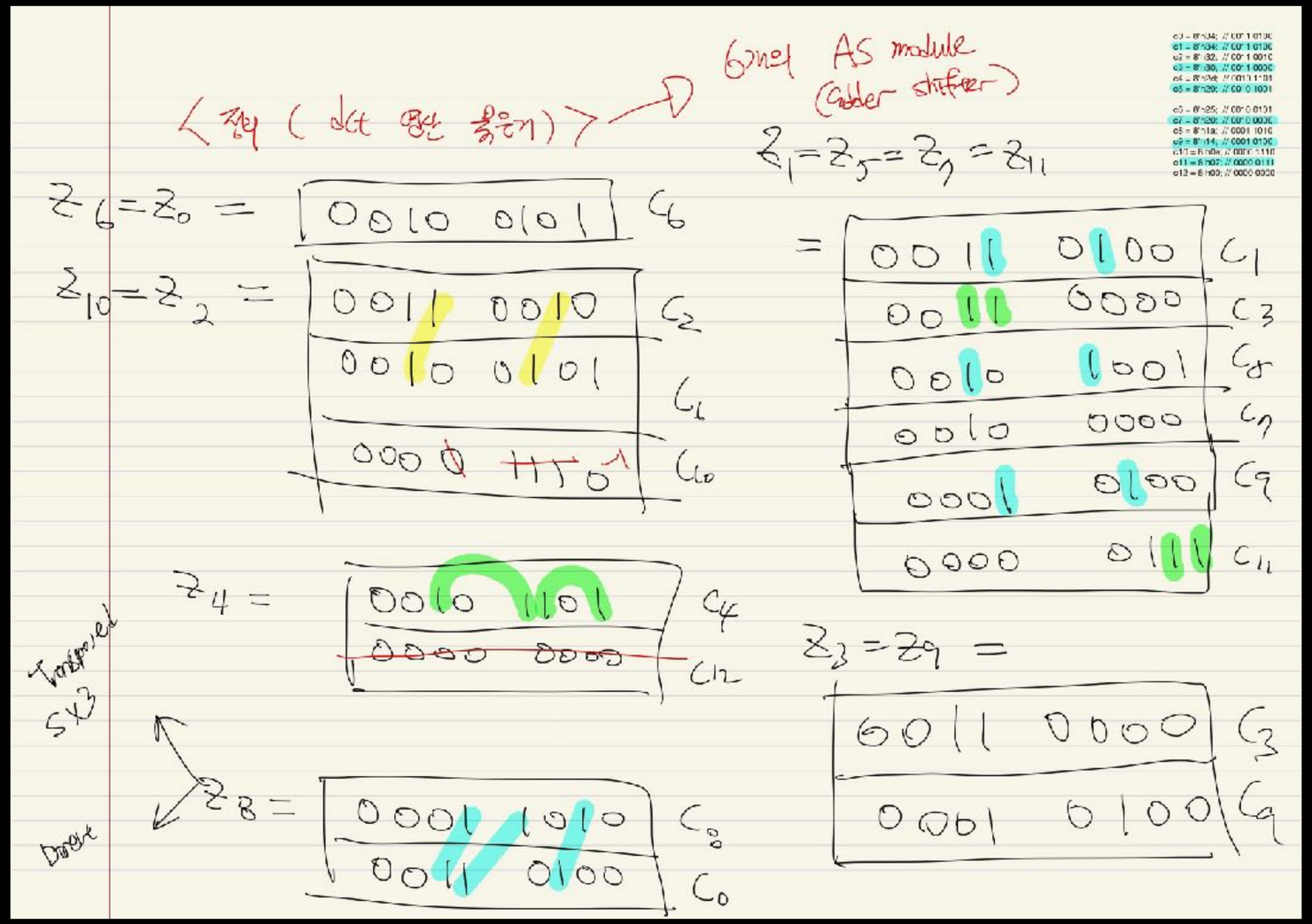
## Synthesis Results

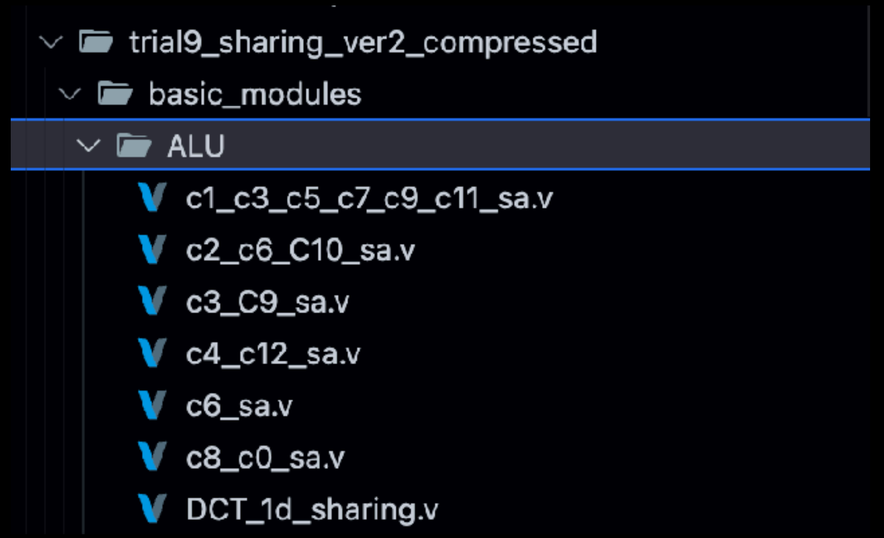
Total cell area: 2784806.500000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 255781 |
| DCT_second_stage | 494894 |
| tp_memory_1_top | 455531 |
| tp_memory_1_down | 454262 |
| tp_memory_2_top | 457597 |
| tp_memory_2_down | 455224 |

# Coefficient Common Factor Sharing

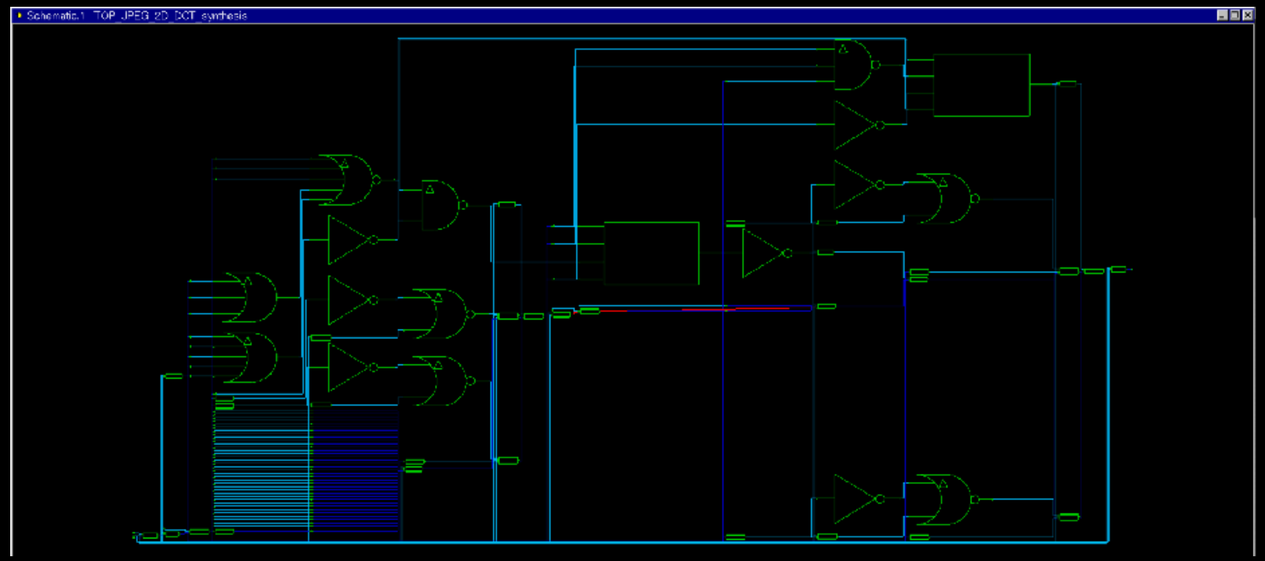
## Ver 5.



# Coefficient Common Factor Sharing

## Synthesis Results




Combinational area: 1150898.065205
Noncombinational area: 1633012.687668
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 2783910.750000

Cell Internal Power = 74.4957 mW (91%)
Net Switching Power = 7.5231 mW (9%)

---

Total Dynamic Power = 82.0188 mW (100%)

# Coefficient Common Factor Sharing

## Synthesis Results

Total cell area: 2784806.500000

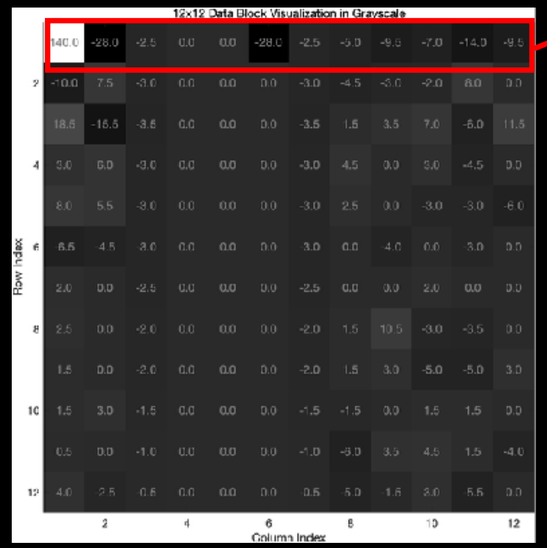
| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 254572 |
| DCT_second_stage | 493156 |
| tp_memory_1_top | 455531 |
| tp_memory_1_down | 454262 |
| tp_memory_2_top | 457613 |
| tp_memory_2_down | 457016 |

# TP_MEM BitWidth Modification

## Ver3. Coefficient Quantized

8 bit → 1D -DCT (row-wise) → 9 bit → 12bit → Transpose Memory → 12 bit → 1D -DCT (column-wise)

24 bit →




12 bit →

Output Memory

Matlab에서 확인 결과,

C_quantization_bit = 8;
Result_1D_DCT_quantization_bit = 9;

가 PNSR >= 30 을 보존하는 마지노선으로 판단

# TP_MEM BitWidth Modification

## Ver 6.

8 bit

1D -DCT
(row-wise)

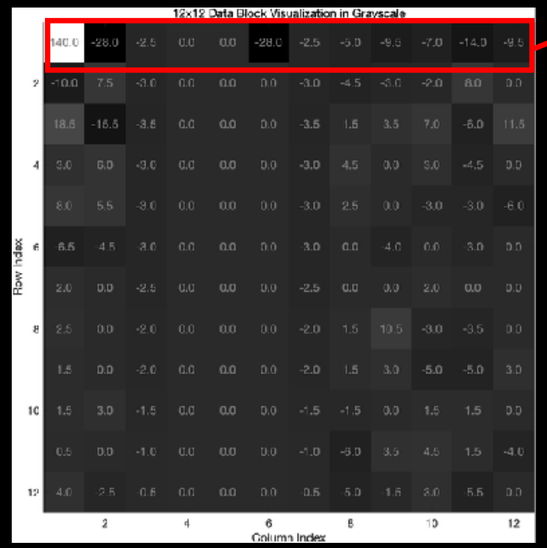
9 bit

Transpose
Memory

9 bit

1D -DCT
(column-wise)

21 bit → 24 bit

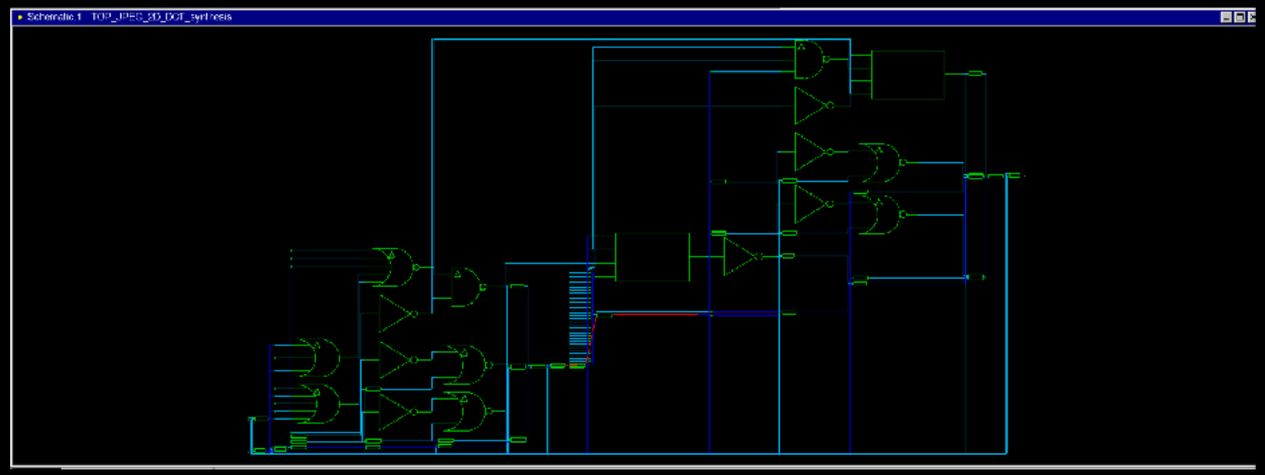



12 bit

Output
Memory

# TP_MEM BitWidth Modification

## Synthesis Results



Combinational area: 1032785.803139
Noncombinational area: 1438873.545822
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 2471659.250000

Cell Internal Power = 66.5028 mW (91%)
Net Switching Power = 6.8448 mW (9%)

---

Total Dynamic Power = 73.3476 mW (100%)

# TP_MEM BitWidth Modification

## Synthesis Results

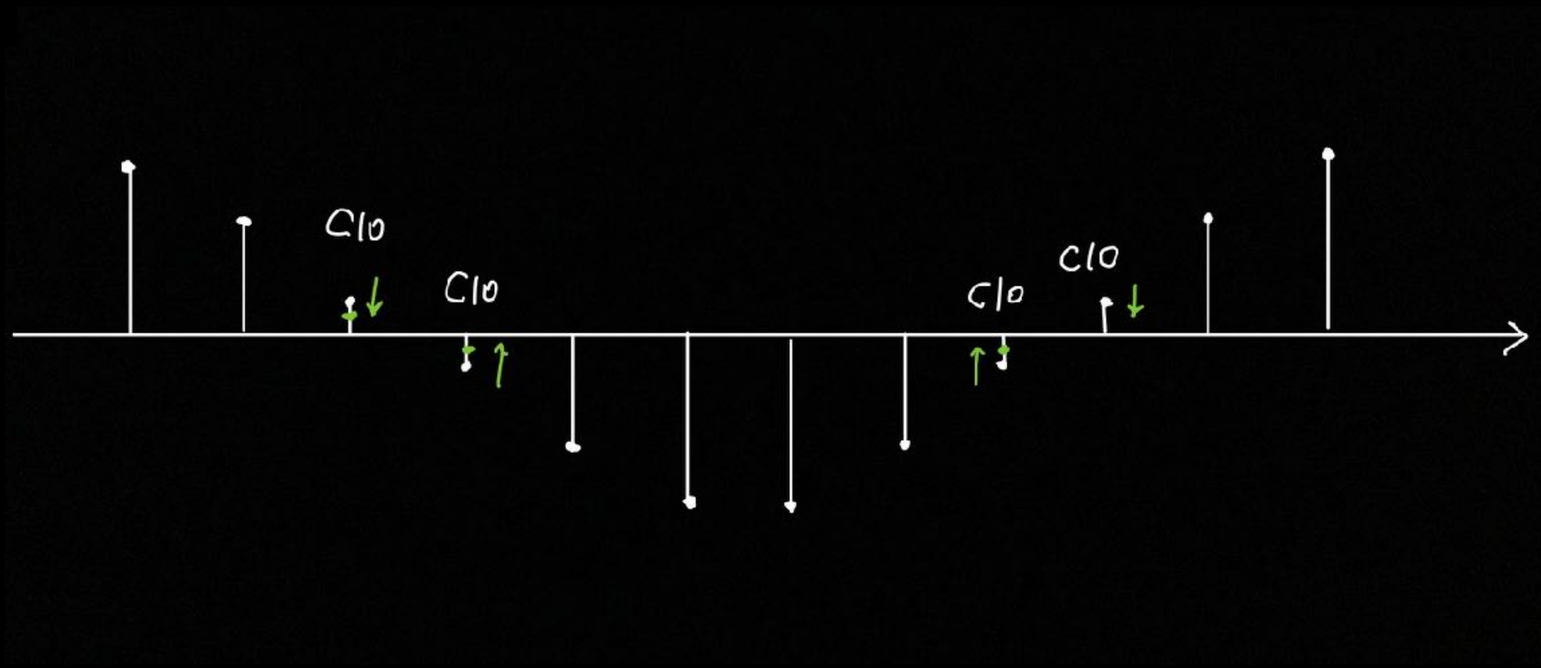
Total cell area: 2471659.250000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 254339 |
| DCT_second_stage | 421764 |
| tp_memory_1_top | 342704 |
| tp_memory_1_down | 343292 |
| tp_memory_2_top | 457033 |
| tp_memory_2_down | 456186 |

# Coefficient Quantization with Frequency basis

## Ver 7.

3) $C_2$ $C_6$ $C_{10}$ $-C_{10}$ $-C_6$ $-C_2$ $-C_2$ $-C_6$ $-C_{10}$ $C_{10}$ $C_6$ $C_2$




```
// coefficient original
parameter signed c0 = 8'h34;
parameter signed c1 = 8'h30;        // 34 to 30
parameter signed c2 = 8'h32;
parameter signed c3 = 8'h30;
parameter signed c4 = 8'h2d;
parameter signed c5 = 8'h30;        // 29 to 30

parameter signed c6 = 8'h25;
parameter signed c7 = 8'h20;
parameter signed c8 = 8'h1a;
parameter signed c9 = 8'h18;        // 14 to 18
parameter signed c10 = 8'h09;       // 0e to 09
parameter signed c11 = 8'h06;       // 07 to 06
parameter signed c12 = 8'h00;
```

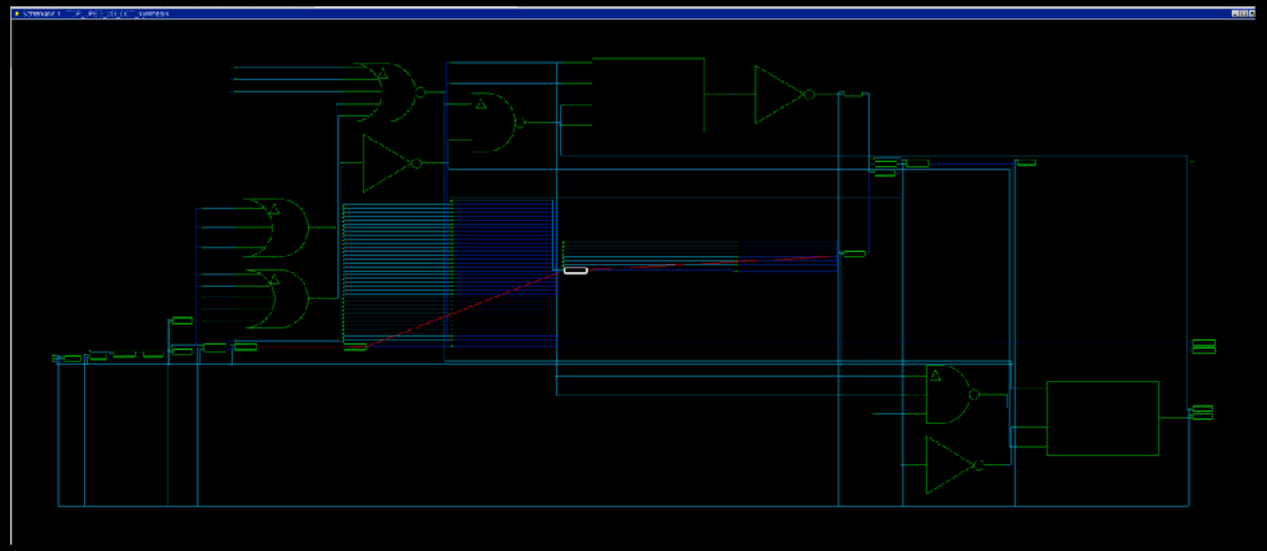
C10 : 8'b0e → 8'b09

PNSR >= 30

C10의 변화가 adder shifter의 개수를 줄여줌

# Coefficient Quantization with Frequency basis

## Synthesis Results



```
Combinational area:          863372.584072
Noncombinational area:       1438508.594666
Net Interconnect area:       undefined  (No wire load specified)
---------------------------------------------------------------------
Total cell area:             2301881.250000


Cell Internal Power  =  64.3520 mW   (92%)
Net Switching Power  =   5.8506 mW    (8%)
---------------------------------------------------------
Total Dynamic Power    =  70.2026 mW  (100%)
```

# Coefficient Quantization with Frequency basis

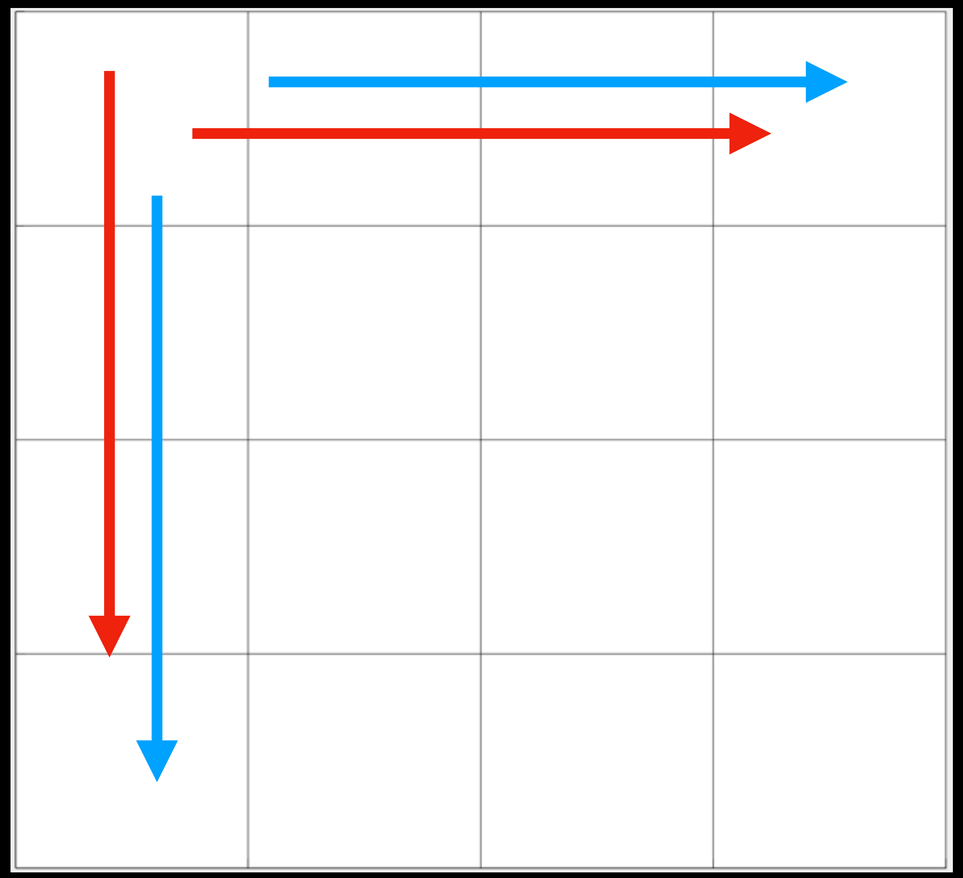
## Synthesis Results

Total cell area: 2301881.250000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 190588 |
| DCT_second_stage | 314821 |
| tp_memory_1_top | 342745 |
| tp_memory_1_down | 343359 |
| tp_memory_2_top | 457597 |
| tp_memory_2_down | 456684 |

# TP_MEM Merging (2 to 1)

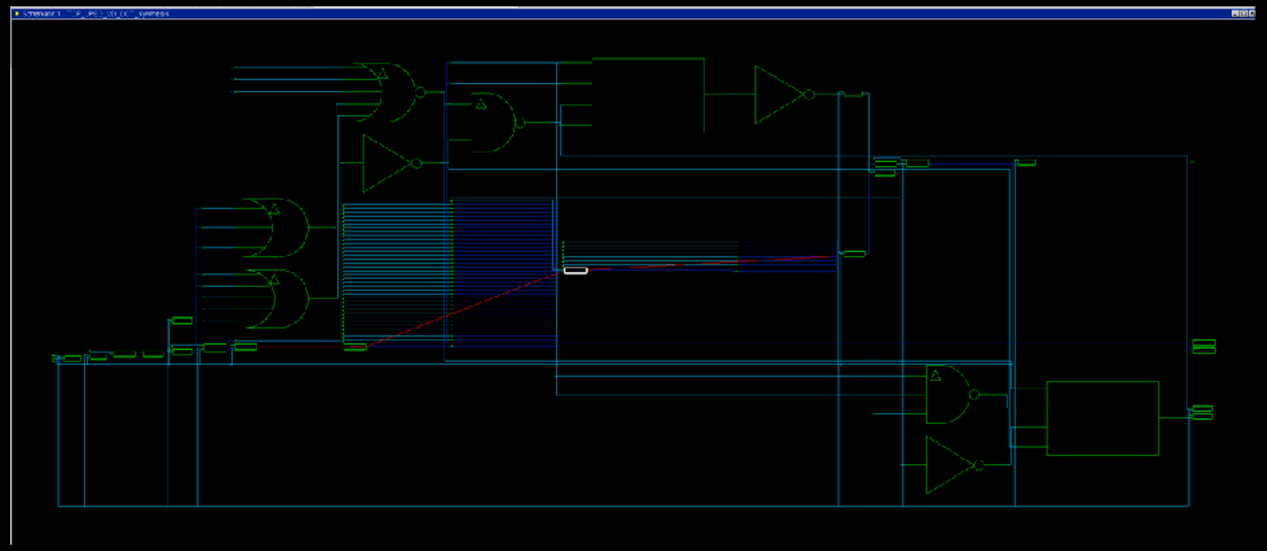
## Ver 8.



1) Row 방향으로 4행 쓰기
2) Column 방향으로 1열 읽기
3) Column 방향 1열 dff 넘어갈 때,
   앞단 dff에서 원래 row 방향으로 써야하는거 column 방향 빈칸에 쓰기
4) 다음 사이클에는 Row 방향으로 읽기

# TP_MEM Merging (2 to 1)

## Synthesis Results



Combinational area: 982024.576344
Noncombinational area: 802077.497498
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 1784102.125000

Cell Internal Power = 43.9568 mW (87%)
Net Switching Power = 6.8168 mW (13%)

---

Total Dynamic Power = 50.7736 mW (100%)

# TP_MEM Merging (2 to 1)

## Synthesis Results

Total cell area: 1784102.125000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 192363 |
| DCT_second_stage | 318677 |
| tp_memory_1 | 471420 |
| tp_memory_2 | 636736 |

# Remaining Optimization

## Final

A. Deleting Internal DFFs

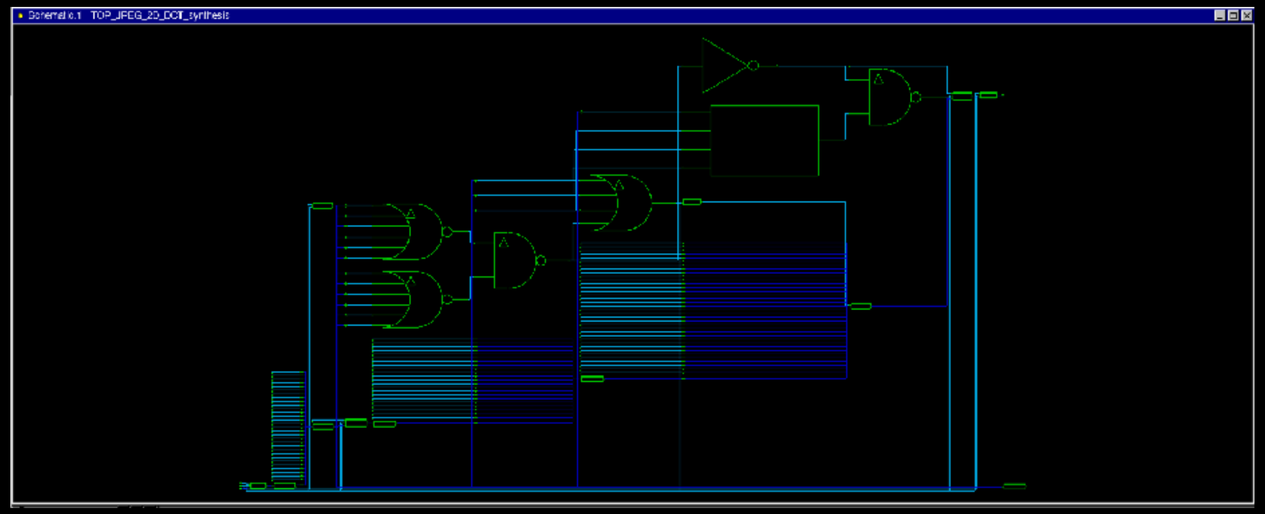
B. Sign extension Muxing removing (making DCT seperated)

C. DCT2 Works with BW=9 → 3’b000 is added after DCT2

D. Pin controll within counter 16bit

# Remaining Optimization

## Synthesis Results



Combinational area: 918795.763302
Noncombinational area: 688361.828934
Net Interconnect area: undefined (No wire load specified)

---

Total cell area: 1607157.625000

Cell Internal Power = 45.7402 mW (79%)
Net Switching Power = 11.9728 mW (21%)

---

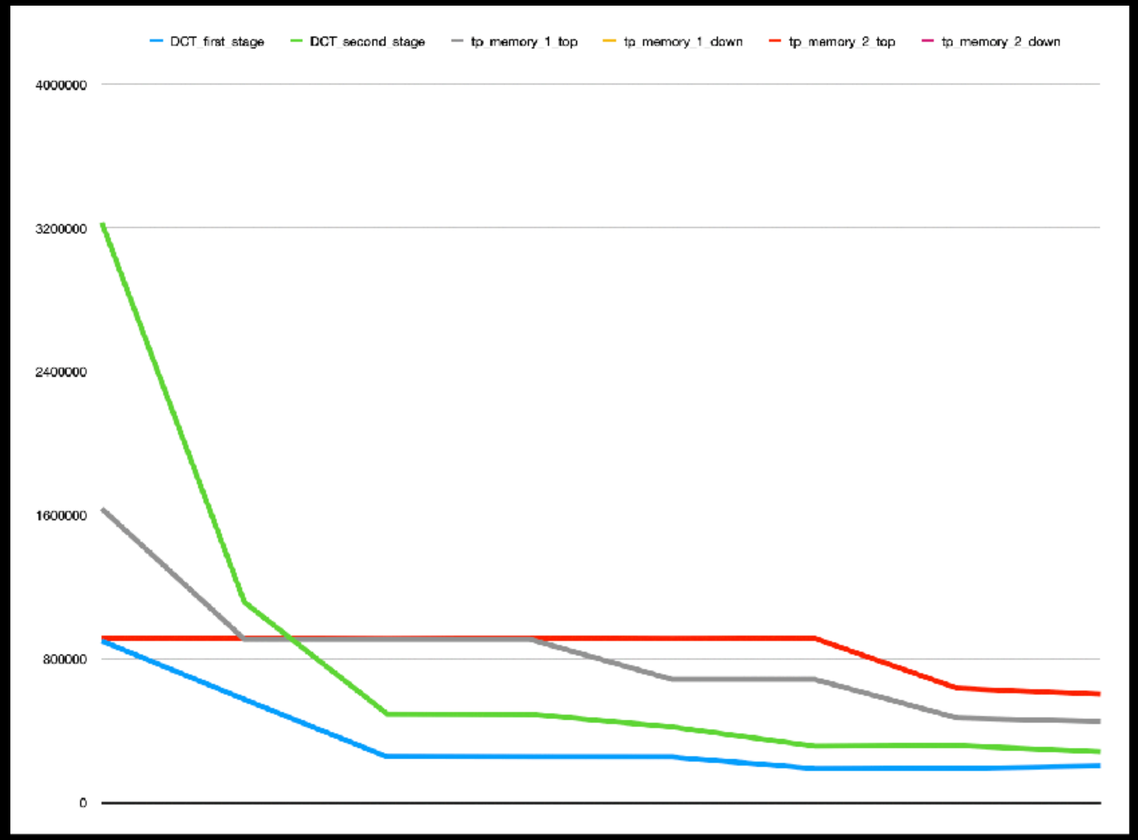
Total Dynamic Power = 57.7131 mW (100%)

# Remaining Optimization

## Synthesis Results

Total cell area: 1607157.625000

| Module | Global Cell Area |
|---|---|
| DCT_first_stage | 204174 |
| DCT_second_stage | 283267 |
| tp_memory_1 | 453243 |
| tp_memory_2 | 603389 |



# PSNR


Original image #1
size : 480x480
Restored image #1
PSNR : 3.125122e+01
Original image #2
size : 480x480
Restored image #2
PSNR : 3.281301e+01
Original image #3
size : 480x480
Restored image #3
PSNR : 3.345518e+01
Original image #4
size : 480x480
Restored image #4
PSNR : 3.343614e+01
Original image #5
size : 480x480
Restored image #5
PSNR : 3.035567e+01
Original image #6
size : 480x480
Restored image #6
PSNR : 3.375567e+01
Original image #7
size : 480x480
Restored image #7
PSNR : 3.234799e+01
Original image #8
size : 480x480
Restored image #8
PSNR : 3.393061e+01

# Timing Diagram

```
                                                    0.44       9.83 f
DCT_first_stage/z10_shifter_adder/add_0_root_add_24_3/U1_15/OUTC (fadd1s3)
                                                    0.38      10.21 f
DCT_first_stage/z10_shifter_adder/add_0_root_add_24_3/U1_16/OUTC (fadd1s3)
                                                    0.38      10.59 f
DCT_first_stage/z10_shifter_adder/add_0_root_add_24_3/U1_17/OUTS (fadd1s3)
                                                    0.84      11.43 r
DCT_first_stage/z10_shifter_adder/add_0_root_add_24_3/SUM[17] (c2_c6_C10_sa_1_DW01_add_2)
                                                    0.00      11.43 r
DCT_first_stage/z10_shifter_adder/out[17] (c2_c6_C10_sa_1)
                                                    0.00      11.43 r
DCT_first_stage/dct_out[37] (DCT_1d_first)          0.00      11.43 r
internal_BW_maker/in[37] (BW_maker)                 0.00      11.43 r
internal_BW_maker/out[16] (BW_maker)                0.00      11.43 r
tp_memory_1/i_data[16] (TP_MEM_mreged_BW9)          0.00      11.43 r
tp_memory_1/U2757/Q (nnd2s3)                        0.14      11.57 f
tp_memory_1/U90/Q (nb1s4)                           0.26      11.83 f
tp_memory_1/U2015/Q (nnd2s2)                        0.17      12.01 r
tp_memory_1/array_reg[10][7]/DIN (dffles1)          0.00      12.01 r
data arrival time                                             12.01

clock clk (rise edge)                              12.50      12.50
clock network delay (ideal)                         0.00      12.50
tp_memory_1/array_reg[10][7]/CLK (dffles1)          0.00      12.50 r
library setup time                                 -0.49      12.01
data required time                                            12.01
--------------------------------------------------------------------------
data required time                                            12.01
data arrival time                                            -12.01
--------------------------------------------------------------------------
slack (MET)                                                   0.00
```

# Afterward

A. Overflow Checker Modification → Based on DCT matrix Frequency

B. More quantization Methods → {0, 1, 2}