Generate States.

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May 23, 2023

There is some magic hides in the You right that if the amplitudes depends on the number of the qubits, then there is

1 Equivalence to Fusion-controlled gates problem.

1.1 Stage (1) - Fusion-controlled circuit.

For a circuit, U denotes by U^c, the controlled version of it. Define the fusion-controlled gate to be the circuit

$$(U \otimes V)^c : 0^\Delta \otimes 0^U \otimes 0^V \rightarrow \begin{cases} 00^{\Delta-1}U0^U0^V & x_0 = 0 \\ 10^{\Delta-1}0^UV0^V & else \end{cases}$$

We first show that given U^c, V^c one can implement at the same depth cost the circuit $(U \otimes V)^c$

1.2 stage (2) - Induction.

Assume that for any set of given 2^{n-1} amplitudes encoding a state ψ there is a $\log(n-1)$ circuit $U_\psi^{(n-1)}$ that generate ψ. Recall that any state in a n-dimisional space could be write as $\psi = \alpha_0 0\psi_0 + \alpha_1 1\psi_1$. By the assumption there are $U_{\psi_0}^{(n-1)}, U_{\psi_1}^{(n-1)}$ circuits each at depth at most $\log n$ generate ψ_0 and ψ_1 corespondly. We are going to construct a circuit that computes ψ by the following:

1. Prepare $2 \times S_{n-1} + 1$ anciles. And arrange them by $S_{n-1}\ |0|\ S_{n-1}$.
2. Rotate the middle qubit as follow: $0 \mapsto \alpha_0 0 + \alpha_1 1$.
3. Apply $\left(U_{\psi_0}^{(n-1)} \otimes U_{\psi_1}^{(n-1)}\right)^c$ to have
$$\alpha_0 00^{\Delta-1}U_{\psi_0}^{(n-1)}0^{(n-1)}0^{(n-1)} + \alpha_1 10^{(\Delta-1)}0^{(n-1)}U_{\psi_1}^{(n-1)}0^{(n-1)}$$
4. Now apply control swap, use the Δth qubit as the control wire and swap between S_0,S_1. That yields the state:
$$0^{\Delta-1}\left(\alpha_0 0U_{\psi_0}^{(n-1)}0^{(n-1)} + \alpha_1 1U_{\psi_1}^{(n-1)}0^{(n-1)}\right)0^{(n-1)}$$
5. By induction, the above state expanse to $\psi \otimes 0^*$.

So if we denote by $d(n), S(n)$ the depth and the space needed to compute a general state correspond to a given amplitude, It follows by the recursion that:

$$S(n) = T_S[S(n-1)]$$

$$d(n) = T_d[d(n-1)] + \overbrace{1}^{\text{rotation}} + \overbrace{n-1}^{\text{swap}} = T_d[d(n-1)] + n$$

2 First Soultion $\times 4$ Space.

1. Prapere $+2$ qubits.
2. Apply CX from the first qubit to the second.
3. Apply U^c negative-controlled by the first qubit over the first S_u qubits, and in parallel apply V^c controlled by the second qubit over the S_v quibtis.
4. Apply CX from the first qubit to the second. (reverse step 2).

Clearly $T_S[S(n)] = 2 \cdot S(n) + 2$ and $T_d[d(n)] = 1 + d(n) + 1$ And that sumup to:

$$S(n) = T_S[S(n-1)] = 2T_S[S(n-2)] + 2$$

$$= 2 \cdot 2^{n-1} ... + 2 \cdot 2^2 + 2 \cdot 2 + 2$$

$$= 2 \cdot 2^n$$

$$d(n) = T_d[d(n-1)] + \overbrace{1}^{\text{rotation}} + \overbrace{n-1}^{\text{swap}} = T_d[d(n-1)] + n$$

3 Second Solution $\times 2$ Space.

3.1 Stage (1) - Fusion-controlled circuit.

For a circuit, U denotes by U^c, the controlled version of it. We first show that given U^c, V^c one can implement at the same depth cost the circuit $(U \otimes V)^c$. It's well known that U^c could be obtained by U by adding single qubits gates on U wires and connecting Cnot gates from the control wire to U wires. Notice that for running $(V \otimes U)^c$ it's sufficient to handle the Conts as each of the single qubits gates operate independently in parallel. Consider the following recipe:

On the ith iteration of the circuits,

1. If there is no conflict between U^c and V^c, meaning that either only one of them uses the control wire at that step or that neither of them, then $(U \otimes V)^c_t \leftarrow U^c_t \otimes V^c_t$
2. Else, at the i step the controlled wire flow for both of them, So denote by x_c, x_v, x_u the tree bits such at time t

4 Third Solution T.C.S Approach.