Shane Duffy
ECE-363 Lab 1

Supplemental Work

PART 2: Seq. Logic Design.

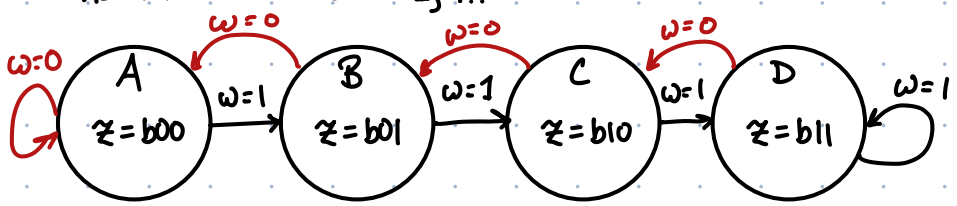
Step 1: DFF → TODO: Output Log

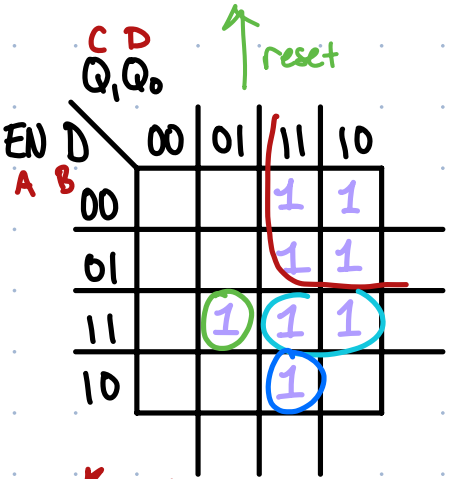
Step 2: FSM DIAGRAM

SOME OUTPUT $z = \{b00, b01, b10, b11\}$

SOME INPUT $w = \{0, 1\}$

ASSUMING ENABLE = 1; ...



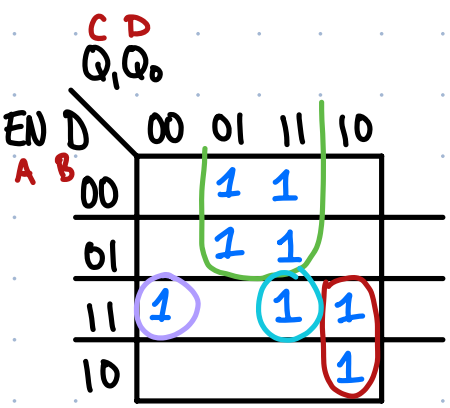


STATE TABLE:

PS ($Q_1 Q_0$)	NS en=0 d=x ($Q_1^* Q_0^*$)	NS en=1 d=0 ($Q_1^* Q_0^*$)	NS en=1 d=1 ($Q_1^* Q_0^*$)	OUT
00	00	00	01	00
01	01	00	10	01
10	10	01	11	10
11	11	10	11	11

$Q_1^* = A'C + ABC + ABC'D + AB'CD$

$Q_1^* = E'Q_1 + EDQ_1 + ABQ_1'Q_0 + ED'Q_1Q_0$



$Q_0^* = A'D + AC'D' + ABC'D' + ABCD$

$Q_0^* = E'Q_0 + EQ_1'Q_0' + EDQ_1'Q_0' + EDQQ_0$

STATE TABLE:

	NS			
PS	en=0 d=X	en=1 d=0	en=1 d=1	OUT
00	00	00	01	00
01	01	00	10	01
10	10	01	11	10
11	11	10	11	11
$Q_1 Q_0$	$Q_1^* Q_0^*$	$Q_1^* Q_0^*$	$Q_1^* Q_0^*$	$O_1 O_0$

$O_1 = Q_1$ //

$O_2 = Q_2$