FPGA Based Feedforward System for Photonic Simulation and Quantum Computing Applications

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This document has answers to some questions contained in chapter 3 of the book RTL Hardware Design Using VHDL by Pong P. Chu. [1].

A 3.1

```
library ieee;
use ieee.std_logic_1664.all;
use ieee.numeric_std.all;

entity mem_cir is
port (
  addr : in std_logic_vector(11 downto 0);
  wr_n : in std_logic;
  oe_n : out std_logic;
  data : inout std_logic_vector(8 downto 0)
);
```

References

[1] P. P. Chu, RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability. Hoboken, NJ: Wiley-Interscience, 2006.