Designing 5V Tolerant PRISM® PCMCIA Radio Cards

Application Note | March 2002 | AN9980.1

Background

The specification issued by the PCMCIA consortium officially recognizes 3V-only cards. Such a device is recognized by unique mechanical keying and voltage strapping on the 68- pin PCMCIA interface connector and by a special entry in the Card Information Structure (CIS) file read by Microsoft® Windows®. Intersil's 3V reference designs include the PRISM® II HWB3163 and PRISM 2.5 ISL37300P radio cards. Additionally, the PRISM 3 ISL37101P reference design is soon to be released. According to the PCMCIA specification, such 3V-only cards should only be powered by 3.3 ± 0.3 VDC under all circumstances. Intersil's reference designs are compliant with this specification and therefore function properly under these conditions.

All computers that support PCMCIA cards incorporate PC interface controllers (PCIC) for the card's electrical interface. With the specific electrical interface and low voltage mechanical keying used on Intersil's PCMCIA cards, the PCIC must initially apply 3.3V. All of the above information is clearly and unambiguously stated in the PCMCIA specification. Note that the low-voltage keying prevents insertion of the cards in older laptops which do not support 3.3V operation.

Unfortunately, there are some systems in the marketplace (laptop/notebook PCs with Windows OS) that do not comply with the PCMCIA Specification. These systems initially apply 5V to any PC card, even cards that are low-voltage keyed and electrically configured for 3V. This non-compliance to the PC card specification forces PC card manufacturers who want to support these systems into the unfortunate position of having to tolerate the errant initial application of 5V.

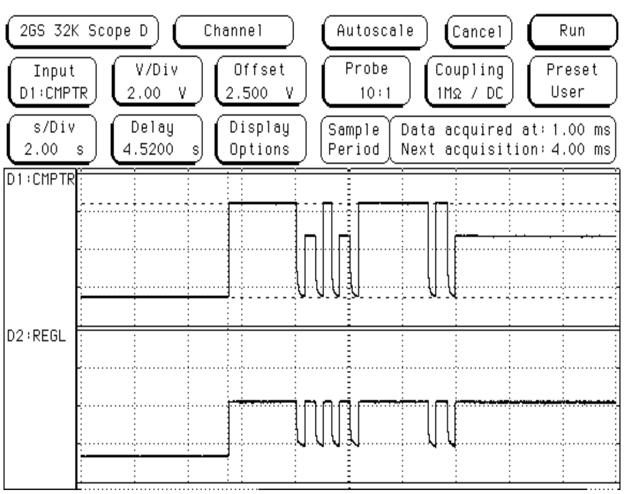

FIGURE 1. TYPICAL VOLTAGE TRANSIENT ON BOOTING COMPUTER

This overvoltage condition is captured in the upper trace of Figure 1. This data was measured in a new laptop computer while powering an ISL37101P PRISM 3 PCMCIA assembly. Note, in the upper trace, that the computer initially applies 5V to the card, followed by several transitions between 0V, 3.3V and 5V and finally settling at 3.3V. Furthermore, the power bus takes approximately eight seconds to stabilize!

In the past, the incidence of non-compliant laptop computers was very low. Recently, however, some major brands are appearing on the market with this 5V transient. To better support our customers, Intersil has opted to modify its designs to make them capable of correctly handling the 5V transients, i.e. 5V tolerant.

General

Intersil currently supports PCMCIA reference designs utilizing three different chipsets.

TABLE 1. INTERSIL PCMCIA REFERENCE RADIOS

Chipset	Radio Model
PRISM II	HWB3163
PRISM 2.5	ISL37300P
PRISM 3	ISL37101P

This application note discusses solutions applicable to all three radios. Details, however, vary slightly depending on the specific radio model.

In order to make a radio 5V tolerant, a 2.84V low dropout voltage regulator (LDO) is added in series with the digital power bus feeding the Medium Access Controller (MAC), Baseband Processor (BBP) (or Combo chip, if these two are combined), SRAM and Flash (or EEPROM). Additionally, on the ISL37300P and HWB3163 designs, the analog power supply pins on the BBP or Combo chip must also be fed from this LDO. These Intersil PRISM devices are all rated for operation down to 2.7 VDC. The various RF power amplifiers used in these chipsets are designed to be able to withstand 5V as long as they remain disabled. This requires that the amplifier's power enable pin (PE) remain low during this transient period. All other power buses used in the designs are already fed through separate voltage regulators so need not be routed through the LDO. The net result is that radio performance will not be affected by these changes. The effect of adding this LDO may be seen in the lower trace of Figure 1. Clearly, this regulator clips the voltage transient and ensures proper operation of the card. The selection of the LDO is critical. Special attention needs to be paid to the minimum guaranteed output voltage under load conditions.

Detailed circuit changes for each of the radios are discussed in the following sections. The reference designs for the

ISL37300P and ISL37101P radios will be officially revised to incorporate 5V tolerance and Intersil reference design customers are encouraged to periodically check the Premier Website for these upgrades. Recommended changes to the HWB3163 design are presented below, however the reference design will not be officially revised since it is a more mature design. Nevertheless, Intersil customers are encouraged to incorporate this upgrade.

Changes to the ISL37101P Radio

As noted in the *General* section above, a MAXIM MAX8867EUK29 (or MAX8867EZK29) 2.84V LDO Voltage Regulator, U6, was added in series with the power bus supplying the IO_VDDD and COREVDDD pins to the ISL3871 COMBO Chip (U5) as well as the Vcc pins to the SRAM (U1), FLASH (U2) and EEPROM (U9) memories. The EZK regulator is a lower profile version of the EUK device and they are otherwise identical. The complete reference design is available on Intersil's Premier Web site. These devices are all rated for operation down to 2.7 VDC so no effect on radio performance occurs. The analog voltage pins to the ISL3871 chip are fed from the regulated VCCA 2.84V bus on previous ISL37101P designs so no change is necessary here.

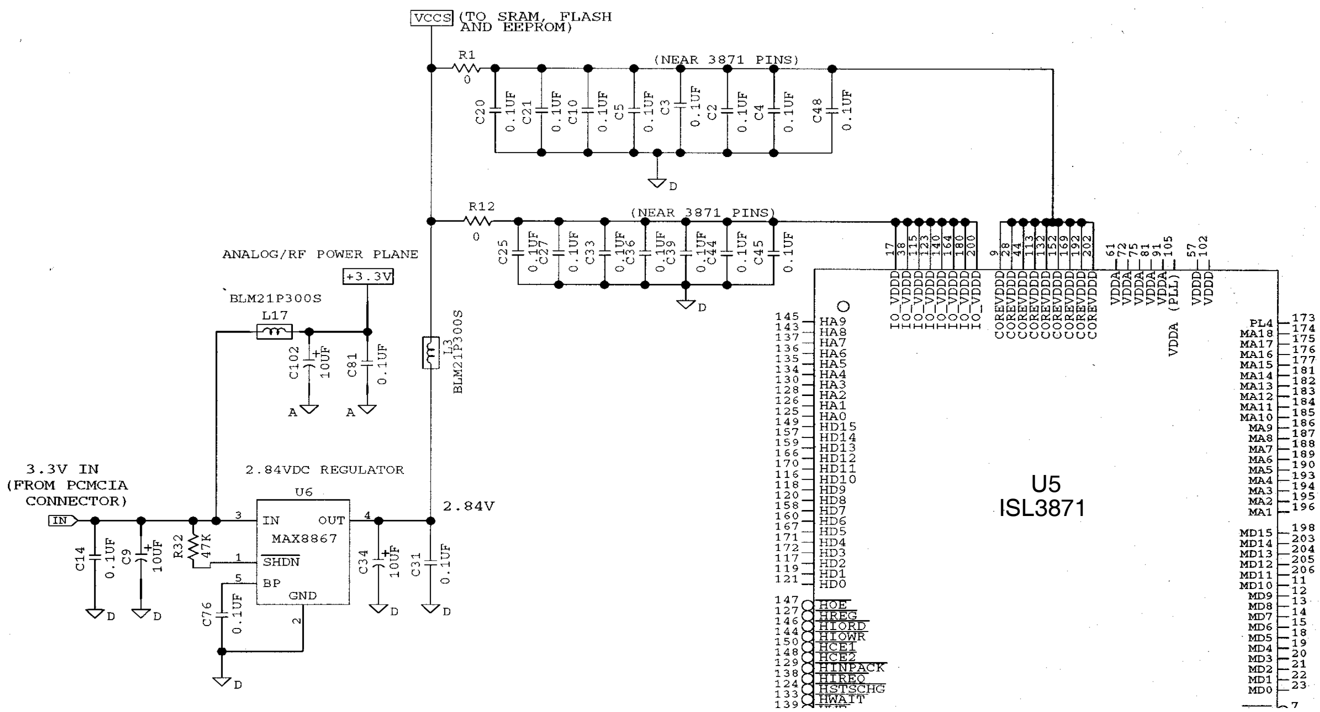

FIGURE 2. CHANGES TO ISL37101P PRISM 3 PCMCIA RADIO

Changes to the ISL37300P Radio

A change similar to that noted in the radio above was added here. However, since the LDO regulator must support the additional current drawn by the analog section of the ISL3873 Combo chip, U4 (approximately 30ma), a single MAX8867 regulator was not deemed adequate. Note that the LDO must deliver a minimum of 2.7 VDC to the Combo chip and memories, even at the low end of the input supply rail specification, 3.0V.

An extensive study of other LDO regulators from a variety of manufacturers was conducted. Interestingly, even LDO regulators rated for substantially higher currents did not provide guarranteed lower voltage drop under worst case conditions compared to the MAX8867. Also, the higher current LDO regulators were significantly higher priced.

The problem was solved by employing two MAX8867EUK29 or MAX8867EZK29 regulators with their inputs and outputs connected in parallel. These regulators utilize a P-Channel MOSFET for the pass element. Under lightly loaded conditions, the regulator with the highest regulator voltage will be active. The pass element of the other regulator will be biased off by virtue of the analog voltage comparator in this unit sensing that the output voltage is too high compared to its internal voltage reference. As the current drain increases however, the output voltage of the active regulator will begin to slightly fall and a point will eventually be reached at which the second regulator will begin to supply significant output current. The EZK regulator is a lower profile version of the EUK device and they are otherwise identical.

The net effect of using two parallel LDO regulators is to essentially double the output current available at a particular differential voltage drop. This provides more than adequate drive capability.

The performance of single and paralled MAX8867 voltage regulators is shown in Figure 3 for a supply voltage of 3.0VDC. The actual circuit changes are shown in Figure 5. Consult Intersil's Premier Web site for further details.

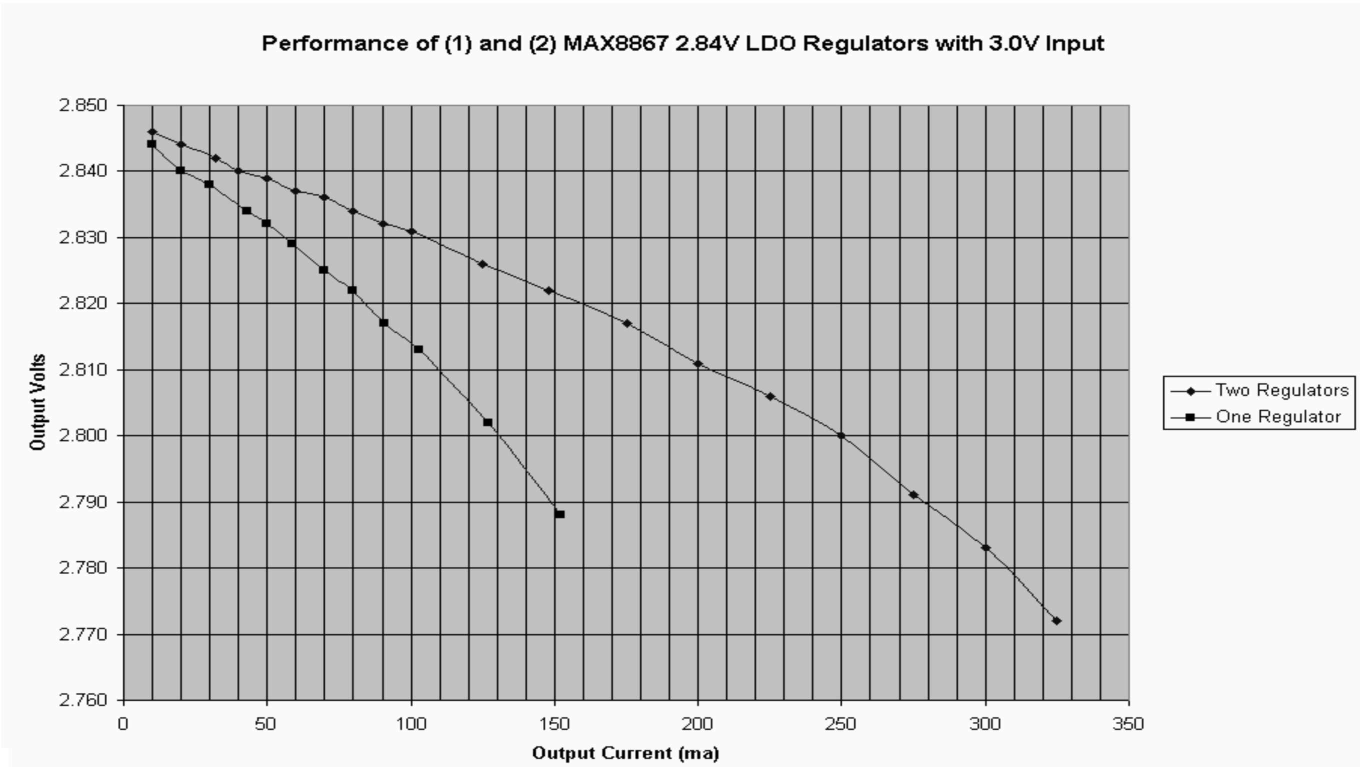

FIGURE 3. PERFORMANCE OF MAX8867 2.84V LDO REGULATORS

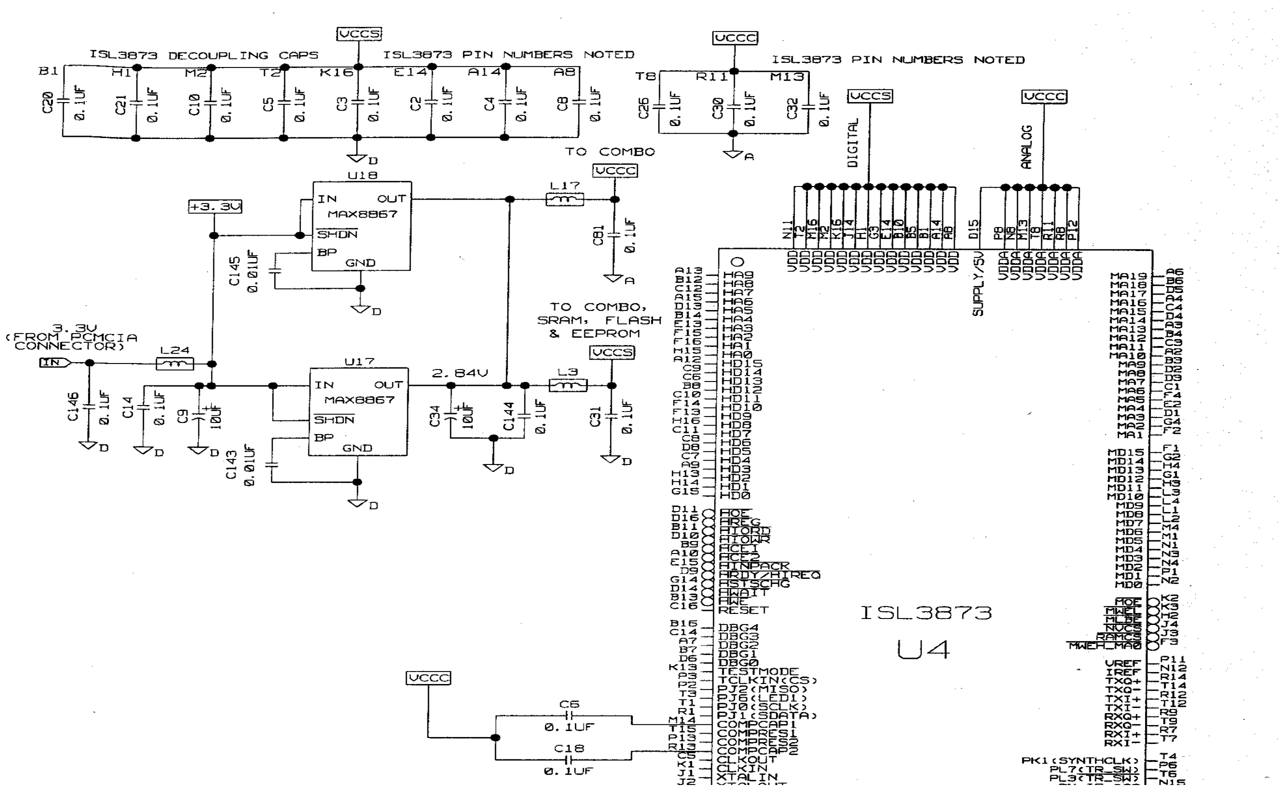

FIGURE 4. CHANGES TO ISL37300P PRISM 2.5 PCMCIA RADIO

Changes to the HWB3163 Radio

The 5V tolerant modifications to this radio are basically the same as that applied to the ISL37300P radio above with the exception that this older design uses separate BBP and MAC IC's instead of a Combo chip.

Several different combinations of BBP and MAC IC's were used in this design. These include the HFA3861A, HFA3861B and HFA3863 BBP and the HFA3841 and HFA3842 MAC. Although the design illustrated below is for the HFA3861B BBP and HFA3841 MAC, the same solution should work equally well with the other chip combinations.

Once again, the voltage feed to the MAC, FLASH, SRAM and digital pins of the BBP, i.e. the entire VCCS power bus is fed from the output of the paralleled MAX8867EUK29 (or MAX8867EZK29) LDO regulators. Additionally, the voltage for the analog pins of the BBP, formerly fed from the 3.3V bus is now fed from a new 2.84V bus labeled VCCD on the diagram in Figure 5 (next page). VCCD is derived from the output of the LDO regulator through separate decoupling components in order to properly isolate the analog and digital power buses.

CAUTION: Microsoft Windows 2000 Service Pack 3 (SP3) must be installed by users who have field-installed the Windows 2000 operating system on their laptop computers. If SP3 is not installed, some PCMCIA Controllers apply a 5V supply during operation to 3V PCMCIA cards instead of switching to 3.3V. Failure to install SP3 may result in permanent damage to Intersil's line of 3V PCMCIA radio cards.

If, however, Windows 2000 was factory-installed by the laptop manufacturer, this condition will probably not occur. If in doubt, check with the manufacturer.

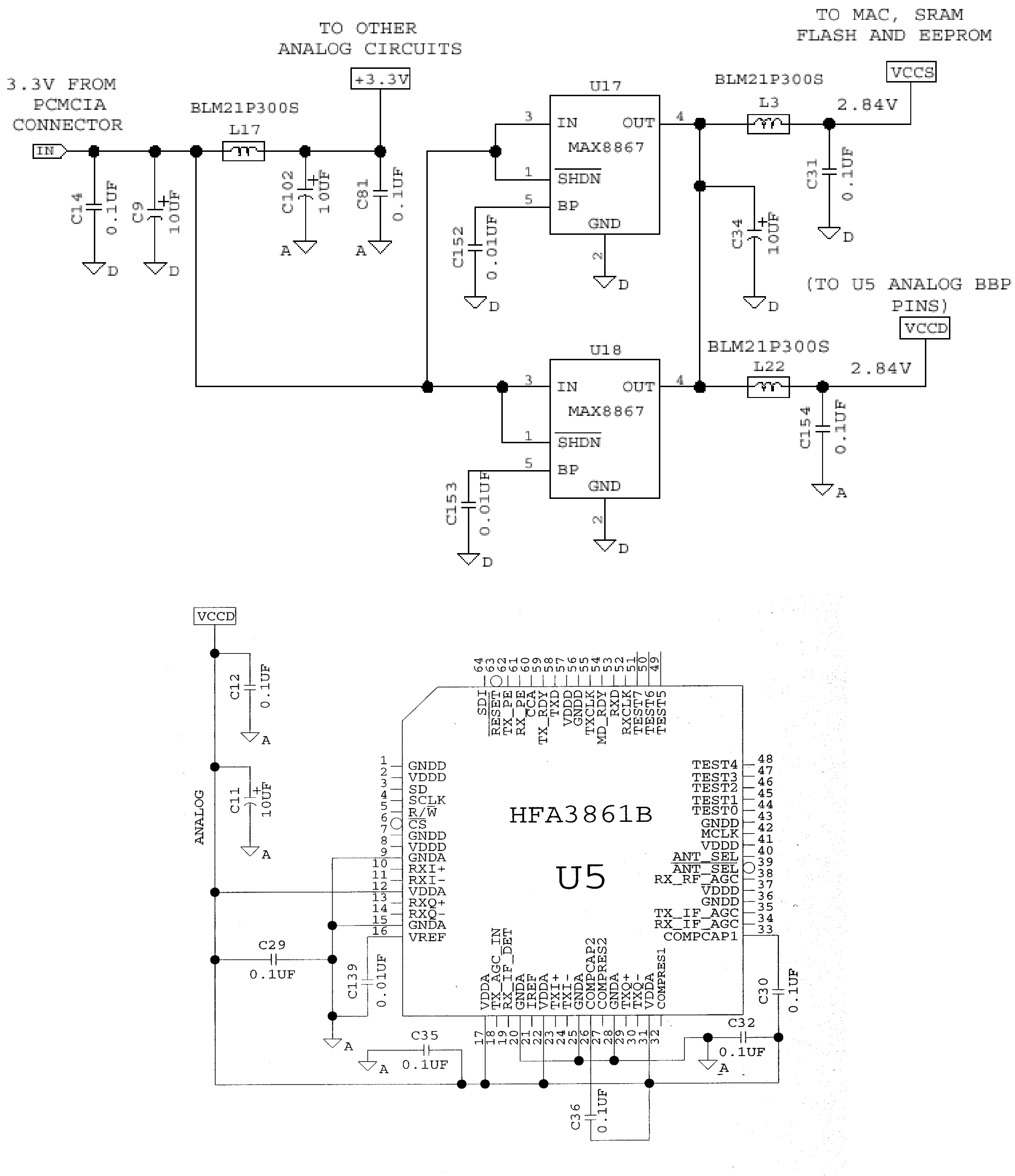

FIGURE 5. CHANGES TO THE HWB3163 PRISM II PCMCIA RADIO

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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
7585 Irvine Center Drive
Suite 100
Irvine, CA 92618
TEL: (949) 341-7000
FAX: (949) 341-7123

Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7946

EUROPE
Intersil Europe Sarl
Ave. William Graisse, 3
1006 Lausanne
Switzerland
TEL: +41 21 6140560
FAX: +41 21 6140579

ASIA
Intersil Corporation
Unit 1804 18/F Guangdong Water Building
83 Austin Road
TST, Kowloon Hong Kong
TEL: +852 2723 6339
FAX: +852 2730 1433