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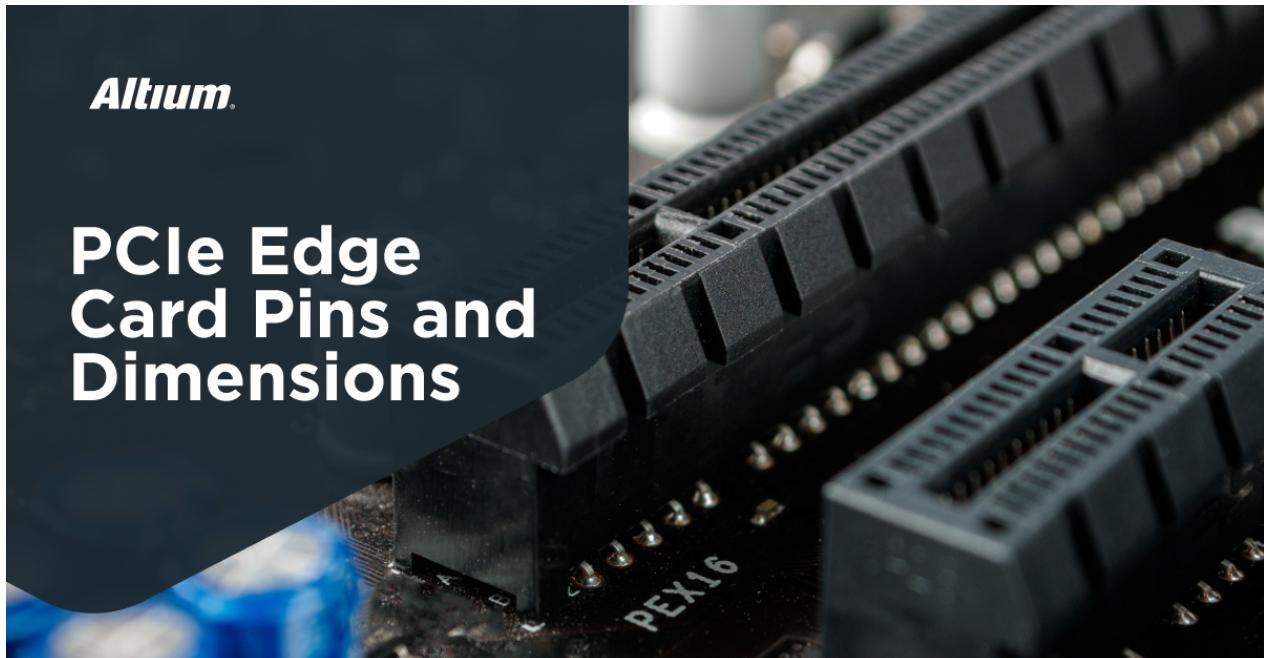
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Learning Hub High-Speed Design PCB Design and Pinout For PCIe Edge Cards

PCB Design and Pinout For PCIe Edge Cards



Zachariah Peterson | Created: July 13, 2024 | Updated: July 17, 2025



The most common add-in card in standard desktop computers and embedded computers is the PCIe card. PCIe add-in cards come in multiple form factors and use an edge slot connector, mounting either vertically or at a right angle along a motherboard. You also have different types of PCIe devices, such as SSDs or modules that plug into an M.2 connector.

In this article, I'll cover the mechanical and electrical requirements for PCIe add-in cards that use the standard vertical edge connector typically found in desktop computers or servers. PCIe add-in cards have specific mechanical specifications for card shape and size that must be followed to fit snugly within an edge connector.

Unfortunately, the mechanical specifications for these edge connectors are buried in the PCIe standard. Designers often have to reverse-engineer an existing card outline to use it in a PCIe card PCB. In this blog, I've created a PCIe card template that you can use for your projects. This template is a good starting point, as it shows the mechanical keying and pin requirements for the card, but

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How to Design a PCIe Edge Card | Altium Designer Tips



PCIe Card Mechanical and Electrical Requirements

PCIe add-in cards use a PCIe slot connector that imposes mechanical constraints and determines signal integrity. Below are some important considerations for PCIe slot connectors used in these cards:

- **Lane Standardization:** Slot connectors are standardized for a specific number of lanes (1x, 4x, 8x, 16x, and the less commonly used 32x).
- **Generation Compatibility:** Slot connectors are rated for specific PCIe generations and are backward compatible.
- **Component Types:** Slot connectors can be through-hole components or SMD components, though newer generation connectors tend to be SMD.
- **Expanded Connectors:** A larger slot connector can accommodate smaller add-in cards if required by the design.
- **Keying and Orientation:** Slot connectors are keyed to determine the orientation of the PCIe card during installation. This keying must be included in the add-in card.

PCIe add-in cards typically have a flange that attaches to the card, allowing it to sit against the chassis of a computer. This flange limits the dimensions of standard PCIe add-in cards.

Example PCIe Slot Connectors

Some example slot connectors are shown below. Anyone who has opened up a desktop computer or server will recognize these edge connectors. The connectors shown are available from Samtec, although other vendors like Amphenol provide their own edge connectors.



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8-lane (top) and 16-lane (bottom) PCIe edge connectors (Amphenol)

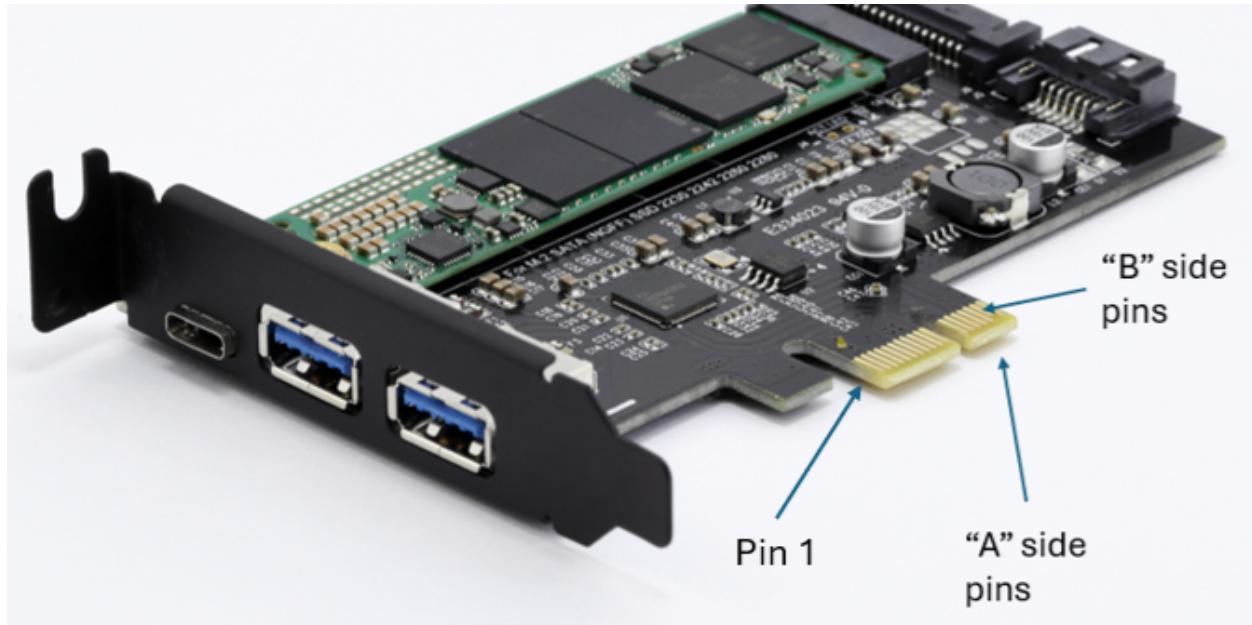
Given the size and placement of the edge connector and the card flanges, mechanical modeling is usually necessary to verify the form and fit within the enclosure. For newer generations of PCIe, SI simulations are also required to verify channel bandwidth and total losses. Beyond these considerations, designers must construct the card pinout to accommodate the required number of lanes.

Number of Lanes in the PCIe Card Pinout

The card pinout in a PCIe connector depends on the number of lanes and includes additional interfaces, such as [JTAG](#). There are also power ports and numerous ground pins distributed across the card edge. The pins have a 1.0 mm pitch, with PCIe RX and TX lanes interleaved with ground pins.

All PCIe edge card pinouts have an A-side and a B-side. These sides are labeled and shown in the image below.

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The pinouts for PCIe cards are detailed in tables. As the number of lanes increases, new sections are added to the pinout tables.

1x Lanes

Pin #	B-side Name	Function	A-side Name	Function
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS

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10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PERST#	PCI-Express Reset signal
Mechanical Key	N/A	N/A	N/A	N/A
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference CLK (+)
14	TX0_P	TX Lane 0 (+)	REFCLK-	Reference CLK (-)
15	TX0_N	TX Lane 0 (-)	GND	Ground
16	GND	Ground	RX0_P	RX Lane 0 (+)
17	PRSNT#2	Hotplug detect	RX0_N	RX Lane 0 (-)
18	GND	Ground	GND	Ground

4x Lanes

Pin #	B-side Name	Function	A-side Name	Function
19	TX1_P	TX Lane 1 (+)	RSVD	Reserved
20	TX1_N	TX Lane 1 (-)	GND	Ground
21	GND	Ground	RX1_P	RX Lane 1 (+)
22	GND	Ground	RX1_N	RX Lane 1 (-)
23	TX2_P	TX Lane 2 (+)	GND	Ground



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25	GND	Ground	RX2_P	RX Lane 2 (+)
26	GND	Ground	RX2_N	RX Lane 2 (-)
27	TX3_P	TX Lane 3 (+)	GND	Ground
28	TX3_N	TX Lane 3 (-)	GND	Ground
29	GND	Ground	RX3_P	RX Lane 3 (+)
30	RSVD	Reserved	RX3_N	RX Lane 3 (-)
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved

8x Lanes

Pin #	B-side Name	Function	A-side Name	Function
33	TX4_P	TX Lane 4 (+)	RSVD	Reserved
34	TX4_N	TX Lane 4 (-)	GND	Ground
35	GND	Ground	RX4_P	RX Lane 4 (+)
36	GND	Ground	RX4_N	RX Lane 4 (-)
37	TX5_P	TX Lane 5 (+)	GND	Ground
38	TX5_N	TX Lane 5 (-)	GND	Ground
39	GND	Ground	RX5_P	RX Lane 5 (+)
40	GND	Ground	RX5_N	RX Lane 5 (-)

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42	TX6_N	TX Lane 6 (-)	GND	Ground
43	GND	Ground	RX6_P	RX Lane 6 (+)
44	GND	Ground	RX6_N	RX Lane 6 (-)
45	TX7_P	TX Lane 7 (+)	GND	Ground
46	TX7_N	TX Lane 7 (-)	GND	Ground
47	GND	Ground	RX7_P	RX Lane 7 (+)
48	PRSNT#2	Hot plug detect	RX7_N	RX Lane 7 (-)
49	GND	Ground	GND	Ground

16x Lanes

Pin #	B-side Name	Function	A-side Name	Function
50	TX8_P	TX Lane 8 (+)	RSVD	Reserved
51	TX8_N	TX Lane 8 (-)	GND	Ground
52	GND	Ground	RX8_P	RX Lane 8 (+)
53	GND	Ground	RX8_N	RX Lane 8 (-)
54	TX9_P	TX Lane 9 (+)	GND	Ground
55	TX9_N	TX Lane 9 (-)	GND	Ground
56	GND	Ground	RX9_P	RX Lane 9 (+)
57	GND	Ground	RX9_N	RX Lane 9 (-)

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59	TX10_N	TX Lane 10 (-)	GND	Ground
60	GND	Ground	RX10_P	RX Lane 10 (+)
61	GND	Ground	RX10_N	RX Lane 10 (-)
62	TX11_P	TX Lane 11 (+)	GND	Ground
63	TX11_N	TX Lane 11 (-)	GND	Ground
64	GND	Ground	RX11_P	RX Lane 11 (+)
65	GND	Ground	RX11_N	RX Lane 11 (-)
66	TX12_P	TX Lane 12 (+)	GND	Ground
67	TX12_N	TX Lane 12 (-)	GND	Ground
68	GND	Ground	RX12_P	RX Lane 12 (+)
69	GND	Ground	RX12_N	RX Lane 12 (-)
70	TX13_P	TX Lane 13 (+)	GND	Ground
71	TX13_N	TX Lane 13 (-)	GND	Ground
72	GND	Ground	RX13_P	RX Lane 13 (+)
73	GND	Ground	RX13_N	RX Lane 13 (-)
74	TX14_P	TX Lane 14 (+)	GND	Ground
75	TX14_N	TX Lane 14 (-)	GND	Ground
76	GND	Ground	RX14_P	RX Lane 14 (+)
77	GND	Ground	RX14_N	RX Lane 14 (-)



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79	TX15_N	TX Lane 15 (-)	GND	Ground
80	GND	Ground	RX15_P	RX Lane 15 (+)
81	PRSNT#2	Hot plug present detect	RX15_N	RX Lane 15 (-)
82	RSVD#2	Hot Plug Detect	GND	Ground

There are some key points to note. The two power rails are at 12 V and 3.3 V; these are typically supplied off the card, so PCIe cards usually do not carry regulators for these voltages. Power regulators can be included on PCIe cards as needed. [Isolated DC-DC converters](#) are rare on PCIe cards, except in specific use cases like Power over Ethernet (PoE), which requires 54 V generated on the PCIe card.

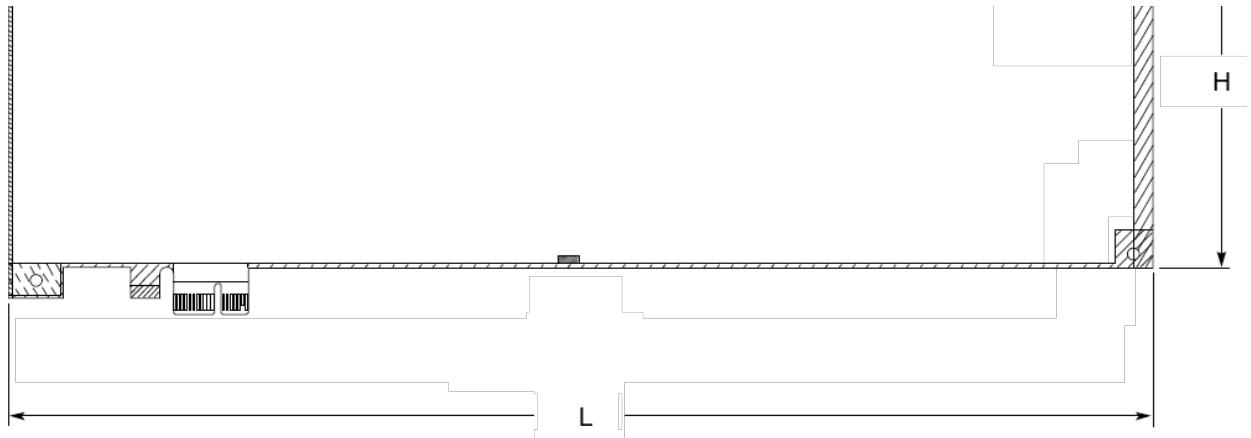
PCIe Add-in Card Board Size

The overall board dimensions, excluding the area for edge card pins, are defined by the PCIe standard. The board size does not depend on the number of lanes, but is related to the faceplate size along the card edge. The values in the table below are maximum allowed values.

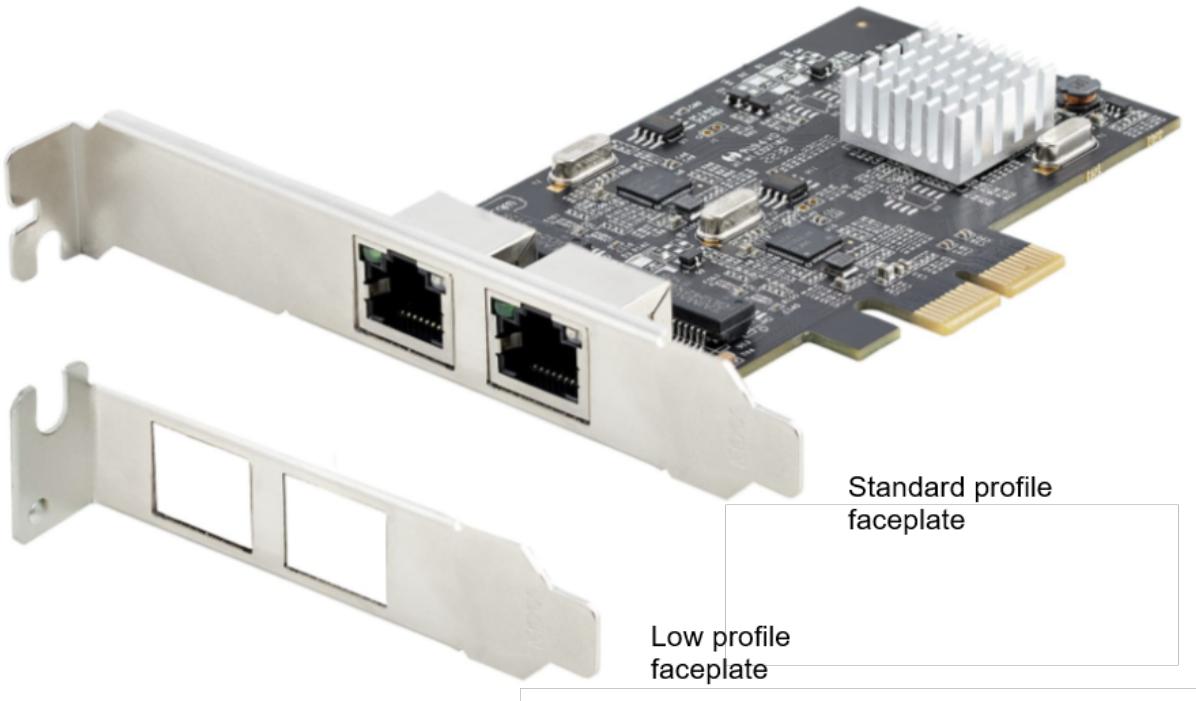
Full Length	(L x H x W) = 312 x 111.15 x 20.32 (mm)
3/4 Length	(L x H x W) = 312 x 111.15 x 20.32 (mm)
Half Length	(L x H x W) = 167.65 x 111.15 x 20.32 (mm)
Low-profile	(L x H x W) = 167.65 x 68.9 x 20.32 (mm)

The image below shows the L and H dimensions. Note that the W dimension is the z-axis profile of the PCB, including its components.

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Low-profile cards and standard profile cards can be distinguished by their faceplate. These cards use the same connector and pinout, but they are designed with different bracket/faceplate assembly, as shown in the image below.



One common form factor is an eight-lane card, which has 89 pins on both the A-side and B-side. Designers should note that each RX and TX lane is interleaved with ground pins to maintain differential impedance and minimize crosstalk between PCIe lanes.

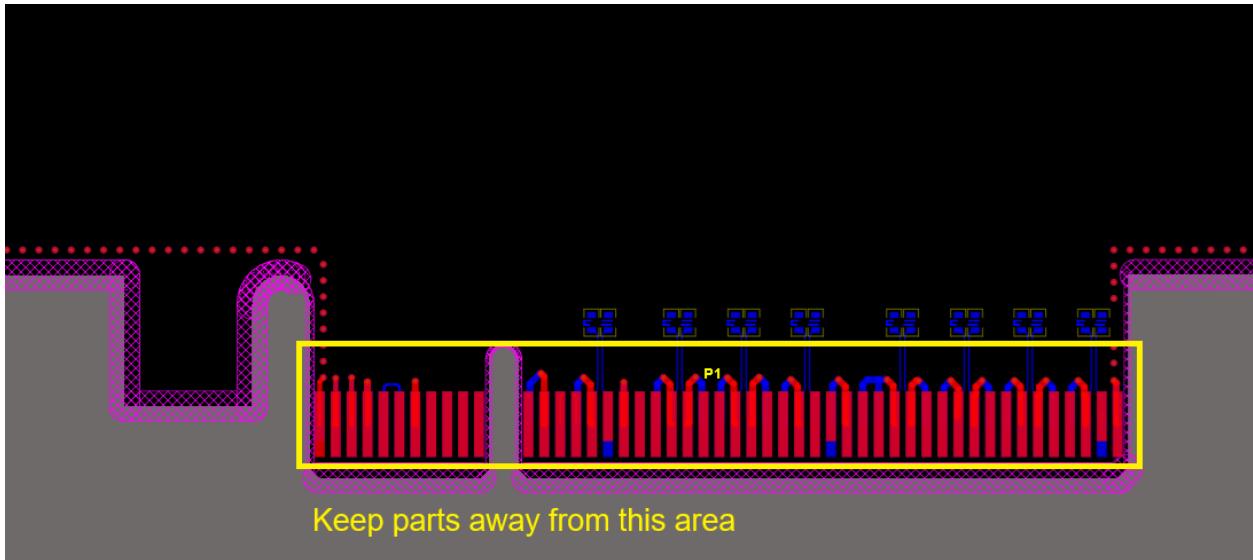
PCIe Edge Card Layout Guidelines

PCIe edge cards function similarly to other high-speed PCBs. They typically have a standard thickness of 62 mil. Designers can mix and match materials to create a stack-up and include power and ground planes. PCIe lanes follow standard routing as they transition from the edge connector

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Routing into the edge connector: Newer generation PCIe connectors should ideally be SMD connectors as this eliminates stubs that would normally be present on through-hole pins. Typically if a high-reliability connection is needed, a through-hole version can be used but with routing on the back layers in order to **eliminate any stubs**. This will help ensure signal integrity during the transition into the PCIe edge card.

Component keep-out areas: Define a keep-out area on the top edge of the connector. This area can contain traces but should avoid components. Typically, **coupling capacitors** are placed near the keying region, with other components positioned above them. However, coupling capacitors could be placed on the motherboard/main board design before the signals reach the PCIe edge connector.



Edge clearance rules: Define a board edge clearance rule, typically around 10 mils. Clearances may need to be increased near the keying area with a board edge keepout (see above) to prevent exposure of copper along the board edge, reducing the risk of short circuits. Keeping the clearances larger in this area gives an allowance for any mechanical damage that may arise along the card edge.

Grounding: The grounding strategy for a PCIe card is typically to have all components over a single system ground and have a separate chassis ground for the card faceplate. A common application of PCIe cards is as an add-in card for networking (copper or fiber). For a wired Ethernet connection, there will be a chassis ground requirement around the ring in order to ground the shroud on the RJ45 connector block.

Other applications may also require a chassis ground. Generally, the faceplate is connected to chassis ground due to its direct connection to the device enclosure, while the rest of the components on the PCB will sit over a uniform ground plane.

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PCIe Edge Card Template Example

The PCIe edge card template shown below is sized for 8x lanes in a standard edge connector. The card is sized below the maximum dimensions defined in the PCIe standard, so the card size can be changed as you see fit. Feel free to download this edge card template and use it in your own projects.

The screenshot shows the Altium 365 Viewer interface. At the top, there's a navigation bar with icons for Layers/Objects, SCH, PCB, and 3D, followed by search and filter tools. The main workspace is mostly empty, with a few code snippets visible in the right panel:

- [\$plugins.Download.viewTitle\$] (with a close button)
- [\$plugins.Download.viewApp.sectionTi...]
- [\$plugins.Download.fileTypes.altium...]
- [\$ins.Download.viewApp.downloadBu...]

In the bottom left corner, there's a logo for "ALTIUM 365 VIEWER".

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About Author

Zachariah Peterson has an extensive technical background in academia and industry. He currently provides research, design, and marketing services to companies in the electronics industry. Prior to working in the PCB industry, he taught at Portland State University and conducted research on random laser theory, materials, and stability. His background in scientific research spans topics in nanoparticle lasers, electronic and optoelectronic semiconductor devices, environmental sensors, and stochastics. His work has been published in over a dozen peer-reviewed journals and conference proceedings, and he has written 2500+ technical articles on PCB design for a number of companies. He is a member of IEEE Photonics Society, IEEE Electronics Packaging Society, American Physical Society, and the Printed Circuit Engineering Association (PCEA). He previously served as a voting member on the INCITS Quantum Computing Technical Advisory Committee working on technical standards for quantum electronics, and he currently serves on the IEEE P3186 Working Group focused on Port Interface Representing Photonic Signals Using SPICE-class Circuit Simulators.

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