

University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design

ASSIGNMENT 2 DUE Tuesday November 8, 2016 AT BEGINNING OF CLASS

Neatness Counts!

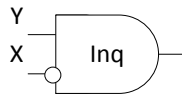
It is expected that answers to assignments are either typed or written **extremely** neatly. In all cases, the Karnaugh Maps formats below for **must** be used, either copied and edited to add the required bits and circles or printed and written on. Also, all circuits should be drawn electronically using a circuit drawing package.

1. Simplify the following expression, using Boolean algebra, to minimal SOP form. Show (absolutely) every Boolean algebra rule used in the simplification. (Less steps will yield better marks!)

a. $F_1 = \bar{P} \bar{R} S + \bar{P} \bar{Q} R + \bar{P} Q \bar{R} + \bar{P} R \bar{S}$

b. $F_2 = (A + D + E)(\bar{A} + B + \bar{C})(\bar{A} + B + \bar{D})(A + \bar{C})$

2. An *Inquiry* gate has two inputs (X and Y); the output is 0 except when X=0 and Y=1.



Realize the function $F = \bar{A}B + A\bar{C}$ using only inquiry gates.

- Note: Only A, B, C and 0 and 1 may be used as gate inputs.
- Hint: 4 gates are sufficient.

3. Find a minimum network to realize $F = \bar{A} \bar{B} \bar{D} + \bar{B} \bar{C} \bar{D}$ using only 2-input NOR gates. Only A, B, C and D are available and not their complements. (4 gates are sufficient).
4. Find a minimum network to realize $Z = ab'e'f + c'e'f + d'e'f + gh$ using only 2-input NAND gates.
5. Consider the function specified by the Karnaugh map below:

AB\CD	00	01	11	10
00	1	1		1
01	1	1	1	
11			1	
10			1	

- a. Realize the function using an 8-to-1 multiplexer with control inputs A, B and D.
- b. Repeat, this time realize the function using a 4-to-1 multiplexer. Select the control inputs to minimize the number of added gates.
6. Text (Mano, Kime, Martin, 5th edition) , page 106 #2-29, or
Text (Mano, Kime, Martin, 4th edition) , page 330 #6-4
7. Text (Mano, Kime, Martin, 5th edition) , page 107 #2-30, or
Text (Mano, Kime, Martin, 4th edition) , page 330 #6-5
8. Text (Mano, Kime, Martin, 5th edition) , page 107 #2-31, or
Text (Mano, Kime, Martin, 4th edition) , page 331 #6-6

9. Consider the following VHDL process. **A** and **B** are input ports of type integer, and **Tout** is an output port of type integer.

```

ARCHITECTURE test2 IS
  SIGNAL T1,T2 : integer;
  PROCESS (A,B)
    VARIABLE V1: integer;
  BEGIN
    T1 <= A+B;
    IF (A=5) THEN
      V1 := 3;
      T2 <= V1 + T1 +2;
    ELSE
      V1 := 4;
      T2 <= T1 + B;
    END IF;
    Tout <= T2 + A;
  END PROCESS;
END test2;

```

Assume that **A=0** , **B=0** , **T1=0** , **T2=0** , **V1=0** and that **A** changes from **0** to **5**. What are the final values of **T1** , **T2** , **V1** , **Tout** after the process is executed and it goes back to the suspended state? Justify and explain your answer. (4 marks for the correct answers and 4 marks for a logical explanation).

10. Text (Mano, Kime, Martin, 5th edition) , page 109 #2-34, or
Text (Mano, Kime, Martin, 4th edition) , page 201 #4-20
11. Text (Mano, Kime, Martin, 5th edition) , page 281 #4-7, or
Text (Mano, Kime, Martin, 4th edition) , page 282 #5-7
12. Text (Mano, Kime, Martin, 5th edition) , page 282 #4-8, or
Text (Mano, Kime, Martin, 4th edition) , page 282 #5-8
13. Text (Mano, Kime, Martin, 5th edition) , page 282 #4-9, or
Text (Mano, Kime, Martin, 4th edition) , page 282 #5-9
14. Text (Mano, Kime, Martin, 5th edition) , page 282 #4-10, or
Text (Mano, Kime, Martin, 4th edition) , page 282 #5-10

Some Karnaugh maps for your editing pleasure

A\BC	00	01	11	10
0				
1				

AB\CD	00	01	11	10
00				
01				
11				
10				

Change the variables if your expressions require different variable names!

