University of Victoria
Faculty of Engineering
Department of Computer Science
CSc 355 Digital Logic and Computer Organization

MIDTERM EXAM October 26, 2015

NAME: LillAnne. (Print)

ID NUMBER: _____

SIGNATURE: _____

TIME: 75 minutes
INSTRUCTOR: LillAnne Jackson

Question	Value	Mark
1	10	
2	10	
3	8	
4	8	
5	6	
6	2	
7	4	
8	8	
9	4	
TOTAL	60	

STUDENTS MUST CHECK THE NUMBER OF PAGES IN THIS EXAMINATION PAPER BEFORE BEGINNING TO WRITE, AND REPORT ANY DISCREPANCY IMMEDIATELY TO THE INVIGILATOR

- The questions are to be answered on the examination paper.
- The exam is **NOT** open book. Calculators are **NOT** permitted.
- A copy of the *Boolean Algebra Formulae* are provided as the last page of this exam.
- For your convenience, there are unfilled Karnaugh maps placed on some pages in this document. It is certainly possible that there are more or less than the number that might be needed.
- The marks assigned to each question are printed within square brackets.
- There are 10 pages in this document, including this cover page and the final (formulae) page.
- It is strongly recommended that you read the entire exam through from beginning to end before beginning to answer the questions.

1. **[10 mark]** Use Boolean Algebra to simplify the following logical expression to a minimal Sum-of-Products form:

$$F = X(W + YZ) + Y(\overline{W}\,\overline{X} + XY) + W\overline{Y}Z$$

Show (absolutely) every Boolean algebra rule used in the simplification.

$= WX + XYZ + \bar{W}\bar{X}Y + XY + W\bar{Y}Z$ | dist, idempot

$= WX + Y(X + \bar{X}\bar{W}) + W\bar{Y}Z$ | ~~simplif~~ dist.

$= WX + Y(\bar{W} + X) + W\bar{Y}Z$ | simplif.

$= WX + \bar{W}Y + XY + W\bar{Y}Z$ | dist.

~~$+WX + \bar{W}Y + (W + \bar{W})XY + W\bar{Y}Z$~~

$= WX + \bar{W}Y + W\bar{Y}Z$ | consensus

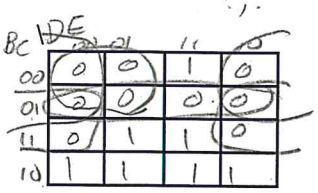
from Kmap
$WX + \bar{W}Y + W\bar{Y}Z$

2. **[10 marks]** Convert the following expression into the specified forms:

a. Convert $F = (B + C\overline{D} + DE)(\overline{C} + BE)$ into minimal Product-of-Sums form.

$= B\overline{C} + B\overline{E} + C\overline{C}\,\overline{D} + BC\overline{D}E + \overline{C}BE + BDE$ distributive,

$= B\overline{C} + BE + \overline{C}DE$

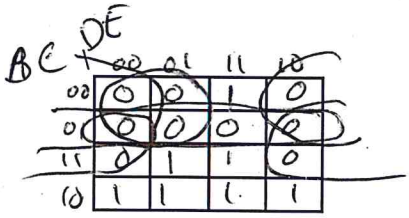


$\overline{F} = \overline{B}C + \overline{B}\,\overline{D} + C\overline{E} + \overline{B}$

$F = B\overline{C} + BE + BC\overline{D}E + \overline{C}DE + BDE$ dist.

For POS - first find $\overline{F}$

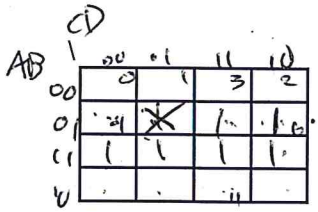
$\overline{F} = \overline{B}C + C\overline{E} + \overline{B}\,\overline{E} + \overline{B}\,\overline{D}$ ✱



$F = (B + \overline{C})(\overline{C} + E)(B + \overline{E})(D + \overline{B})$ ✱

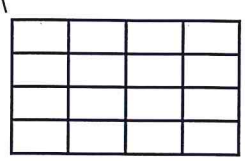
b. Convert $F = (AB + C)(B + \overline{C}D)$ into Sum-of-Minterms form.

$= AB + AB\overline{C}D + BC$ ✱



$F = AB\overline{C}\,\overline{D} + AB\overline{C}D + ABC\overline{D} + ABCD + \overline{A}B\overline{C}D + \overline{A}BCD$

$F = \sum m(6, 7, 12, 13, 14, 15)$



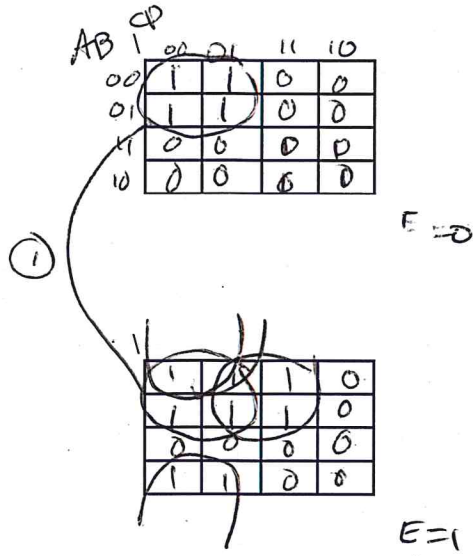
3. **[8 marks]** Implement the following function using a minimum number of 2-input NAND gates. (At most 4 inverters can also be used.)

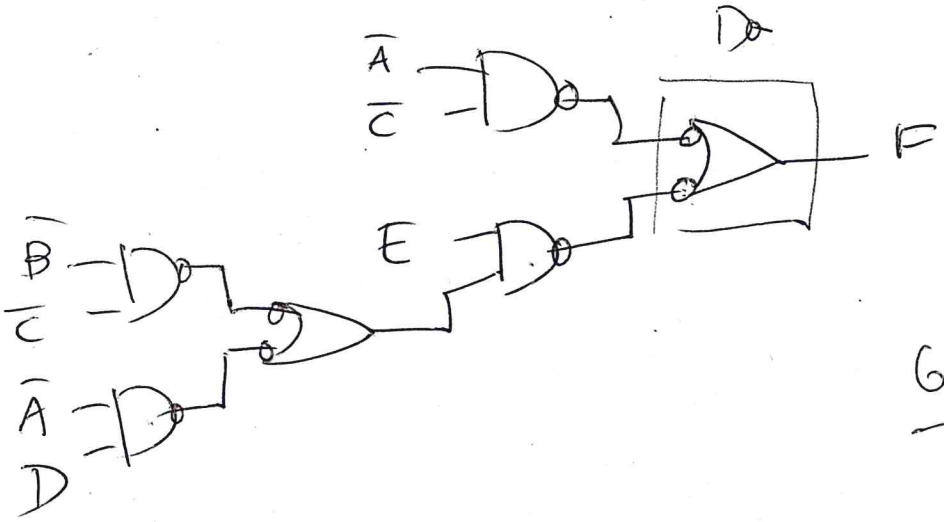
$$F = \overline{A}\,\overline{C}\,\overline{E} + \overline{A}\,\overline{C}\,\overline{D} + \overline{A}\,DE + A\overline{B}\,\overline{C}\,E$$

& SOP

$$F = \overline{A}\,\overline{C} + \overline{A}\,DE + \overline{B}\,\overline{C}\,E$$

$$= \overline{A}\,\overline{C} + E(\overline{A}D + \overline{B}\overline{C})$$

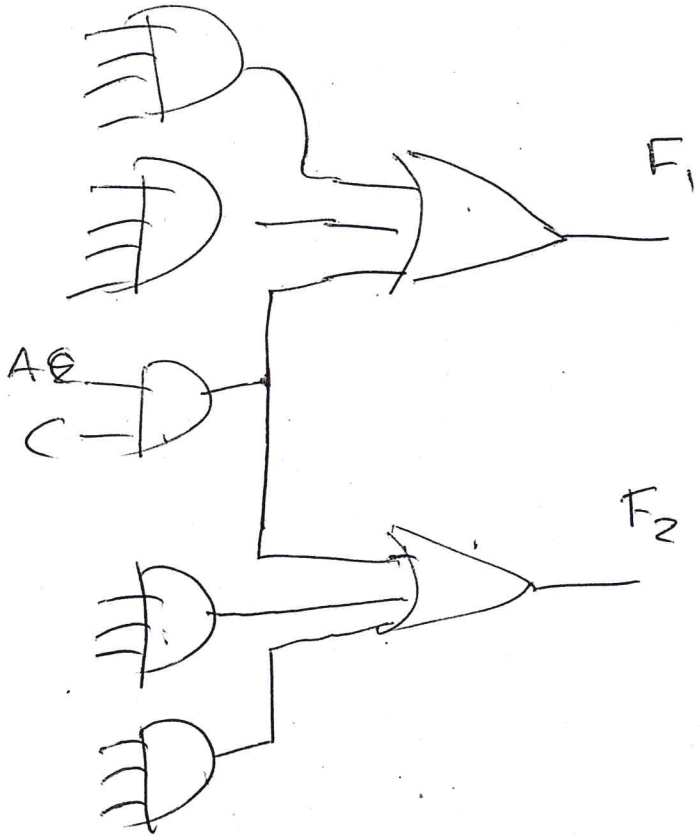


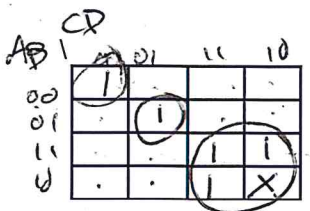


6 NAND

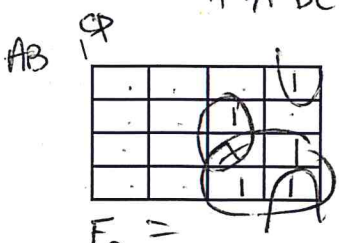
4. **[8 marks]** Implement the following 2 functions using a minimum number of AND and OR gates and Inverters.

$F_1(A,B,C,D) = \sum m(0,5,11,14,15);\ d = \sum m(10)$, and
$F_2(A,B,C,D) = \sum m(2,\ 7,10,11,14);\ d = \sum m(15)$

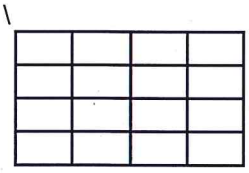


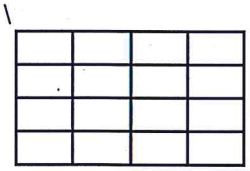


$F_1 = AC + A\bar{B}\bar{C}\bar{D} + \bar{A}BC\bar{D}$



$F_2 = AC + BCD + \bar{B}\bar{C}\bar{D}$





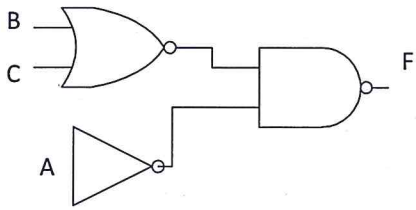
$F_1 = AC + \bar{A}\bar{C}(\bar{B}D + B\bar{D})$

$F_2 = AC + C(\bar{B}D + B\bar{D})$

7 gates

4 inverters

5. **[6 marks]** Create a timing diagram for the following circuit, with two different assumptions:

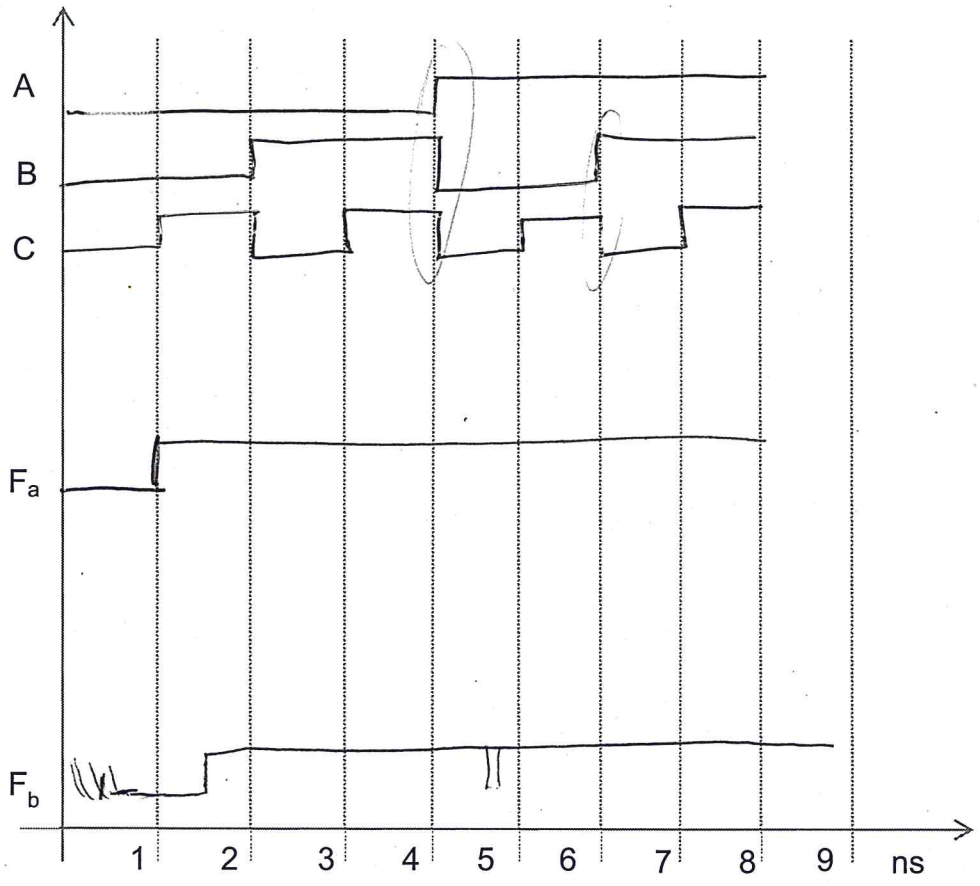


$\overline{B+C \cdot \overline{A}} = \overline{B\overline{C}} + A$

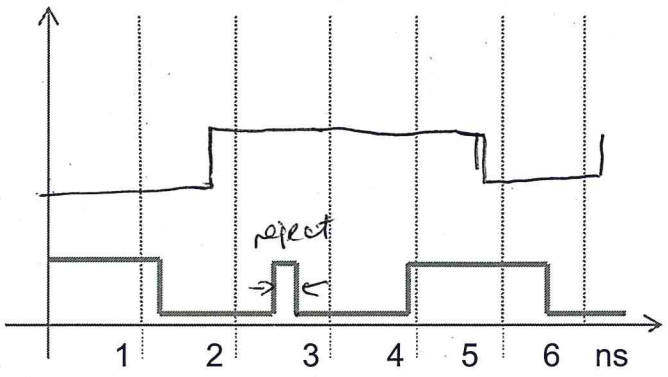
$(B+C)+A$

a. For F_a, assume all circuit components are ideal and have no delays,

b. For F_b, assume that the NAND and NOR gates each have an inertial delay of 0.25 ns and the inverter has an inertial delay of 0.5 ns.



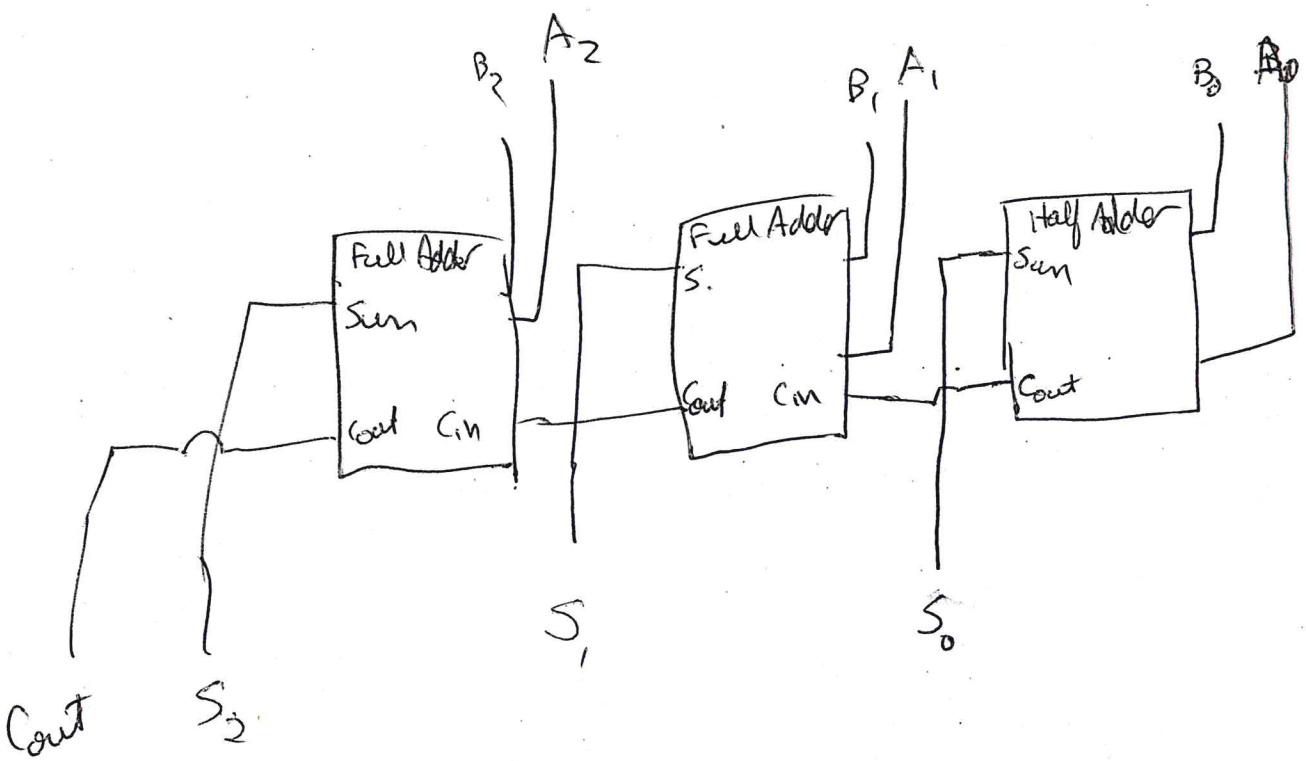
6. **[2 marks]** The waveform below is applied to an inverter with an intertial delay of .5 ns and a rejection time of .3ns. Complete the timing diagram below to show the output of the inverter:



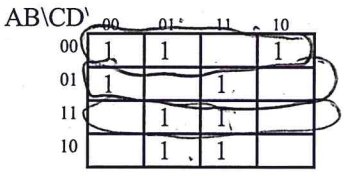
7. **[4 marks]** Create a 3-bit adder from Half-Adder and Full-Adder circuits. Carefully label the circuits and all inputs and outputs.

$A = A_2 A_1 A_0$

$B = B_2 B_1 B_0$

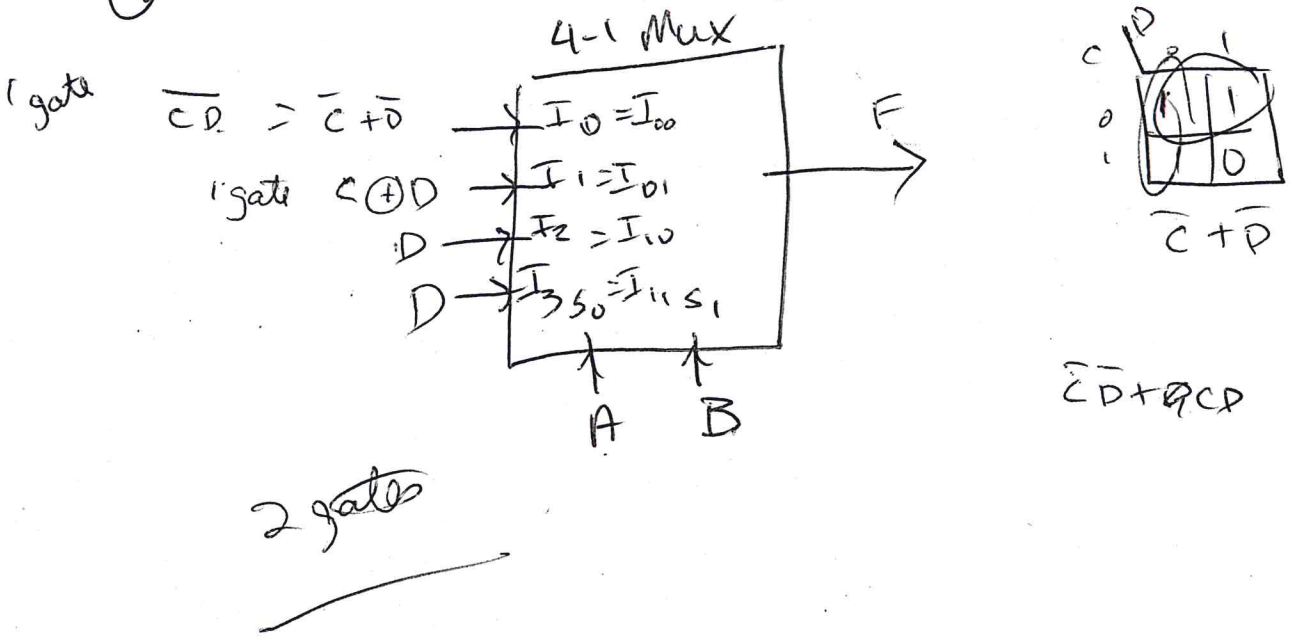


8. **[8 marks]** Consider the function specified by the Karnaugh map below:



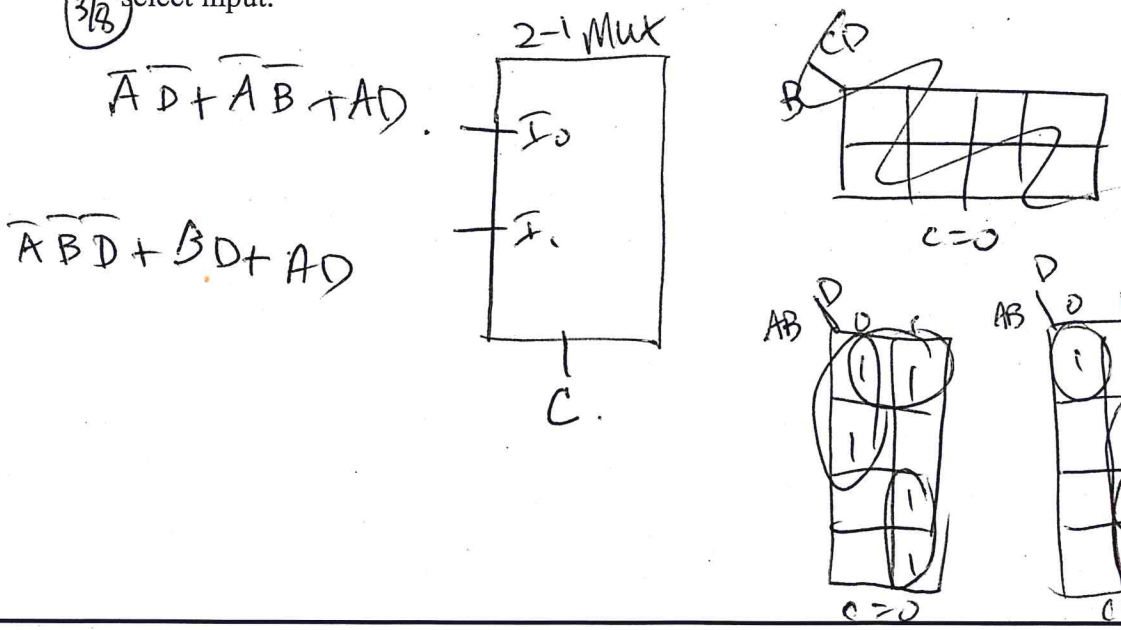
a. Realize the function using a 4-to-1 multiplexer that uses a minimum number of added gates and inverters.

5/8



b. Re –do: This time realize the function using a 2-1 multiplexer that attaches C to the select input.

3/8



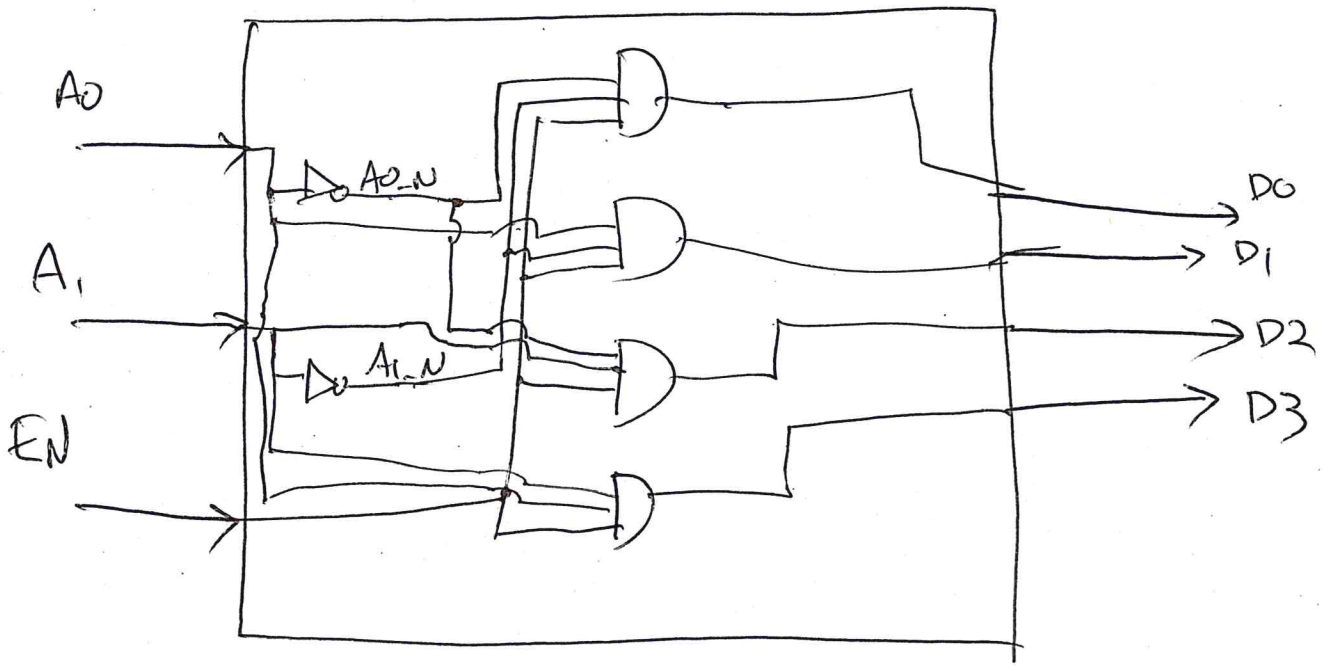
9. **[4 marks]** Consider the following VHDL description:

```
Entity test9 is
     Port (A0, A1, EN: in std_logic;
     D: out std_logic_vector(3 downto 0);
End test9;

Architecture implementation of test9 is
Signal A0_n, A1_n: std_logic;
Begin
     D0 <= A0_n and A1_n and EN;
     A0_n <= not A0;
     D1 <= A0 and A1_n and EN;
     D2 <= A0_n and A1 and EN;
     A1_n <= not A1;
     D3 <= A0 and A1 and EN;
End implementation;
```

These statements are executed concurrently (ie, not sequentially)

a. Draw a logic diagram that corresponds to the architecture.



b. This diagram corresponds to the combinatorial circuit described in class. Which type of circuit is this?

Decoder.

The End