University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
Lab 4: VHDL for Combinational Circuits

Introduction

This is not a lab in which you construct circuits using the DDE boards.

The goal of this lab is to expose you to programming and designing circuits with VHDL. You will:

- learn how to compile and simulate a VHDL description of a circuit;
- learn how to describe the circuit functionality in VHDL and verify it, given a circuit specification;
- learn how to analyze a given VHDL description.

<Observe that there is no pre-lab exercise this week.>

In-Lab Exercises: Complete In the Lab

4. DesignWorks Tutorial

- Work through the DesignWorks tutorial, as posted on the course Connex site (Lab4_DWTutorial.pdf).

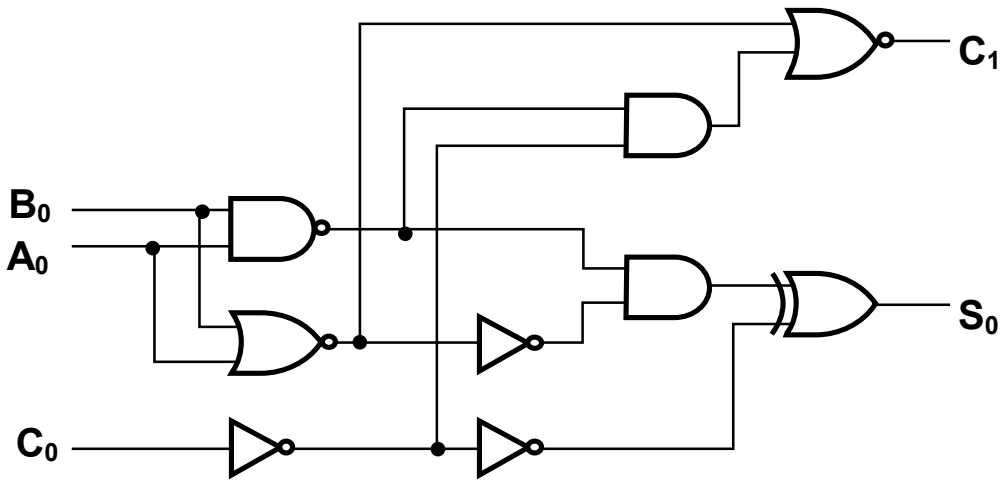
5. VHDL Tutorial

- Work through the VHDL tutorial, as posted on the course Connex site (Lab4_DWTutorialVHDL.pdf).

6. Use VHDL: to create a component description

- Use VHDL to create, then compile and simulate, a structural architecture that implements the **`LabCircuit`** entity below, with a structural VHDL architecture that implements the circuit further below .

```
entity LabCircuit is
 port (A0,B0,C0: in std_logic;
       C1,S0: out std_logic);
end LabCircuit;
```



4. Consider the following description of a circuit.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY circuit2 IS
  PORT(   sel : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
          i0,i1,i2,i3 : IN STD_LOGIC;
          dataout : OUT STD_LOGIC);
END circuit2 ;

ARCHITECTURE dataflow OF circuit2 IS
BEGIN
  dataout <= i0 WHEN sel = "00"
  ELSE i1 WHEN sel = "01"
  ELSE i2 WHEN sel = "10"
  ELSE i3 WHEN sel = "11"
  ELSE 'X';
END dataflow;
```

a) Why, in the description, are there only four **WHEN** conditions?

_____

b) What is the meaning of the last **ELSE "X"** statement clause?

_____

_____

c) Sketch a timing diagram that shows a simulation of this circuit:

d) What circuit does this architecture represent?

_____