

University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
Lab 3: Multiplexer & Adder Circuits

Introduction

The goal of this lab is for you to prepare the design of the combinational circuits that will be implemented on the DDE board during the lab session.

The objectives of this lab are to be able to:

- Use a multiplexer to implement an arbitrary truth table.
- Use the information of data sheets for combinational circuits to decide how to connect all inputs.
- Get more experience on the physical DDE board by designing another combinational circuit.
- Develop the truth table for a combinational logic problem.
- Use Karnaugh maps to simplify the expressions.

NOTE: DesignWorks and Visio, which are available in the lab, are excellent tools for drawing logical circuit diagrams. The lab is available during building hours and as follows:

- Mondays before 11:30 and after 3:30
- Tuesdays before 11:30 and after 7
- Wednesdays before 11:30 and after 2:30
- Thursdays before 9:30 and after 5:30
- Fridays before 9:30 and after 3:30.

The pre-lab worksheet is to be completed and submitted in Class on Friday, September , 2016. It will, however, continue to be accepted in the instructor's office (EOW 206) until 4pm that day. After that time, however, it will **not** be accepted and no grade will be recorded for a pre-lab delivered later!!!

Please submit early, rather than late!

Chips Used in this Lab

- 7402 quad 2-input NOR chips (3 chips)
- 74151 data selector / multiplexer

Part 1: Pre-Lab Exercises: Complete Before the Lab

Neatness & Use of the Worksheet counts: Pre-lab grades are being allocated for extremely neat use of the pre-lab worksheet provided.

1. **Circuit 1 Using a Multiplexer:** A simple (but not too secure!) data security system encodes (or converts) from one form to another before storage or transmission. Design a circuit to encode unsigned 4-bit binary numbers. The scheme will add an extra bit, labeled as "X", added according the following rule. Each number will have 5 bits, the 4 bits of the unsigned binary number plus a parity bit X. The encoding works as follows:
 - All numbers exactly divisible by 4 (without any remainder) must be transmitted with even parity. (Recall that even parity means that the number of '1' bits in ABCDX is even).

- All other numbers must be transmitted with odd parity. (The number of '1' bits in ABCDX is odd).
- 2. Create a truth table that has: a row for every input combination and an indication of the corresponding output bit X. (Also, it might be helpful to indicate the decimal equivalent of the number and whether or not the number is exactly divisible by 4.)
 - Include your truth table on the Pre-Lab 3 worksheet.
- 3. Create a Karnaugh map for bit X.
 - Include your Karnaugh map on the Pre-Lab 3 worksheet.
- 4. Design an implementation of this function (that is, to realize "X") using a 74151 8-input multiplexer. Three of the four inputs (A, B, C or D) will be attached to the select inputs. Make a decision on which 3 to use, such that the resulting circuit has a minimum number of gates or inverters required.
- 5. Examine the data sheet provided for the 74151 8-input multiplexer and determine the appropriate connection to each data input to the 74151.
- 6. The 74151 input called 'strobe' must be connected for the circuit to function. Review the data sheet and decide how to connect it. Include this information on pre-Lab 3 worksheet
- 7. **Circuit 2 Design a Full Adder:** A full adder circuit that adds two binary digits, X and Y, plus an input carry digit, C, and produces two outputs, S and Co is to be designed. The output S is the least significant bit of the sum and Co is the most significant bit of the sum. Redraw the circuit using 2-input NOR gates and inverters on the main inputs, A, B, C and D.
- 8. Create a truth table which shows all the possible input conditions and the resulting outputs.
 - Include your truth table on the Pre-Lab 3 worksheet.
- 9. Plot the results onto two Karnaugh maps, one for S and one for Co, then determine the minimal SOP and POS expressions for each output.
 - Show your work and the simplified equations for S and Co on the Pre-Lab 3 worksheet.
- 10. Design circuits for S and Co that use 2-input NOR gates only. The optimal implementation needs only 9 NOR gates (but answers with 11 are acceptable – do not believe everything on the web, where many sites imply the minimal NOR circuit needs 12 gates).
 - Include your circuit on the Pre-lab 3 worksheet.

NOTE: You can and should check your solutions to the pre-lab exercises with your course instructor or the TA who holds office hours).

Part 2: Procedures for the In-Lab Exercises

1. Greet your lab instructor and review your marked Pre-Lab Worksheet 3. Inform him/her that you have reviewed the posted solution set before attending the lab.
2. Build the multiplexer circuit as designed in the Pre-Lab exercise and test to ensure it functions.
3. Demo the working circuit to your instructor.
4. Build the adder circuit as designed in the Pre-Lab exercise and test to ensure it functions.
5. Demo the working circuit to your instructor.
6. If you have time left at the end of the lab: experiment with the DesignWorks software, which is on the lab computers. Observe that, in addition to drawing circuits, the software can also simulate circuit operations. This software **will** be used in some future labs.

Pre-Lab Worksheet #3

NAME: _____ LAB Section: B0__

2. Truth table:

[illegible]

3. Karnaugh Map:

AB\CD	00	01	11	10
00				
01				
11				
10				

5&6. Your Circuit: (Please be neat & indicate pin numbers on all chips.)

Strobe is connected to: _____

8. Truth Table:

9.

A\BC	00	01	11	10
0				
1				

A\BC	00	01	11	10
0				
1				

10. Your Circuit: (Please be neat & indicate pin numbers on all chips.)