University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
Lab 5: Introduction to Sequential Circuits

Introduction

This lab explores basic sequential logic circuits, that is, circuits that contain memory. Here you analyze three such single bit memory units (S-R latches, D latches, and D flip-flops). The objectives of this lab are to become familiar with latches and flip-flops, specifically to:

- Construct an S-R latch and study its behaviour.
- Construct a D latch and study its behaviour.
- Study the behaviour of a D flip-flop.
- Build and use a binary counter, a 7-segment decoder driver and a 7-segment LED decimal display.

NOTE: DesignWorks is available in the lab, which has no scheduled classes on Mondays!
The pre-lab worksheet is to be completed and submitted **before** the deadline, as follows:

1) In Class (10-11:20 am) on Monday, November 2, 2015; or
2) In the instructors office hours (3-5 pm) on Monday, November 2, 2015; or
3) Into the box in the service window in EOW 206 before it closes (4 pm) on Tuesday, November 3, 2015.

Absolutely no submissions slid under doors or left in various mail boxes will be accepted. Please do not knock on the EOW 206 window after it closes, they have been instructed not to accept in that case. Please submit early, rather than late!

Chips Used in this Lab

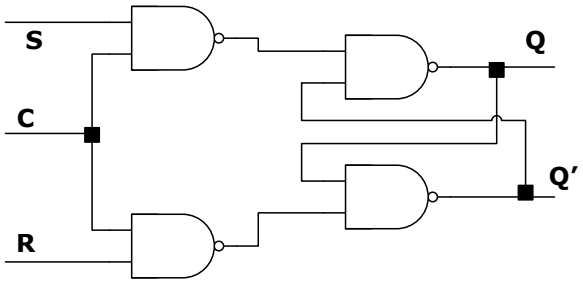
- 7474 dual D flip-flop
- 74193 up/down binary counter
- 9368 7-segment decoder driver
- 7-segment display

Part 1: Pre-Lab Exercises: Complete Before the Lab

Neatness & Use of the Worksheet counts: Pre-lab grades are being allocated for extremely neat use of the pre-lab worksheet provided, and for including a DesignWorks circuit where requested. (It reduces marking time significantly!)

Pre-Lab #1 [8 marks]

The circuit below is an S-R Latch with a Control Input, labelled “C”. The Control input restricts the Latch's sensitivity.



a) [2] Complete in a truth table with a row for every input combination of S, R, C and Q (Q=current state) and an output column for Q+ (Q+=next state). Q+ is your prediction of the output.
b) [6] Draw the circuit using DesignWorks and simulate it with the appropriate logical sequence to: (1)
   i. start in a stable state with Q=0;
   ii. set Q=1 and then go back to a stable state;
   iii. reset Q=0 and then go back to a stable state.

   Print the result of the simulation, including the changes on the internal lines (label them appropriately), together with the circuit diagram.

Pre-Lab #2 [12 marks]

Design problems are often simplified by having all transitions in a system occur synchronously (i.e., at the same time) by using a clock. The output changes occur only at specific clock events (typically when the clock goes high, or the clock goes low). Some ICs have inputs (*asynchronous inputs*) that directly change the output whenever they are changed. Such a D-type flip-flop with *edge-triggering* and *asynchronous inputs* is the 7474.

Edge-triggering means that the circuit is enabled only on a transition from low to high or from high to low of the clock. The former is *leading edge-triggered* (or *positive edge-triggered*) and the latter is *trailing edge-triggered* (or *negative edge-triggered*). The *Set* (or *Preset*) and *Reset* (or *Clear*) inputs are asynchronous because they cause an immediate change in state without regard for the clock.

IMPORTANT: Distinguish the functionality of the synchronous versus the asynchronous inputs of a flip-flop.

a) [6] Create a wiring diagram (Using DesignWorks or Visio) for a D flip-flop using one of the two flip-flops available on a 7474 chip. Connect a data switch to the D input, LEDs to the appropriate Q and Q' outputs, a logic switch to the appropriate clock input, data switches to the appropriate Preset and Clear inputs. Label all parts of the diagram, then print and attach to the worksheet.

b) [3] Fill in the table a with your prediction of the output. If you use one row for each combination of the inputs, you will use all of the rows in the table, but you can also give complete details by only using a smaller number of rows.

c) [3] Are the preset and clear inputs active **high** or active **low**? Explain your answer.

Pre-Lab #3 [20 marks]

The required data sheets (abbreviated) for the 74193 are available in the Lab Resources.

- In computer systems, decimal numbers are usually encoded into binary. It requires four binary digits to represent a single decimal digit; a J-K FF or a latch can represent each binary digit.
- A 7-segment display is widely used for the display of a decimal digit in electronic watches, clocks, and appliances. The 7-segment display consists of seven LED segments arranged in the shape of an eight. You are going to use this display in conjunction with a counter to display numbers.
- The 74193 4-bit binary counter counts from 0 through 15 and then recycles, that is it counts as follows: 0, 1…14, 15, 0, 1,…

Examine the data sheets of the 74193 binary counter carefully. In particular, look at the description and the timing diagrams of the typical *clear, load* and *count* sequences. Answer the following questions:

a) [2] What values should be applied to the inputs of the counter to obtain the **CLEAR** function? What is the output that is expected from the counter when it is cleared?

b) [2] What values should be applied to the inputs of the counter to obtain the **LOAD** function? What is the output that is expected from the counter when it is loaded?

c) [2] What values should be applied to the inputs of the counter to cause it to count down? What is the output that is expected from the counter when it is counting down?

d) [2] Is this circuit a leading edge or trailing edge triggered counter?

e) [6] Create a wiring diagram for the 74193 so that it can be cleared, loaded and it can count down. Connect the outputs **Aout, Bout, Cout** and **Dout** to four LED's such that **Dout** is the most significant. Use DesignWorks or Visio for your drawing and label it.

f) [6] A 7-segment display is a small chip that contains seven LEDs configured in a *square-8 pattern* as shown in the diagram below. In order to function, it requires an extra circuit called the *7-segment display driver*, which is the 9368 chip shown in the diagram just below the 7-segment. The display driver latches the input binary number and generates the appropriate seven outputs with sufficient power to light the segments of the display. The seven outputs, "**a**" through "**g**", are intended to be connected to a 7-segment display. If one of the outputs (**a** through **g**) is high, the corresponding LED segment illuminates. For example, if inputs are **0001** (e.g. the output of the binary counter for decimal 1), only segments **b** and **c** glow. Use the data sheet for the 9368 to determine all the connections for the display driver and draw a pin-out diagram for the circuit above. . Use DesignWorks or Visio for your drawing and label it.

Part 2: Procedures for the In-Lab Exercises

1. Greet your lab instructor and review your marked Pre-Lab Worksheet 5. Inform him/her that you have reviewed the posted solution set before attending the lab.
2. Build the circuit as designed in the Pre-Lab exercises #1, 2 and 3 and test to ensure they function.
3. Demo the working circuits to your instructor.

Pre-Lab Worksheet #5 NAME: _____ LAB Section: B0__

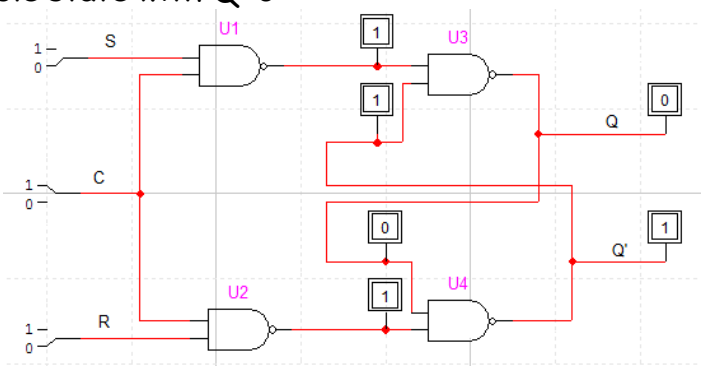
Pre-Lab 1, part a) Truth table:

C	S	R	Q	Q+
0	X	X	0	0
0	X	X	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

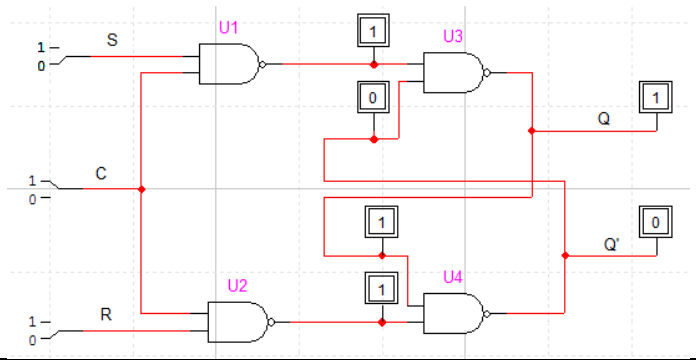
Note that the last 2 rows are race conditions!

Pre-Lab 1, part b) Print and attach the result of the simulation

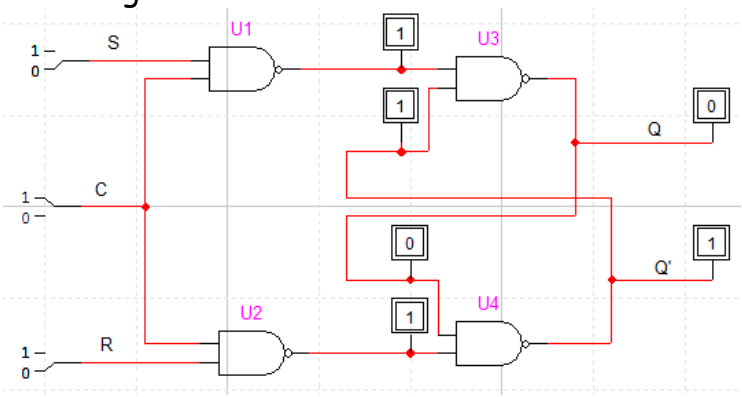
start in a stable state with Q=0



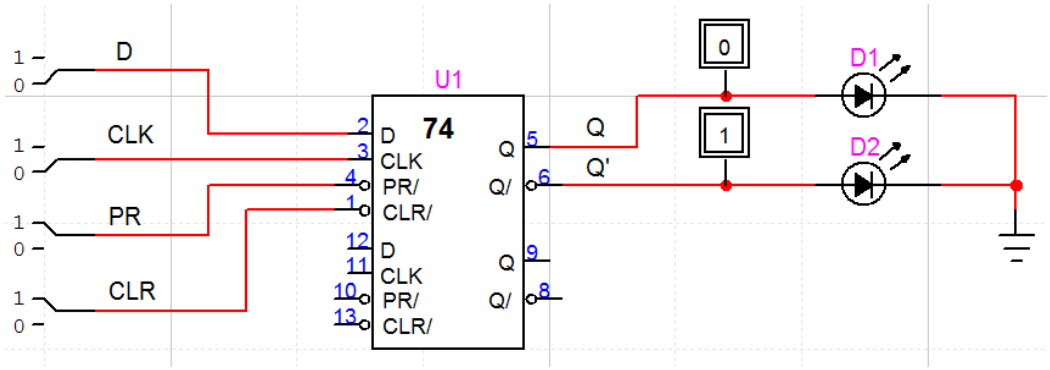
set Q=1 and then go back to a stable state



reset Q=0 and then go back to a stable state



Pre-Lab 2, part a) Print and attach the wiring diagram



Pre-Lab 2, part b) Truth Table

Preset	Clear	Clk	D	Q	Q+
0	0	X	X	X	undef
0	1	X	X	X	1
1	0	X	X	X	0
1	1	0	X	0	0
1	1	0	X	1	1
1	1	➔1	0	X	0
1	1	➔1	1	X	1

Pre-Lab2, part c) Are the preset and clear inputs active **high** or active **low**? Explain your answer

Both are active low

Pre-lab 3, part a) What values should be applied to the inputs of the counter to obtain the **CLEAR** function? What is the output that is expected from the counter when it is cleared

CLR = 1
Qa = Qb = Qc = Qd = 0

Pre-lab 3, part b) What values should be applied to the inputs of the counter to obtain the **LOAD** function? What is the output that is expected from the counter when it is loaded?

LOAD = 0
Qa = A, Qb = B, Qc = C, Qd = D

Pre-lab 3, part c) What values should be applied to the inputs of the counter to cause it to count down? What is the output that is expected from the counter when it is counting down?

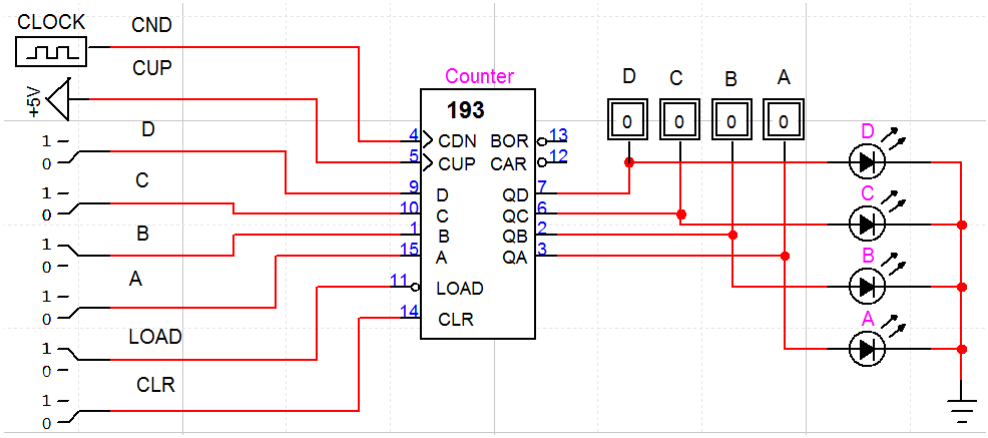
CLR=0, LOAD=1, CUP=1, CDN=clock/switch
The output should decrement by one by each leading edge of the input clock.

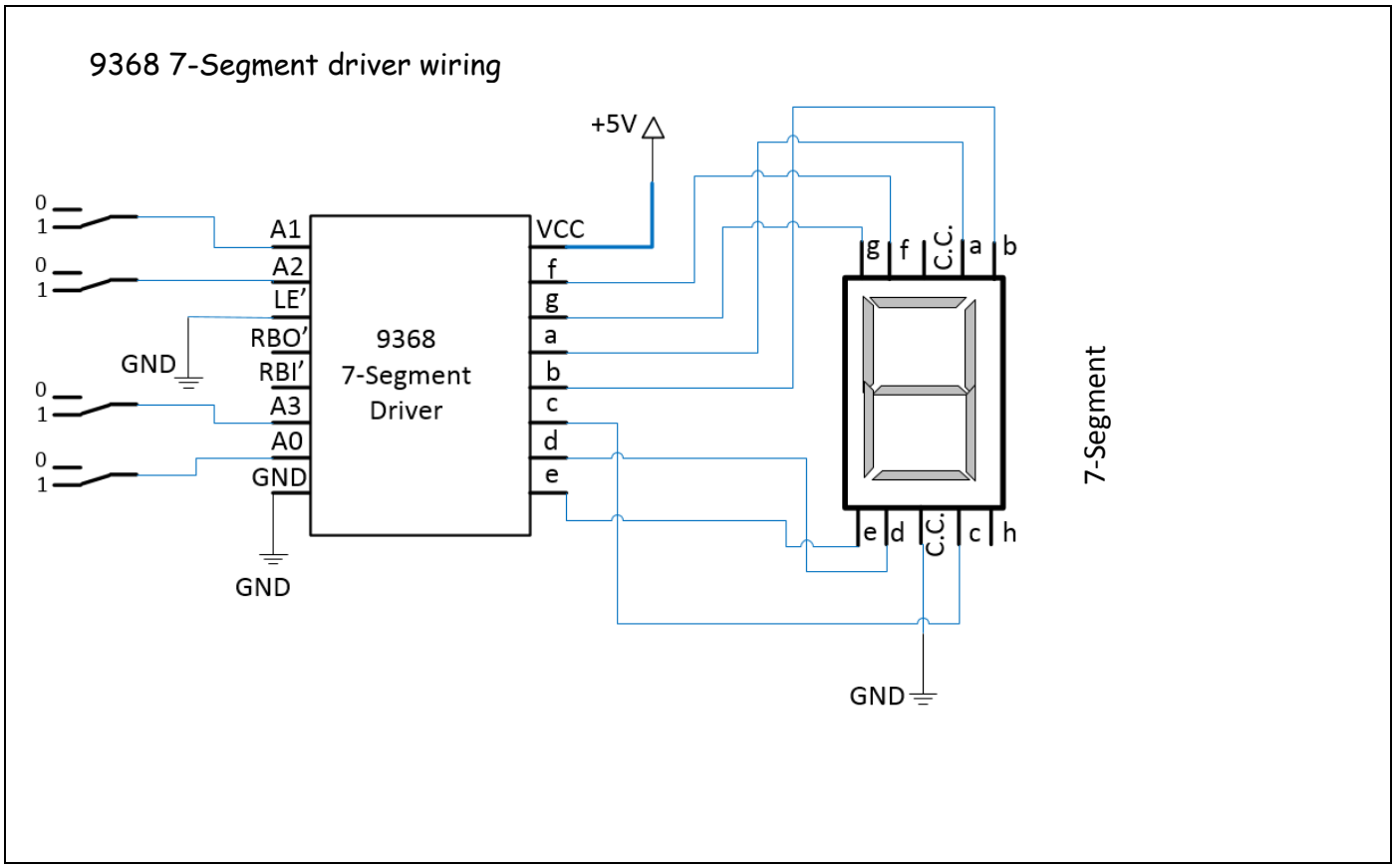
Pre-lab 3, part d) Is this circuit a leading edge or trailing edge triggered counter?

It is a leading edge triggered counter

Pre-lab 3, parts e) and f) Print and attach the wiring diagram(s).

74LS193 wiring




9368 7-Segment driver wiring
+5V
0
1
0
1
0
1
0
1
A1
A2
LE'
RBO'
RBI'
A3
A0
GND
GND
GND
9368
7-Segment
Driver
VCC
f
g
a
b
c
d
e
g
f
C.C.
a
b
e
d
C.C.
c
h
GND
7-Segment