University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
ASSIGNMENT 3
DUE: Wednesday November 30 IN CLASS

Neatness Counts!

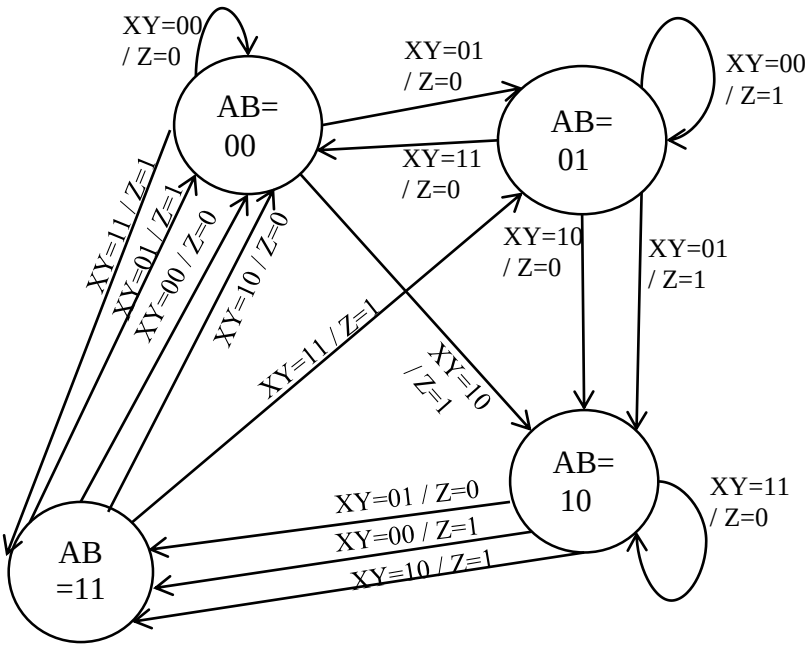
1. Design a finite state machine as a clocked Mealy sequential network with one input **X** and one output **Z**. The machine is a recognizer that has an output trigger sequence and a reset output to zero sequence. If the input sequence '0 1 1 0' occurs then the output changes to '1' coincident with the last bit of the sequence. The output remains at '1' until the reset sequence '0 1 0' is received on the input and, in this case, the output changes to '0' coincident with the last bit of the sequence. Initially, output **Z** is '0'.

   For example,

   X = 0 0 1 0 0 0 1 1 0 0 1 0 1 0 1 1 0 0 0 0 0 1 0 1
   Z = 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0 1 1 1 1 1 1 0 0

   For the design, provide a state graph, the corresponding state table and the output table. Number the states $\mathbf{S_0}$, $\mathbf{S_1}$, … Maximum marks will be given for a correct solution with the minimum number of states. **Do not** continue the design beyond this point. (In particular, there is no need to implement using flip-flops.)

2. The state diagram for a sequential circuit is given below:



   The encoded state table for the circuit is given in Table 5-15 (4th edition) or Table 4-14 (5th edition) of your textbook.

   Assuming the circuit is to be designed using two JK Flip-flops, determine the flip-flop input equations, J_A, K_A, J_B, and K_B.

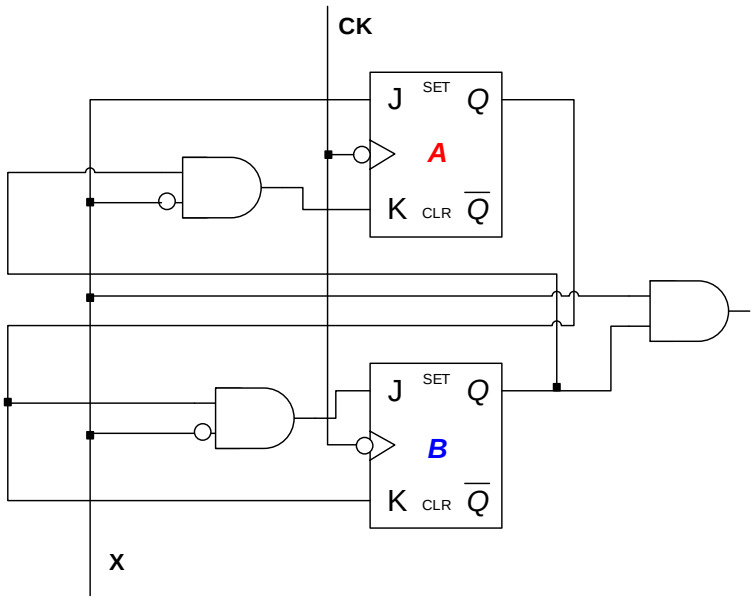
3. Text (Mano, Kime, Martin, 5th edition) , page 283 #4-14 – parts a) b) and c) only, or
   Text (Mano, Kime, 4th edition) , page 283 #5-14 – parts a) b) and c) only.

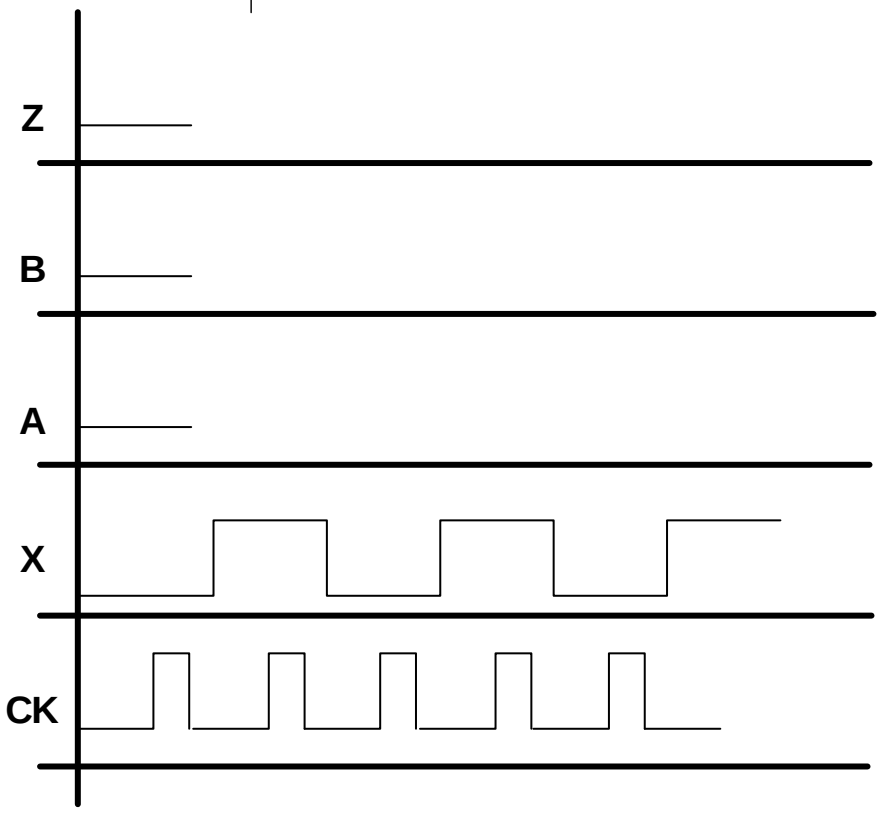
4. A gated latch (G-L FF) behaves as follows:

   If G = 0, the flip-flop does not change state.
   If G = 1, the next state of the flip-flop is equal to the value of L,
   where G and L are the two inputs to the flip flop.

   Derive the characteristic (next- state) equation for the flip-flop.

5. Complete the timing diagram for the sequential circuit shown.





6. Design a static RAM memory cell, using a set-reset flip flop for the internal storage and any other devices you require, with the following features. There are two control lines, **X** and **Y**, an input line **Ip**, and an output line **Op** (there is no clock). The values of **X**, **Y** and **Ip** require the following actions to be taken:
   - **X** = 0, **Y** = 0 : the memory cell is not selected (flip-flop contents unchanged, **Op** is to be in the high impedance state **Z**)
   - **X** = 1, **Y** = 1 : read the memory cell (output **Op** is equal to contents of flip-flop)
   - **X** = 1, **Y** = 0 : write to the memory cell (flip-flop contents to be equal to value on **Ip, Op** is to be in the high impedance state **Z**)

   X = 0, **Y** = 1 : toggle the memory cell (invert the flip-flop contents, **Op** is to be in the high impedance state **Z**).

7. Text (Mano, Kime, Martin, 5th edition) , page 287 #4-23, or
Text (Mano, Kime, 4th edition) , page 287 #5-22.

8. Text (Mano, Kime, Martin, 5th edition) , page 287 #4-25, or
Text (Mano, Kime, 4th edition) , page 288 #5-24.

9. Text (Mano, Kime, Martin, 5th edition) , page 318 #**5-1**, or
Text (Mano, Kime, 4th edition) , page 330 #6-1.

10. Text (Mano, Kime, Martin, 5th edition) , page 318 #**5-2**, or
Text (Mano, Kime, 4th edition) , page 330 #6-2.

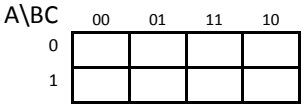
11. Text (Mano,
Text (Ma

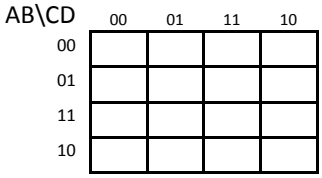
CANCEL #11 : There is an error in the question number for 4th edition!!

12. Text (Mano, Kime, Martin, 5th edition) , page 478 #**8-1**
Text (Mano, Kime, 4th edition) , page 490 #9-1

13. Text (Mano, Kime, Martin, 5th edition) , page 482 #**8-17**
Text (Mano, Kime, 4th edition) , page 494 #9-17

Some Karnaugh maps for your editing pleasure





Change the variables if your expressions require different variable names