University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
Lab 5: Introduction to Sequential Circuits

Introduction

This lab explores basic sequential logic circuits, that is, circuits that contain memory. Here you analyze three such single bit memory units (S-R latches, D latches, and D flip-flops). The objectives of this lab are to become familiar with latches and flip-flops, specifically to:

- Construct an S-R latch and study its behaviour.
- Study the behaviour of a D flip-flop, with both asynchronous and synchronous inputs.
- Build and use a binary counter, a 7-segment decoder driver and a 7-segment LED decimal display.

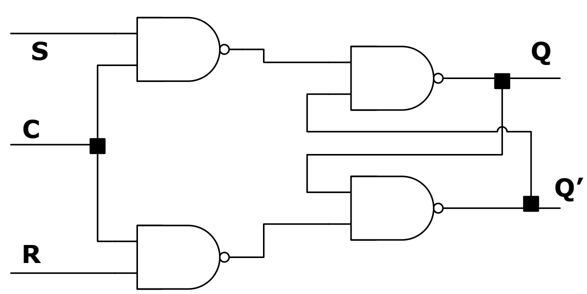
NOTE: The pre-lab worksheet is to be completed and submitted in class on Friday, October 21, in the office hour that immediately follows or before 4:00 in EOW 206.

Chips Used in this Lab

- 7400 Quad 2-input NAND gates
- 7474 dual D flip-flop
- 74193 up/down binary counter
- 9368 7-segment decoder driver
- 7-segment display

Part 1: Pre-Lab Exercises: Complete Before the Lab

1. The circuit below is an S-R Latch with a Control Input, labelled "C". The Control input restricts the Latch's sensitivity.



   a) Complete in a truth table with a row for every input combination of S, R, C and Q (where Q is the current state of Q) and an output column for Q+ (where Q+ is the next state of Q). In particular, Q+ is your prediction of the output.
   b) Draw the circuit using on 7400 (NAND gate chip), labeling the pins that you will use for circuit construction. (DesignWorks works very well for this drawing!)

2. Design problems are often simplified by having all transitions in a system occur synchronously (i.e., at the same time) by using a clock. The output changes occur only at specific clock events (typically when the clock goes high, or the clock goes low). A D flip-flop has one input, called D, and one output, called Q. Whatever value is on the D input will appear on the Q output, only after the clock event. That is, there is a

'delay' from the input to the output. It is precisely this delay that effectively forms memory. This use of the clock event is often called Edge-triggering, which means that the circuit is enabled only on a transition from low to high or from high to low of the clock. The former is *leading edge-triggered* (or *positive edge-triggered*) and the latter is *trailing edge-triggered* (or *negative edge-triggered*).

IMPORTANT: Distinguish the functionality of the synchronous versus the asynchronous inputs of a flip-flop.

In addition, some ICs have inputs (*asynchronous inputs*) that directly change the output whenever they are changed. The 7474 circuit is a D-type flip-flop with *edge-triggering* (or *synchronous*) inputs and also *asynchronous* inputs. The *Set* (or *Preset*) and *Reset* (or *Clear*) inputs of the 7474 are called asynchronous because they cause an immediate change in state without regard for the clock.

a) Examine the datasheet provided for the 7474 D flip-flop. Create a wiring diagram for a D flip-flop using one of the two flip-flops available on a 7474 chip. The asynchronous inputs are CLR and PR while the synchronous inputs are D and Q. The output is Q (aka Q+). Connect a data switch to the D input, LEDs to the appropriate Q and Q' outputs, a logic switch to the appropriate clock input, data switches to the appropriate Preset and Clear inputs. Label all parts of the diagram.

b) Create a truth table that shows your prediction of the output. While one row can be used for each combination of the inputs, it is also possible to give complete details by only using 'x' to represent some inputs, compressing the table.

c) Are the preset and clear inputs active **high** or active **low**? Explain your answer.

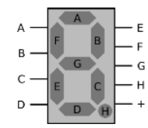
3. In computer systems, decimal numbers are usually encoded into binary. It requires four binary digits to represent a single decimal digit; a flip-flop or a latch can be used represent each binary digit. The 74193 is a pre-made 4-bit binary counter that counts from 0 through 15 and then recycles, that is it counts as follows: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1,… In addition, a 7-segment display is a device that is widely used for the display of a decimal digit in electronic watches, clocks, and appliances. The 7-segment display consists of seven small LED segments arranged in the shape of an eight. You are going to use this display in conjunction with a counter to display numbers.

a) Examine the data sheets of the 74193 binary counter carefully. In particular, look at the description and the timing diagrams of the typical *clear, load* and *count* sequences. Answer the following questions:

- What values should be applied to the inputs of the counter to obtain the **`CLEAR`** function? What is the output that is expected from the counter when it is cleared?
- What values should be applied to the inputs of the counter to obtain the **`LOAD`** function? What is the output that is expected from the counter when it is loaded?
- What values should be applied to the inputs of the counter to cause it to count down? What is the output that is expected from the counter when it is counting down?
- Is this circuit a leading edge or trailing edge triggered counter?

b) Create a wiring diagram for the 74193 so that it can be cleared, loaded and it can count down. Connect the outputs **`Aout, Bout, Cout`** and **`Dout`** to four LED's such that **`Dout`** is the most significant.

c) A 7-segment display is a small chip that contains seven LEDs configured in a *square-8 pattern* as shown: In order to function, it requires an extra circuit called the *7-segment display driver*, which is the 9368 chip shown in the diagram just below the 7-segment. The display driver latches the input binary number and generates the appropriate seven outputs with sufficient power to light the segments of the display. The seven outputs, "**a**" through "**g**", are intended to be connected to a 7-segment display. If one of the outputs (**a** through **g**) is high, the corresponding LED segment illuminates. For example, if inputs are **0001** (e.g. the output of the binary counter for decimal 1), only segments **b** and **c** glow. Use the data sheet for the 9368 to determine all the connections for the display driver and draw a pin-out diagram for the circuit above.



Part 2: Procedures for the In-Lab Exercises

1. Greet your lab instructor and review your marked Pre-Lab Worksheet 5. Inform him/her that you have reviewed the posted solution set before attending the lab.
2. Build the circuit as designed in the Pre-Lab exercises #1, 2 and 3 and test to ensure they function.
3. Demo the working circuits to your instructor.

Pre-Lab Worksheet #5 NAME: ________________ LAB Section: B0__

Pre-Lab 1, part a) Truth table:

C	S	R	Q	Q+

Pre-Lab 1, part b) Draw or print the circuit constructed using one 7400.

Pre-Lab 2, part a) Draw or print the wiring diagram

Pre-Lab 2, part b) Truth Table:

Preset	Clear	Clk	D	Q	Q+

Pre-Lab2, part c) Are the preset and clear inputs active **high** or active **low**? Explain your answer

Pre-lab 3, part a) Answers can be obtained from the data sheet for the 74193

- What values should be applied to the inputs of the counter to obtain the **CLEAR** function? ______
  What is the output that is expected from the counter when it is cleared? ________
- What values should be applied to the inputs of the counter to obtain the **LOAD** function? _______
  What is the output that is expected from the counter when it is loaded? ______________________
- What values should be applied to the inputs of the counter to cause it to count down? _________
  What is the output that is expected from the counter when it is counting down? ______________
- Is this circuit a leading edge or trailing edge triggered counter? _________________

Pre-lab 3, part b) and c) Print or draw the wiring diagram(s).