University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
Lab 6: Introduction to Sequential Circuits

Introduction

This lab provides practice designing and (possibly) implementing a Finite State Machine (FSM) starting either from some initial specifications of the problem to be solved or from a given State Diagram.

Observe that the lab was not posted in time for a Monday or Tuesday pre-lab submission date. <Sorry!> So, the pre-lab exercise will be due at the beginning of the lab. The lab hours will be used to review your solutions together and, if time, to construct and test one of the designs.

Chips Available for this Design

- 7400 quad 2-input NAND chip (3 chips)
- 7410 triple 3-input NAND chip
- 7476 dual JK flip-flop chip
- 7404 hex inverter
- 7474 dual D flip-flop chip

Pre-Lab Exercises <Give solutions to Lab Instructor at beginning of Lab.>

1. Pre-Lab #1 : FSM #1

You are part of a design team that has been asked to design a controller for a home heating system to be marketed across the cold Canadian prairies.[1] Heat is provided from two sources, a natural gas fired furnace and a passive solar window system that includes insulated shutters. If the sun is shining[2] the windows provide enough heat to warm the building. When there are clouds in the sky and during the night the windows shed heat and the shutters must be closed.

The specification of the controller is as follows:

- There are two external inputs (both simulated using data switches):
- **D**, which is to be attached to a solar detector. However, in the laboratory testing environment, a simple data switch is used to simulate the input from this device. Hence D set to 1 indicates that the sun is shining and a 0 indicates that it is not.
- **T**, which is to be attached to a thermostat placed inside the house. It returns a 1 when the building needs more heat and a 0 when it does not.

The controller can be in four different states:

- **S0**: In this state the furnace (F) is off and the shutters (S) are closed. Thus state **S0** is labeled with two bit state variables, F = 0 and S = 0.
- **S1**: In this state the furnace is on and the shutters are open. Thus state **S1** is labeled with two bit state variables, F = 1 and S = 1.
- **S2**: In this state the furnace is on and the shutters are closed. Thus state **S2** is labeled with two bit state variables, F = 1 and S = 0.

[1] In this climate it is very cold for half the year and every home must be heated.
[2] Fortunately the sun shines frequently.

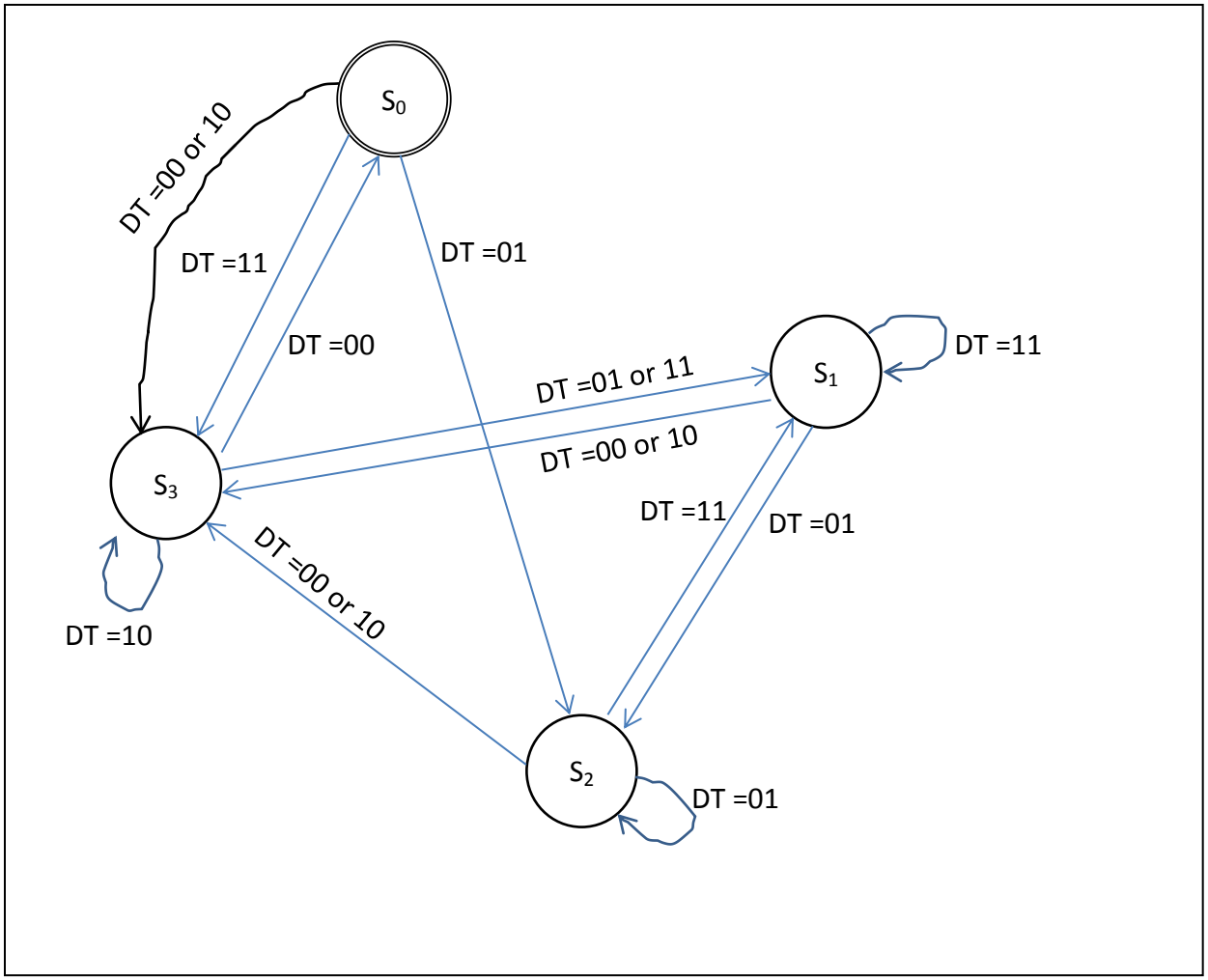
- **S3**: In this state the furnace is off and the shutters are open. Thus state **S3** is labeled with two bit state variables, F = 0 and S = 1.

The table below indicates the results of the analysis phase of this project.

From state	Input sensors: DT=	Go to state:
S0	01	Goto S2
	11	Goto S3
S1	01	Goto S2
	11	Goto S1
S2	01	Goto S2
	11	Goto S1
S3	01	Goto S1
	11	Goto S1
	00	Goto S0

All other input combinations cause the system to go to state S3. The sequential machine for the controller has four states and uses two state variables for this purpose, F and S. F and S can be monitored using two output LEDs

a) Draw the state diagram for a FSM to represent the given specifications.



b) Write an encoded state table (transition table) corresponding to the state diagram of the previous step.

Present State		Next State F^+ S^+			
F	**S**	**DT = 00**	**DT = 01**	**DT = 10**	**DT = 11**
0	0	01	10	01	01
0	1	00	11	01	11
1	0	01	10	01	11
1	1	01	10	01	11

c) Fill in the Karnaugh maps for the next states F^+, S^+, and write minimal sum-of-products equations for F^+, S^+ (show your work).

FS\DT	00	01	11	10
00	0	1	0	0
01	0	1	1	0
11	0	1	1	0
10	0	1	1	0

F+

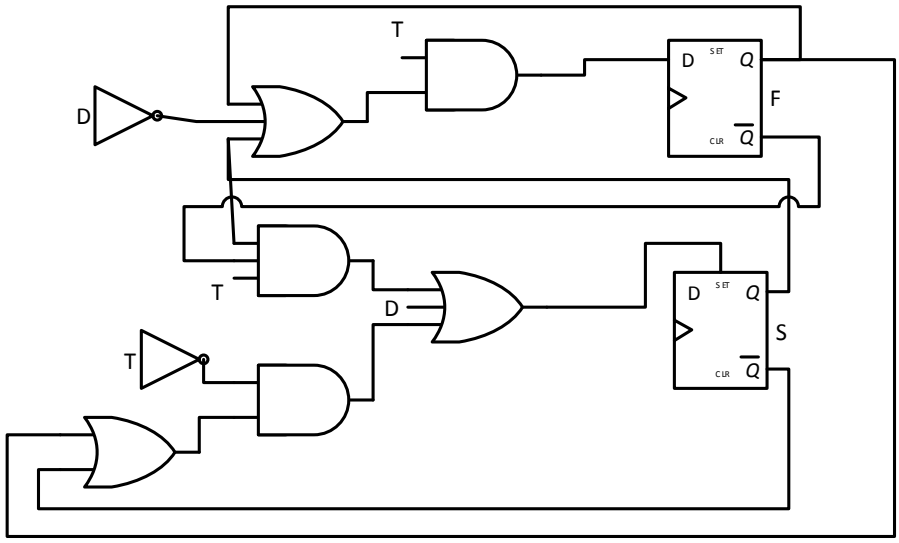
FS\DT	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	1	0	1	1
10	1	0	1	1

S+

d) For the circuit itself, it has been decided to use D flip-flops, so you can directly use the equations (i.e., D=Q+) obtained in the previous step for the implementation of the input logic. Draw the complete circuit diagram, including pin numbers, for your design. It is best to attach a separate piece of paper (properly labeled).

Note: A maximum of one 7474, three 7400, one 7404 and one 7410 chips can be used for this experiment.

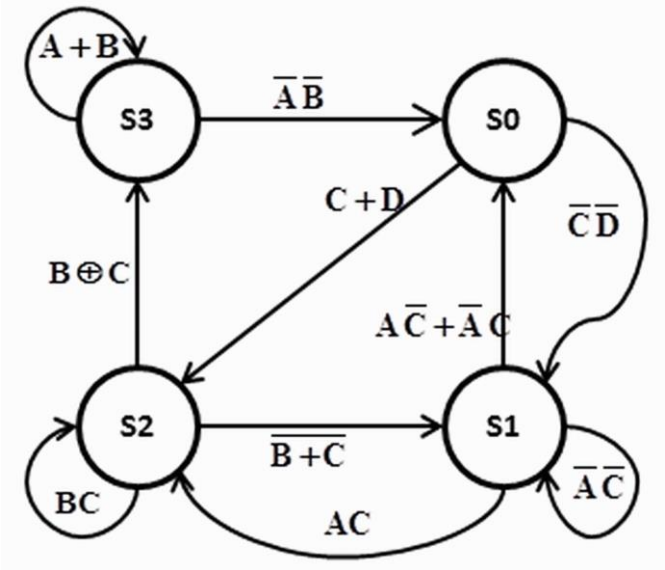
$F^+ = D'T + ST + FT = T(D'+S+F)$ $\quad S+ = S'T' + FT' + D + F'ST = T'(S'+F) + D + F'ST$



2. Pre-Lab #2: FSM #2

Design a circuit with the specifications described below.

- **External inputs**: A, B, C and D, controlled from the data switches.
- **Number of states**: 4 (The state assignment to be used is defined below.)
- **Outputs**: Two LEDs to monitor the values of the state variables, called X and Y.
- **State diagram**: shown below.



a) Complete a state table corresponding to the state diagram. Use *don't cares* for input combinations, where appropriate, so that your table can be abbreviated, and you can use exactly one row for each product term required for the relevant condition. In the example below, the first four rows are shown as a guide. Make sure that the total number of possible rows, that is, input combinations for the variables A, B, C and D, covers all the 16 possibilities for each state. An initial portion of the table is shown here – it is up to you to fill in a complete one. You may not need all of the rows shown in the table (my solution only uses 14 rows).

present state	condition				next state
	A	B	C	D	
S_0	x	x	0	0	S_1
S_0	x	x	1	x	S_2
S_0	x	x	x	1	S_2
S_1	0	x	0	x	S_1
S_1	1	x	1	x	S_2
S_1	1	x	0	x	S_0
S_1	0	x	1	x	S_0
S_2	x	1	1	x	S_2
S_2	x	1	0	x	S_3

S_2	x	0	1	x	S_3
S_2	x	0	0	x	S_1
S_3	1	x	x	x	S_3
S_3	x	1	x	x	S_0

b) Complete the encoded state table (transition table) corresponding to the state table of the previous step. Use the following state assignment (it will be just the first and last columns that change – the number of rows you use will be the same as in the previous part):

State	X	Y
S0	0	0
S1	0	1
S2	1	0
S3	1	1

present state	condition				next state
	A	B	C	D	
00	x	x	0	0	01
00	x	x	1	x	10
00	x	x	x	1	10
01	0	x	0	x	01
01	1	x	1	x	10
01	1	x	0	x	00
01	0	x	1	x	00
10	x	1	1	x	10
10	x	1	0	x	11
10	x	0	1	x	11
10	x	0	0	x	01
11	1	x	x	x	11
11	x	1	x	x	11
11	0	0	x	x	00

c) Fill in the Karnaugh maps for the next states X^+, Y^+. Remember that X^+ and Y^+ are functions of X, Y, A, B, C and D. Please use this ordering of inputs.

AB\CD	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	0	1	1	1
10	0	1	1	1

XY=00

AB\CD	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	1	1
10	0	0	1	1

XY=01

Map for X+

AB\CD	00	01	11	10
00	0	0	1	1
01	1	1	1	1
11	1	1	1	1
10	0	0	1	1

XY=10

AB\CD	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

XY=11

AB\CD	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	1	0	0	0
10	1	0	0	0

XY=00

AB\CD	00	01	11	10
00	1	1	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

XY=01

Map for Y+

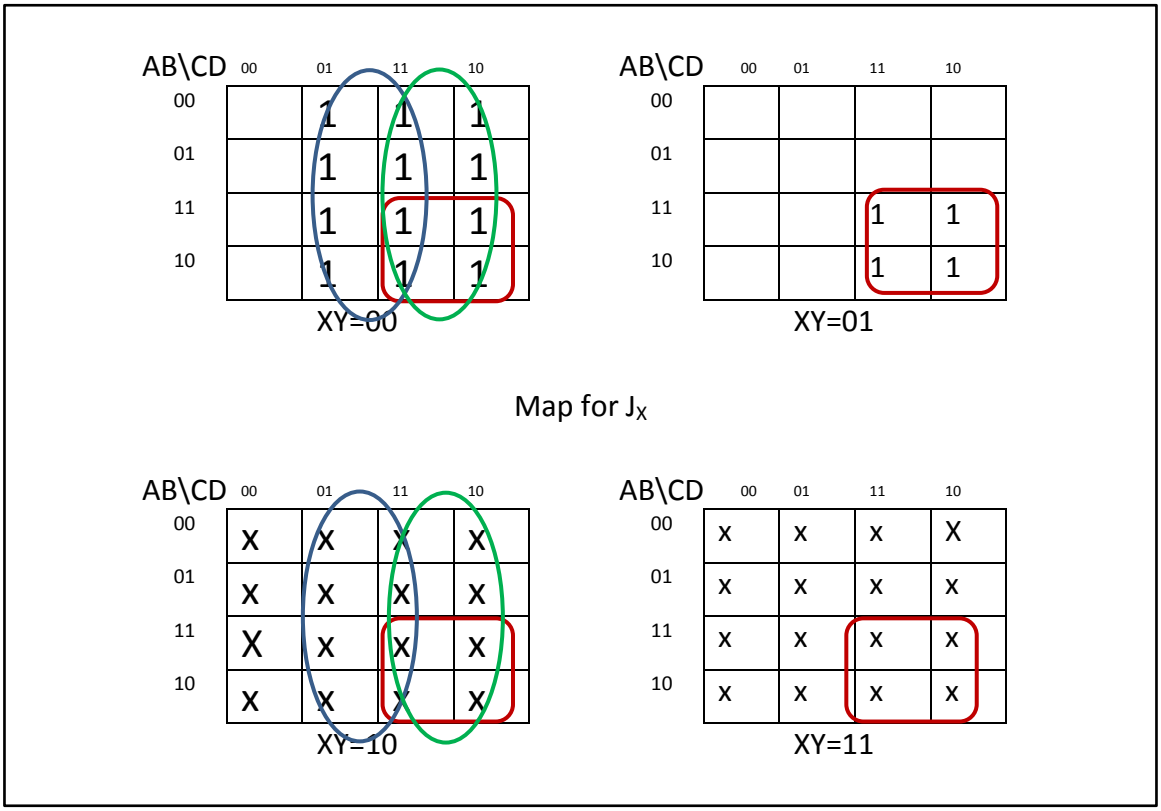
AB\CD	00	01	11	10
00	1	1	1	1
01	1	1	0	0
11	1	1	0	0
10	1	1	1	1

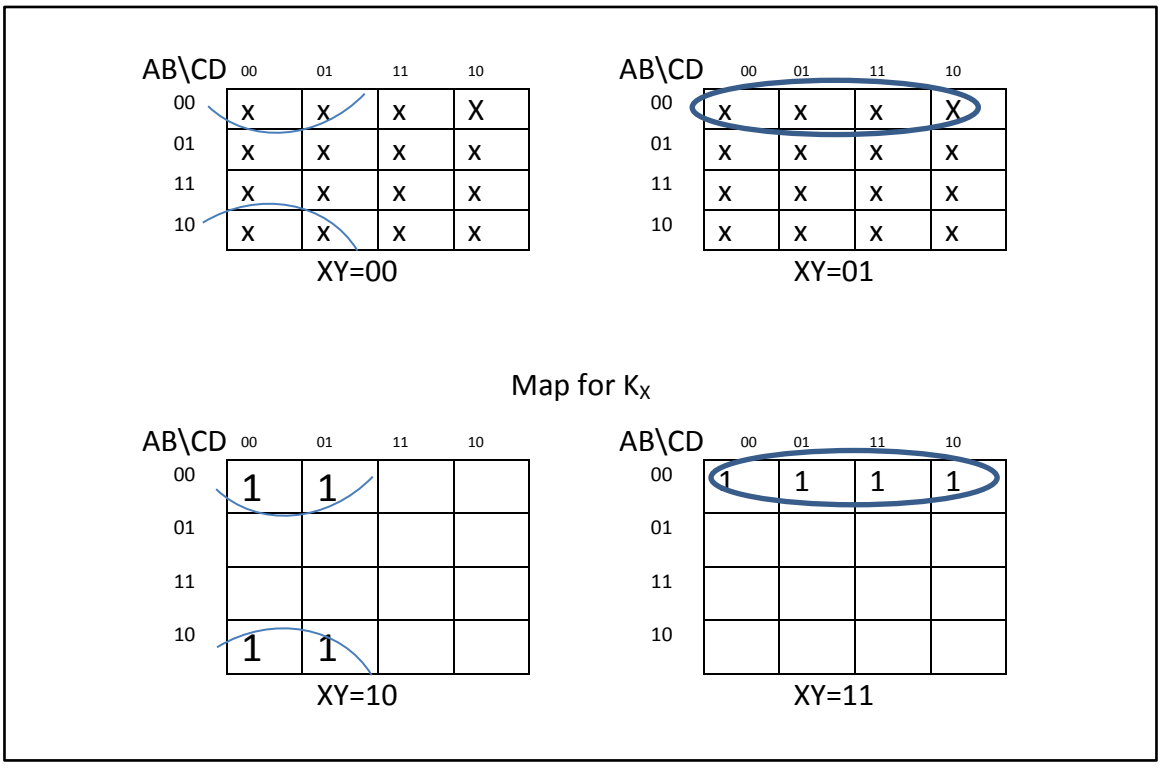
XY=10

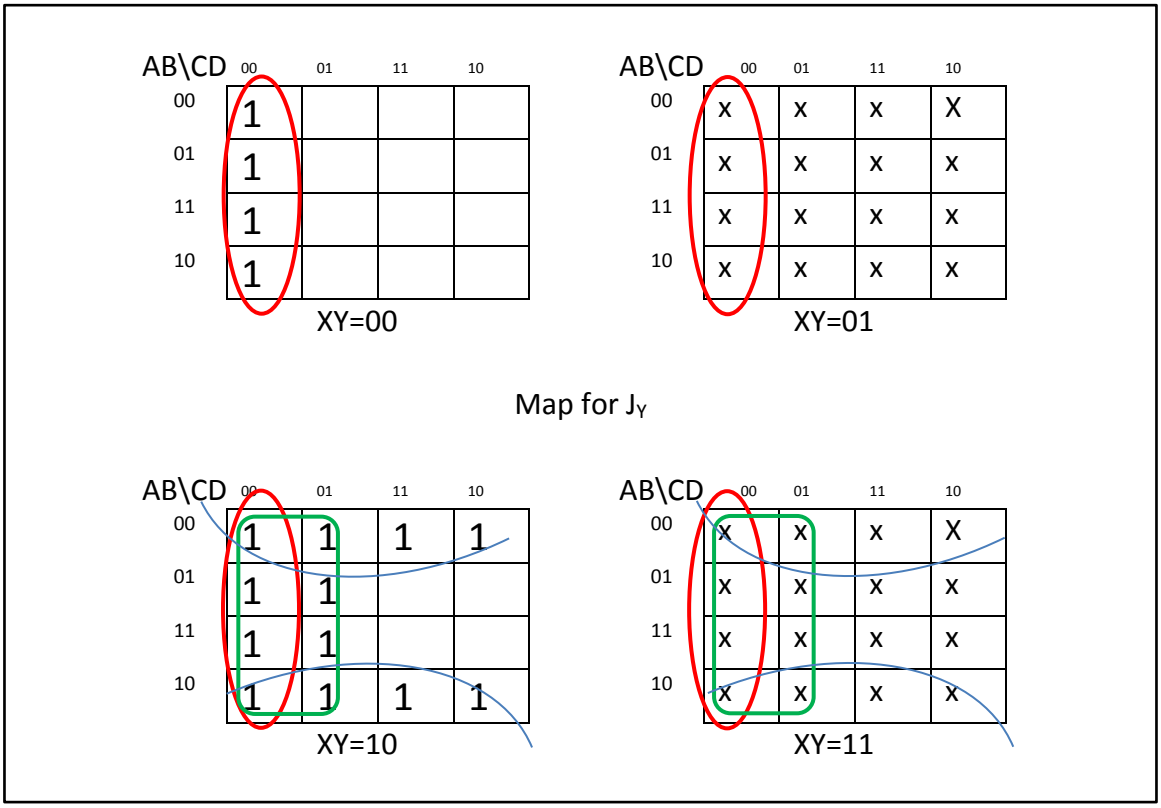
AB\CD	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

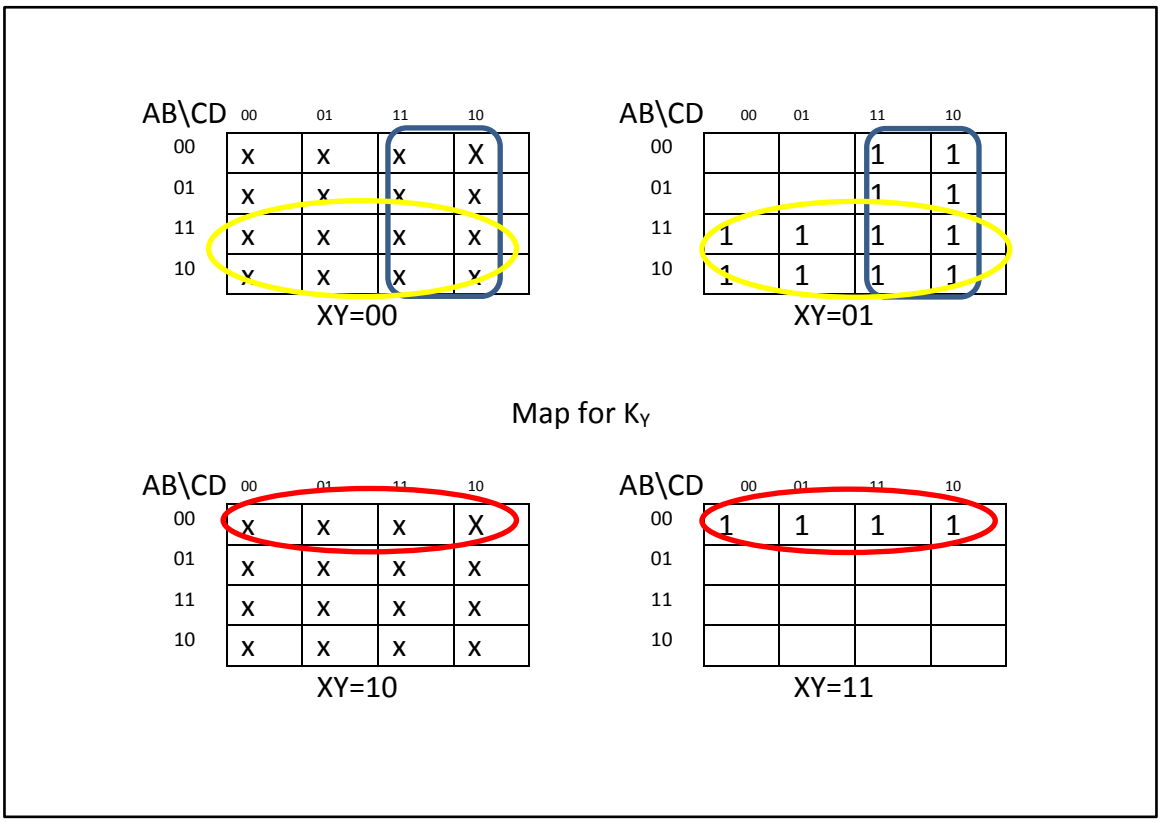
XY=11

a) From these maps, fill in the maps for the inputs for J-K flip flops representing X and Y. You need 4 Karnaugh maps of 6 inputs each (use the ones on the next two pages). Hence deduce the sum-of-products equations and minimize them using Karnaugh maps. Show your work.






AB\CD
00 01 11 10
00 1
01 1
11 1
10 1
XY=00
AB\CD
00 01 11 10
00 x x x X
01 x x x x
11 x x x x
10 x x x x
XY=01
Map for J_Y
AB\CD
00 01 11 10
00 1 1 1 1
01 1 1
11 1 1
10 1 1 1 1
XY=10
AB\CD
00 01 11 10
00 x x x X
01 x x x x
11 x x x x
10 x x x x
XY=11


AB\CD
00 01 11 10
00 x x x X
01 x x x x
11 x x x x
10 x x x x
XY=00
AB\CD
00 01 11 10
00 1 1
01 1 1
11 1 1 1 1
10 1 1 1 1
XY=01
Map for K_Y
AB\CD
00 01 11 10
00 x x x X
01 x x x x
11 x x x x
10 x x x x
XY=10
AB\CD
00 01 11 10
00 1 1 1 1
01
11
10
XY=11

a) Draw the complete circuit diagram, including pin numbers, for your design. It is best to attach a separate piece of paper (properly labeled).

Note: A maximum of three 7400 chips, one 7404 chip, one 7410 chip and one 7476 chip can be used for this experiment.

$J_x = DY' + CY' + AC = Y'(C+D) + AC$

$K_x = B'C'Y' + A'B'Y$

$J_y = C'D' + C'X + B'X = (C+D)' + X(C'+B')$

$K_y = AX' + CX' + A'B'X = X'(A+C) + A'B'X$

Part 2: Procedures for the In-Lab Exercises

1. Greet your lab instructor and show your completed Pre-Lab 6. Work with her/him and groups of your colleagues to demonstrate the correctness of your solution.
2. Build one of the circuits as designed in the Pre-Lab exercises and test to ensure they function.