University of Victoria
Department of Computer Science
CSC 355 Digital Logic and Computer Design
Lab 8: A Bus for the VSCS

This week there is no pre-lab exercise to be completed.

Introduction

The goal of this lab is to add a bus to the VCVS designed in lab 6, allowing the system to be expanded to include such useful things as memory and I/O devices. This Lab is entirely completed using Design Works.

A **possible architectural** block diagram of a simple computer is shown in Figure 1**.**

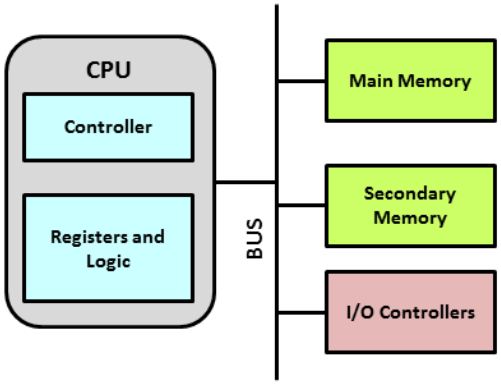


Figure 1

This lab focuses on the design of the bus, or more accurately the busses. If the system contains more than one memory location and/or device that is external to the CPU, it requires one bus to carry the addresses of the various devices and another to carry the data.

Specifications of the VCVS

Recall that the VCVS is an 8-bit accumulator architecture with a 3-bit instruction. In Lab 8 we allowed switches to input the data to the accumulator (register A) and the code. In this lab a common bus will be placed between the VCVS and 'memory'. Two memory locations will be simulated by two DesignWorks 'registers'. See Figure 2.

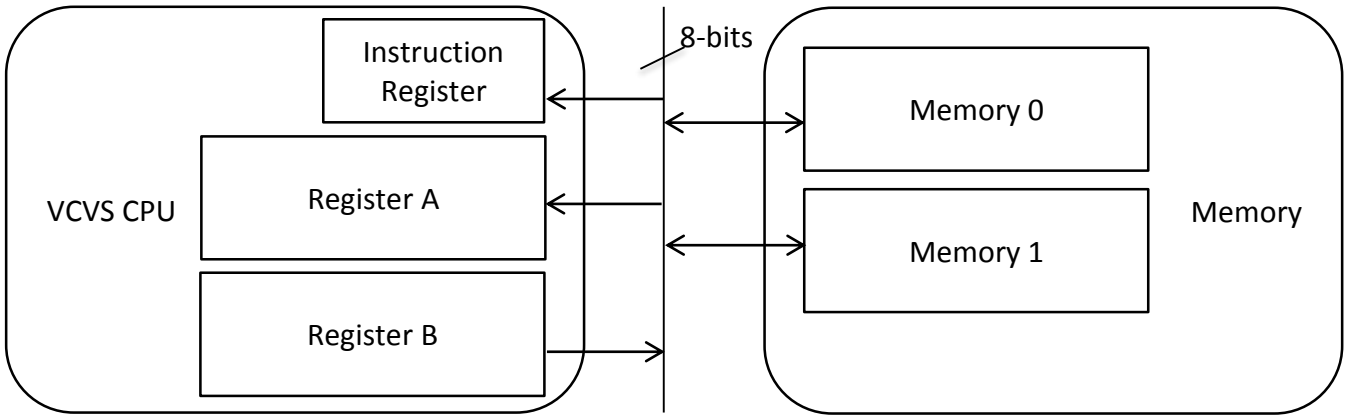
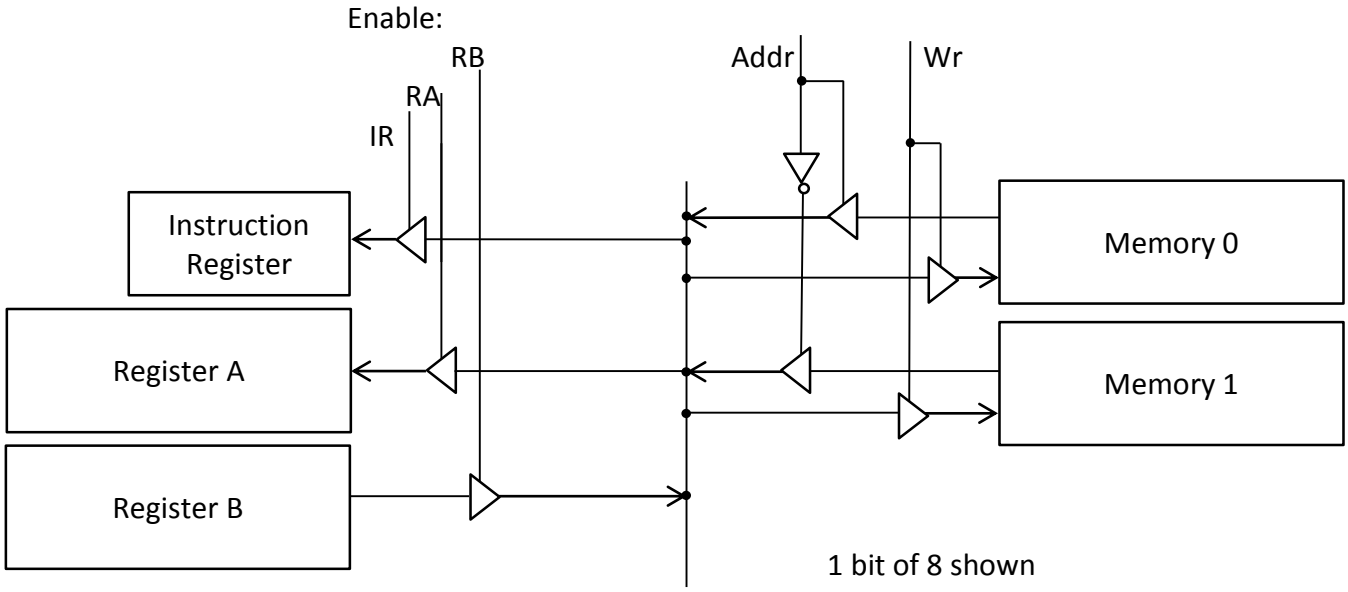


Figure 2

Control, which chooses which registers or memory are enabled, is simulated by switches. The bus itself is created with tri-state buffers. See Figure 3.



The control signals are defined as follows:

IR	Instruction Register Enable
RA	Register A Enable
RB	Register B Enable
Addr	Address (Only 1 bit of address is required because there are only 2 memory locations,.
Wr	1 = Write; 0 = Read

Pre-Lab Exercise

Read this document and think about how it might be created using Design Works.
<No submission required.>

In-Lab Exercises

Using DesignWorks, create an 8-bit bus for the VCVS.

Test and show the operation of the bus to your lab instructor.

Discuss with your instructor

- the effect of having more memory.
- How the switches that simulate the control signals could be replaced in a real system.