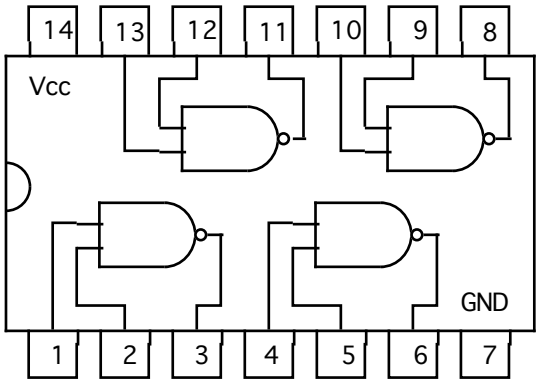
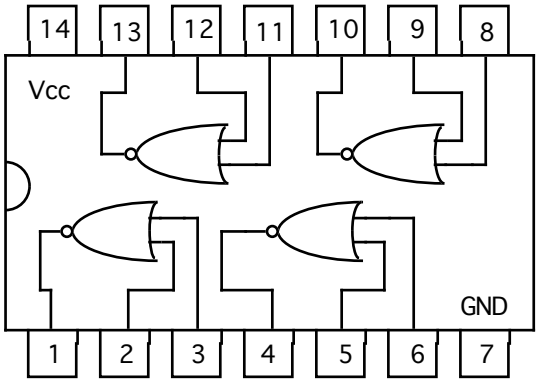
CSC 355 Chipset – Logic and Connection Diagrams

DM7400 quad 2-input NAND LOGIC AND CONNECTION DIAGRAM



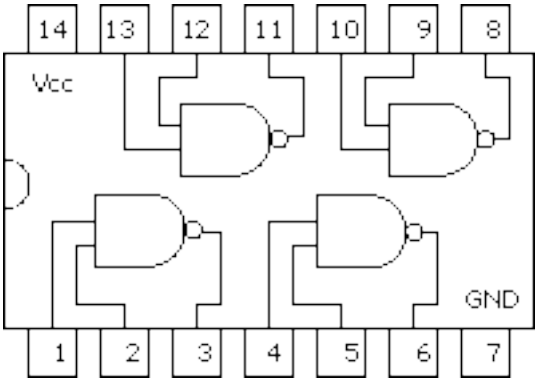
DM7402 quad 2-input NOR



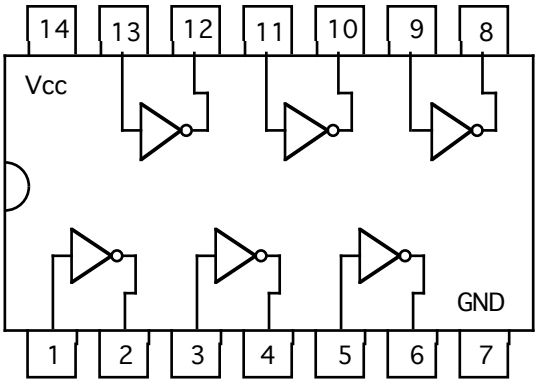
Note: The 7400 and 7402 have differnent input/ouput pin assignments!

DM7403 quad 2-input NAND (open-collector)

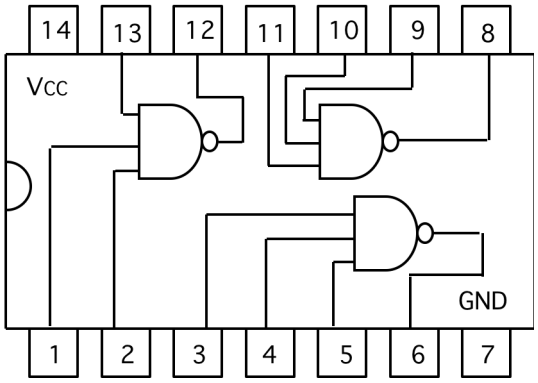
7403 open collector is designed for applications where the normal "totem-pole" output configuration is not wanted. Aside from the output, the circuitry is identical to the standard quad 2-input gate (7400).



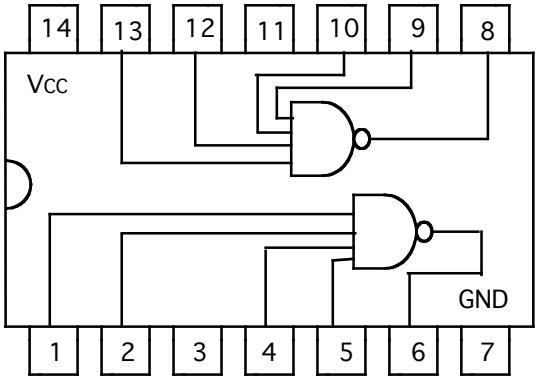
DM7404 hex inverter **LOGIC AND CONNECTION DIAGRAM**



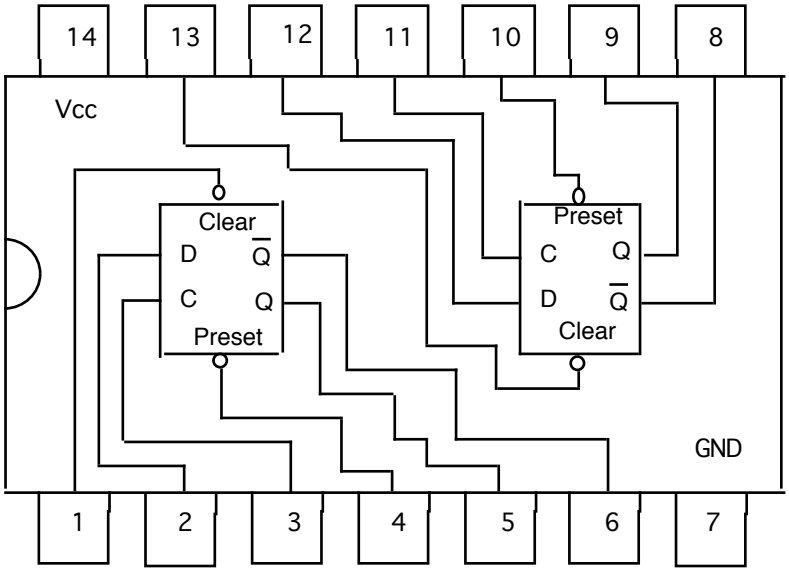
DM7410 triple 3-input NAND



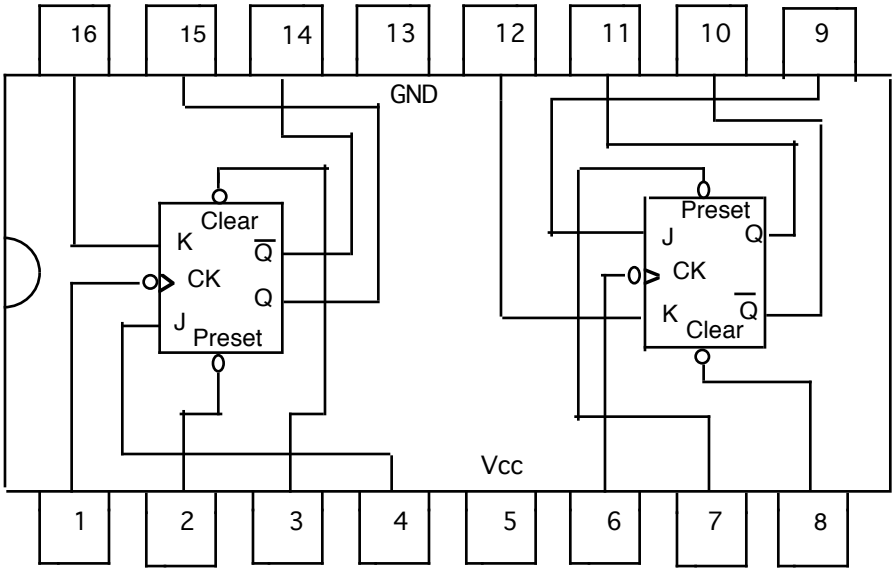
DM7420 4-input NAND



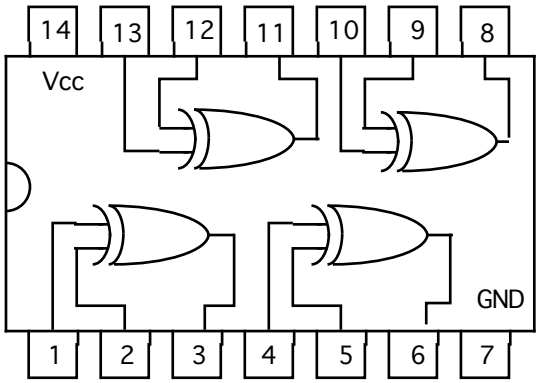
DM7474 dual D flip flop **LOGIC AND CONNECTION DIAGRAM**



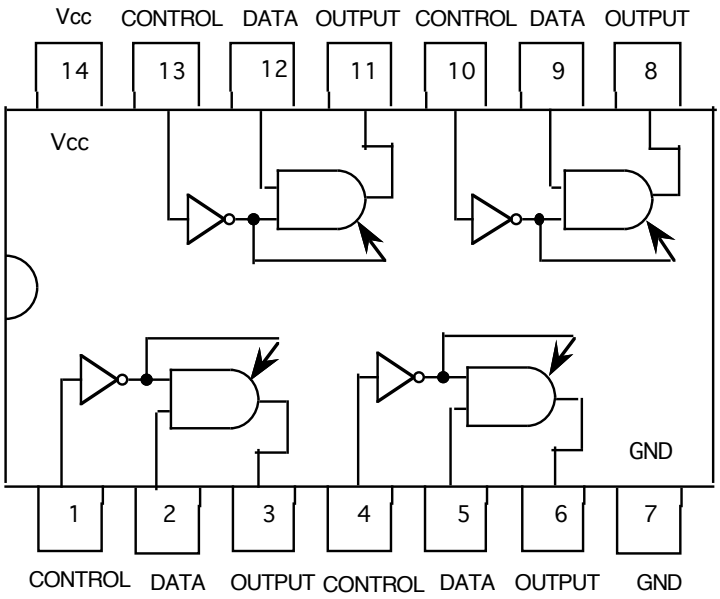
DM7476 dual JK flip flop **LOGIC AND CONNECTION DIAGRAM**



DM7486 quad 2-input EXOR **LOGIC AND CONNECTION DIAGRAM**



DM74125 tri-state quad buffer **LOGIC AND CONNECTION DIAGRAM**

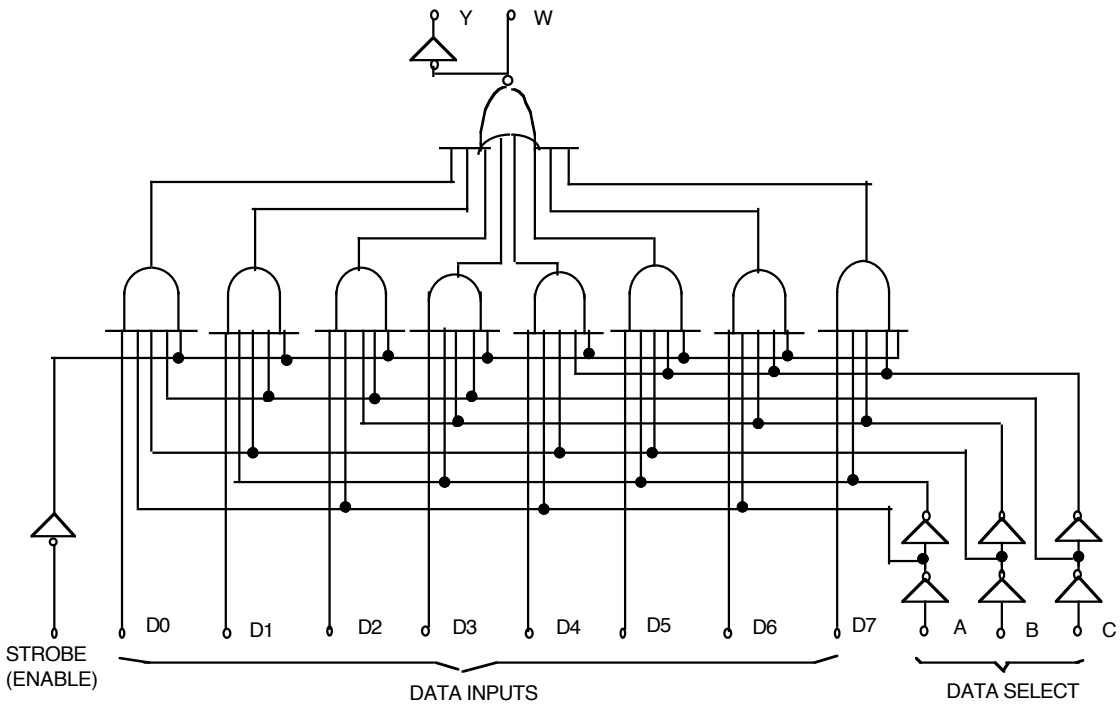


TRUTH TABLE

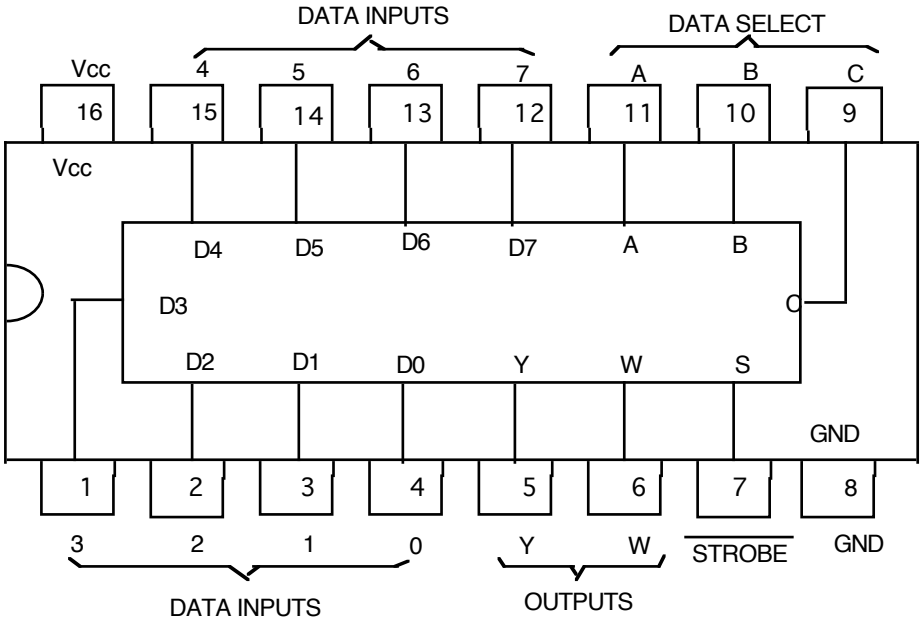
DATA	CONTROL	OUTPUT
1	O	1
0	O	0
X	1	Hi-Z

x = Irrelevant

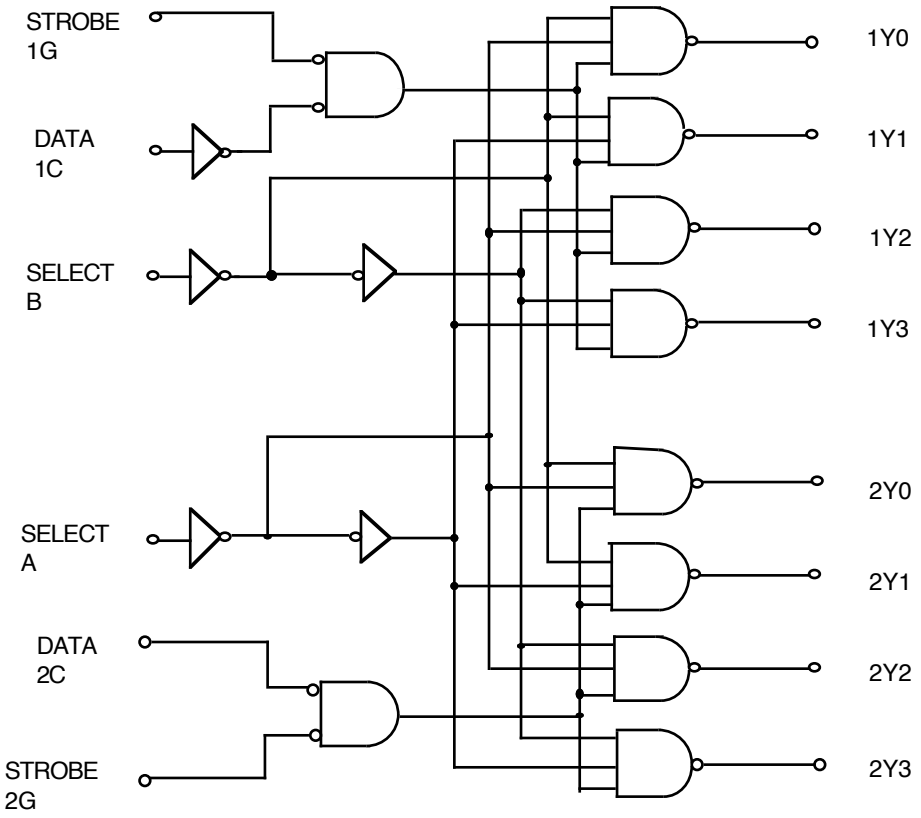
DM74151 Data selector/multiplexer **LOGIC DIAGRAM**



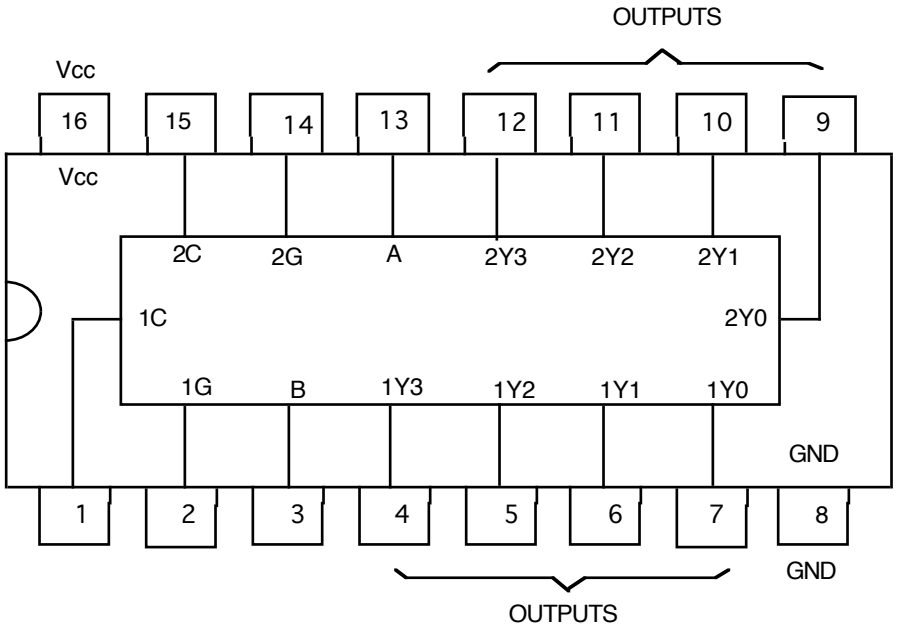
CONNECTION DIAGRAM



DM74155 dual decoder/demultiplexer **LOGIC DIAGRAM**

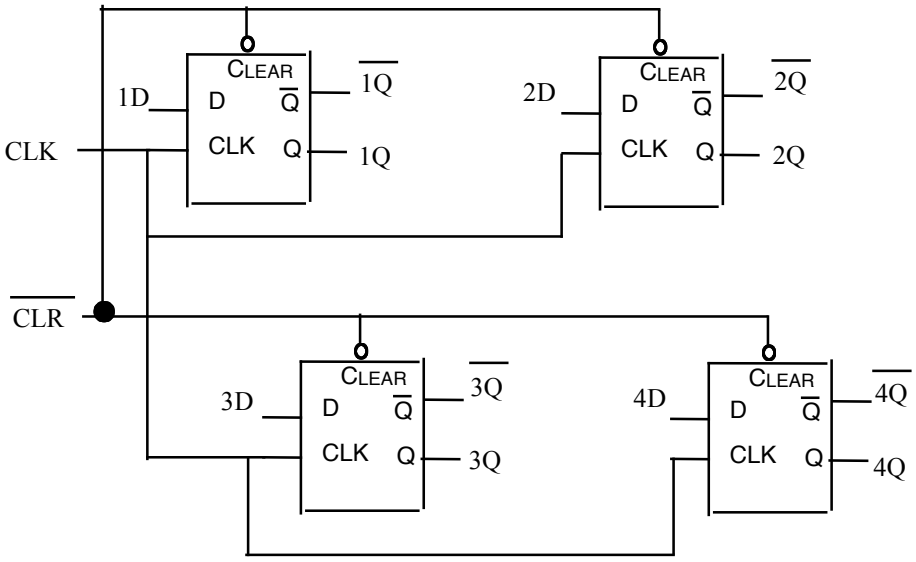


CONNECTION DIAGRAM

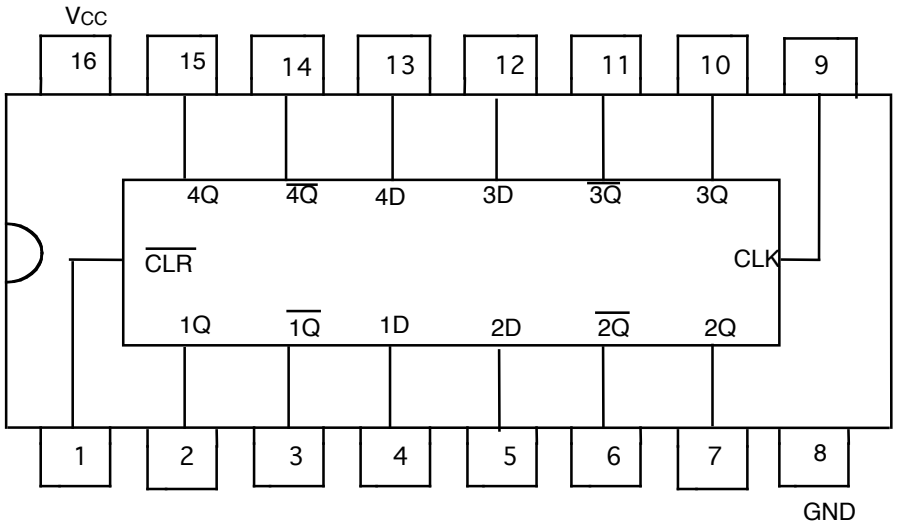


DM74175 quad D flip flop **LOGIC DIAGRAM**

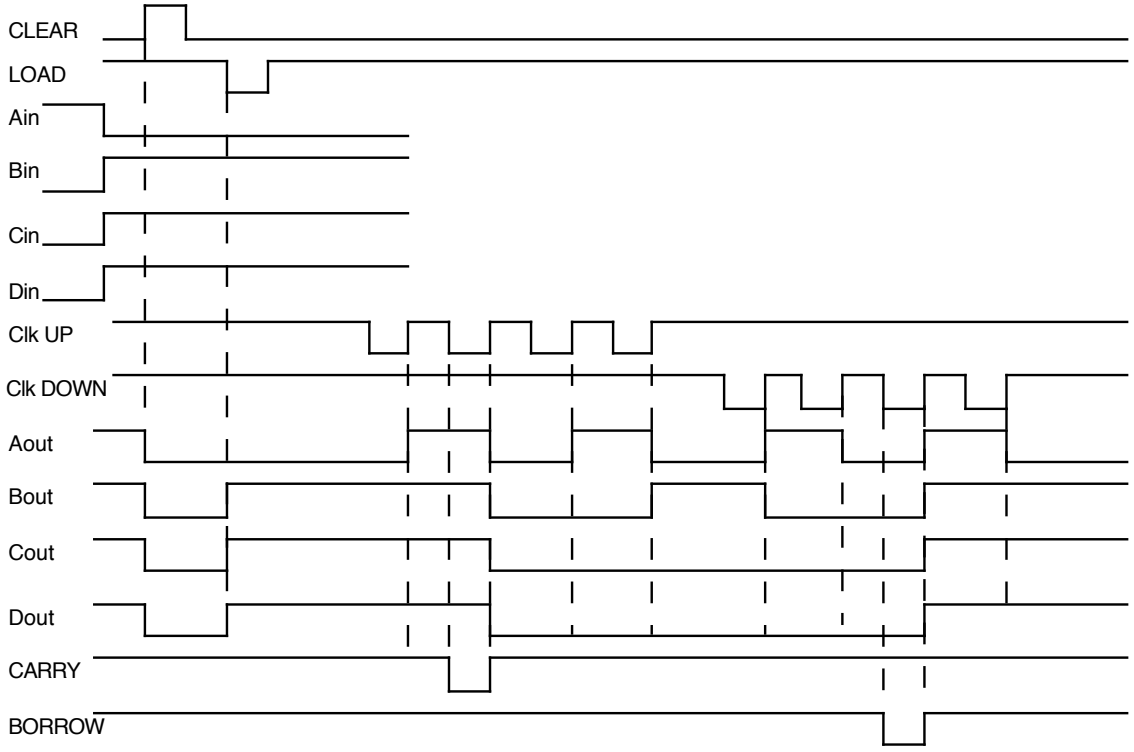
LOGIC DIAGRAM



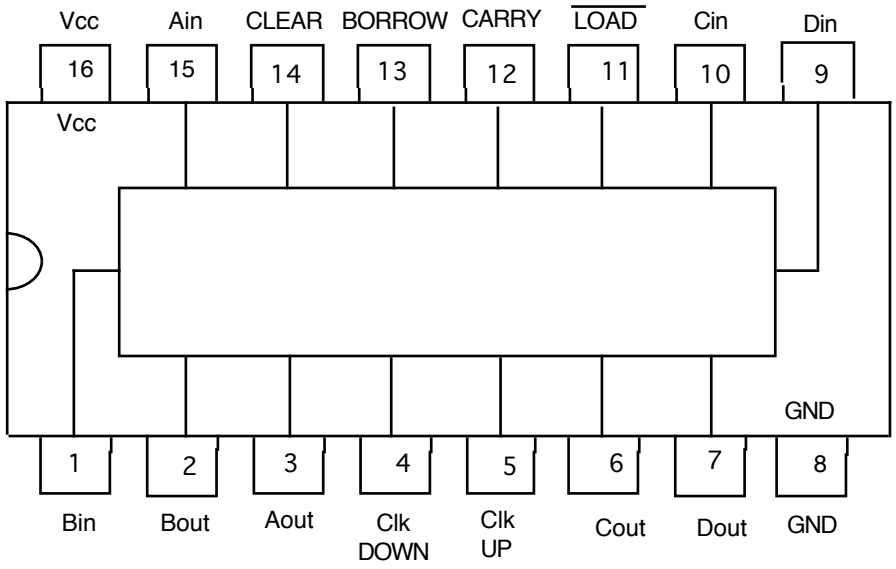
CONNECTION DIAGRAM



DM74193 up/down binary counter **LOGIC WAVEFORMS**



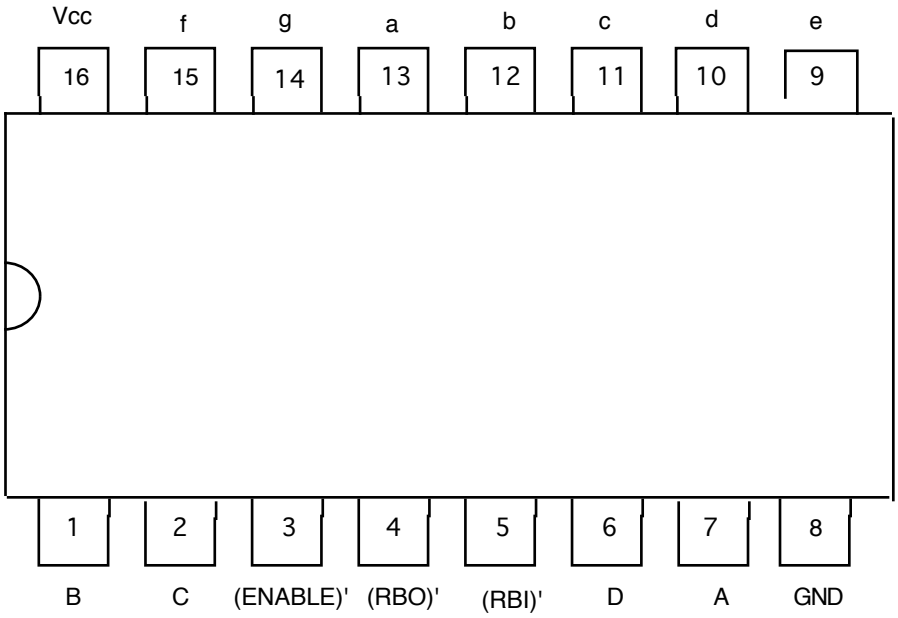
CONNECTION DIAGRAM



Notes - to count up, connect pin 4 to high and pin 5 to clock; to count down, connect pin 4 to clock and pin 5 to high. D is the most significant bit.

9368 7-Segment decoder driver

CONNECTION DIAGRAM



7-Segment display

CONNECTION DIAGRAM