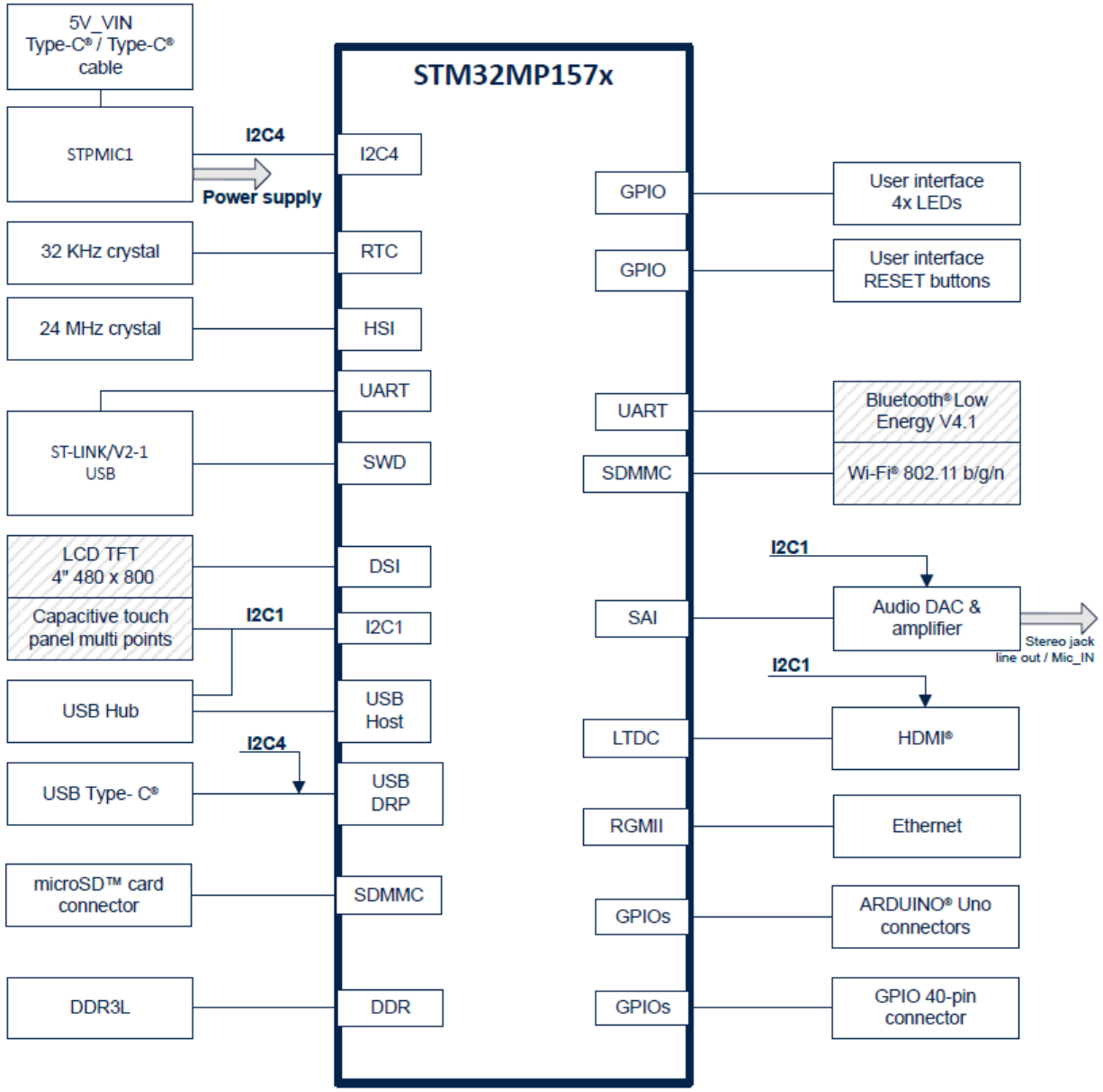
Introduction to STM32MP1

Hardware Block Diagram



Power, Reset and Clock

STM32MP1 Power Architecture

BUCK1
BUCK2
BUCK3
BUCK4
LDO1
LDO2
LDO3
LDO4
LDO5
LDO6
REFDDR

VDD_CORE
VDD_DDR
VTT_DDR
Powering PMIC system control
1V8_AUDIO
3V3_HDMI
1V2_HDMI
VDDA
VDD_USB
VREF_DDR

VDD_CORE (1.8V - 3.3V)
VDDA
VDD_USB
STM32MP1

1V8_AUDIO
Low Power Stereo codec with headphone Amplifier

VDD_DDR (1.35)
VTT_DDR
VREF_DQ_DDR
VREF_CA_DDR
DDR3L

3V3_HDMI
1V2_HDMI
HDMI Transmitter

PMIC Power supplies control registers

Regulator	Target	Output Voltage	Rated Current	Programming step	Description
BUCK1	SoC	0.725V - 1.5V	1500mA	25mV	Rail automatically turned on after 3ms
BUCK2	DDR	1V - 1.5V	1000mA	50mV	Rail won’t be turned on automatically

PMIC Power Supplies Control Registers

Register	Address	Reset value	Description
BUCKx MAIN mode control registers	0x20 to 0x23	0bXXXXXX0X	• X depends on programmed value in NVM • Used to enable or disable the buck convertors • Used to configure the mode (High power mode or Low power mode) • Used to set the output voltage
REFDDR MAIN mode control register	0x24	0x0000000X	• X depends on programmed value in NVM • Used to enable or disable the regulator
LDO[1, 2, 5, 6] MAIN mode control registers	0x25, 0x26, 0x29, 0x2A	0b0XXXXX00	• X depends on programmed value in NVM • Used to enable or disable the LDO's • Used to set the output voltage
LDO3 MAIN mode control register	0x27	0bXXXXXX00	• X depends on programmed value in NVM • Used to enable or disable the buck convertors • Used to configure the mode (Normal mode or Bypass mode) • Used to set the output voltage
LDO4 MAIN mode control register	0x28	0x0000000X	

Power controller

- There are 3 voltage rails which are available in STM32F407
  - V_{DD} → Powers everything excluding ADC
  - V_{DDA} → Powers ADC
  - V_{BAT} → powers Real time clock, RTC backup registers and backup SRAM when V_{DD} is turned off
- STM32F407 needs 1.8V – 3.6V as an input voltage
  - Internal linear voltage regulates input voltage into 1.2V

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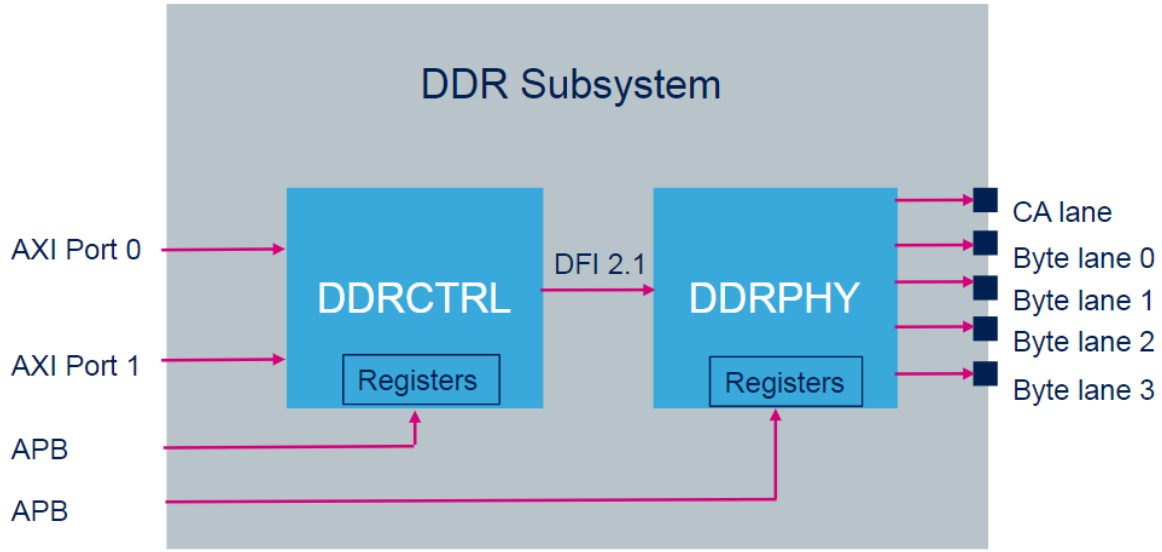
DDR Subsystem

Features of DDR Subsystem

- Supports multiple SDRAM standards → DDR3, LPDDR2, LPDDR3
- Max frequency upto 533Mhz
- Interface width can be fully populated (x32) or half populated (x16)
- Memory density limited to 1GB
- Single rank only

DDRSS Introduction

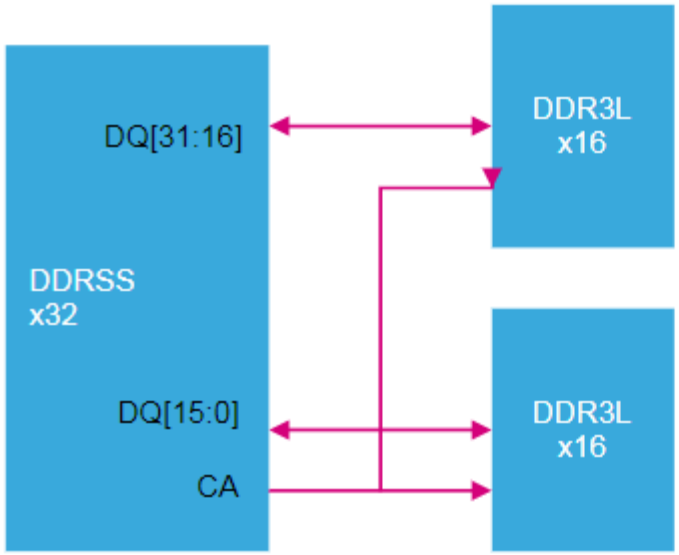
- DDRSS composed of,
  - DDR Controller
    - Does AXI port arbitration
    - Converts AXI bus transactions into SDRAM commands at the DFI interface
    - Schedule SDRAM commands according to the traffic classes (QOS) for optimal DDR utilization
    - Obey SDRAM timing requirements
    - Schedule SDRAM refreshes
    - Manage power consumption and thermals
  - DDR PHY
    - Incharge of driving Command address (CA) and write data (DQ/DQS) to SDRAM according to JDEC
    - Read data from SDRAM according to JDEC
    - Supports initialization of PHY and SDRAM



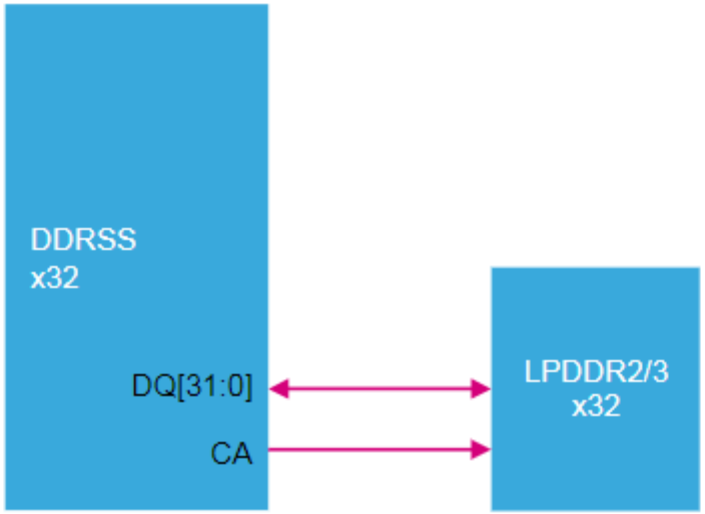
DDR PHY

- DDR PHY uses a byte lane architecture for best signal delay matching
- DDR PHY uses DLL based architecture with an,
  - MDLL → Master DLL → Command address bus
  - MSDLL → Master Slave DLL → For byte lane
- DLL's are used to,
  - Delay CK/CK# signals by 180 incase of SDR, 90 incase of DDR
  - Delay output DQS/DQS# by 90
  - Delay input DQS/DQS# by 90

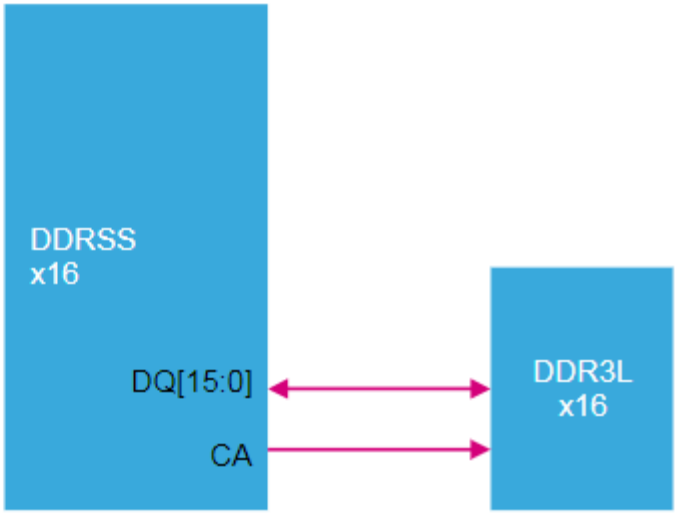
SDRAM Topology



Fly-by topology



Point 2 Point topology (x32)



Point 2 Point topology (x16)

Refresh

- Software Request Refresh
  - Set DDRCTLR_RFSHCTL3.dis_auto_refresh bit to 1. When this bit is set Memory controller internal refresh timers are disabled
  - Refresh command can be issued by setting DDRCTRL_DBGCMD.rank0_refresh to 1
  - We have to poll DDRCTRL_DBGSTAT.rank0_refresh_busy bit to check refresh was completed or not? DDRCTRL_DBGSTAT.rank0_refresh_busy == 0 means completed
- Hardware Refresh
  - Set DDRCTLR_RFSHCTL3.dis_auto_refresh bit to 0

DDRMC Registers

Register	Register Description	Offset	Reset value	Description

DDRCTRL_MSTR	DDRCTRL master register 0	0x0	0x0004 0001	• DRAM memory type
				• DRAM burst length (Minimum BL must be programmed to BL8)
				• Enable/Disable the DLL
				  • For Lower frequency operation we can disable the DLL
				  • For Higher frequency operation we have to enable the DLL
				• Data bus width (Full DQ, Half DQ, Quarter DQ)
				• Use 2T timing or 1T timing
				• Burst chop length

DDRCKMOD Control

DDRCKMOD	KERDCG	DPHYCG	Description
000	Normal	Normal	Software Self Refresh mode (SSR) MC CLK → According to clock enable bits PHY CLK → According to clock enable bits
001	Auto	Normal	Automatic Self Refresh mode (ASR1) MC CLK → MC clock enabled automatically when there is a transaction from CPU (HW Clock gating). When CPU generates a transaction through AXI bus, memory controller requests the RCC engine to enable MC clock using cactive_ddrc signal. PHY CLK → According to clock enable bits
101	Auto	Auto	Full Automatic Self Refresh mode (ASR2) MC CLK → MC clock enabled automatically when there is a transaction from CPU (HW Clock gating). When CPU generates a transaction through AXI bus, memory controller requests the RCC engine to enable MC clock using cactive_ddrc signal. PHY CLK → DDRPHYCEN must be set to 1 and DDRPHYCLPEN must be set to 0
?			Hardware Self refresh mode
?			Full Hardware Self refresh mode

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Powering PMIC system control
1V8_AUDIO
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STM32MP1
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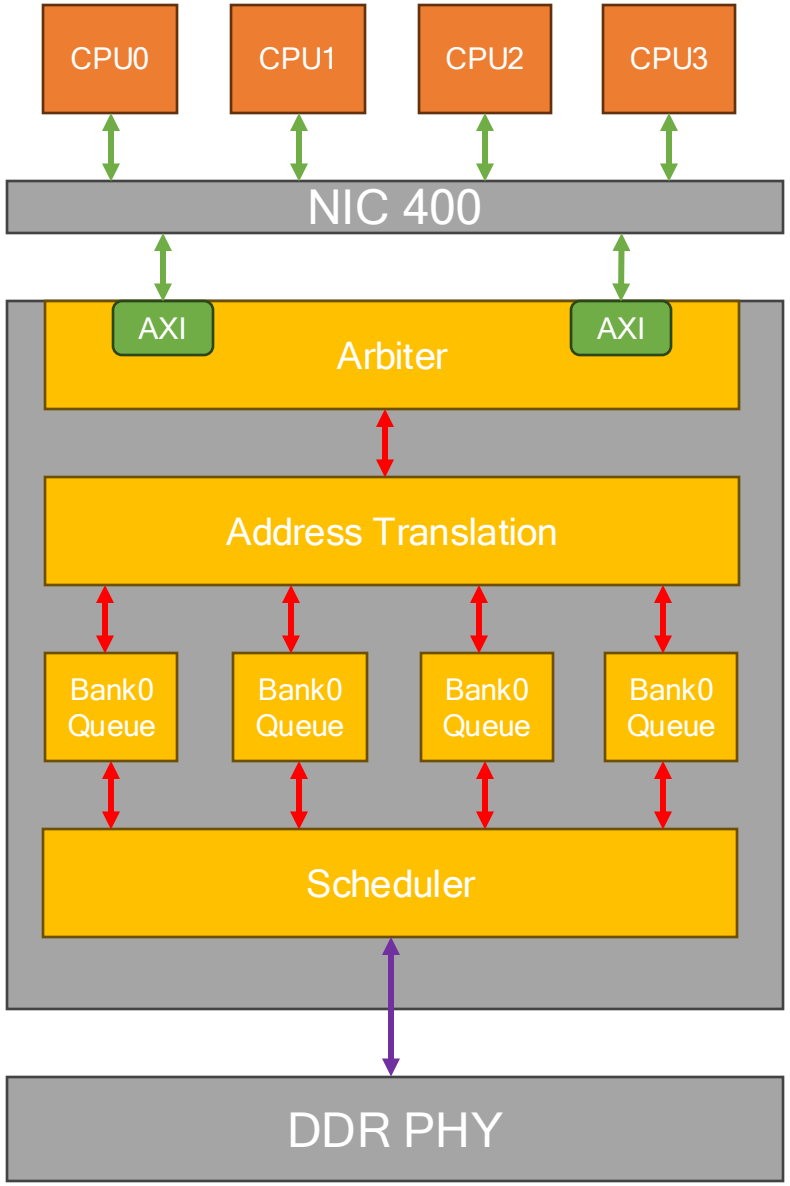
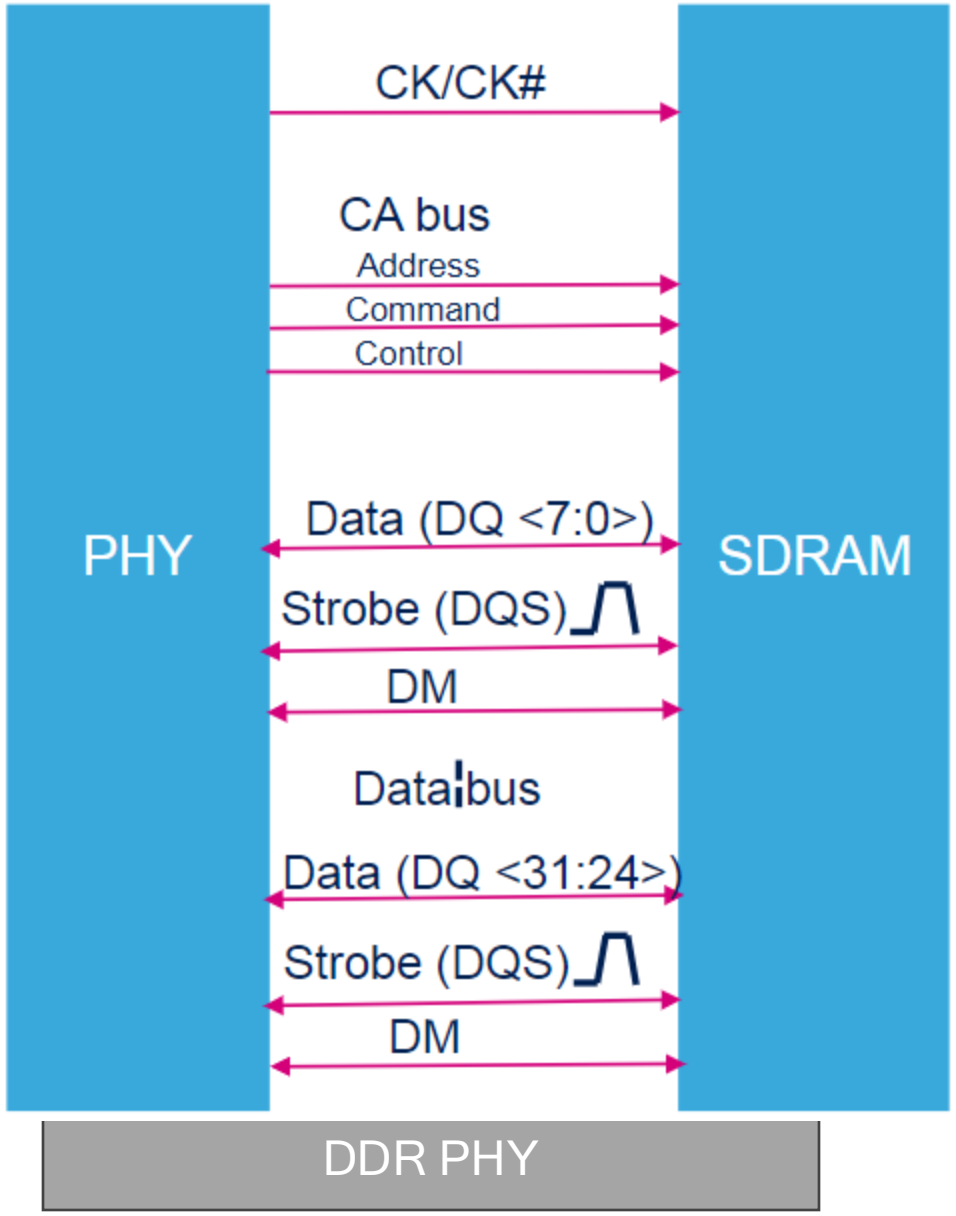
Low Power Stereo codec with headphone Amplifier
1V8_AUDIO

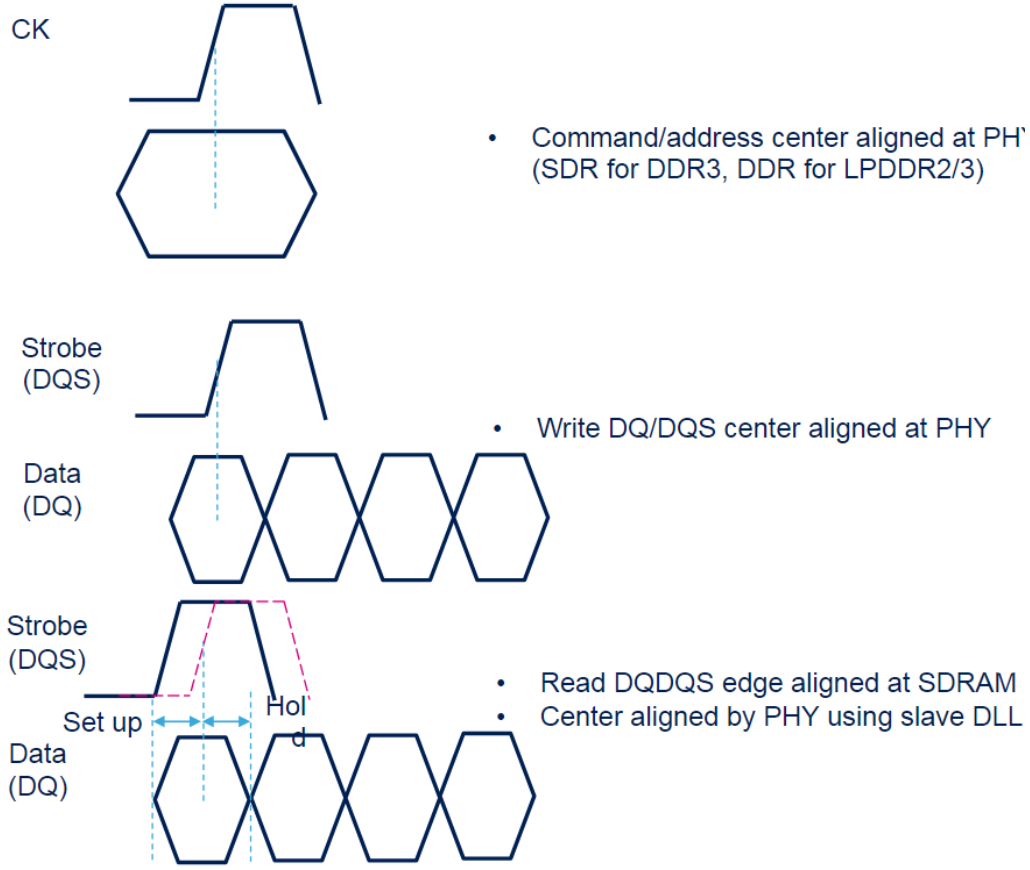
DDR3L
VDD_DDR
VTT_DDR
VREF_DQ_DDR
VREF_CA_DDR

HDMI Transmitter
3V3_HDMI
1V2_HDMI


CPU0
CPU1
CPU2
CPU3
NIC 400
AXI
AXI
Arbiter
Address Translation
Bank0 Queue
Bank0 Queue
Bank0 Queue
Bank0 Queue
Scheduler
DDR PHY

MC Block Diagram





- Command/address center aligned at PHY (SDR for DDR3, DDR for LPDDR2/3)
- Write DQ/DQS center aligned at PHY
- Read DQDQS edge aligned at SDRAM
- Center aligned by PHY using slave DLL

MC Block Diagram