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6

SystemVerilog LAB6

After completing this lab, you should be able to:

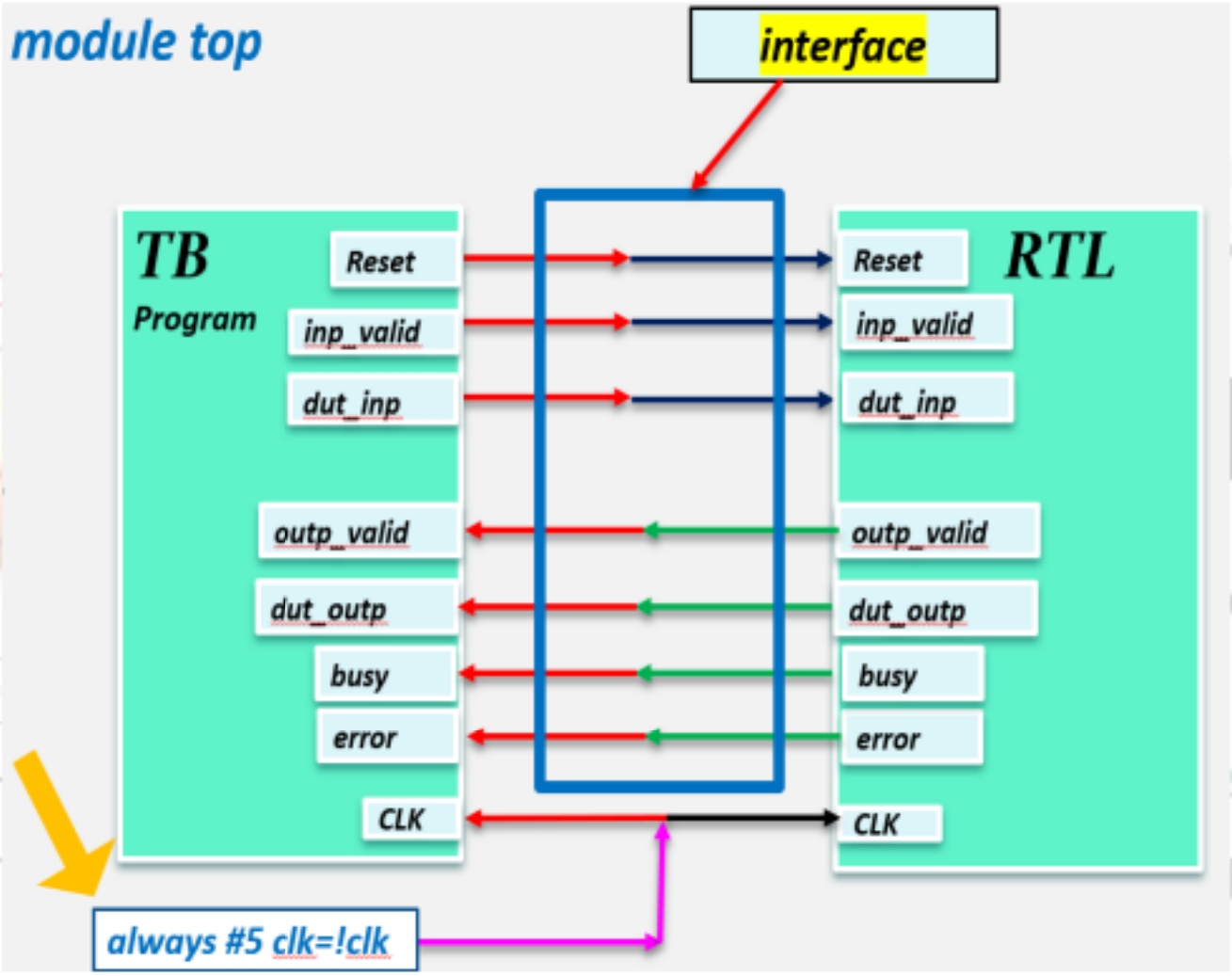
Implement interface.

Understand how to define signals in interface.

Understand how to instantiate interface inside top module.

Understand how to connect signals of interface to dut and program block.

Verify DUT behavior with the help of self-checking mechanism in program block(testbench).


module top
interface
TB
Program
Reset
inp_valid
dut_inp
outp_valid
dut_outp
busy
error
CLK
RTL
Reset
inp_valid
dut_inp
outp_valid
dut_outp
busy
error
CLK
always #5 clk=!clk

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LAB6: Use lab6 directory for this lab

Step 1: Define interface with required signals in it.

1) Open file top.sv and define interface with required signals to connect to DUT and TB.
   Refer specification to know the required signals (I/O Pins).
   Add this code in Section7 in top.sv
   Ex:

```
interface router_if ();
logic reset;
logic [7:0] dut_inp;
logic inp_valid;
.....
.....
//Define all the signals
endinterface
```


Step 2: Instantiate interface on top module.

1) Open top.sv and instantiate interface with instance name "router_if_inst".
   Add this code in Section8 in top.sv
   Ex:

```
router_if router_if_inst ();
```

Step 3: Connect interface signals to ports of DUT and TB.

1) Open top.sv and Instantiate router_dut with instance name dut_inst along with port connections.
2) Connect interface signals to DUT ports in port connection. Use name-based port mapping.
   Add this code in Section3 in top.sv

Ex:

```
router_dut  dut_inst (.clk(clk),
                      .reset(router_if_inst.reset),
                      .dut_inp(router_if_inst.dut_inp),
                      .inp_valid(router_if_inst.inp_valid),
                      //Connect rest of the ports
                      ……);
```

3) Instantiate program block with instance name tb_inst along with port connections.
4) Connect interface signals to TB ports in port connection. Use name based port mapping.
   Add this code in Section4 in top.sv

Ex:

```
testbench  tb_inst (.clk(clk),
                    .reset(router_if_inst.reset),
                    .dut_inp(router_if_inst.dut_inp),
                    .inp_valid(router_if_inst.inp_valid),
                    //Connect rest of the ports
                    ……);
```

Step 7: Run the simulation and validate the output of DUT with the results printed by self-checking mechanism.

1. Copy lab5/testbench.sv into lab6 directory and run the simulation.
2. Check the test Passed or Failed and debug the if there are any failures.