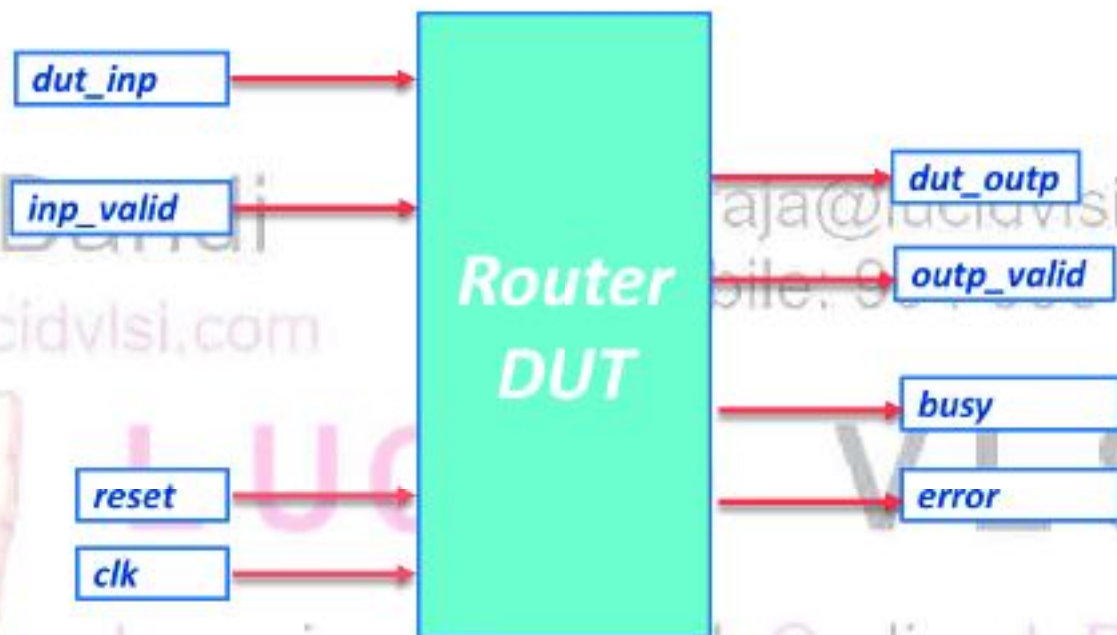




## Router DUT Specification:



**\*\*DUT supplied in the lab is strictly for testbench purpose and not synthesizable\*\***



# LUCID VLSI

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## I/O PINS:

| Pin Name          | Direction     | Size (bits) | Functionality   |
|-------------------|---------------|-------------|---|
| <i>clk</i>        | <i>input</i>  | 1           | All operations happen at posedge of clk   |
| <i>reset</i>      | <i>input</i>  | 1           | Active high, asynchronous reset pin   |
| <i>dut_inp</i>    | <i>input</i>  | 8           | Input Data pin.   |
| <i>inp_valid</i>  | <i>input</i>  | 1           | Indicates valid packet on <i>dut_inp</i><br>Value 1 indicates <i>start of packet</i> .<br>Value 0 indicates <i>end of packet</i>  |
| <i>dut_outp</i>   | <i>output</i> | 8           | Output Data pin.  |
| <i>outp_valid</i> | <i>output</i> | 1           | Indicates valid data on <i>dut_outp</i><br>Value 1 indicates <i>start of packet</i> .<br>Value 0 indicates <i>end of packet</i> .   |
| <i>busy</i>       | <i>output</i> | 1           | Indicates router availability.<br>Value 1 indicates router is busy and don't drive any packet on <i>data_inp</i> .<br>Value 0 indicates router is ready to accept the packet. |
| <i>error</i>      | <i>output</i> | 4           | Refer page 4 for full description of this pin   |



Input data port (**dut\_inp**) is 8-bit wide.

One can drive 8-bits into router per clock.

Input port **inp\_valid** indicates *start/end of packet*.

Value **high** on **inp\_valid** indicates **start of packet** and **low** indicates **end of packet**.

Output data port (**dut\_outp**) is 8-bits wide and DUT can output 8-bits per clock.

Output port **outp\_valid** will be driven by DUT and indicates *start/end of packet*.

Value **high** on **outp\_valid** indicates **start of packet** and **low** indicates **end of packet**.

Output pin **busy** indicates router availability.

Value 1 indicates router is busy and don't drive any packet on **dut\_inp**.

Value 0 indicates router is ready to accept the packet.

Minimum packet length is 12 bytes and max is 2000 bytes.

Below is the **packet format** which comes as input to dut.

RTL accepts 8-bits per clock.

| SA     | DA     | Length (length of complete packet) | CRC (of payload) | Payload         |
|--------|--------|------------------------------------|------------------|-----------------|
| 1 byte | 1 byte | 4 bytes                            | 4 bytes          | 2-to-1990 bytes |





DUT internally calculates CRC (of payload only) and if that is not matching with CRC in the received packet then *packet will be dropped*.

Output port **"error"** is a 4-bit port and indicates the error status of the router.

Below table lists the error codes and their meaning

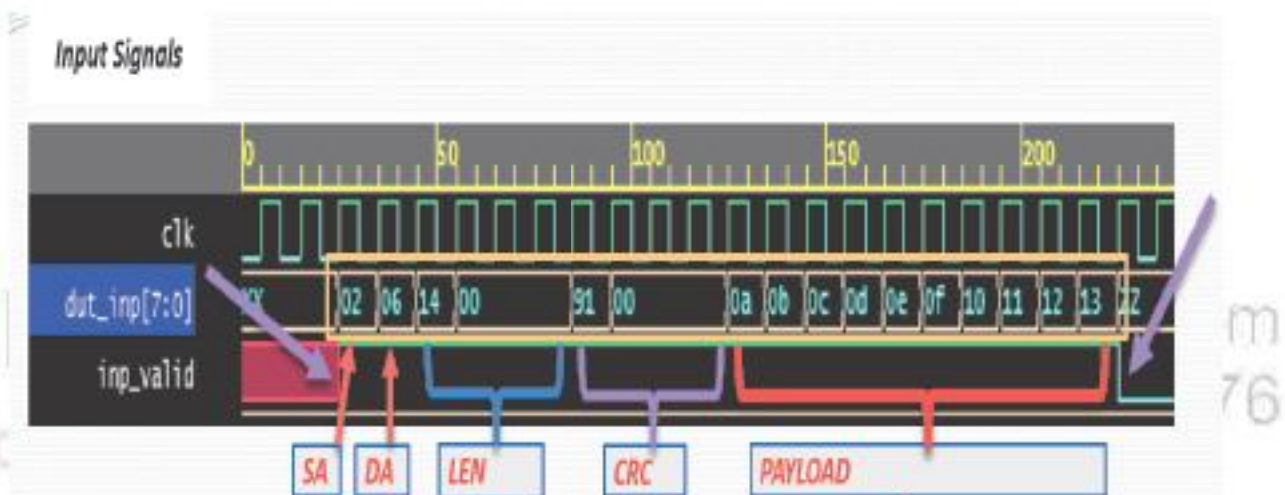
| Error code:<br>Value | Meaning   |
|----------------------|---|
| 0                    | Router Successfully processed packet.   |
| 1                    | Protocol Violation. <i>Packet driven while Router is busy.</i>  |
| 2                    | <i>Packet Dropped due to CRC mismatch.</i>  |
| 3                    | <i>Packet Dropped due to Minimum packet size mismatch.</i>  |
| 4                    | <i>Packet Dropped due to Maximum packet size mismatch.</i>  |
| 5                    | Packet Corrupted.<br>Packet dropped due to packet length mismatch.<br>Step 1: Check value of len filed of packet driven from TB<br>Step 2: Check total number of bytes received in DUT in the waveform (Check dut_inp).<br>Check value of Step 1 matching with Step 2 or not. |



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Reference input waveform:



Reference output waveform:

