HD66772

Amorphous Silicon/Low-temperature Poly-silicon TFT Panel 528-channel Source Driver with Internal RAM for 260-thousand-color Displays

(Customized specification for SAMSUNG Electronics)

REJxxxxxxx-xxxxZ
Rev.1.1-3
Oct.14.2003

Description

The HD66772 528-channel source driver LSI is used in combination with the HD66774 gate driver/power-supply IC to display 176RGB-by-240-dot graphics on TFT color LCD displays in 262,144 colors. As well as signals for amorphous silicon TFTs, the HD66772 is capable, in conjunction with the HD667P00 (power-supply IC), of outputting the signals for the control of low-temperature poly-silicon TFTs.

The HD66772's bit-operation functions, 8/9/16/18-bit high-speed bus interface, and high-speed RAM-write functions enable the efficient transfer of data and the high-speed rewriting of data in the graphics RAM. The HD66772's 6/16/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17 to 0) and VSYNC interface (system interface + VSYNC) provide interfaces for use with animated displays. These interfaces provide a window-addressing function that facilitates the construction of a display in any area of the screen and allows the simultaneous display of animated images and the contents of internal RAM without concern for the static image areas.

The HD66772 and HD66774 have various functions for reducing the power consumption of an LCD system. The HD66772 features low-voltage operation (1.8 V min.) and an internal RAM from which it is able to drive a maximum of 176RGB-by-240-dot color images, while the HD66774 features an interface to drive the 240 TFT gate lines and voltage-followers to generate the LCD-driving voltage. Since the HD66772 incorporates a circuit that interfaces with the HD66774, it is capable of setting instructions for the HD66774. The device supports functions such as an eight-color display function and standby and sleep modes that allow precise power control by software. This LSI is suitable for any medium-sized or small portable product that is battery driven and requires a long battery life, such as digital cellular phones that support a WWW browser and small PDAs.

Features

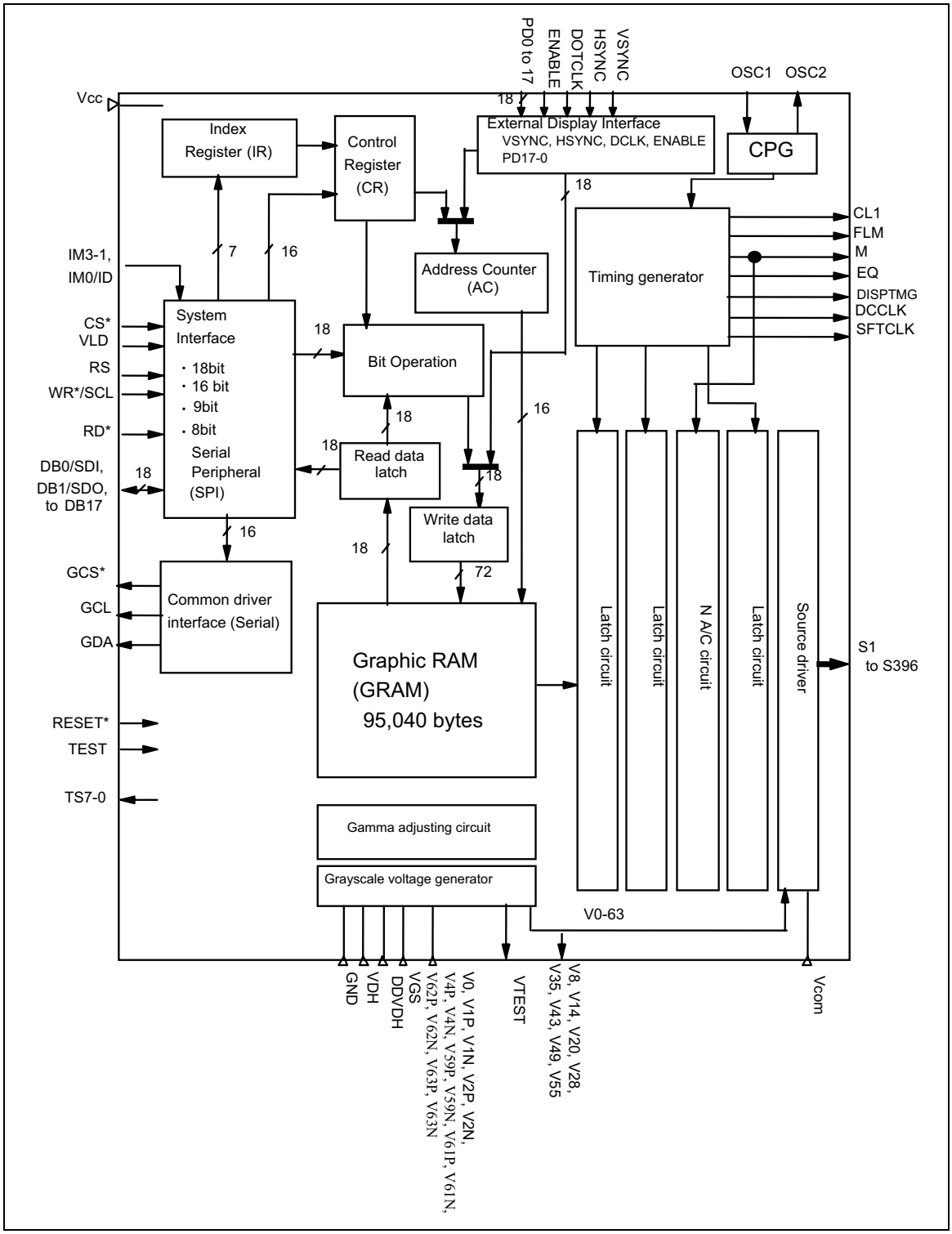
- 176RGB x 240-dot graphics display LCD controller/driver for 262,144 TFT colors (when used with the HD66774)
- Control signals for the low-temperature poly-silicon TFT-panel compatible gate driver (HD66772 + HD667P00)
- System interfaces
  - 8-/9-/16-/18-bit high-speed bus interface
  - Serial peripheral interface (SPI)
- Interfaces for use with animated displays
  - 6-/8-/18-bit RGB-I/F (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17 to 0)
  - VSYNC-I/F (system I/F + VSYNC)
- High-speed burst-RAM write function
- A window-addressing function allows writing to the set of addresses in RAM that correspond to a window's shape.
  - The interfaces for animated displays facilitate the placing of animated pictures in any area of the screen.
  - Selective transmission to the animated-display area reduces the amount of data transmitted.
  - The contents of internal RAM may be displayed at the same time as the animated display.
- Bit-operations for graphics processing:
  - Write data mask function in bit units
  - Logical operations and conditional writing in units of pixels
- Various functions for controlling color displays:
  - Simultaneous availability of 262,144 colors (γ-correction function)
  - Vertical scrolling in raster-row units
- Features for low-power operation include:
  - Vcc = 1.8 to 3.3 V (low-voltage range)
  - DDVDH = 4.5 to 5.5 V (liquid-crystal driving voltage)
  - Power-save functions such as the standby and sleep modes
  - Partial LCD drive that displays two sub-screens in any position
  - Maximum 12-times step-up circuit for the liquid-crystal driving voltage (HD66774)
  - Voltage followers to decrease the flow of direct current in the LCD drive's bleeder-resistors (HD66774)
- Built-in circuit for interfacing with the HD66774 gate-driver/power-supply IC
- Maximum 176RGB-by-240-dot display in combination with the HD66774 gate-driver/power-supply IC
- 95,040 bytes of internal RAM
- 528-output liquid-crystal display driver
- n-raster-row AC liquid-crystal drive (can be set to a different polarity each line)

- Internal oscillation and hardware reset
- Reversible direction for the feeding of signals from RAM to the source driver

Type Numbers

Type Number	External Appearance
HD667A72BP	Die with gold bump (straight output arrangement)
HD667B72BP	Die with gold bump (laced output arrangement)

Block diagram



Pin Function

Table 1

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM3-1, IM0/ID</td><td>3</td><td>I</td><td>GND or V_{CC}</td><td>Settings select the MPU-interface mode as listed below.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>Setting disabled</td><td></td></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>Vcc</td><td>Setting disabled</td><td></td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>GND</td><td>80-system 16-bit interface</td><td>DB17 to 10 and 8 to 1</td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 8-bit interface</td><td>DB17 to 10</td></tr>
<tr><td>GND</td><td>Vcc</td><td>GND</td><td>ID</td><td>Clocked serial peripheral interface (SPI)</td><td>DB1 to 0</td></tr>
<tr><td>GND</td><td>Vcc</td><td>Vcc</td><td>*</td><td>Setting disabled</td><td></td></tr>
<tr><td>Vcc</td><td>GND</td><td>GND</td><td>GND</td><td>Setting disabled</td><td></td></tr>
<tr><td>Vcc</td><td>GND</td><td>GND</td><td>Vcc</td><td>Setting disabled</td><td></td></tr>
<tr><td>Vcc</td><td>GND</td><td>Vcc</td><td>GND</td><td>80-system 18-bit interface</td><td>DB17 to 0</td></tr>
<tr><td>Vcc</td><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 9-bit interface</td><td>DB17 to 9</td></tr>
<tr><td>Vcc</td><td>Vcc</td><td>*</td><td>*</td><td>Setting disabled</td><td></td></tr>
</table>
When the serial interface is selected, the IM0 pin is used to set the ID code for the device.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Selects the HD66772:
Low: the HD66772 is selected and is accessible
High: HD66772 is not selected and is inaccessible
Must be fixed to the GND level when not in use.</td></tr>
<tr><td>VLD</td><td>1</td><td>I</td><td>MPU</td><td>Indicates whether or not the data is valid when writing to the RAM.
Low: Valid (Writing data to RAM)
High: Invalid (Not writing data to RAM)
The RAM address will be updated whether VLD is high or low.
Must be fixed to the GND level when not in use.
This signal remains available when an external display interface is in use.
<table>
<tr><th>CS</th><th>VLD</th><th>RAM Write</th><th>RAM Address</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>1</td><td>*</td><td>Invalid</td><td>Hold</td></tr>
</table></td></tr>
</table>

Signals	Number of Pins	I/O	Connected to	Functions
RS	1	I	MPU	Selects the register. Low: Index/status High: Control Fix to the “Vcc” or “GND” level while using SPI.
WR*/SCL	1	I	MPU	For an 80-system bus interface, serves as a write strobe signal. Data is written on this signal’s low level. For a synchronous clock interface, serves as the synchronous clock signal.
RD*	1	I	MPU	For an 80-system bus interface, serves as a read-strobe signal. Data is read on this signal’s low level. Fix to the “Vcc” or “GND” level while using SPI.
DB0/SDI	1	I/O	MPU	Serves as an I/O line in data transfer via an 18-bit parallel bidirectional data bus. The following pins are used in parallel transfer. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and DB8-DB1 18-bit bus: DB17-DB0 Unused pins must be fixed to the Vcc or GND level. Serves as the serial data input pin (SDI) of a clock-synchronous serial interface. The input level is read on the rising edge of the SCL signal.
DB1/SDO	1	I/O	MCU	Serves as an I/O line in data transfer via a 18-bit parallel bidirectional data bus. The following pins are used in parallel transfer. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and 8 to 1 18-bit bus: DB17-DB0 Unused pins must be fixed to the Vcc or GND level. Serves as the serial data output pin (SDO) of a clock-synchronous serial interface. Output is from the falling edge of the SCL signal.
DB2-DB17	16	I/O	MPU	Serve as pins for a bidirectional and parallel data bus. The following pins are used in parallel transfer. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and 8 to 1 18-bit bus: DB17-DB0 Unused pins must be fixed to the Vcc or GND level.

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>Indicates whether or not RAM data is valid when the RGB interface is in use.
Low: Selected (access enabled)
High: Not selected (access disabled)
Must be fixed to the Vcc level when not in use.
According to the setting of EPL resister, EVABLE signals reverse its polarity.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>LVD</th><th>RAM Write</th><th>RAM Address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
</table></td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Frame synchronization signal
This signal is active low.
Must be fixed at the Vcc level when not in use.</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Raster-row synchronization signal
This signal is active low.
Must be fixed at the Vcc level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU</td><td>Dot-clock signal
This signal is active low. Data is read on its falling edge.
Must be fixed at the Vcc level when not in use.</td></tr>
<tr><td>PD0–PD17</td><td>18</td><td>I</td><td>MPU</td><td>Serves as a 18-bit bus for RGB data. The following pins are used in transfer on this bus.
6-bit bus: DB17-DB12
16-bit bus: DB17-DB13 and 11 to 1
18-bit bus: DB17-DB0
Must be fixed unused pins to the Vcc or GND level.</td></tr>
<tr><td>S1–S528</td><td>528</td><td>O</td><td>LCD</td><td>Outputs voltages for supply to the LCD.
The SS bit can change the direction with which segment signals are obtained from RAM. For example, if SS = 0, the data at RAM address 0000 is output on S1. If SS = 1, it is output on S528.
S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).</td></tr>
<tr><td>CL1</td><td>1</td><td>O</td><td>HD66774</td><td>The one-raster-row-cycle pulse is output.
*Connect either right or left terminal of a chip. Set unused pins open.</td></tr>
<tr><td>M</td><td>1</td><td>O</td><td>HD66774</td><td>Output for the AC-cycle signal.
*Connect either right or left terminal of a chip. Set unused pins open.</td></tr>
<tr><td>FLM</td><td>1</td><td>O</td><td>HD66774</td><td>Output for the frame-start pulse.
*Connect either right or left terminal of a chip. Set unused pins open.</td></tr>
</table>

Signals	Number of Pins	I/O	Connected to	Functions
EQ	1	O	HD66774	Indicates setting of the Vcom output to its high-impedance state during transitions of Vcom when Vcom is being AC-cycled. Low: VcomH or VcomL is being output on the Vcom pin. High: Vcom pin is in high-impedance state. *Connect either right or left terminal of a chip. Set unused pins open.
DISPTMG	1	O	HD66774	Gate-off signal during the partial display. Low: Outputs Voff signal. High: Outputs normal signal. *Connect either right or left terminal of a chip. Set unused pins open.
DCCLK	1	O	HD66774	Outputs the clock signal for the step-up circuit. *Connect either right or left terminal of a chip. Set unused pins open.
SFTCLK	1	O	HD66774	The one-raster-row-cycle pulse is output. *Connect either right or left terminal of a chip. Set unused pins open.
GCL	1	O	HD66774	Clock signal for the serial transfer of register settings to the gate-driver/power-supply IC. Data is output on the falling edges of this signal. *Connect either right or left terminal of a chip. Set unused pins open.
GDA	1	O	HD66774	Data signal for the serial transfer of register settings to the gate-driver/power-supply IC. *Connect either right or left terminal of a chip. Set unused pins open.
GCS*	1	O	HD66774	Chip-select signal for the HD66772. Low: the HD66772 is selected and can receive serially transferred data. High: the HD66772 is not selected and cannot receive serially transferred data. *Connect either right or left terminal of a chip. Set unused pins open.
DDVDH	1	I	HD66774	Input for the LCD-driving voltage, which can be provided by the HD66774. VDH (max.) ≤ DDVDH - 0.5 V
VDH	1	I	HD66774	Reference level for grayscale voltage generation circuit, which can be provided by the HD66774. VDH (max.): DDVDH-0.5V.
Vcom	1	I	HD66774	Signal for the equalizer functions All LCD outputs (S1-S528) are shorted to the Vcom level (high-impedance). When VcomL is lower than 0 V, this signal should not be connected.
V_{CC}, GND	2	—	Power supply	V_{CC}: + 1.8 V to + 3.3 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Resistor for the oscillator	For connecting an external resistor for R-C oscillation. An external clock signal should be supplied through OSC1 with OSC2 open-circuit.

Signals	Number of Pins	I/O	Connected to	Functions
RESET1* RESET2*	1	I	MPU or external R-C circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. Input data through RESET1 or RESET2. Unused pins should not be connected.
VccDUM		O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM		O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy1,4, 19,20	4	—	—	Dummy pad. Must be left disconnected.
Dummy5-18 Dummy21-34	28	—	—	Dummy pad. Can be connected to COG panel wiring.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
V0, V1P, V2P, V4P, V59P, V61P, V62P, and V63P	8	I or O	Stabilizing capacitor	Internal op-amp outputs that produce a positive polarity (V0 can be used for both polarities) when the internal op-amp is on (SAP2-0 ="001", "010", "001", "100", or "101"). For connection to stabilizing capacitors.
V1N, V2N, V4N, V59N, V61N, V62N, and V63N	7	I or O	Stabilizing capacitor	Internal op-amp outputs that produce a negative polarity when the internal op-amp is on (SAP2-0 ="001", "010", "001", "100", or "101"). For connection to stabilizing capacitors.
V8, V14, V20, V28, V35, V43, V49, and V55	8	O	Open	Test pins. Must not be connected.
VGS	1	I	GND or External resistor	Reference level for the grayscale-voltage generation circuit. For connection to a variable resistor that adjusts the source-driver level for a panel.
VTEST	1	O	Open	Test pin. Must not be connected.
TS0-TS7	8	O	Open	Test pins. Must not be connected.

Patents of dummy pin which is used to fix pin to VCC or GND are pending and granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484
Korean Application No. 19997002322
Taiwanese Application No.086103756
(PCT/JP96/02728(W098/12597)

■HD667A72 Pad Assignment (Straight)

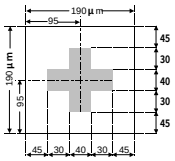
-Chip size: 17.84mm x R7.17mm
-Chip thickness: 400μm(typ.)
-Pad coordinate: Pad center
-Pad Origin: Chip center

Au bump size:
(1) 80μm×80μm
DUMMY1(NO.1),RESET1(No.2)～TS7(NO.148),
DUMMY2(NO.149)～DUMMY4(NO.151),
DUMMY19(NO.216),DUMMY20(NO.645)
(2) 25μm×140μm
S51(NO.644)～S478(NO.217)

(3) 140μm×25μm
S1(NO.696)～S50(NO.646),S528(NO.166)～S479(NO.215),
DUMMY5(NO.152)～DUMMY18(NO.165),
DUMMY21(NO.697)～DUMMY34(NO.710)

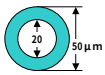
-Au bump pitch: Refer to the PAD coordinate
-Au bump hight: 15μm(typ.)

the PAD coordinate.
Alignment Mark
(1)Assign two points
coordinate (X, Y) = (±8647.0, -1404.0)

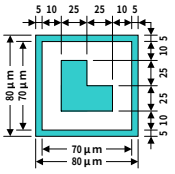


(2－a) coordinate (X, Y) = (-8787.9, 1350)

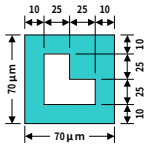
(2－b) coordinate (X, Y) = (8787.9, 1350)



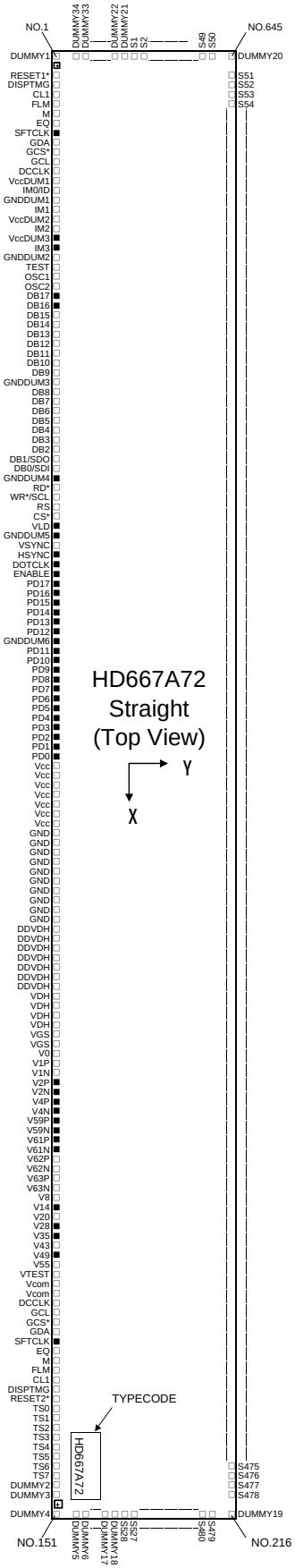
(3－a) coordinate (X, Y) = (-8658, 1452.9)



(3－b) coordinate (X, Y) = (8658, 1452.9)



■New assignment pad from 770 in I/O part



PAD Coordinate (Straight)

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-8788	-1453	81	GND	82	-1453	161	DUMMY14	8750	-900	241	SI54	7580	1415	321	SI74	4380	1415
2	RESET1 *	-8474	-1453	82	GND	182	-1453	162	DUMMY15	8750	-860	242	SI53	7540	1415	322	SI73	4340	1415
3	DISPTMG	-8339	-1453	83	GND	282	-1453	163	DUMMY16	8750	-820	243	SI52	7500	1415	323	SI72	4300	1415
4	CL1	-8204	-1453	84	GND	382	-1453	164	DUMMY17	8750	-780	244	SI51	7460	1415	324	SI71	4260	1415
5	FLM	-8069	-1453	85	GND	482	-1453	165	DUMMY18	8750	-740	245	SI50	7420	1415	325	SI70	4220	1415
6	M	-7934	-1453	86	GND	582	-1453	166	SI28	8750	-700	246	SI49	7380	1415	326	SI69	4180	1415
7	EQ	-7799	-1453	87	GND	682	-1453	167	SI27	8750	-660	247	SI48	7340	1415	327	SI68	4140	1415
8	SFTCLK	-7664	-1453	88	GND	782	-1453	168	SI26	8750	-620	248	SI47	7300	1415	328	SI67	4100	1415
9	GDA	-7529	-1453	89	GND	882	-1453	169	SI25	8750	-580	249	SI46	7260	1415	329	SI66	4060	1415
10	GCS*	-7394	-1453	90	GND	982	-1453	170	SI24	8750	-540	250	SI45	7220	1415	330	SI65	4020	1415
11	GCL	-7259	-1453	91	DDVDH	1133	-1453	171	SI23	8750	-500	251	SI44	7180	1415	331	SI64	3980	1415
12	DCCLK	-7124	-1453	92	DDVDH	1233	-1453	172	SI22	8750	-460	252	SI43	7140	1415	332	SI63	3940	1415
13	VCCDUM1	-6974	-1453	93	DDVDH	1333	-1453	173	SI21	8750	-420	253	SI42	7100	1415	333	SI62	3900	1415
14	M0/ D	-6874	-1453	94	DDVDH	1433	-1453	174	SI20	8750	-380	254	SI41	7060	1415	334	SI61	3860	1415
15	GNDDUM1	-6774	-1453	95	DDVDH	1533	-1453	175	SI19	8750	-340	255	SI40	7020	1415	335	SI60	3820	1415
16	M1	-6674	-1453	96	DDVDH	1633	-1453	176	SI18	8750	-300	256	SI39	6980	1415	336	SI59	3780	1415
17	VCCDUM2	-6574	-1453	97	DDVDH	1733	-1453	177	SI17	8750	-260	257	SI38	6940	1415	337	SI58	3740	1415
18	M2	-6474	-1453	98	VDH	1883	-1453	178	SI16	8750	-220	258	SI37	6900	1415	338	SI57	3700	1415
19	VCCDUM3	-6373	-1453	99	VDH	1983	-1453	179	SI15	8750	-180	259	SI36	6860	1415	339	SI56	3660	1415
20	M3	-6273	-1453	100	VDH	2083	-1453	180	SI14	8750	-140	260	SI35	6820	1415	340	SI55	3620	1415
21	GNDDUM2	-6173	-1453	101	VDH	2183	-1453	181	SI13	8750	-100	261	SI34	6780	1415	341	SI54	3580	1415
22	TEST	-6073	-1453	102	VGS	2334	-1453	182	SI12	8750	-60	262	SI33	6740	1415	342	SI53	3540	1415
23	OSC1	-5923	-1453	103	VGS	2434	-1453	183	SI11	8750	-20	263	SI32	6700	1415	343	SI52	3500	1415
24	OSC2	-5773	-1453	104	V0	2584	-1453	184	SI10	8750	20	264	SI31	6660	1415	344	SI51	3460	1415
25	DB17	-5623	-1453	105	V1 P	2734	-1453	185	SI09	8750	60	265	SI30	6620	1415	345	SI50	3420	1415
26	DB16	-5523	-1453	106	V1 N	2884	-1453	186	SI08	8750	100	266	SI29	6580	1415	346	SI49	3380	1415
27	DB15	-5423	-1453	107	V2 P	3034	-1453	187	SI07	8750	140	267	SI28	6540	1415	347	SI48	3340	1415
28	DB14	-5323	-1453	108	V2 N	3184	-1453	188	SI06	8750	180	268	SI27	6500	1415	348	SI47	3300	1415
29	DB13	-5223	-1453	109	V4 P	3334	-1453	189	SI05	8750	220	269	SI26	6460	1415	349	SI46	3260	1415
30	DB12	-5122	-1453	110	V4 N	3484	-1453	190	SI04	8750	260	270	SI25	6420	1415	350	SI45	3220	1415
31	DB11	-5022	-1453	111	V59 P	3635	-1453	191	SI03	8750	300	271	SI24	6380	1415	351	SI44	3180	1415
32	DB10	-4922	-1453	112	V59 N	3785	-1453	192	SI02	8750	340	272	SI23	6340	1415	352	SI43	3140	1415
33	DB9	-4822	-1453	113	V61 P	3935	-1453	193	SI01	8750	380	273	SI22	6300	1415	353	SI42	3100	1415
34	GNDDUM3	-4722	-1453	114	V61 N	4085	-1453	194	SI00	8750	420	274	SI21	6260	1415	354	SI41	3060	1415
35	DB8	-4622	-1453	115	V62 P	4235	-1453	195	SI99	8750	460	275	SI20	6220	1415	355	SI40	3020	1415
36	DB7	-4522	-1453	116	V62 N	4385	-1453	196	SI98	8750	500	276	SI19	6180	1415	356	SI39	2980	1415
37	DB6	-4422	-1453	117	V63 P	4535	-1453	197	SI97	8750	540	277	SI18	6140	1415	357	SI38	2940	1415
38	DB5	-4322	-1453	118	V63 N	4685	-1453	198	SI96	8750	580	278	SI17	6100	1415	358	SI37	2900	1415
39	DB4	-4222	-1453	119	V8	4836	-1453	199	SI95	8750	620	279	SI16	6060	1415	359	SI36	2860	1415
40	DB3	-4122	-1453	120	V14	4936	-1453	200	SI94	8750	660	280	SI15	6020	1415	360	SI35	2820	1415
41	DB2	-4022	-1453	121	V20	5036	-1453	201	SI93	8750	700	281	SI14	5980	1415	361	SI34	2780	1415
42	DB1/ SDO	-3921	-1453	122	V28	5136	-1453	202	SI92	8750	740	282	SI13	5940	1415	362	SI33	2740	1415
43	DB0/ SDI	-3821	-1453	123	V35	5236	-1453	203	SI91	8750	780	283	SI12	5900	1415	363	SI32	2700	1415
44	GNDDUM4	-3721	-1453	124	V43	5336	-1453	204	SI90	8750	820	284	SI11	5860	1415	364	SI31	2660	1415
45	RD*	-3621	-1453	125	V49	5436	-1453	205	SI89	8750	860	285	SI10	5820	1415	365	SI30	2620	1415
46	WR*/ SCL	-3521	-1453	126	V55	5536	-1453	206	SI88	8750	900	286	SI09	5780	1415	366	SI29	2580	1415
47	RS	-3421	-1453	127	VTEST	5636	-1453	207	SI87	8750	940	287	SI08	5740	1415	367	SI28	2540	1415
48	CS*	-3321	-1453	128	VCOM	5786	-1453	208	SI86	8750	980	288	SI07	5700	1415	368	SI27	2500	1415
49	VLD	-3221	-1453	129	VCOM	5886	-1453	209	SI85	8750	1020	289	SI06	5660	1415	369	SI26	2460	1415
50	GNDDUM5	-3121	-1453	130	DCCLK	6036	-1453	210	SI84	8750	1060	290	SI05	5620	1415	370	SI25	2420	1415
51	VSYNC	-3021	-1453	131	GCL	6171	-1453	211	SI83	8750	1100	291	SI04	5580	1415	371	SI24	2380	1415
52	HSYNC	-2921	-1453	132	GCS*	6306	-1453	212	SI82	8750	1140	292	SI03	5540	1415	372	SI23	2340	1415
53	DOTCLK	-2821	-1453	133	GDA	6441	-1453	213	SI81	8750	1180	293	SI02	5500	1415	373	SI22	2300	1415
54	ENABLE	-2721	-1453	134	SFTCLK	6576	-1453	214	SI80	8750	1220	294	SI01	5460	1415	374	SI21	2260	1415
55	PD17	-2620	-1453	135	EQ	6711	-1453	215	SI79	8750	1260	295	SI00	5420	1415	375	SI20	2220	1415
56	PD16	-2520	-1453	136	M	6846	-1453	216	DUMMY19	8788	1453	296	SI99	5380	1415	376	SI19	2180	1415
57	PD15	-2420	-1453	137	FLM	6981	-1453	217	SI78	8540	1415	297	SI98	5340	1415	377	SI18	2140	1415
58	PD14	-2320	-1453	138	CL1	7116	-1453	218	SI77	8500	1415	298	SI97	5300	1415	378	SI17	2100	1415
59	PD13	-2220	-1453	139	DISPTMG	7251	-1453	219	SI76	8460	1415	299	SI96	5260	1415	379	SI16	2060	1415
60	PD12	-2120	-1453	140	RESET2 *	7386	-1453	220	SI75	8420	1415	300	SI95	5220	1415	380	SI15	2020	1415
61	GNDDUM6	-2020	-1453	141	TS0	7537	-1453	221	SI74	8380	1415	301	SI94	5180	1415	381	SI14	1980	1415
62	PD11	-1920	-1453	142	TS1	7637	-1453	222	SI73	8340	1415	302	SI93	5140	1415	382	SI13	1940	1415
63	PD10	-1820	-1453	143	TS2	7737	-1453	223	SI72	8300	1415	303	SI92	5100	1415	383	SI12	1900	1415
64	PD9	-1720	-1453	144	TS3	7837	-1453	224	SI71	8260	1415	304	SI91	5060	1415	384	SI11	1860	1415
65	PD8	-1620	-1453	145	TS4	7937	-1453	225	SI70	8220	1415	305	SI90	5020	1415	385	SI10	1820	1415
66	PD7	-1520	-1453	146	TS5	8037	-1453	226	SI69	8180	1415	306	SI89	4980	1415	386	SI09	1780	1415
67	PD6	-1419	-1453	147	TS6	8137	-1453	227	SI68	8140	1415	307	SI88	4940	1415	387	SI08	1740	1415
68	PD5	-1319	-1453	148	TS7	8237	-1453	228	SI67	8100	1415	308	SI87	4900	1415	388	SI07	1700	1415
69	PD4	-1219	-1453	149	DUMMY2	8387	-1453	229	SI66	8060	1415	309	SI86	4860	1415	389	SI06	1660	1415
70	PD3	-1119	-1453	150	DUMMY3	8487	-1453	230	SI65	8020	1415	310	SI85	4820	1415	390	SI05	1620	1415
71	PD2	-1019	-1453	151	DUMMY4	8788	-1453	231	SI64	7980	1415	311	SI84	4780	1415	391	SI04	1580	1415
72	PD1	-919	-1453	152	DUMMY5	8750	-1260	232	SI63	7940	1415	312	SI83	4740	1415	392	SI03	1540	1415
73	PD0	-819	-1453	153	DUMMY6	8750	-1220	233	SI62	7900	1415	313	SI82	4700	1415	393	SI02	1500	1415
74	Vcc	-669	-1453	154	DUMMY7	8750	-1180	234	SI61	7860	1415	314	SI81	4660	1415	394	SI01	1460	1415
75	Vcc	-569	-1453	155	DUMMY8	8750	-1140	235	SI60	7820	1415	315	SI80	4620	1415	395	SI00	1420	1415
76	Vcc	-469	-1453	156	DUMMY9	8750	-1100	236	SI59	7780	1415	316	SI79	4580	1415	396	SI99	1380	1415
77	Vcc	-369	-1453	157	DUMMY10	8750	-1060	237	SI58	7740	1415	317	SI78	4540	1415	397	SI98	1340	1415
78	Vcc	-269	-1453	158	DUMMY11	8750	-1020	238	SI57	7700	1415	318	SI77	4500	1415	398	SI97	1300	1415
79	Vcc	-168	-1453	159	DUMMY12	8750	-980	239	SI56	7660	1415	319	SI76	4460	1415	399	SI96	1260	1415
80	Vcc	-68	-1453	160	DUMMY13	8750	-940	240	SI55	7620	1415	320	SI75	4420	1415	400	SI95	1220	1415

No.	pad name	X	Y
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402	S293	1140	1415
403	S292	1100	1415
404	S291	1060	1415
405	S290	1020	1415
406	S289	980	1415
407	S288	940	1415
408	S287	900	1415
409	S286	860	1415
410	S285	820	1415
411	S284	780	1415
412	S283	740	1415
413	S282	700	1415
414	S281	660	1415
415	S280	620	1415
416	S279	580	1415
417	S278	540	1415
418	S277	500	1415
419	S276	460	1415
420	S275	420	1415
421	S274	380	1415
422	S273	340	1415
423	S272	300	1415
424	S271	260	1415
425	S270	220	1415
426	S269	180	1415
427	S268	140	1415
428	S267	100	1415
429	S266	60	1415
430	S265	20	1415
431	S264	-20	1415
432	S263	-60	1415
433	S262	-100	1415
434	S261	-140	1415
435	S260	-180	1415
436	S259	-220	1415
437	S258	-260	1415
438	S257	-300	1415
439	S256	-340	1415
440	S255	-380	1415
441	S254	-420	1415
442	S253	-460	1415
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444	S251	-540	1415
445	S250	-580	1415
446	S249	-620	1415
447	S248	-660	1415
448	S247	-700	1415
449	S246	-740	1415
450	S245	-780	1415
451	S244	-820	1415
452	S243	-860	1415
453	S242	-900	1415
454	S241	-940	1415
455	S240	-980	1415
456	S239	-1020	1415
457	S238	-1060	1415
458	S237	-1100	1415
459	S236	-1140	1415
460	S235	-1180	1415
461	S234	-1220	1415
462	S233	-1260	1415
463	S232	-1300	1415
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485	S210	-2180	1415
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487	S208	-2260	1415
488	S207	-2300	1415
489	S206	-2340	1415
490	S205	-2380	1415
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492	S203	-2460	1415
493	S202	-2500	1415
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507	S188	-3060	1415
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510	S185	-3180	1415
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512	S183	-3260	1415
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652	S44	-8750	1020
653	S43	-8750	980
654	S42	-8750	940
655	S41	-8750	900
656	S40	-8750	860
657	S39	-8750	820
658	S38	-8750	780
659	S37	-8750	740
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661	S35	-8750	660
662	S34	-8750	620
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666	S30	-8750	460
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668	S28	-8750	380
669	S27	-8750	340
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689	S7	-8750	-460
690	S6	-8750	-500
691	S5	-8750	-540
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693	S3	-8750	-620
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695	S1	-8750	-700
696	DUMMY21	-8750	-740
697	DUMMY22	-8750	-780
698	DUMMY23	-8750	-820
699	DUMMY24	-8750	-860
700	DUMMY25	-8750	-900
701	DUMMY26	-8750	-940
702	DUMMY27	-8750	-980
703	DUMMY28	-8750	-1020
704	DUMMY29	-8750	-1060
705	DUMMY30	-8750	-1100
706	DUMMY31	-8750	-1140
707	DUMMY32	-8750	-1180
708	DUMMY33	-8750	-1220
709	DUMMY34	-8750	-1260

■HD667BA72 PAD Assignment (Laced

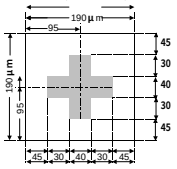
-Chip size: 17.84mm x 3.17mm
-Chip thickness: 400 μm(typ.)
-PAD Coordinate: PAD center
-PAD Origin: Chip center

-Au bump size:
(1) 80 μm×80 μm
DUMMY1(N0.1),RESET1(No.2)～TS7(NO.148),
DUMMY2(NO.149)～DUMMY4(NO.151),
DUMMY19(NO.216),DUMMY20(NO.645)
(2) 40 μm×63 μm
S51(NO.644)～S478(NO.217)

(3) 63 μm×40 μm
S1(NO.696)～S50(NO.646),S528(NO.166)～S479(NO.215),
DUMMY5(NO.152)～DUMMY18(NO.165),
DUMMY21(NO.697)～DUMMY34(NO.710)

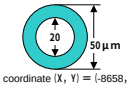
=Au bump pitch: Refer to the PAD coordinate
-Au bump height: 15 μm(typ.)
Number in this drawing indicate number in PAD coordinate.

-Alignment Mark
(1) Assign: two points
coordinate (X, Y) = (±8647.0, -1404.0)

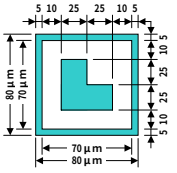


(2－a) coordinate (X, Y) = (-8787.9, 1350)

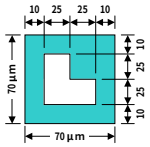
(2－b) coordinate (X, Y) = (8787.9, 1350)



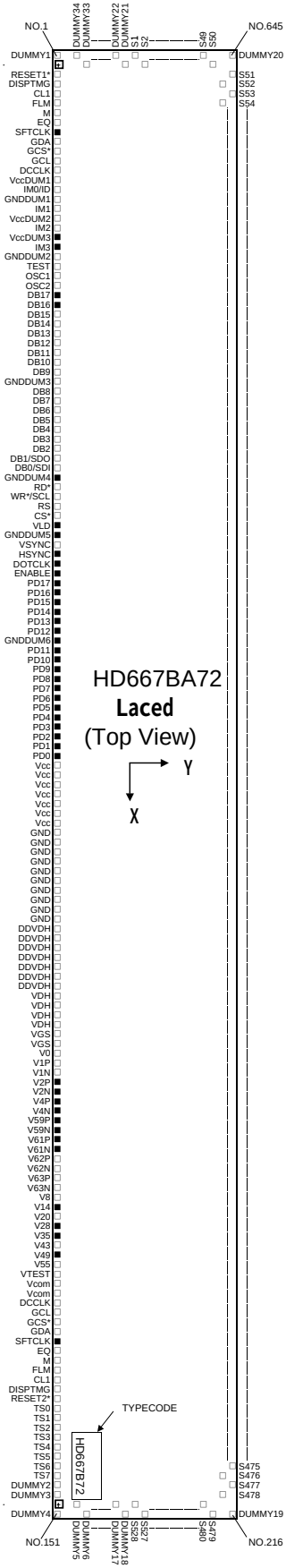
(3－a) coordinate (X, Y) = (-8658, 1452.9)



(3－b) coordinate (X, Y) = (8658, 1452.9)



■New assignment pad from 770 in I/O part



PAD Coordinate (Laced)

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-8788	-1453	81	GND	82	-1453	161	DUMMY14	8796	-900	241	SI54	7580	1368	321	SI74	4380	1368
2	RESET1 *	-8474	-1453	82	GND	182	-1453	162	DUMMY15	8703	-860	242	SI53	7540	1461	322	SI73	4340	1461
3	DISPTMG	-8339	-1453	83	GND	282	-1453	163	DUMMY16	8796	-820	243	SI52	7500	1368	323	SI72	4300	1368
4	CL1	-8204	-1453	84	GND	382	-1453	164	DUMMY17	8703	-780	244	SI51	7460	1461	324	SI71	4260	1461
5	FLM	-8069	-1453	85	GND	482	-1453	165	DUMMY18	8796	-740	245	SI50	7420	1368	325	SI70	4220	1368
6	M	-7934	-1453	86	GND	582	-1453	166	SI28	8703	-700	246	SI49	7380	1461	326	SI69	4180	1461
7	EQ	-7799	-1453	87	GND	682	-1453	167	SI27	8796	-660	247	SI48	7340	1368	327	SI68	4140	1368
8	SFTCLK	-7664	-1453	88	GND	782	-1453	168	SI26	8703	-620	248	SI47	7300	1461	328	SI67	4100	1461
9	GDA	-7529	-1453	89	GND	882	-1453	169	SI25	8796	-580	249	SI46	7260	1368	329	SI66	4060	1368
10	GCS*	-7394	-1453	90	GND	982	-1453	170	SI24	8703	-540	250	SI45	7220	1461	330	SI65	4020	1461
11	GCL	-7259	-1453	91	DDVDH	1133	-1453	171	SI23	8796	-500	251	SI44	7180	1368	331	SI64	3980	1368
12	DCCLK	-7124	-1453	92	DDVDH	1233	-1453	172	SI22	8703	-460	252	SI43	7140	1461	332	SI63	3940	1461
13	VCCDUM1	-6974	-1453	93	DDVDH	1333	-1453	173	SI21	8796	-420	253	SI42	7100	1368	333	SI62	3900	1368
14	M0/ ID	-6874	-1453	94	DDVDH	1433	-1453	174	SI20	8703	-380	254	SI41	7060	1461	334	SI61	3860	1461
15	GNDDUM1	-6774	-1453	95	DDVDH	1533	-1453	175	SI19	8796	-340	255	SI40	7020	1368	335	SI60	3820	1368
16	M1	-6674	-1453	96	DDVDH	1633	-1453	176	SI18	8703	-300	256	SI39	6980	1461	336	SI59	3780	1461
17	VCCDUM2	-6574	-1453	97	DDVDH	1733	-1453	177	SI17	8796	-260	257	SI38	6940	1368	337	SI58	3740	1368
18	M2	-6474	-1453	98	VDH	1883	-1453	178	SI16	8703	-220	258	SI37	6900	1461	338	SI57	3700	1461
19	VCCDUM3	-6373	-1453	99	VDH	1983	-1453	179	SI15	8796	-180	259	SI36	6860	1368	339	SI56	3660	1368
20	M3	-6273	-1453	100	VDH	2083	-1453	180	SI14	8703	-140	260	SI35	6820	1461	340	SI55	3620	1461
21	GNDDUM2	-6173	-1453	101	VDH	2183	-1453	181	SI13	8796	-100	261	SI34	6780	1368	341	SI54	3580	1368
22	TEST	-6073	-1453	102	VGS	2334	-1453	182	SI12	8703	-60	262	SI33	6740	1461	342	SI53	3540	1461
23	OSC1	-5923	-1453	103	VGS	2434	-1453	183	SI11	8796	-20	263	SI32	6700	1368	343	SI52	3500	1368
24	OSC2	-5773	-1453	104	V0	2584	-1453	184	SI10	8703	20	264	SI31	6660	1461	344	SI51	3460	1461
25	DB17	-5623	-1453	105	V1 P	2734	-1453	185	SI09	8796	60	265	SI30	6620	1368	345	SI50	3420	1368
26	DB16	-5523	-1453	106	V1 N	2884	-1453	186	SI08	8703	100	266	SI29	6580	1461	346	SI49	3380	1461
27	DB15	-5423	-1453	107	V2 P	3034	-1453	187	SI07	8796	140	267	SI28	6540	1368	347	SI48	3340	1368
28	DB14	-5323	-1453	108	V2 N	3184	-1453	188	SI06	8703	180	268	SI27	6500	1461	348	SI47	3300	1461
29	DB13	-5223	-1453	109	V4 P	3334	-1453	189	SI05	8796	220	269	SI26	6460	1368	349	SI46	3260	1368
30	DB12	-5122	-1453	110	V4 N	3484	-1453	190	SI04	8703	260	270	SI25	6420	1461	350	SI45	3220	1461
31	DB11	-5022	-1453	111	V59 P	3635	-1453	191	SI03	8796	300	271	SI24	6380	1368	351	SI44	3180	1368
32	DB10	-4922	-1453	112	V59 N	3785	-1453	192	SI02	8703	340	272	SI23	6340	1461	352	SI43	3140	1461
33	DB9	-4822	-1453	113	V61 P	3935	-1453	193	SI01	8796	380	273	SI22	6300	1368	353	SI42	3100	1368
34	GNDDUM3	-4722	-1453	114	V61 N	4085	-1453	194	SI00	8703	420	274	SI21	6260	1461	354	SI41	3060	1461
35	DB8	-4622	-1453	115	V62 P	4235	-1453	195	SI99	8796	460	275	SI20	6220	1368	355	SI40	3020	1368
36	DB7	-4522	-1453	116	V62 N	4385	-1453	196	SI98	8703	500	276	SI19	6180	1461	356	SI39	2980	1461
37	DB6	-4422	-1453	117	V63 P	4535	-1453	197	SI97	8796	540	277	SI18	6140	1368	357	SI38	2940	1368
38	DB5	-4322	-1453	118	V63 N	4685	-1453	198	SI96	8703	580	278	SI17	6100	1461	358	SI37	2900	1461
39	DB4	-4222	-1453	119	V8	4836	-1453	199	SI95	8796	620	279	SI16	6060	1368	359	SI36	2860	1368
40	DB3	-4122	-1453	120	V14	4936	-1453	200	SI94	8703	660	280	SI15	6020	1461	360	SI35	2820	1461
41	DB2	-4022	-1453	121	V20	5036	-1453	201	SI93	8796	700	281	SI14	5980	1368	361	SI34	2780	1368
42	DB1/ SDO	-3921	-1453	122	V28	5136	-1453	202	SI92	8703	740	282	SI13	5940	1461	362	SI33	2740	1461
43	DB0/ SDI	-3821	-1453	123	V35	5236	-1453	203	SI91	8796	780	283	SI12	5900	1368	363	SI32	2700	1368
44	GNDDUM4	-3721	-1453	124	V43	5336	-1453	204	SI90	8703	820	284	SI11	5860	1461	364	SI31	2660	1461
45	RD*	-3621	-1453	125	V49	5436	-1453	205	SI89	8796	860	285	SI10	5820	1368	365	SI30	2620	1368
46	WR*/ SCL	-3521	-1453	126	V55	5536	-1453	206	SI88	8703	900	286	SI09	5780	1461	366	SI29	2580	1461
47	RS	-3421	-1453	127	VTEST	5636	-1453	207	SI87	8796	940	287	SI08	5740	1368	367	SI28	2540	1368
48	CS*	-3321	-1453	128	VCOM	5786	-1453	208	SI86	8703	980	288	SI07	5700	1461	368	SI27	2500	1461
49	VLD	-3221	-1453	129	VCOM	5886	-1453	209	SI85	8796	1020	289	SI06	5660	1368	369	SI26	2460	1368
50	GNDDUM5	-3121	-1453	130	DCCLK	6036	-1453	210	SI84	8703	1060	290	SI05	5620	1461	370	SI25	2420	1461
51	VSYNC	-3021	-1453	131	GCL	6171	-1453	211	SI83	8796	1100	291	SI04	5580	1368	371	SI24	2380	1368
52	HSYNC	-2921	-1453	132	GCS*	6306	-1453	212	SI82	8703	1140	292	SI03	5540	1461	372	SI23	2340	1461
53	DOTCLK	-2821	-1453	133	GDA	6441	-1453	213	SI81	8796	1180	293	SI02	5500	1368	373	SI22	2300	1368
54	ENABLE	-2721	-1453	134	SFTCLK	6576	-1453	214	SI80	8703	1220	294	SI01	5460	1461	374	SI21	2260	1461
55	PD17	-2620	-1453	135	EQ	6711	-1453	215	SI79	8796	1260	295	SI00	5420	1368	375	SI20	2220	1368
56	PD16	-2520	-1453	136	M	6846	-1453	216	DUMMY19	8788	1453	296	SI99	5380	1461	376	SI19	2180	1461
57	PD15	-2420	-1453	137	FLM	6981	-1453	217	SI78	8540	1368	297	SI98	5340	1368	377	SI18	2140	1368
58	PD14	-2320	-1453	138	CL1	7116	-1453	218	SI77	8500	1461	298	SI97	5300	1461	378	SI17	2100	1461
59	PD13	-2220	-1453	139	DISPTMG	7251	-1453	219	SI76	8460	1368	299	SI96	5260	1368	379	SI16	2060	1368
60	PD12	-2120	-1453	140	RESET2 *	7386	-1453	220	SI75	8420	1461	300	SI95	5220	1461	380	SI15	2020	1461
61	GNDDUM6	-2020	-1453	141	TS0	7537	-1453	221	SI74	8380	1368	301	SI94	5180	1368	381	SI14	1980	1368
62	PD11	-1920	-1453	142	TS1	7637	-1453	222	SI73	8340	1461	302	SI93	5140	1461	382	SI13	1940	1461
63	PD10	-1820	-1453	143	TS2	7737	-1453	223	SI72	8300	1368	303	SI92	5100	1368	383	SI12	1900	1368
64	PD9	-1720	-1453	144	TS3	7837	-1453	224	SI71	8260	1461	304	SI91	5060	1461	384	SI11	1860	1461
65	PD8	-1620	-1453	145	TS4	7937	-1453	225	SI70	8220	1368	305	SI90	5020	1368	385	SI10	1820	1368
66	PD7	-1520	-1453	146	TS5	8037	-1453	226	SI69	8180	1461	306	SI89	4980	1461	386	SI09	1780	1461
67	PD6	-1419	-1453	147	TS6	8137	-1453	227	SI68	8140	1368	307	SI88	4940	1368	387	SI08	1740	1368
68	PD5	-1319	-1453	148	TS7	8237	-1453	228	SI67	8100	1461	308	SI87	4900	1461	388	SI07	1700	1461
69	PD4	-1219	-1453	149	DUMMY2	8387	-1453	229	SI66	8060	1368	309	SI86	4860	1368	389	SI06	1660	1368
70	PD3	-1119	-1453	150	DUMMY3	8487	-1453	230	SI65	8020	1461	310	SI85	4820	1461	390	SI05	1620	1461
71	PD2	-1019	-1453	151	DUMMY4	8788	-1453	231	SI64	7980	1368	311	SI84	4780	1368	391	SI04	1580	1368
72	PD1	-919	-1453	152	DUMMY5	8703	-1260	232	SI63	7940	1461	312	SI83	4740	1461	392	SI03	1540	1461
73	PD0	-819	-1453	153	DUMMY6	8796	-1220	233	SI62	7900	1368	313	SI82	4700	1368	393	SI02	1500	1368
74	Vcc	-669	-1453	154	DUMMY7	8703	-1180	234	SI61	7860	1461	314	SI81	4660	1461	394	SI01	1460	1461
75	Vcc	-569	-1453	155	DUMMY8	8796	-1140	235	SI60	7820	1368	315	SI80	4620	1368	395	SI00	1420	1368
76	Vcc	-469	-1453	156	DUMMY9	8703	-1100	236	SI59	7780	1461	316	SI79	4580	1461	396	SI99	1380	1461
77	Vcc	-369	-1453	157	DUMMY10	8796	-1060	237	SI58	7740	1368	317	SI78	4540	1368	397	SI98	1340	1368
78	Vcc	-269	-1453	158	DUMMY11	8703	-1020	238	SI57	7700	1461	318	SI77	4500	1461	398	SI97	1300	1461
79	Vcc	-168	-1453	159	DUMMY12	8796	-980	239	SI56	7660	1368	319	SI76	4460	1368	399	SI96	1260	1368
80	Vcc	-68	-1453	160	DUMMY13	8703	-940	240	SI55	7620	1461	320	SI75	4420	1461	400	SI95	1220	1461

No.	pad name	X	Y
401	S294	1180	1368
402	S293	1140	1461
403	S292	1100	1368
404	S291	1060	1461
405	S290	1020	1368
406	S289	980	1461
407	S288	940	1368
408	S287	900	1461
409	S286	860	1368
410	S285	820	1461
411	S284	780	1368
412	S283	740	1461
413	S282	700	1368
414	S281	660	1461
415	S280	620	1368
416	S279	580	1461
417	S278	540	1368
418	S277	500	1461
419	S276	460	1368
420	S275	420	1461
421	S274	380	1368
422	S273	340	1461
423	S272	300	1368
424	S271	260	1461
425	S270	220	1368
426	S269	180	1461
427	S268	140	1368
428	S267	100	1461
429	S266	60	1368
430	S265	20	1461
431	S264	-20	1368
432	S263	-60	1461
433	S262	-100	1368
434	S261	-140	1461
435	S260	-180	1368
436	S259	-220	1461
437	S258	-260	1368
438	S257	-300	1461
439	S256	-340	1368
440	S255	-380	1461
441	S254	-420	1368
442	S253	-460	1461
443	S252	-500	1368
444	S251	-540	1461
445	S250	-580	1368
446	S249	-620	1461
447	S248	-660	1368
448	S247	-700	1461
449	S246	-740	1368
450	S245	-780	1461
451	S244	-820	1368
452	S243	-860	1461
453	S242	-900	1368
454	S241	-940	1461
455	S240	-980	1368
456	S239	-1020	1461
457	S238	-1060	1368
458	S237	-1100	1461
459	S236	-1140	1368
460	S235	-1180	1461
461	S234	-1220	1368
462	S233	-1260	1461
463	S232	-1300	1368
464	S231	-1340	1461
465	S230	-1380	1368
466	S229	-1420	1461
467	S228	-1460	1368
468	S227	-1500	1461
469	S226	-1540	1368
470	S225	-1580	1461
471	S224	-1620	1368
472	S223	-1660	1461
473	S222	-1700	1368
474	S221	-1740	1461
475	S220	-1780	1368
476	S219	-1820	1461
477	S218	-1860	1368
478	S217	-1900	1461
479	S216	-1940	1368
480	S215	-1980	1461

No.	pad name	X	Y
481	S214	-2020	1368
482	S213	-2060	1461
483	S212	-2100	1368
484	S211	-2140	1461
485	S210	-2180	1368
486	S209	-2220	1461
487	S208	-2260	1368
488	S207	-2300	1461
489	S206	-2340	1368
490	S205	-2380	1461
491	S204	-2420	1368
492	S203	-2460	1461
493	S202	-2500	1368
494	S201	-2540	1461
495	S200	-2580	1368
496	S199	-2620	1461
497	S198	-2660	1368
498	S197	-2700	1461
499	S196	-2740	1368
500	S195	-2780	1461
501	S194	-2820	1368
502	S193	-2860	1461
503	S192	-2900	1368
504	S191	-2940	1461
505	S190	-2980	1368
506	S189	-3020	1461
507	S188	-3060	1368
508	S187	-3100	1461
509	S186	-3140	1368
510	S185	-3180	1461
511	S184	-3220	1368
512	S183	-3260	1461
513	S182	-3300	1368
514	S181	-3340	1461
515	S180	-3380	1368
516	S179	-3420	1461
517	S178	-3460	1368
518	S177	-3500	1461
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520	S175	-3580	1461
521	S174	-3620	1368
522	S173	-3660	1461
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524	S171	-3740	1461
525	S170	-3780	1368
526	S169	-3820	1461
527	S168	-3860	1368
528	S167	-3900	1461
529	S166	-3940	1368
530	S165	-3980	1461
531	S164	-4020	1368
532	S163	-4060	1461
533	S162	-4100	1368
534	S161	-4140	1461
535	S160	-4180	1368
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537	S158	-4260	1368
538	S157	-4300	1461
539	S156	-4340	1368
540	S155	-4380	1461
541	S154	-4420	1368
542	S153	-4460	1461
543	S152	-4500	1368
544	S151	-4540	1461
545	S150	-4580	1368
546	S149	-4620	1461
547	S148	-4660	1368
548	S147	-4700	1461
549	S146	-4740	1368
550	S145	-4780	1461
551	S144	-4820	1368
552	S143	-4860	1461
553	S142	-4900	1368
554	S141	-4940	1461
555	S140	-4980	1368
556	S139	-5020	1461
557	S138	-5060	1368
558	S137	-5100	1461
559	S136	-5140	1368
560	S135	-5180	1461

No.	pad name	X	Y
561	S134	-5220	1368
562	S133	-5260	1461
563	S132	-5300	1368
564	S131	-5340	1461
565	S130	-5380	1368
566	S129	-5420	1461
567	S128	-5460	1368
568	S127	-5500	1461
569	S126	-5540	1368
570	S125	-5580	1461
571	S124	-5620	1368
572	S123	-5660	1461
573	S122	-5700	1368
574	S121	-5740	1461
575	S120	-5780	1368
576	S119	-5820	1461
577	S118	-5860	1368
578	S117	-5900	1461
579	S116	-5940	1368
580	S115	-5980	1461
581	S114	-6020	1368
582	S113	-6060	1461
583	S112	-6100	1368
584	S111	-6140	1461
585	S110	-6180	1368
586	S109	-6220	1461
587	S108	-6260	1368
588	S107	-6300	1461
589	S106	-6340	1368
590	S105	-6380	1461
591	S104	-6420	1368
592	S103	-6460	1461
593	S102	-6500	1368
594	S101	-6540	1461
595	S100	-6580	1368
596	S99	-6620	1461
597	S98	-6660	1368
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607	S88	-7060	1368
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610	S85	-7180	1461
611	S84	-7220	1368
612	S83	-7260	1461
613	S82	-7300	1368
614	S81	-7340	1461
615	S80	-7380	1368
616	S79	-7420	1461
617	S78	-7460	1368
618	S77	-7500	1461
619	S76	-7540	1368
620	S75	-7580	1461
621	S74	-7620	1368
622	S73	-7660	1461
623	S72	-7700	1368
624	S71	-7740	1461
625	S70	-7780	1368
626	S69	-7820	1461
627	S68	-7860	1368
628	S67	-7900	1461
629	S66	-7940	1368
630	S65	-7980	1461
631	S64	-8020	1368
632	S63	-8060	1461
633	S62	-8100	1368
634	S61	-8140	1461
635	S60	-8180	1368
636	S59	-8220	1461
637	S58	-8260	1368
638	S57	-8300	1461
639	S56	-8340	1368
640	S55	-8380	1461

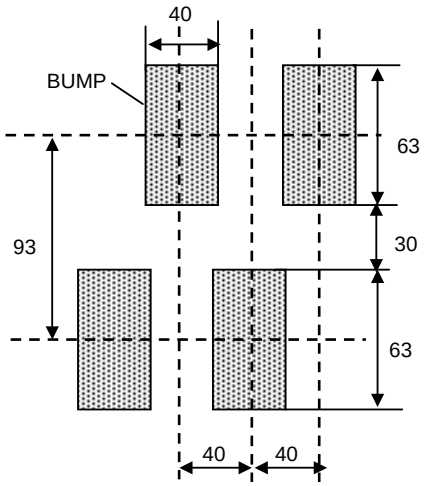
No.	pad name	X	Y
641	S54	-8420	1368
642	S53	-8460	1461
643	S52	-8500	1368
644	S51	-8540	1461
645	DUMMY20	-8788	1453
646	S50	-8703	1260
647	S49	-8796	1220
648	S48	-8703	1180
649	S47	-8796	1140
650	S46	-8703	1100
651	S45	-8796	1060
652	S44	-8703	1020
653	S43	-8796	980
654	S42	-8703	940
655	S41	-8796	900
656	S40	-8703	860
657	S39	-8796	820
658	S38	-8703	780
659	S37	-8796	740
660	S36	-8703	700
661	S35	-8796	660
662	S34	-8703	620
663	S33	-8796	580
664	S32	-8703	540
665	S31	-8796	500
666	S30	-8703	460
667	S29	-8796	420
668	S28	-8703	380
669	S27	-8796	340
670	S26	-8703	300
671	S25	-8796	260
672	S24	-8703	220
673	S23	-8796	180
674	S22	-8703	140
675	S21	-8796	100
676	S20	-8703	60
677	S19	-8796	20
678	S18	-8703	-20
679	S17	-8796	-60
680	S16	-8703	-100
681	S15	-8796	-140
682	S14	-8703	-180
683	S13	-8796	-220
684	S12	-8703	-260
685	S11	-8796	-300
686	S10	-8703	-340
687	S9	-8796	-380
688	S8	-8703	-420
689	S7	-8796	-460
690	S6	-8703	-500
691	S5	-8796	-540
692	S4	-8703	-580
693	S3	-8796	-620
694	S2	-8703	-660
695	S1	-8796	-700
696	DUMMY21	-8703	-740
697	DUMMY22	-8796	-780
698	DUMMY23	-8703	-820
699	DUMMY24	-8796	-860
700	DUMMY25	-8703	-900
701	DUMMY26	-8796	-940
702	DUMMY27	-8703	-980
703	DUMMY28	-8796	-1020
704	DUMMY29	-8703	-1060
705	DUMMY30	-8796	-1100
706	DUMMY31	-8703	-1140
707	DUMMY32	-8796	-1180
708	DUMMY33	-8703	-1220
709	DUMMY34	-8796	-1260

BUMP Arrangement

BUMP Arrangement

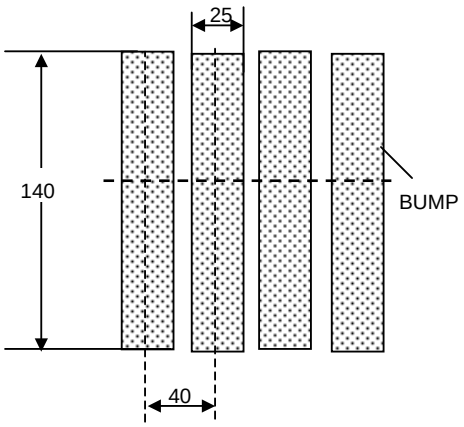
S1 S528

Laced Output Arrangement



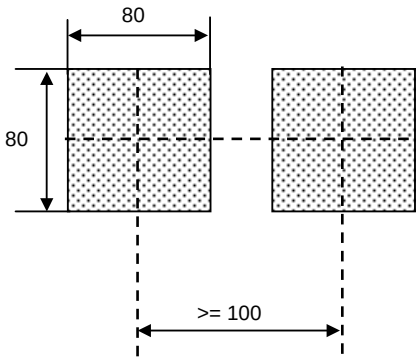
Unit: um

Straight Output Arrangement



Unit: um

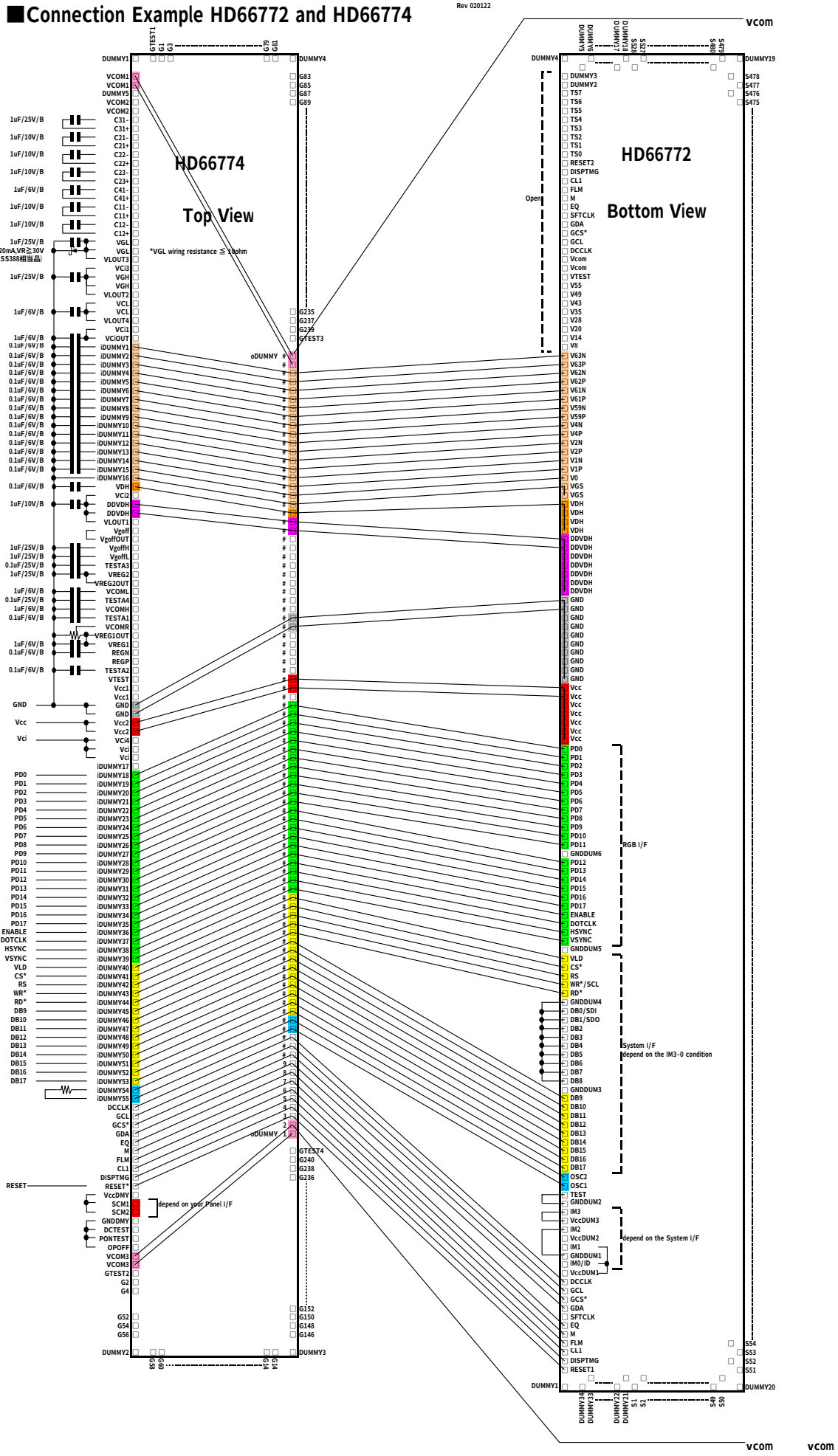
DUMMY1, RESET1 TS7,
DUMMY2 DUMMY4

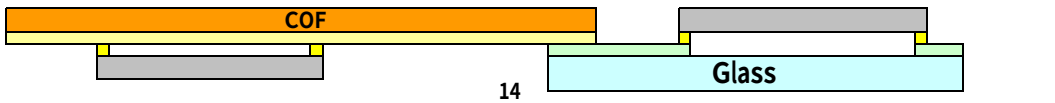


Unit: um

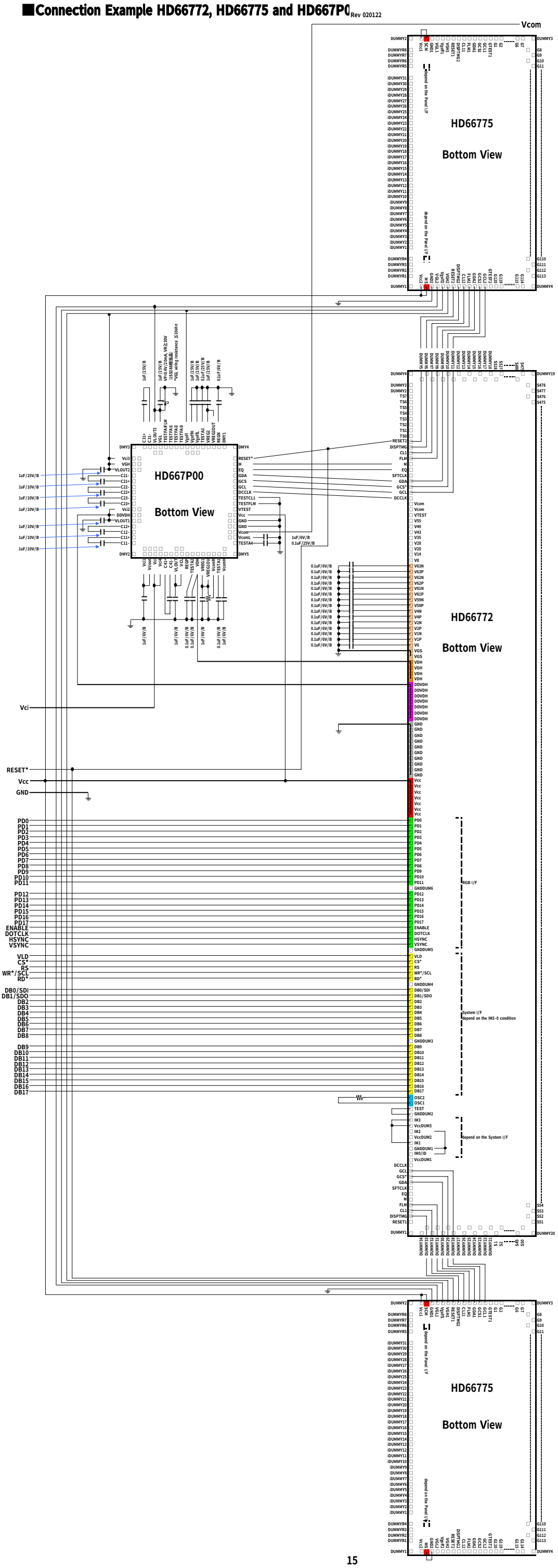
■Connection Example HD66772 and HD66774

Rev 020122





■Connection Example HD66772, HD66775 and HD667P0 Rev 020122



Block Function

System Interface

The HD66772 has five high-speed system interfaces: an 80-system 18-bit/16-bit/9-bit/8-bit bus and a clocked serial peripheral (SPI: Serial Peripheral Interface) port. The interface mode is selected by the IM3-0 pins.

The HD66772 has three registers: a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 2 Register Selection (8/9/16/18 Parallel Interface)

80-system Bus

WR*	RD*	RS*	Operation
0	1	0	Writing of an index to the IR
1	0	0	Reading of internal status
0	1	1	Writing to control registers or the GRAM through the WDR
1	0	1	Reading from the GRAM through the RDR

Table 3 Values of CS and VLD during RAM Write

CS*	VLD*	Operations
0	0	Data is written to the GRAM. RAM address is updated.
1	0	Data is not written to the GRAM. RAM address is not updated.
0	1	Data is not written to the GRAM. RAM address is updated.
1	1	Data is not written to the GRAM. The RAM address is not updated.

Note: The value of VLD only has a meaning for the RAM write instructions.

Table 4 Register Selection (Serial Peripheral Interface)

Start bytes			
WR*	**RD***	**RS***	**Operations**
0	1	0	Writing of an index into IR
1	0	0	Reading of internal status
0	1	1	Writing into control registers and the GRAM through the WDR
1	0	1	Reading from the GRAM through the RDR

External Display Interface

The HD66772 incorporates RGB and VSYNC interfaces as external interfaces for the reproduction of animated displays. When the RGB-I/F is selected, the synchronization signals, which are VSYNC, HSYNC, and DOTCLK and are supplied from the external interfaces, are available for use in operating the display. The data for display (PD17-0) are written according to the values of the data enable signal (ENABLE) and data valid signal (VLD) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. This allows flicker-free updating of the screen. When the VSYNC-I/F is selected, operations other than frame synchronization by the VSYNC signal are synchronized with the internal clock. The data for display is written to the GRAM via the conventional system interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

Switching from and to the conventional system interface is done by instructions. The interface, therefore, can be selected according to whether the screen is displaying moving or still pictures. All data written via the RGB-I/F are written to the GRAM. Therefore, data is only transferred when the screen is updated, which reduces the amount of data transferred and the consumption of power when moving pictures are being displayed.

Bit Operations

The HD66772 supports the following functions: a write data mask function that selects and writes data into the GRAM in bit units and logic operation functions that perform logic operations or conditional determination the contents of the control registers and writes into the GRAM. For details, see the section on the graphics operation functions.

Address Counter (AC)

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has 18 bits/pixel and stores the bit-pattern data of 176 x 240 bytes.

Grayscale Voltage Generation Circuit

The grayscale voltage generation circuit generates LCD-driving voltages according to the grayscale data set in the γ-correction register. 262,144 colors are simultaneously available for display. For details, see the section on the γ-correction register.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. The timing generator generates the interface signals (M, FLM, CL1, EQ, DCCLK, DISPTMG, and SFTCLK) for the gate-driver/power-supply IC.

Oscillation Circuit (OSC)

The HD66772 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 528 source drivers (S1 to S528).

Display pattern data is latched when 528-bit data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The shift direction of 528-bit data can be changed by the SS bit by selecting an appropriate direction for the device mounting configuration.

Interface with Gate driver

A serial interface circuit provides an interface with the HD66774. When sending an instruction setting from the HD66772 to the HD66774, a register setting value from within the HD66772 is transferred via the serial interface circuit. A transfer is started by setting a serial transfer enable in the HD66772. However, transfer to and reading from the HD66774 are not possible during standby. For details, see the Gate serial transfer to and from the gate driver.

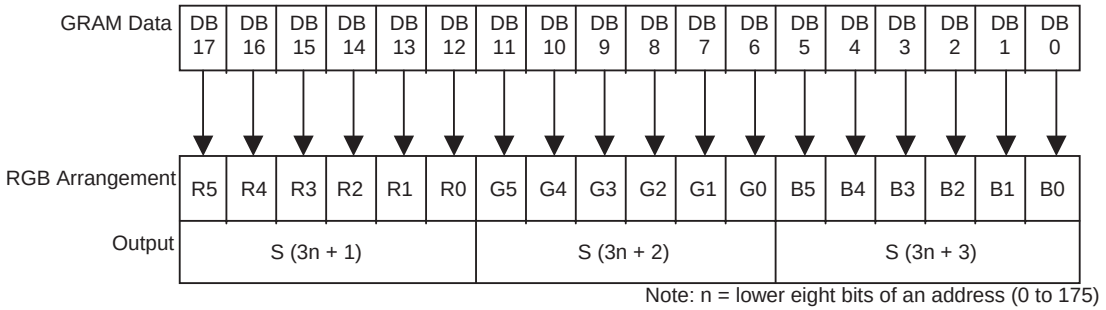
GRAM Address Map (HD66772)

Table 5 Relationship between GRAM Addresses and Placement in the Display (SS = 0)

S/G Pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS = 0	GS = 1	PD 17		PD 0	PD 17		PD 0	PD 17		PD 0	PD 17		PD 0		PD 17		PD 0	PD 17		PD 0	PD 17		PD 0	PD 17		PD 0
G1	G240	"0000"H			"0001"H			"0002"H			"0003"H				"0080"H			"0081"H			"0082"H			"00AF"H		
G2	G239	"0100"H			"0101"H			"0102"H			"0103"H				"0180"H			"0181"H			"0182"H			"01AF"H		
G3	G238	"0200"H			"0201"H			"0202"H			"0203"H				"0280"H			"0281"H			"0282"H			"02AF"H		
G4	G237	"0300"H			"0301"H			"0302"H			"0303"H				"0380"H			"0381"H			"0382"H			"03AF"H		
G5	G236	"0400"H			"0401"H			"0402"H			"0403"H				"0480"H			"0481"H			"0482"H			"04AF"H		
G6	G235	"0500"H			"0501"H			"0502"H			"0503"H				"0580"H			"0581"H			"0582"H			"05AF"H		
G7	G234	"0600"H			"0601"H			"0602"H			"0603"H				"0680"H			"0681"H			"0682"H			"06AF"H		
G8	G233	"0700"H			"0701"H			"0702"H			"0703"H				"0780"H			"0781"H			"0782"H			"07AF"H		
G9	G232	"0800"H			"0801"H			"0802"H			"0803"H				"0880"H			"0881"H			"0882"H			"08AF"H		
G10	G231	"0900"H			"0901"H			"0902"H			"0903"H				"0980"H			"0981"H			"0982"H			"09AF"H		
G11	G230	"0A00"H			"0A01"H			"0A02"H			"0A03"H				"0A80"H			"0A81"H			"0A82"H			"0AAF"H		
G12	G229	"0B00"H			"0B01"H			"0B02"H			"0B03"H				"0B80"H			"0B81"H			"0B82"H			"0BAF"H		
G13	G228	"0C00"H			"0C01"H			"0C02"H			"0C03"H				"0C80"H			"0C81"H			"0C82"H			"0CAF"H		
G14	G227	"0D00"H			"0D01"H			"0D02"H			"0D03"H				"0D80"H			"0D81"H			"0D82"H			"0DAF"H		
G15	G226	"0E00"H			"0E01"H			"0E02"H			"0E03"H				"0E80"H			"0E81"H			"0E82"H			"0EAF"H		
G16	G225	"0F00"H			"0F01"H			"0F02"H			"0F03"H				"0F80"H			"0F81"H			"0F82"H			"0FAF"H		
G17	G224	"1000"H			"1001"H			"1002"H			"1003"H				"1080"H			"1081"H			"1082"H			"10AF"H		
G18	G223	"1100"H			"1101"H			"1102"H			"1103"H				"1180"H			"1181"H			"1182"H			"11AF"H		
G19	G222	"1200"H			"1201"H			"1202"H			"1203"H				"1280"H			"1281"H			"1282"H			"12AF"H		
G20	G221	"1300"H			"1301"H			"1302"H			"1303"H				"1380"H			"1381"H			"1382"H			"13AF"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G232	G8	"E800"H			"E801"H			"E802"H			"E803"H				"E880"H			"E881"H			"E882"H			"E8AF"H		
G234	G7	"E900"H			"E901"H			"E902"H			"E903"H				"E980"H			"E981"H			"E982"H			"E9AF"H		
G235	G6	"EA00"H			"EA01"H			"EA02"H			"EA03"H				"EA80"H			"EA81"H			"EA82"H			"EAAF"H		
G236	G5	"EB00"H			"EB01"H			"EB02"H			"EB03"H				"EB80"H			"EB81"H			"EB82"H			"EBAF"H		
G237	G4	"EC00"H			"EC01"H			"EC02"H			"EC03"H				"EC80"H			"EC81"H			"EC82"H			"ECAF"H		
G238	G3	"ED00"H			"ED01"H			"ED02"H			"ED03"H				"ED80"H			"ED81"H			"ED82"H			"EDAF"H		
G239	G2	"EE00"H			"EE01"H			"EE02"H			"EE03"H				"EE80"H			"EE81"H			"EE82"H			"EEAF"H		
G240	G1	"EF00"H			"EF01"H			"EF02"H			"EF03"H				"EF80"H			"EF81"H			"EF82"H			"EFAF"H		

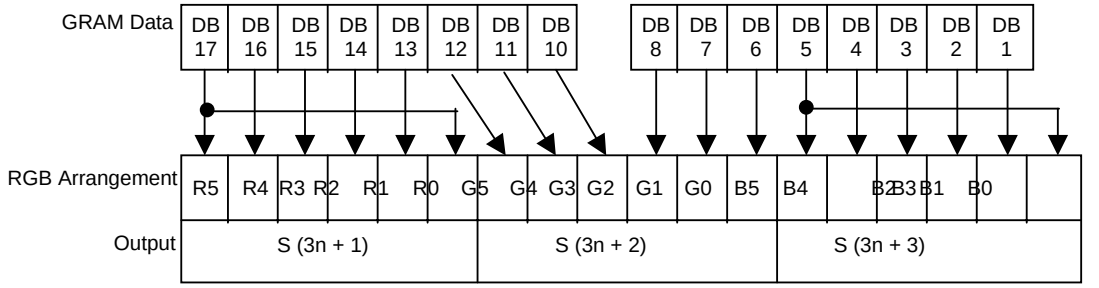
The ways that data is read from the GRAM for display when SS = “00”, BGR = “0” are shown below.

80-System 18-Bit Interface



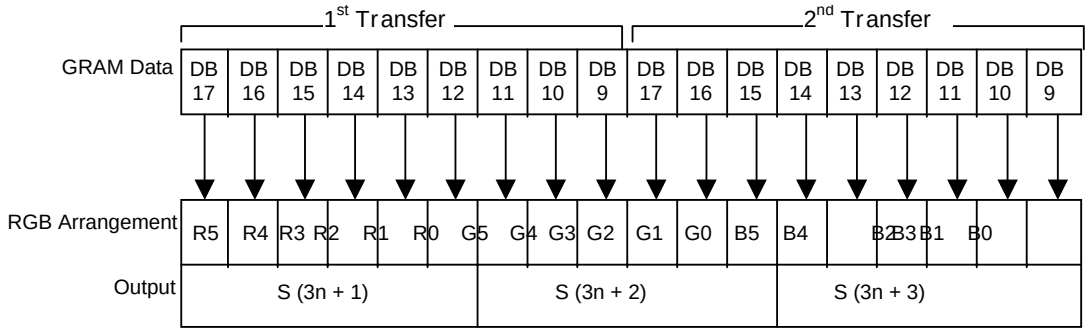
Note: n = lower eight bits of an address (0 to 175)

80-System 16-Bit Interface



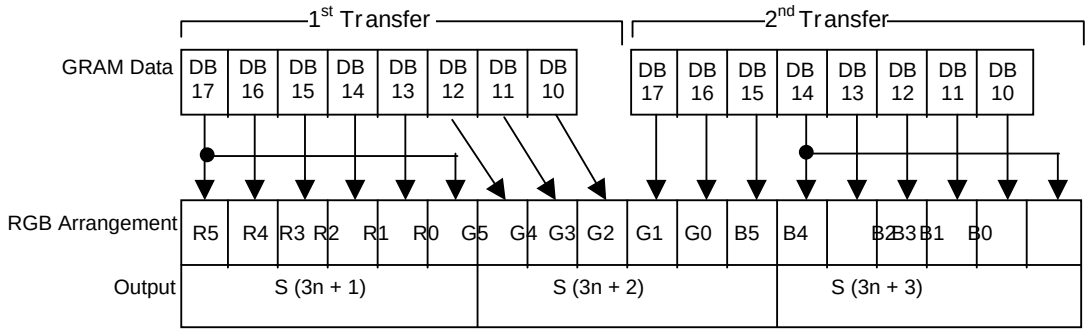
Note: n = lower eight bits of an address (0 to 175)

80-System 9-Bit Interface



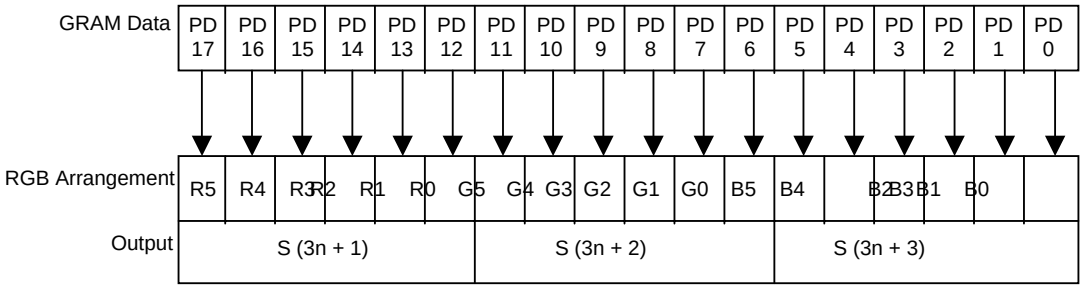
Note: n = lower eight bits of an address (0 to 175)

80-System 8-Bit Interface/SPI (twice transmission)



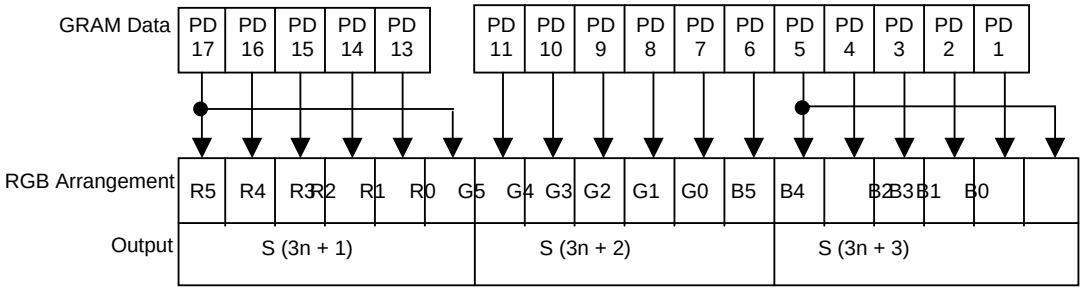
Note: n = lower eight bits of an address (0 to 175)

18-Bit RGB Interface



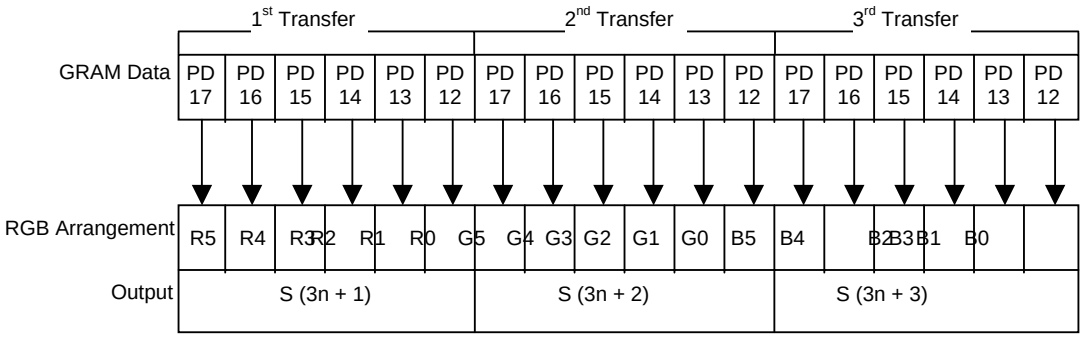
Note: n = lower eight bits of an address (0 to 175)

16-Bit RGB Interface



Note: n = lower eight bits of an address (0 to 175)

6-Bit RGB Interface



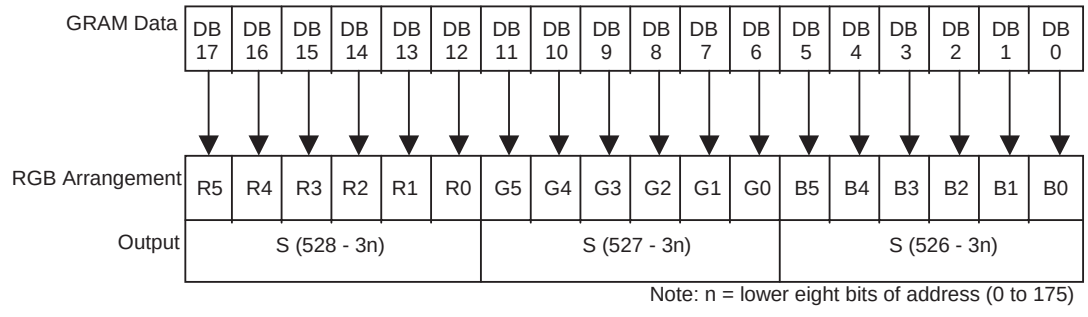
Note: n = lower eight bits of an address (0 to 175)

Table 6 Relationship between GRAM Addresses and Placement in the Display (SS = 1/BGR=1)

S/G Pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12		S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS = 0	GS = 1	PD 0		PD 17	PD 0		PD 17	PD 0		PD 17	PD 0		PD 17		PD 0		PD 17	PD 0		PD 17	PD 0		PD 17	PD 0		PD 17	PD 0		PD 17
G1	G240	"00AF"H			"00AE"H			"00AD"H			"00AC"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G239	"01AF"H			"01AE"H			"01AD"H			"01AC"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G238	"02AF"H			"02AE"H			"02AD"H			"02AC"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G237	"03AF"H			"03AE"H			"03AD"H			"03AC"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G236	"04AF"H			"04AE"H			"04AD"H			"04AC"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G235	"05AF"H			"05AE"H			"05AD"H			"05AC"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G234	"06AF"H			"06AE"H			"06AD"H			"06AC"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G233	"07AF"H			"07AE"H			"07AD"H			"07AC"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G232	"08AF"H			"08AE"H			"08AD"H			"08AC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G231	"09AF"H			"09AE"H			"09AD"H			"09AC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G230	"0AAF"H			"0AAE"H			"0AAD"H			"0AAC"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G229	"0BAF"H			"0BAE"H			"0BAD"H			"0BAC"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G228	"0CAF"H			"0CAE"H			"0CAD"H			"0CAC"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G227	"0DAF"H			"0DAE"H			"0DAD"H			"0DAC"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G226	"0EAF"H			"0EAE"H			"0EAD"H			"0EAC"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G225	"0FAF"H			"0FAE"H			"0FAD"H			"0FAC"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G224	"10AF"H			"10AE"H			"10AD"H			"10AC"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G223	"11AF"H			"11AE"H			"11AD"H			"11AC"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G222	"12AF"H			"12AE"H			"12AD"H			"12AC"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G221	"13AF"H			"13AE"H			"13AD"H			"13AC"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮																									
G232	G8	"E8AF"H			"E8AE"H			"E8AD"H			"E8AC"H			.....	"E803"H			"E802"H			"E801"H			"E800"H		
G234	G7	"E9AF"H			"E9AE"H			"E9AD"H			"E9AC"H			.....	"E903"H			"E902"H			"E901"H			"E900"H		
G235	G6	"EAAF"H			"EAAE"H			"EAAD"H			"EAAC"H			.....	"EA03"H			"EA02"H			"EA01"H			"EA00"H		
G236	G5	"EBAF"H			"EBAE"H			"EBAD"H			"EBAC"H			.....	"EB03"H			"EB02"H			"EB01"H			"EB00"H		
G237	G4	"ECAF"H			"ECAE"H			"ECAD"H			"ECAC"H			.....	"EC03"H			"EC02"H			"EC01"H			"EC00"H		
G238	G3	"EDAF"H			"EDAE"H			"EDAD"H			"EDAC"H			.....	"ED03"H			"ED02"H			"ED01"H			"ED00"H		
G239	G2	"EEAF"H			"EEAE"H			"EEAD"H			"EEAC"H			.....	"EE03"H			"EE02"H			"EE01"H			"EE00"H		
G240	G1	"EFAF"H			"EFAE"H			"EFAD"H			"EFAC"H			.....	"EF03"H			"EF02"H			"EF01"H			"EF00"H		

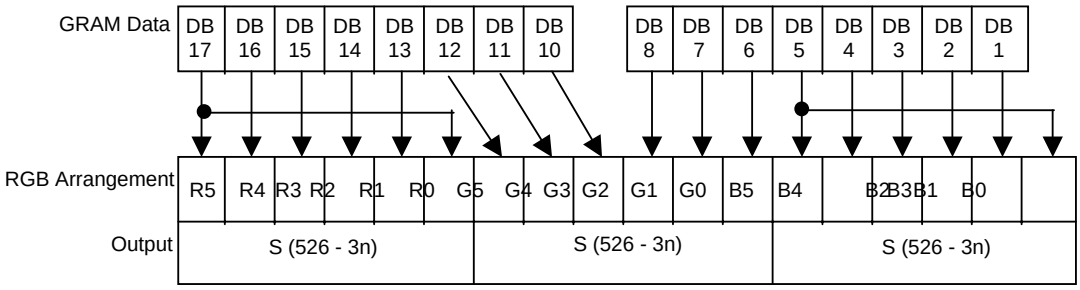
The ways that data is read from the GRAM for display when SS is set are shown below.

80-System 18-Bit Interface



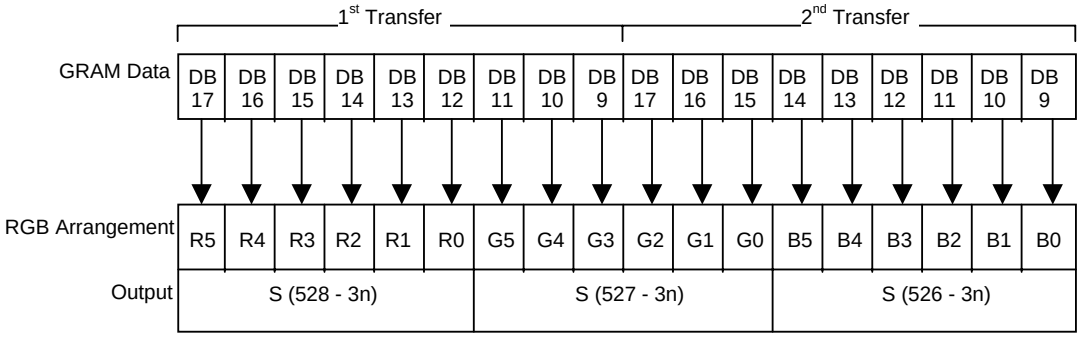
Note: n = lower eight bits of address (0 to 175)

80-System 16-Bit Interface



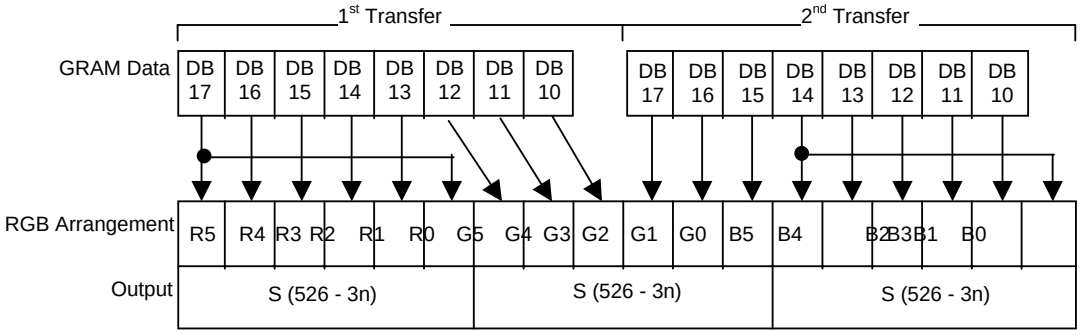
Note: n = lower eight bits of address (0 to 175)

80-System 9-Bit Interface



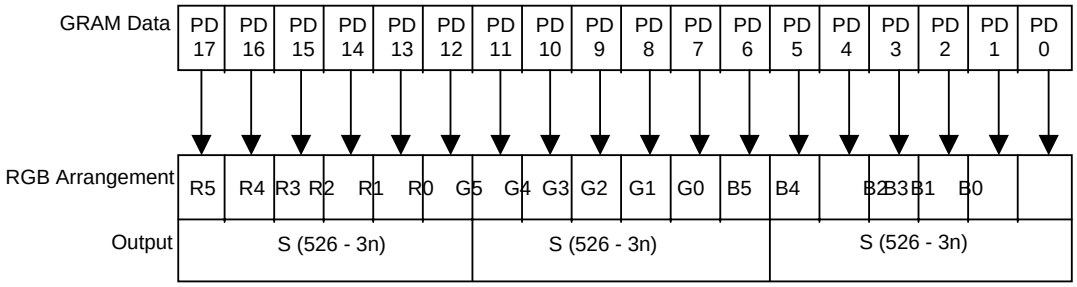
Note: n = lower eight bits of address (0 to 175)

80-System 8-Bit Interface / SPI (twice transmission)



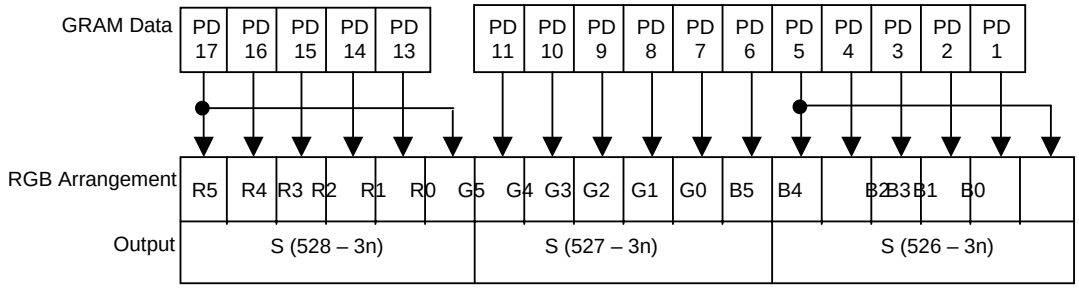
Note: n = lower eight bits of address (0 to 175)

18-Bit RGB Interface



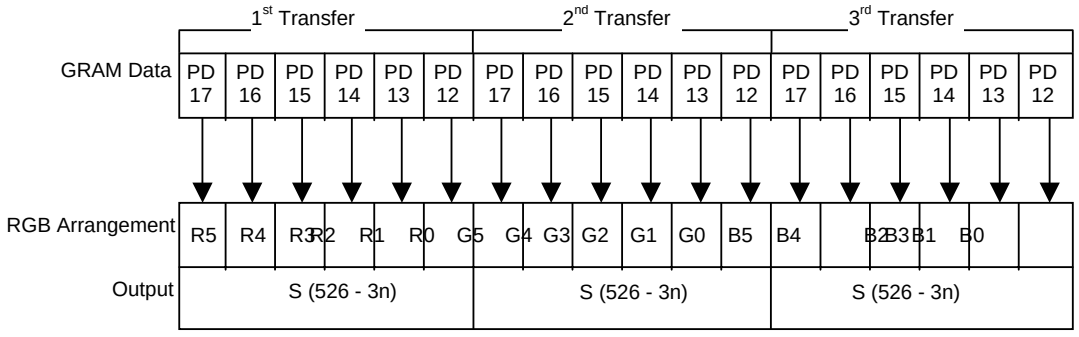
Note: n = lower eight bits of address (0 to 175)

16-Bit RGB Interface



Note: n = lower eight bits of address (0 to 175)

6-Bit RGB Interface



Note: n = lower eight bits of address (0 to 175)

Instructions

Outline

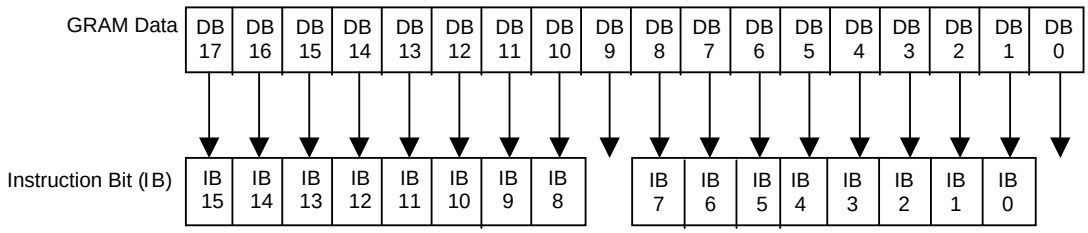
The HD66772 has an 18-bit bus architecture. Before the internal operation of the HD66772 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66772 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the internal 16-bit data bus signals (DB15 to DB0), make up the HD66772 instructions. The accesses to the GRAM use the internal 18-bit data bus. There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale γ-adjustment
- Interface with the gate driver and power supply IC

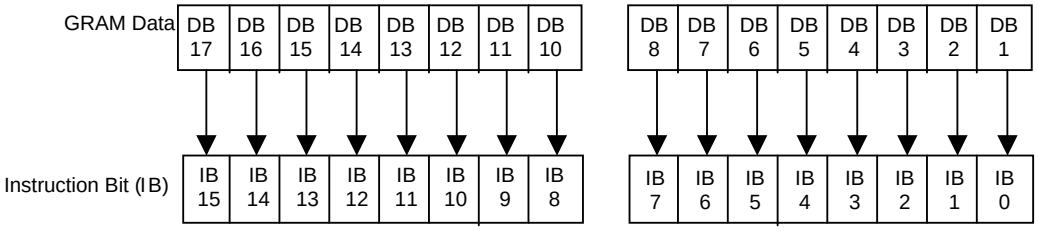
Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can reduce the amount of transferred data and lighten the microcomputer program load with the window address function.

The 16-bit instruction assignments (IB15-0) differ according to the interface as is shown below. Issuing of instructions should be in accord with the data format in use.

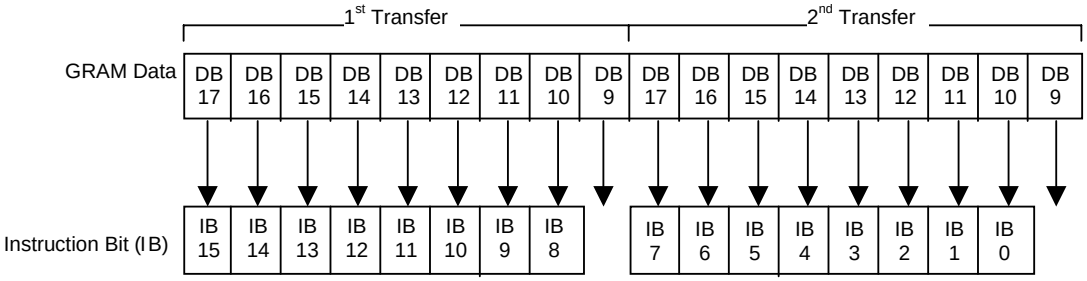
80-System 18-Bit Interface



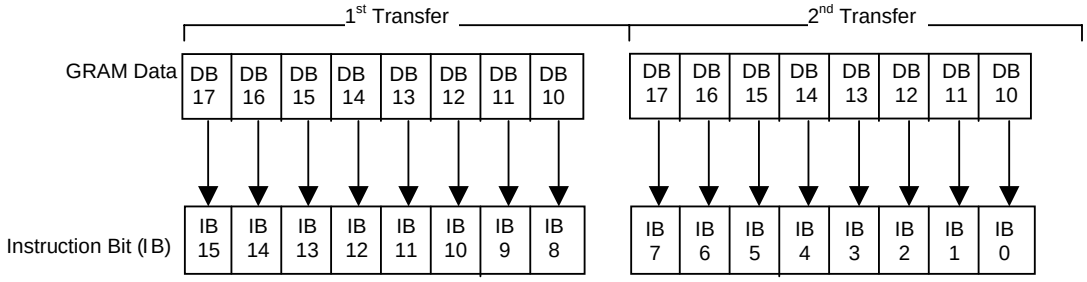
80-System 16-Bit Interface



80-System 9-Bit Interface



80-System 8-Bit Interface (SPI two transfers/pixel)



Ensure that you are aware of the assignments of instruction bits (IB15-0) for each interface that are illustrated below.

Index

The index instruction specifies the RAM control indexes (R00h to R4Fh). It sets the register number in the range of 00000 to 111111 in binary form. Those instruction bits of the index register which are not allocated to the index register should not be accessed.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66772.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 2 Status Read Instruction

Start Oscillation (R00h)

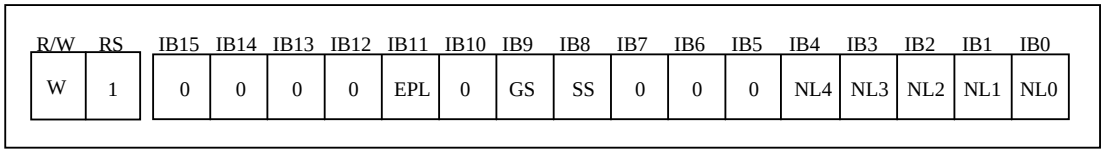
The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, 0772H is read.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	0

Figure 3 Start Oscillation Instruction

Driver Output Control (R01h)



R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	EPL	0	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 4 Driver Output Control Instruction

GS: Selects the output shift direction of a gate driver. The scan order is set to match the specifications of the gate driver. Select an appropriate direction for the device's configuration. When used with a HD66771, it is possible to select scanning in both directions in sequence. When a HD66774 is used, any of six scanning modes may be selected by using the GS bit and SCM2-1 settings. For details, see the data sheet for HD66774.

SS: Selects the output shift direction of the source driver. When SS = 0, the sequence is from S1 to S528. When SS = 1, the sequence is from S528 to S1. In addition, SS and BGR bits should be specified when the bit order for R, G, and B are changed. When SS = 0 and BGR = 0, R, G, and B are assigned in order from the S1 pin. When SS = 1 and BGR = 1, R, G, and B are assigned in order from the S528 pin. Rewrite data to the RAM whenever you change the SS and BGR bits.

EPL: Set the polarity of ENABLE pin while using RGB interface.

EPL = "0": ENABLE = "Low" / Writes data of PD17-0.

: ENABLE = "High"/ Does not write data of PD17-0.

EPL ="1": ENABLE = "High" / Writes data of PD17-0.

: ENABLE = "Low" / Does not write data of PD17-0.

The table below shows the relationship between EPL, ENABLE, VLD and RAM access.

Table 5

EPL	ENABLE	VLD	RAM write	RAM address
0	0	0	Valid	Updated
0	0	1	Invalid	Updated
0	1	*	Invalid	Hold
1	0	*	Invalid	Hold
1	1	0	Valid	Updated
1	1	1	Invalid	Updated

Note: The GS bit is used to set the gate driver. Control by the gate driver is according to this bit's value. For details, see the data sheet for the gate driver.

NL4-0: Specify the number of raster–rows to be driven. The number is adjusted in units of eight. Mapping of addresses in the GRAM is independent of this setting. The selected size should be larger than the panel to be driven.

Table 6 NL Bits

NL4	NL3	NL2	NL1	NL0	Display Size	LCD Raster-Rows	Gate-Driver Lines Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	528 x 16 dots	16	G1–G16
0	0	0	1	0	528 x 24 dots	24	G1–G24
0	0	0	1	1	528 x 32 dots	32	G1–G32
0	0	1	0	0	528 x 40 dots	40	G1–G40
0	0	1	0	1	528 x 48 dots	48	G1–G48
0	0	1	1	0	528 x 56 dots	56	G1–G56
0	0	1	1	1	528 x 64 dots	64	G1–G64
0	1	0	0	0	528 x 72 dots	72	G1–G72
		.			.	.	.
		.			.	.	.
		.			.	.	.
		.			.	.	.
		.			.	.	.
1	0	0	0	0	528 x 200 dots	200	G1–G200
1	0	0	0	1	528 x 208 dots	208	G1–G208
1	0	0	1	0	528 x 216 dots	216	G1–G216
1	0	0	1	1	528 x 224 dots	224	G1–G224
1	0	1	0	0	528 x 232 dots	232	G1–G232
1	0	1	0	1	528 x 240 dots	240	G1–G240

Note: A front porch period (set in the FP register) and back porch period (set in the BP register) will respectively be inserted as blank periods (all gates output Vgoff level) before and after the driver scans through all of the gates.

LCD-Driving-Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

FLD1-0: Specify the number of fields when an n-field interlaced drive is used. For details, see the section on interlaced driving.

Note: This function is not available when the external display interface is in use. In that case, FLD1 should be 0 and FLD0 should be 1.

Table 7 FLD Bits

FLD1	FLD0	Number of Fields
0	0	Setting disabled
0	1	1
1	0	Setting disabled
1	1	3

B/C: When B/C = 0, a field-AC waveform is generated and the LCD-driving signal alternates frame by frame. When B/C = 1, an n-raster-row AC waveform is generated and its polarity alternates on each raster-row specified by bits EOR and NW5–NW0 of the LCD-driving-waveform control register. For details, see the section on the n-raster-row reversed AC drive.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Note: The FLD1-0 bits are instruction bits for the gate driver. Control by the gate driver is according to the values of these bits. For details, see the data sheet on the gate driver.

Entry Mode (R03h)

Compare Register 1 (R04h)

Compare Register 2 (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0
W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

Figure 6 Entry Mode and Compare Register Instruction

The write data sent from the microcomputer is modified in the HD66772 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High-Speed RAM Write Mode section.

I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD7-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

AM: Sets the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

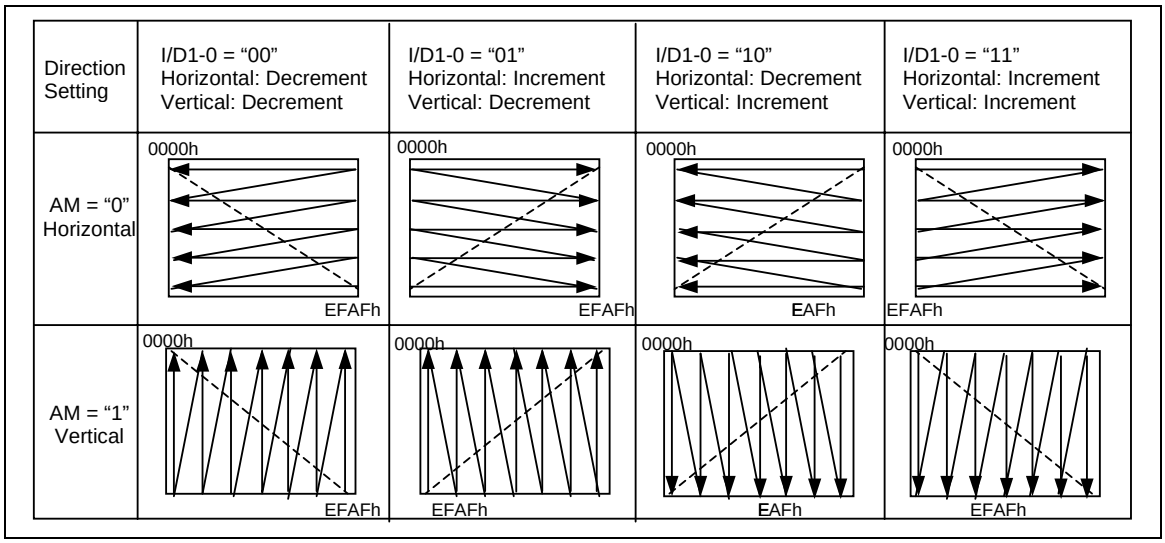


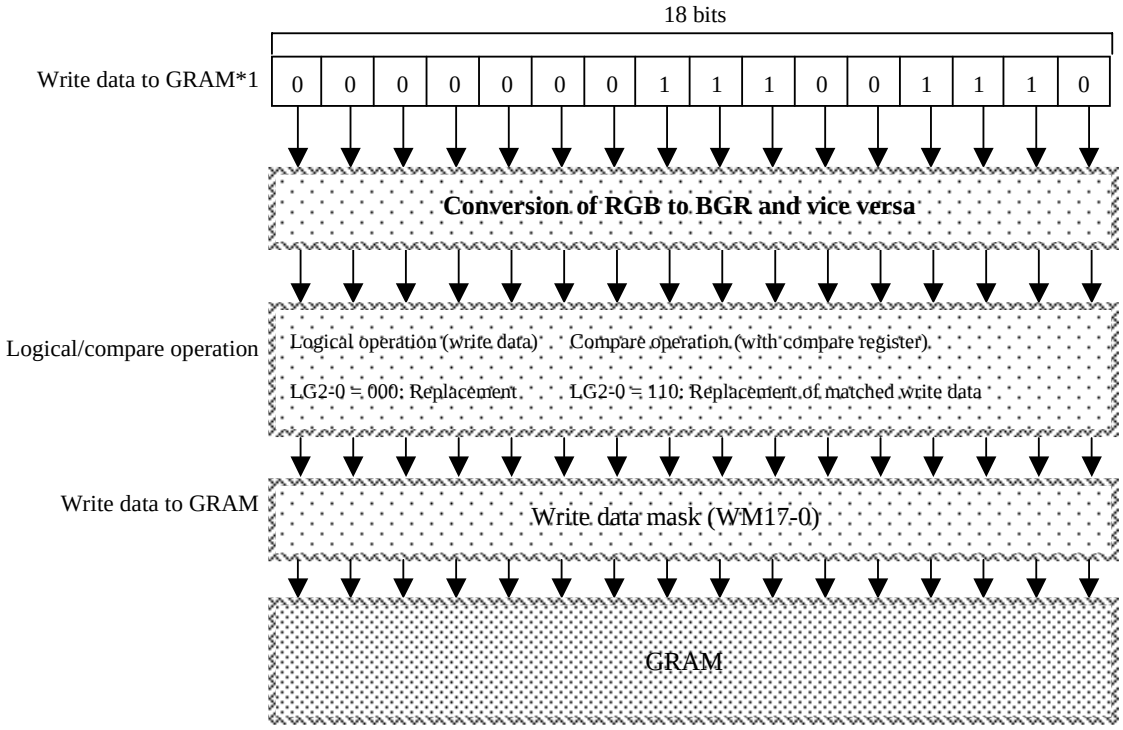
Figure 7 Address Direction Settings

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP17–0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

CP17–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

Note: This function is not available when the external display interface is in use. LG2 - 0 should be "000", respectively.

BGR: In the writing of 18 bits of data to RAM, this bit may be used to reverse the bit order from R, G, and B to B, G, and R. Please be aware that setting BGR to 1 will convert the order of the CP17-0 and WM17-0 bits in the same way.



Note1: Data is written to the GRAM in 18-bit units. Logical and compare operations are also performed in 18-bit units. For the bit assignment for each interface, see the section parallel transfer.

2: The write data mask (WM17-0) is set by the register in the RAM write data mask section.

Figure 8 Logical/Comparison Operation and Swapping for the GRAM

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VL	SPT	0	0	GON	DTE	CL	REV	D1	D0

Figure 9 Display Control Instruction 1

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the section on screen-division driving function.

Table 8 PT Bits

		Source Output for Non-Display Area		Gate Output for Non-Display Area
PT1	**PT0**	**Positive Polarity**	**Negative Polarity**	**Gate Driver Used**
0	0	V63	V0	Normal Drive
0	1	V63	V0	Vgoff
1	0	GND	GND	Vgoff
1	1	High impedance	High impedance	Vgoff

VLE2–1: When CL = 1, the first screen is vertically scrolled. When VLE2 = 1, the 2nd screen is vertically scrolled. It is not possible to simultaneously control the vertical scrolling of both screens.

Note: This function is not available when the external display interface is in use. In such a case, both VLE2 and 1 should be clear (0).

Table 9 VLE Bits

VLE2	**VLE1**	**Image on 1st Screen**	**Image on 2nd Screen**
0	0	Stationary	Stationary
0	1	Stationary	Scrolled
1	0	Scroll	Stationary
1	1	Setting disabled	Setting disabled

CL: VLE1 = 1 selects the eight color display mode. For details, see the section on the eight-color display mode.

Table 10 CL Bit

CL	**Number of Colors**
0	262,144
1	8

SPT: SPT = 1 selects the two-division driving of the LCD. For details, see the section on the screen-division driving function.

Note: This function is not available when the external display interface is in use. In such a case, SPT should be clear (0).

REV: REV = 1 selects the inversion of the display of all characters and graphics. For details, see the section on the inverted display function. Making it possible to invert the grayscale levels allows the display of the same data on both normally white and normally black panels.

The output on the source lines during the periods of the front and back porch and blanking of the partial display is determined by PT1-0.

Table 11 Source Output in the Display Area

REV	GRAM Data	Source Output in the Display Area* Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	⋮	⋮	⋮
	18'h3FFFFF	V0	V63
1	18'h00000	V0	V63
	⋮	⋮	⋮
	18'h3FFFFF	V63	V0

Note: The output on the source lines during the periods of the front and back porch and blanking of the partial display is determined by PT1-0.

GON: When GON = 0, the gate-off level will be GND.

DTE: When DTE = 0, the DISPTMG output will be fixed to GND.

Table 12 GON Bit

GON	Gate Output
0	Vgon/GND
1	Vgon/Vgoff

Table 13 DTE Bit

DTE	DISPTMG Output
0	Halt (GND)
1	Operation (Vcc/GND)

D1–0: The display is on when D1 = 1 and off when D1 = 0. When the display is off, the data for display is retained in the GRAM, and can instantly be redisplayed by setting D1 = 1. When D1 is 0 (i.e., the display is off) all of the source outputs are set to the GND level. This allows the HD66772 to control the charging current for the LCD during AC driving.

When D1–0 = 01, the internal display operations of the HD66772 continue although the actual display is off. When D1-0 = 00, the internal display operations halt and the display is also switched off.

These bits, in combination with GON and DTE, control the display. For details, see the section on the flow for setting instructions.

Table 14 D 1-0

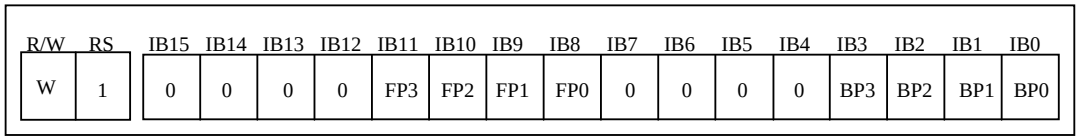
D1	D0	Source Output	HD67772 Internal Operations	Gate-Driver Control Signals (CL1, FLM, and M)l
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Note 2 : Data can be written to the GRAM from the microcomputer regardless of the contents of D1-0.

3 : In sleep and standby modes, "00" will be read. However, the contents of D1-0 before entering the sleep and standby modes will be held.

Note: The GON bit is used to set the gate driver. Control by the gate driver is according to this bit's value. For details, see the data sheet for the gate driver.

Display Control 2 (R08h)



R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

Figure 10 Display Control Instruction 2

FP3-0/BP3-0: Set the periods of blanking (the front and back porch), which are placed at the beginning and end of the display. FP3-0 are for a front porch and BP3-0 are for a back porch. When a front and back porch are set, the settings should meet the following conditions.

BP + FP = 16 raster-rows

FP ≥ 2 raster-rows

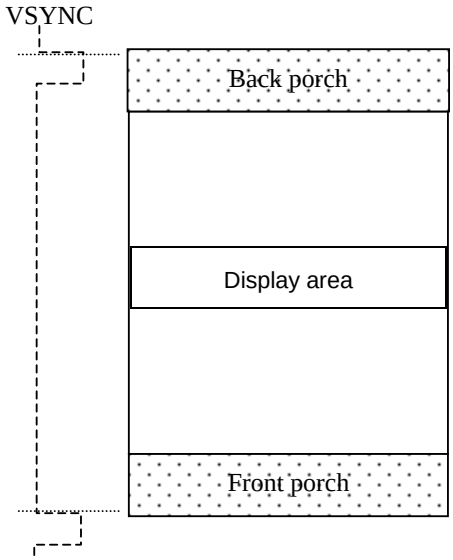
BP ≥ 2 raster-rows

When the external display interface is in use, the front porch (FP) will start on the falling edge of the VSYNC signal and display operation commences at the end of the front-porch period. The back porch (BP) will start when data for the number of raster-rows specified by the NL bits has been displayed. During the period between the completion of the back-porch period and the next VSYNC signal, the display will remain blank.

Note: In the internal clock operation mode, the blanking periods described above should be BP = 0011 (3 raster-rows) and FP = 0101 (5 raster-rows)

Table 15 FP and BP

FP3	**FP2**	**FP1**	**FP0**	**Number of Raster Periods in the Front Porch**
BP3	**BP2**	**BP1**	**BP0**	**Number of Raster Periods in the Back Porch**
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
	. .			. .
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting disabled



Note: The output timing to LCD panels displayed two raster-rows after the input synchronization signal.

Set BP3-0, FP3-0 within the range indicated below.

Table 16

Operation of internal clock	FLD1-0 = 01	BP>= 2 line	FP >= 2 line	FP +BP <= 16 line
	FLD1-0 = 11	BP= 3 line	FP = 5 line	
RGB interface		BP >= 2 line	FP >= 2 line	FP +BP <= 16 line
VSYNC interface		BP >= 2 line	FP >= 2 line	FP +BP = 16 line

Gate Driver Interface Control (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0
R	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0

Figure 11 Gate Driver Interface Control Instruction

IDX2-0: Index bits that select instructions for the gate-driver/power-supply IC. The instruction that corresponds to the setting made here is transferred, with the index, to the gate-driver/power-supply IC via the serial interface. These instructions are transferred in bit rows as shown below. The upper 3 bits correspond to IDX2-0. The IDX2-0 setting at the time of transfer selects the instruction for the gate-driver/power-supply IC as listed below.

To change an instruction setting on the gate-driver/power-supply IC, first change the instruction bit on the HD66772, select the instruction, which includes the changed instruction bit, from the list below, by setting IDX2-0 as required. The instruction is transferred to the gate-driver/power-supply IC as the transfer starts (TE=1), and is the executed**.**

TE: Serial transfer enable for the gate-driver/power-supply IC. When TE=0, serial transfer is possible. Do not change the instruction during transfer. When TE=1, transfer starts. TE returning to 0 indicates the end of the transfer. Note that, serial transfer to the gate-driver/power-supply IC requires 18 clock cycles at most. Do not change the instruction during the transfer.

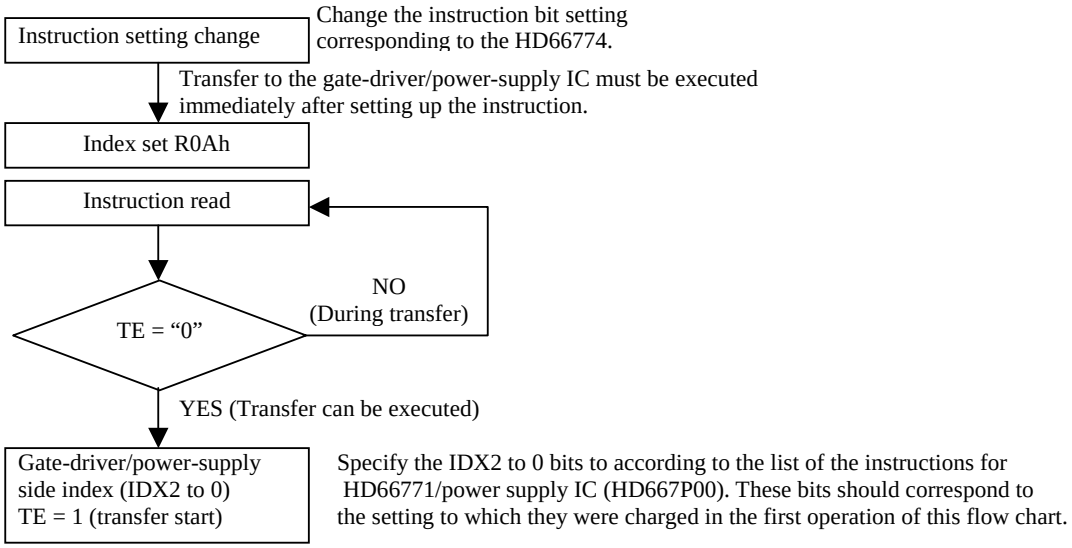
* New instructions should be transferred to the gate-driver/power-supply IC soon after they have been set on the HD66772.

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	GON	VCOMG	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP
0	0	1	CAD	VRL3	VRL2	VRL1	VRL0	PON	VRH3	VRH2	VRH1	VRH0	VC2	VC1	VC0
0	1	0	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	VCM4	VCM3	VCM2	VCM1	VCM0
0	1	1	Setting disabled												
1	0	0	Setting disabled												
1	0	1	Setting disabled												
1	1	0	EPL	0	GS	NL4	NL3	NL2	NL1	NL0	SCN4	SCN3	SCN2	SCN1	SCN0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	FLD1	FLD0

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	GON	VCOMG	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP
0	0	1	CAD	VRL3	VRL2	VRL1	VRL0	PON	VRH3	VRH2	VRH1	VRH0	VC2	VC1	VC0
0	1	0	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	VCM4	VCM3	VCM2	VCM1	VCM0
0	1	1	Setting disabled												
1	0	0	Setting disabled												
1	0	1	Setting disabled												
1	1	0	*	*	*	*	*	*	*	*	*	*	*	*	*
1	1	1	*	*	*	*	*	*	*	*	*	*	*	*	*

*These bits are registers for gate-driver IC.

Figure 12 Gate Interface: Serial Transfer Sequence



Note 1. Transfer to the gate-driver/power-supply IC must take place immediately after setting up the instruction.

Note 2. The serial transfer period takes a maximum of 1/fosc x 18clock cycles (sec).

Note 3. Serial transfer cannot be executed in standby mode. If the chip enters standby mode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again because correct transfer is not guaranteed in this situation.

Note 4. Serial transfer can be forcibly suspended by writing TE = 0. Transfer must be executed again because correct transfer is not guaranteed in this situation.

Note 5. Do not enter standby mode during transfer r forcibly terminate transfer except incase of emergency. Before executing, confirm that the transfer is completed.

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 13 Frame Cycle Control Instruction

RTN3-0: Set the 1H period (1 raster-row).

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN 3-0). When changing the number of raster-rows, adjust the frame frequency. For details, see the frame frequency adjustment Function section. When RGB interface is in use, this function will not be available.

Table 17 RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Clock Cycles per Raster-row
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
		:		:
1	1	1	0	30
1	1	1	1	31

Table 18 DIV Bits and Clock Frequency

DIV1	DIV0	Division Ratio	Internal Operating Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

* fosc = R-C oscillation frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line} + 16)} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency
Line: number of driven raster-rows (NL bit)
Division ratio: DIV bit
Clock cycles per raster-row: RTN bit

EQ1-0: Equalized period is added as specified by bits of EQ1-0. The equalization signal is output for AC raster-rows.

Table 19 EQ Bits

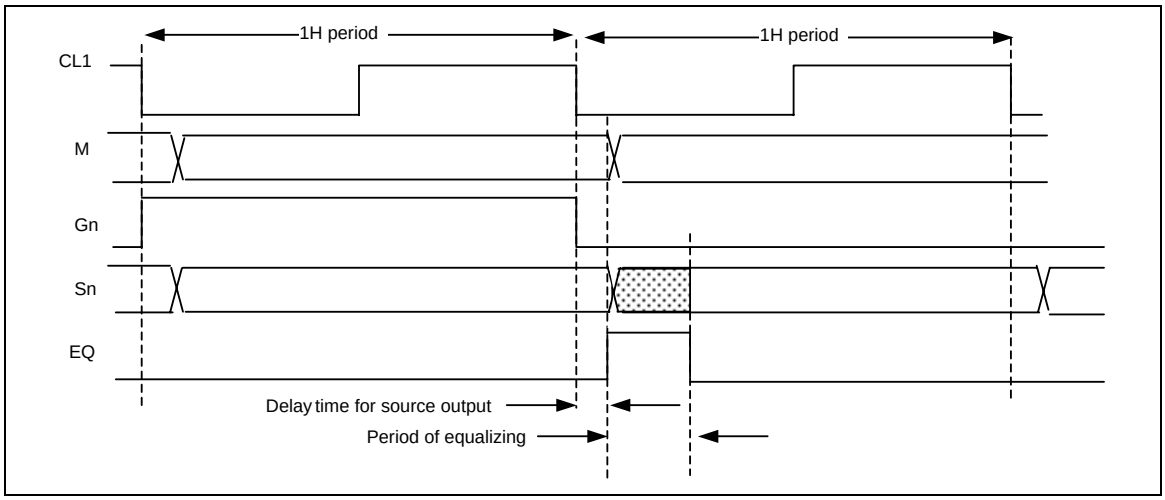
EQ1	EQ0	Equalized period: Internal Operation (synchronized with the internal operating clock)	Equalized period: RGB I/F Operation (synchronized with DOTCLK)
0	0	Not equalized	Not equalized
0	1	1 clock	8 clock
1	0	2 clock	16 clock
1	1	3 clock	24 clock

SDT1-0: Specify the timing on which a source signal is output after falling edge of a gate signal.

Table 20 SDT Bits

SDT1	SDT0	Delay Time for Source Signal Internal Operation (synchronized with the internal operating clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	1 clock	8 clock
0	1	2 clock	16 clock
1	0	3 clock	24 clock
1	1	4 clock	32 clock

Note: The amount of source delay is defined from the falling edge of the CL1.

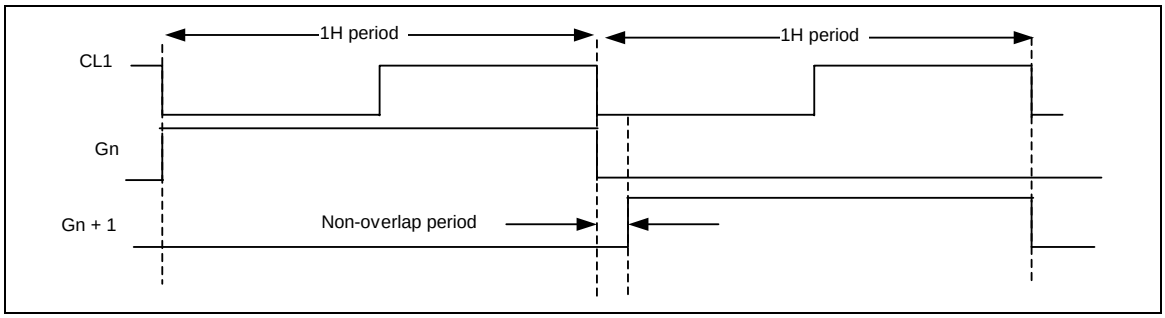


NO1-0: Specify the amount of non-overlap time.

Table 21 NO Bits

NO1	NO0	Non-overlap time Internal Operation (synchronized with the internal operating clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	0 clock	0 clock
0	1	4 clock	32 clock
1	0	6 clock	48 clock
1	1	8 clock	64 clock

Note: The amount of non-overlap time is defined from the falling edge of the CL1.



Note : The values specified by the bits of EQ,SDT1-0, and NO1-0 vary in a reference clock for each interface mode.

Internal operation mode	:	Internal R-C oscillation clock
RGB-I/F mode	:	DOTCLK
VSYNC-I/F	:	Internal R-C oscillation clock

External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM2	0	0	RIM1	RIM0

RIM1–0: Specify the RGB I/F mode when the RGB interface is used. Specifically, this setting specifies the mode when the bits of DM and RM are set to RGBI/F. These bits should be set before display operation through the RGB I/F and should not be set during operation.

Table 22 RIM Bits

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one-time transfer/pixel)
0	1	16-bit RGB interface (one-time transfer/pixel)
1	0	6-bit RGB interface (three-time transfers/pixel)
1	1	Setting disabled

DM1–0:.Specify the display operation mode. The interface can be set based on the bits of DM1-0. This setting enables switching interfaces between internal operation and the external display interface. Switching between two external display interfaces (RGB-I/F ad VSYNC-I/F) should not be done.

Table 23 DM Bits

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Specifies the interface for RAM accesses. RAM accesses can be performed through the interface specified by the bits of RM1-0. When the display data is written via the RGB-I/F, 1 should be set. This bit and the DM bits can be set independently. The display data can be rewritten via the system interface by clearing this bit while the RGB interface is used.

Table 24 RM Bits

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Depending on the external display interface settings, different interfaces for use can be specified to match the display state. While displaying moving pictures (RGB-I/F/VSYNC-I/F), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

Table 25 Display state and interfaces

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note 1 : The instruction register can only be set through the system interface.

2 : Switching between RGB-I/F and VSYNC-I/F cannot be done.

3 : The RGB-I/F mode should not be changed during RGB I/F operation.

4 : For the transition flow for each operation mode, see the External Display Interface section.

5 : RGB-I/F and VSYNC-I/F should be used in high-speed write mode (HWM = 1).

Internal clock operation mode

All the display operations are controlled by signals generated by the internal clock in internal clock operation mode. All inputs through the external display interface are invalid. The internal RAM can be accessed only via the system interface.

RGB interface mode (1)

The display operations are controlled by the frame synchronization clock (VSYNC), raster-row synchronization signal (VSYNC), and dot clock (DCLK) in RGB interface mode. These signals should be supplied during display operation in this mode.

The display data is transferred to the internal RAM via PD17-0 for each pixel. Combining the function of the high-speed write mode and the window address enables display of both the moving picture area and the internal RAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred.

The periods of the front (FP) and back (BP) porch and the display are automatically generated in the HD66772 by counting the raster-row synchronization signal (HSYNC) based on the frame synchronization signal (VSYNC). When pixel data is transferred via PD 17 to 0, the transfer should be operated according to the settings above.

RGB interface mode (2)

When RGB-I/F is in use, data can be written to RAM via the system interface. This write operation should be performed while data for display is not being transferred via RGB-I/F (ENABLE = High). Before the next data transfer for display via RGB-I/F, the setting above should be changed, and then the address and index (R22h) should be set.

VSYNC interface mode

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When data is written to the internal RAM with the required speed after the falling edge of VSYNC, moving pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

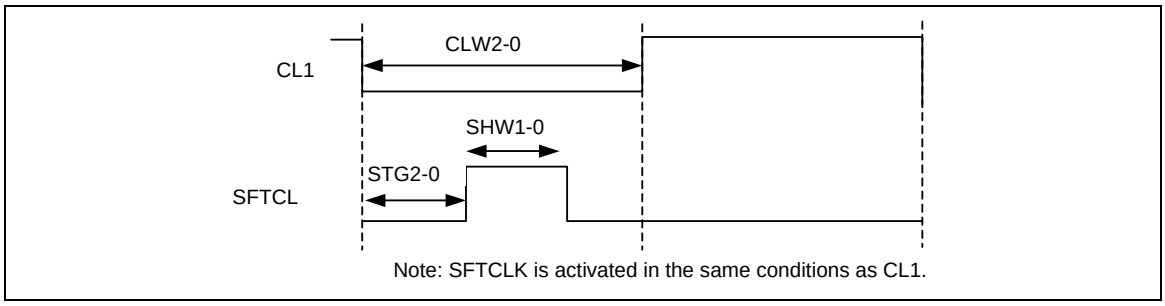
In VSYNC-I/F mode, only the VSYNC input is valid. The other input signals for the external display interface are invalid.

The periods of the front porch (FP), back porch (BP), and display period (NL) are automatically generated by the frame synchronization signal (VSYNC) according to the settings of the HD66772 registers.

LTPS Interface Control (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	CLW2	CLW1	CLW0	0	0	SHW1	SHW0	0	STG2	STG1	STG0

The HD66772 outputs timing signals for controlling a low-temperature poly-silicon TFT (LTPS-TFT) panel with built-in gates. The HD66772's output level is shifted to the LTPS-TFT level so that the HD66772 directly connects the LTPS-TFT. For details, see the section on LTPS-TFT control.



STG2–0: Specify the pulse output timing of the SFTCLK signal.

Table 26 STG Bits

			Pulse Output Timing of SFTCLK	
STG 2	**STG 1**	**STG 0**	**Internal Operation (Internal Clock)**	**RGB-I/F (DOTCLK)**
0	0	0	0 clock	0 clock
0	0	1	1 clock	8 clock
0	1	0	2 clock	16 clock
0	1	1	3 clock	24 clock
1	0	0	4 clock	32 clock
1	0	1	5 clock	40 clock
1	1	0	6 clock	48 clock
1	1	1	7 clock	56 clock

Note: The values indicate the number of clocks after the falling edge of CL1.

SHW1–0: Specify the high pulse width of the SFTCLK signal.

Table 27 SHW Bits

SHW 1	SHW 0	High Pulse Width of SFTCLK Internal Operation (Internal Clock)	RGB-I/F (DOTCLK)
0	0	1 clock	8 clock
0	1	2 clock	16 clock
1	0	3 clock	24 clock
1	1	4 clock	32 clock

Limitations on SFTCLK timing settings

STG2-0 + SHW1-0 ≤ 8 clock: Internal operation mode

STG2-0 + SHW1-0 ≤ 64 clock: RGB-I/F mode

CLW2–0: Specify the low pulse width of the CL1 signal.

Table 28 CLW Bits

CLW 2	CLW 1	CLW 0	Low Pulse Width of CL1 Internal Operation (Internal Clock)	RGB-I/F (DOTCLK)
0	0	0	1 clock	8 clock
0	0	1	2 clock	16 clock
0	1	0	3 clock	24 clock
0	1	1	4 clock	32 clock
1	0	0	5 clock	40 clock
1	0	1	6 clock	48 clock
1	1	0	7 clock	56 clock
1	1	1	8 clock	64 clock

Note: The values indicate the number of clocks after the falling edge of CL1.

Power Control 1 (R10h)
Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
W	1	CAD	0	0	VRN4	VRN3	VRN2	VRN1	VRN0	0	0	0	VRP4	VRP3	VRP2	VRP1	VRP0

Figure 14 Power Control Instruction

SAP2-0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the LCD. When the amount of fixed current is large, function of an operation amplifier stabilizes. But the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

During operation with no display, when SAP2–0 = 000, the current consumption can be reduced by halting the operational amplifier and step-up circuit operation.

Table 29 SAP Bits

SAP2	SAP1	SAP0	Op-amp Current
0	0	0	Halt
0	0	1	Small
0	1	0	Small/medium
0	1	1	Medium
1	0	0	Medium/large
1	0	1	Large
1	1	0	Setting disabled
1	1	1	Setting disabled

BT2–0: Switch the output factor for step-up. Adjust scale factor of the step-up circuit to meet the voltage used. Lower amplification of the step-up circuit consumes less current.

DC2–0: Select the operating frequency for the step-up circuit. When this frequency is high, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. Adjust the frequency by considering both the display quality and the current consumption.

AP2–0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the LCD. When the amount of fixed current is large, the LCD driving ability and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

During operation with no display, when AP2–0 = 000, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SLP: When SLP = 1, the HD66772 enters sleep mode, in which the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only serial transfer to a gate-driver/power-supply IC and the following instructions can be executed during sleep mode.

Power control (BS2–0, DC2–0, AP2–0, SLP, STB, VC2-0, CAD, VR3-0, VRL3-0, VRH4-0, VCOMG, VDV4-0, and VCM4-0 bits)

Common interface control (TE, IDX)

During sleep mode, other GRAM data and instructions cannot be updated, although they are retained.

STB: When STB = 1, the HD66772 enters standby mode, in which display operation completely stops, halting all internal operations including the internal R-C oscillator. In addition, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during standby mode.

a. Standby mode cancel (STB = 0)

b. Start oscillation

During standby mode, GRAM data and instructions may be lost. To prevent this, they must be set again after standby mode is canceled. Serial transfer to the common driver is not possible when it is in standby mode. Transfer the data again after standby mode is canceled.

CAD: Set according to the configuration of the TFT

CAD = 0 Set when Cst is set.

CAD = 1 Set when Cadd is set.

VRP4-0: Controls the 64-grayscale amplitude (positive polarity). For details, see the section on the instruction bits for the amplitude adjustment circuit.

VRN4-0: Controls the 64-grayscale amplitude (negative polarity). For details, see the section on the instruction bits for the amplitude adjustment circuit.

Note: The BS2-0, DC2-0, AP2-0, SLP, and CAD bits are for setting the power-supply IC. Control based on the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

Power Control 3 (R12h)

Power Control 4 (R13h)

Power Control 5 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
W	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

VC2-0: The reference voltages of VREG1OUT, VREG2OUT, and VciOUT can be set to any voltage specified by the ratio of Vci. When VC2 = "1", it is possible to stop the internal reference voltage generator. This setting enables VREG1OUT and VREG2OUT to generate any voltage by using REGP and REGN as reference voltages, respectively.

VRL3-0: Sets an amplification factor for VREG2OUT, which is a voltage for the reference voltage VREG2 to generate Vgoff. The amplification factor can be set to -2 to -8.5 times the REGN input.

PON: Operation start bit for the step-up 3 circuit. PON = 0 is to stop and PON = 1 is to start operation.

VRH3-0: Sets an amplification factor for VREG1OUT, which is a voltage for the reference voltage VREG2 to generate VDH. The amplification factor can be set to 1.45 to 2.85 times the REGP input.

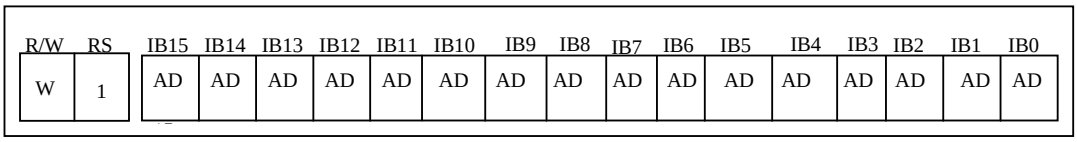
VCOMG: When VCOMG = 1, VcomL can output a negative voltage of up to -5 V. When VCOMG = 0, VcomL is at GND level and amplifiers for a negative voltage stop. This reduces power consumption. When VCOMG = 0 and Vcom AC drive is performed, the settings for VDV4-0 are invalid. In this case, adjust the AC amplification of the Vcom and Vgoff with VcomH using VCM 4-0.

VDV4-0: Sets amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. The amplification factors can be set to 0.6 to 1.23 times the VREG1 input. When Vcom AC drive is not performed, the settings are invalid.

VCM4-0: Sets the VcomH voltage, which is positive when Vcom AC drive is being performed. The amplification factor can be set to 0.4 to 0.98 times the VREG1 input. Setting VCM4-0 to "1111" stops the internal resistor adjustment, and the external resistor connected to VcomR can be used to adjust VcomH.

Note: The VC2-0, VRL3-0, PON, VRH3-0, VCOMG, VDV4-0, and VCM4-0 bits are for the power-supply IC. Control according to the bits' values is executed by the power-supply IC. For details, see the data sheet for the power-supply IC.

RAM Address Set (R21h)



R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD

Figure 15 RAM Address Set Instructions

AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting the addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in standby mode. Ensure that the address is set within the specified window address.

When RGB-I/F is in use (RM = 1), AD15-0 will be set at the falling edge of the VSYNC signal.

When the internal clock operation and VSYNC-I/F (RM = 1) are in use, AD15-0 will be set upon execution of an instruction.

Table 30 GRAM Address Range

AD15–AD0	GRAM Setting
0000H – 00AFH	Bitmap data for G1
0100H – 01AFH	Bitmap data for G2
0200H – 02AFH	Bitmap data for G3
0300H – 03AFH	Bitmap data for G4
:	:
EC00H – ECAFH	Bitmap data for G237
ED00H – EDAFH	Bitmap data for G238
EE00H – EEAFH	Bitmap data for G239
EF00H – EFAFH	Bitmap data for G240

Write Data to GRAM (R22h)

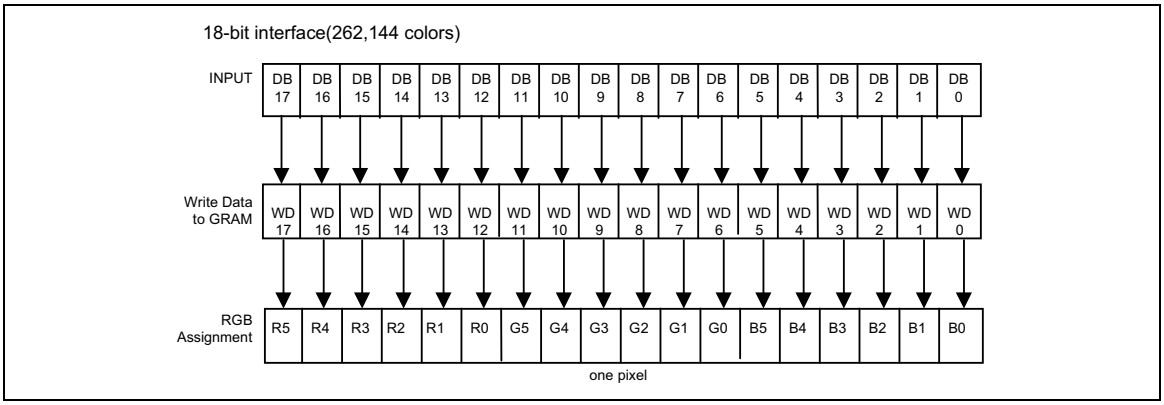
	R/W	RS	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
	W	1	RAM write data (WD17-0) The pin assignment for DB17-0 varies for each interface (see below).															
When RGB-I/F	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD	WD		

WD17–10: GRAM data is expanded to 18 bits to be written. Please keep in mind that the expansion format varies for each interface.

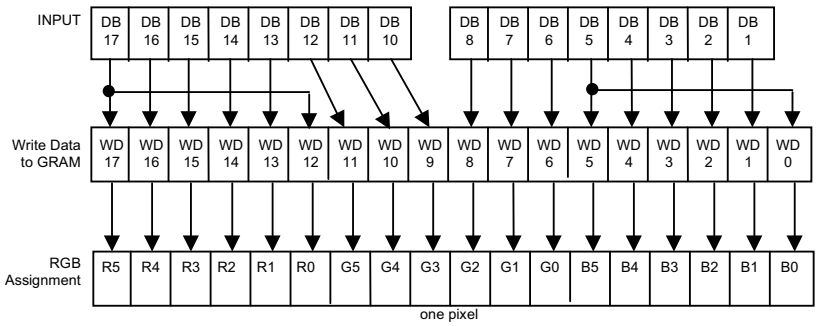
The grayscale level is determined by the GRAM data. The address is automatically updated by the bits of AM and I/D after GRAM writing. GRAM cannot be accessed in standby mode. When the 8- or 16-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the RB data to its LSB.

When data is written to RAM used by RGB-I/F via the system interface, please make sure that write data conflicts do not occur.

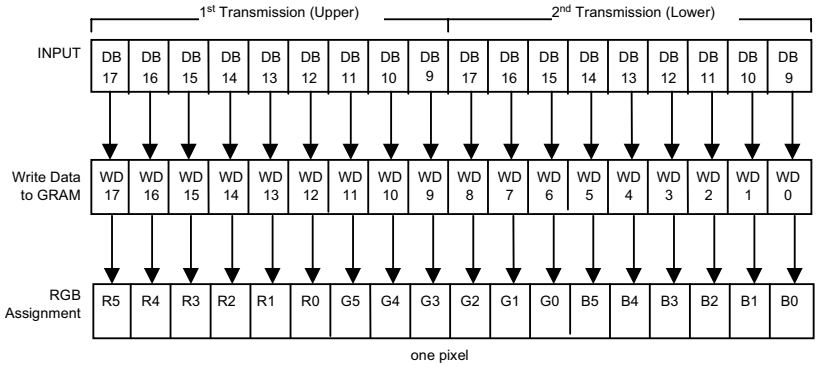
When the 18-bit RGB-I/F is in use, 18-bit data is written to RAM via PD17-0 and 262,144 colors are available. When the 16-bit RGB-I/F is in use, the MSB is written to its LSB and 65,536 colors are available.



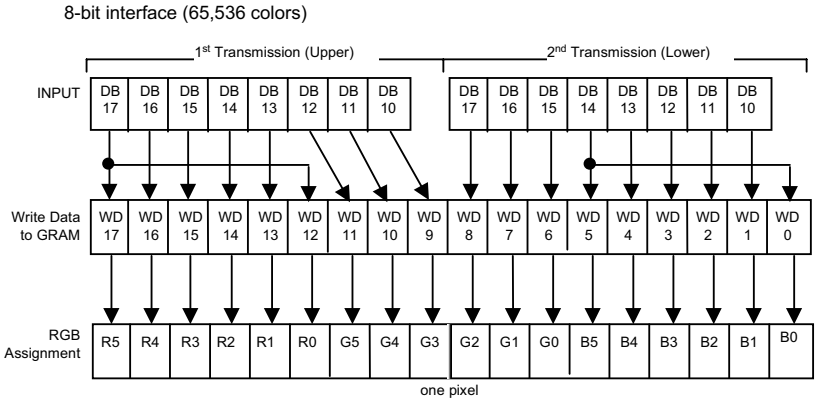
16-bit interface(65,536 colors)



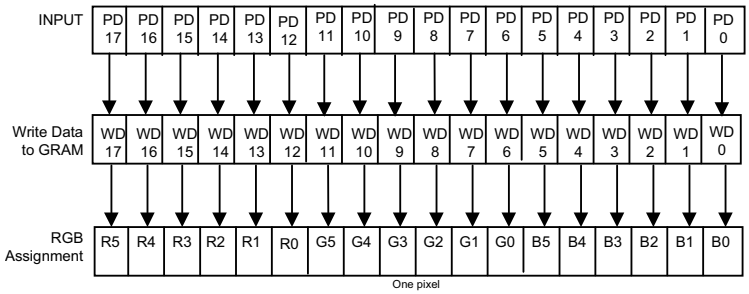
9-bit interface (262,144 colors)



8-bit interface (65,536 colors)

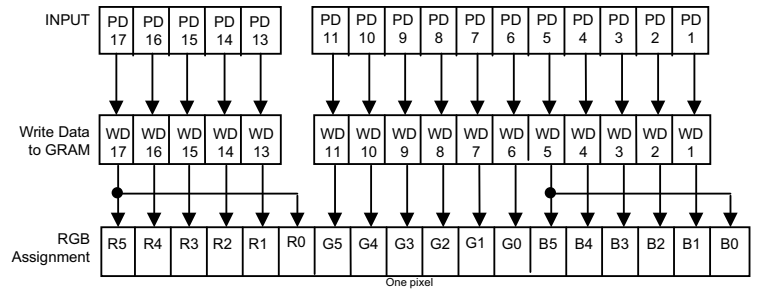


18-bit RGB interface (262,144 colors)



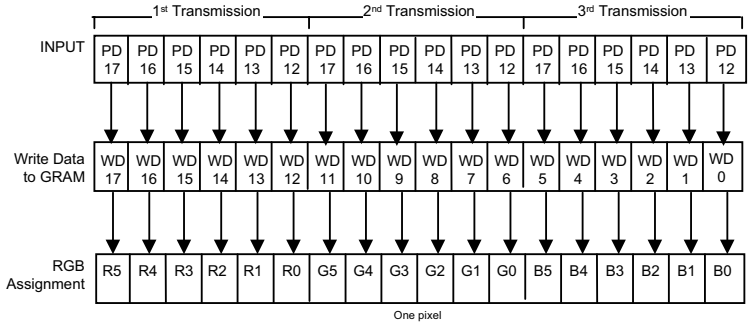
Set the index register when writing data through an RGB interface.

16-bit RGB interface (65,563 colors)



Set the index register when writing data through an RGB interface.

6-bit RGB interface (262,144 colors)



Set the index register when writing data through an RGB interface.

Table 31 GRAM Data and LCD Output

GRAM Data Setting	Grayscale Polarity		GRAM Data Setting	Grayscale Polarity	
RGB	Negative	Positive	RGB	Negative	Positive
000000	V0	V63	100000	V32	V31
000001	V1	V62	100001	V33	V30
000010	V2	V61	100010	V34	V29
000011	V3	V60	100011	V35	V28
000100	V4	V59	100100	V36	V27
000101	V5	V58	100101	V37	V26
000110	V6	V57	100110	V38	V25
000111	V7	V56	100111	V39	V24
001000	V8	V55	101000	V40	V23
001001	V9	V54	101001	V41	V22
001010	V10	V53	101010	V42	V21
001011	V11	V52	101011	V43	V20
001100	V12	V51	101100	V44	V19
001101	V13	V50	101101	V45	V18
001110	V14	V49	111110	V46	V17
001111	V15	V48	111111	V47	V16
010000	V16	V47	110000	V48	V15
010001	V17	V46	110001	V49	V14
010010	V18	V45	110010	V50	V13
010011	V19	V44	110011	V51	V12
010100	V20	V43	110100	V52	V11
010101	V21	V42	110101	V53	V10
010110	V22	V41	110110	V54	V9
010111	V23	V40	110111	V55	V8
011000	V24	V39	111000	V56	V7
011001	V25	V38	111001	V57	V6
011010	V26	V37	111010	V58	V5
011011	V27	V36	111011	V59	V4
011100	V28	V35	111100	V60	V3
011101	V29	V34	111101	V61	V2
011110	V30	V33	111110	V62	V1
011111	V31	V32	111111	V63	V0

RAM Access via RGB-I/F and System I/F

All the data for display is written to the internal RAM in the HD66772 when RGB-I/F is in use. In this method, data, including that in both the moving picture area and the screen update frame, can only be transferred via RGB-I/F. In addition to using the high-speed write mode (HWM = 1) and the window address function, the power consumption can be reduced and high-speed access can be achieved while moving pictures are being displayed. Data for display that is not in the moving picture area or the screen update frame can be rewritten via the system interface.

RAM can be accessed via the system interface when RGB-I/F is in use. When data is written to RAM during RGB-I/F mode, the ENABLE bit should be high to stop data writing via RGB-I/F, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is low. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB-I/F. When a RAM write conflict occurs, data writing is not guaranteed.

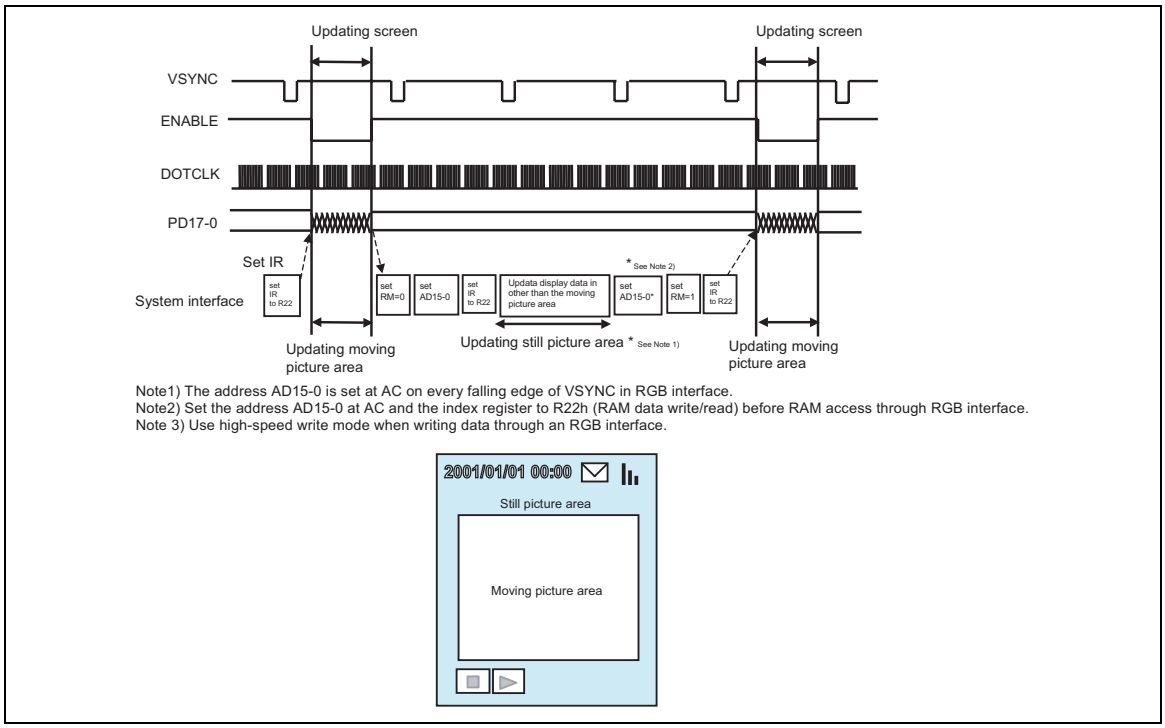


Figure 16 Example of Updating Still Picture Area during Displaying Moving Picture

Read Data from GRAM (R22h)

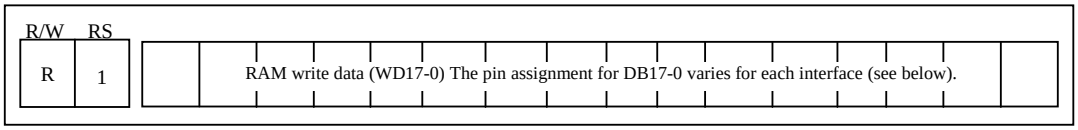


Figure 17 Read Data from GRAM Instructions

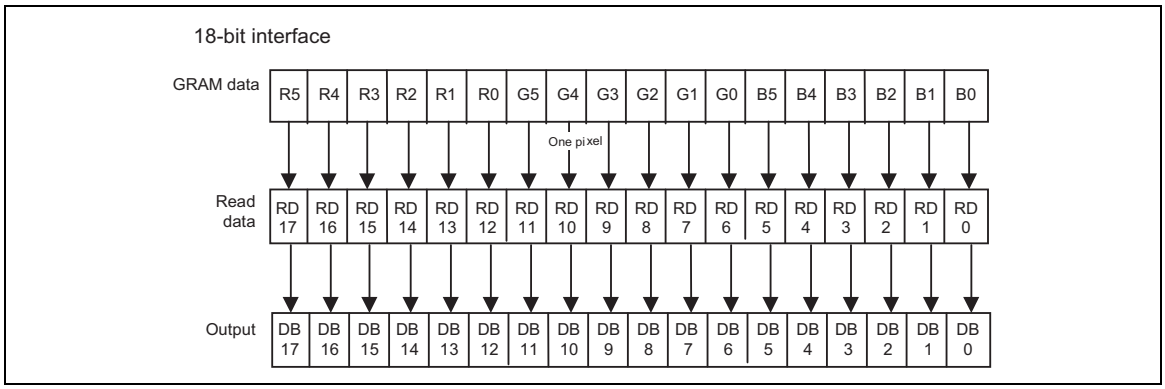
RD17–0: Read 18-bit data from GRAM.

When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data in the data bus (DB17–0) becomes invalid and the second-word read is normal.

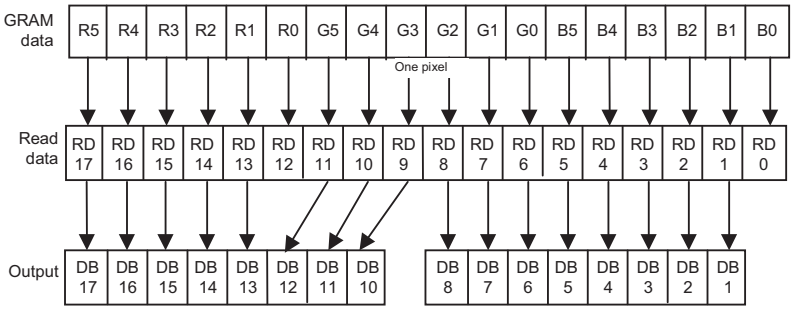
When bit processing, such as a logical operation, is performed by the HD66772, only one read can be processed since the latched data in the first word is used. Please make sure bit processing is performed in 18-bit units.

When the 8-/16-bit interface is in use, the LSB of RB write data will not be read.

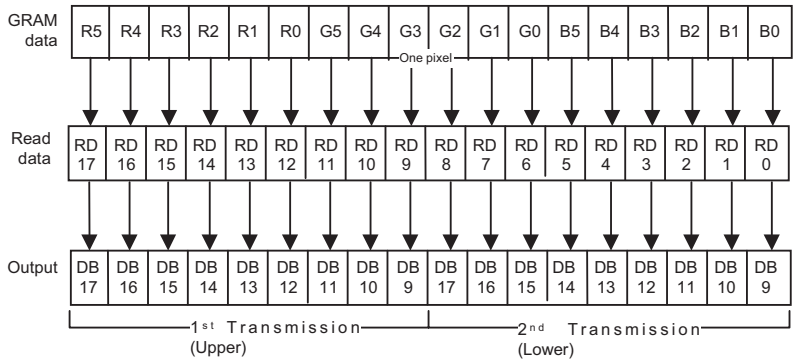
When RGB-I/F is in use, this function is not available.



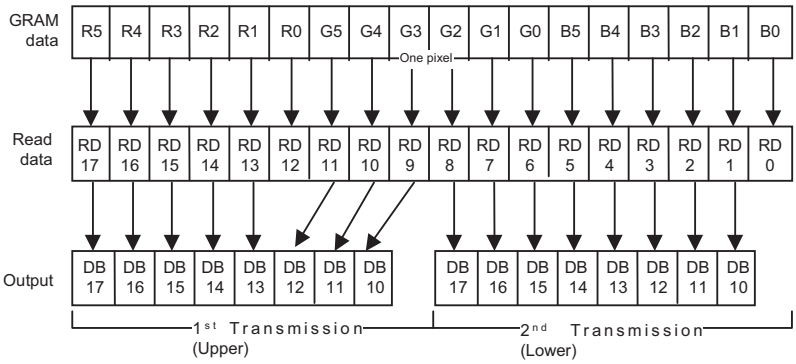
16-bit interface



9-bit interface



8-bit interface / SPI



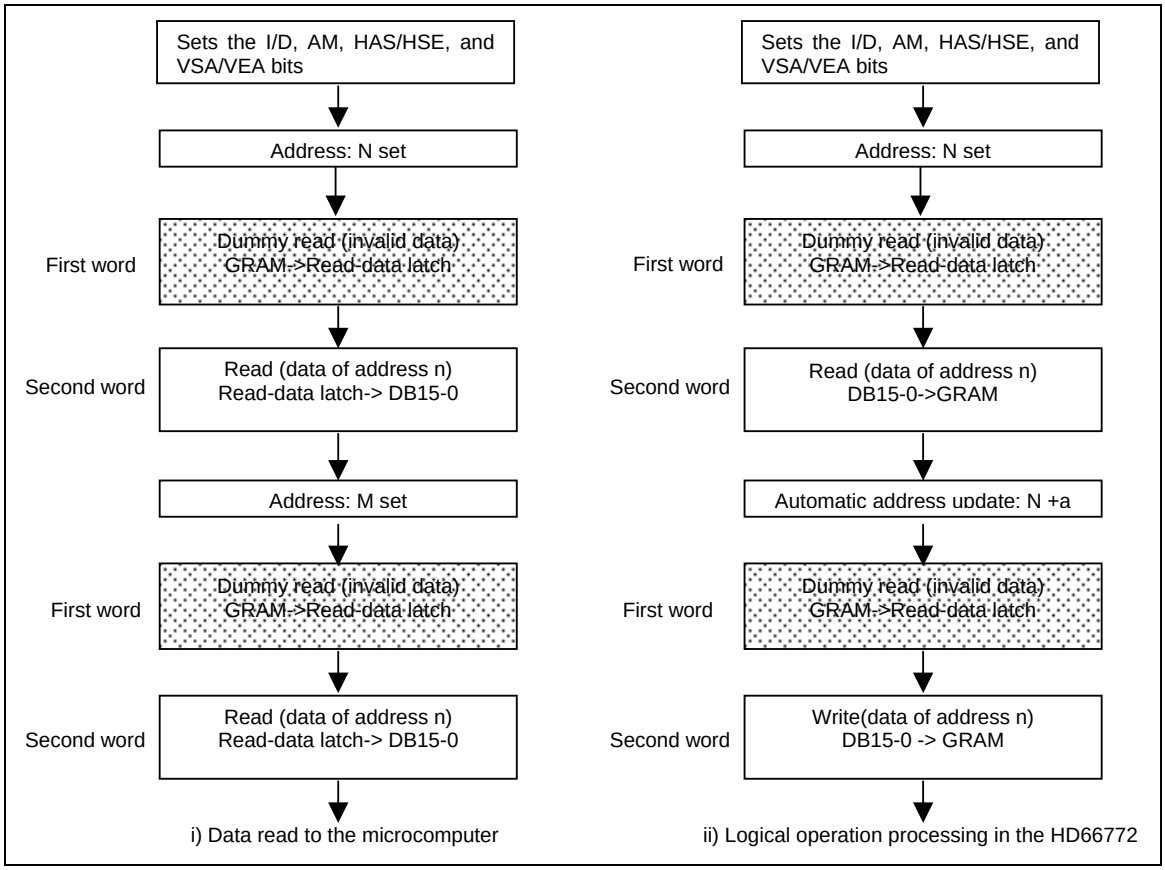


Figure 18 GRAM Read Sequence

RAM Write Data Mask (R23h)

RAM Write Data Mask (R24h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	WM	WM	WM	WM	WM	WM	0	0	WM	WM	WM	WM	WM	WM
W	1	0	0	0	0	0	1	1	1	0	1	WM	WM	WM	WM	WM	WM

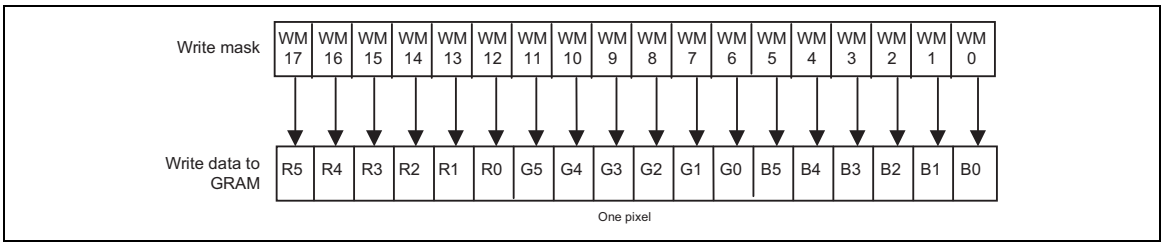
Figure 19 RAM Write Data Mask Instructions

WM17–0: In writing to GRAM, these bits mask the writing in a bit unit. When WM17 = 1, this bit masks the MSB of the write data and does not write to GRAM. Similarly, the WM14–0 bits mask the data written to GRAM in a bit unit. For details, see the Graphics Operation Function section.

Please make sure the write data to GRAM (18-bit data) is masked.

When the 8-/16-bit interface is in use, the LSB of RB write data will not be read.

When RGB-I/F is in use, this function is not available.



γ Control Instructions

γ Control (R30h to R3Fh)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP	PKP	PKP	0	0	0	0	0	PKP	PKP	PKP
R31	W	1	0	0	0	0	0	PKP	PKP	PKP	0	0	0	0	0	PKP	PKP	PKP
R31	W	1	0	0	0	0	0	PKP	PKP	PKP	0	0	0	0	0	PKP	PKP	PKP
R33	W	1	0	0	0	0	0	PRP	PRP	PRP	0	0	0	0	0	PRP	PRP	PRP
R34	W	1	0	0	0	0	0	PKN	PKN	PKN	0	0	0	0	0	PKN	PKN	PKN
R35	W	1	0	0	0	0	0	PKN	PKN	PKN	0	0	0	0	0	PKN	PKN	PKN
R36	W	1	0	0	0	0	0	PKN	PKN	PKN	0	0	0	0	0	PKN	PKN	PKN
R37	W	1	0	0	0	0	0	PRN	PRN	PR N	0	0	0	0	0	PRN	PRN	PRN
R3F	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VDR	VDR

Figure 20 γ Control Instructions

PKP52-00 :The γ fine adjustment registers for positive polarity

PRP12-00 :The γ gradient adjustment registers for positive polarity

PKNP52-00:The γ fine adjustment registers for negative polarity

PRN12-00:The γ gradient adjustment registers for negative polarity

VDR1-0:The grayscale average adjustment resistor.

For details, see the section on the γ adjustment

Position Control Instructions

Gate Scan Position (R40h)

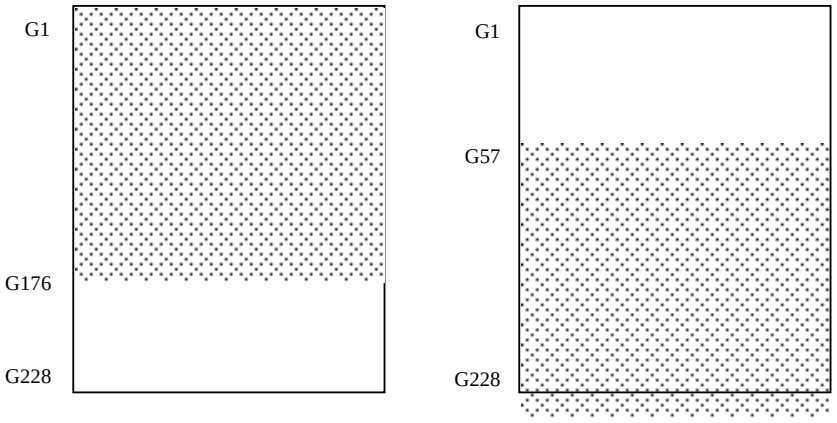
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 21 Gate Scan Position Instructions

SCN4-0: Specifies the position at which gate driver scanning starts. Set the data to match the gate driver's specification.

Table 32 SCN Bits (Example of HD66772)

					Scan Start Position	
SC4	**SC3**	**SC2**	**SC1**	**SC0**	**GS = 0**	**GS = 1**
0	0	0	0	0	G1	G228
0	0	0	0	1	G9	G220
0	0	0	1	0	G17	G212
. .	. .	. .	. .	. .	. .	. .
1	1	0	1	0	G209	G20
1	1	0	1	1	G217	G12



GS = 0
NL = 10101
SCM4-0 = 00000

GS = 0
NL = 10101
SCM4-0 = 00111

Note: Set the value so that the sum of NL and the end point of the gate scan are 2323 or less.

Figure 22 Relationship between NL and SCL Set Values

Note: The SCN4-0 bits are for setting the gate driver. Control based on the bits' values is executed by the gate driver. For details, see the data sheet for the gate driver.

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 23 Vertical Scroll Control Instructions

VL7–10: Specify the amount of scroll in the display to enable smooth vertical scrolling. Any raster-row from 0 to 240 can be displayed with scrolling. After the 240th raster-row is displayed, the display restarts from the 1st raster-row. The display-start raster-row (VL7–10) is valid only when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00. (VLE1 is the 1st-screen vertical-scroll enable bit, and VLE2 is the 2nd-screen vertical-scroll enable bit.)

*: When the external display interface is in use, this function is not available.

Table 33 VL Bits and Display-start Raster-row

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Amount of Scrolling (Number of raster-row)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	0	1	0	1	1	1	0	238
1	0	1	0	1	1	1	1	239

Note: Do not set to over 239 (EFh) raster-rows.

1st-Screen Driving Position (R42h)

2nd-Screen Driving Position (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20

Figure 24 1st-Screen Driving Position and 2nd-Screen Driving Position Instructions

SS17–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver.

SE17–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS17–10 = 07H and SE17–10 = 10H are set, the LCD driving is performed from G8 to G17, and non-selection driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ EFH. For details, see the Screen-division Driving Function section.

SS27–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver. The second screen is driven when SPT = 1.

SE27–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SPT = 1, SS27–20 = 20H, and SE27–20 = 4FH are set, the LCD driving is performed from G33 to G80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ EFH. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R44h)

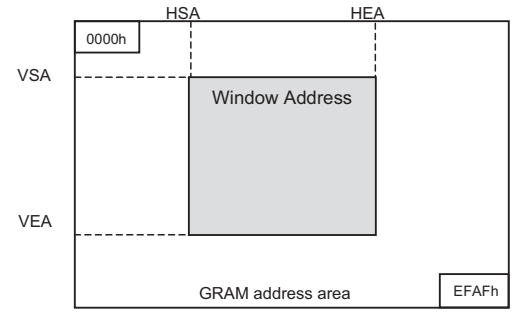
Vertical RAM Address Position (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 25 Horizontal/Vertical RAM Address Position Instructions

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ AFh.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ VSA7-0 ≤ VEA7-0 ≤ EFh.



Note 1. Ensure that the window address area is within the GRAM address space.
2. In high-speed write mode, data are written to GRAM in four-words. Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.
3. Set RAM address within the window address area. In high-speed write mode, set RAM address within the area containing dummy area. For details, see the High-Speed Burst RAM Write Function section.

Instruction List

Table 34

	Reg. No	Register name	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Index	–	Index	*	*	*	*	*	*	*	*	*	*	IB5	IB4	IB3	IB2	IB1	IB0
Status read	–	Status read	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
Display control	00 h	Start oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
		Device code read	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	0
	01 h	Driver output control	0	0	0	0	EPL (0)	0	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (1)
	02 h	LCD-driving-waveform	0	0	0	0	FLI1 (0)	FLI0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)
	03 h	Entry mode	0	0	0	BGR (0)	0	0	HWM (0)	0	0	0	ID1 (1)	ID0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)
	04 h	Compare register 1	0	0	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)
	05 h	Compare register 2	0	0	0	0	0	0	0	0	0	0	CP17 (0)	CP16 (0)	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)
	06 h	Setting disabled																
	07 h	Display control 1	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)
	08 h	Display control 2	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
	09 h	Setting disabled																
	0 Ah	Gate driver interface control	0	0	0	0	0	0	0	TE (0)	0	0	0	0	0	IDX2 (0)	IDX1 (0)	IDX0 (0)
	0 Bh	Frame cycle control	NO1 (0)	NO0 (0)	SDT1 (0)	SDT0 (0)	EQ1 (0)	EQ0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)
	0 Ch	External display interface control	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)
	0 Dh	LTPS interface control	0	0	0	0	0	CLV2 (1)	CLV1 (1)	CLV0 (1)	0	0	SHV1 (0)	SHV0 (0)	0	STG2 (0)	STG1 (0)	STG0 (0)
	0 Eh	Setting disabled																
	0 Fh	Setting disabled																
Power Control	10 h	Power control 1	0	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	BT2 (0)	BT1 (0)	BT0 (0)	DC2 (0)	DC1 (0)	DC0 (0)	AP2 (0)	AP1 (0)	AP0 (0)	SLP (0)	STB (0)
	11 h	Power control 2	CAD (0)	0	0	VRN4 (0)	VRN3 (0)	VRN2 (0)	VRN1 (0)	VRN0 (0)	0	0	0	VRP4 (0)	VRP3 (0)	VRP2 (0)	VRP1 (0)	VRP0 (0)
	12 h	Power control 3	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2 (0)	VC1 (0)	VC0 (0)
	13 h	Power control 4	0	0	0	0	VRL3 (0)	VRL2 (0)	VRL1 (0)	VRL0 (0)	0	0	0	PCN (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)
	14 h	Power control 5	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)
	15 h	Setting disabled																
	16 h	Setting disabled																
	17 h	Setting disabled																
	18 h	Setting disabled																
	19 h	Setting disabled																
	1 Ah	Setting disabled																
	1 Bh	Setting disabled																
	1 Ch	Setting disabled																
	1 Dh	Setting disabled																
	1 Eh	Setting disabled																
	1 Fh	Setting disabled																
RAM Access	20 h	Setting disabled																
	21 h	RAM address set	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
	22 h	RAM data write/ read	RAM write data (WD17-0)/ RAM read data (RD17-0) : Bit assignment varies for selected interface.															
	23 h	RAM data write mask 1	0	0	WM1 (0)	WM0 (0)	WM8 (0)	WM6 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM8 (0)	WM2 (0)	WM1 (0)	WM0 (0)
	24 h	RAM data write mask 2	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)
	25 h	Setting disabled																
	26 h	Setting disabled																
	27 h	Setting disabled																
	28 h	Setting disabled																
	29 h	Setting disabled																
	2 Ah	Setting disabled																
	2 Bh	Setting disabled																
	2 Ch	Setting disabled																
	2 Dh	Setting disabled																
	2 Eh	Setting disabled																
	2 Fh	Setting disabled																

Note 1: Parenthitic numbers are the initial values for each bit.

Note 2: Do not access the instructions which is described above that setting is disabled.

Table 34 (continued)

γ Control	30 h	γ Control 1	0	0	0	0	0	PKP12 (0)	PKP11 (0)	PKP10 (0)	0	0	0	0	0	PKP02 (0)	PKP01 (0)	PKP00 (0)
	31 h	γ Control 2	0	0	0	0	0	PKP32 (0)	PKP31 (0)	PKP30 (0)	0	0	0	0	0	PKP22 (0)	PKP21 (0)	PKP20 (0)
	32 h	γ Control 3	0	0	0	0	0	PKP52 (0)	PKP51 (0)	PKP50 (0)	0	0	0	0	0	PKP42 (0)	PKP41 (0)	PKP40 (0)
	33 h	γ Control 4	0	0	0	0	0	PRP12 (0)	PRP11 (0)	PRP10 (0)	0	0	0	0	0	PRP02 (0)	PRP01 (0)	PRP00 (0)
	34 h	γ Control 5	0	0	0	0	0	PKN12 (0)	PKN11 (0)	PKN10 (0)	0	0	0	0	0	PKN02 (0)	PKN01 (0)	PKN00 (0)
	35 h	γ Control 6	0	0	0	0	0	PKN32 (0)	PKN31 (0)	PKN30 (0)	0	0	0	0	0	PKN22 (0)	PKN21 (0)	PKN20 (0)
	36 h	γ Control 7	0	0	0	0	0	PKN52 (0)	PKN51 (0)	PKN50 (0)	0	0	0	0	0	PKN42 (0)	PKN41 (0)	PKN40 (0)
	37 h	γ Control 8	0	0	0	0	0	PRN12 (0)	PRN11 (0)	PRN10 (0)	0	0	0	0	0	PRN02 (0)	PRN01 (0)	PRN00 (0)
	38 h	Setting disabled																
	39 h	Setting disabled																
	3 Ah	Setting disabled																
	3 Bh	Setting disabled																
	3 Ch	Setting disabled																
	3 Dh	Setting disabled																
	3 Eh	Setting disabled																
	3 Fh	γ Control 9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VDR11 (0)	VDR10 (0)
Position Control	40 h	Gate scan start position	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
	41 h	Vertical scroll control	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
	42 h	1 st screen driving position	SE17 (1)	SE16 (1)	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
	43 h	2 nd screen driving position	SE27 (1)	SE26 (1)	SE25 (1)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)
	44 h	Horizontal RAM address position	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
	45 h	Vertical RAM address position	VEA7 (1)	VEA6 (1)	VEA5 (1)	VEA4 (0)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
	46 h	Setting disabled																
	47 h	Setting disabled																
	48 h	Setting disabled																
	49 h	Setting disabled																
	4 Ah	Setting disabled																
	4 Bh	Setting disabled																
	4 Ch	Setting disabled																
	4 Dh	Setting disabled																
	4 Eh	Setting disabled																
	4 Fh	Setting disabled																
	*	Setting disabled																
	*	Setting disabled																
	*	Setting disabled																

Note 1: Parenthitic numbers are the initial values for each bit.
Note 2: Do not access the instructions which is described above that setting is disabled.

Reset Function

The HD66772 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period, no instruction or GRAM data access from the MPU is accepted. Reset the gate-driver/power-supply IC as its settings are not automatically reinitialized when the HD66772 is reset. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 11101, SS = 0, GS = 0, EPL = “0”)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
4. Entry mode set (HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode, BGR = 0)
5. Compare register (CP17–0: 00 0000 0000 0000 0000)
6. Display control 1 (PT1-0 = 00, VLE2-1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL = 0: 65536-color mode, REV = 0, D1–0 = 00: Display off)
7. Display control 2 (BP3-0 = 1000, FP3-0 = 1000)
8. Gate driver interface control (TE = 0, IDX2-0 = 000)
9. Frame cycle control (NO1-0 = 00, SDT1-0 = 00, EQ1-0 = 00: No equalization, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clocks in 1H period)
10. External display interface (RIM1-0 = 00: 18-bit RGB interface, DM1-0 = 00: Operated by internal operating clock, RM = 0: System interface)
11. LTPS interface control (STG2-0 = 000, SHW1-0 = 00, CLW2-0 = 000)
12. Power control 1 (SAP2-0 = 000, BT2-0 = 000, DC2–0 = 000, AP2–0 = 000: LCD power off, SLP = 0, STB = 0: Standby mode off)
13. Power control 2 (CAD = 0, VRN4-0 = 00000, VR4-0 = 00000)
14. Power control 3 (VC2-0 = 000)
15. Power control 4 (VRL3-0 = 0000, PON = 0, VRH3-0 = 0000)
16. Power control 5 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
17. RAM address set (AD15–0 = 0000H)
18. RAM write data mask (WM17–0 = 18’h00000: No mask)
19. γ control
    (PKP02-00 = 000, PKP12-10 = 000, PKP22-20 = 000, PKP32-30 = 000,
    PKP42-40 = 000, PKP52-50 = 000, PRP02-00 = 000, PRP12-10 = 000,
    PKN02-00 = 000, PKN12-10 = 000, PKN22-20 = 000, PKN32-30 = 000,
    PKN42-40 = 000, PKN52-50 = 000, PRN02-00 = 000, PRN12-10 = 000)
20. Gate scan starting position (SCN4-0 = 00000)
21. Vertical scroll (VL7–0 = 00000000)
22. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
23. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
24. Horizontal RAM address position (HEA7-0 = 10000011, HSA7-0 = 00000000)
25. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

Output Pin Initialization:

1. LCD driver output pins (source outputs): Output GND level
2. Oscillator output pin (OSC2): Outputs oscillation signal
3. Gate interface signals (GCS*, GCL, and GDA): Halt
4. Timing signals (CL1, M, FLM, DISPTMG, and DCCLK): Halt

Interface Specifications

The HD66772 incorporates a system interface, which is used to set instructions, and an external display interface, which is used to display moving pictures. Selecting these interfaces to match the screen data (moving or still) enables efficient transfer of data for display.

The external display interface includes RGB-I/F and VSYNC-I/F. This allows flicker-free screen update.

When RGB-I/F is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The data for display (PD17-0) is written according to the values of the data enable signal (ENABLE) and data valid signal (VLD), in synchronization with the VSYNC, HSYNC, and DOTCLK signals. The data for display is written to GRAM, so that data transfer is reduced only when switching the screen. In addition, using the window address function enables rewriting only to the internal RAM area to display moving pictures. Using this function also enables simultaneously display of the moving picture area and the RAM data that was written.

While displaying moving pictures, the data for display should be written in high-speed write mode, which achieves both low power consumption and high-speed access via RGB-I/F or VSYNC-I/F.

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When writing to the internal RAM is done within the required time after the falling edge of VSYNC, moving pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

The HD66772 has four operation modes for each display state. These settings are specified by control instructions for external display interface. Transitions between modes should follow the transition flow.

Table 35 Operation modes and interfaces

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still picture)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving picture)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still picture while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note 1: Instruction registers can only be set via system interface.
2: RGB-I/F and VSYNC-I/F cannot be used at the same time.
3: RGB-I/F mode (RIM-0) cannot be set while RGB I/F is operating.
4: For mode transitions, see the section on the external display interface.
5: RGB-I/F and VSYNC-I/F modes should be used in high-speed write mode (HWM = 1).

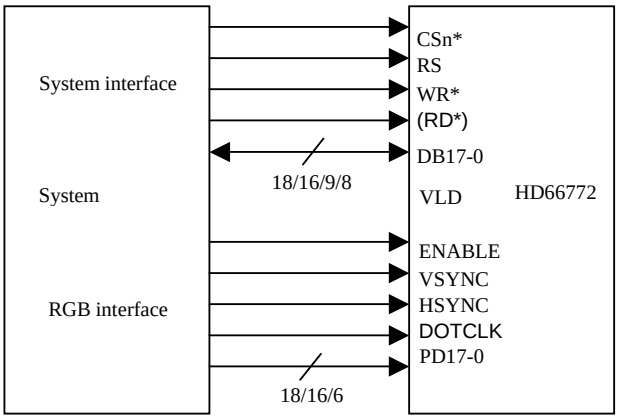


Figure 27 RGB Interface and HD66772

System Interface

The following interfaces are available as system interface. It is determined by setting bits of IM3-0. Instructions and RAM accesses can be performed via the system interface.

Table 36 IM bits

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin
GND	GND	GND	GND	Setting disabled	
GND	GND	GND	Vcc	Setting disabled	
GND	GND	Vcc	GND	80-system 16-bit interface	DB17 to 10 and 8 to 1
GND	GND	Vcc	Vcc	80-system 8-bit interface	DB17 to 10
GND	Vcc	GND	ID	Clocked serial peripheral interface (SPI)	DB1 to 0
GND	Vcc	Vcc	*	Setting disabled	
Vcc	GND	GND	GND	Setting disabled	
Vcc	GND	GND	Vcc	Setting disabled	
Vcc	GND	Vcc	GND	80-system 18-bit interface	DB17 to 0
Vcc	GND	Vcc	Vcc	80-system 9-bit interface	DB17 to 9
Vcc	Vcc	*	*	Setting disabled	

80-system 18-bit interface

80-system 18-bit parallel data transfer can be used by setting IM3/2/1/0 pins to Vcc/GND/Vcc/GND levels.

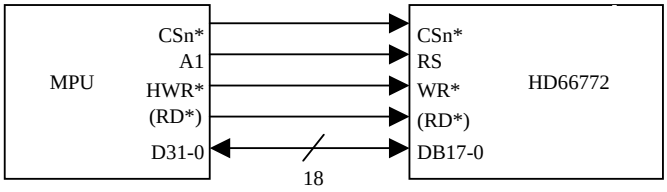
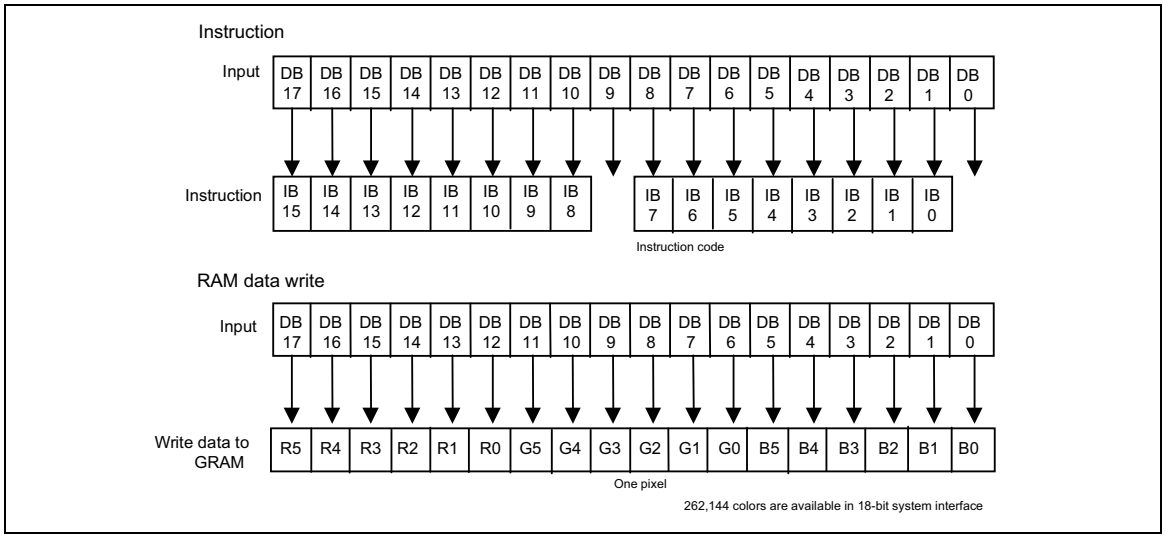


Figure 28 Example of Interface with the 18-bit Microcomputer

Data format for 18-bit interface



80-system 16-bit interface

80-system 16-bit parallel data transfer can be used by setting IM3/2/1/0 pins to GND/GND/Vcc/GND levels.

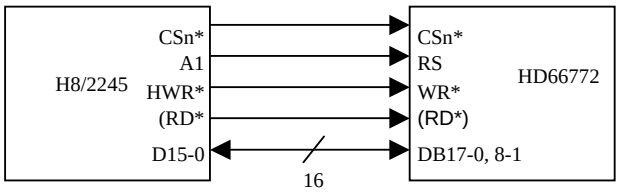
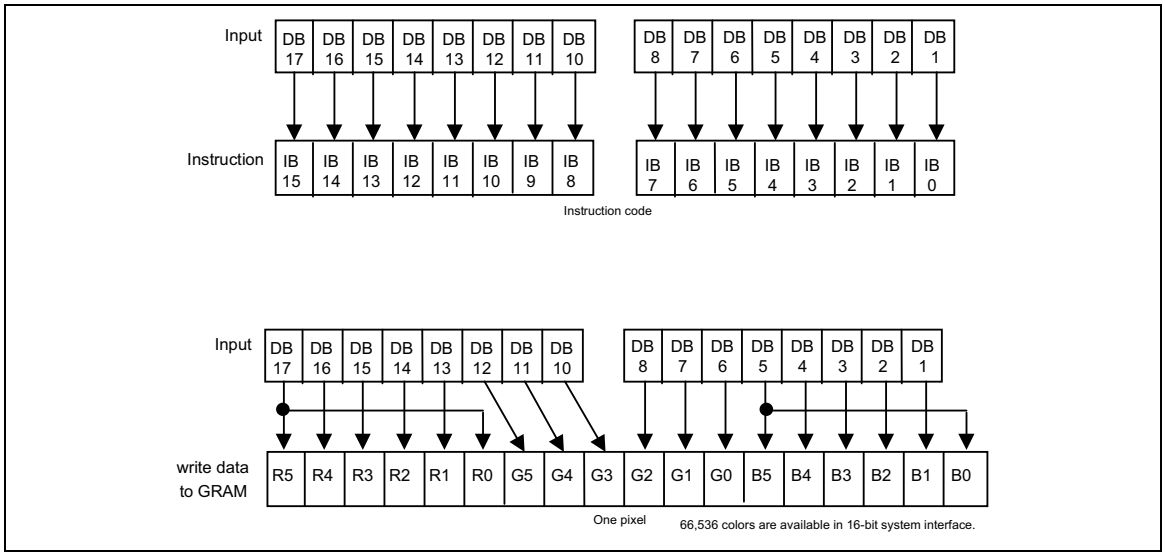


Figure 29 Example of Interface with the 16-bit Microcomputer

Data format for 16-bit interface



80-system 9-bit interface

80-system 9-bit parallel data transfer can be used by setting IM3/2/1/0 pins to Vcc/GND/Vcc/Vcc levels. 16-bit instruction is divided into two parts, which are lower and upper, and the upper eight bits are first transferred. The LSB of the bus is not used. RAM data is also divided into two parts, which are lower and upper, and the upper nine bits are first transferred. Unused pins (DB8-0) must be fixed to the Vcc or GND level. Ensure that upper bytes have to be written when writing the index register.

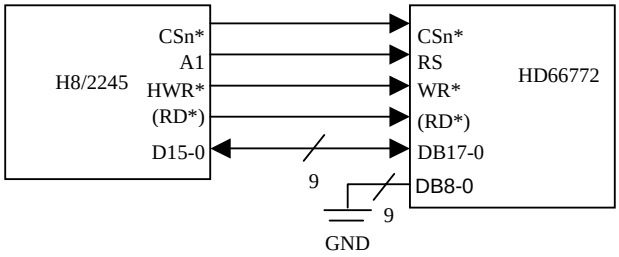
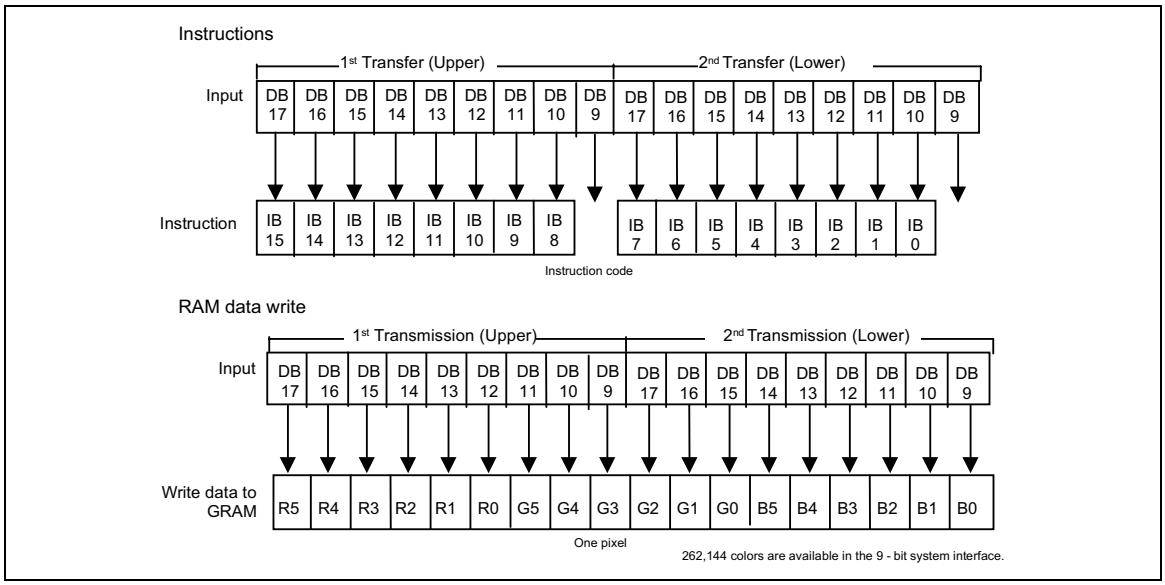


Figure 30 Example of Interface with the 9-bit Microcomputer

Data format for 9-bit interface



Note:Transfer synchronization function for an 9-bit bus interface.

The HD66772 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 9-bit data transfer in the 9-bit bus interface. Noise causing transfer mismatch between the nine upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

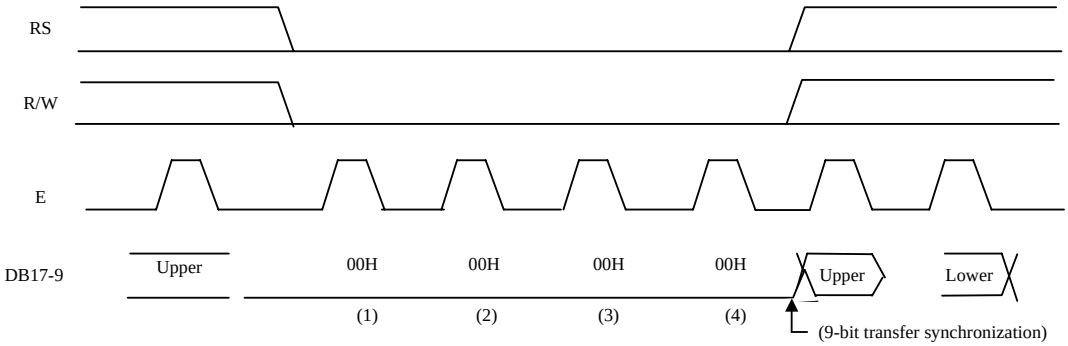


Figure 31 9-bit Transfer Synchronization

80-system 8-bit interface

80-system 8-bit parallel data transfer can be used by setting IM3/2/1/0 pins to GND/GND/Vcc/Vcc levels. 16-bit instruction is divided into two parts, which are lower and upper, and the upper eight bits are first transferred. The LSB of the bus is not used. RAM data is also divided into two parts, which are lower and upper, and the upper nine bits are first transferred. Data for RAM write is expanded to 18-bit data in this LSI. Unused pins (DB9-0) must be fixed to the Vcc or GND level. Ensure that upper bytes have to be written when writing the index register.

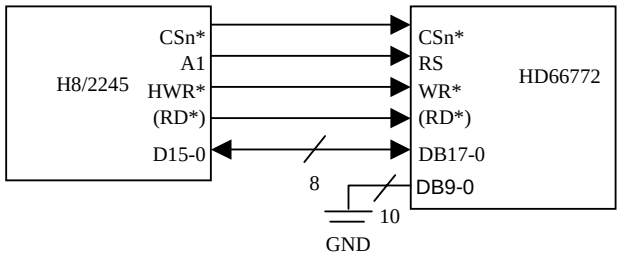
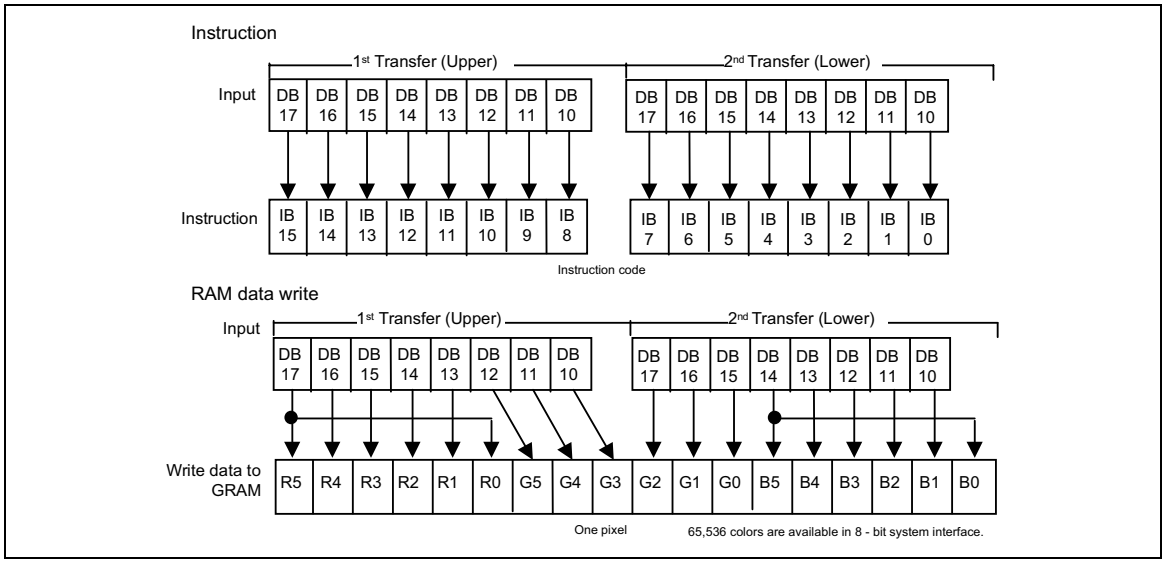


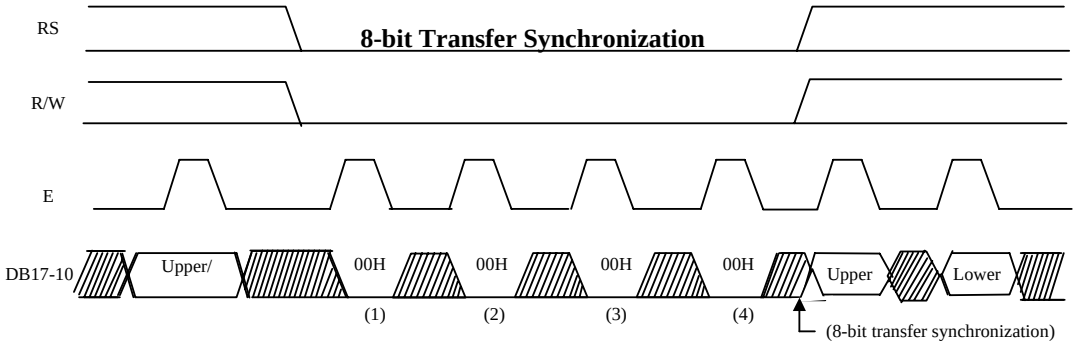
Figure 32 Example of Interface with the 8-bit Microcomputer

Data format for 8-bit interface



Note:Transfer synchronization function for an 8-bit bus interface

The HD66772 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.



Serial clock synchronized interface (SPI)

Setting the IM3 pin to the GND level, the IM2 pin to the Vcc level, the IM1 pin to the GND level allows standard clock-synchronized serial data (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins which are not used must be fixed at Vcc or GND.

The HD66772 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66772 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66772. The HD66772, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66760 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

When writing to RAM via this serial interface, the data is written to the GRAM after two-byte data has been transferred. The MSB of RB data is added to its LSB so that data to be written to the RAM will be 18 bits.

After receiving the start byte, the HD66772 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66772 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. Data for RAM write is expanded to 18-bit data in this LSI.) After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The HD66763 starts to read correct RAM data from the fifth byte.

Table 37 Start Byte Format

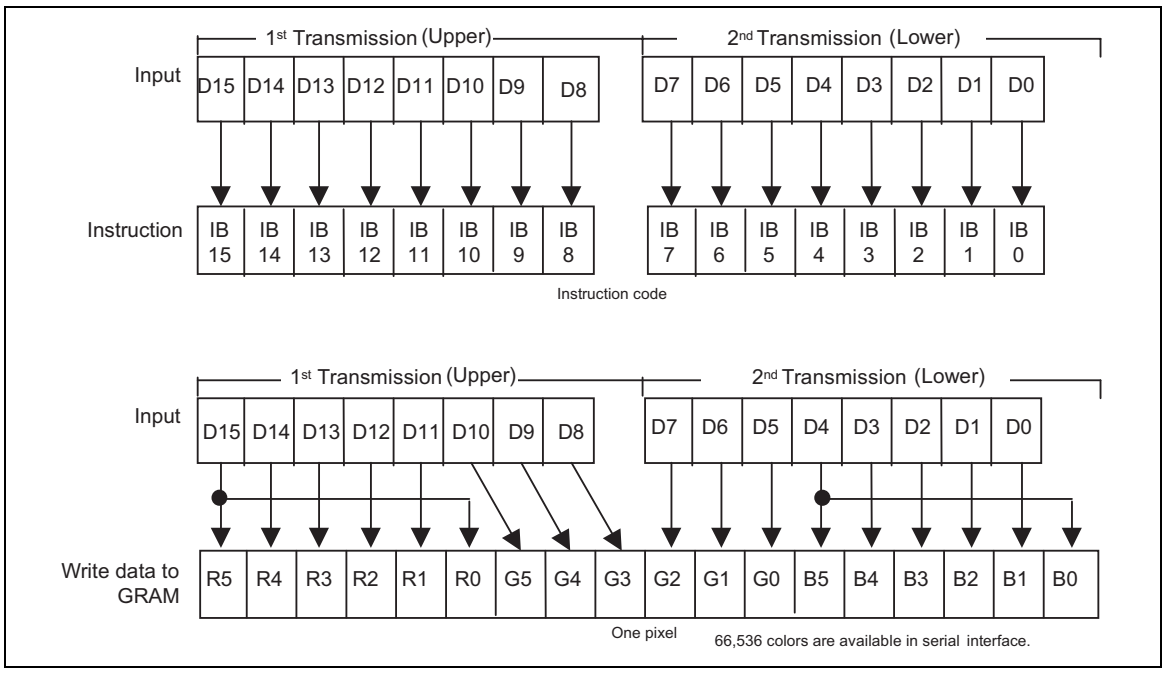
Transfer Bit	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

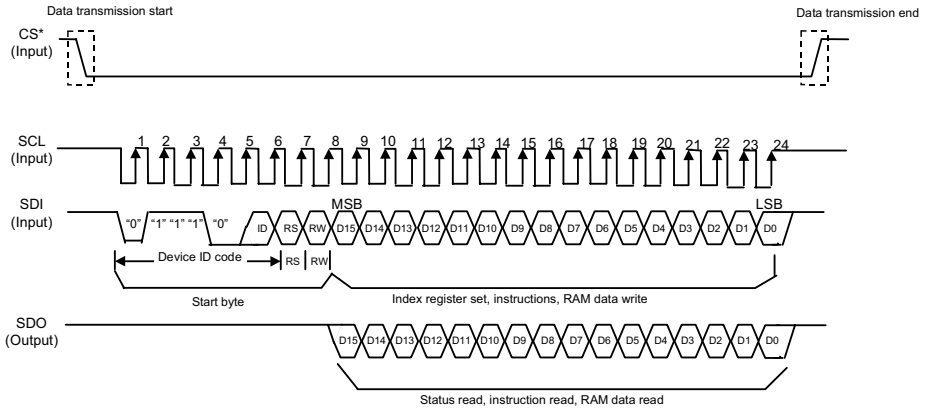
Table 38 RS and R/W Bit Function

RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

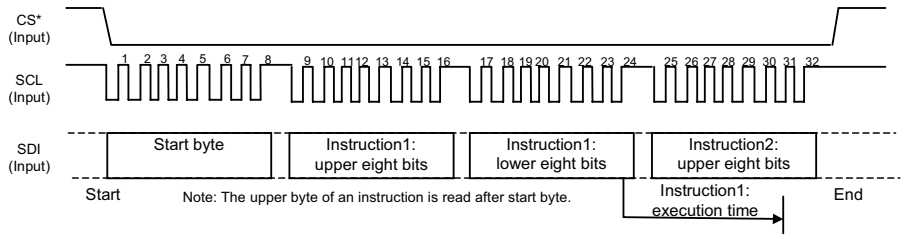
Data format for serial interface



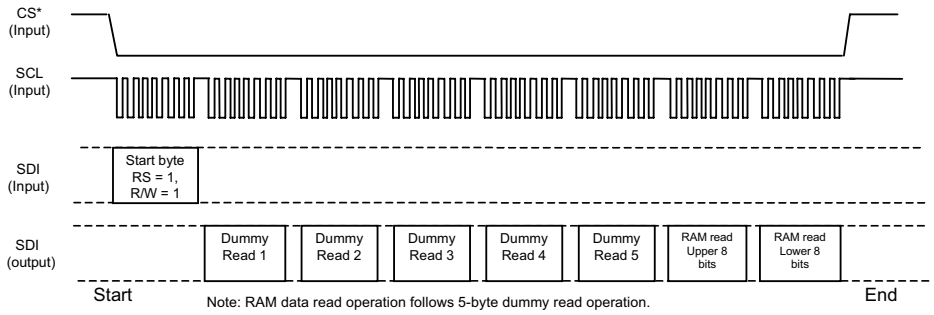
A)Basic data transmission through SPI



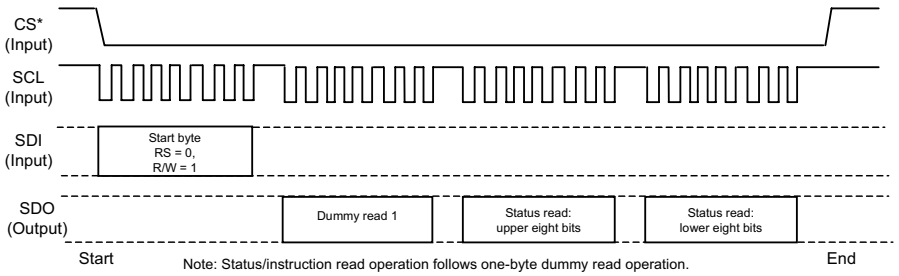
B)Consecutive data transmission through SPI



C) RAM data read transmission through SPI



D) Status read / instruction read



VSYNC Interface

The HD66772 incorporates VSYNC-I/F, which enables moving pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display moving pictures.

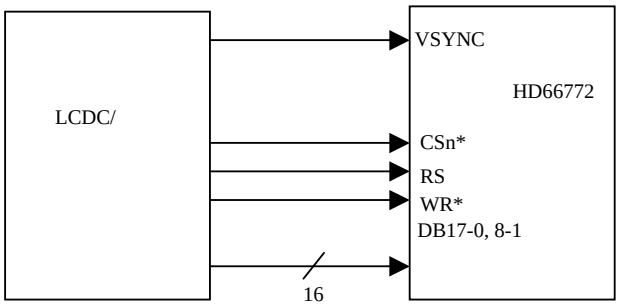


Figure 35 Example of VSYNC Interface

When DM1-0 = 10 and RM = 0, VSYNC-I/F is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of moving pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during moving picture display operation. The high-speed write mode (HWM = 1) achieves both low power consumption and high-speed access.

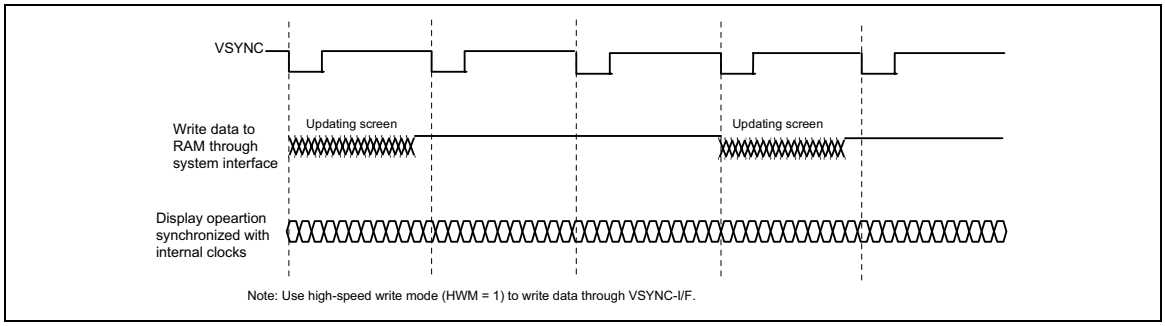


Figure 36 Moving Picture Data Transfer via VSYNC Interface

VSYNC-I/F requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below.

- Internal clock frequency (fosc) [Hz] = Frame frequency × (Display raster-row (NL) + Front porch (FP) + Back porch (BP)) × 16 Clock × Fluctuation
- Minimum speed for RAM writing [Hz] > 176 × Display raster-row (NL) / {((Back porch (BP) + Display raster-row (NL) - Margin) × 16 clock) / fosc}

Note: When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

Example

Display size 176 RGB × 240 raster-rows

Display raster-row 240 raster-rows (NL = 11110)

Back/front porch 14/2 raster-rows (BP = 1110/FP = 0010)

Frame frequency 60 Hz

Internal clock frequency (fosc) Hz = 60 Hz × (240 + 2 + 14) × 16 Clock × 1.1 / 0.9 = 300 kHz

Note 1: Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% fluctuation within the VSYNC period is assumed.

Note 2: The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.

Minimum speed for RAM writing Hz > 176 × 240 / {((14 + 240 - 2) raster-rows × 16 clock) / 300 kHz} = 3.14 MHz

Note 3: In this case RAM writing starts immediately after the falling edge of VSYNC.

Note 4: The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

Therefore, when RAM writing starting immediately after the falling edge of VSYNC is performed at 3.14 MHz or more, the data for display can be rewritten before display operation starts. This means that flicker-free display operation is achieved.

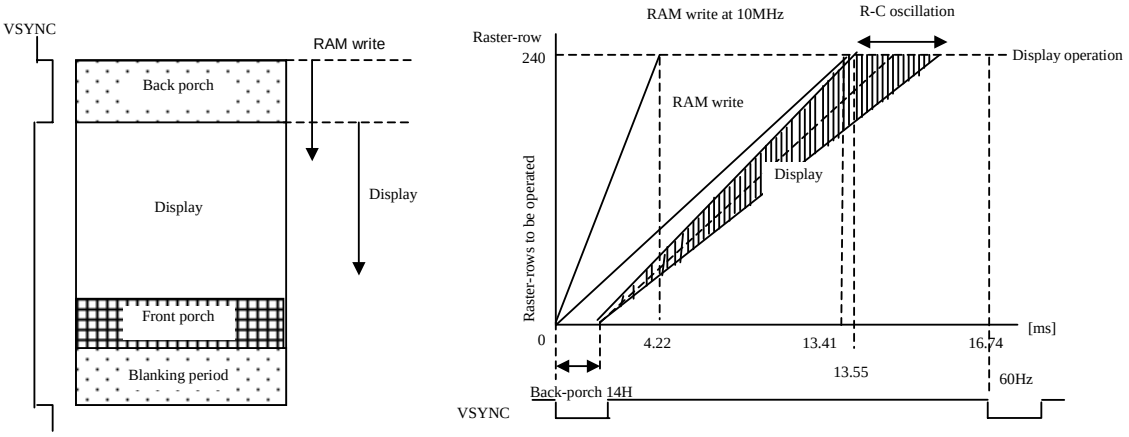


Figure 37 Operation for VSYNC Interface

Usage on VSYNC Interface

1. The Example above is a calculated value. Please keep in mind that a margin for these factors is also needed. Because production variation of the internal oscillator requires consideration.

2. The example above is a calculated value of rewriting the whole screen. A limitation of the moving picture area generates a margin for the RAM write speed.

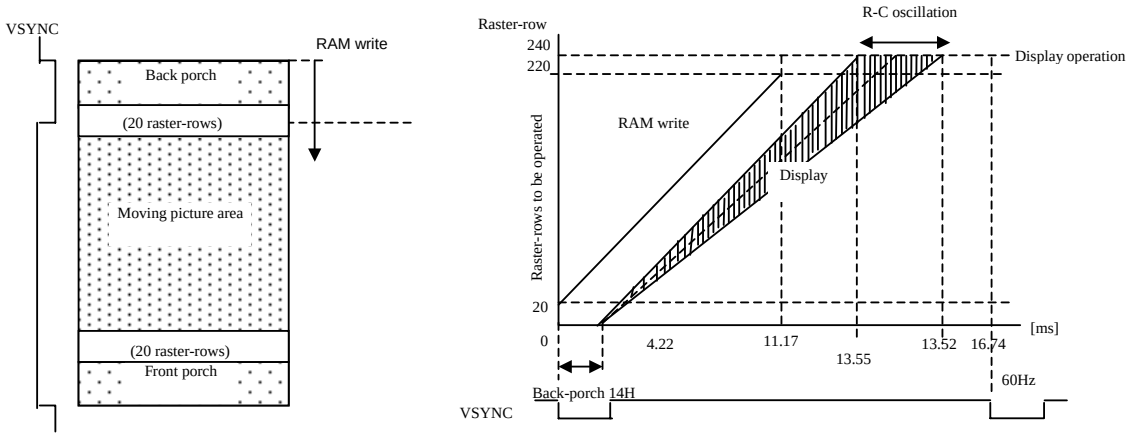


Figure 38 Limitation of Moving Picture Area

3. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

4. Transition between the internal clock operation mode (DM1-0 = 00) and VSYNC interface mode will be valid after the completion of the screen which is displayed when the instruction is set.

5. Partial display, vertical scroll, and interlaced driving functions are not available on VSYNC interface mode.

6. The VSYNC interface is performed by the method above, therefore, AM bit should be 0.

7. Data for display should be written in high-speed write mode (HWM = 1) when the VSYNC interface is in use.

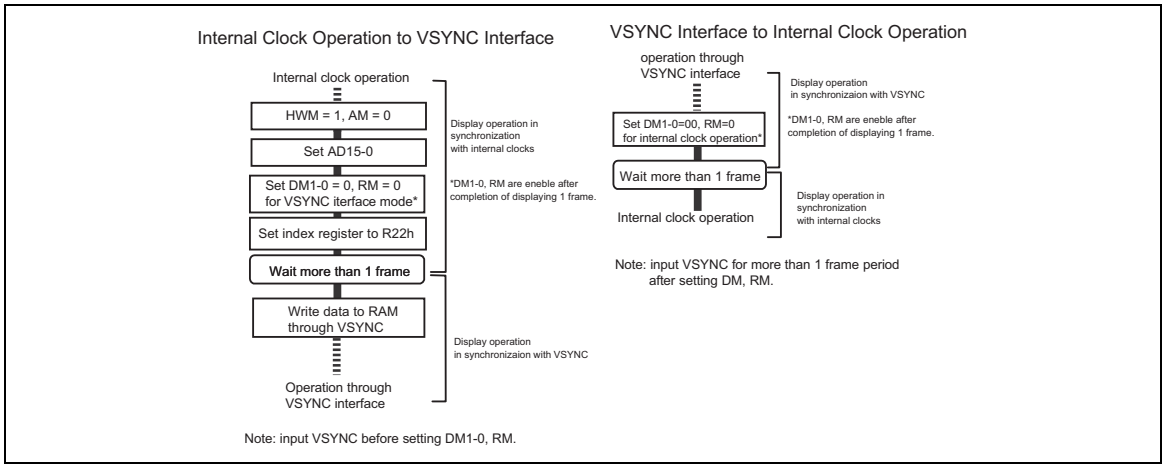


Figure 39 Transition between the Internal Operating Clock Mode and VSYNC Interface Mode

External Display Interface

The following interfaces are available as external display interface. It is determined by setting bits of RIM1-0. RAM accesses can be performed via the RGB interface.

Table 39 RIM bits

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17-0
0	1	16-bit RGB interface	PD17-13, 11-1
1	0	6-bit RGB interface	PD17-12
1	1	Setting disabled	

Note: Multiple interfaces cannot be used.

RGB interface

The RGB-I/F is performed in synchronization with VSYNC, HSYNC, and DOTCLK. Combining the function of the high-speed write mode and the window address enables transfer only the screen to be updated and reduce the power consumption.

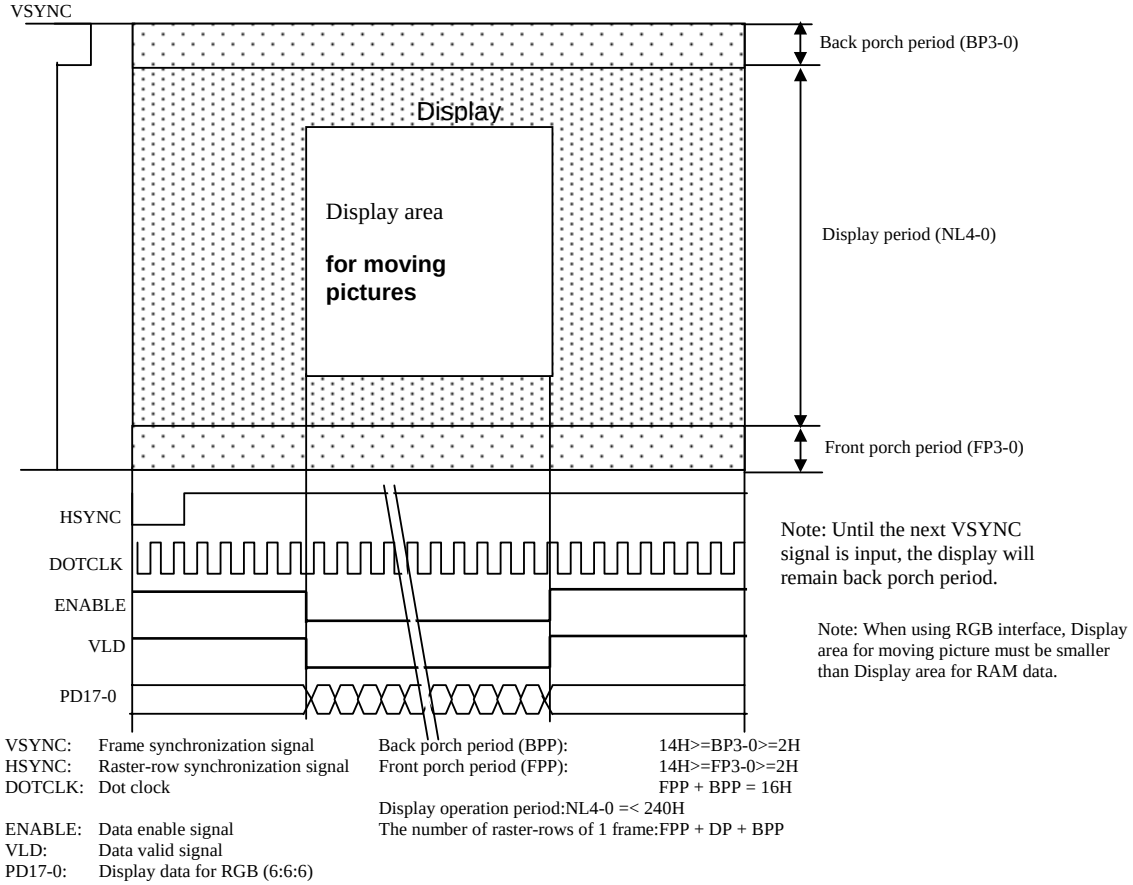


Figure 40 RGB Interface

VLD and ENABLE signals

The relationship between VLD and ENABLE signals is shown below.

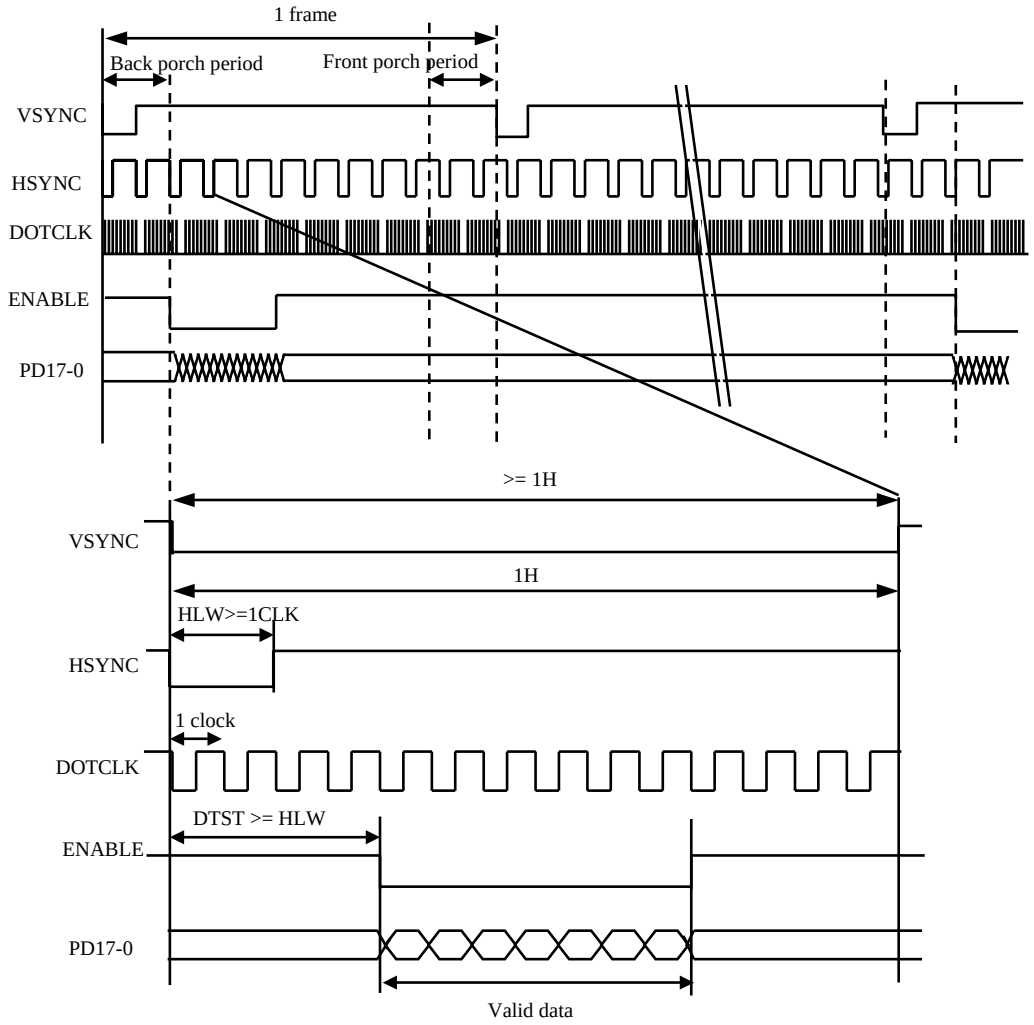
Table 40 Relationship between VLD and ENABLE

EPL	ENABLE	VLD	RAM Write	RAM Address
0	0	0	Valid	Updated
0	0	1	Invalid	Updated
0	1	*	Invalid	Hold
1	0	*	Invalid	Hold
1	1	0	Valid	Updated
1	1	1	Invalid	Updated

RGB interface timing

16-/18-bit RGB interface timing

Timing chart for RGB-I/F is shown below.



VLW: The period in which VSYNC is low level

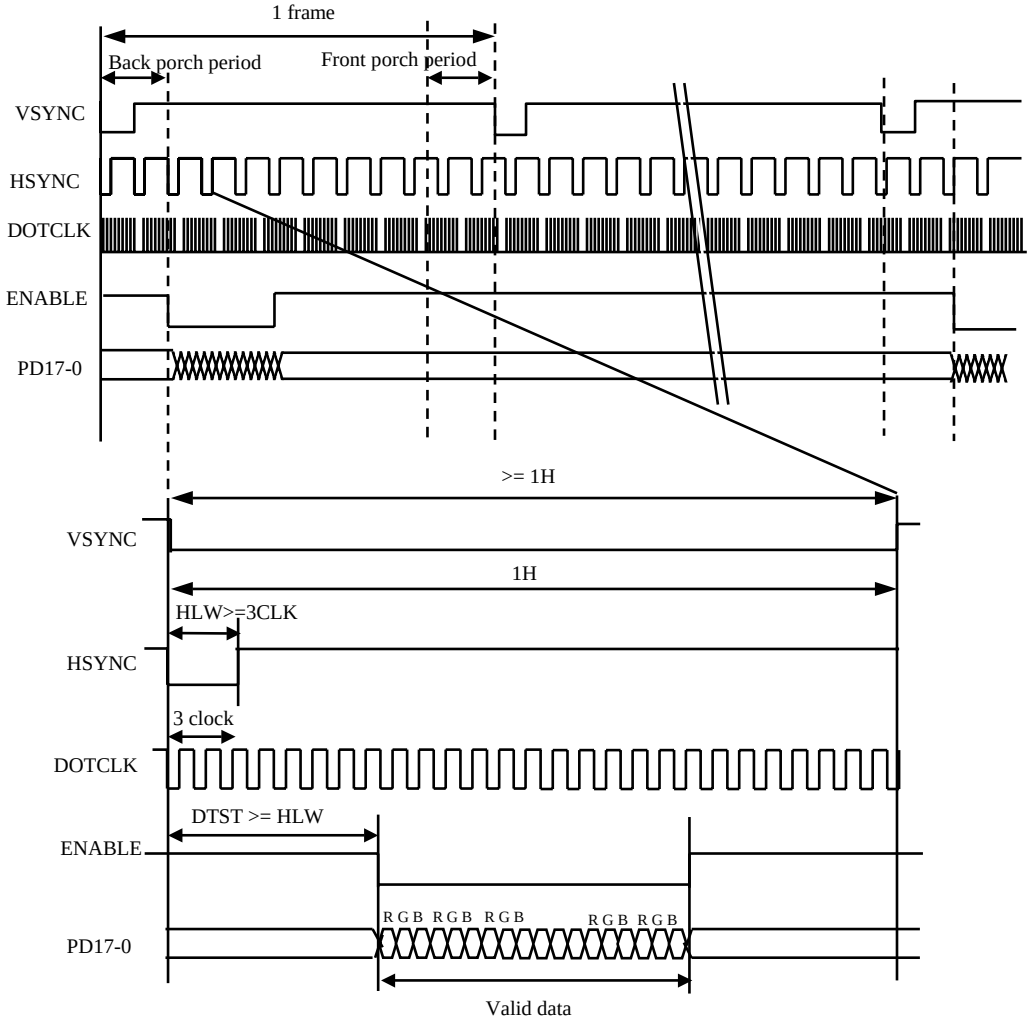
HLW: The period in which HSYNC is low level

Note: Data for display should be written in the high-speed write mode (HWM = 1) in VSYNC-I/F is in use.

Figure 41 16-/18-bit RGB Interface Timing

6-bit RGB interface timing

Timing chart for RGB-I/F is shown below.



VLW: The period in which VSYNC is low level

HLW: The period in which HSYNC is low level

Note1: Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.

2: VSYNC, HSYNC, EVABLE, DOTCLK, VLD, and PD17-2 should be transferred in units of three clocks.

Figure 42 6-bit RGB Interface Timing

Moving picture display

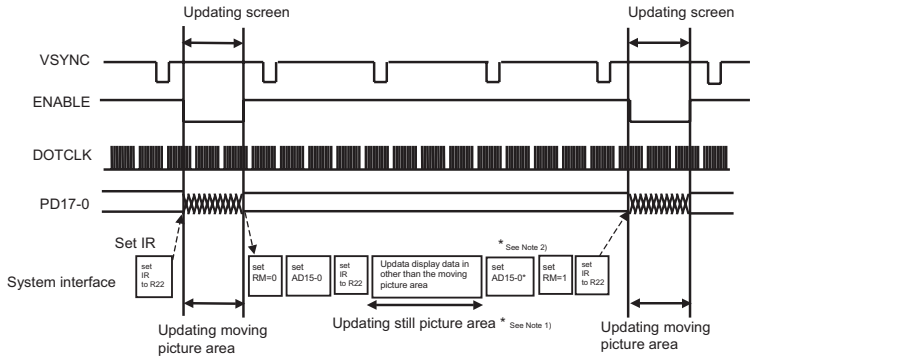
The HD66772 incorporates RGB interface to display moving pictures and RAM to store data for display. For displaying moving pictures, the HD66772 has the following features.

- Moving picture area can only be transferred by the window address function
- The high-speed write mode achieves both low power consumption and high-speed access
- Moving picture area to be rewritten can only be transferred.
- Reducing the amount of data transferred enables reduce the power consumption to the whole system.
- Still picture area, such as an icon, can be updated while displaying moving pictures combining with the system interface.

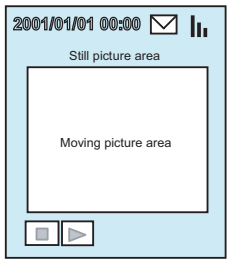
RAM access via the system interface when RGB-I/F is in use

RAM can be accessed via the system interface when RGB-I/F is in use. When data is written to RAM during RGB-I/F mode, the ENABLE bit should be high to stop data writing via RGB-I/F, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is low. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB-I/F. When a RAM write conflict occurs, data writing is not guaranteed.

Example of display moving picture via RGB-I/F and updating still picture via the system interface are shown below.



Note1) The address AD15-0 is set at AC on every falling edge of VSYNC in RGB interface.
Note2) Set the address AD15-0 at AC and the index register to R22h (RAM data write/read) before RAM access through RGB interface.
Note 3) Use high-speed write mode when writing data through an RGB interface.



6-bit RGB interface

6-bit RGB interface can be used by setting RIM1-0 pins to 10. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17-12), the data valid signal (VLD), and the data enable signal(ENABLE). Unused pins (DB11 to 0) must be fixed to the Vcc or GND level.

Note: Instructions should be set via the system interface.

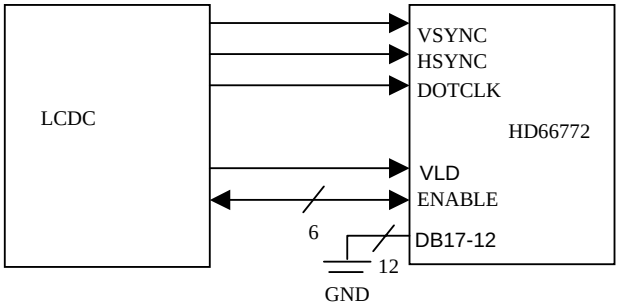
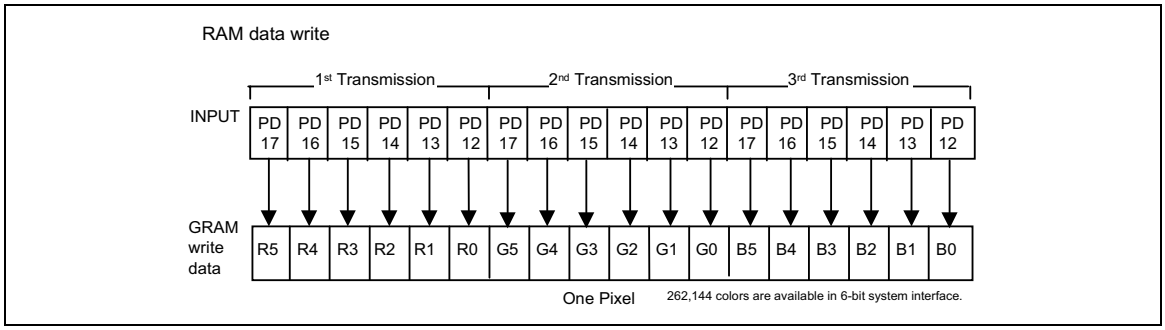


Figure 44 Example of 6-Bit RGB Interface

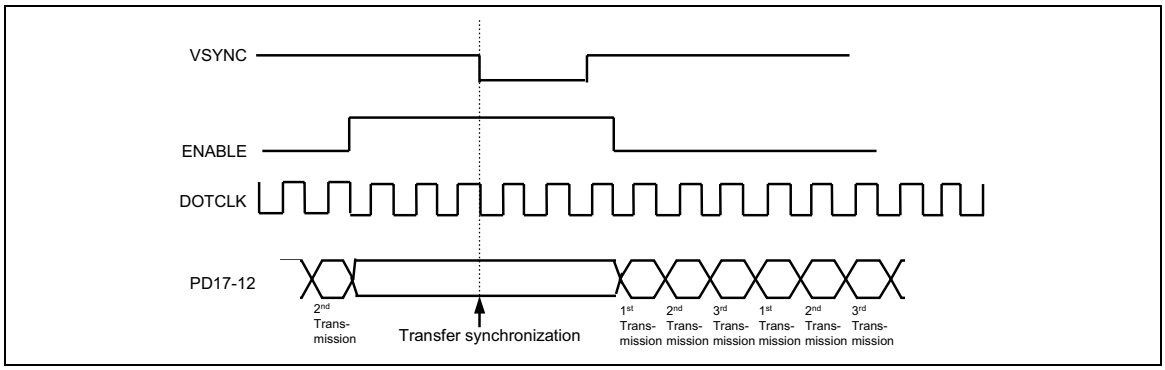
Data format for 6-bit interface



Note: Transfer synchronization function for a 6-bit bus interface

The HD66772 has the transfer counter to count 1st, 2nd and 3rd data transfer in the 6-bit bus interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected by a reset triggered on the falling edge of VSYNC, which means the beginning of a frame. The next transfer restarts correctly. In this method, when data is consecutively transferred such as displaying moving pictures, the effect of transfer mismatch will be reduced and recover normal operation.

Note: The internal display is operated in units of three DOTCLK. When the DOTCLK is not input in units of pixels, clock mismatch occurs and the frame which is operated and the next frame are not displayed correctly.



16-bit RGB interface

16-bit RGB interface can be used by setting RIM1-0 pins to 01. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM in synchronization with display operation via 6-bit RGB data bus (PD17-13 and 11-1), the data valid signal (VLD) and data enable signal (ENABLE).

Note: Instructions should be set via the system interface.

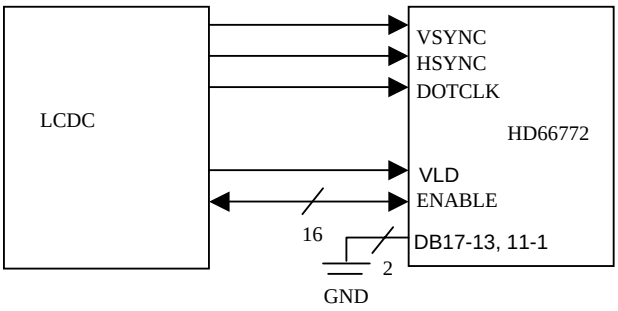
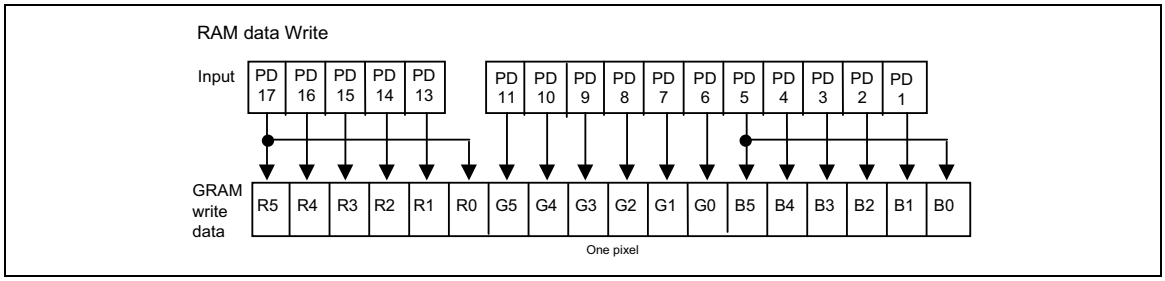


Figure 46 Example of 16-Bit RGB Interface

Data format for 16-bit interface



18-bit RGB interface

18-bit RGB interface can be used by setting MIF1-0 pins to 01. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM in synchronization with display operation via 6-bit RGB data bus (PD17-13 and 11-1), the data valid signal (VLD) and data enable signal (ENABLE).

Note: Instructions should be set via the system interface.

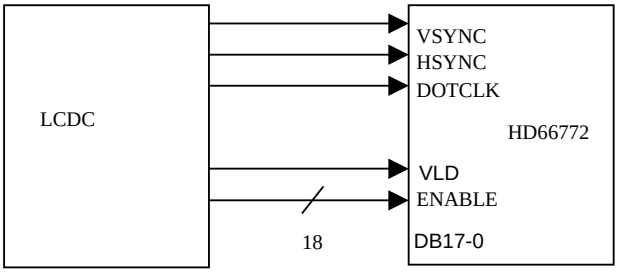
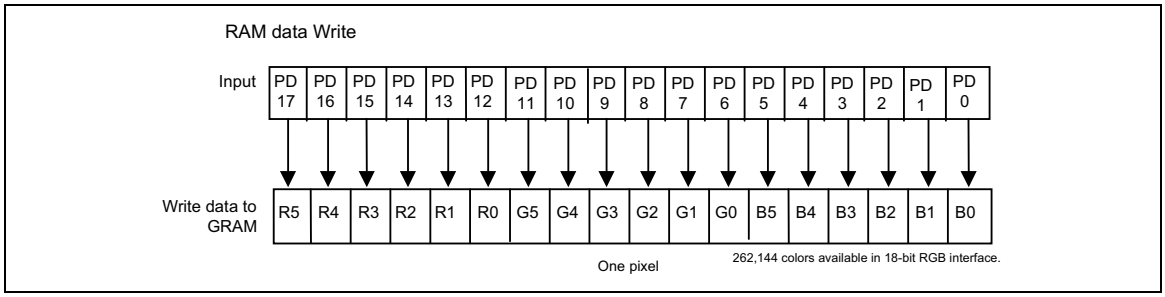


Figure 47 Example of 18-Bit RGB Interface

Data format for 18-bit interface



Usage on external display interface

a) When external display interface is in use, the following functions are not available.

Table 41 Relationship between VLD and ENABLE

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced driving	Not available	Available
Graphics operation function	Not available	Available

b) VSYNC, HSYNC, and DOTCLK signals should be supplied during display operation via RGB-I/F.

c) Please make sure that when setting bits of NO1-0, SDT1-0, and EQ1-0 in RGB-I/F, the clock on which operations are based changes from the internal operating clock to DCLK.

d) RGB data is transferred for three clock cycles in 6-bit RGB-I/F. Data transferred, therefore, should be transferred in units of RGB.

e) Interface signals, VSYNC, HSYNC, DOTCL, ENABLE, VLD, and PD17-0 should be set in units of RGB (pixels) to match RGB transfer.

f) Transitions between internal operation mode and external display interface should follow the mode transition sequence shown below.

g) During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

h) RGB-I/F should be used in high-speed write mode (HWM = 1).

i) An address set is done on the falling edge of VSYNC every frame in RGB-I/F.

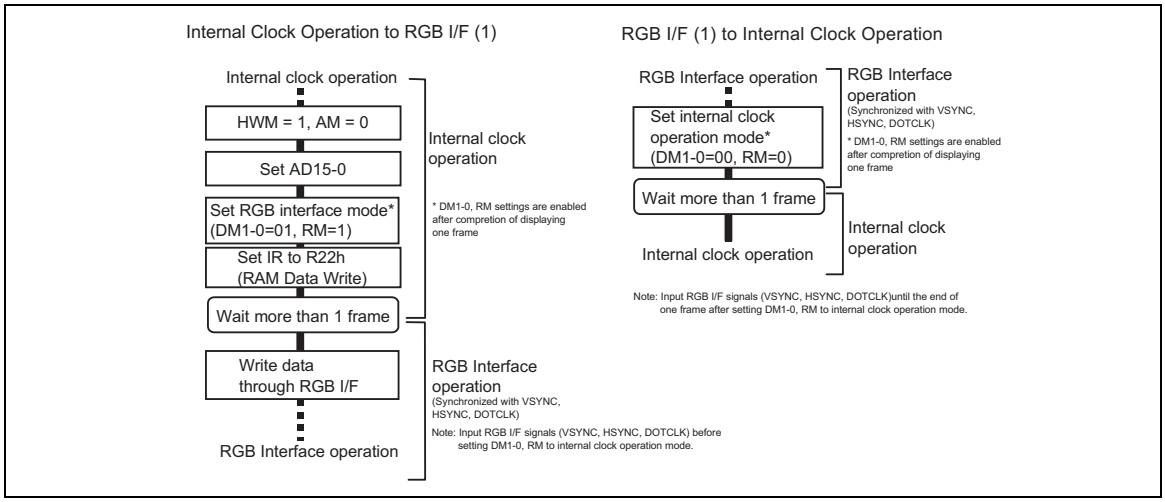
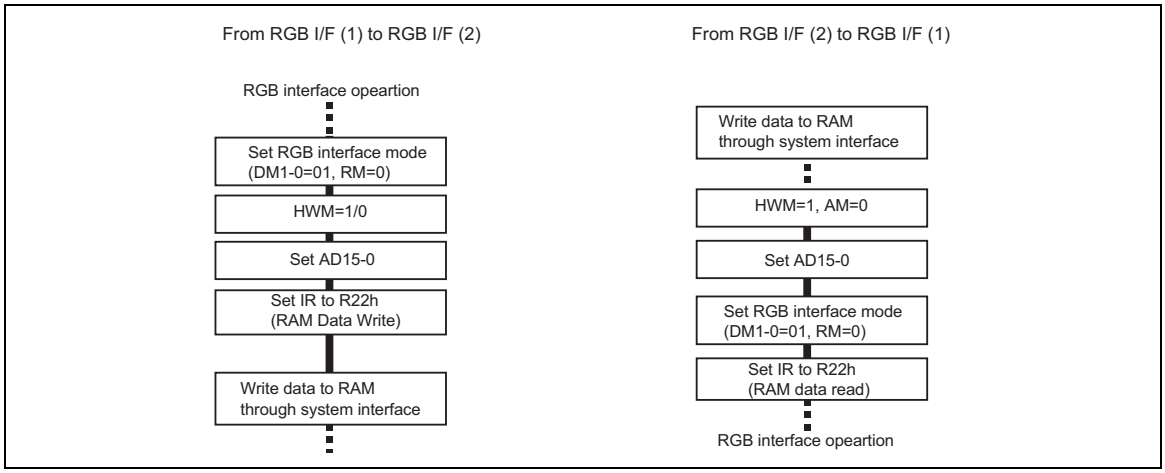


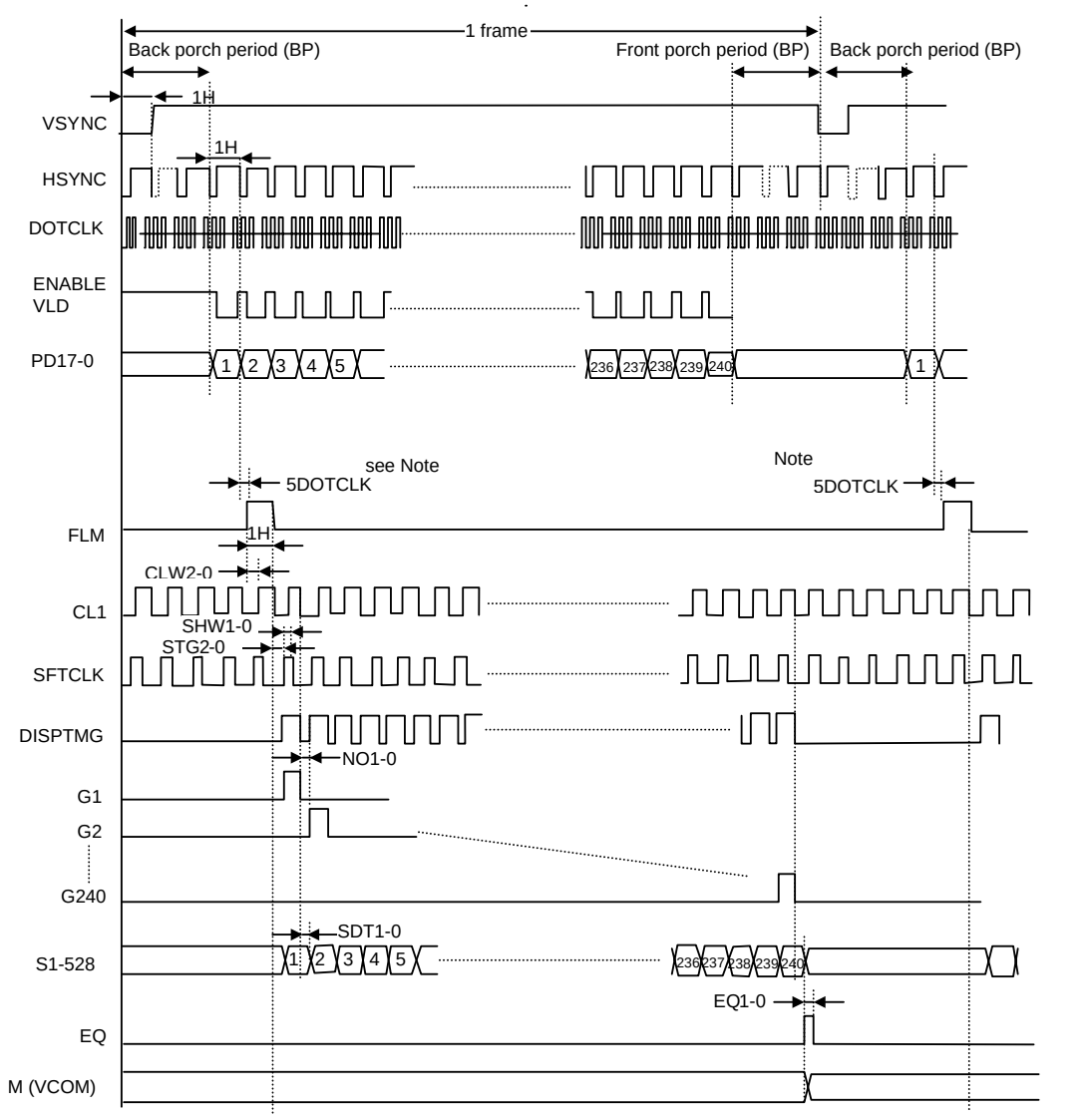
Figure 48 Transition between the Internal Operating Clock Mode and RGB Interface Mode



Timing of LCD Panel I/F

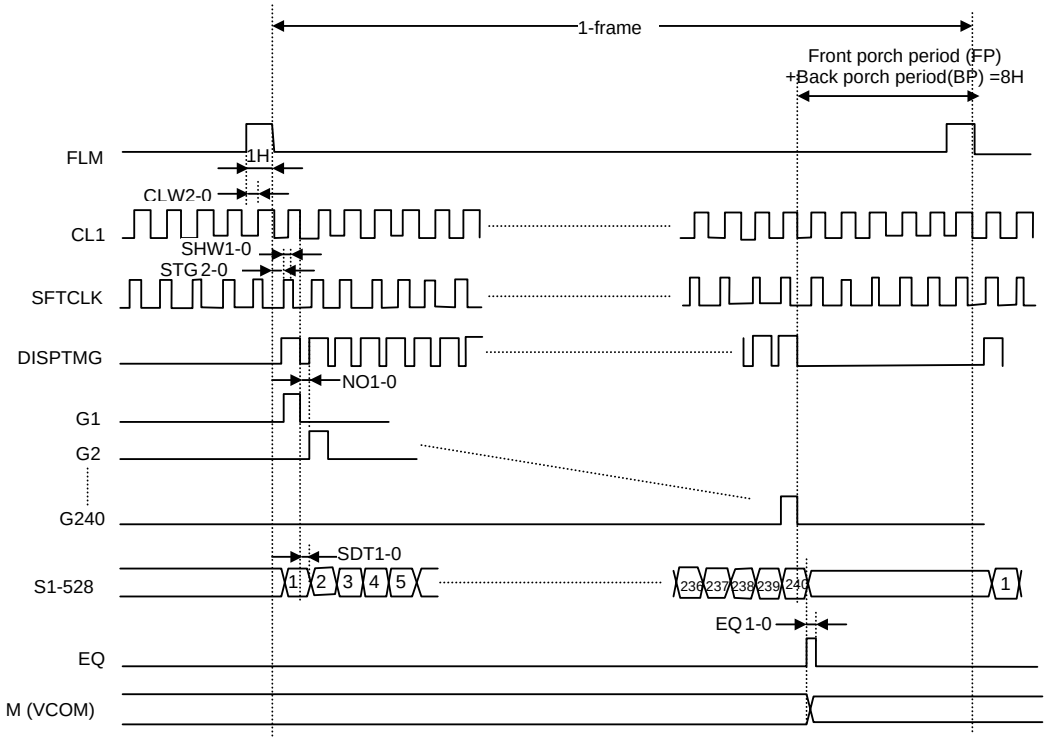
Relationship between RGB I/F signal and LCD panel signal while internal clock and RGB I/F is operating.

(1) Timing of LCD panel I/F while RGB I/F is operating



Note: When using 6-bit RGB I/F, the first rising edge of FLM delay is DOTCLK from a falling edge of HSYNC.

(2) Timing of LCD panel I/F while internal clock is operating



(3) Resistor Setting

Table 42 CL1 signal "Low" width setting

CLW2	CLW1	CLW0	CL1 signal low period	
			Internal clock operation (1clock = internal oscillation clock)	RGB I/F operation (1 clock = DOUTCLK)
0	0	0	1 clock	8 clock
0	0	1	2 clock	16 clock
0	1	0	3 clock	24 clock
0	1	1	4 clock	32 clock
1	0	0	5 clock	40 clock
1	0	1	6 clock	48 clock
1	1	0	7 clock	56 clock
1	1	1	8 clock	64 clock

Setting value above "above are clock of CL1 signal from a falling edge

Table 43EQ signal "High" width setting

EQ1	EQ0	Equalize period	
		Internal clock operation (1clock = internal oscillation clock)	RGB I/F operation (1 clock = DOUTCLK)
0	0	Non equalization	Non equalization
0	1	1 clock	8 clock
1	0	2 clock	16 clock
1	1	3 clock	24 clock

Table 44 Delay amount of source output

SDT 1	STD 0	Delay amount of source output	
		Internal clock operation (1clock = internal oscillation clock)	RGB I/F operation (1 clock = DOUTCLK)
0	0	1 clock	8 clock
0	0	2 clock	16 clock
0	1	3 clock	24 clock
0	1	4 clock	32 clock

Delay amount of source is defined from a falling edge of CL1.

Table 45 Amount of non-over lap for gate output

No 1	No 0	Amount of non-over lap	
		Internal clock operation (1clock = internal oscillation clock)	RGB I/F operation (1 clock = DOUTCLK)
0	0	0 clock	0 clock
0	1	4 clock	32 clock
1	0	6 clock	48 clock
1	1	8 clock	64 clock

Delay amount of source is defined from a falling edge of CL1.

Table 46 SFTCLK signal position of pulse output

STG2	STG1	STG0	SFTCLK signal position of pulse output	
			Internal clock operation (1clock = internal oscillation clock)	RGB I/F operation (1 clock = DOUTCLK)
0	0	0	0 clock	1 clock
0	0	1	1 clock	8 clock
0	1	0	2 clock	16 clock
0	1	1	3 clock	24 clock
1	0	0	4 clock	32 clock
1	0	1	5 clock	40 clock
1	1	0	6 clock	48 clock
1	1	1	7 clock	56 clock

Note: Setting value above “above are clock of CL1 signal from a falling edge.

Table 47 SFTCLK signal “High” period

SHW1	SHW 0	SFTCLK signal High period	
		Internal clock operation (1clock = internal oscillation clock)	RGB I/F operation (1 clock = DOUTCLK)
0	0	1 clock	8 clock
0	1	2 clock	16 clock
1	0	3 clock	24 clock
1	1	4 clock	32 clock

Low-temperature poly-silicon TFT panel control

The HD66772 outputs timing signals (FLM, CL1 and SFTCLK) for controlling a low-temperature poly-silicon TFT (LTPS-TFT) panel with built-in gates. The output level of the HD66772's signals, FLM, CL1 and SFTCLK, is shifted to the LTPS-TFT level so that the HD66772 directly connects the LTPS-TFT.

The HD667P00 incorporates ports with level shifter for LTPS-TFT.

Source driver (HD66772)

Table 48 Output signals

Output control timing signal	FLM (Output for the frame-start pulse)	
	CL1 (Output for the one-raster-row-cycle pulse)	The low pulse width is variable by bits of CLW2-0..
	SFTCLK (Output for the one-raster-row-cycle pulse	The output timing is variable by bits of STG2-0 and SHW1-0.

Power supply IC (HD667P00)

Table 49 Power supply

Level shifter	Built-in level shifter for converting amplitude Input (Vcc - GND) → Output (VGH to -VGH)
Port for LTPS	Input (CL1/SFTCLK) → Output (TESTFAI1)
	Input (FLM) → Output (TESTFAIIN)

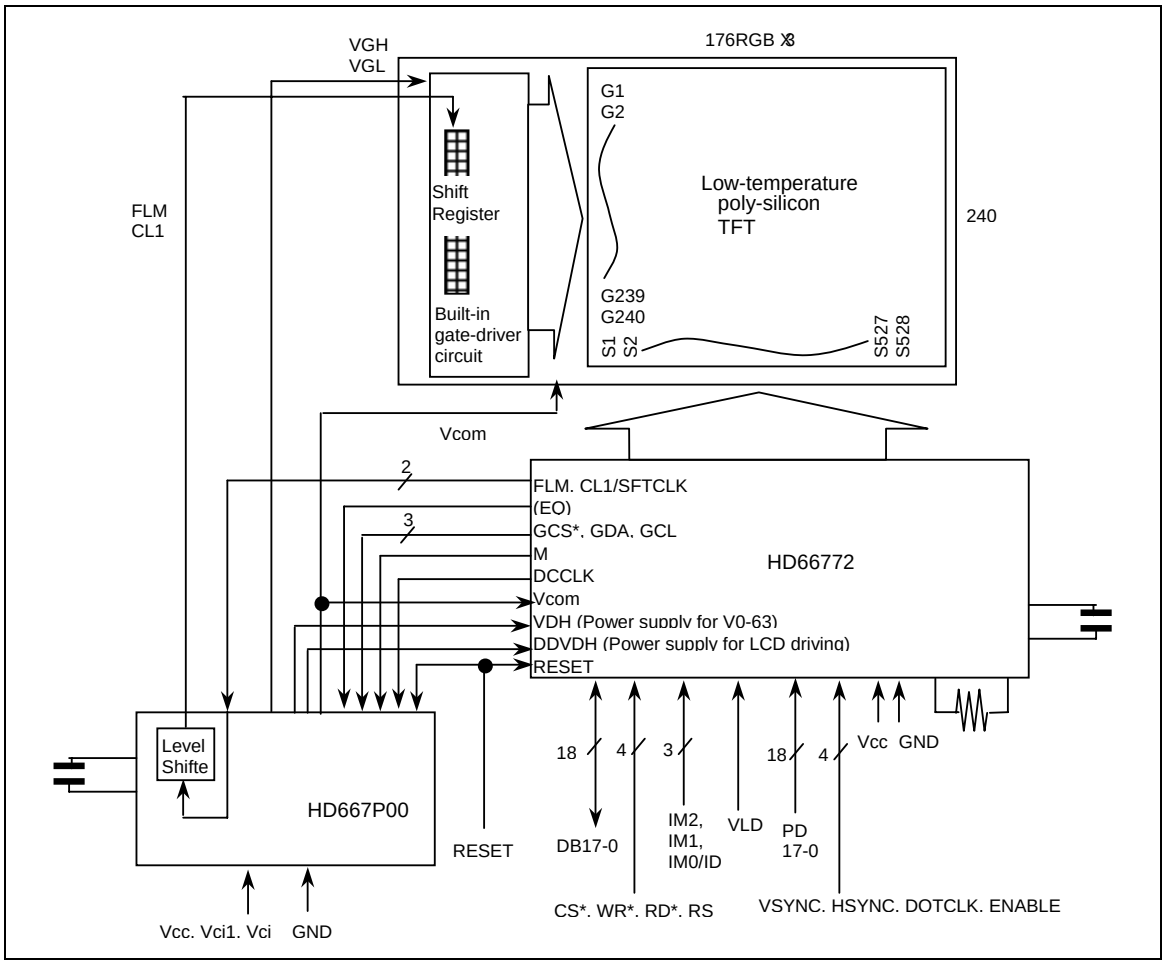


Figure 49 System Configuration

Output timing for HD66772 signals

The HD66772 outputs timing signals (FLM, CL1 and SFTCLK) for controlling a low-temperature poly-silicon TFT (LTPS-TFT) panel with built-in gates. Output timing of CL1 can be changed by LTPS-TFT control instruction.

Output timing should be specified to match the gate circuit configuration in the LTPS-TFT.

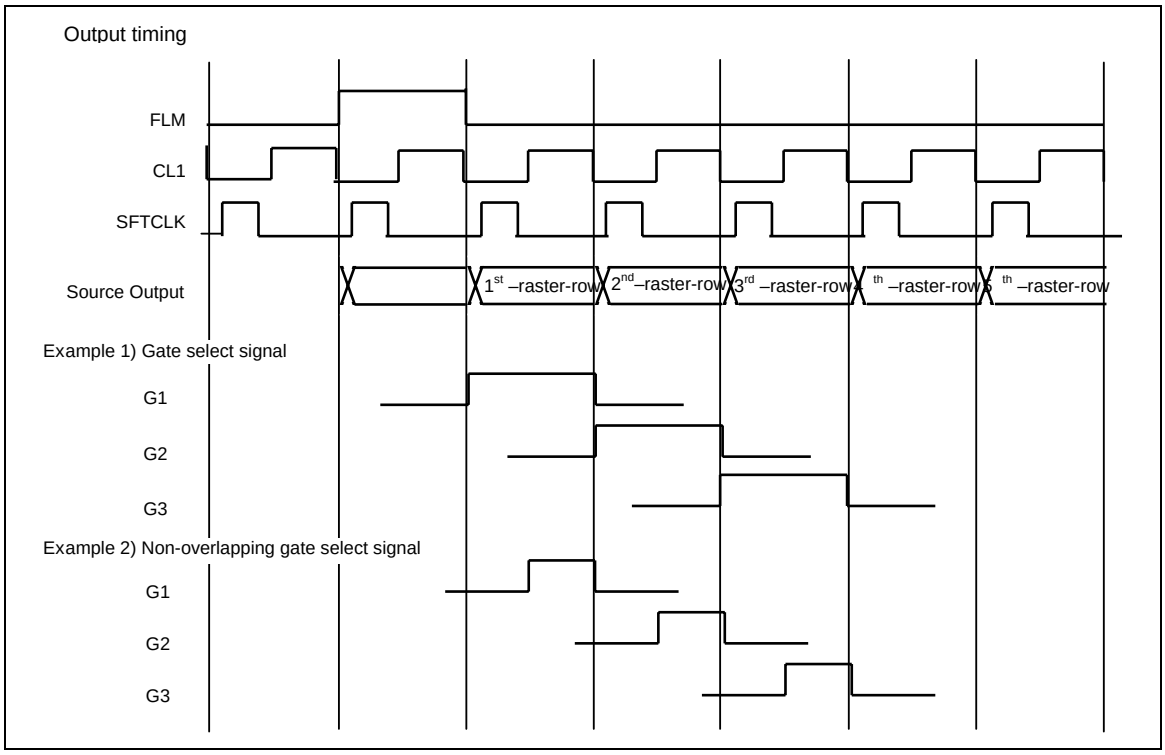


Figure 50 Output Timing

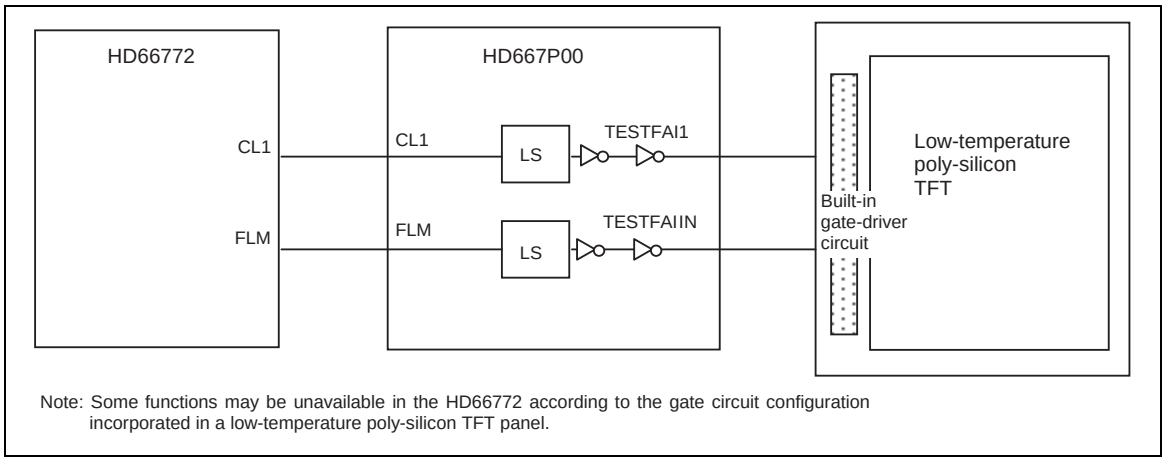


Figure 51 Example of LTPS-TFT Control Signals

High-Speed Burst RAM Write Function

The HD66772 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications which require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66772 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

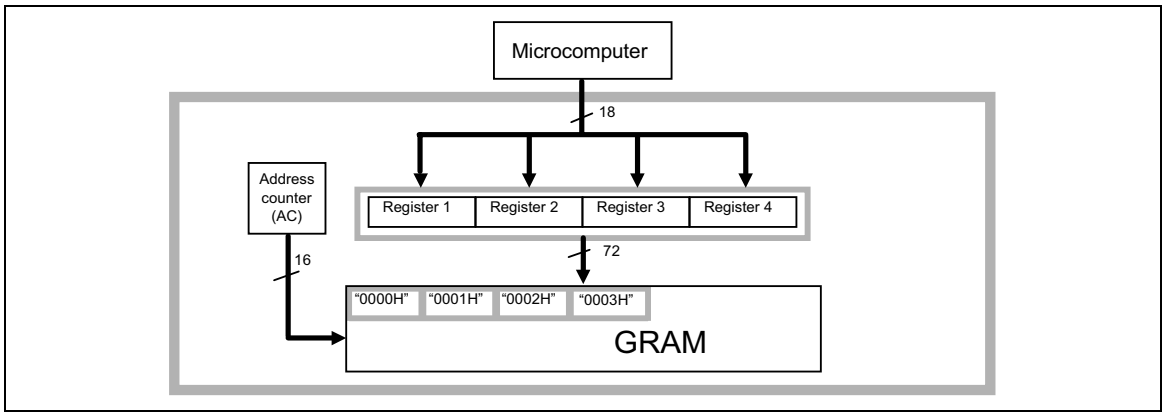


Figure 52 Flow of Operation in High-Speed Consecutive Writing to RAM

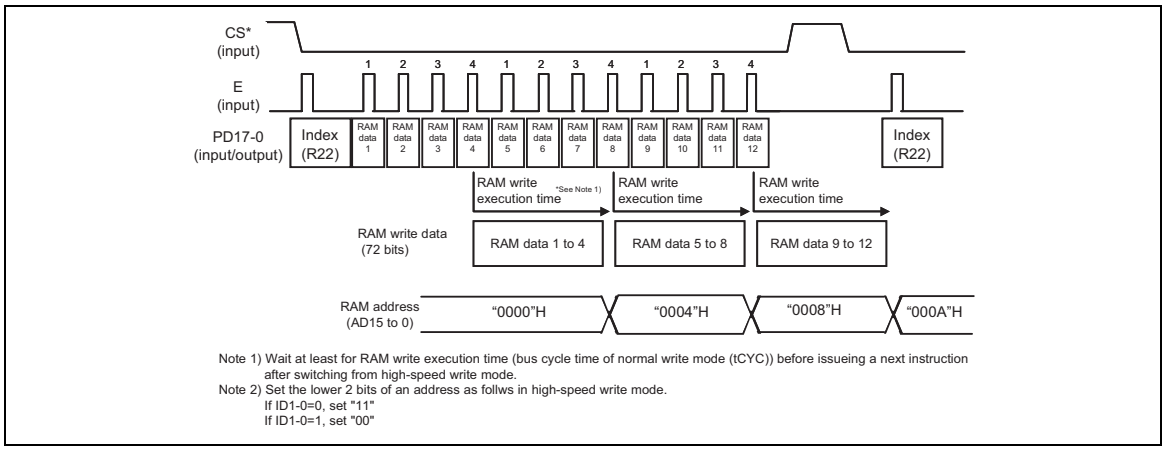
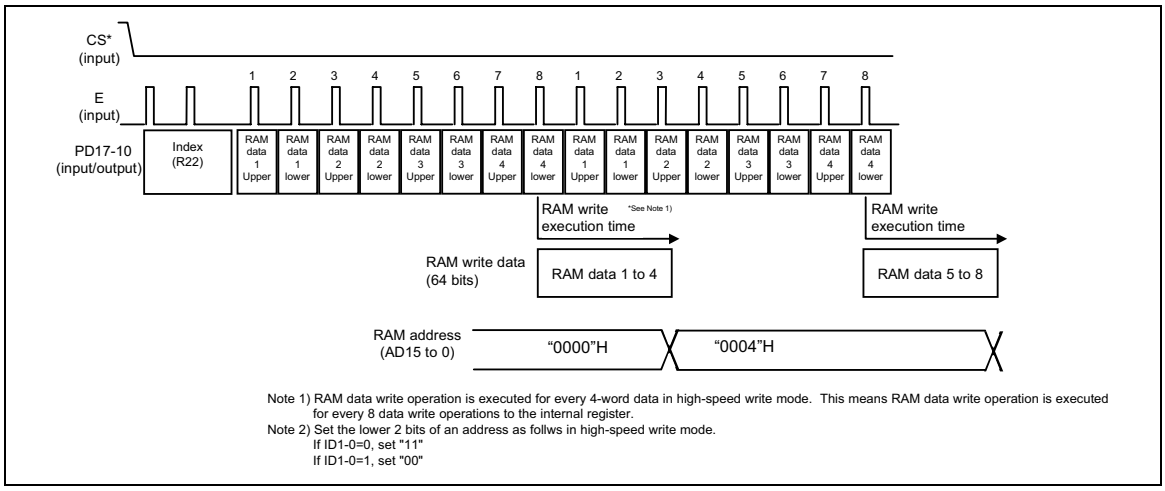


Figure 53 Example of the Operation of High-Speed Consecutive Writing to RAM



Note 1) RAM data write operation is executed for every 4-word data in high-speed write mode. This means RAM data write operation is executed for every 8 data write operations to the internal register.
Note 2) Set the lower 2 bits of an address as follws in high-speed write mode.
If ID1-0=0, set "11"
If ID1-0=1, set "00"

Figure 54 Example of the Operation of High-Speed Consecutive Writing to RAM (8-Bit Interface)

When high-speed RAM write mode is used, note the following.

Notes: 1. The logical and compare operations cannot be used.
2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.
*When ID0=0, the lower two bits in the address must be set to 11 and be written to RAM.
*When ID0=1, the lower two bits in the address must be set to 00 and be written to RAM.
3. Data is written to RAM each four words. If less than four words of data are written to RAM, the last data will not be written to RAM.
4. When the index register and RAM data write (22H) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.
5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 50 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	**High-Speed RAM Write (HWM=1)**
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
BGR function	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	the horizontal range(HSA/HSE): more than four words the number of horizontal writing : 4N (N>=2)
External display interface	Can be used	Can be used
AM Setting	AM = 1/0	AM = 0

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Number of dummy write operations of a row must be 4N.

Table 51 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

Table 52 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of 4 × N operations, including the dummy writes.

Horizontal access count =

first dummy write count + write data count + last dummy write count = 4 × N

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).

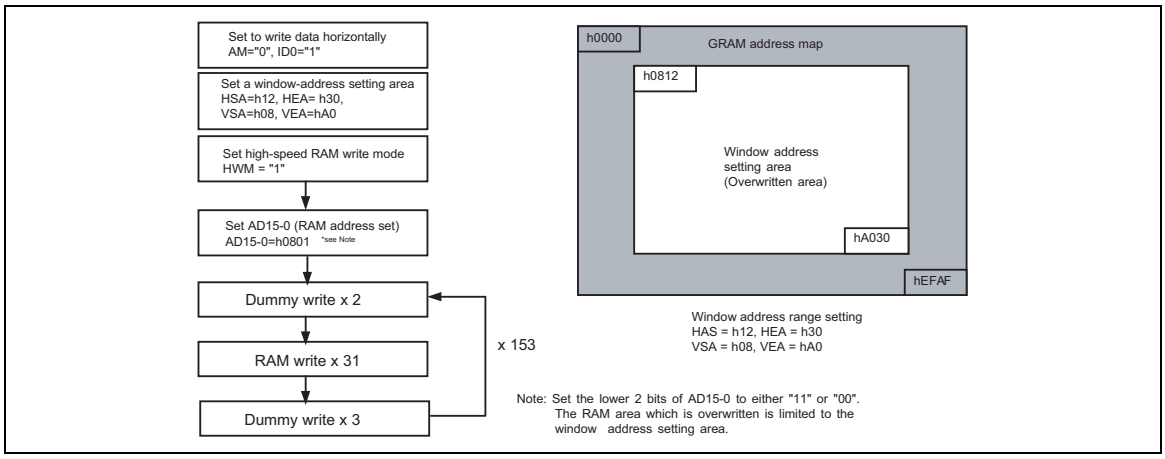


Figure 55 Example of the High-Speed RAM Write with a Window Address-Range Specification

Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7 to 0, end: HEA 7 to 0) or the vertical address register (start: VSA7 to 0, end: VEA7 to 0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]

(horizontal direction) 00H ≤ HSA7 to 0 ≤ HSA7 to 0 ≤ AFH

(vertical direction) 00H ≤ VSA7 to 0 ≤ VEA7 to 0 ≤ EFH

[Restriction on address settings during the window address]

(RAM address) HSA7 to 0 ≤ AD7 to 0 ≤ HEA7 to 0

VSA7 to 0 ≤ AD15 to 8 ≤ VEA7 to 0

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.

ID0=0: The lower two bits of the address must be set to 11.

ID0=1: The lower two bits of the address must be set to 00.

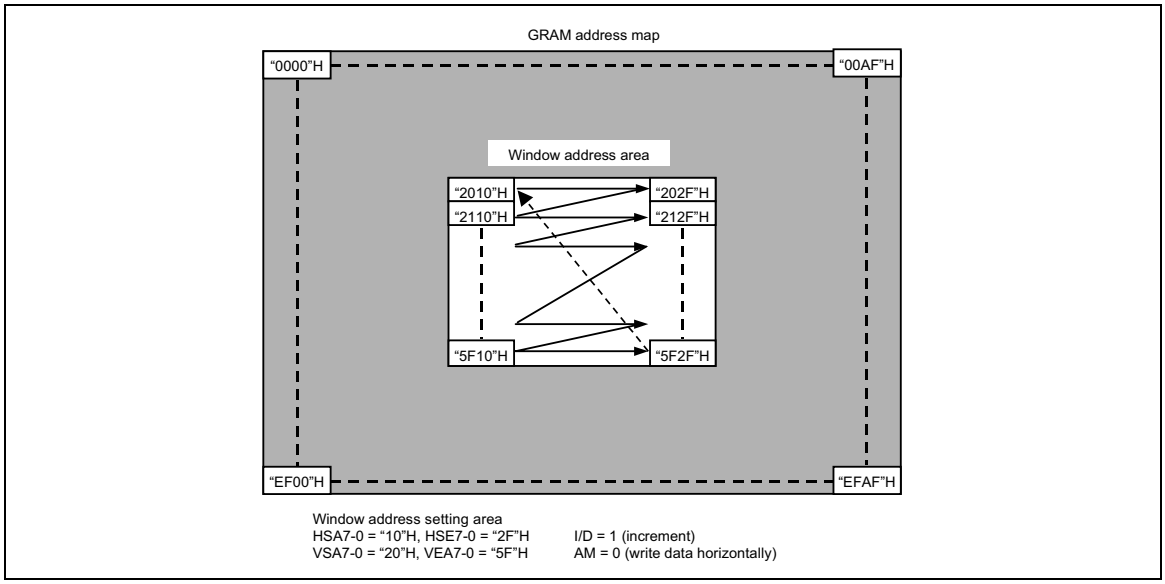


Figure 56 Example of Address Operation in the Window Address Specification

Graphics Operation Function

The HD66772 can greatly reduce the load of the microcomputer graphics software processing through the 18-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 18-bit write data.
2. A conditional write function that compares the write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the write from the microcomputer.

Table 53 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement
Write mode 2	0/1	1	000	Vertical data replacement
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement
Write mode 4	0/1	1	110 111	Conditional vertical data replacement

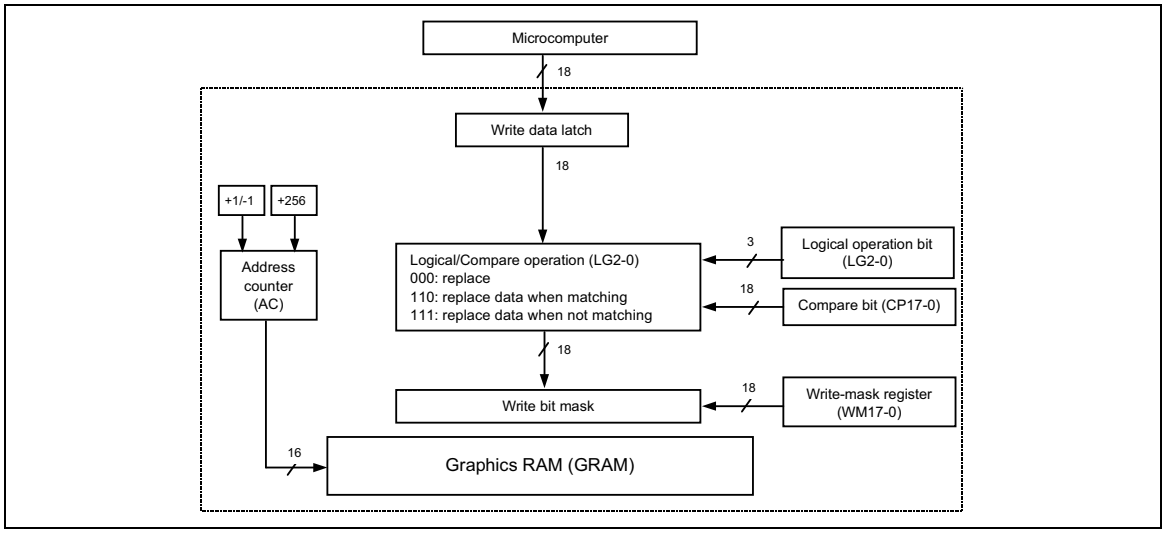


Figure 57 Data Processing Flow of the Graphics Operation

Write-data Mask Function

The HD66772 expands 16-bit data sent from the microcomputer to 18-bit data (when 18-bit interface is in use, data is not expanded). A bit-wise write-data mask function controls writing the 18-bit data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM17–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

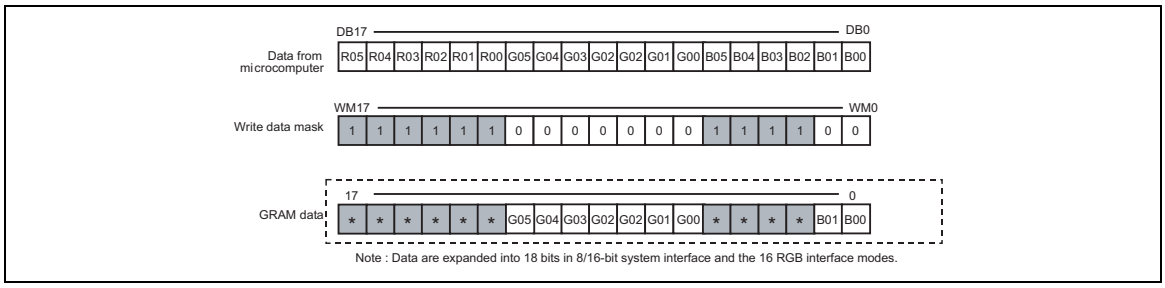


Figure 58 Example of Write-data Mask Function Operation

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2–0 = 000

This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM17–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

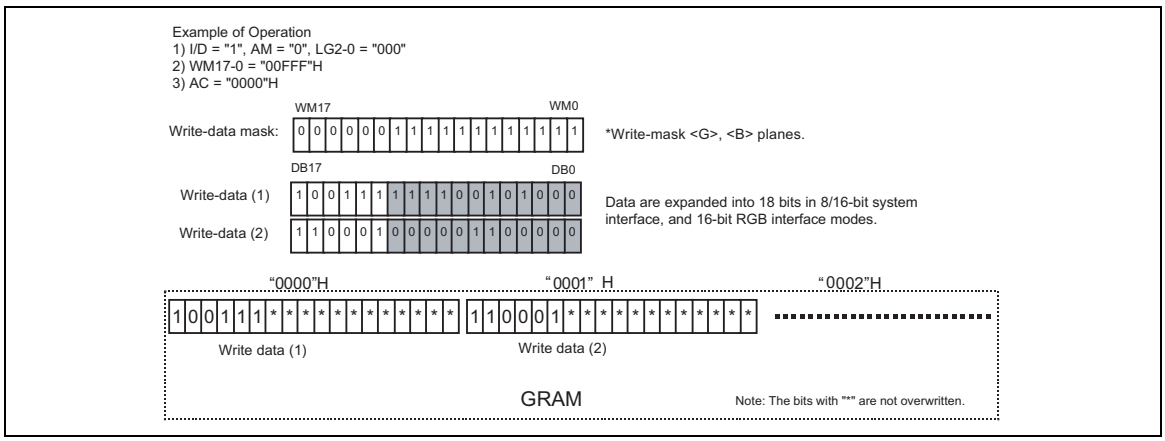


Figure 59 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM17–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

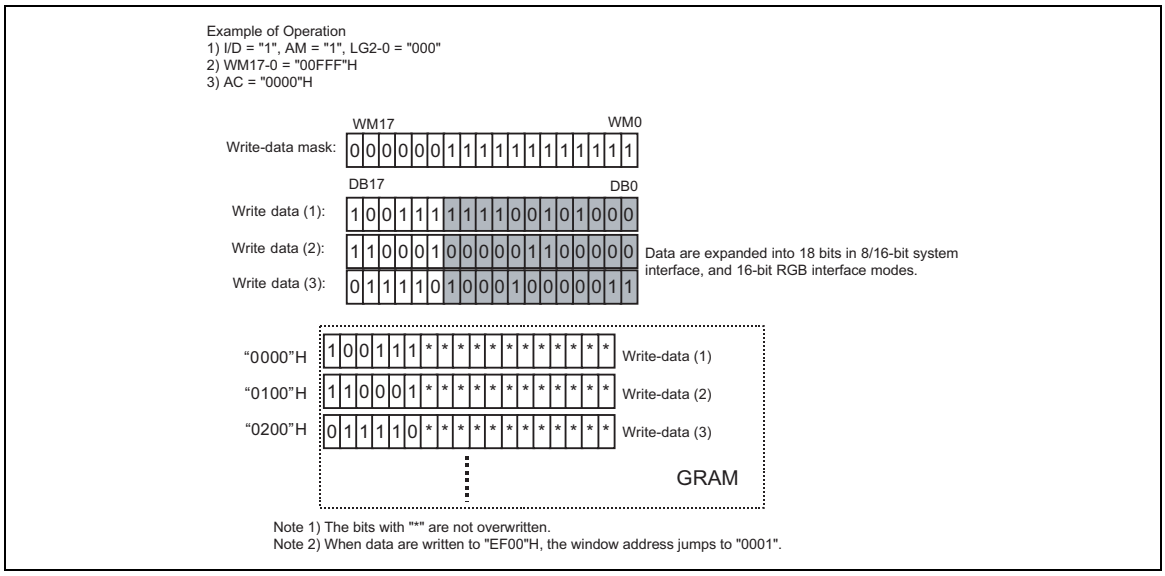


Figure 60 Writing Operation of Write Mode 2

Write mode 3: AM = 0, LG2–0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP17–0). When the result of the comparison in units of pixels satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM17–0) are also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

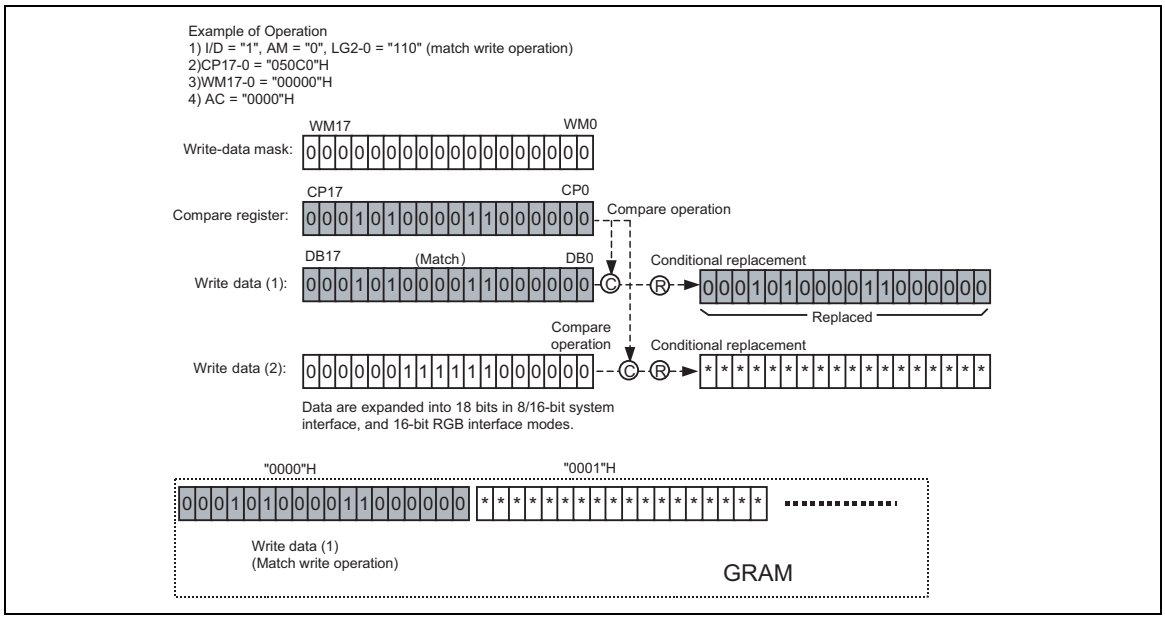


Figure 61 Writing Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

   This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP17–0) to write the data. When the result by the comparison in units of pixels satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, write-data mask function (WM17–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

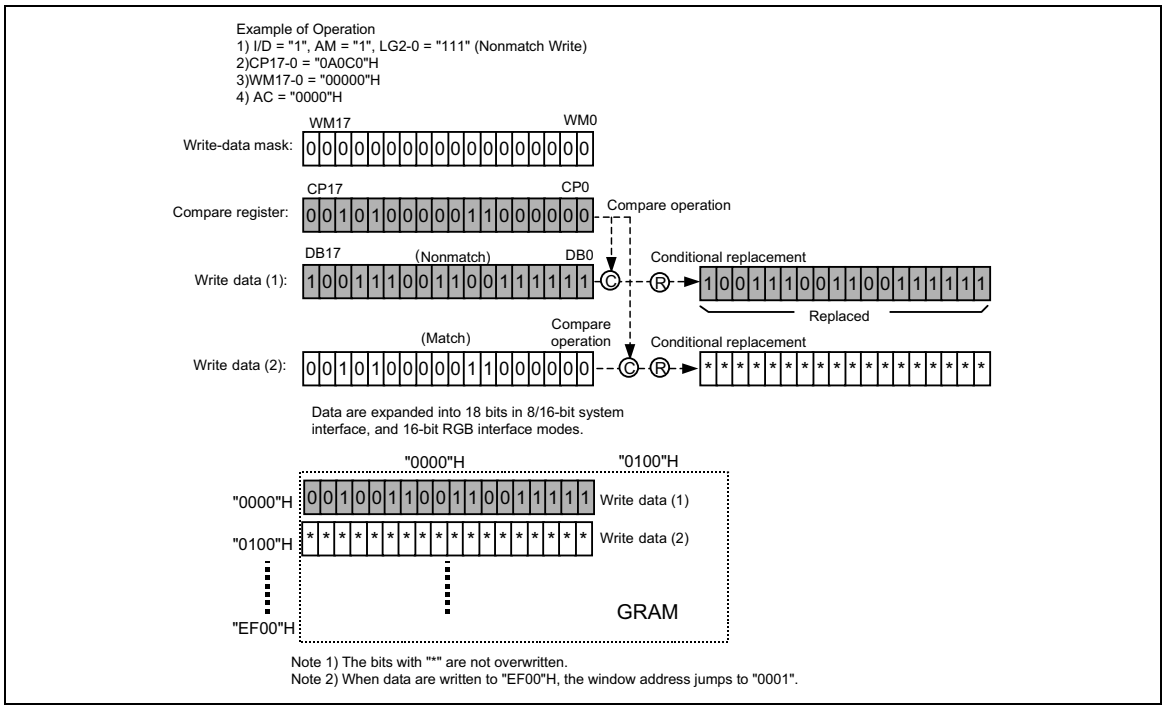
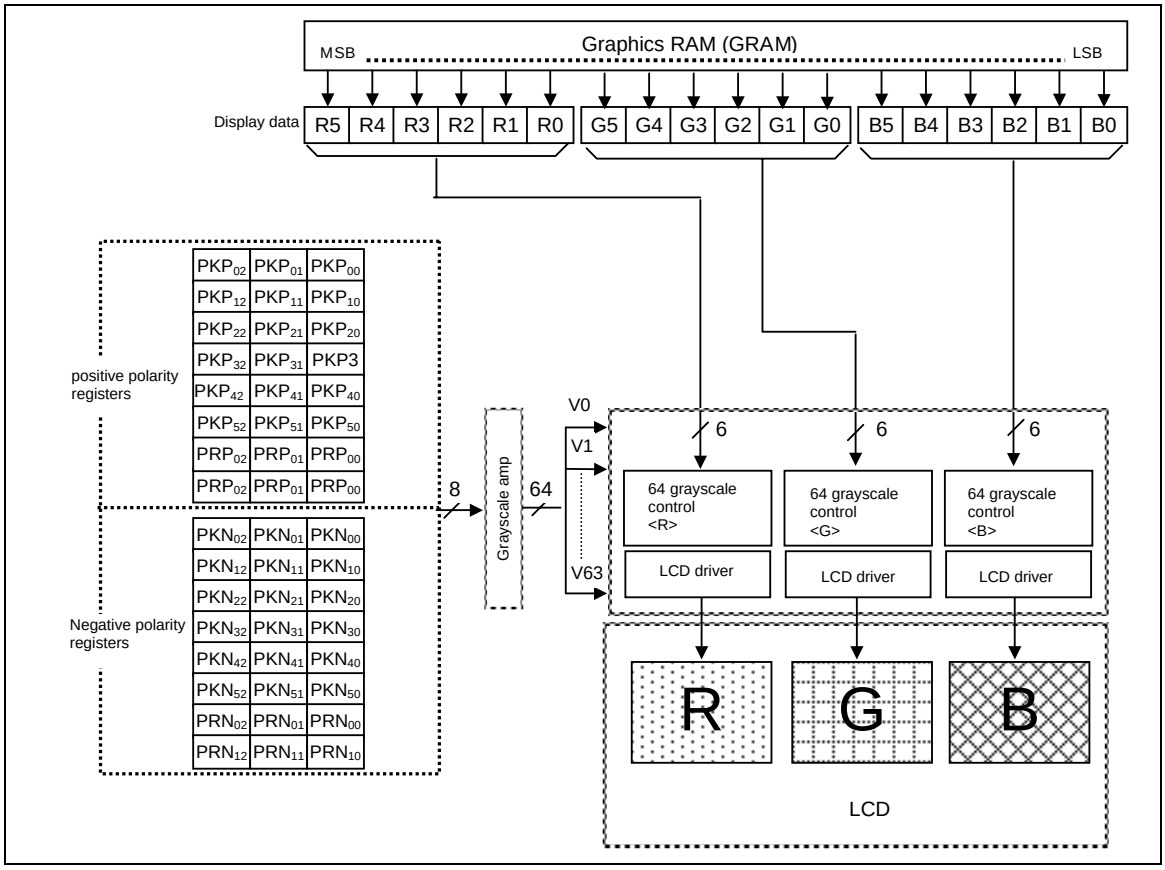


Figure 62 Writing Operation of Write Mode 4

γ-Correction Function

The HD66772 incorporates a γ-correction function to simultaneously display 262,144 colors. The γ-correction operation specifies eight levels of grayscale with gradient-adjustment and fine-adjustment registers. Select the polarity of these registers to match the LCD panel used. These registers are available for both polarities.



Configuration of Grayscale Amplifier

Eight levels (VIN0-7) are specified by the gradient-adjustment and fine-adjustment registers. 64 levels (V0-63) are generated by ladder resistors, which divide each level specified by the registers into more detailed levels.

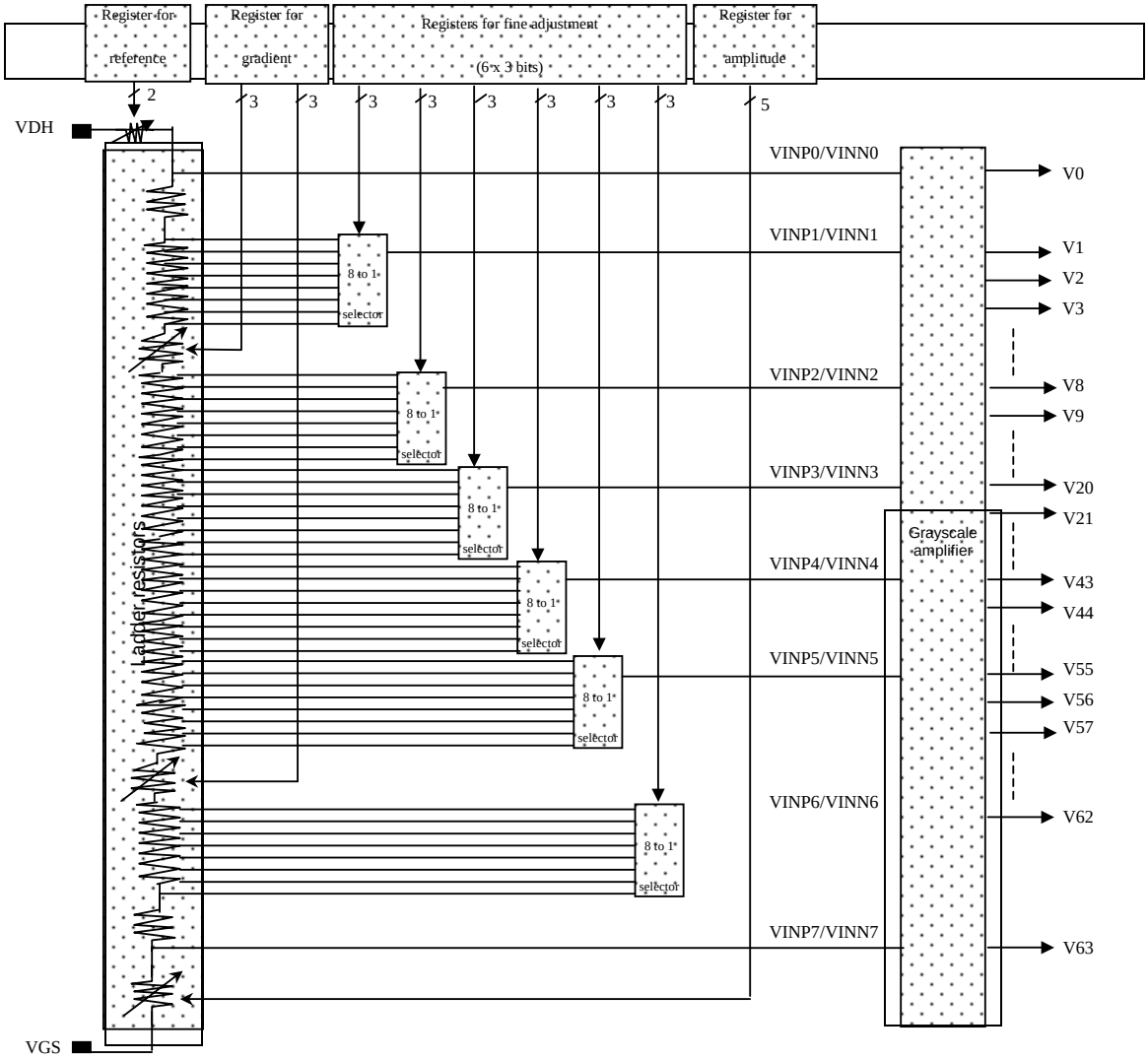


Figure 64 Configuration of Grayscale Amplifier

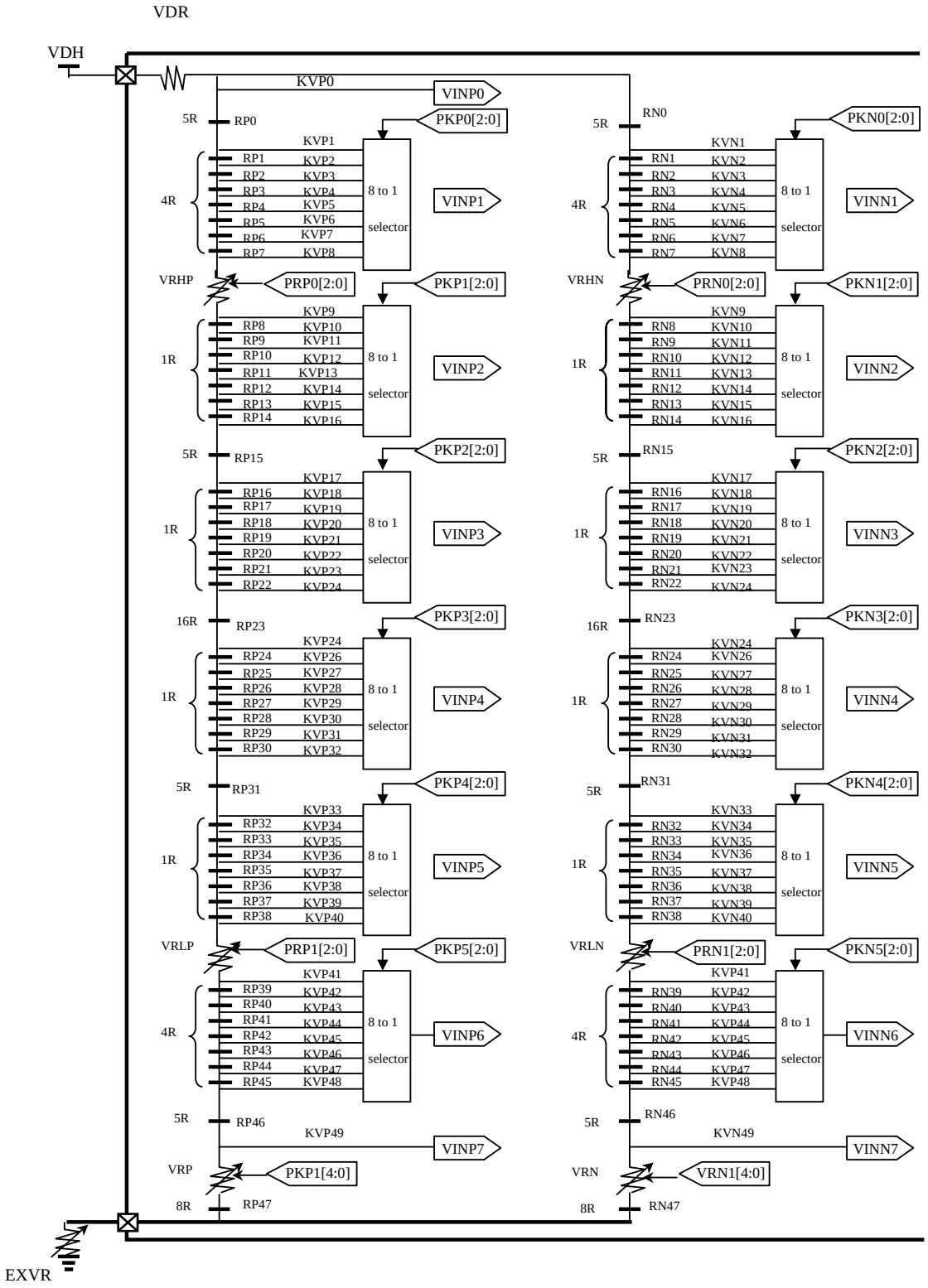
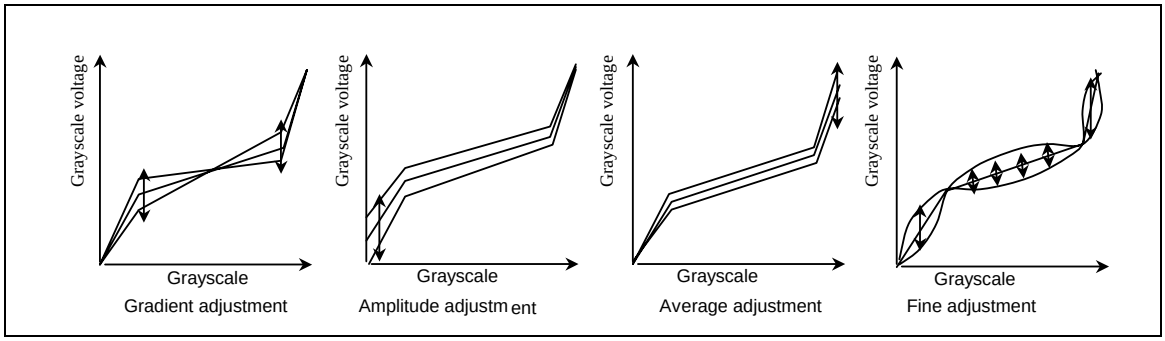


Figure 65 Ladder Amplifiers and 8 to 1 Selectors

γ-Correction Registers

This block has register groups for specifying a grayscale voltage that meets the γ-characteristics for the LCD panel used. These registers are divided into four groups, which correspond to the gradient, amplitude, average value and fine adjustment of the grayscale characteristics for the voltage. The polarity of each register can be specified independently. (average value and R, G, and B are common.)



1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. This function is implemented by controlling the variable resistor (VRHP (N)/VRL (N)) in the ladder resistor block for grayscale voltage generation. A register can be separated into positive/negative polarities to perform an asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling the variable resistor (VRP (N)) under the ladder resistor block for grayscale voltage generation. The VDH level can be adjusted higher. There is an independent register on the positive/negative polarities as well as the gradient adjustment register.

3. Resister of average value

Resister of average value is used to adjust the average value of the grayscale voltage. This function is implemented by controlling the variable resistor (VDR) above the ladder resistor block for grayscale voltage generation. This resistor is common to both the positive and negative.

4. Fine adjustment registers

The fine adjustment register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

Table 54 γ-Correction Registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 2 to 0	PRN0 2 to 0	Variable resistor VRHP (N)
	PRP1 2 to 0	PRN1 2 to 0	Variable resistor VRLP (N)
Amplitude adjustment	VRP 4 to 0	VRN 4 to 0	Variable resistor VRP (N)
Average adjustment	VDR 1 to 0		Variable resistor VDR
Fine adjustment	PKP0 2 to 0	PKN0 2 to 0	8-to-1 selector (voltage level of grayscale 1)
	PKP1 2 to 0	PKN1 2 to 0	8-to-1 selector (voltage level of grayscale 8)
	PKP2 2 to 0	PKN2 2 to 0	8-to-1 selector (voltage level of grayscale 20)
	PKP3 2 to 0	PKN3 2 to 0	8-to-1 selector (voltage level of grayscale 43)
	PKP4 2 to 0	PKN4 2 to 0	8-to-1 selector (voltage level of grayscale 55)
	PKP5 2 to 0	PKNS5 2 to 0	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8 to 1 selector

Block configuration

The block consists of two ladder resistors including variable one, and 8 to 1 selector which selects one voltage level generated by the ladder resistors and outputs the reference voltage for grayscale voltage. Furthermore, the block has pins to connect a variable resistor. It can adjust the variation between panels.

Variable resistor

The variable resistors are three types, gradient adjustment(VRHP(N)/VRLP(N)), amplitude adjustment (VRP(N)), and average adjustment (VDR). The resistances are set by the gradient adjustment and amplitude adjustment registers. Their relationship is shown below.

Table 55 Gradient adjustment

Contents of Register PRP(N) 2-0	Resistance VRP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 56 Amplitude adjustment

Contents of Register VRP(N) 4-0	Resistance VRP(N)
00000	0R
00001	1R
00010	2R
⋮	⋮
11101	29R
1111	30R
1111	31R

Table 57Average Control

Contents of Register VDR 1-0	Resistance VDR
00	0R
01	4R
10	8R
11	12R

8 to 1 selector

In the 8 to 1 selector, the voltage level can be selected from the levels which are generated by ladder resistors, and be output the six types of the reference voltage, the VIN1 to VIN 6. The following figure explains the relationship between the fine adjustment register and the selecting voltage.

Table 58 KVPP and KVPN

Contents of Register	**Selected Voltage**					
PKP(N)2-0	**VINP(N)1**	**VINP(N)2**	**VINP(N)3**	**VINP(N)4**	**VINP(N)5**	**VINP(N)6**
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels are determined by the following formulas.

Table 59 Voltage calculation formula (positive polarity) 1

Table Voltage Calculation Formula (positive polarity) 1

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VDH*r	-	VINP0
KVP1	VINP0 - ΔV * 5R /SUMRP	PKP02-00= 000	VINP1
KVP2	VINP0 - ΔV * 9R /SUMRP	PKP02-00= 001	
KVP3	VINP0 - ΔV * 13R /SUMRP	PKP02-00= 010	
KVP4	VINP0 - ΔV * 17R /SUMRP	PKP02-00= 011	
KVP5	VINP0 - ΔV * 21R /SUMRP	PKP02-00= 100	
KVP6	VINP0 - ΔV * 25R /SUMRP	PKP02-00= 101	
KVP7	VINP0 - ΔV * 29R /SUMRP	PKP02-00= 110	
KVP8	VINP0 - ΔV * 33R /SUMRP	PKP02-00= 111	
KVP9	VINP0 - ΔV * (33R+VRHP) /SUMRP	PKP12-10= 000	VINP2
KVP10	VINP0 - ΔV * (34R+VRHP) /SUMRP	PKP12-10= 001	
KVP11	VINP0 - ΔV * (35R+VRHP) /SUMRP	PKP12-10= 010	
KVP12	VINP0 - ΔV * (36R+VRHP) /SUMRP	PKP12-10= 011	
KVP13	VINP0 - ΔV * (37R+VRHP) /SUMRP	PKP12-10= 100	
KVP14	VINP0 - ΔV * (38R+VRHP) /SUMRP	PKP12-10= 101	
KVP15	VINP0 - ΔV * (39R+VRHP) /SUMRP	PKP12-10= 110	
KVP16	VINP0 - ΔV * (40R+VRHP) /SUMRP	PKP12-10= 111	
KVP17	VINP0 - ΔV * (45R+VRHP) /SUMRP	PKP22-20= 000	VINP3
KVP18	VINP0 - ΔV * (46R+VRHP) /SUMRP	PKP22-20= 001	
KVP19	VINP0 - ΔV * (47R+VRHP) /SUMRP	PKP22-20= 010	
KVP20	VINP0 - ΔV * (48R+VRHP) /SUMRP	PKP22-20= 011	
KVP21	VINP0 - ΔV * (49R+VRHP) /SUMRP	PKP22-20= 100	
KVP22	VINP0 - ΔV * (50R+VRHP) /SUMRP	PKP22-20= 101	
KVP23	VINP0 - ΔV * (51R+VRHP) /SUMRP	PKP22-20= 110	
KVP24	VINP0 - ΔV * (52R+VRHP) /SUMRP	PKP22-20= 111	
KVP25	VINP0 - ΔV * (68R+VRHP) /SUMRP	PKP32-30= 000	VINP4
KVP26	VINP0 - ΔV * (69R+VRHP) /SUMRP	PKP32-30= 001	
KVP27	VINP0 - ΔV * (70R+VRHP) /SUMRP	PKP32-30= 010	
KVP28	VINP0 - ΔV * (71R+VRHP) /SUMRP	PKP32-30= 011	
KVP29	VINP0 - ΔV * (72R+VRHP) /SUMRP	PKP32-30= 100	
KVP30	VINP0 - ΔV * (73R+VRHP) /SUMRP	PKP32-30= 101	
KVP31	VINP0 - ΔV * (74R+VRHP) /SUMRP	PKP32-30= 110	
KVP32	VINP0 - ΔV * (75R+VRHP) /SUMRP	PKP32-30= 111	
KVP33	VINP0 - ΔV * (80R+VRHP) /SUMRP	PKP42-40= 000	VINP5
KVP34	VINP0 - ΔV * (81R+VRHP) /SUMRP	PKP42-40= 001	
KVP35	VINP0 - ΔV * (82R+VRHP) /SUMRP	PKP42-40= 010	
KVP36	VINP0 - ΔV * (83R+VRHP) /SUMRP	PKP42-40= 011	
KVP37	VINP0 - ΔV * (84R+VRHP) /SUMRP	PKP42-40= 100	
KVP38	VINP0 - ΔV * (85R+VRHP) /SUMRP	PKP42-40= 101	
KVP39	VINP0 - ΔV * (86R+VRHP) /SUMRP	PKP42-40= 110	
KVP40	VINP0 - ΔV * (87R+VRHP) /SUMRP	PKP42-40= 111	
KVP41	VINP0 - ΔV * (87R+VRHP+VRLP) /SUMRP	PKP52-50= 000	VINP6
KVP42	VINP0 - ΔV * (91R+VRHP+VRLP) /SUMRP	PKP52-50= 001	
KVP43	VINP0 - ΔV * (95R+VRHP+VRLP) /SUMRP	PKP52-50= 010	
KVP44	VINP0 - ΔV * (99R+VRHP+VRLP) /SUMRP	PKP52-50= 011	
KVP45	VINP0 - ΔV * (103R+VRHP+VRLP) /SUMRP	PKP52-50= 100	
KVP46	VINP0 - ΔV * (107R+VRHP+VRLP) /SUMRP	PKP52-50= 101	
KVP47	VINP0 - ΔV * (111R+VRHP+VRLP) /SUMRP	PKP52-50= 110	
KVP48	VINP0 - ΔV * (115R+VRHP+VRLP) /SUMRP	PKP52-50= 111	
KVP49	VINP0 - ΔV * (120R+VRHP+VRLP) /SUMRP	-	VINP7

r : {[(SUMRP*SUMRN)/(SUMRP+SUMRN)]/[(SUMRP*SUMRN)/(SUMRP+SUMRN)]+EXVR}

SUMRP : Sum of positive ladder resistors = 128R + VRHP + VRLP + VRP

SUMRN : Sum of negative ladder resistors = 128R + VRHN + VRLN + VRN

ΔV: Difference of voltage between KV0 and KV49

= VDH * SUMRP * SUMRN / [SUMRP * SUMRN + EXVR * (SUMRP + SUMRN)]

Table 60 Voltage calculation formula (positive polarity) 2

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VINP2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VINP6
V63	VINP7

Note: The folloing relationship should be retained.

DDVDH-V0 > 0.5V

DDVDH-V8 > 1.1V

V55-GND > 1.1V

Table 61 Voltage calculation formula (negative polarity) 1

Pin	Formula	Fine adjustment register value	Reference voltage
KVN0	VDH*r	-	VINN0
KVN1	VINN0 - ΔV * 5R /SUMRN	PKN02-00= 000	VINN1
KVN2	VINN0 - ΔV * 9R /SUMRN	PKN02-00= 001	
KVN3	VINN0 - ΔV * 13R /SUMRN	PKN02-00= 010	
KVN4	VINN0 - ΔV * 17R /SUMRN	PKN02-00= 011	
KVN5	VINN0 - ΔV * 21R /SUMRN	PKN02-00= 100	
KVN6	VINN0 - ΔV * 25R /SUMRN	PKN02-00= 101	
KVN7	VINN0 - ΔV * 29R /SUMRN	PKN02-00= 110	
KVN8	VINN0 - ΔV * 33R /SUMRN	PKN02-00= 111	
KVN9	VINN0 - ΔV * (33R+VRHN) /SUMRN	PKN12-10= 000	VINN2
KVN10	VINN0 - ΔV * (34R+VRHN) /SUMRN	PKN12-10= 001	
KVN11	VINN0 - ΔV * (35R+VRHN) /SUMRN	PKN12-10= 010	
KVN12	VINN0 - ΔV * (36R+VRHN) /SUMRN	PKN12-10= 011	
KVN13	VINN0 - ΔV * (37R+VRHN) /SUMRN	PKN12-10= 100	
KVN14	VINN0 - ΔV * (38R+VRHN) /SUMRN	PKN12-10= 101	
KVN15	VINN0 - ΔV * (39R+VRHN) /SUMRN	PKN12-10= 110	
KVN16	VINN0 - ΔV * (40R+VRHN) /SUMRN	PKN12-10= 111	
KVN17	VINN0 - ΔV * (45R+VRHN) /SUMRN	PKN22-20= 000	VINN3
KVN18	VINN0 - ΔV * (46R+VRHN) /SUMRN	PKN22-20= 001	
KVN19	VINN0 - ΔV * (47R+VRHN) /SUMRN	PKN22-20= 010	
KVN20	VINN0 - ΔV * (48R+VRHN) /SUMRN	PKN22-20= 011	
KVN21	VINN0 - ΔV * (49R+VRHN) /SUMRN	PKN22-20= 100	
KVN22	VINN0 - ΔV * (50R+VRHN) /SUMRN	PKN22-20= 101	
KVN23	VINN0 - ΔV * (51R+VRHN) /SUMRN	PKN22-20= 110	
KVN24	VINN0 - ΔV * (52R+VRHN) /SUMRN	PKN22-20= 111	
KVN25	VINN0 - ΔV * (68R+VRHN) /SUMRN	PKN32-30= 000	VINN4
KVN26	VINN0 - ΔV * (69R+VRHN) /SUMRN	PKN32-30= 001	
KVN27	VINN0 - ΔV * (70R+VRHN) /SUMRN	PKN32-30= 010	
KVN28	VINN0 - ΔV * (71R+VRHN) /SUMRN	PKN32-30= 011	
KVN29	VINN0 - ΔV * (72R+VRHN) /SUMRN	PKN32-30= 100	
KVN30	VINN0 - ΔV * (73R+VRHN) /SUMRN	PKN32-30= 101	
KVN31	VINN0 - ΔV * (74R+VRHN) /SUMRN	PKN32-30= 110	
KVN32	VINN0 - ΔV * (75R+VRHN) /SUMRN	PKN32-30= 111	
KVN33	VINN0 - ΔV * (80R+VRHN) /SUMRN	PKN42-40= 000	VINN5
KVN34	VINN0 - ΔV * (81R+VRHN) /SUMRN	PKN42-40= 001	
KVN35	VINN0- ΔV * (82R+VRHN) /SUMRN	PKN42-40= 010	
KVN36	VINN0 - ΔV * (83R+VRHN) /SUMRN	PKN42-40= 011	
KVN37	VINN0 - ΔV * (84R+VRHN) /SUMRN	PKN42-40= 100	
KVN38	VINN0 - ΔV * (85R+VRHN) /SUMRN	PKN42-40= 101	
KVN39	VINN0 - ΔV * (86R+VRHN) /SUMRN	PKN42-40= 110	
KVN40	VINN0 - ΔV * (87R+VRHN) /SUMRN	PKN42-40= 111	
KVN41	VINN0 - ΔV * (87R+VRHP+VRLN) /SUMRN	PKN52-50= 000	VINN6
KVN42	VINN0 - ΔV * (91R+VRHP+VRLN) /SUMRN	PKN52-50= 001	
KVN43	VINN0 - ΔV * (95R+VRHP+VRLN) /SUMRN	PKN52-50= 010	
KVN44	VINN0 - ΔV * (99R+VRHP+VRLN) /SUMRN	PKN52-50= 011	
KVN45	VINN0 - ΔV * (103R+VRHP+VRLN) /SUMRN	PKN52-50= 100	
KVN46	VINN0 - ΔV * (107R+VRHP+VRLN) /SUMRN	PKN52-50= 101	
KVN47	VINN0 - ΔV * (111R+VRHP+VRLN) /SUMRN	PKN52-50= 110	
KVN48	VINN0 - ΔV * (115R+VRHP+VRLN) /SUMRN	PKN52-50= 111	
KVN49	VINN0 - ΔV * (120R+VRHP+VRLN) /SUMRN	-	VINN7

r : {[(SUMRP*SUMRN)/(SUMRP+SUMRN)]/[(SUMRP*SUMRN)/(SUMRP+SUMRN)]+EXVR}

SUMRP : Sum of positive ladder resistors = 128R + VRHP + VRLP + VRP

SUMRN : Sum of negative ladder resistors = 128R + VRHN + VRLN + VRN

ΔV: Difference of voltage between KV0 and KV49

= VDH * SUMRP * SUMRN / [SUMRP * SUMRN + EXVR * (SUMRP + SUMRN)]

Table 50 Voltage calculation formula (negative polarity) 2

Table Voltage Calculation Formula (negative polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V43+(V20-V43)*(11/23)
V1	VINN1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINN2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINN4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINN3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINN5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINN6
V31	V43+(V20-V43)*(12/23)	V63	VINN7

Note: The folloing relationship should be retained.

DDVDH-V0 > 0.5V

DDVDH-V8 > 1.1V

V55-GND > 1.1V

Relationship between RAM data and output level

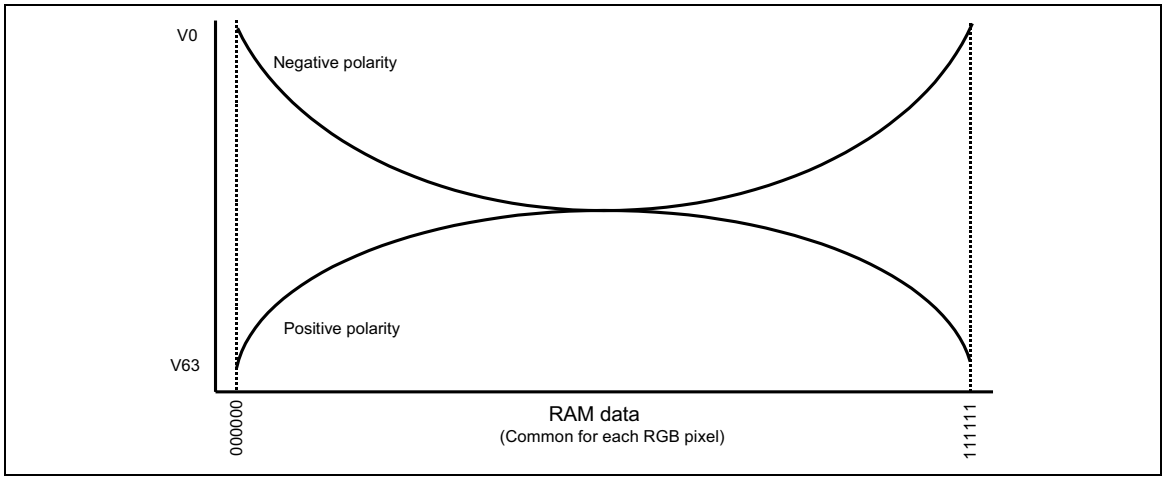


Figure 67 Relationship between RAM Data and Output Voltage

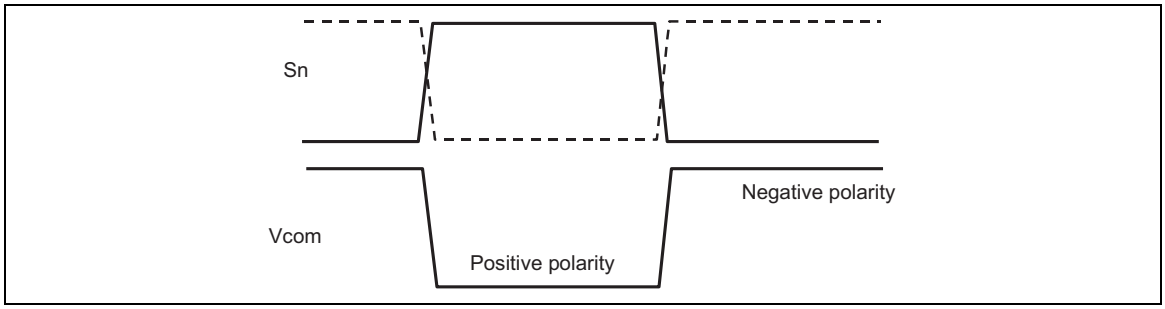


Figure 68 Relationship between Source Output and Vcom

8-color Display Mode

The HD66772 incorporates an 8-color display mode. The grayscale level to be used is V0 and V63, and the other levels (V1-V62) are stopped. This, therefore, achieved to reduce the power consumption.

γ-fine-adjustment registers, PKP00-PKP52 and PKN00-PKN52 are invalid in 8-color display mode. Since V1-V62 are stopped, the RGB data in the GRAM should be set to 000000 or 111111 before setting the mode so that V0 or V63 is selected.

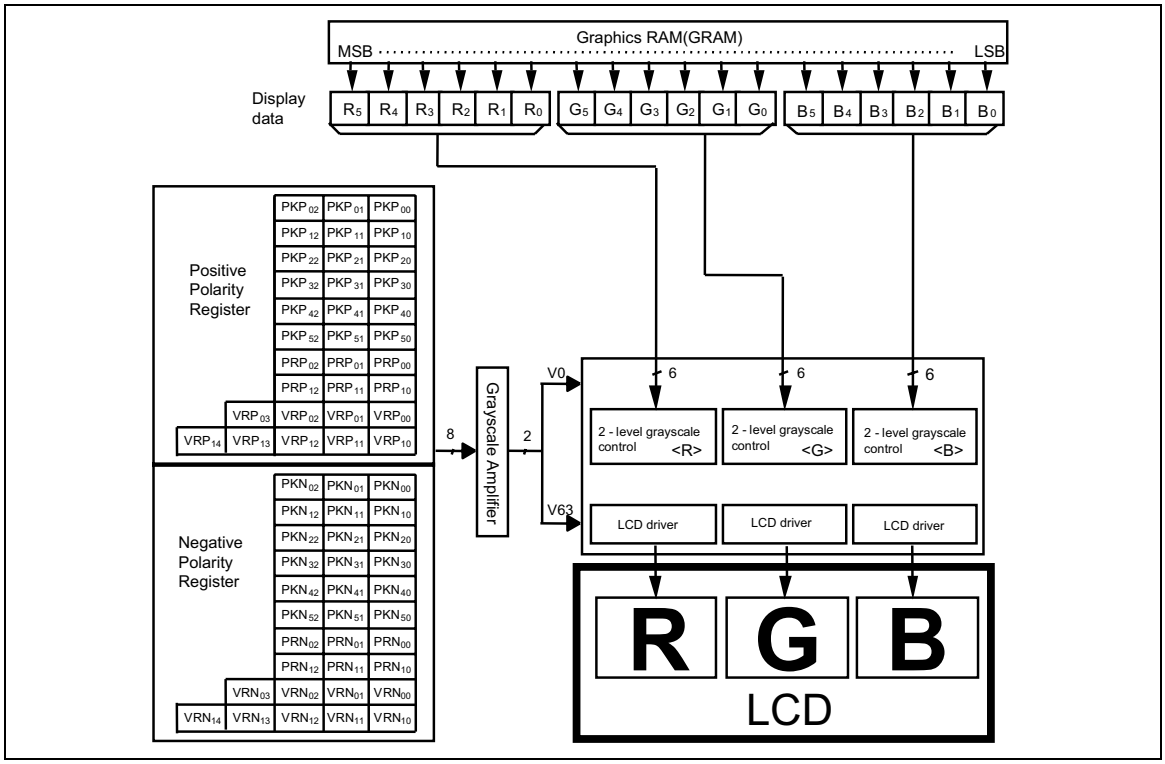
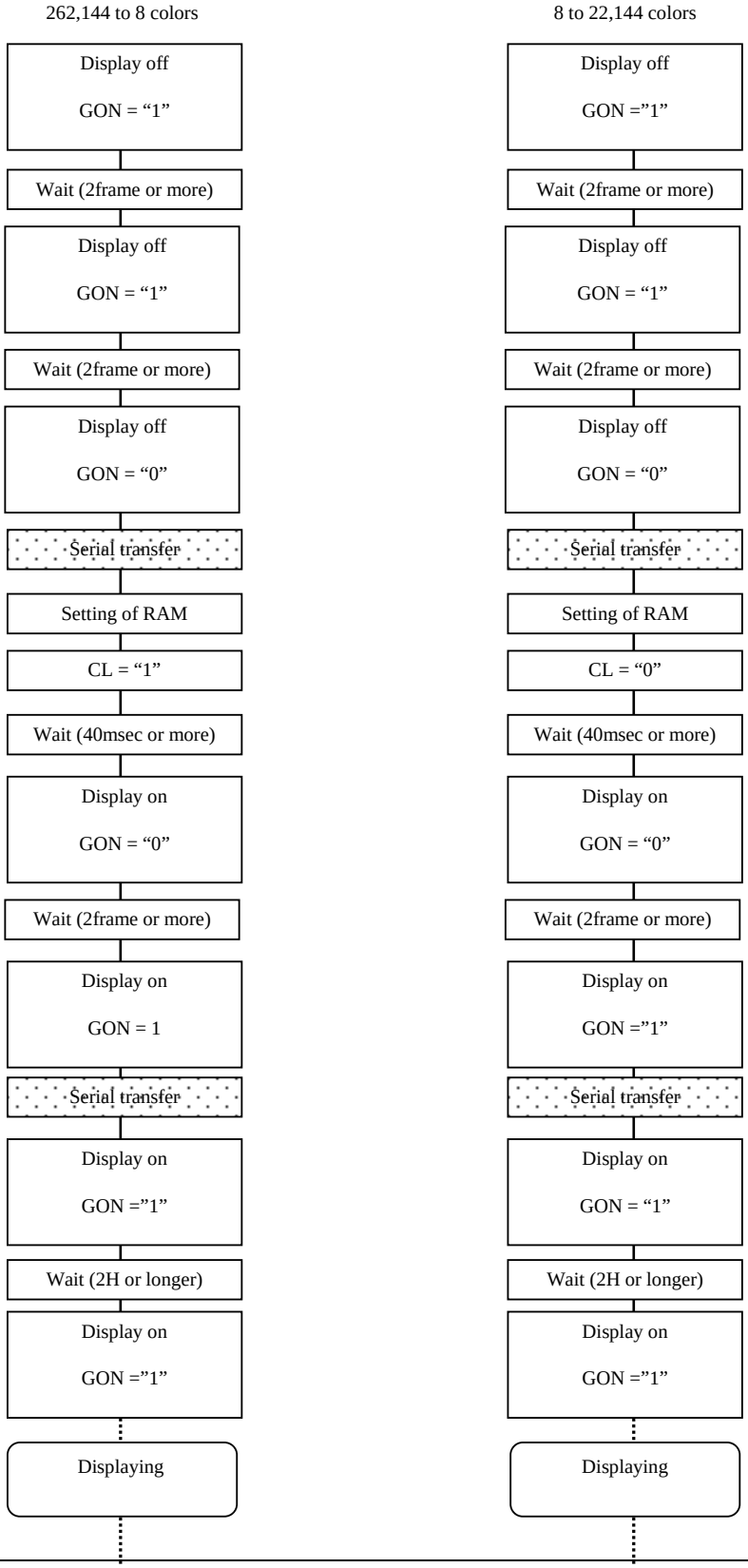


Figure 69 Grayscale Control


262,144 to 8 colors
Display off
GON = “1”
Wait (2frame or more)
Display off
GON = “1”
Wait (2frame or more)
Display off
GON = “0”
Serial transfer
Setting of RAM
CL = “1”
Wait (40msec or more)
Display on
GON = “0”
Wait (2frame or more)
Display on
GON = 1
Serial transfer
Display on
GON =”1”
Wait (2H or longer)
Display on
GON =”1”
Displaying
8 to 22,144 colors
Display off
GON =”1”
Wait (2frame or more)
Display off
GON = “1”
Wait (2frame or more)
Display off
GON = “0”
Serial transfer
Setting of RAM
CL = “0”
Wait (40msec or more)
Display on
GON = “0”
Wait (2frame or more)
Display on
GON =”1”
Serial transfer
Display on
GON = “1”
Wait (2H or longer)
Display on
GON =”1”
Displaying

Example of System Configuration

The connecting method is changed by setting of the Vcom voltage. The following diagram indicates a connection example of the HD66772 and HD667P00 when VcomL < 0V, 0V ≤ VcomL < 0.5V.

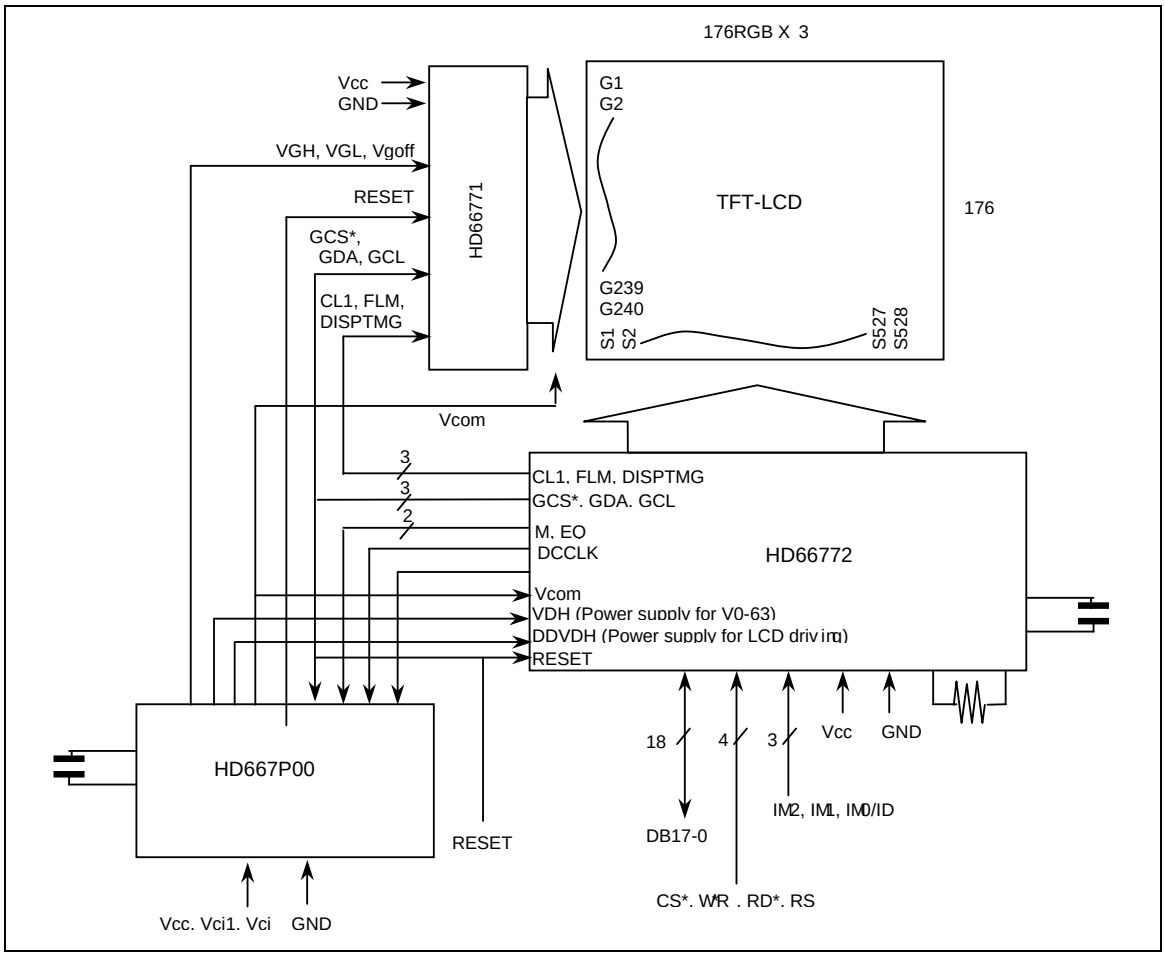
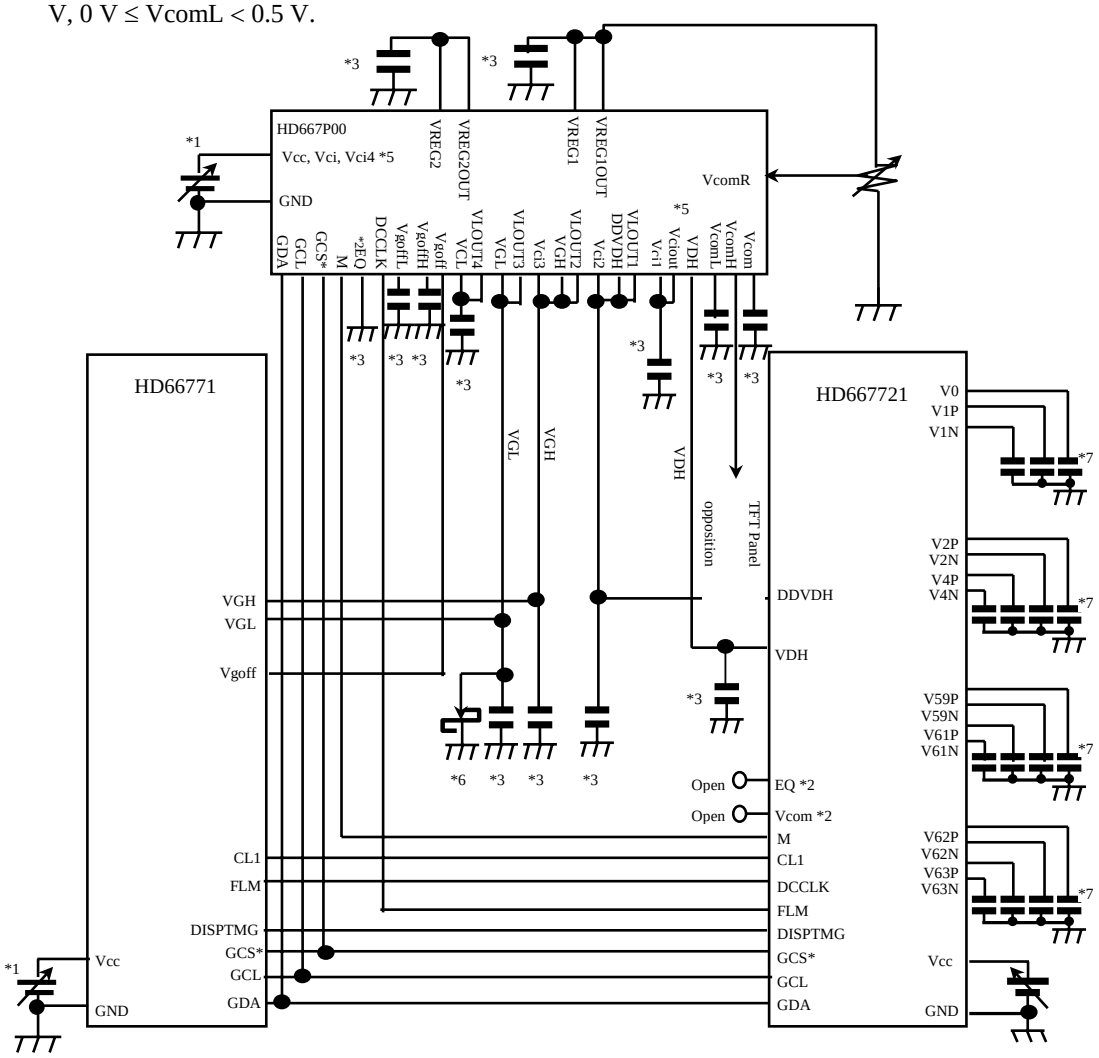


Figure 71 System Configuration

Example of Connection to HD66771 and HD667P00

The connecting method is changed by setting of the Vcom voltage.

The following diagram indicates a connection example of the HD66771 and HD667P00 when VcomL < 0 V, 0 V ≤ VcomL < 0.5 V.



Note 1: Vcc (GND) input to HD66772, HD6771, and HD67P00 should be the same.

2: EQ pin of HD66772 should be connected to one of HD667P00. Vcom pins of HD66772 should not be connected. EQ pin of HD667P00 should be connected to ones of HD667P00. Vcom pins should not be supplied 5.5V or more.

3: Use 1-uF capacitors for stabilizing.

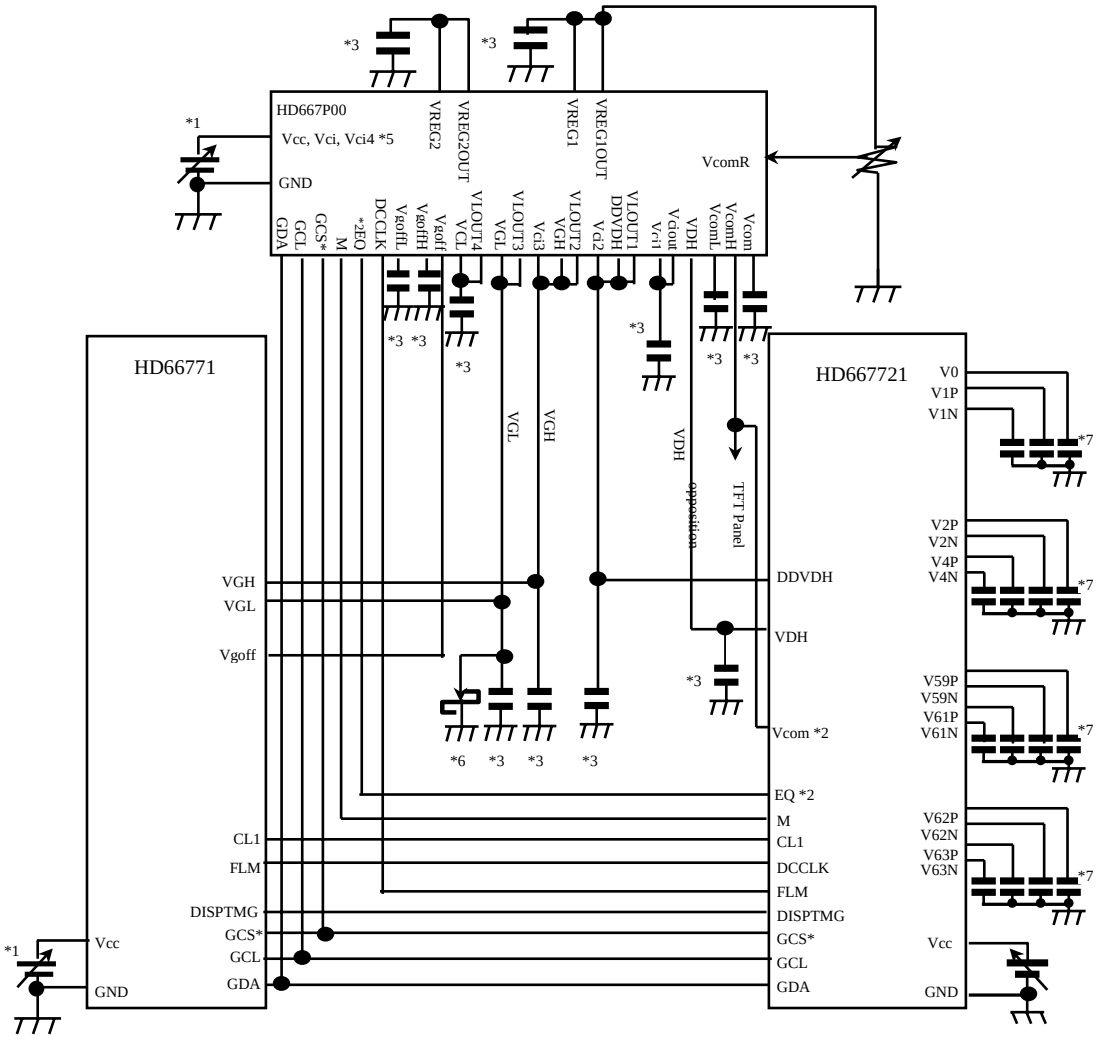
4: The following capacitors are not described here. Connect these capacitors according to the HD667P00 pin function. C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31- to C41-, and C41+

5: Vci should be supplied an external voltage of 2.5 to 3.3V. Connect Vciout to Vci1 or supply an external voltage of 2.5 to 3.3V to Vci1. When Vci1 is connected an external voltage, Vciout should not be connected.

6: Connect a Schottky barrier diode (approximately VF = 0.4V/ 20mA and VR330V).

7: Use 0.1-mF capacitors for stabilizing.

The following diagram indicates a connection example of the gate driver, HD66771 and power supply IC when 0 V ≤ VcomL < 5.5V and an equalizing function is used



Note 1: Vcc (GND) input to HD66772, HD6771, and HD67P00 should be the same.

2: EQ pin of HD66772 should be connected to one of HD667P00. Vcom pins of HD66772 should not be connected. EQ pin of HD667P00 should be connected to ones of HD667P00. Vcom pins should not be supplied 5.5V or more.

3: Use 1-uF capacitors for stabilizing.

4: The following capacitors are not described here. Connect these capacitors according to the HD667P00 pin function. C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31- to C41-, and C41+

5: Vci should be supplied an external voltage of 2.5 to 3.3V. Connect Vciout to Vci1 or supply an external voltage of 2.5 to 3.3V to Vci1. When Vci1 is connected an external voltage, Vciout should not be connected.

6: Connect a Schottky barrier diode (approximately VF = 0.4V/ 20mA and VR330V).

7: Use 0.1-mF capacitors for stabilizing.

Figure 73 Example of Connection to HD66771 when 0 V ≤ VcomL < 5.5 V

Specification of capacitor connected to HD667P00

The following table indicates the specification of capacitor connected to HD667P00.

Table 62

Product	Capacity of Capacitor	Recommendation resist pressure for capacitor	Connect pins
HD667P00 HD66774	1uF (B Character)	6V	VREG1OUT, Vciout, C41-/+*1, VLOUT4*1, VcomH, VcomL*1
		10V	VLOUT1, C11-/+, C12-/+, C21-/+, C22-/+, C23-/+
		25V	VREG2OUT, VLOUT2, VLOUT3, C31/+, VgoffH*1 , VgoffL
	0.1uF (B Character)	6V	VDH, (TESTA1) *2 , (TESTA2) *2, (REGN) *2
		25V	(TESTA3) *2 , (TESTA4) *2
HD66772	0.1uF (B Character)	6V	V0,V1P, V1N, V2P, V2N, V4P, V4N, V59P, V59N, V61P, V61N, V62P, V62N, V63P, V63N

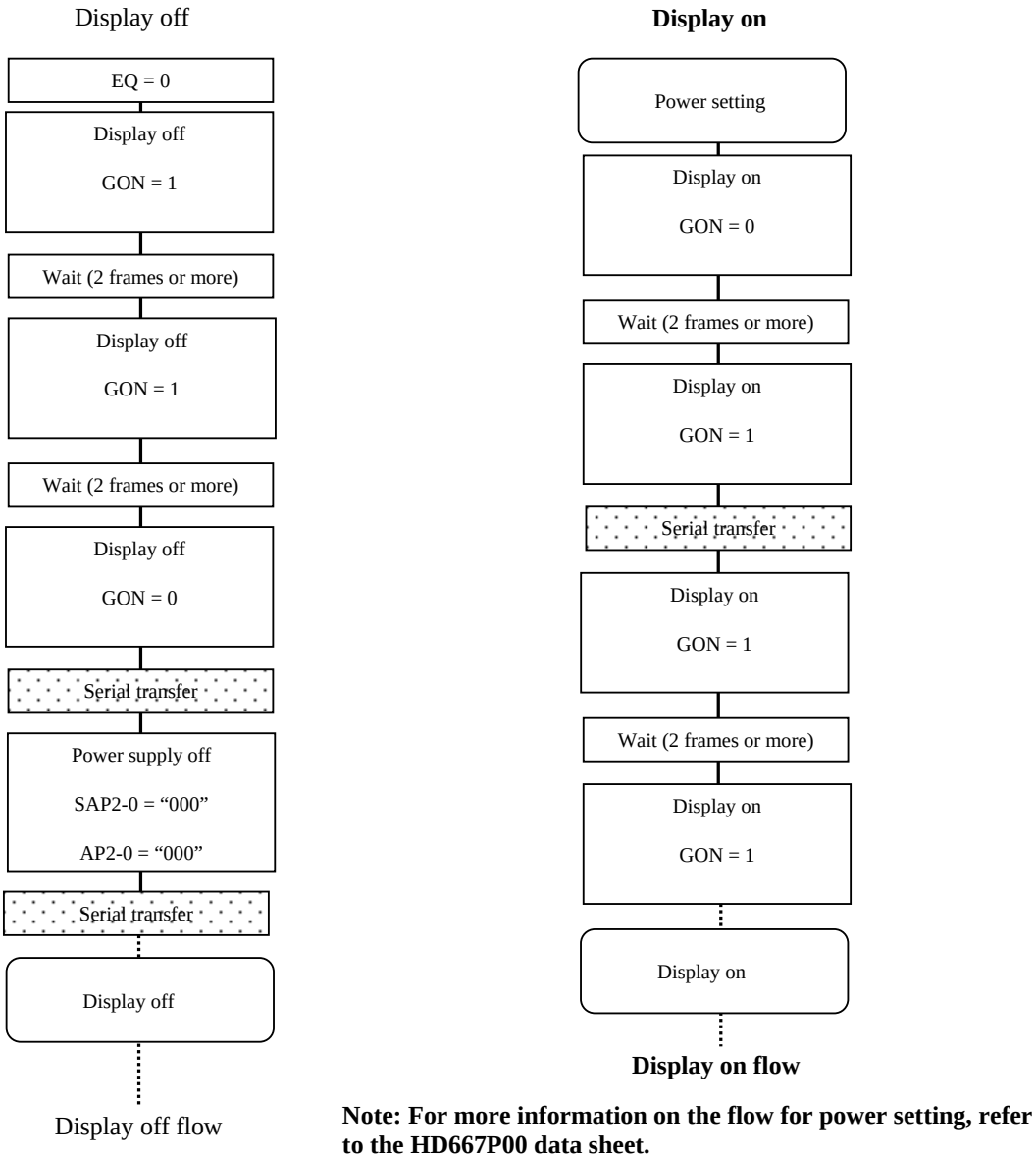
*1 According to the mode set to HD667P00, there is some cases in which capacitor is unnecessary.

*2 Connect a capacitor to stabilize picture. Be noticed that power consumption may rise in great amount.

Instruction Setting Flow

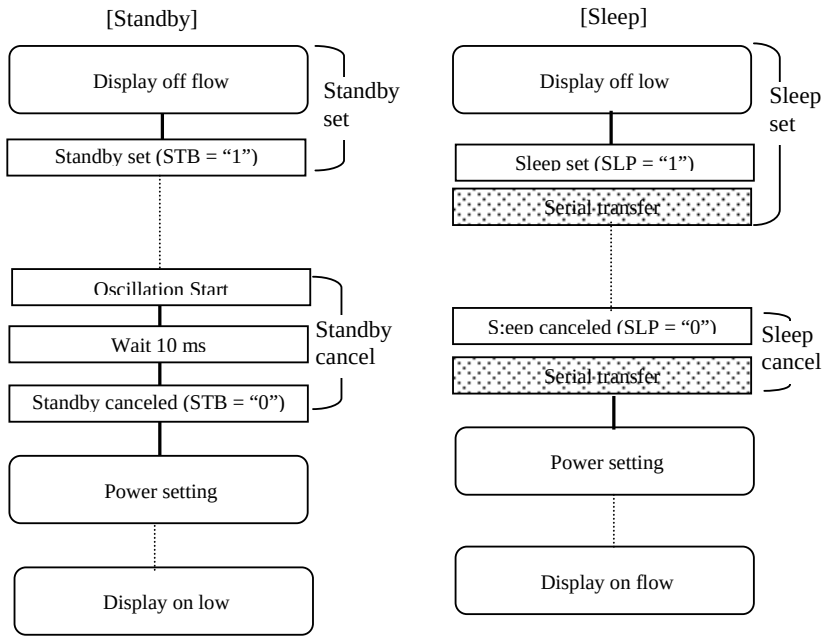
When the HD66771/HD667P00 are used, follow the instruction setting flow. The instruction setting for the HD66771/HD667P00 is executed by the serial interface. When the instruction for the HD66771/HD667P00 is set, the serial transfer must be executed to the HD66771/HD667P00. The transfer to the HD66771/HD667P00 must be executed immediately after the instruction set.

Follow the below serial transfer flow about each setting and then transfer must be executed.



Note: For more information on the flow for power setting, refer to the HD667P00 data sheet.

Figure 74 Instruction Setting Flow



Note: For more information on the flow for power settings, refer to the HD667P00 data sheet.

Figure 75 Instruction Setting Flow (standby and sleep modes)

Oscillation Circuit

The HD66772 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

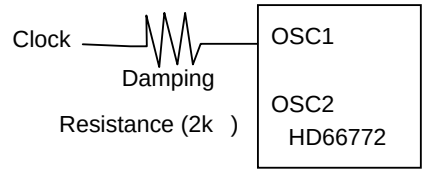
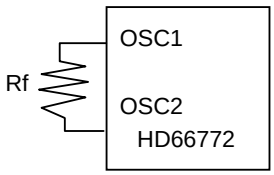


Figure 76 Oscillation Circuits (external clock mode)



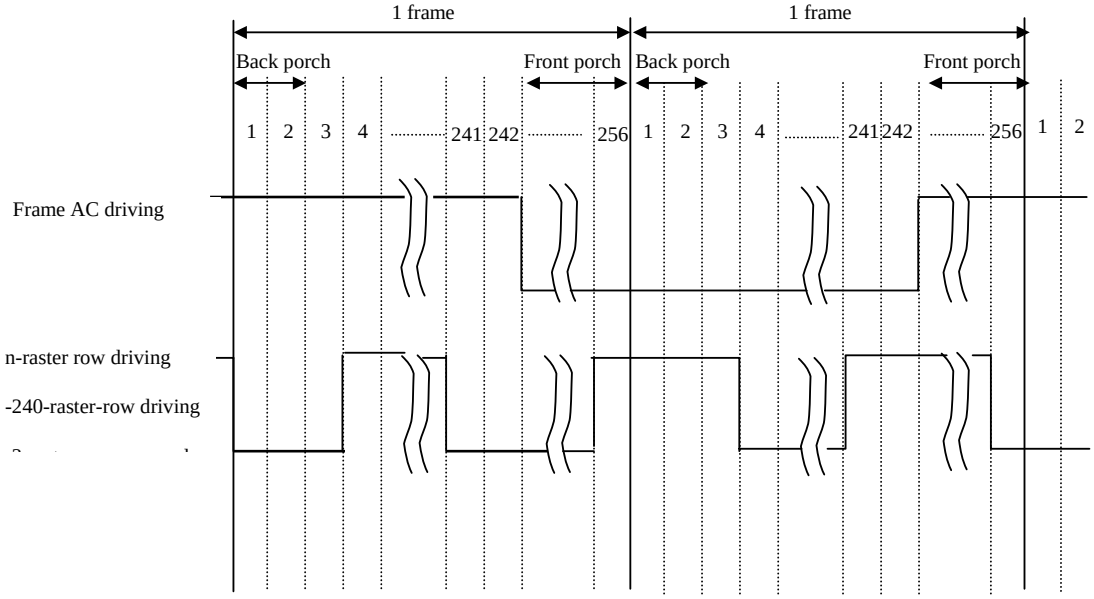
Note: The Rf resistance must be located near the OSC1/OSC2 pin on the master side.

Figure 77 Oscillation Circuits (external resistance oscillation mode)

n-raster-row Reversed AC Drive

The HD66772 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: In an n-raster row driving, EOR should be “1” so that DC bias voltage is not applied.

Figure 78 Example of an AC Signal under n-raster-row Reversed AC Drive

Interlaced Driving

The HD66772 supports the interlaced driving to avoid flicker. One frame is divided into n-field to drive.

Determine the number of fields after confirmation of the display quality with the actual LCD panel. The gate selection where the number of fields is 1 or 3 are shown in table, the output waveform when 3-field interlaced driving is performed is shown in figure.

Table 63 FLD and filed

GS = 0

FLD1-0	**01**		**11**	
Field / Gate		**1**	**2**	**3**
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
⋮	⋮	⋮	⋮	⋮
G173	O	O		
G174	O		O	
G175	O			O
G176	O	O		

GS = 1

FLD1-0	**01**		**11**	
Field / Gate		**1**	**2**	**3**
G228	O	O		
G227	O		O	
G226	O			O
G225	O	O		
G224	O		O	
G223	O			O
G222	O	O		
G221	O		O	
G220	O			O
⋮	⋮	⋮	⋮	⋮
G56	O	O		
G55	O		O	
G54	O			O
G53	O	O		

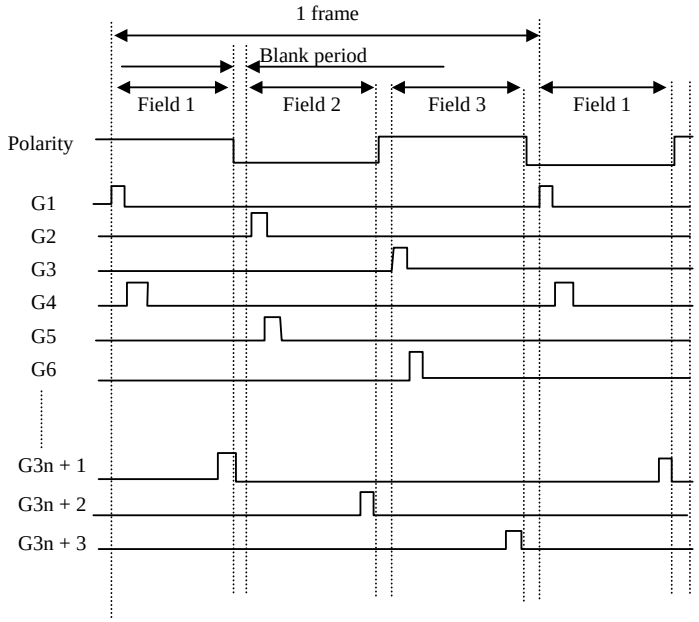


Figure 79 Output Timing for Interlaced Gate Signals when Three-Field is Selected

AC Drive Timing

The following diagram indicates the timing of changing polarity on the each A/C drive method. LCD drive polarity is changed after every frame. After the A/C this timing, the blank (all outputs from the gate: Vgoff output) in a 16H period is inserted. Also, LCD drive polarity is change after every field when it is on the interlace drive and blank is inserted in every timing. The amount of blanking periods becomes 16H in a frame. When the reversed n-raster-row is driving, a blank period of the 16H period is inserted after all screens are drawn.

Note: The settings for the front and back porch should be the number of fields or more when the interlaced drive is in use.

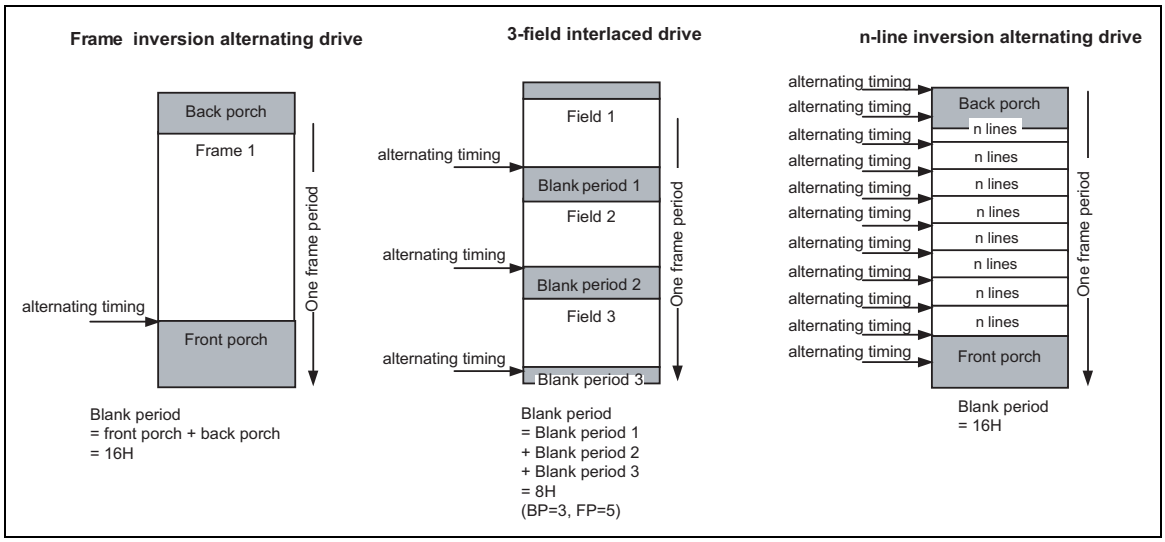


Figure 80 AC Drive Timing

Frame-Frequency Adjustment Function

The HD66772 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive as the oscillation frequency is always same.

If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1-H period bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{fosc}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line} + 8)} \text{ [Hz]}$$

fosc: R-C oscillation frequency

Line: number of drive raster-rows (NL bit)

Clock cycles per raster-row: RTN bit

Division ratio: DIV bit

Example Calculation In the case of the maximum frame frequency = 60 Hz

Number of drive raster-rows: 240

1-H period: 16 clock cycles (RTN3-0 = 0000)

Operation clock division ratio: 1 division

fosc = 60 Hz × (0 + 16) clock × 1 division × (240 + 16) lines = 246 (kHz)

In this case, the R-C oscillation frequency becomes 246 kHz. The external resistance value of the R-C oscillator must be adjusted to be 246 kHz. The display duty can be changed by the partial display, etc. and the frame frequency can be the same by setting the RNT bit and DIV bit to achieve the following.

Screen-division Driving Function

The HD66772 can select and drive two screens at any position with the screen-driving position registers (R42 and R43). Any two screens required for display are selectively driven, thus reducing power consumption.

For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R42). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen driving position register (R43). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must be the number of LCD drive raster-rows or less.

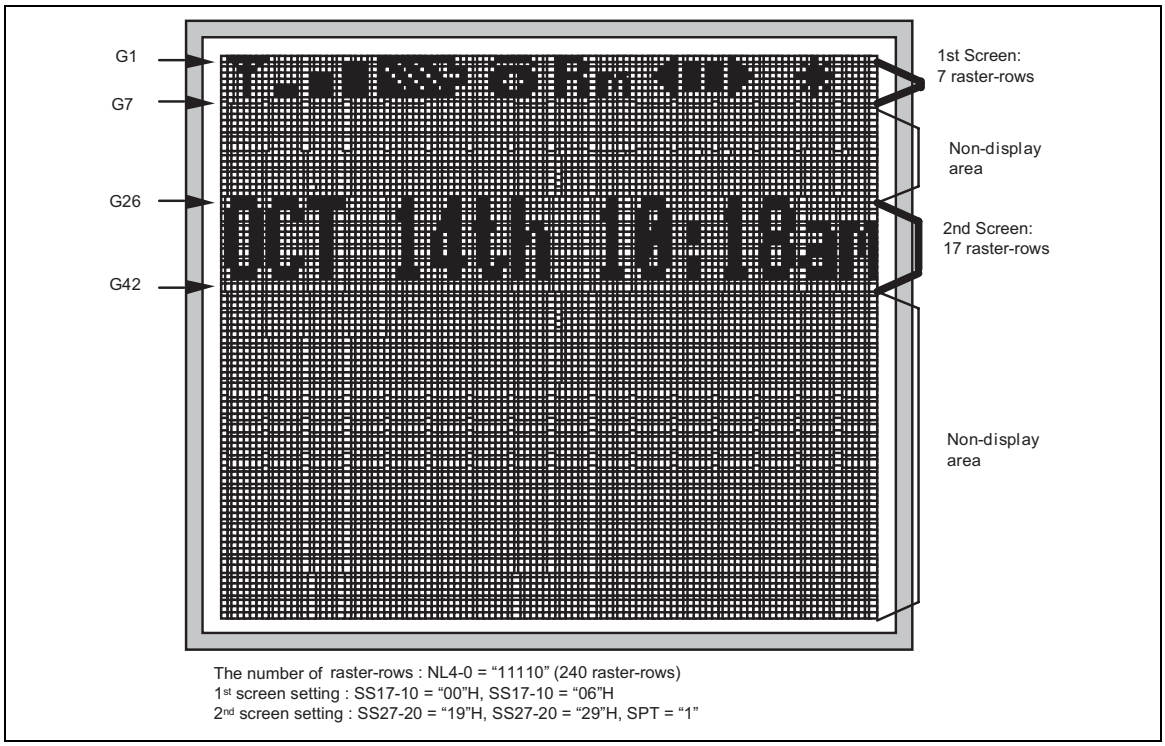


Figure 81 Example of Screen-Division

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R42) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R43) for the HD66772. Note that incorrect display may occur if the restrictions are not satisfied.

Table 64 Restrictions on the One Screen Driving (STP = 0)

Register Settings	Display Operation
(SE17-10) - (SS17-10) = NL	Whole screen display The area of (SE17-10) - (SS17-10) is normally displayed.
(SE17-10) - (SS17-10) < NL	Partial screen display The area of (SE17-10) - (SS17-10) is normally displayed. In all other display area refers to the output level based on the PT setting (non-display).
(SE17-10) - (SS17-10) > NL	Setting disabled

Notes: 1. SS17-10 ≤ SE17-0 ≤ "EF"H
2. The SS27-20 and SE27-20 settings are ignored.

Table 65 Restrictions on the Two Screen Driving (STP = 1)

Register Settings	Display Operation
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) = NL	Whole screen display The area of (SE27-20) - (SS17-10) is normally displayed.
((SE17-10) - (SS17-10)) + ((SE27-20) - (S27-20)) < NL	Partial screen display The area of (SE27-10) - (SS17-10) is normally displayed. In all other display area refers to the output level based on the PT setting (non-display).
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) > NL	Setting disabled

Notes: 1. SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ EFH
2. The ((SE27-20) - (SS17-10)) setting should be NL or less.

The driver output can be set for non-display area during the partial display. Determine based on characteristic of the display panels.

Table 66 Source and gate outputs for non-display area

		Source Output for Non-Display Area		Gate Output for Non-Display Area
PT1	PT0	Positive Polarity	Negative Polarity	Gate Driver Used
0	0	V63	V0	Normal Operation
0	1	V63	V0	Vgoff
1	0	GND	GND	Vgoff
1	1	High-Z	High-Z	Vgoff

Setting of the partial display should follow the flow shown below.

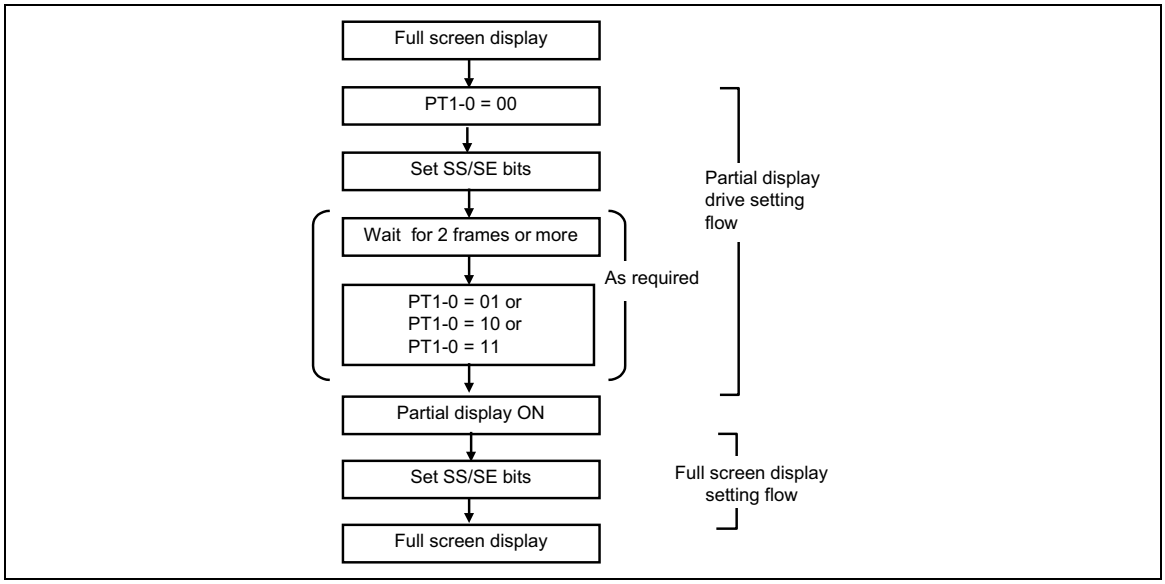


Figure 82 Setting of Partial Display

Absolute Maximum Ratings

Table 67

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	Vcc	V	-0.3 to + 4.6	1, 2
Power supply voltage (2)	Vcil	V	-0.3 to + 6.0	1, 3
Input voltage	Vt	V	-0.3 to Vcc + 0.3	1
Operating temperature	Topr	°C	-40 to + 85	1, 4
Storage temperature	Tstg	°C	-55 to + 110	1, 5

Note 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

Note 2. Vcc ≥ GND must be maintained

Note 3. DDVDH ≥ GND must be maintained.

Note 4.For die and wafer products, specified up to 85 °C.

Note 5.This temperature specifications apply to the TCP package.

DC Characteristics

Table 68 (V_{CC} = 1.8 to 3.7 V, Ta = –40 to +85°C*[1])

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	V_{CC} = 1.8 to 3.7 V	0.7 V_{CC}	—	V_{CC}	2, 3
Input low voltage (1) (OSC1 pin)	$V_{IL}1$	V	V_{CC} = 1.8 to 3.7 V	–0.3	—	0.15V_{CC}	2, 3
Input low voltage (2) (Except OSC1 pin)	$V_{IL}2$	V	Vcc=1.8V to 2.4V	-0.3	—	0.15Vcc	2,3
			Vcc=2.4V to 3.7V	-0.3	—	0.2Vcc	2,3
Output high voltage (1) (DB0-17 pins)	V_{OH1}	V	I_{OH} = –0.1 mA	0.75V_{CC}	—	—	2
Output low voltage (1) (DB0-17 pins)	V_{OL1}	V	V_{CC} = 1.8 to 2.4 V, I_{OL} = 0.1 mA	—	—	0.2 V_{CC}	2
			VCC = 2.4 to 3.7 V, I_{OL} = 0.1 mA	—	—	0.15V_{CC}	2
I/O leakage current	I_{Li}	µA	Vin = 0 to V_{CC}	–1	—	1	4
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	µA	R-C oscillation; fosc = 250kHz (240line) V_{CC} = 3.0 V, Ta = 25°C, RAM data 0000h	—	190	300	5,6
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	µA	Vcc = 3V, Ta<=50°C	—	0.1	5	
			Vcc = 3V, Ta>50°C	—	—	20	5
LCD Power Current (DDVDH-GND)	I_{LCD}	µA	Vcc=3V, VLCD=5.5V, VDH=5.0V, CR Oscillation; fosc=250kHz(240line), Ta=25°C, RAMdata:0000h, REV="0", SAP="001", VRN4-0="0", PKP52-00="0", PRP12-00="0", VRN4-0=VRP4-0="0" PKP52-00="0", PRP12-00="0"	—	500	650	5,6
LCD Driving Voltage (DDVDH-GND)	V_{LCD}	V	—	4.5	—	5.5	—
Output Voltage deviation	∠Vo	mV	—	—	5	—	7
Variation of average output voltage	∠V∠	mV	—	—	—	35	8

AC Characteristics

(V_{CC} = 1.7 to 3.7 V, Ta = –40 to +85°C*[1])

Table 69 Clock Characteristics (V_{CC} = 1.8 to 3.7 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	fcp	kHz	V_{CC} = 1.8 to 3.3 V	100	270	600	9
External clock duty ratio	Duty	%	V_{CC} = 1.8 to 3.3 V	45	50	55	9
External clock rise time	trcp	µs	V_{CC} = 1.8 to 3.3 V	—	—	0.2	9
External clock fall time	tfcp	µs	V_{CC} = 1.8 to 3.3 V	—	—	0.2	9
R-C oscillation clock	f_{OSC}	kHz	Rf = TBD V_{CC} = 3 V	244	305	366	10

80-system Bus Interface Timing Characteristics

Table 70 Normal Write Mode (HWM=0) (Vcc = 1.8 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 88	600	—	—
	Read	t_{CYCR}	ns	Figure 88	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 88	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 88	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 88	300	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 88	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 88	—	—	25
Setup time	Write (RS to CS*,WR*)	t_{AS}	ns	Figure 88	0	—	—
	Read (RS to CS*, RD*)				10	—	—
Address hold time		t_{AH}	ns	Figure 88	5	—	—
VLD setup time		t_{VS}	ns	Figure 88	60	—	—
VLD hold time		t_{VH}	ns	Figure 88	15	—	—
Write data set up time		t_{DSW}	ns	Figure 88	60	—	—
Write data hold time		t_{H}	ns	Figure 88	15	—	—
Read data delay time		t_{DDR}	ns	Figure 88	—	—	200
Read data hold time		t_{DHR}	ns	Figure 88	5	—	—

Table 71 High-Speed Write Mode (HWM=1) (Vcc = 1.8 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 88	200	—	—
	Read	t_{CYCR}	ns	Figure 88	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 88	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 88	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 88	90	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 88	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 88	—	—	25
Set up time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 88	0	—	—
	Read (RS to CS*, RD*)				10	—	—
Address hold time		t_{AH}	ns	Figure 88	5	—	—
VLD setup time		t_{VS}	ns	Figure 88	60	—	—
VLD hold time		t_{VH}	ns	Figure 88	15	—	—
Write data set up time		t_{DSW}	ns	Figure 88	60	—	—
Write data hold time		t_{H}	ns	Figure 88	15	—	—
Read data delay time		t_{DDR}	ns	Figure 88	—	—	200
Read data hold time		t_{DHR}	ns	Figure 88	5	—	—

Table 72 Normal Write Mode (HWM=0) (Vcc = 2.4 to 3.7 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 88	250	—	—
	Read	t_{CYCR}	ns	Figure 88	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 88	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 88	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 88	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 88	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 88	—	—	25
Set up time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 88	0	—	—
	Read (RS to CS*, WR*)				10	—	—
Address hold time		t_{AH}	ns	Figure 88	2	—	—
VLD set up time		t_{VS}	ns	Figure 88	25	—	—
VLD hold time		t_{VH}	ns	Figure 88	2	—	—
Write data setup time		t_{DSW}	ns	Figure 88	25	—	—
Write data hold time		t_{H}	ns	Figure 88	2	—	—
Read data delay time		t_{DDR}	ns	Figure 88	—	—	200
Read data hold time		t_{DHR}	ns	Figure 88	5	—	—

Table 73 High-Speed Write Mode (HWM=1) (Vcc = 2.4 to 3.7 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 88	100	—	—
	Read	t_{CYCR}			500	—	—
Write low-level pulse width		PW_{Lw}	ns	Figure 88	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 88	250	—	—
Write high -level pulse width		PW_{HW}	ns	Figure 88	40	—	—
Read high -level pulse width		PW_{HR}	ns	Figure 88	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 88	—	—	—
Set up time	Write (RS to CS*, WR*)	$t_{WRr, WRf}$	ns	Figure 88	0	—	25
	Read (RS to CS*, RD*)				10	—	—
Address hold time		t_{AH}	ns	Figure 88	2	—	—
VLD set-up time		t_{VS}	ns	Figure 88	25	—	—
VLD hold time		t_{VH}	ns	Figure 88	2	—	—
Write data set up time		t_{DSW}	ns	Figure 88	25	—	—
Write data hold time		t_{H}	ns	Figure 88	2	—	—
Read data delay time		t_{DDR}	ns	Figure 88	—	—	200
Read data hold time		t_{DHR}	ns	Figure 88	5	—	—

Clock Synchronized Serial Interface Timing Characteristics

Table 74 (Vcc = 1.8 to 2.4 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	us	Figure 89	0.1	—	20
	Read (transmitted)	t_{SCYC}	us	Figure 89	0.5	—	20
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 89	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 89	230	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 89	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 89	230	—	—
Serial clock rise/fall time		$t_{scr, tscf}$	ns	Figure 89	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 89	20	—	—
Chip select hold time		t_{CH}	ns	Figure 89	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 89	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 89	30	—	—
Serial input data delay time		t_{SOD}	ns	Figure 89	—	—	200
Serial input data hold time		t_{SOH}	ns	Figure 89	5	—	—

Table 75 (Vcc = 2.4 to 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	us	Figure 89	0.1	—	20
	Read (transmitted)	t_{SCYC}	us	Figure 89	0.35	—	20
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 89	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 89	150	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 89	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 89	150	—	—
Serial clock rise/fall time		$t_{scr, scf}$	ns	Figure 89	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 89	20	—	—
Chip select hold time		t_{CH}	ns	Figure 89	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 89	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 89	30	—	—
Serial output data delay time		t_{SOD}	ns	Figure 89	—	—	130
Serial output data hold time		t_{SOH}	ns	Figure 89	5	—	—

Table 76 Reset Timing Characteristics (V_{CC} = 1.8 to 3.7 V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 90	1	—	—
Reset rise time	t_{rRES}	us	Figure 90	—	—	10

RGB interface timing characteristics

Table 77 <<18/16 bit RGB interface (HWM =1), Vcc = 1.8V to 2.4V>>

Item	Symbol	Unit	Timing diagram	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 91	0	—	1
ENABLE Set up time	tENS	ns	Figure 91	20	—	—
ENABLE Hold time	tENH	ns	Figure 91	80	—	—
VLD Set up time	tVLS	ns	Figure 91	20	—	—
VLD Hold time	tVLH	ns	Figure 91	80	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 91	90	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 91	90	—	—
DOTCLK cycle time	tCYCD	ns	Figure 91	200	—	—
Data Set up time	tPDS	ns	Figure 91	20	—	—
Data Hole time	tPDH	ns	Figure 91	80	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 91	—	—	25

Table 78 <<18/16 bit RGB interface (HWM = 1), Vcc = 2.4V to 3.7 V>>

Item	Symbol	Unit	Timing diagram	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 91	0	—	1
ENABLE Set up time	tENS	ns	Figure 91	10	—	—
ENABLE Hold time	tENH	ns	Figure 91	20	—	—
VLD Set up time	tVLS	ns	Figure 91	10	—	—
VLD Hold time	tVLH	ns	Figure 91	40	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 91	40	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 91	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 91	100	—	—
Data Set up time	tPDS	ns	Figure 91	10	—	—
Data Hole time	tPDH	ns	Figure 91	40	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 91	—	—	25

Table 79 <<6 bit RGB interface (HWM = 1), Vcc = 1.8V to 2.4 V>>

Item	Symbol	Unit	Timing diagram	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 91	0	—	1
ENABLE Set up time	tENS	ns	Figure 91	20	—	—
ENABLE Hold time	tENH	ns	Figure 91	50	—	—
VLD Set up time	tVLS	ns	Figure 91	20	—	—
VLD Hold time	tVLH	ns	Figure 91	65	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 91	50	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 91	50	—	—
DOTCLK cycle time	tCYCD	ns	Figure 91	120	—	—
Data Set up time	tPDS	ns	Figure 91	20	—	—
Data Hold time	tPDH	ns	Figure 91	65	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 91	—	—	25

Table 80 <<6 bit RGB interface (HWM = 1), Vcc = 2.4V to 3.3 V>>

Item		Symbol	Unit	Timing diagram	min.	typ.	max.
VSYNC/HSYNC Set up time		tSYNCS	clock	Figure 91	0	—	1
ENABLE Set up time		tENS	ns	Figure 91	10	—	—
ENABLE Hold time		tENH	ns	Figure 91	20	—	—
VLD Set up time		tVLS	ns	Figure 91	10	—	—
VLD Hold time	Vcc=2,4 to2,7V	tVLH	ns	Figure 91	40	—	—
	Vcc=2,7 to 3,7V	tVLH	ns	Figure 91	30	—	—
DOTCLK “Low” Level pulse width		PWDL	ns	Figure 91	30	—	—
DOTCLK “High” Level pulse width		PWDH	ns	Figure 91	30	—	—
DOTCLK cycle time		tCYCD	ns	Figure 91	70	—	—
Data Set up time		tPDS	ns	Figure 91	10	—	—
Data Hole time	Vcc=2,4 to 2,7V	tPDH	ns	Figure 91	40	—	—
	Vcc=2,7 to 3,7V	tPDH	ns	Figure 91	30	—	—
DOTCLK, VSYNC, HSYNC rising and falling time		trgbr, trgbf	ns	Figure 91	—	—	25

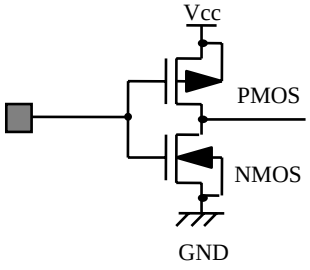
Table 81 LCD driver output

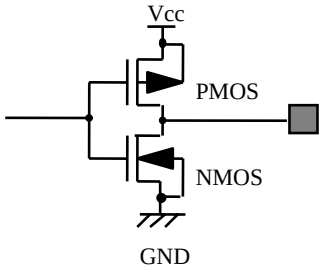
Item	Sign	Unit	Condition for measure	min.	typ.	max.	Note
Delay time of driver output	tdd	µs	Vcc=3V, VLCD=5.5V, VDH=5.0V, CR oscillation ;fosc=270kHz(240 lines), Ta=25°C、REV="0", SAP="001", VRN4-0="0",VRP4-0="0"	—	40	—	(11)

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85°C.

2. The following three circuits are I pin, I/O pin, O pin configurations.





Pins: DB15 -DB2,
DB1/SD0. DB0/SD1

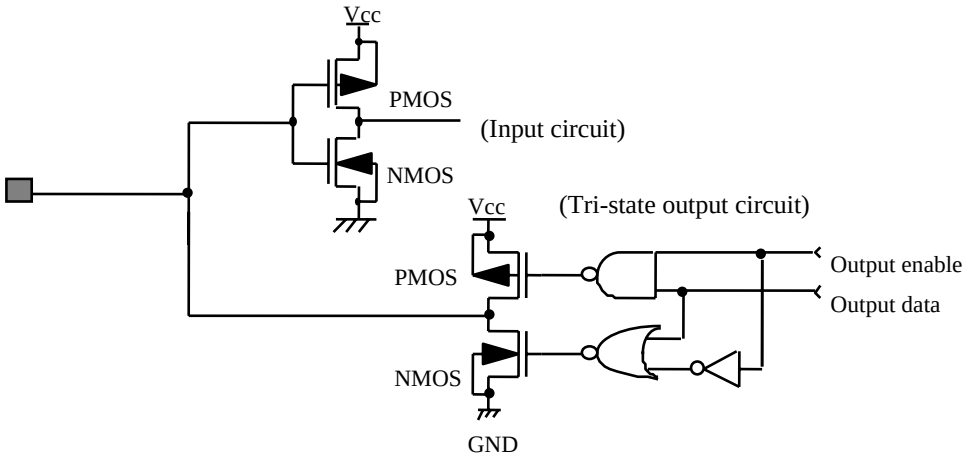


Figure 83 I/O Pin Configuration

3. The TEST pin must be grounded and the IM2/1 and IM0/ID pins must be grounded or connected to Vcc.

4. Applies to the resistor value (RSEG) between VSH, GND pins and segment signal pins.

5. This excludes the current flowing through output drive MOSs.

6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.

7. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure).

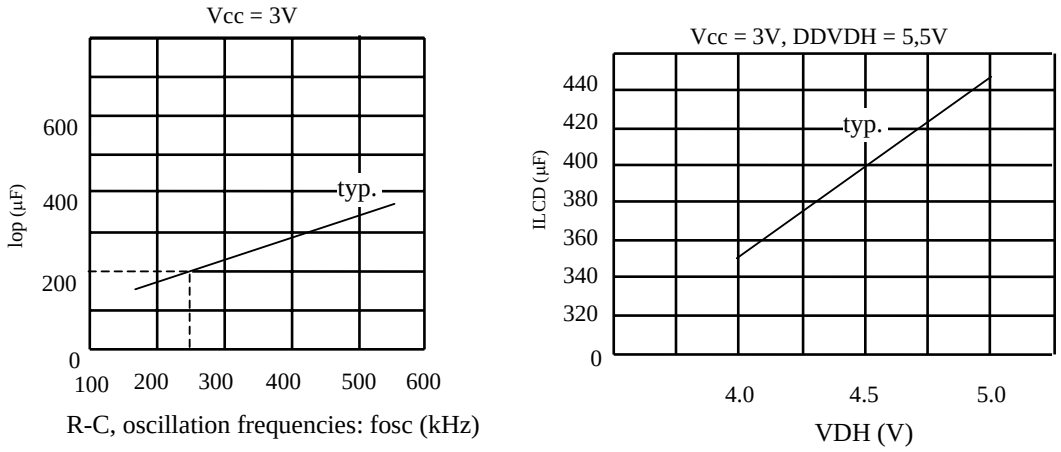


Figure 84 Relationship between the Operation Frequency and Current Consumption

8. Each SEG output voltage is within ±0.15 V of the LCD voltage (VSH, GND) when there is no load.

9. Applies to the external clock input (figure).

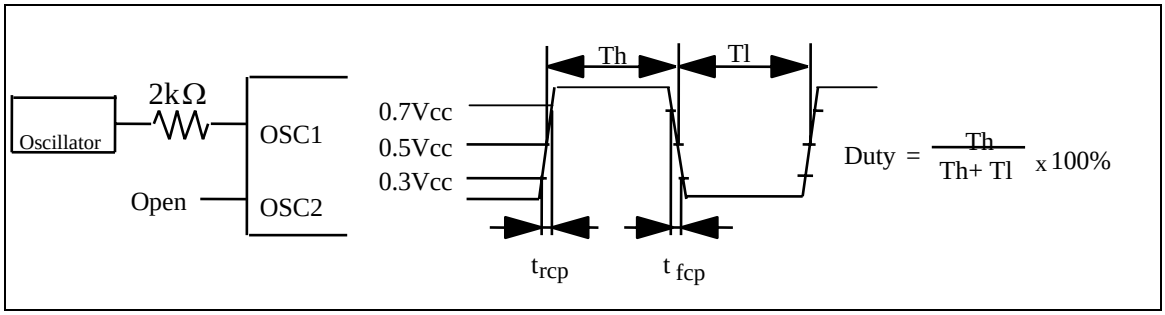
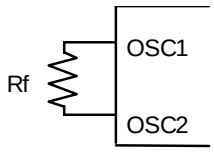


Figure 85 External Clock Supply

10. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).



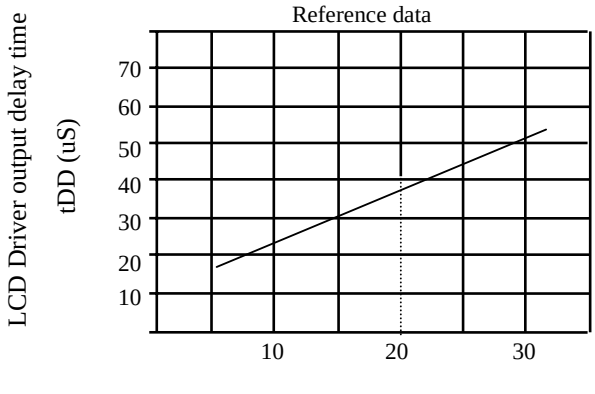
Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 86 Internal Oscillation

Table 82 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance	R-C Oscillation Frequency: fosc				
(Rf)	Vcc = 1.8 V	Vcc = 2 V	Vcc = 2.4 V	Vcc = 3 V	Vcc = 3.3 V
110 kΩ	299	333	372	401	411
150 kΩ	234	258	284	305	311
180 kΩ	202	222	243	258	263
200 kΩ	186	203	222	235	240
240 kΩ	160	173	188	198	202
270 kΩ	145	157	169	177	181
300 kΩ	132	143	153	161	163
390 kΩ	106	113	121	126	128
430 kΩ	97	104	110	115	116

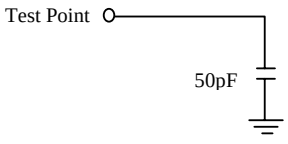
11. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).



Vcc =3V, VLCD = 5.5V, VDH = 5.0V, CR Oscillation; fosc = 270kHz (240line), Ta = 25°C, REV = “0”, SAP =”001”, VRN4-0 = “0”, VRP4-0 = “0”, PKP52-00 = “0”, PRP12-00 = “0”, All pins chnge at the same time from same grayscale. The time till output level reaches ±35v when VCOM polarity changes. Load resistance R = 10k/pin

AC characteristic measuring load circuit

Data bus: DB17-DB0, PD17-0



LCD driver output characteristic measuring load circuit

LCD output: S1- S528

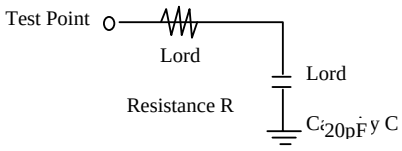
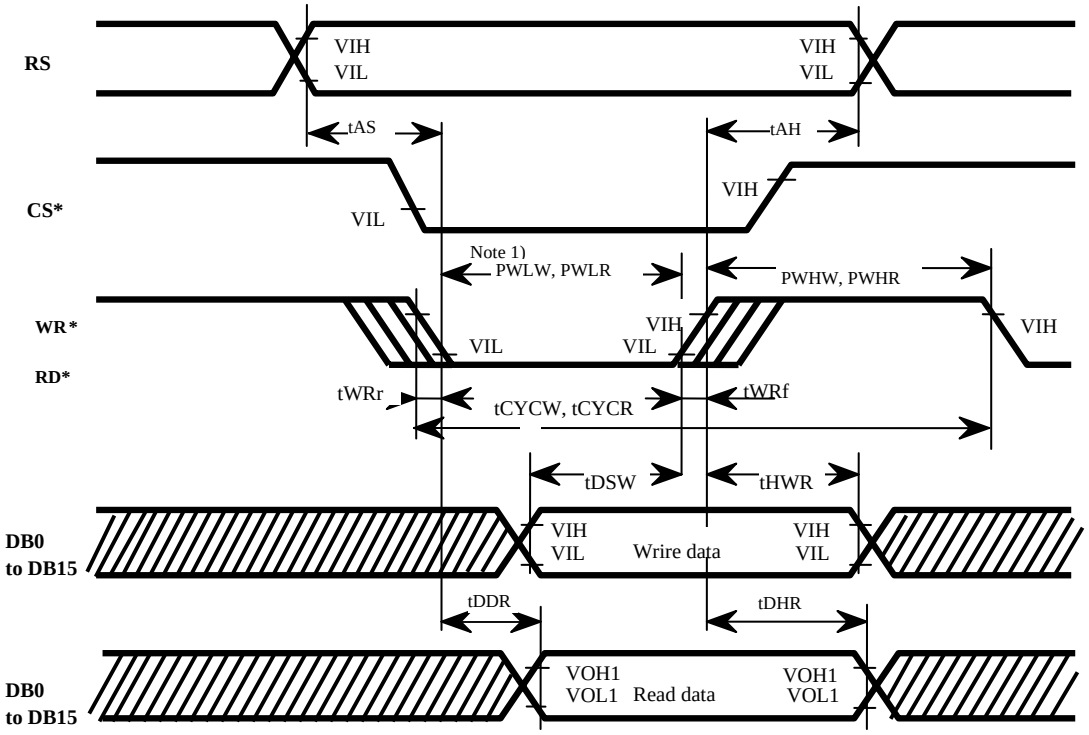


Figure 87 Test circuit

80-system Bus Operation



Note 1) PWLW and PWLR is specified in the overlapped period when CS* is low and WR* or RD* is low.

Note 2) Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used. Fix the DB7-0 pins to Vcc or GND.

Figure 88 80-system Interface Timing

Clock Synchronized Serial Interface Operation

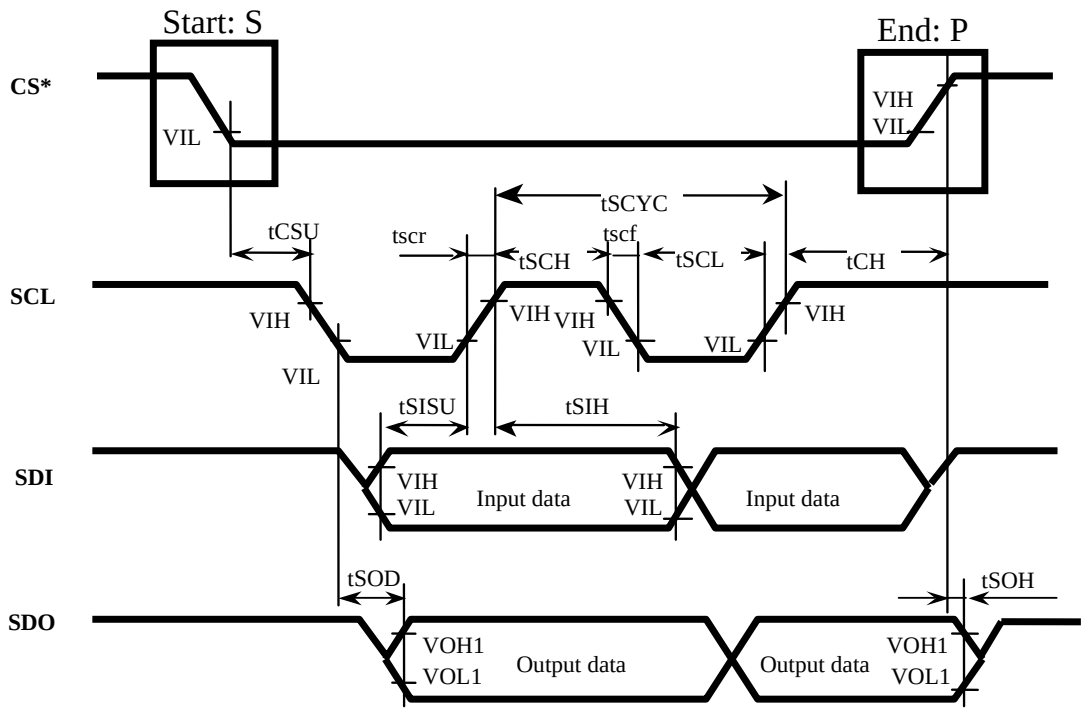


Figure 89 Clock Synchronized Serial Interface Timing

Reset operation

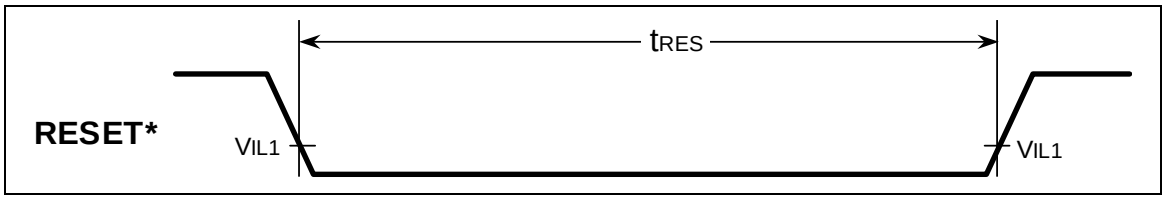


Figure 90 Reset Timing

RGB I/F Operation

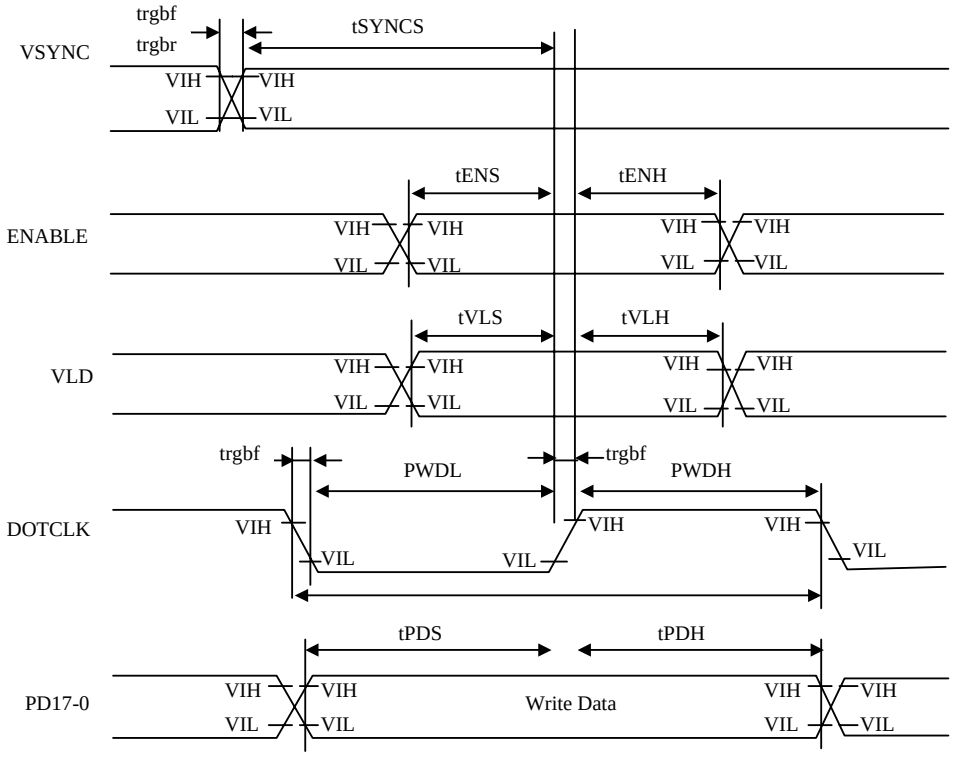


Figure 91 RGB I/F Timing

LCD driver output

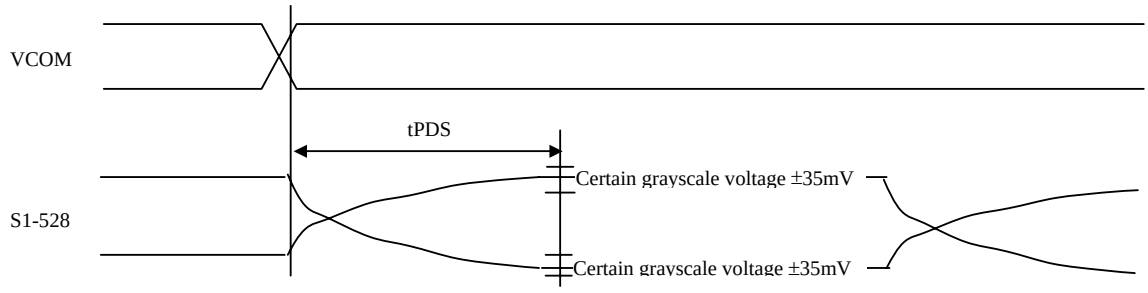


Figure 92 LCD output Timing

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Colophon 0.0

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.1-3	2003.10.14	First issue		