디지털논리회로 2 담당교수: 이준환, 공영호
(컴퓨터정보공학부)

2021 년 2 학기 중간고사

중간고사

"꿈을 가지십시오, 그리고 정열적이고 명예롭게 이루십시오."
2021 년 10 월 25 일 (월) 18:00 ~ 19:30

Honor code (명예 서약)

- 공학도는 학생으로서 그리고 전문가로서 개인의 품위를 지켜야 합니다.
- 공학도는 안전과 건강과 공평성을 수호할 수 있는 명예로운 사람들입니다.
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- 숙제나 설계과제는 모두 "scratch" 부터 작성하십시오. 즉, 다른 사람 (web 포함)의 결과나 이전 학기 수업결과를 copy 하거나 그 변형을 제출하는 것은 명예서약 위반 입니다. 여러분이 제출한 숙제나 과제결과는 모든 부분을 여러분이 설명할 수 있어 야 하고 재생성 할 수 있어야 합니다.
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본인은 위 명예서약을 준수하고 본 시험을 자신의 온전한 지식으로 답하였음을 서약합니다.

이름: (서명)
학번:
학과:

필독:
답안을 서술식으로 작성할 경우, 주어와 술어를 명확히, 그리고 가능하면 전문용어를 사용하여 작성하여야 좋은 답안입니다. 무슨 이야기를 하려는 것인지 짐작할 수 있더라도, 문장 자체의 뜻이 명확하지 않을 경우, 감점될 수 있습니다.

- You should present explanation (or procedure) for all the questions except Question 1.
(1번문제를 제외하고, 서술형으로 작성하여야만 점수를 얻을 수 있습니다. 단답형으로 작성 시 0점)

- For Question 1, you will get +1 point for each correct answer but you will get -1 point for each wrong answer. If you just remain blank (not T nor F), you will get no point (0 point) (1번문제는 맞으면 +1점, 틀리면 -1점, 비워두면 0점입니다.)

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1. **(5점, 각 문항당 1점)** Write T (TRUE) if the statement is correct, otherwise write F (FALSE) **(Point: +1 (correct) or 0 (blank) or -1 point (incorrect))**

   (i) The delay of Ripple Carry Adder (RCA) is always slower than that of Carry Look Ahead Adder (CLA). **(T or F)**

   (ii) The `always` block should be used with `posedge` or `negedge` (i.e., clock signal). **(T or F)**

   (iii) A finite state machine (FSM) design consists of combinational and sequential circuits. **(T or F)**

   (iv) When a logic circuit satisfies setup time constraints, the logic circuit could operate correctly. **(T or F)**

   (v) Binary encoding requires fewer flipflops than one-hot encoding. **(T or F)**

2. **(15점, 각 문항당 3점)** Fill the blank

   (i) Setup time is defined as the minimum amount of time [_____] the clock's active edge that data must be stable.

   (ii) In Verilog, [_____] command is used to read data from the file in hexadecimal

   (iii) The left-hand side of a statement in an always block must be a [ ].

   (iv) [ ] time violation occurs because the path delay from a flipflop output to a flipflop input is too short.

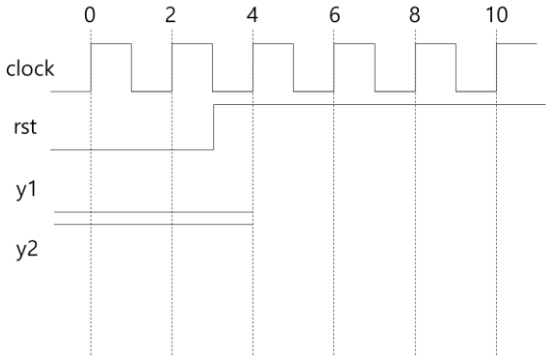
   (v) A 16-bit binary number 1100101011111110 is same as [ ] in hexadecimal.

3. **(총 15점)**

   (1) **(5점)** Complete the timing diagram of the following Verilog code.

```
module P3 (y1, y2, clk, rst);
    output y1, y2;
    input clk, rst;
    reg y1, y2;

    always @(posedge clk or negedge rst) begin
        if (~rst) begin
            y1 = 0;
            y2 = 1;
        end
        else begin
            y1 = y2;
            y2 = y1;
        end
    end
endmodule
```



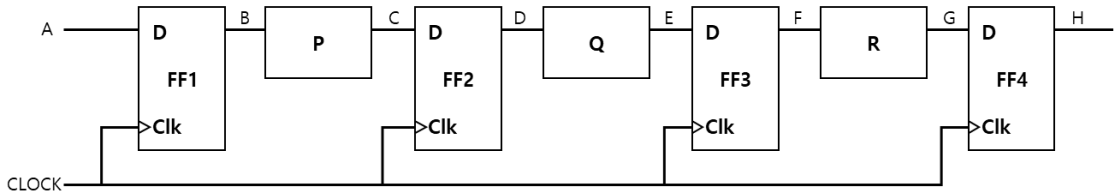
   (2) **(10점)** When all the equal (=) signs are changed into (<=) in the above Verilog code, how's the timing diagram changed? Provide reasons for your answer.

4. **(15점)** Assume an arithmetic logic unit (ALU) with two 32-bit input values (i.e., A[31:0] and B[31:0]) and 3-bit opcode to support addition, subtraction, and logic operations (i.e., AND, OR, NOT A, NOT B, XOR, XNOR). The outputs of the ALU are a 32-bit result 'RESULT[31:0]', 32-bit carry out 'CO[31:0]' and a set of flags (C,N,Z,V) depending on the result.

   (1) **(5점)** Write logic equations of C, N, Z ,V flags, using only AND, OR, NOT, and XOR gates with RESULT[31:0] and CO[31:0].

   (2) **(10점)** Explain how we can use the ALU for comparison of two values: i.e., A<B, A=B, or A>B.

5. **(20점)** The following circuit is with four flipflops (FF1, FF2, FF3, and FF4) and three combinational modules (P, Q, R).



Assumptions: all the flipflops are rising-edge triggered. The timing constraints for the circuit is as follows.

i) Each flipflop requires 1ns to obtain a valid output after a clock transition (i.e., clock-to-output (tCO) delay).

ii) The setup time of each flipflop is 2ns.

iii) The propagation delays of P, Q, and R are in the range of 2~3ns, 3~5ns, 3~4ns respectively.

(20점) Derive the maximum operating frequency of the circuit.

6. **(10점)** A circuit with a 3-bit unsigned input X[2:0] and a 3-bit unsigned output Y[2:0] is required to perform a decoding function as described by the following pseudo-code:

```
if X < 3
    Y = X
else if X < 5
    Y = X + 3
else
    Y = X – 1
```

Write a Verilog code for the decoder circuit with the following interface declarations.

(Note: you should use ‘case’ statement. ‘if-else’ statement is not allowed. The default output value is 3’bX)

```
module decoder(X,Y);
    input [2:0] X;
    output [2:0] Y;
```

7. **(25점)** A 3-way up-down counter behaves as follows.

- The counter counts 0,1,2,0,1,2,0 … and so on only when the signal UP is high.
- The counter counts 2,1,0,2,1,0,2, … and so on only when the signal UP is low and the signal DN is high.
- UP and DN signals cannot be high at the same time.
- When both UP and DN signals are low, the counter remains the current state.
- When reset_n signal is low, the counter becomes 0 (initial state).

(1) **(10점)** Design a state transition diagram for this counter.

(2) **(15점)** Write a Verilog code for this 3-way up-down counter according to the guidelines given in class.

8. **(15점)** You are designing a 16-bit adder between flip-flops operating with the clock frequency of 500MHz. In this case, which is the better design between the 16-bit ripple carry adder and the 16-bit carry look ahead adder designs? Compare the worst-case delay of a 16-bit ripple-carry adder and a 16-bit carry look ahead adder with 4-bit blocks. Assume that each two-input gate delay is 50 ps and that a full adder t_{FA} delay is 150 ps.