Frequency Shift Keying (FSK)

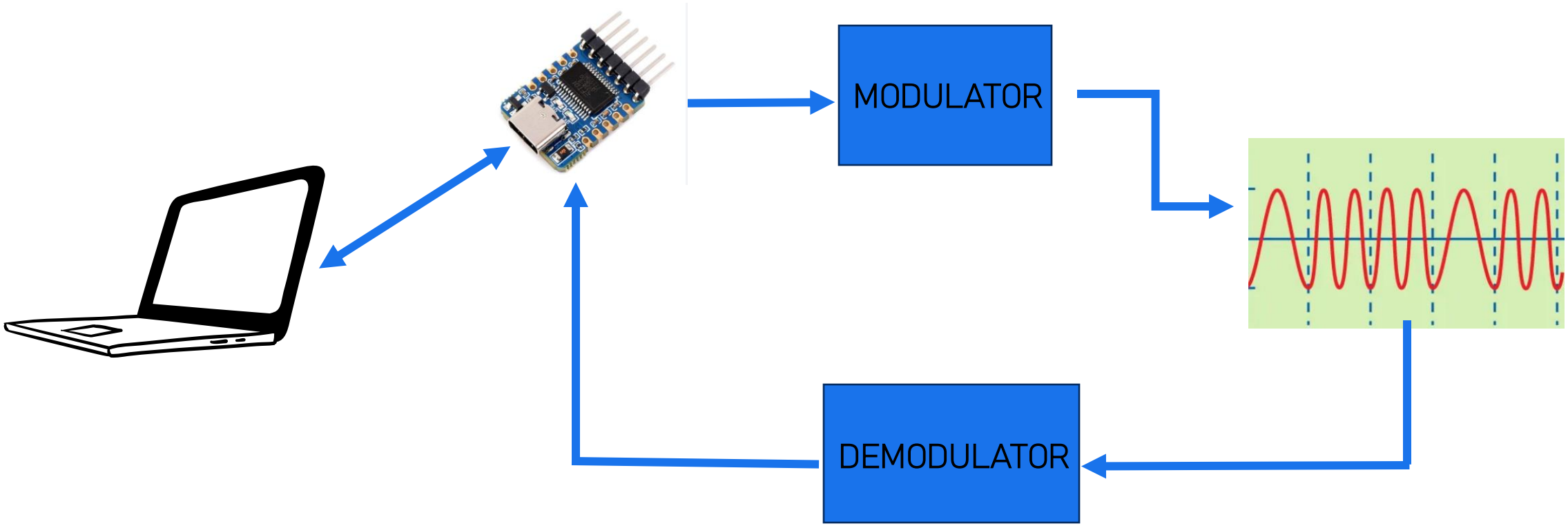
DUNCAN WOOD

ENCE 4110

11/12/2025

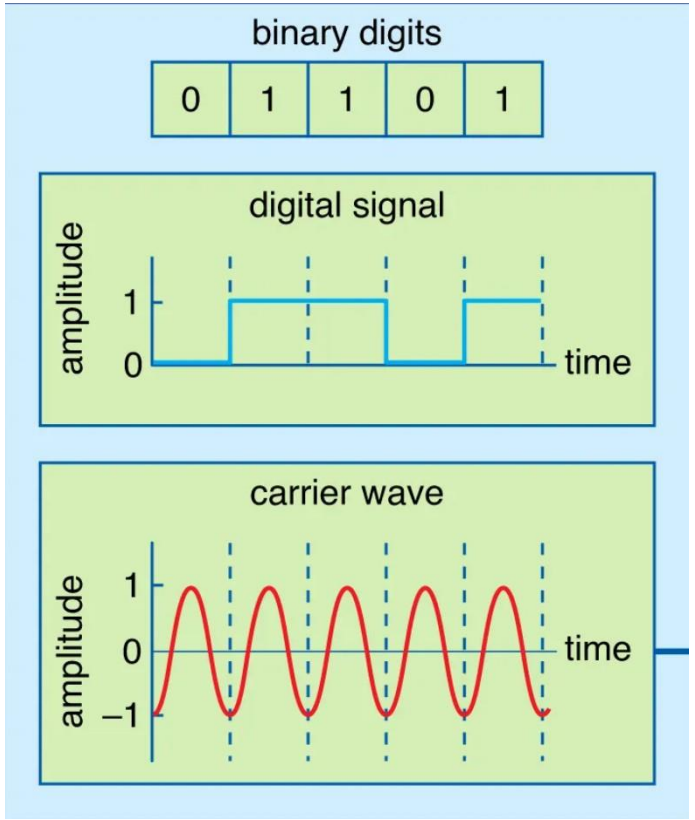
Introduction

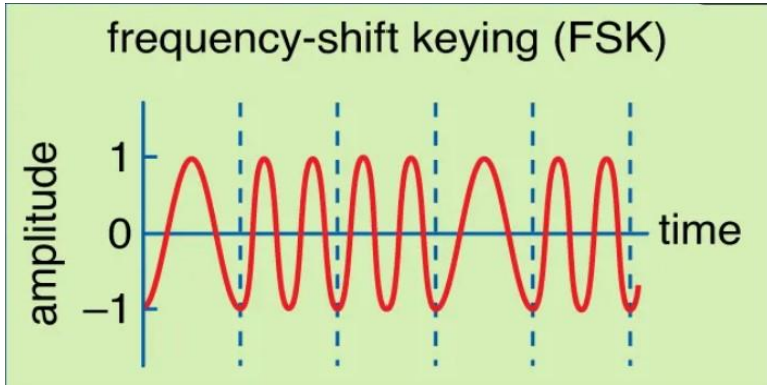
Problem: Convert UART data into modulated FSK signal and send it back to the PC demodulated



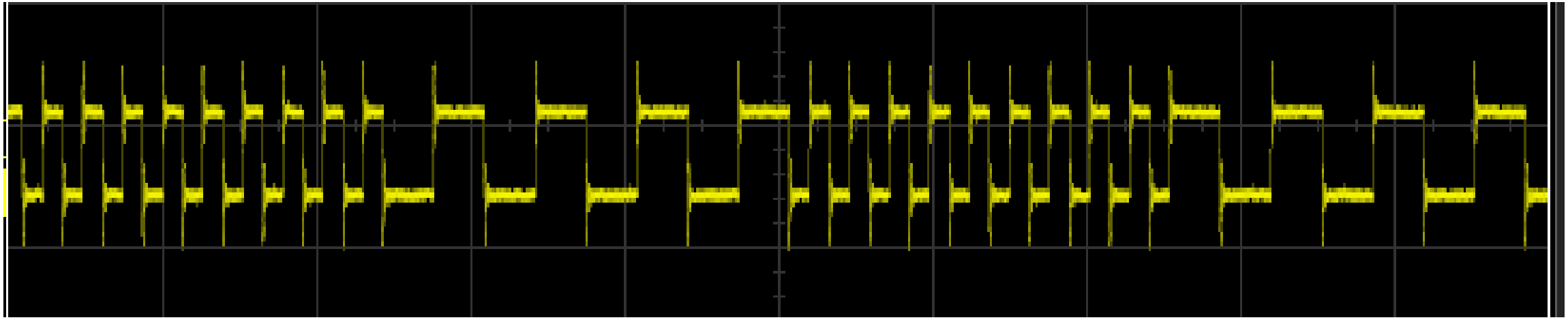
What is Frequency Shift Keying?

- FSK is a digital modulation technique widely used in modern technology.
- Bluetooth, digital radios, remotes.
- The digital counterpart of Frequency Modulation (FM)

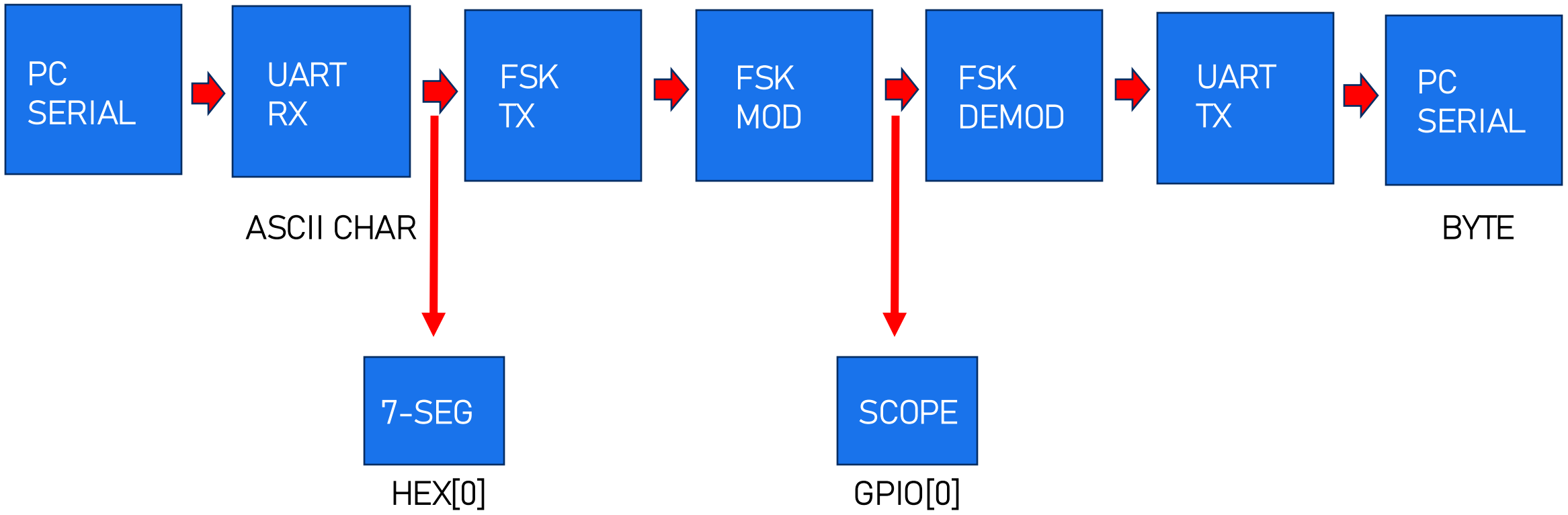




In this system...

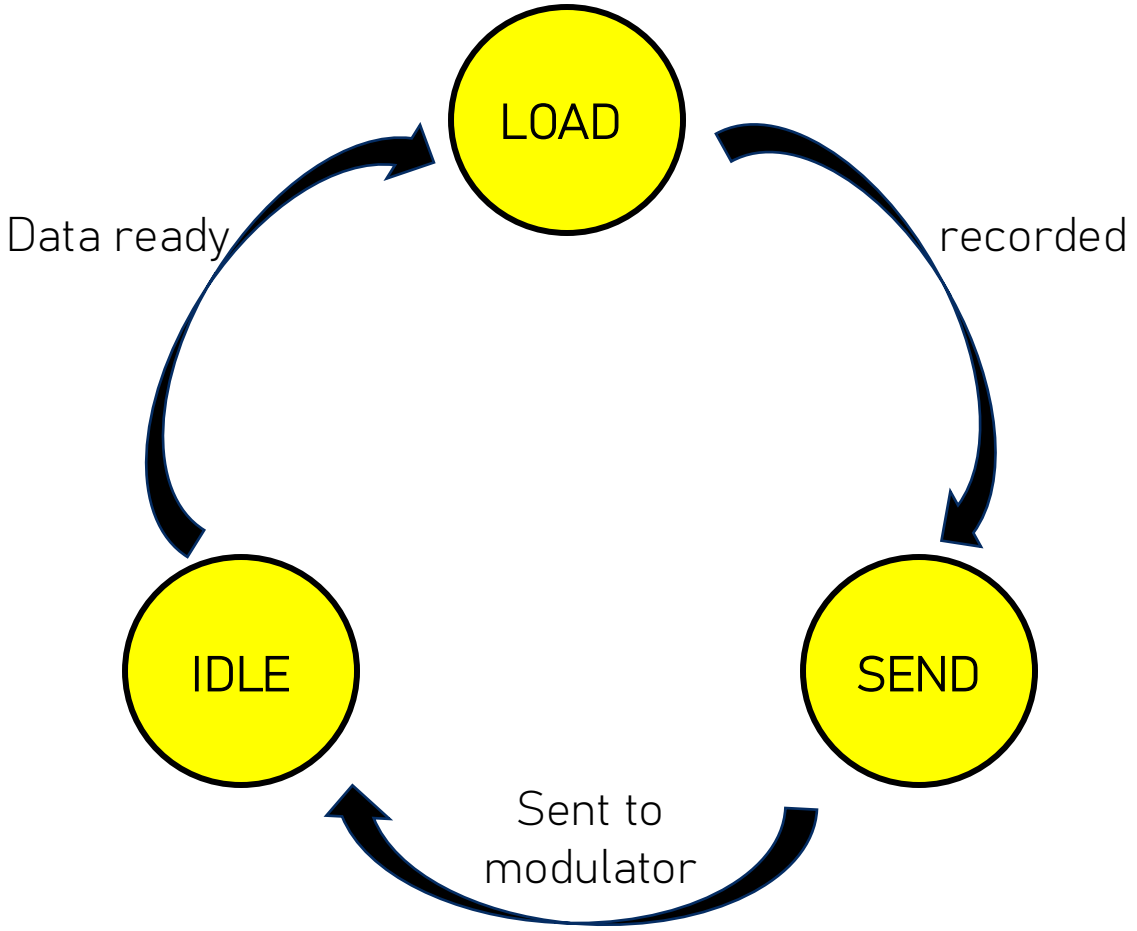


System Overview



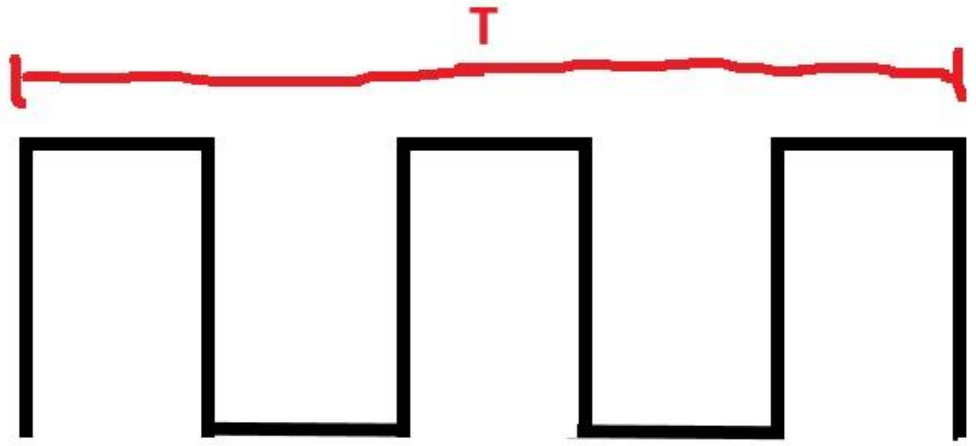
FSK Transmit FSM

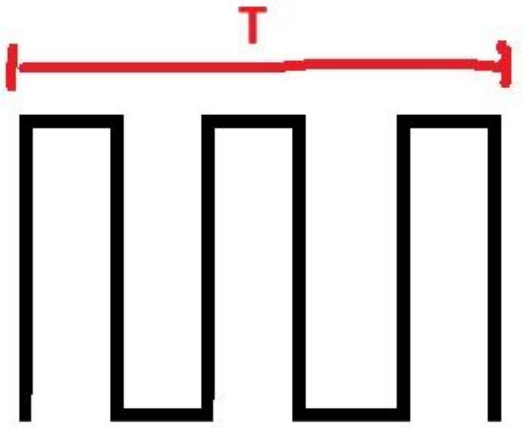
- Serializes byte into 10-bit frame (start, data, stop)
- Holds each bit for defined number of clock cycles; the symbol period.
- Synchronizes the UART data with the FSK modulator.



Symbol Timing

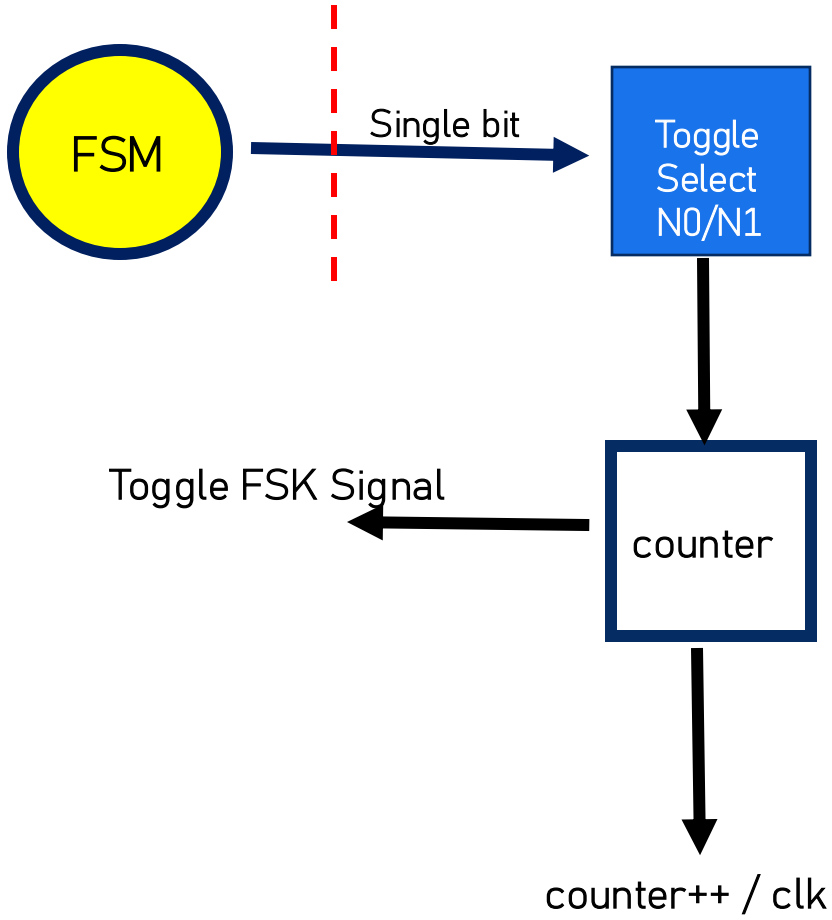
- UART Baud: 115200
- FPGA Clock: 50 MHz
- Clocks per symbol = 50e6 / 115200 ≈ 434
- One bit = 434 clock cycles → one full tone interval





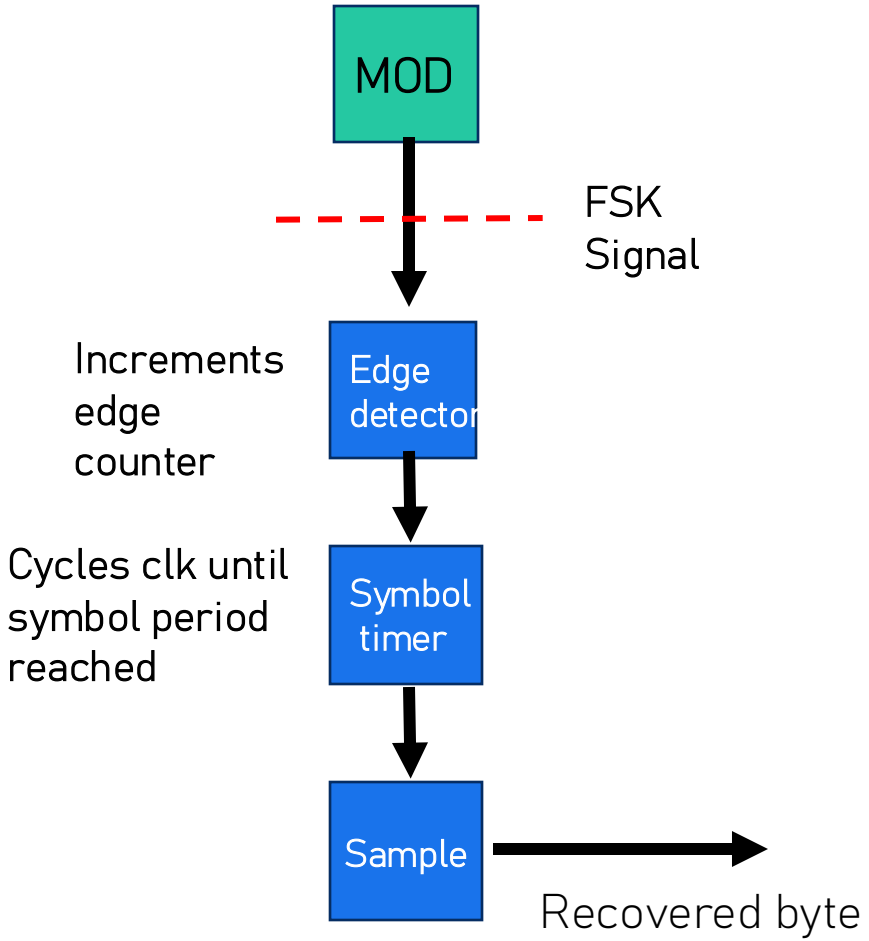
FSK Modulator

- Simple toggle-counter structure:
  - Counter resets when reaching N_0/N_1
  - Output bit flips on reset → square wave
- Frequency
  - f=1/(2xN)
  - If bit==1 use **N1** (shorter interval → higher frequency).
  - If bit==0 use **N0** (longer interval → lower frequency).



FSK Demodulator

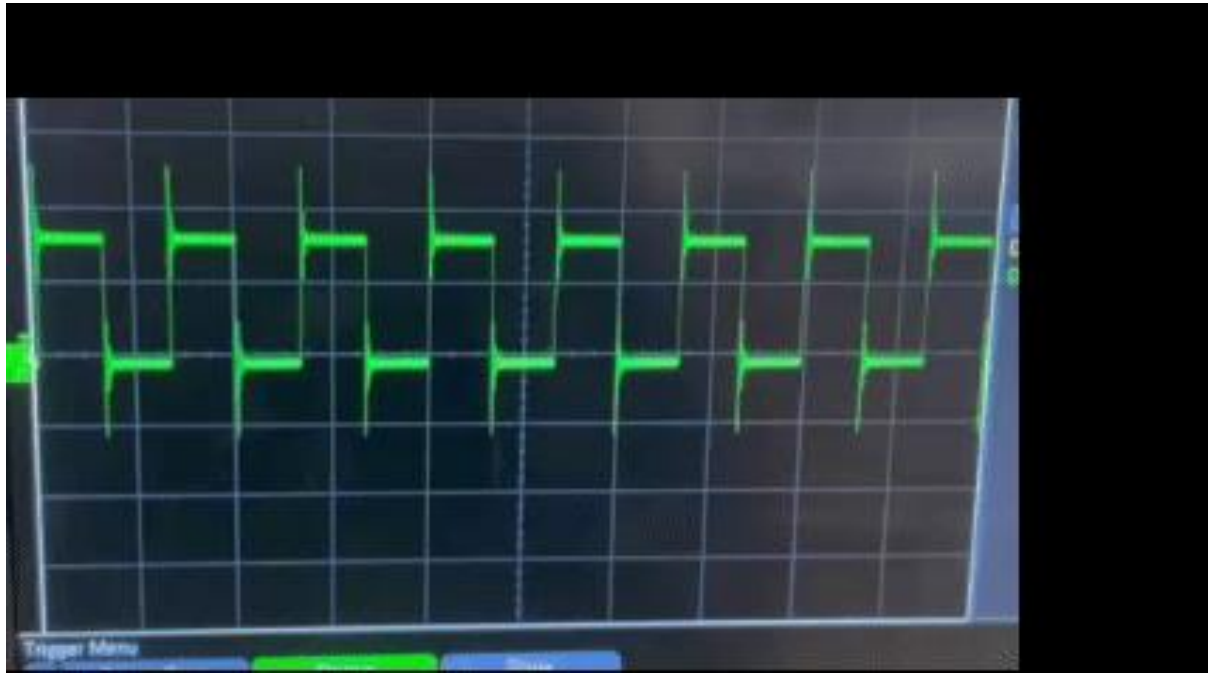
- Edge-counting demodulator:
  - Detect transitions of **`fsk_in`**
  - Count edges per symbol window (434 clocks)
  - Compare to threshold (~20 edges)
- Decision rule:
  - More edges → high tone → bit = 1
  - Fewer edges → low tone → bit = 0
- Reassemble bits into bytes

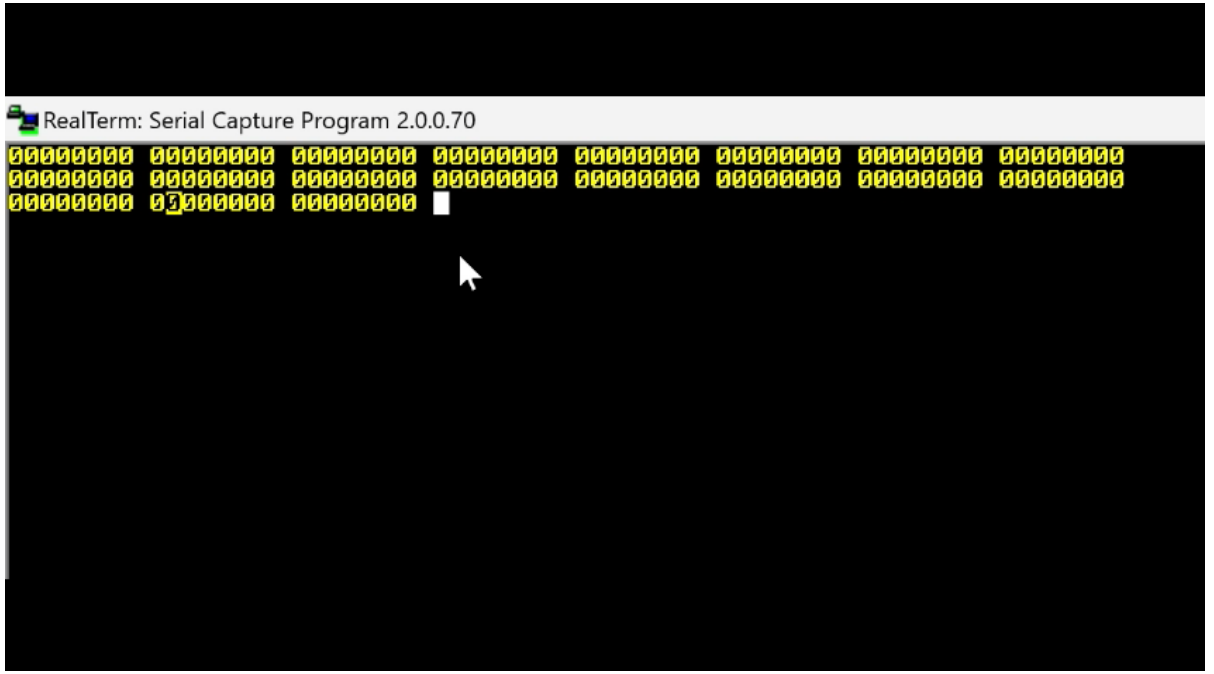


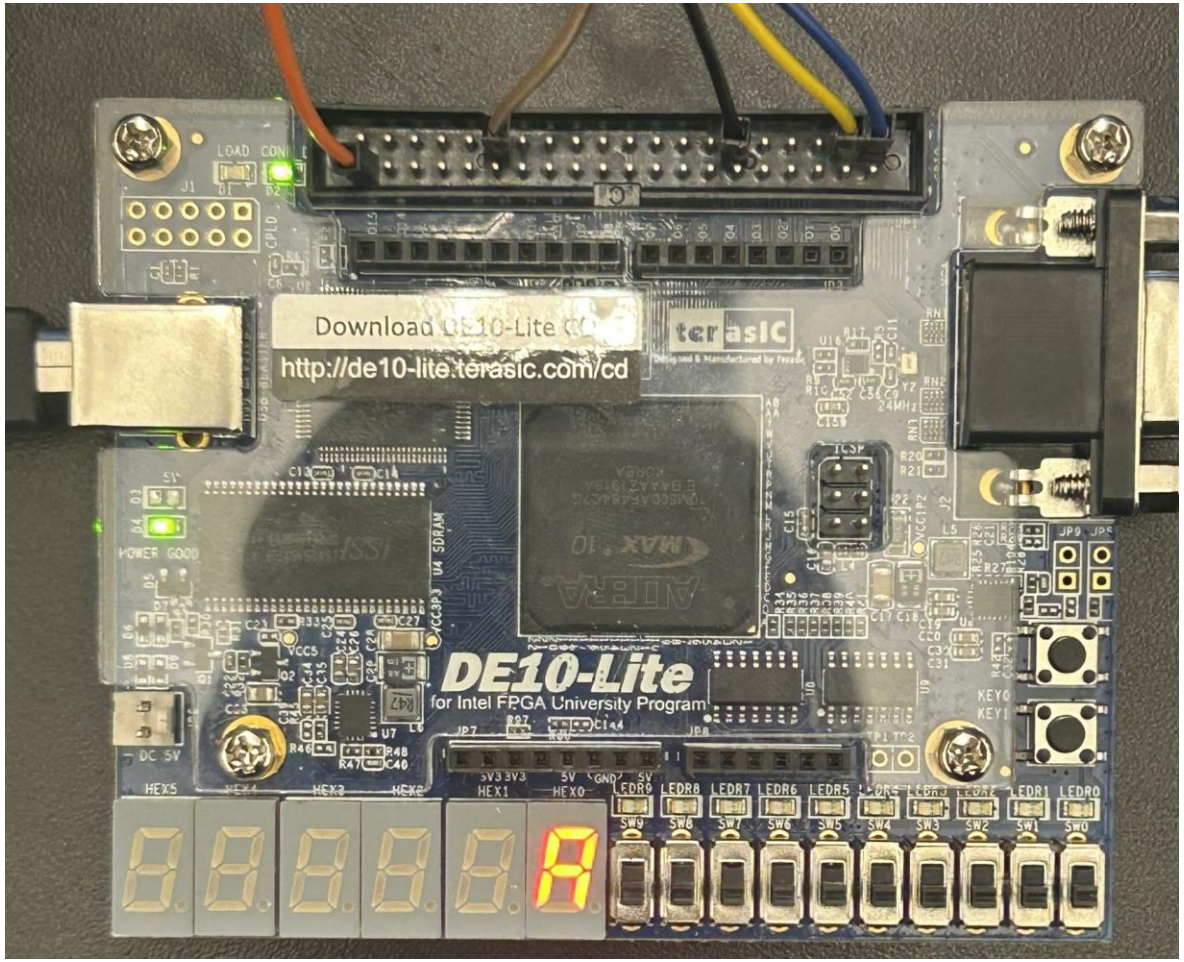
UART Transmitter / Receiver

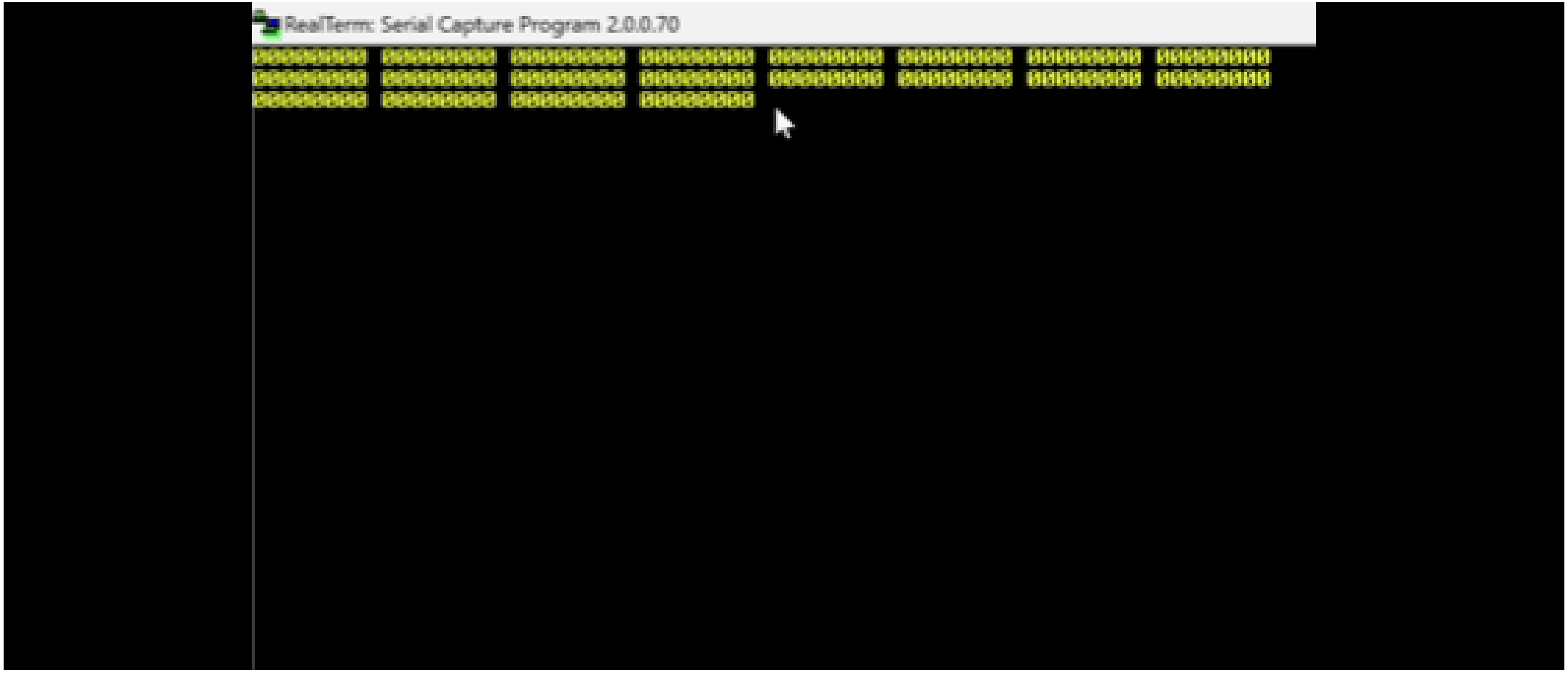
- Receive and transmit the input and output message of the FSK logic.

Testing and Verification






Download DE10-Lite CD
http://de10-lite.terasic.com/cd
terasIC
DE10-Lite
for Intel FPGA University Program


RealTerm: Serial Capture Program 2.0.0.70

Future Work

Problem Observed

- Characters echoed from the demodulator do not match the UART key pressed
- Indicates bit or symbol misalignment between transmitter and receiver timing.

Likely causes

- **Symbol boundary drift** — demodulator's 434-clock window may start mid-symbol
- **Threshold sensitivity** — fixed midpoint (≈ 20 edges) may mis-classify noisy or marginal tones.
- **Byte framing ambiguity** — demodulator doesn't yet detect start/stop bits; it simply groups 8 bits sequentially.

Possible Solution: add protocol layer and additional synchronizer to implement start/stop validation.

Conclusions

- Built a complete digital FSK modem on FPGA.
- .Demonstrated real-time chain:
  - UART RX → FSK TX FSM → Modulator → Demodulator → UART TX

Key Insights

- Timing precision is key for symbol alignment
- Simple edge count demodulation works conceptually but lacks robustness.