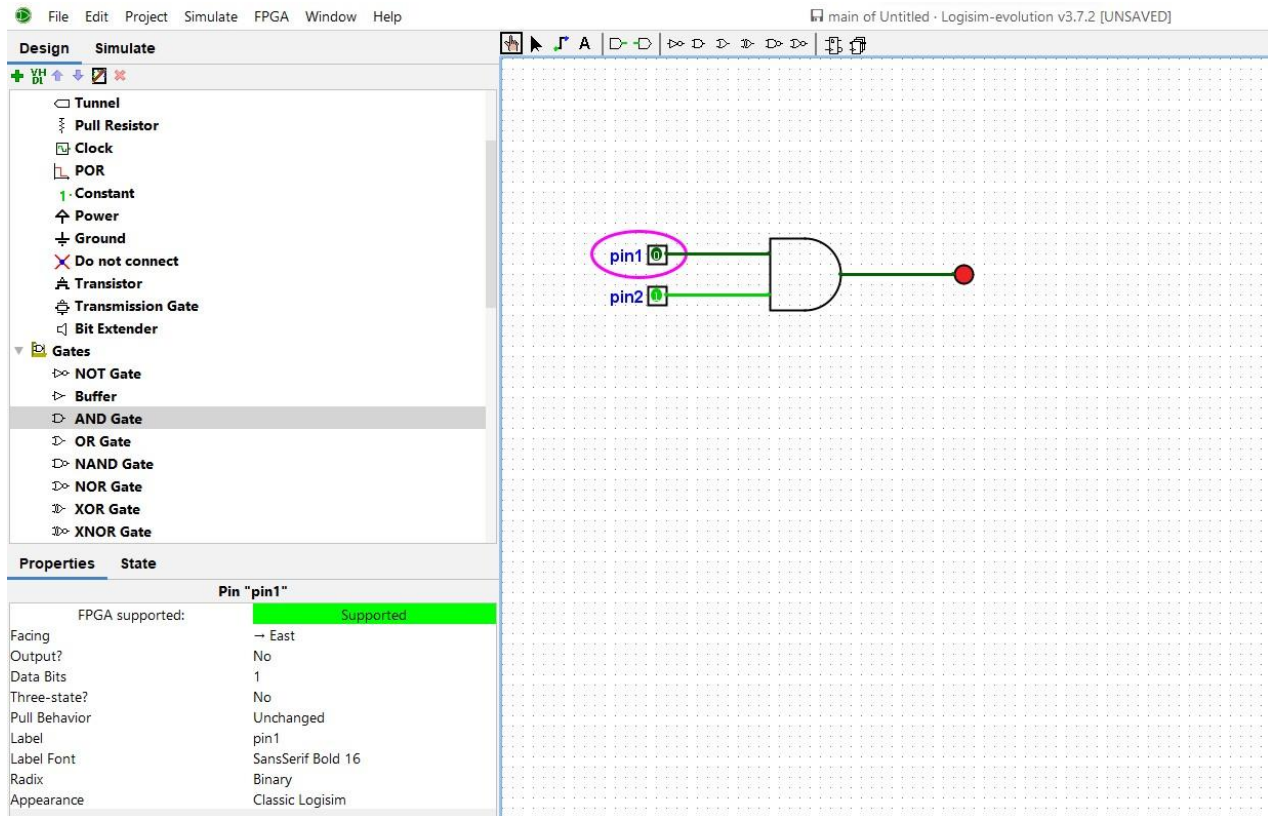


COS10004: Computer Systems

Lab 1

Name: SWH00420 Tran Quoc Dung

Student ID: 103803891



Circuit 1

File Edit Project Simulate FPGA Window Help

main of Circuit2 - Logisim-evolution v3.7.2

Design Simulate

Circuit...

- main
 - Wiring
 - Gates
 - Plexers
 - Arithmetic
 - Memory
 - Input/Output
 - TTL
 - TCL
 - BFH mega functions
 - Input/Output Extra
 - System On a Chip

pin y 0

1

Pin y	Output
0	1
1	0

Circuit 2

File Edit Project Simulate FPGA Window Help

main of Circuit3 - Logisim-evolution v3.7.2

Design Simulate

Circuit...

- main
 - Wiring
 - Gates
 - Plexers
 - Arithmetic
 - Memory
 - Input/Output
 - TTL
 - TCL
 - BFH mega functions
 - Input/Output Extra
 - System On a Chip

0 0

1

Properties State

Pin (180,200)

FPGA supported: Supported

Facing → East

Output? No

Data Bits 1

Three-state? No

Pull Behavior Unchanged

Label HDL Required

Label Font SansSerif Bold 16

Radix Binary

Appearance Classic Logisim

Pin 1	Pin 2	Output
0	0	1
0	1	1
1	0	1
1	1	0

Circuit 3

File Edit Project Simulate FPGA Window Help

main of Circuit4 · Logisim-evolution v3.7.2 [UNSAVED]

Design Simulate

+ VH ↓ ↑ ×

- *Circuit4
 - main
 - Wiring
 - Gates
 - Plexers
 - Arithmetic
 - Memory
 - Input/Output
 - TTL
 - TCL
 - BFH mega functions
 - Input/Output Extra
 - System On a Chip

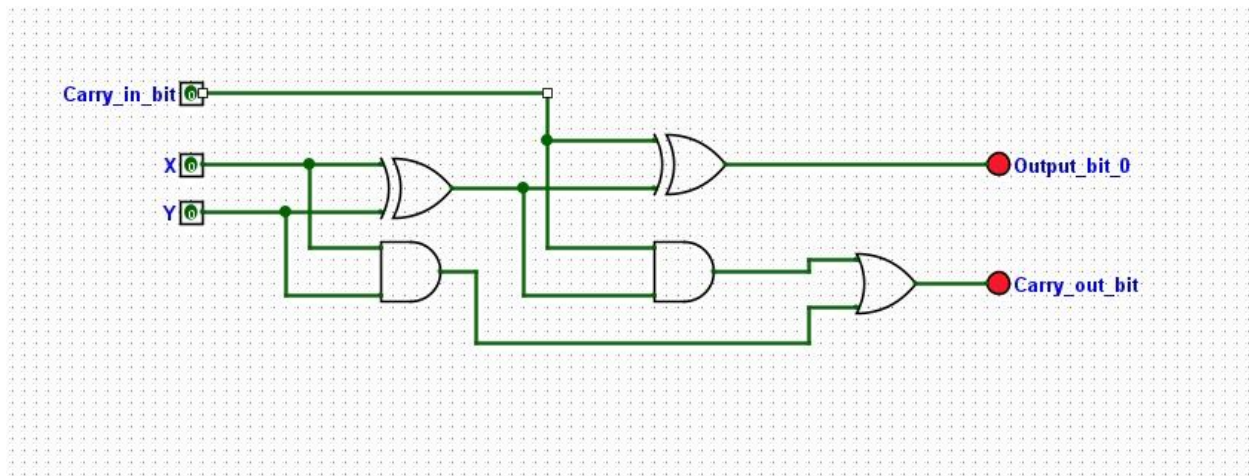
Properties State

Pin "X"

FPGA supported:	Supported
Facing	→ East
Output?	No
Data Bits	1
Three-state?	No
Pull Behavior	Unchanged
Label	X
Label Font	SansSerif Bold 16
Radix	Binary
Appearance	Classic Logisim

Pin 1	Pin 2	Sum Output	Carry Output
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Circuit 4



Input 1	Input 2	Carry In	Sum Output	Carry Output
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Circuit 5