Half Adder

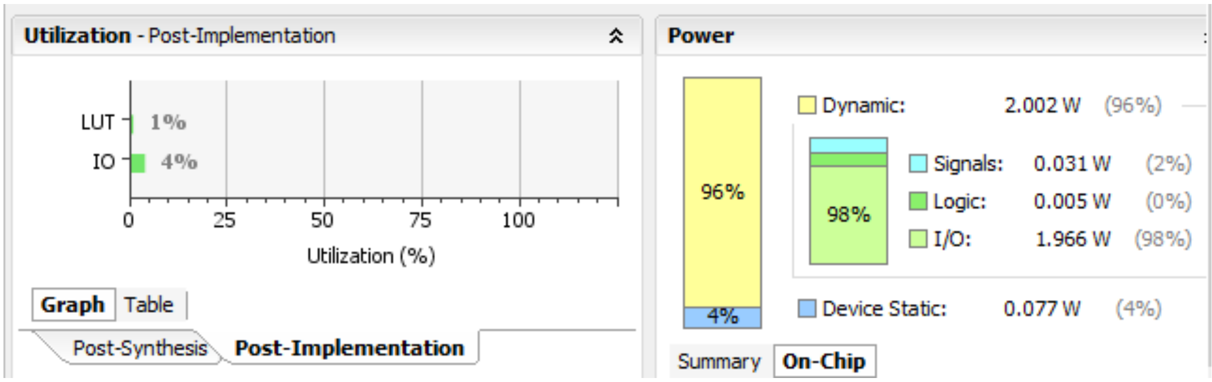
CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity half_adder is
    Port ( a : in STD_LOGIC;
           b : in STD_LOGIC;
           sum : out STD_LOGIC;
           carry : out STD_LOGIC);
end half_adder;

architecture Behavioral of half_adder is

begin
sum<=a xor b;
carry<=a and b;


end Behavioral;
```

PIN LOCK :

```
set_property PACKAGE_PIN R2 [get_ports a]
set_property PACKAGE_PIN T1 [get_ports b]
set_property PACKAGE_PIN U16 [get_ports carry]
set_property PACKAGE_PIN E19 [get_ports sum]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports carry]
set_property IOSTANDARD LVCMOS33 [get_ports sum]
```

POWER CONSUMPTION:



Dynamic: 2.002 W (96%)

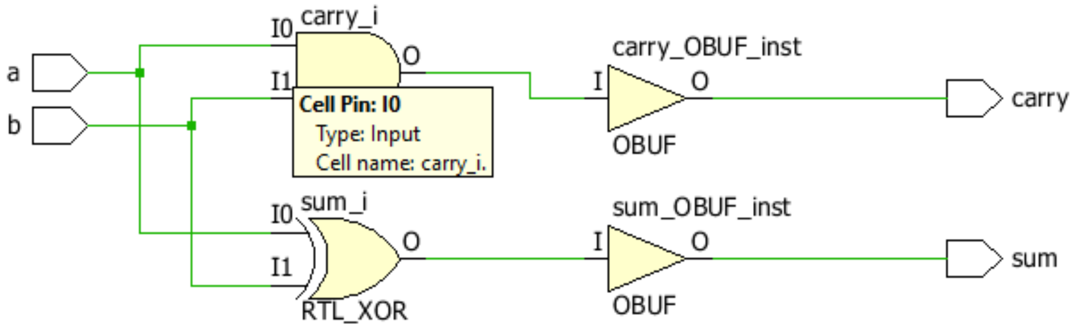
Signals: 0.031 W (2%)

Logic: 0.005 W (0%)

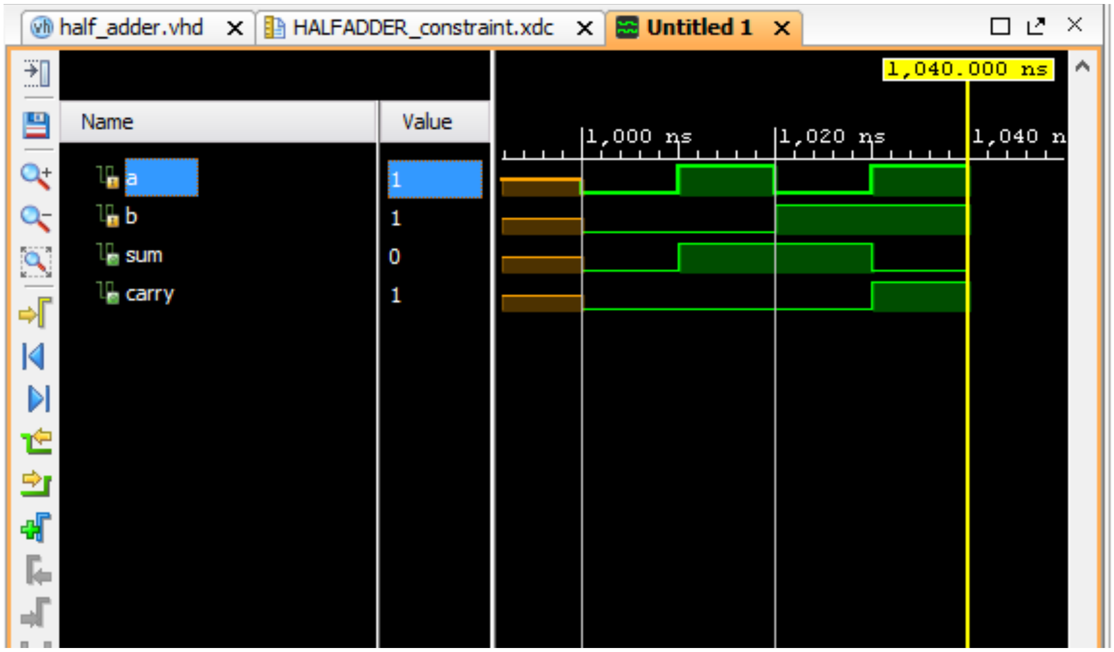
I/O: 1.966 W (98%)

Device Static: 0.077 W (4%)

SCHEMATIC:



SIMULATION:



Name	Value
a	1
b	1
sum	0
carry	1

ALU

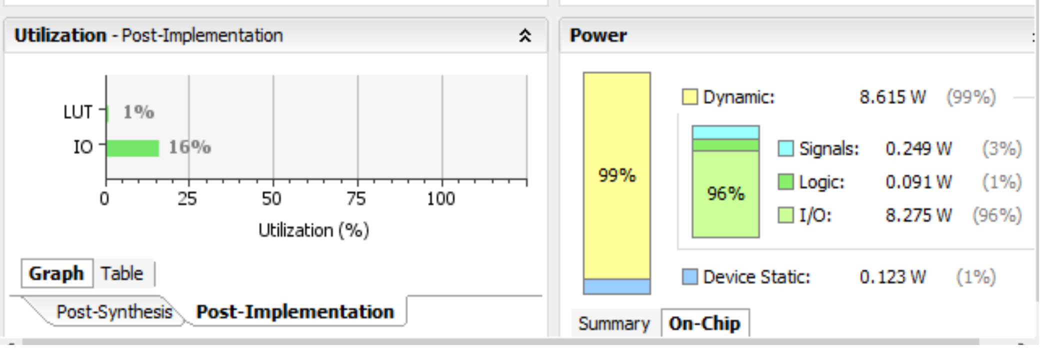
CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_arith.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity alu is
   Port ( areg,breg : in STD_LOGIC_VECTOR (3 downto 0);
          cin,al : in STD_LOGIC;
          op : in STD_LOGIC_VECTOR (1 downto 0);
          dout : out STD_LOGIC_VECTOR (3 downto 0);
          cout : out STD_LOGIC);
end alu;

architecture Behavioral of alu is
signal at  ,bt,dt:std_logic_vector(4 downto 0);

begin
at<='0'&areg;
bt<='0'&breg;
process(at,bt,cin,al,op)
begin

if al='0' then
case op is
when "00" => dt<=at+bt;
when "01" => dt<=at+bt+cin;
when "10" => dt<=at-bt;
when "11" => dt<=at-bt-cin;
when others =>null;
end case;

else
case op is
when "00" => dt<=at and bt;
when "01" => dt<=at or bt;
when "10" => dt<=at xor bt;
when "11" => dt<= not at;
when others =>null;
end case;
end if;
end process;

cout<=dt(4);
dout<=dt(3 downto 0);

end Behavioral;
```

PIN LOCK :

```
set_property PACKAGE_PIN R2 [get_ports areg[3]]
set_property PACKAGE_PIN T1 [get_ports areg[2]]
set_property PACKAGE_PIN U1 [get_ports areg[1]]
set_property PACKAGE_PIN W2 [get_ports areg[0]]

set_property PACKAGE_PIN R3 [get_ports breg[3]]
set_property PACKAGE_PIN T2 [get_ports breg[2]]
set_property PACKAGE_PIN T3 [get_ports breg[1]]
set_property PACKAGE_PIN V2 [get_ports breg[0]]

set_property PACKAGE_PIN V17 [get_ports cin]
set_property PACKAGE_PIN V16 [get_ports al]

set_property PACKAGE_PIN W17 [get_ports op[1]]
set_property PACKAGE_PIN W16 [get_ports op[0]]

set_property PACKAGE_PIN V19 [get_ports dout[3]]
set_property PACKAGE_PIN U19 [get_ports dout[2]]
set_property PACKAGE_PIN E19 [get_ports dout[1]]
set_property PACKAGE_PIN U16 [get_ports dout[0]]

set_property PACKAGE_PIN L1 [get_port cout]


set_property IOSTANDARD LVCMOS33 [get_ports {areg[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {areg[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {areg[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {areg[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {breg[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {breg[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {breg[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {breg[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cin}]
set_property IOSTANDARD LVCMOS33 [get_ports {al}]
set_property IOSTANDARD LVCMOS33 [get_ports {op[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {op[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cout}]
```

POWER CONSUMPTION:

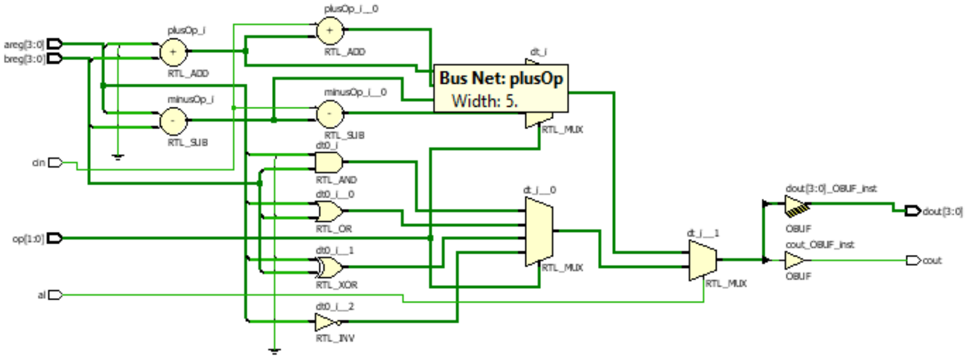


Utilization - Post-Implementation

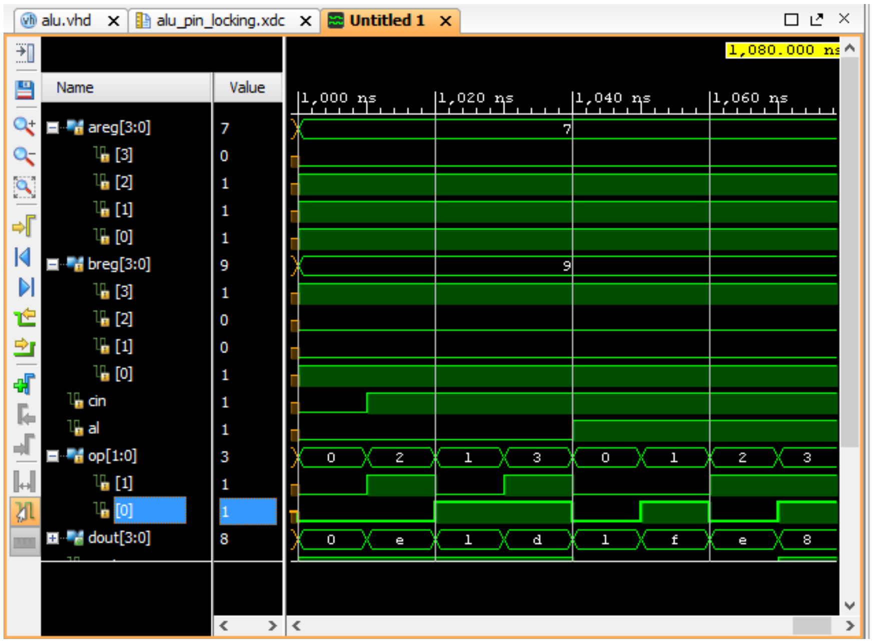
Power

Dynamic:	8.615 W	(99%)
Signals:	0.249 W	(3%)
Logic:	0.091 W	(1%)
I/O:	8.275 W	(96%)
Device Static:	0.123 W	(1%)

SCHEMATIC:



SIMULATION:



Name	Value
areg[3:0]	7
[3]	0
[2]	1
[1]	1
[0]	1
breg[3:0]	9
[3]	1
[2]	0
[1]	0
[0]	1
cin	1
al	1
op[1:0]	3
[1]	1
[0]	1
dout[3:0]	8

DISPLAY

CODE:

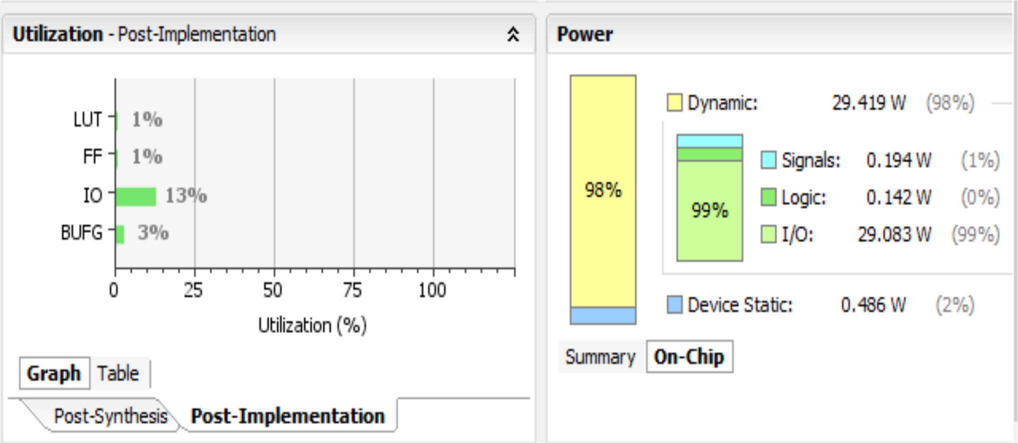
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_arith.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;

entity display is
   Port ( clk,rst : in STD_LOGIC;
         data : out STD_LOGIC_VECTOR (7 downto 0);
         sw1 : out STD_LOGIC_VECTOR (3 downto 0));
end display;

architecture Behavioral of display is
signal tmp : STD_LOGIC_VECTOR (23 downto 0);
signal sclk,srst : STD_LOGIC;
signal sw : STD_LOGIC_VECTOR (1 downto 0);

begin
process(clk,rst)
begin
if clk='1' and clk'event then
if rst='1' then
tmp <=x"00000";
srst<='1';
sclk<='0';

else
tmp<=tmp+1;
if tmp(23)='1' then
srst <= '0';
end if;
sclk <= tmp(22);
end if;
end if;
end process;


process(sclk,srst)
begin
if sclk='1' and sclk'event then
if srst='1' then
sw <="00";

else

case sw is
```

```
when "00" => data <= "11111001"; sw1 <= "1110";
when "01" => data <= "10100100"; sw1 <= "1101";
when "10" => data <= "10110000"; sw1 <= "1011";
when "11" => data <= "10011001"; sw1 <= "0111";
when others => null;
end case;

sw<= sw+1;
end if;
end if;
end process;

end Behavioral;
```

PIN LOCK :

```
set_property PACKAGE_PIN w5 [get_ports clk ]
set_property PACKAGE_PIN w16 [get_ports rst ]
set_property PACKAGE_PIN w7 [get_ports data[0] ]
set_property PACKAGE_PIN w6 [get_ports data[1] ]
set_property PACKAGE_PIN u8 [get_ports data[2] ]
set_property PACKAGE_PIN v8 [get_ports data[3] ]
set_property PACKAGE_PIN u5 [get_ports data[4] ]
set_property PACKAGE_PIN v5 [get_ports data[5] ]
set_property PACKAGE_PIN u7 [get_ports data[6] ]
set_property PACKAGE_PIN v7 [get_ports data[7] ]
set_property PACKAGE_PIN w4 [get_ports sw1[0] ]
set_property PACKAGE_PIN v4 [get_ports sw1[1] ]
set_property PACKAGE_PIN u4 [get_ports sw1[2] ]
set_property PACKAGE_PIN u2 [get_ports sw1[3] ]

set_property IOSTANDARD LVCMOS33 [get_ports {clk} ]
set_property IOSTANDARD LVCMOS33 [get_ports {rst} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[0]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[1]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[2]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[3]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[4]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[5]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[6]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {data[7]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {sw1[0]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {sw1[1]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {sw1[2]} ]
set_property IOSTANDARD LVCMOS33 [get_ports {sw1[3]} ]
```

POWER CONSUMPTION:



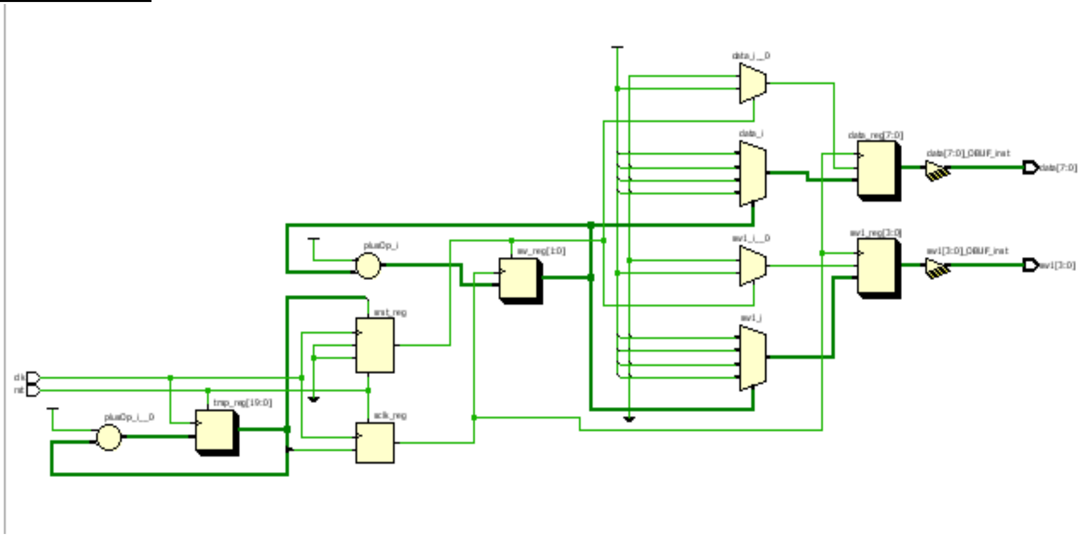
Utilization - Post-Implementation

LUT	1%
FF	1%
IO	13%
BUFG	3%

Power

🟨 Dynamic:	29.419 W	(98%)
Signals:	0.194 W	(1%)
Logic:	0.142 W	(0%)
I/O:	29.083 W	(99%)
🟦 Device Static:	0.486 W	(2%)

SCHEMATIC:



COUNTER

CODE:

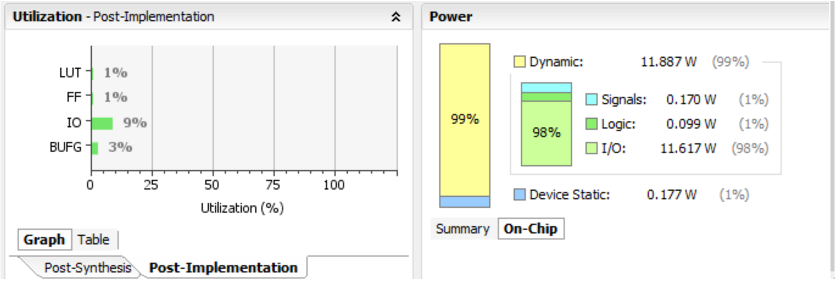
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
use IEEE.STD_LOGIC_arith.ALL;

entity counter is
   Port ( clk,rst : in STD_LOGIC;
        y : out STD_LOGIC_VECTOR (7 downto 0));
end counter;

architecture Behavioral of counter is
signal tmp: std_logic_vector(23 downto 0);
signal sclk,srst : std_logic;
signal yt:std_logic_vector(7 downto 0);

begin
process(clk,rst)
begin
if clk='1' and clk'event then
if rst='1' then
tmp <= x"000000";
srst <= '1';
sclk <= '0';

else
tmp <= tmp + 1;

if tmp(23) = '1' then
srst <= '0';
end if ;
sclk <= tmp(22);
end  if;
end if;
end process;

process(sclk,srst)
begin
if sclk ='1' and sclk'event then
if srst='1' then
yt <= x"00";
 else
 yt <= yt + 1;
 end if;
 end if;
 end process;
 y <= yt;
```

end Behavioral;

PIN LOCK :

```
set_property PACKAGE_PIN w5 [get_ports clk]
set_property PACKAGE_PIN w16 [get_ports rst]
set_property PACKAGE_PIN U16 [get_ports y[0]]
set_property PACKAGE_PIN E19 [get_ports y[1]]
set_property PACKAGE_PIN U19 [get_ports y[2]]
set_property PACKAGE_PIN V19 [get_ports y[3]]
set_property PACKAGE_PIN W18 [get_ports y[4]]
set_property PACKAGE_PIN U15 [get_ports y[5]]
set_property PACKAGE_PIN U14 [get_ports y[6]]
set_property PACKAGE_PIN V14 [get_ports y[7]]

set_property IOSTANDARD LVCMOS33 [get_ports {clk}]
set_property IOSTANDARD LVCMOS33 [get_ports {rst}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y[7]}]
```

POWER CONSUMPTION:



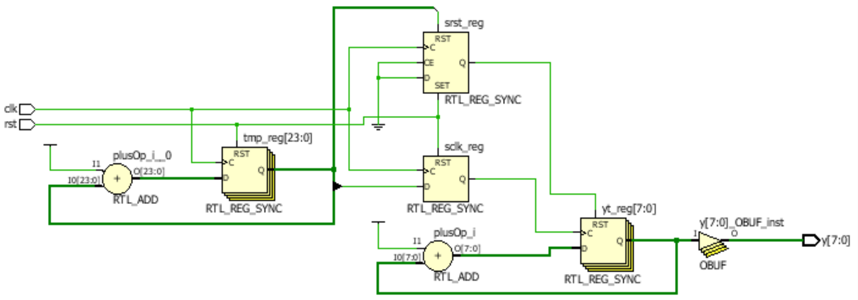
Utilization - Post-Implementation

	Utilization (%)
LUT	1%
FF	1%
IO	9%
BUFG	3%

Power

Dynamic:	11.887 W	(99%)
Signals:	0.170 W	(1%)
Logic:	0.099 W	(1%)
I/O:	11.617 W	(98%)
Device Static:	0.177 W	(1%)

SCHEMATIC:



FIFO

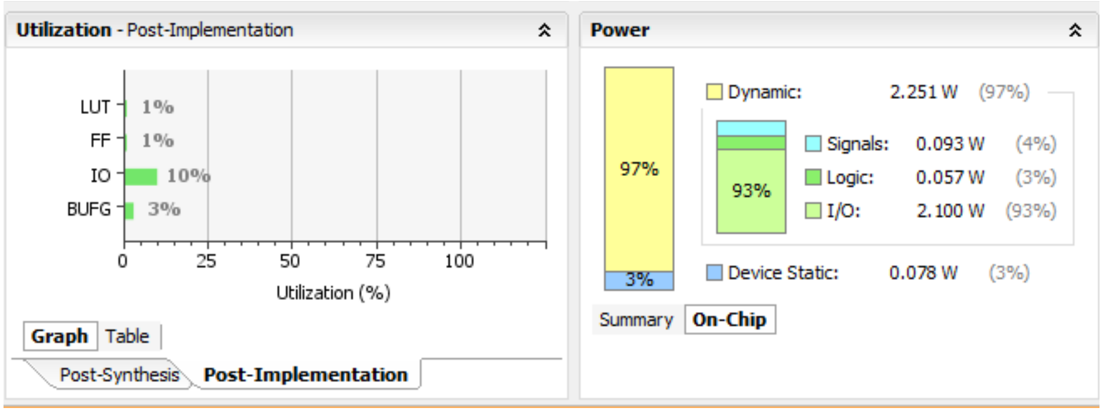
CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_unsigned.ALL;
use IEEE.STD_LOGIC_arith.ALL;

entity fifo is
   Port ( din : in STD_LOGIC_VECTOR (3 downto 0);
          dout : out STD_LOGIC_VECTOR (3 downto 0);
          rw,rst,clk : in STD_LOGIC);
end fifo;

architecture Behavioral of fifo is
type mem is array (0 to 3) of std_logic_vector(3 downto 0);
signal add: std_logic_vector(1 downto 0);
signal a:mem;
begin

process(clk, rst)
begin

if clk='1' and clk'event then
if rst='1' then
add<="00";
else
if rw='0' then
case add is
when "00" => a(0)<= din;
when "01" => a(1)<= din;
when "10" => a(2)<= din;
when "11" => a(3)<= din;
when others => null;
end case;
add <= add+1;

else
case add is
when "00" => dout <= a(0);
when "01" => dout <= a(1);
when "10" => dout <= a(2);
when "11" => dout <= a(3);
when others => null;
end case;
add<= add+1;

end if;
end if;
end if;
end process;

end Behavioral;
```

<u>PIN LOCK :</u>

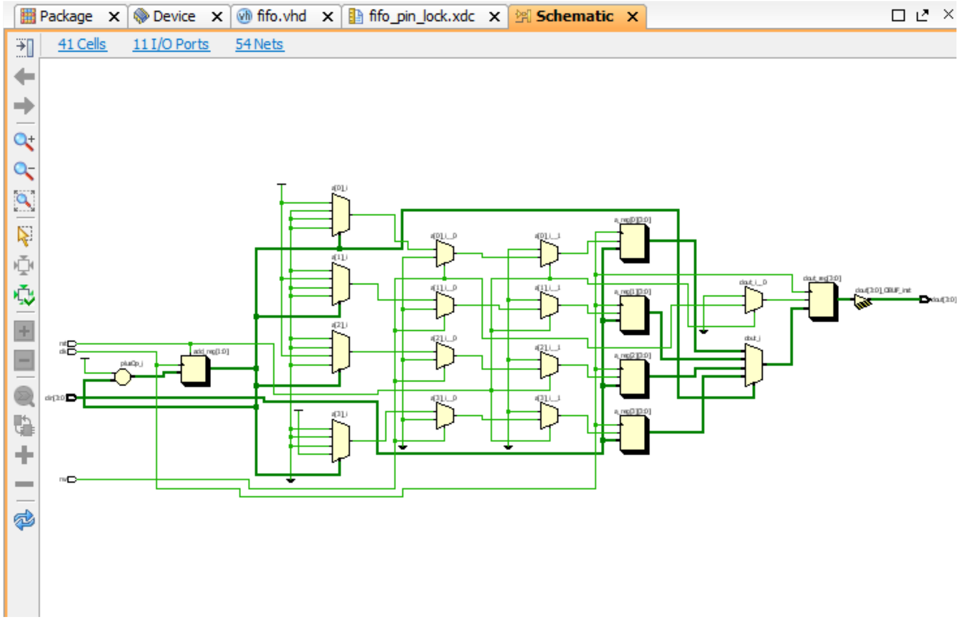
```
set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
set_property PACKAGE_PIN R2 [get_ports clk ]
set_property PACKAGE_PIN T1 [get_ports rst ]
set_property PACKAGE_PIN U1 [get_ports rw ]
set_property PACKAGE_PIN V17 [get_ports din[0] ]
set_property PACKAGE_PIN V16 [get_ports din[1] ]
set_property PACKAGE_PIN W16 [get_ports din[2] ]
set_property PACKAGE_PIN W17 [get_ports din[3] ]
set_property PACKAGE_PIN U16 [get_ports dout[0] ]
set_property PACKAGE_PIN E19 [get_ports dout[1] ]
set_property PACKAGE_PIN U19 [get_ports dout[2] ]
set_property PACKAGE_PIN V19 [get_ports dout[3] ]

set_property IOSTANDARD LVCMOS33 [get_ports {clk}]
set_property IOSTANDARD LVCMOS33 [get_ports {rst}]
set_property IOSTANDARD LVCMOS33 [get_ports {rw}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {dout[3]}]
```

<u>POWER CONSUMPTION:</u>

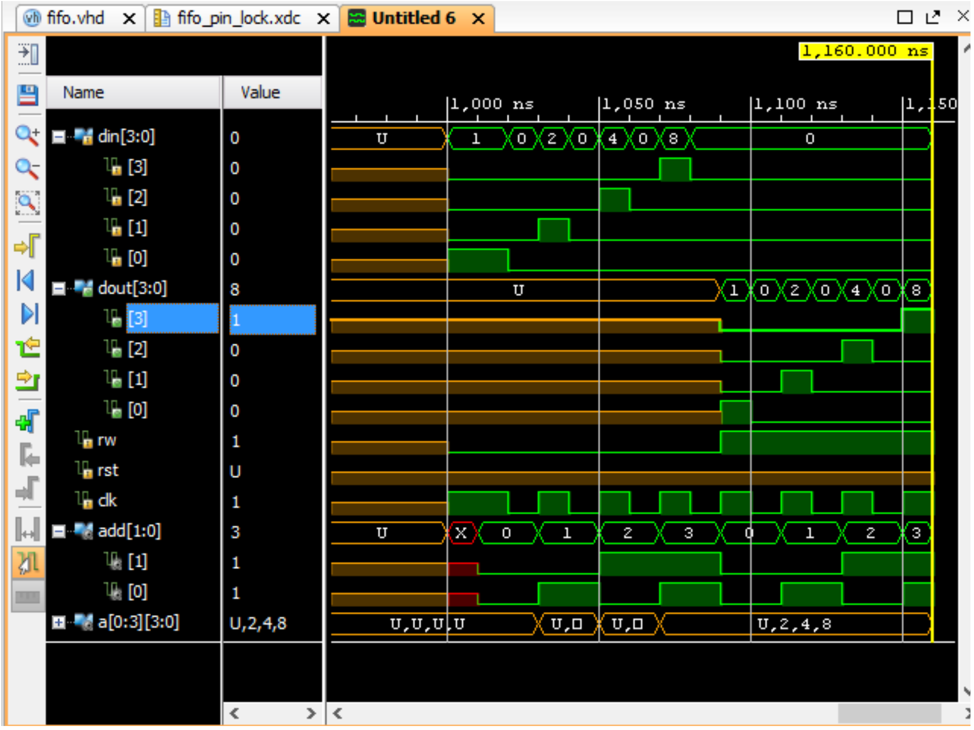


Dynamic:	2.251 W	(97%)
Signals:	0.093 W	(4%)
Logic:	0.057 W	(3%)
I/O:	2.100 W	(93%)
Device Static:	0.078 W	(3%)

SCHEMATIC:



SIMULATION:



Name	Value
din[3:0]	0
[3]	0
[2]	0
[1]	0
[0]	0
dout[3:0]	8
[3]	1
[2]	0
[1]	0
[0]	0
rw	1
rst	U
clk	1
add[1:0]	3
[1]	1
[0]	1
a[0:3][3:0]	U,2,4,8

Universal Shift Register

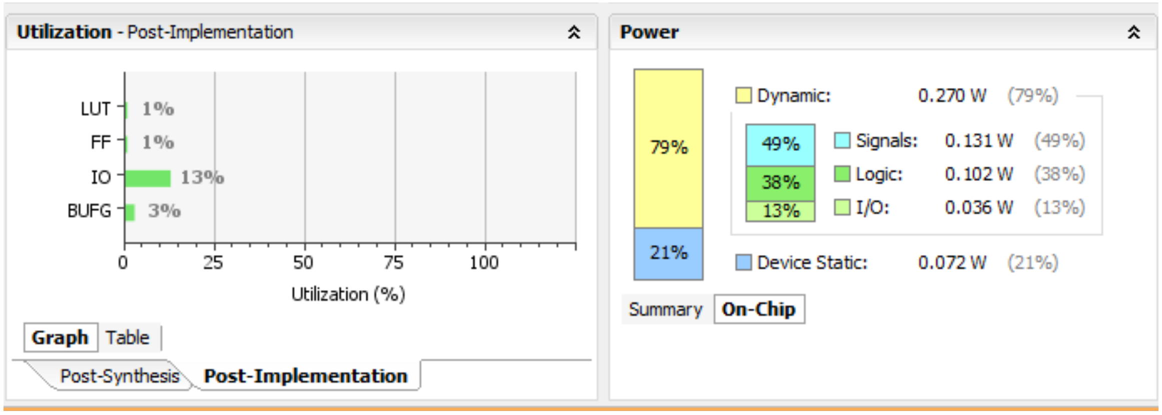
CODE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity shift_reg is
    Port ( din : in STD_LOGIC_VECTOR (3 downto 0);
           dsl : in STD_LOGIC;
           dsr : in STD_LOGIC;
           q : out STD_LOGIC_VECTOR (3 downto 0);
           rst : in STD_LOGIC;
           clk : in STD_LOGIC;
           mode : in STD_LOGIC_VECTOR (1 downto 0));
end shift_reg;

architecture Behavioral of shift_reg is
signal count:integer:=1;
signal tmp: std_logic:='0';
signal tep: std_logic_vector(3 downto 0);
signal clock_out : std_logic;
begin

p1:process(clk)
begin

if clk='1' and clk'event then
count<= count + 1;
if(count= 25000000)
 then
 tmp <= NOT tmp;
 count <=1;
 end if;
end if;
clock_out <= tmp;
end process p1;

p2:process(clock_out, rst,dsl,dsr, din, mode)
begin

if rst = '1' then
tep <= "0000";
elsif( clock_out='1' and clock_out'event) then
case mode is
when "00" => tep <= din;    --parallel load
when "01" => tep <= dsr & tep(3 downto 1);  --right shift
when "10" => tep <= tep (2 downto 0) & dsl;
when others => null;
end case;
end if;
end process p2;
q<=tep;

end Behavioral;
```

PIN LOCK :

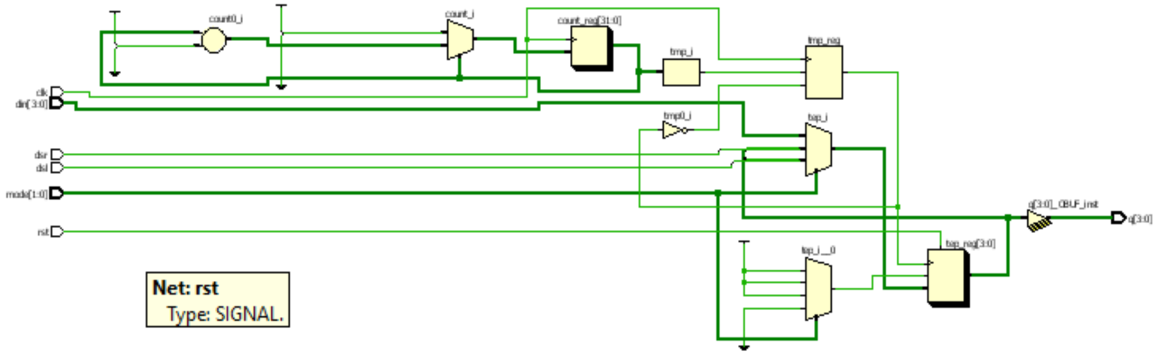
```
set_property PACKAGE_PIN W2 [get_ports {din[0]}]
set_property PACKAGE_PIN U1 [get_ports {din[1]}]
set_property PACKAGE_PIN T1 [get_ports {din[2]}]
set_property PACKAGE_PIN R2 [get_ports {din[3]}]

set_property PACKAGE_PIN R3 [get_ports dsl]
set_property PACKAGE_PIN T2 [get_ports dsr]

set_property PACKAGE_PIN V2 [get_ports {mode[0]}]
set_property PACKAGE_PIN T3 [get_ports {mode[1]}]

set_property PACKAGE_PIN W13 [get_ports rst]
set_property PACKAGE_PIN W5 [get_ports clk]

set_property PACKAGE_PIN V19 [get_ports {q[3]}]
set_property PACKAGE_PIN U19 [get_ports {q[2]}]
set_property PACKAGE_PIN E19 [get_ports {q[1]}]
set_property PACKAGE_PIN U16 [get_ports {q[0]}]

set_property IOSTANDARD LVCMOS33 [get_ports {din[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {din[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {mode[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {mode[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {q[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {q[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {q[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {q[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports dsl]
```

POWER CONSUMPTION:

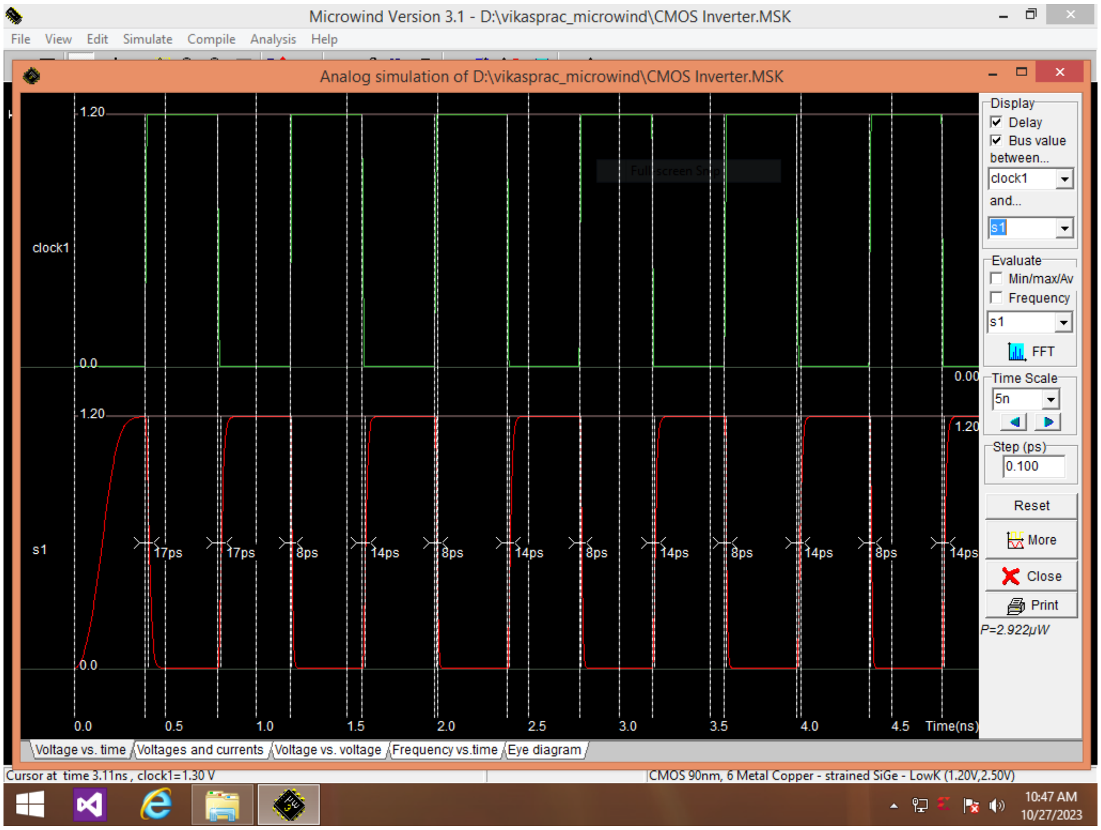


Dynamic:	0.270 W	(79%)
Signals:	0.131 W	(49%)
Logic:	0.102 W	(38%)
I/O:	0.036 W	(13%)
Device Static:	0.072 W	(21%)

SCHEMATIC:



INVETER



Microwind Version 3.1 - D:\vikasprac_microwind\CMOS Inverter.MSK

Analog simulation of D:\vikasprac_microwind\CMOS Inverter.MSK

Display: ☑ Delay ☑ Bus value between... clock1 and... s1

Evaluate: □ Min/max/Av □ Frequency s1

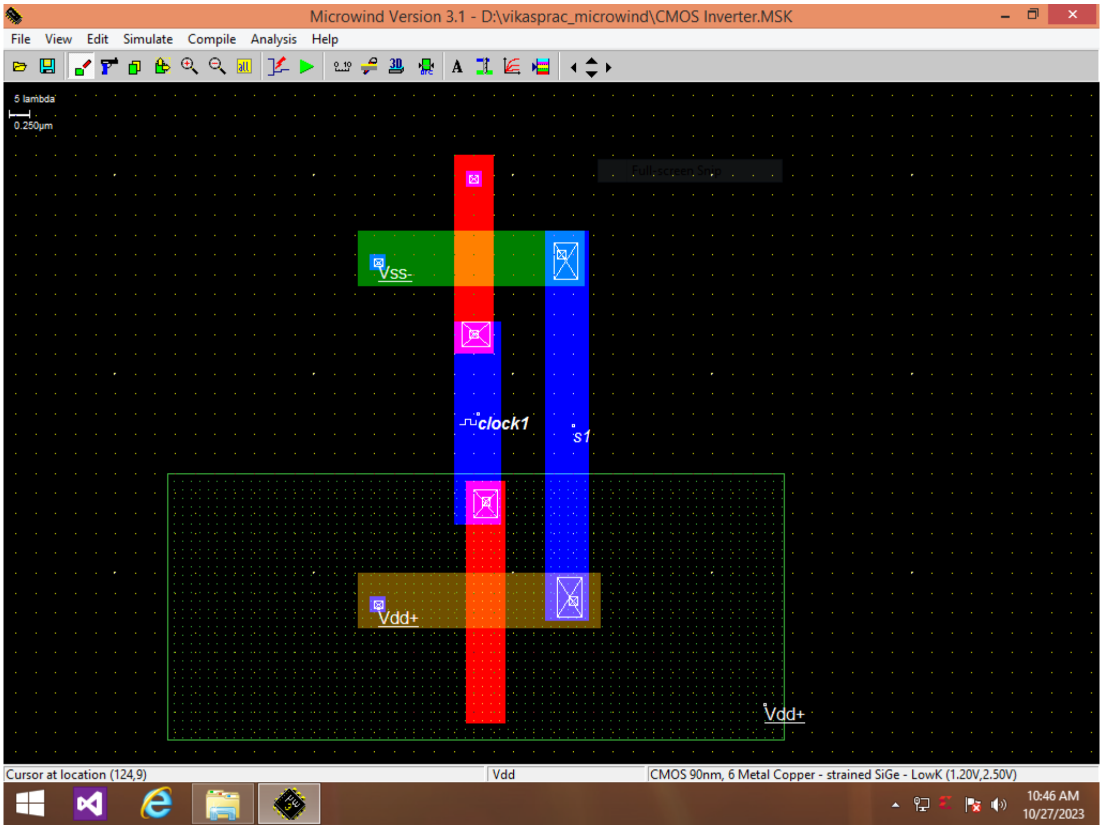
Time Scale: 5n

Step (ps): 0.100

P=2.922µW

Cursor at time 3.11ns , clock1=1.30 V

CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)



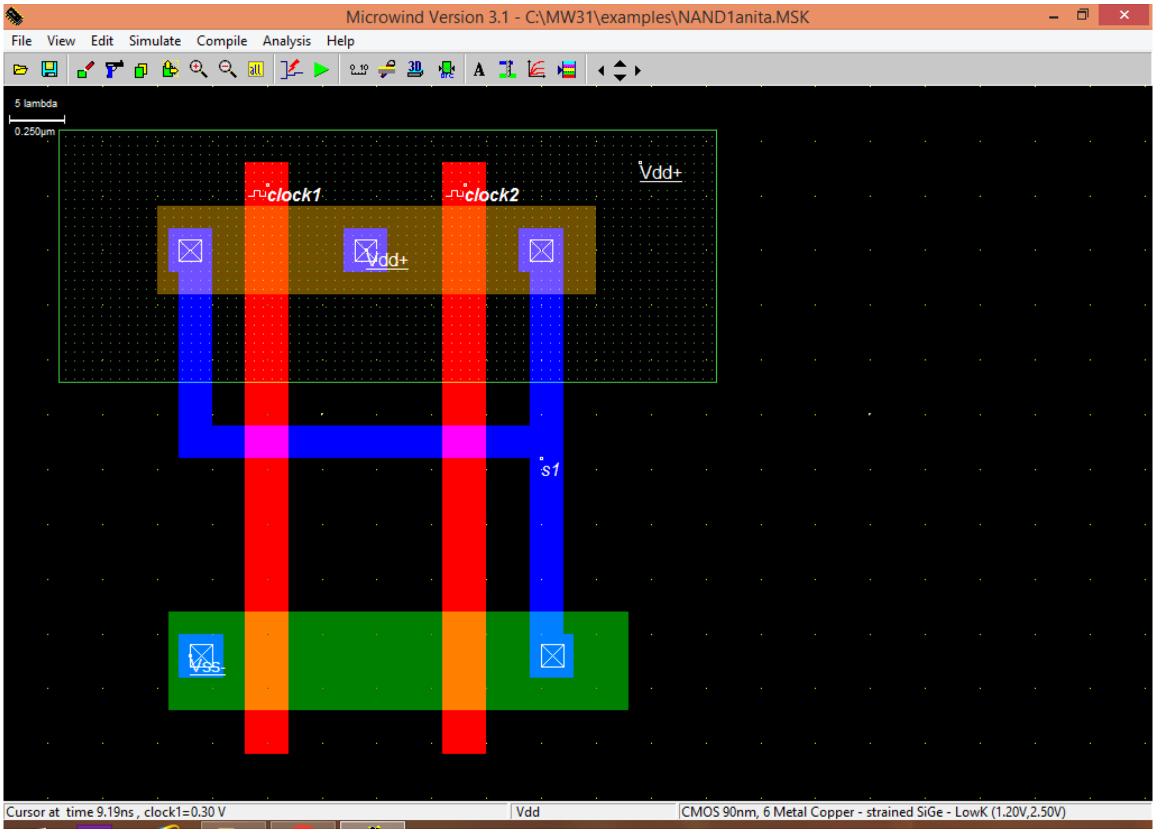
Microwind Version 3.1 - D:\vikasprac_microwind\CMOS Inverter.MSK

Cursor at location (124,9)

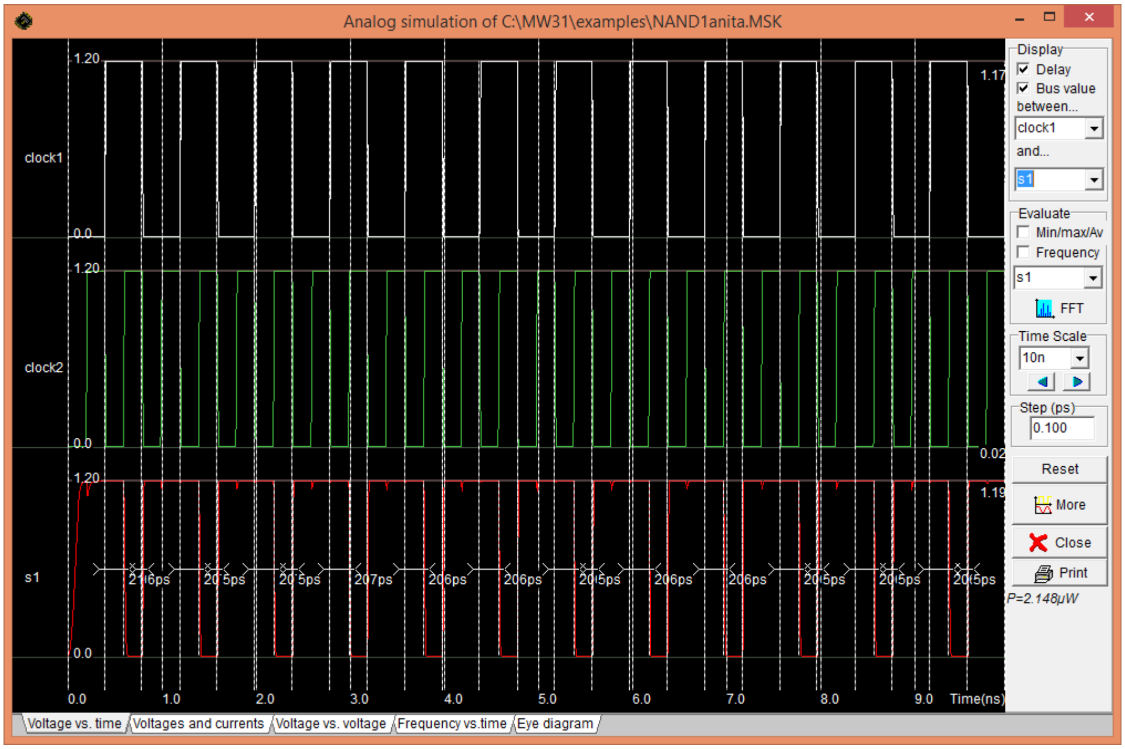
Vdd

CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

NAND



Cursor at time 9.19ns , clock1=0.30 V | Vdd | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)



Display
☑ Delay
☑ Bus value
between...
clock1
and...
s1

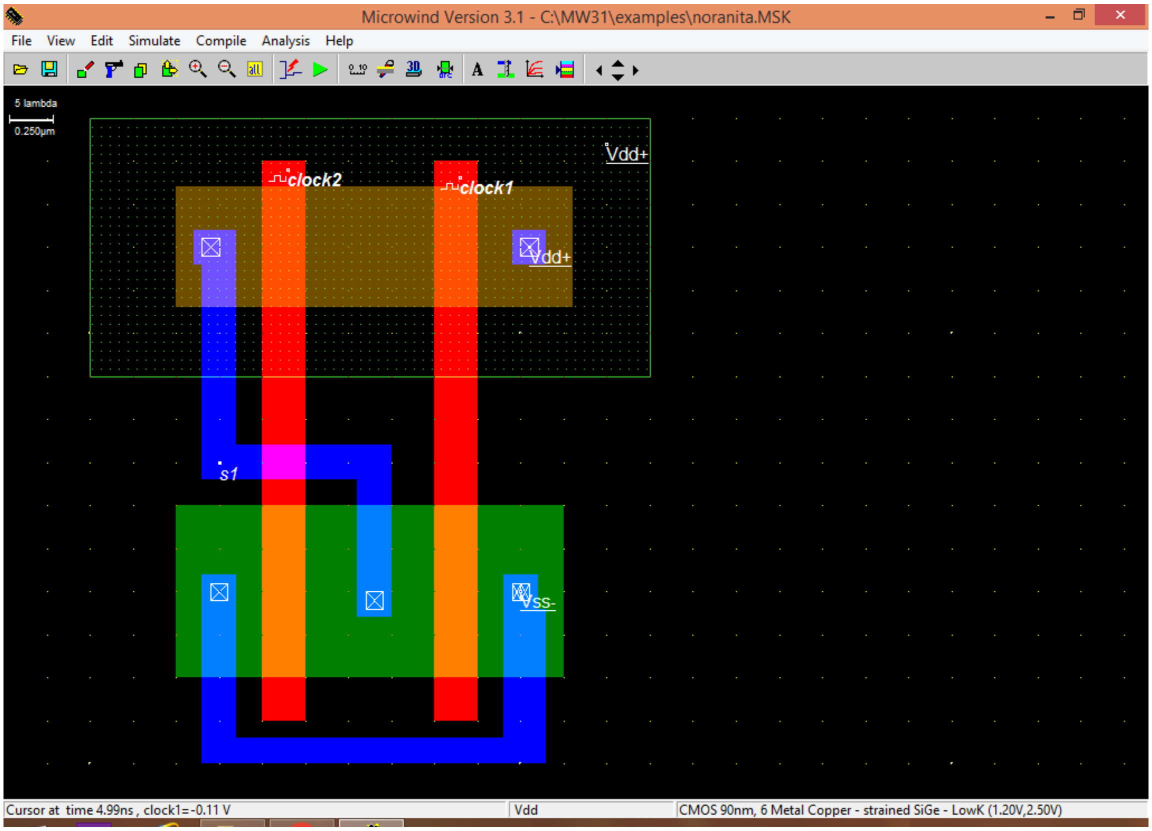
Evaluate
☐ Min/max/Av
☐ Frequency
s1

Time Scale
10n

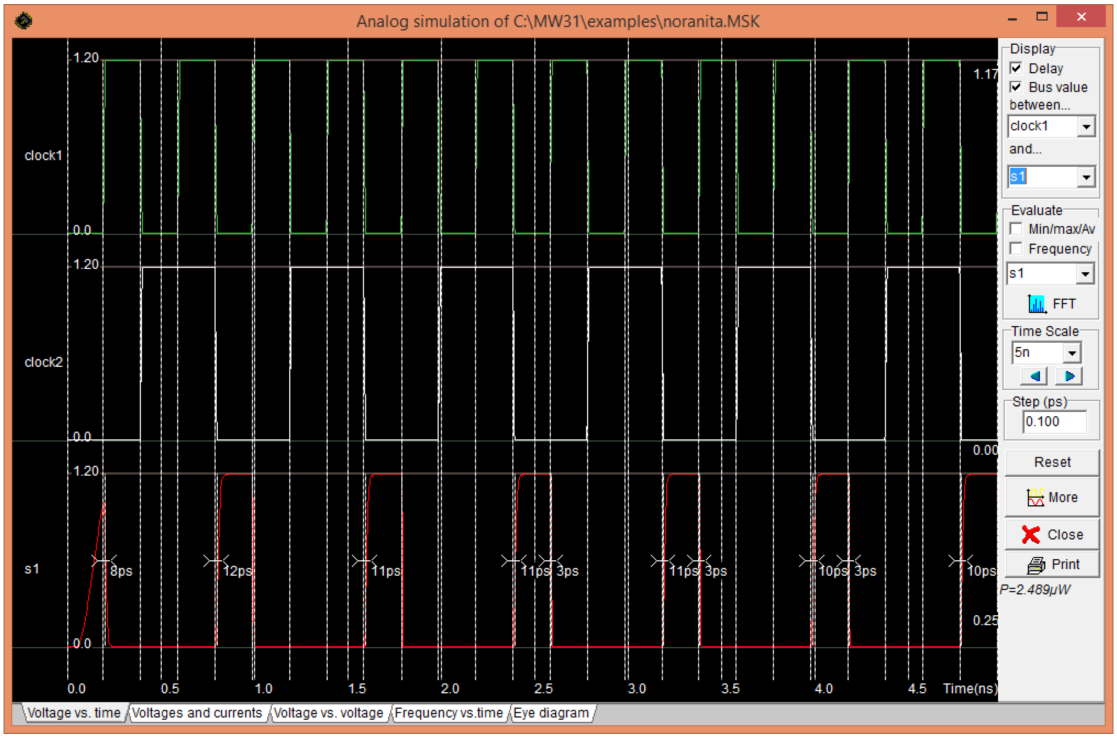
Step (ps)
0.100

P=2.148µW

NOR



Cursor at time 4.99ns , clock1=-0.11 V | Vdd | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)



Display
☑ Delay
☑ Bus value between...
clock1
and...
s1

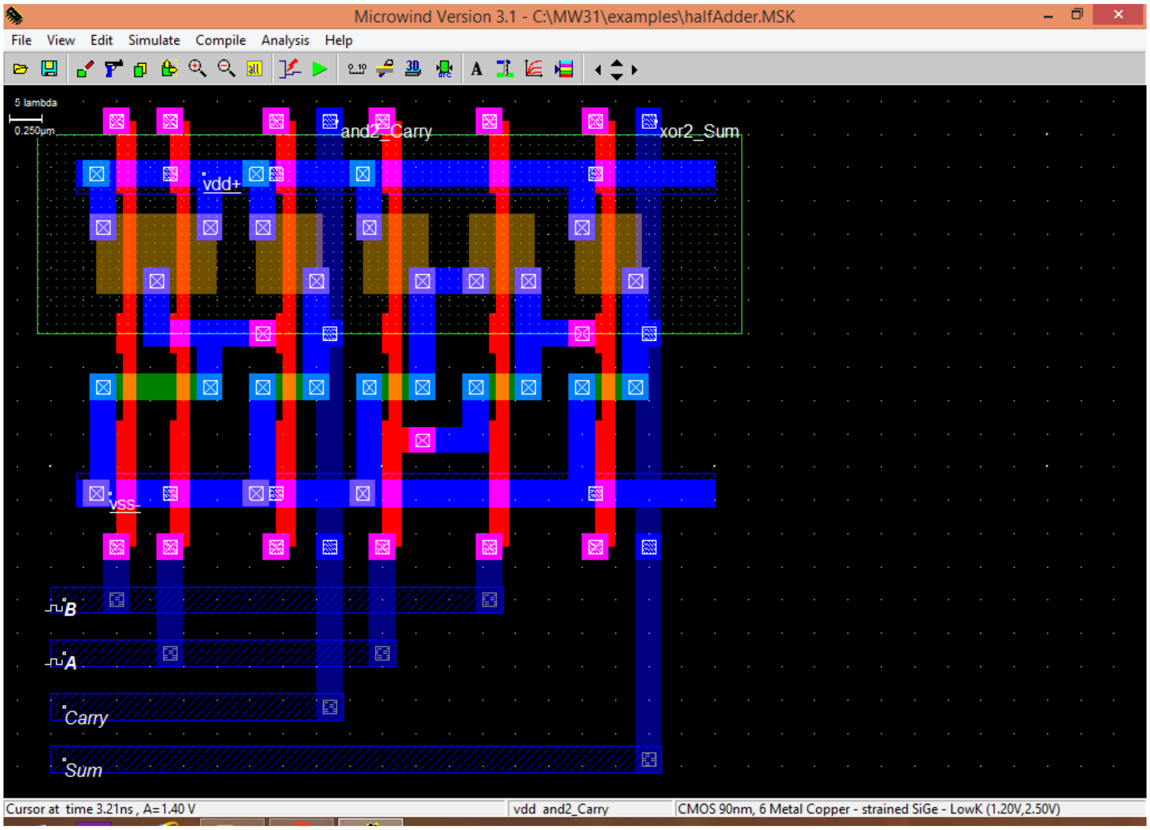
Evaluate
☐ Min/max/Av
☐ Frequency
s1

Time Scale
5n

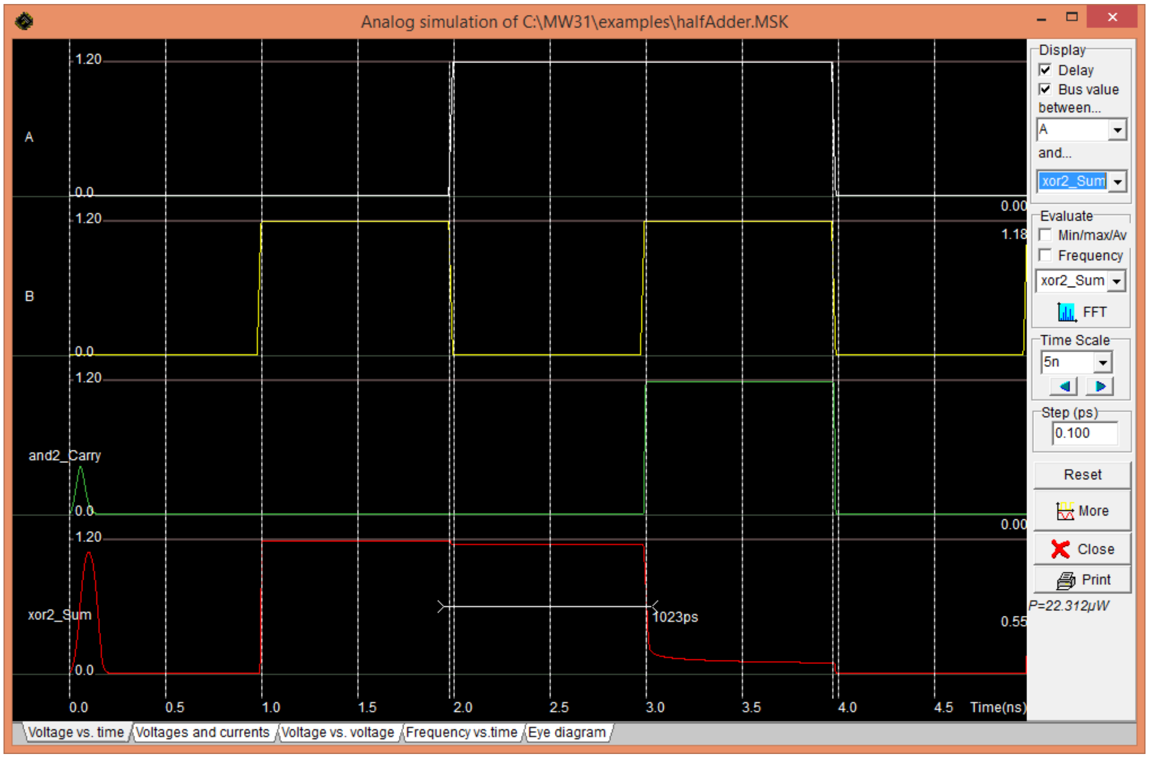
Step (ps)
0.100

P=2.489µW

Half Adder



Cursor at time 3.21ns , A=1.40 V | vdd and2_Carry | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)



Display
☑ Delay
☑ Bus value
between...
A
and...
xor2_Sum

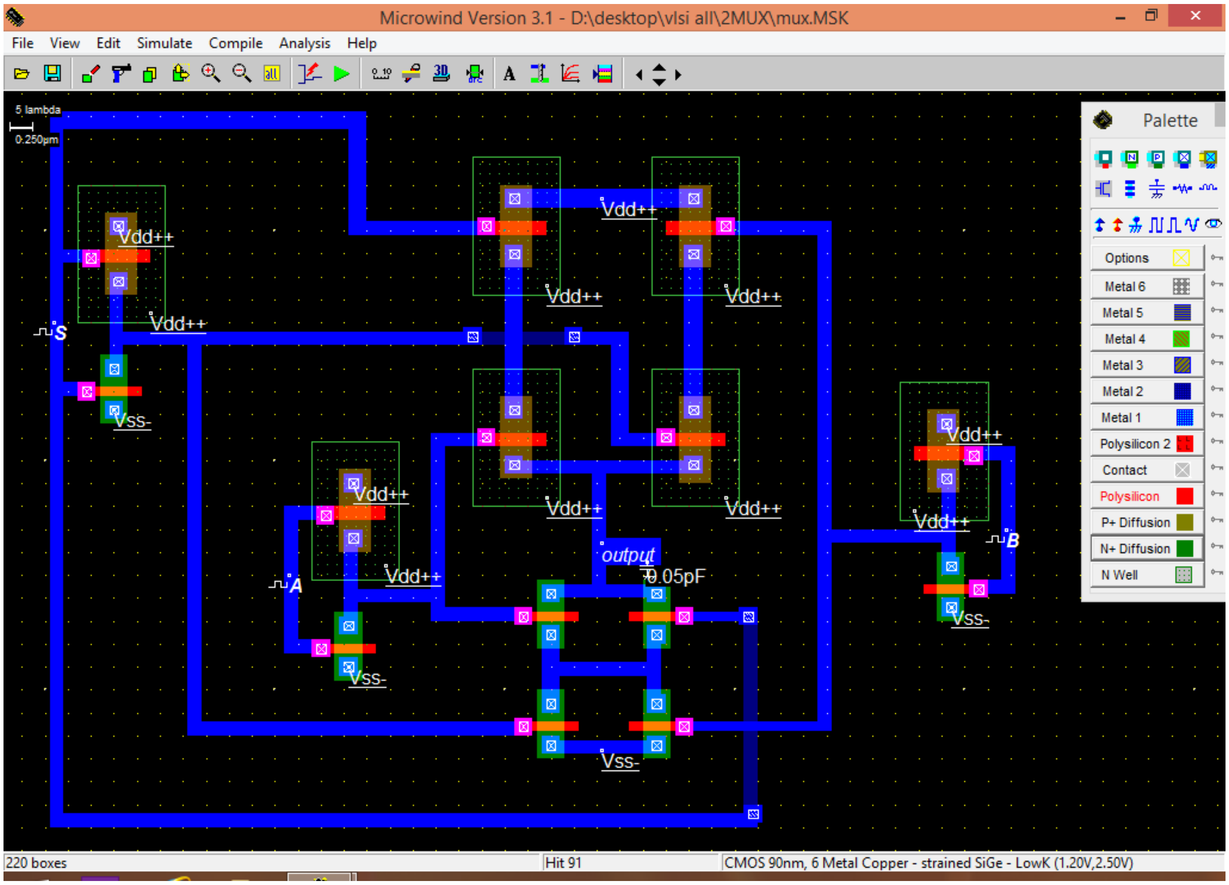
Evaluate
□ Min/max/Av
□ Frequency
xor2_Sum

Time Scale
5n

Step (ps)
0.100

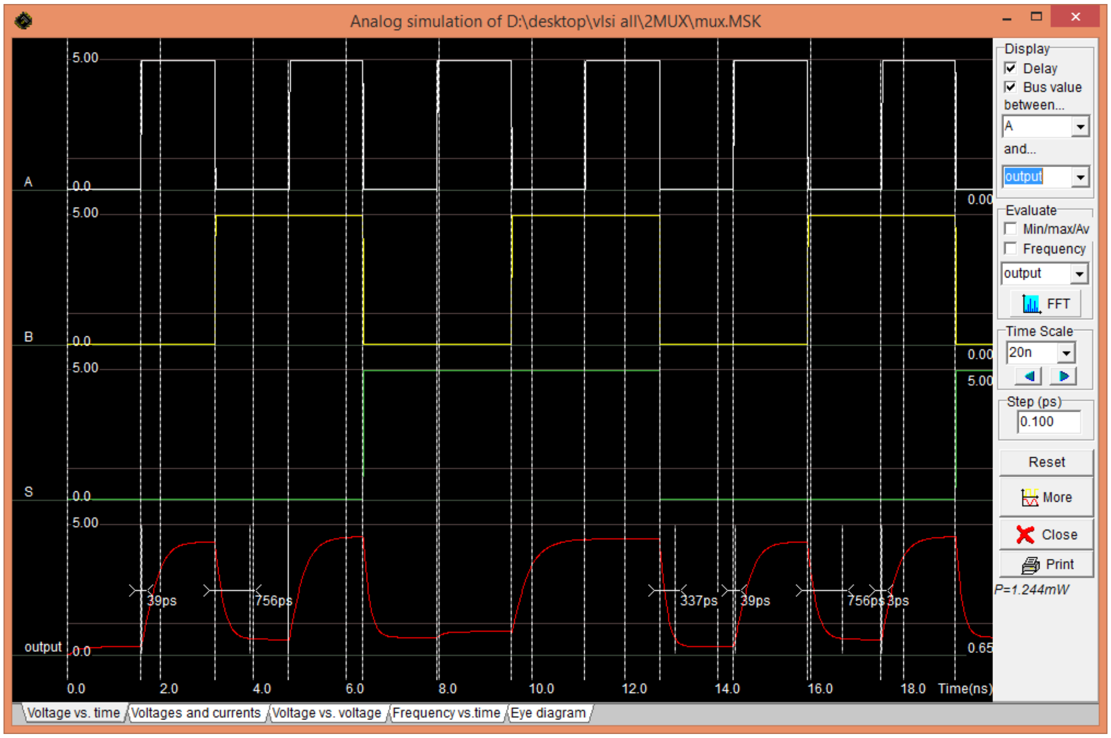
P=22.312µW

2:1 MUX



Microwind Version 3.1 - D:\desktop\vlsi all\2MUX\mux.MSK

220 boxes | Hit 91 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)



Analog simulation of D:\desktop\vlsi all\2MUX\mux.MSK

Display
☑ Delay
☑ Bus value
between...
A
and...
output

Evaluate
☐ Min/max/Av
☐ Frequency
output

Time Scale
20n

Step (ps)
0.100

P=1.244mW