

October 1987 Revised May 2002

MM74C14 Hex Schmitt Trigger

General Description

The MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The positive and negative going threshold voltages V_{T+} and V_{T-} , show low variation with respect to temperature (typ. $0.0005 \text{V}/^\circ\text{C}$ at $V_{CC}=10\text{V})$, and hysteresis, $V_{T+}-V_{T-} \ge 0.2~V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to $\rm V_{\rm CC}$ and GND.

Features

■ Wide supply voltage range: 3.0V to 15V■ High noise immunity: 0.70 V_{CC} (typ.)

■ Low power: TTL compatibility: 0.4 V_{CC} (typ.) 0.2 V_{CC} guaranteed

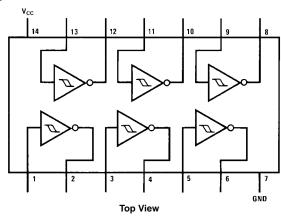
■ Hysteresis: 0.4 V_{CC} (typ.): 0.2 V_{CC} guaranteed

Ordering Code:

Order Number	Package Number	Package Description
MM74C14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74C14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Absolute Maximum Ratings(Note 1)

 $\begin{array}{lll} \mbox{Voltage at Any Pin} & -0.3\mbox{Vto V}_{CC} + 0.3\mbox{V} \\ \mbox{Operating Temperature Range} & -55\mbox{°C to } +125\mbox{°C} \\ \mbox{Storage Temperature Range} & -65\mbox{°C to } +150\mbox{°C} \\ \end{array}$

Power Dissipation

Dual-In-Line 700 mW

 $\begin{tabular}{lll} Small Outline & 500mW \\ Operating V_{CC} Range & 3.0V to 15V \\ \end{tabular}$

Absolute Maximum V_{CC} 18V

Lead Temperature

(Soldering, 10 seconds) 260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics tables provide conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO C	Mos	•				
V_{T+}	Positive Going Threshold Voltage	V _{CC} = 5V	3.0	3.6	4.3	
		V _{CC} = 10V	6.0	6.8	8.6	V
		V _{CC} = 15V	9.0	10.0	12.9	Ī
V _{T-}	Negative Going Threshold Voltage	V _{CC} = 5V	0.7	1.4	2.0	
		V _{CC} = 10V	1.4	3.2	4.0	V
		V _{CC} = 15V	2.1	5.0	6.0	Ī
$V_{T+} - V_{T-}$	Hysteresis	V _{CC} = 5V	1.0	2.2	3.6	
		V _{CC} = 10V	2.0	3.6	7.2	V
		V _{CC} = 15V	3.0	5.0	10.8	Ī
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_{O} = -10 \mu A$	4.5			V
()		$V_{CC} = 10V, I_{O} = -10 \mu A$	9.0			†
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5V, I_{O} = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_{O} = 10 \mu A$			1.0	†
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	V _{CC} = 15V, V _{IN} = 0V	-1.0	-0.005		μА
Icc	Supply Current	V _{CC} = 15V, V _{IN} = 0V/15V		0.05	15	1
		V _{CC} = 5V, V _{IN} = 2.5V (Note 2)		20		1
		V _{CC} = 10V, V _{IN} = 5V (Note 2)		200		μΑ
		V _{CC} = 15V, V _{IN} = 7.5V (Note 2)		600		
CMOS/LPTT	L INTERFACE	•				- I
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5V	4.3			V
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5V			0.7	V
V _{OUT(1)}	Logical "1" Output Voltage	74C, V _{CC} = 4.75V, I _O = -360 μA	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	74C, V _{CC} = 4.75V, I _O = 360 μA			0.4	V
OUTPUT DR	IVE (see Family Characteristics Data	Sheet) T _A = 25°C (Short Circuit Current	t)			1
I _{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{OUT} = 0V$	-1.75	-3.3		mA
	(P-Channel)					
I _{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{OUT} = 0V$	-8.0	-15		mA
	(P-Channel)					
I _{SINK}	Output Sink Current	V _{CC} = 5V, V _{OUT} = V _{CC}	1.75	3.6		mA
S	(N-Channel)					
I _{SINK}	Output Sink Current	V _{CC} = 10V, V _{OUT} = V _{CC}	8.0	16		mA
S	(N-Channel)					

Note 2: Only one of the six inputs is at $\frac{1}{2}$ V_{CC}; the others are either at V_{CC} or GND.

AC Electrical Characteristics (Note 3)

 $T_A=25^{\circ}C,\ C_L=50$ pF, unless otherwise specified

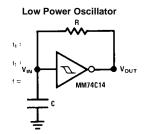
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{PD0}	Propagation Delay	$V_{CC} = 5V$		220	400	n
t _{PD1}	from Input to Output	V _{CC} = 10V		80	200	ns
C _{IN}	Input Capacitance	Any Input (Note 4)		5.0		pF
C _{PD}	Power Dissipation Capacitance	Per Gate (Note 5)		20		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

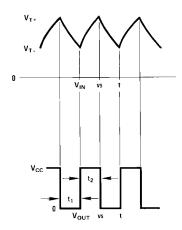
Typical Applications

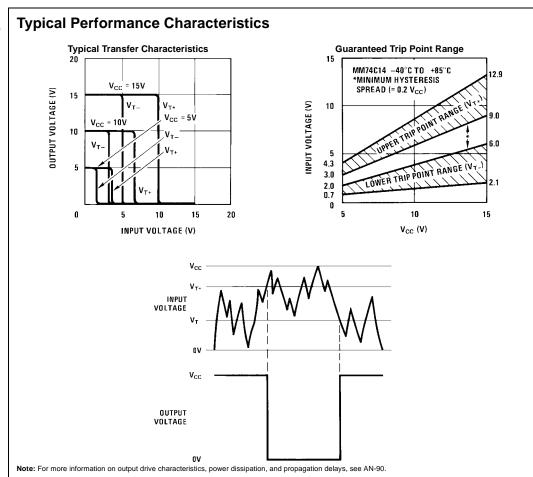


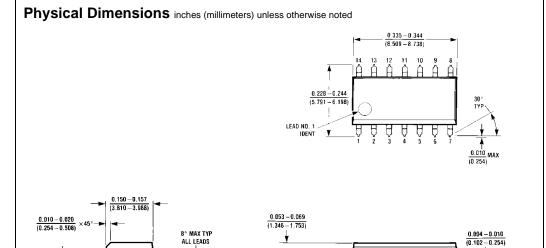
$$\begin{split} t_1 &\approx RC \; \ell \; n \frac{V_{T+}}{V_T} \\ t_1 &\approx RC \; \ell \; n \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \\ f &\approx \frac{1}{RC \; \ell \; n \frac{V_{T+} \left(V_{CC} - V_{T-}\right)}{V_{T-} \left(V_{CC} - V_{T-}\right)}} \approx \frac{1}{1.7 \; RC} \end{split}$$

Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$

V_{CC} ----







14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

0.014 (0.356)

0.050 (1.270) TYP

SEATING PLANE

0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS

0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS

0.004 (0.102) ALL LEAD TIPS $\frac{0.014-0.020}{(0.356-0.508)}\, \rm TYP$

- 0.008 (0.203) TYP

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 IDEN1 1 2 3 4 5 6 7 1 2 3 IDENT $\frac{0.092}{(2.337)}$ DIA 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 0.135 ± 0.005 0.300 - 0.320 (3.429 ± 0.127) $\overline{(7.620 - 8.128)}$ 0.065 0.145 - 0.200 0.060 (1.524) 4° TYP (1.651) (3.683 - 5.080) $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 95° ± 5° 0.020 (0.508)0.125 - 0.150MIN 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381) (7.112)-MIN 0.014 - 0.023 $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584)0.050±0.010 TYP $0.325 \,{}^{+\, 0.040}_{-\, 0.015}$ (1.270 - 0.254) $8.255 + 1.016 \\ -0.381$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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