Concordia University

Department of Computer Science & Software Engineering

Final Exam

Course: **COMP 228, Section DD** **Date: Saturday April 25, 2020**

Instructor: **Samia Hilal** **Time: 14:00-17:00**

Student Name:	
Student ID:	

Exam Instructions & Submission – Read all instructions carefully before starting

1. It is forbidden to communicate or share answers with another student during the exam.
2. The exam booklet has 8 pages including the cover page.
3. You have 3.0 hours to complete the exam; make sure to submit your completed exam within the allowed time.
4. You have to answer all questions on the exam.

5. **Several possible options to complete your Solution:**
   Option 1: Type your answers in a separate word document and submit in word or PDF format. Please make sure to scan and include all rough work (scan, screenshot, etc.) with your submission.
   Option 2: Print the exam booklet and write directly on it. You can use any additional white paper to complete your solution. If you choose to do so, **scan all copies including the cover page with your name and ID, in 1 file and submit**. You need to be able to do this on your own and have the required equipment (scanner). Please make sure to allow sometime to complete this task.
   Option3: If you have the tools to write directly on the .pdf file then feel free to do so.

6. Please Type or write Full Name and ID number on each page of the exam whether you write by hand or type your answers in a word document.
7. Please make sure that all work that you submit is legible and clear. No credit will be given to work that cannot be clearly understood.
8. If you are typing in a file, please make sure to save your work often.
9. If you encounter any problems during the exam, please collect all details: (error messages, screenshots, etc.) and communicate with me immediately by email at samia.hilal@concordia.ca
10. IF you have any questions during the exam, please email me at the same address.
11. I will be available on zoom during the exam if you have any questions. **Please use private chat only**.
12. You can access the zoom session from Moodle course page under ***Virtual Course Meetings***. No password required. Here's the link: https://concordia-ca.zoom.us/j/96362283481 and Meeting ID: 963 6228 3481

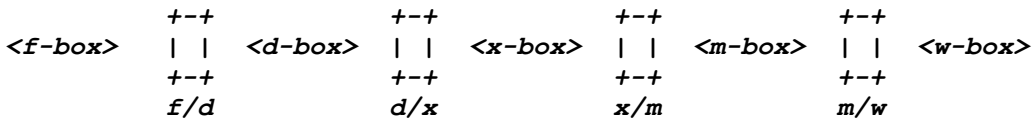
1. **[10 marks] Amdahl's Law.**

On a uniprocessor, portion A of program P consumes 24 seconds, while portion B consumes 822 seconds. On a parallel computer, moderately serial portion A speeds up 4 times, while perfectly parallel portion B speeds up by the number of processors.

1- What is the speedup of program P on 1,024 processors? ---------- times
2- How many processors are required to achieve at least half the theoretical maximum possible speedup on P?

2. **[15 marks] Pipeline Information Flow.**

Consider our instruction-execution pipeline ***with forwarding***: Each of the following 6 questions is independent.



a- When the d-box decodes the instruction 'l.d f6,-24(r2)', the _____ box receives the following 2 values: _____, _____ and calculates a memory address.

b- When the d-box decodes the instruction 'mul.d f6, f2, f4', the _____ box receives the following 2 values: _____, _____ and calculates _____. The w-box will receive the following 2 information: _____, _____ for the same instruction.

c- When the m-box processes the instruction 's.d f6, -4(r4)', it needs to know the _____ _____ that was calculated by the _____. The m-box also receives the value of _____ and updates _____.

d- When the pipeline is processing the instruction 'bne r1, r2, loop the **d-box** performs the following 3 actions (one of the actions is conditional):

1- _____
3- _____
2- _____

e- When a program is to be executed, the _____ gets the address of the _____ _____ in the program; and it gets incremented after each instruction is _____.

f- Explain briefly (3-4 sentences) the data dependency between the following 2 instructions and indicate how it affects the data flow in the pipeline.

	1	**2**	**3**	**4**	**5**	**6**	**7**
add f6, f8, f4	f	d	x	n	w		
s.d f6, 4(r1)		f	d	x	m		

3. [20 marks] Fractional-Number Formats

a) [5 marks] A fixed-point binary number system has 5 whole bits and 3 fractional bits. What is the range of numbers ***in binary*** that can be represented in this format? What is the decimal value of the largest number that can be represented?

b) [6 marks] A fixed-point binary number system has 4 whole bits and 12 fractional bits. Show the (4-hexit) hexadecimal representation of the following decimal numbers 0.375, - 1.33, and 1/40 in this finite format. Do not show recurring sequences.

c) [4 marks] Assume a 16-bit floating point format designed as follows: 4-bit signed exponent and 12-bit fraction. Normalization is strictly enforced. What is the hexadecimal representation of the 16-bit floating point format for 1/40?

d) [5 marks] add the following two hexadecimal floating point numbers represented in the format described in c) above. Express their sum as a (4-hexit) hexadecimal floating point number in the same format. **aacd + cb45**

4. [10 marks] Digital Logic

a) Let 'A' be the ternary connective such that 'Apqr' is equivalent to '(p --> q) /\ (q< --> r)'. We have: p --> q |= =| ~p \/ q. ‘p<-->q’ is true iff ‘p’ and ‘q’ have the same truth value. 'F' and 'T' are constant functions.

Using only {'A', 'F'}, synthesize: ~p |= =| A ___ ___ ___

Using only {'A', 'F', '~'}, synthesize: p /\ q |= =| A ___ ___ ___

5. [15 marks] Instructions with an immediate

a) Assume 32-bit registers, instructions, and memory addresses. Immediates are 16 bits. Consider 'l.d f6, -866(r2)'; where r2 contains the hexadecimal memory address FAFAFAFA. Write the (8-hexit) hexadecimal representation of the 32-bit memory address where the double-precision floating point number ***to be loaded in*** register '**f6**' will be fetched. Show your work.

Answer: __ __ __ __ __ __ __ __

b)) Assume 32-bit registers, instructions, and memory addresses. Immediates are 16 bits. Consider 'bne r1, r2, loop', loop is -288. PC is currently pointing to the hexadecimal memory address AFAFAFAF. Write the (8-hexit) hexadecimal representation of the memory address where the branch will go (the instruction where loop label is). Show your work.

Answer: __ __ __ __ __ __ __ __

6. [10 marks] MIPS code Implementation

The following MIPS code segment executes for several iterations before it stops. Before execution starts, register r1 contains the value 100, register r2 contains the value 156, and registers f4 and f6 are both initialized to zero. The initial memory content is shown below.

Required: Show the final memory content and the values of the registers r1, r2, f4 and f6 after execution stops.

```
Loop:  l.d     f4, 0(r1)
       l.d     f6, 8(r1)
       add.d   f6, f4, f6
       s.d     f6, 16(r1)
       addi    r1, r1, 8
       bne     r1,r2,loop
done: halt
```

Initial Memory Content

Memory Address (decimal)	Initial Memory Content (decimal)	Final Memory Content(decimal)
100	0	
108	1	
116	0	
124	1	
132	0	
140	1	
148	0	
156	1	

7. [20 marks] Memory Hierarchy and Cache

Suppose that we have a computer that uses a memory address of 12-bits. This computer has a 64-byte cache with 16 bytes per frame. The computer accesses a number of memory locations throughout the course of a running program. Suppose this computer uses direct-mapped cache. The system accesses the following memory addresses (given in hex) in this exact order: F2E, A17, 2E0, 44E, 34F, 341, B50, B58

a. What is the hit ratio for the memory reference sequence given above?
b. Show the content of each cache frame following each memory reference (frame content to be shown as tag +frame index)
c. If we keep the same cache size and the same frame size but switch to a **2-way set associative cache** mapping scheme. Given the memory address reference 555, indicate where we would look in the cache to find this data. Indicate which fields will be used to find the exact location?