COMP228-PP Winter 2017 Midterm

1. [20 marks] Digital Logic
'2!' is the ternary **'two'** connective. **'2! pqr'** is true iff precisely two of 'p', 'q', and 'r', are true. **'→'** is the binary conditional connective. **'p → q'** is true iff **'∼p ∨ q'**.
Let **S = {'2!','→'}**.
i) Synthesize **'T'** from **S**.

ii) Synthesize **'F'** from **S**.

iii) Synthesize '∼' from **R = {'2!','T','F'}**.

iv) Synthesize '∧' from **R.**

2. [15 marks] Amdahl's Law
The Exanet interconnection network contains gold wires, optical "wires"(photons),
and routers. Designers want a larger version, but are concerned about cost. In the current version, gold wires make up 45% of the cost, photons 0%, and routers 55%. The new version uses 15 times as many gold wires, and 25 times as many routers. Both items have constant unit cost.

a) The new version is _____ times more expensive.

Exanet's bisection bandwidth is given by [3 * (# of routers)$^{0.875}$] PWs/s.

b) The new version has _____times more bisection bandwidth.
R = # of Routes in original version.

c) The ratio Ws/s/$ has _____ (fallen/risen) by a factor of _____.
new Ws/s (BW2) = 16.72 * BW1
new $ ($2) = 20.5 * $1
BW2/$2 = 16.72/20.5 * BW1/$1 = 0.82
BW2/$2 = 0.82 * BW1/$1

3. [20 marks] Pipeline Information Flow
Consider our instruction-execution pipeline:
<f-box> | | <d-box> | | <x-box> | | <m-box> | | <w-box>

a) The f-box contains/creates two important values (bit patterns) that it makes available to the d-box. These are the _____and the _____.

b) When the d-box decodes **'add r1, r2, r3'**, the information it sends to the x-box is a _____, and the value(s) _____.

c) When the m-box acts on **'l.d f6, -24(r2)'**, it gets a _____from the _____, and the quantity _____from the _____.
d) The w-box is active precisely for those instructions that contain a _____.

4. [20 marks] Instructions with an immediate

a) Assume 32-bit registers, instructions, memory addresses, and adders, and 16-bit immediates. Consider **'s.d f4, 7420(r2)'**. What is the (8-hexit) hexadecimal representation of the 32-bit register that will be added to the base register **'r2'**? Hint: Do calculations in hexadecimal.

b) Assume 64-bit registers, instructions, memory addresses, and adders, and 16-bit immediates. Consider **'bne r1, r2, loop'**, where **'loop'** has the decimal value -3327. What is the (8-hexit) hexadecimal representation of the lowerorder 32 bits of the 64-bit integer that will be added to the base register **'PC'**? Hint: Do calculations in hexadecimal.

5. [25 marks] Fractional-Number Formats
A small computer has 16-bit registers. All numbers are positive, so no sign bit is required.

a) What is the (4-hexit) hexadecimal representation of the (8+8)-bit binary fixed-point format for 31.9? Do not round.

b) The floating-point format is: First four bits for the exponent, and the next 12 bits for the fractional part of the significand. What is the (4-hexit) hexadecimal representation of the 16-bit floating-point format for 7.9? Do not round.

c) Someone has half-converted rational number **'x'** to a fix-point format. So far, we have 'x = 0.<1101>*'. What is the exact value of 'x'? Express 'x' as a fraction reduced to its lowest terms.