COMP228-DD Winter 2017 Midterm

1. [20 marks] Digital Logic

'#' is the ternary majority connective. **'#pqr'** is true iff at least two of 'p', 'q', and 'r', are true. **'←'** is the reversed conditional. **'p ← q'** is true iff **'p** ∨ ∼**q'**. **'+'** is exclusive or. **'p + q'** is true iff 'p' and 'q' have opposite truth values. Let **S = {'#','←','+'}**.

i) Synthesize **'T'** from **S**.

ii) Synthesize **'F'** from **S**.

iii) Synthesize '∼' from **{'#','←','F'}**.

iv) Synthesize '∧' from **{'#','+','F'}**.

2. [15 marks] Amdahl's Law

The Exanet interconnection network contains gold wires, optical wires"(photons), and routers. Designers want a larger version, but are concerned about meeting the power-efficiency requirement, which is 100 words/s/watt. In the current version, gold wires dissipate 35 MWs of power, photons 0 MWs, and routers 105 MWs. The new version uses 17 times as many gold wires, and 13 times as many routers. Both items have constant unit power.

a) The new version dissipates _____ watts. Exanet's bisection bandwidth is given by [10 * (# of gold wires)$_{0.25}$ + 2.6 * (# of routers)$_{0.75}$] GWs/s. The original design has 300 gold wires and 10 routers.

b) The bisection bandwidth of the new version is _____ words/s.

c) The new version has a power efficiency of _____ words/s/watt, which _____ (does/doesn't) meet the power-efficiency requirement.

3. [20 marks] Pipeline Information Flow
Consider our instruction-execution pipeline:
<f-box> | | <d-box> | | <x-box> | | <m-box> | | <w-box>

a) In a pipeline, the f-box increments PC before the current cycle finishes because _____.

b) When the d-box decodes **'l.d f6, -24(r2)'**, the information it sends to the x-box is a _____, the quantity _____, and the value(s) _____.

c) When the d-box decodes **'mul.d f0, f2, f4'**, the register value(s) go to the _____, and register name(s) go to the _____.

d) When the m-box acts on **'s.d f6, -24(r2)'**, it gets a _____ and the value(s) _____from the _____, and the quantity _____from the _____.

4. [20 marks] Instructions with an immediate
a) Assume 32-bit registers, instructions, memory addresses, and adders, and 16-bit immediates. Consider **'s.d f4, 15536(r2)'**. What is the (8-hexit) hexadecimal representation of the 32-bit register that will be added to the base register **'r2'**? Hint: Do calculations in hexadecimal.

b) Assume 64-bit registers, instructions, memory addresses, and adders, and 16-bit immediates. Consider **'bne r1, r2, loop'**, where **'loop'** has the decimal value -3566. What is the (8-hexit) hexadecimal representation of the lowerorder 32 bits of the 64-bit integer that will be added to the base register **'PC'**? Hint: Do calculations in hexadecimal.

5. [25 marks] Fractional-Number Formats
A small computer has 16-bit registers. All numbers are positive, so no sign bit is required.
a) What is the (4-hexit) hexadecimal representation of the (8+8)-bit binary fixed-point format for 21.7? Do not round.

b) The floating-point format is: First four bits for the exponent, and the next 12 bits for the fractional part of the significand. What is the (4-hexit) hexadecimal representation of the 16-bit floating-point format for 3.7? Do not round.

c) Someone has half-converted rational number **'x'** to a floating-point format. So far, we have: i) the sign is '+', ii) the exponent is -4, and iii) the fractional part of the significand is '<1101>*'. What is the exact value of 'x'? Express 'x' as a fraction reduced to its lowest terms.