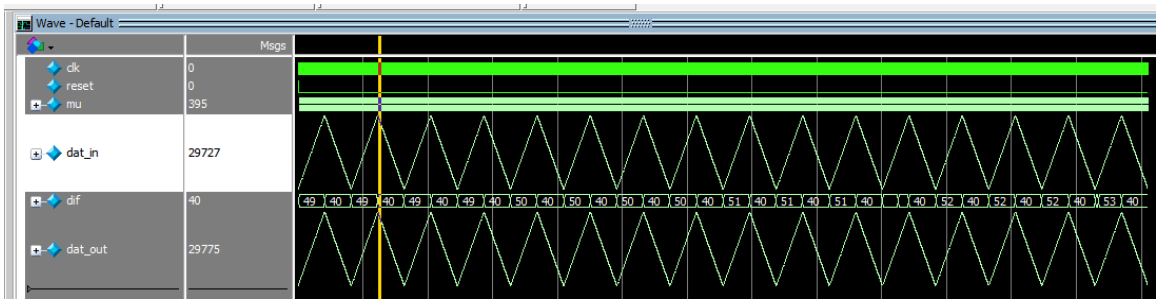
Kelvin Duong A15822315

ECE 260C Lab2

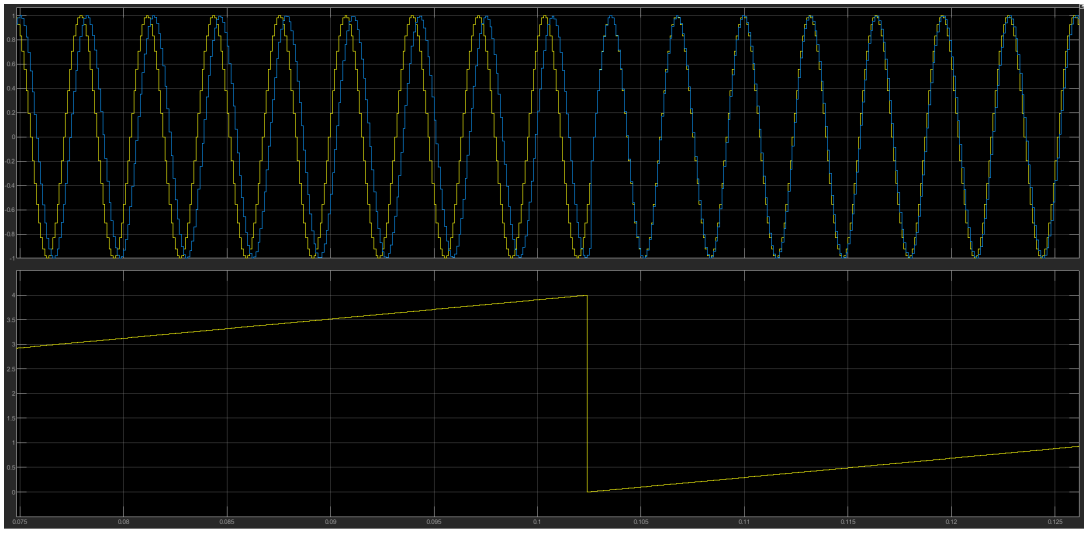
1-2 (provided code is already registered)

waveform using directly coded starte:



As you see the data out is a delayed version of input with variable differences between them

hdl_gen waveform



As you see the output waveform drifts further from the initial waveform then snaps back into sync

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fmax directly coded:

Slow 900mV 100C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	34.98 MHz	34.98 MHz	clk

fmax hdl_gen

Slow 900mV 100C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	24.43 MHz	24.43 MHz	clk

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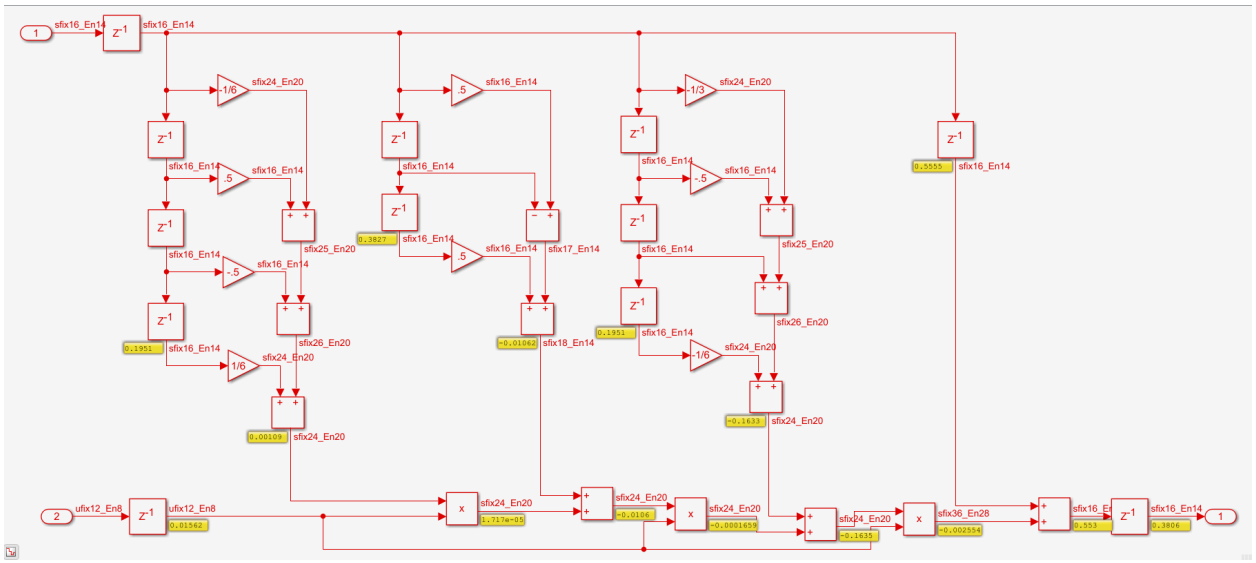
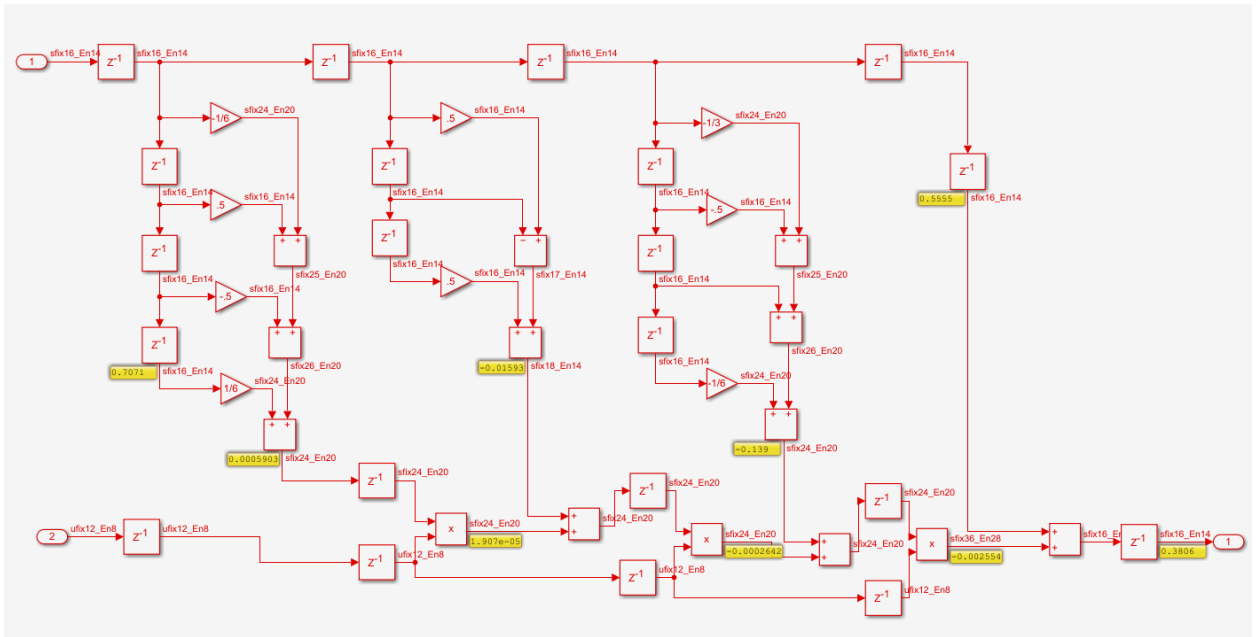
Originally the worst case slack was from Delay to Delay1, I added a pipeline register before each of the multiplies for improved fmax.

Provided:



pipelined (3 cycles afterwards)



You can see it is pipelined correctly as the final output is the same as the one without pipeline

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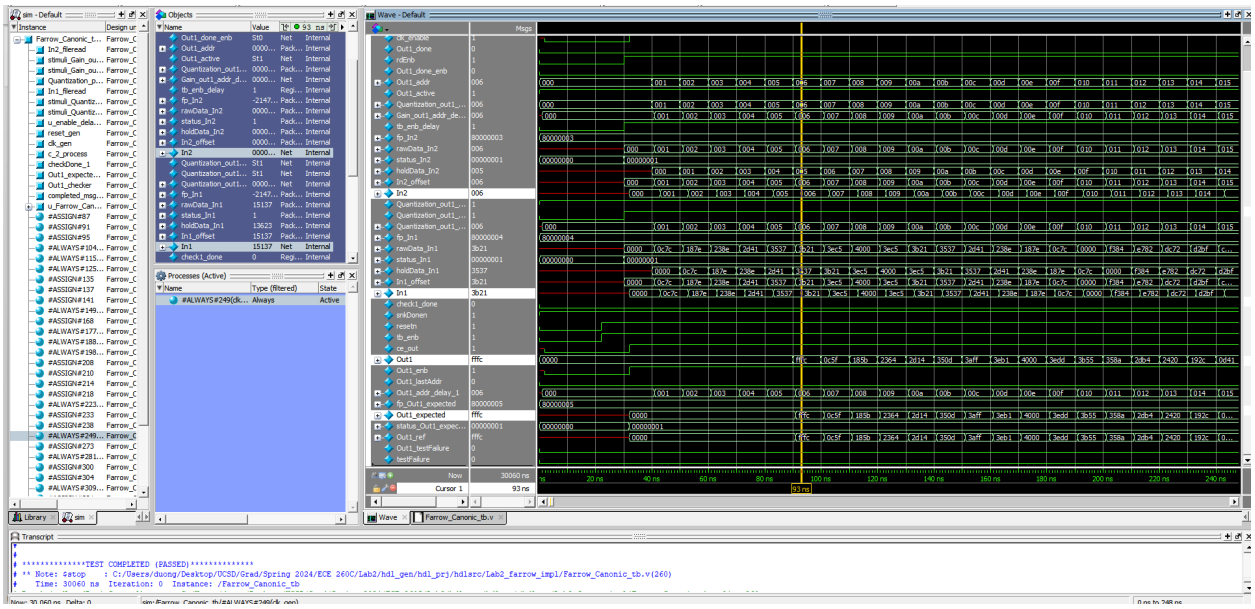
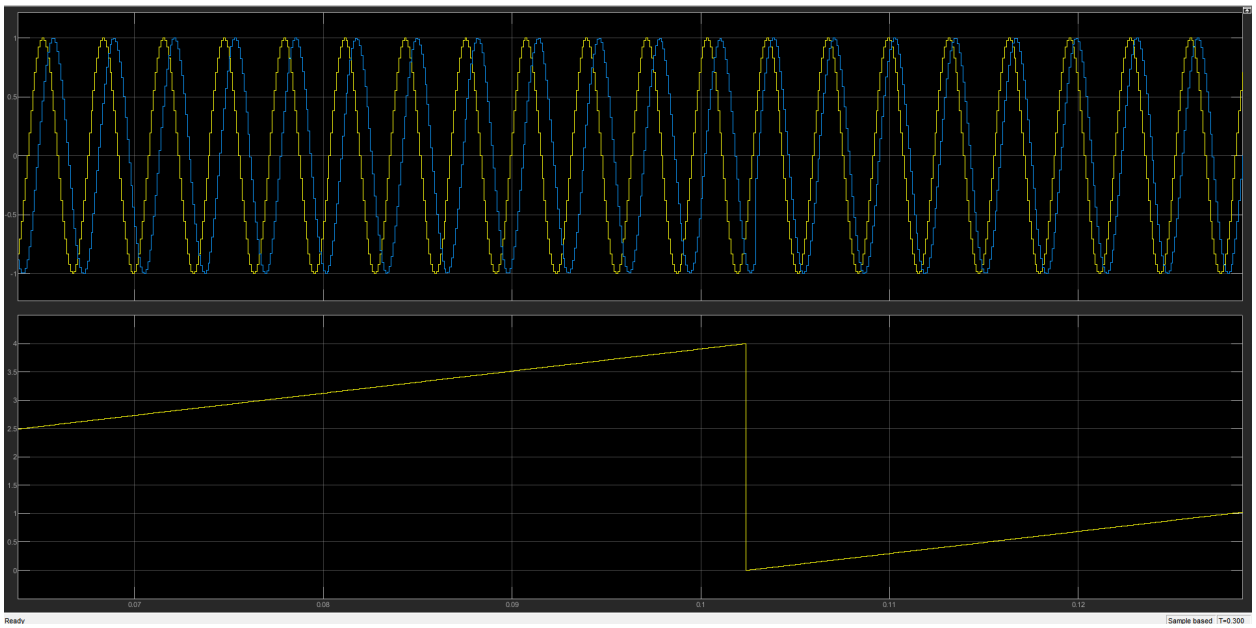
5. waveforms



As you see the actual output matches the expected, in terminal it verifies that it passes all test



You can see that in the simulink waveform the output waveform snaps from having a large offset from the input to a small offset from the input, this has the same behavior as the

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	Fmax	Restricted Fmax	Clock Name
1	83.51 MHz	83.51 MHz	clk

	Slack	From	To	Recommendations
1	-10.974	Delay_out1[1]	Delay7_out1[23]	Report recommendations for this path
2	-10.967	Delay_out1[1]	Delay7_out1[23]	Report recommendations for this path
3	-10.953	Delay_out1[1]	Delay7_out1[23]	Report recommendations for this path
4	-10.946	Delay_out1[1]	Delay7_out1[23]	Report recommendations for this path
5	-10.944	Delay_out1[1]	Delay7_out1[23]	Report recommendations for this path

As seen the new fmax is 83.51 Mhz which is over 3x better performance over the baseline hdl_generated. I only modified the simulink code but if this was done on the directly coded I would expect slightly higher fmax due to the directly coded being slightly more efficient.

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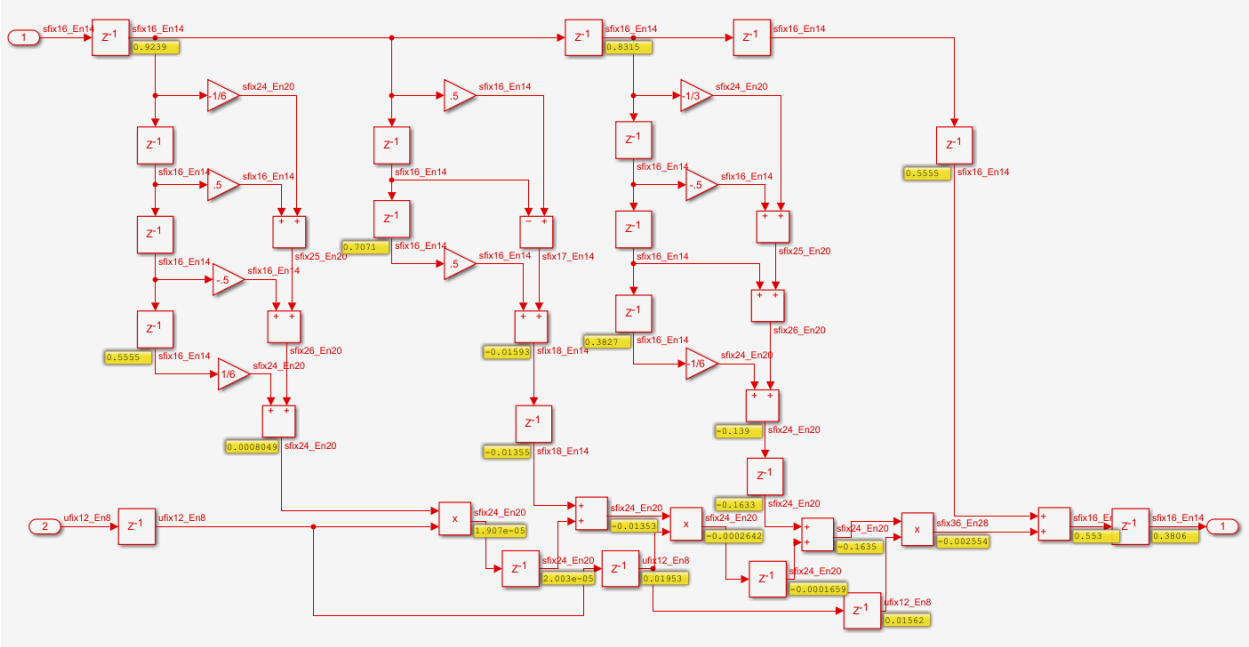
I added registers in various places in the circuit. I saw that I could improve the fmax very easily with this but I had to be careful to delay all parallel paths as to not disrupt the original arithmetic. Initially I did a 2-stage pipeline with a register in between multiply and add, I realized afterwards that this is less efficient than placing registers before the multiplication. The results of my first test are shown below with an fmax of 49.51 Mhz. With the pipeline before the multiplications as shown earlier I was able to achieve a 83.51 Mhz fmax which is significantly higher than the baselines.

other design



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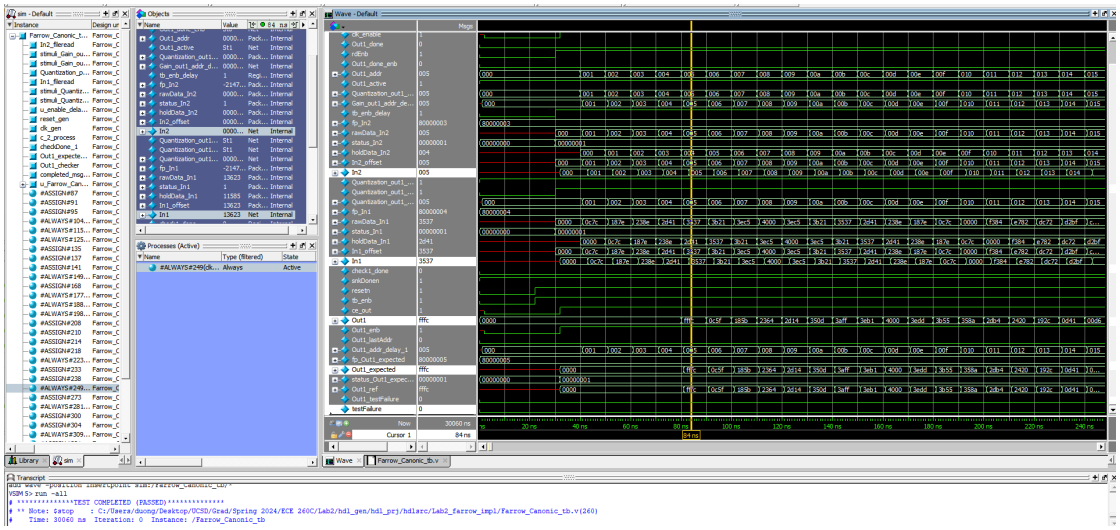

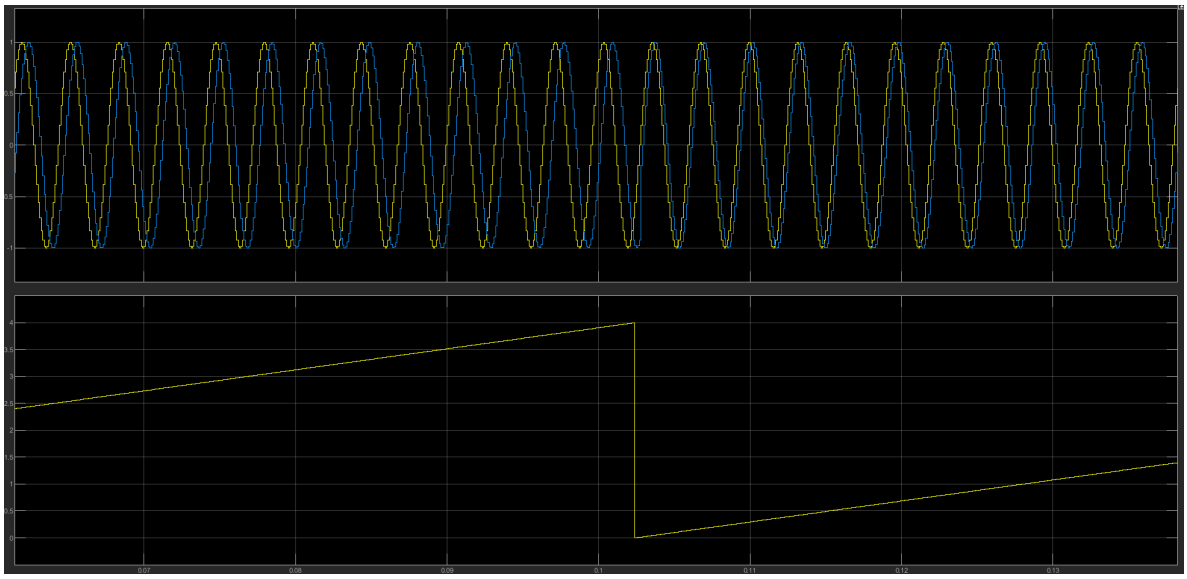

	Fmax	Restricted Fmax	Clock Name
1	49.51 MHz	49.51 MHz	clk

	Slack	From	To	Recommendations
1	-19.198	Delay_out1[7]	Delay7_out1[5]	Report recommendations for this path
2	-19.198	Delay_out1[7]	Delay7_out1[5]	Report recommendations for this path
3	-19.198	Delay_out1[7]	Delay7_out1[5]	Report recommendations for this path
4	-19.198	Delay_out1[7]	Delay7_out1[5]	Report recommendations for this path
5	-19.198	Delay_out1[7]	Delay7_out1[5]	Report recommendations for this path