Microcontroller (Notes 1)

Embedded Systems

Systems (electrical or electromechanical devices) controlled by Special purpose computer encapsulated inside it

Mechatronic systems

Systems in which mechanical hardware are integrated with information – driven systems (Micro-controllers)

n-bit processor

1-Processor works only on n-bit of data at a time
2-Data larger than n-bit has to be broken into n-bit pieces to be processed

SOC is the full system, often the computer on a chip, or at least that is the goal. They are very powerful compared to mere micro controllers. SOC may have large amount of memory, peripheral interfaces, radio/wireless connection.May be multicore.

Microcontrollers are processor chips with inbuilt peripheral components, ADC,DAC and some memory. Designing a system is easier with these than with a raw microprocessor.

L1 And L2

Most modern CPUs now have a cache memory **(L1)**, on the same silicon wafer as the CPU, to provide the CPU with instructions at the same clock speed as the CPU.

An additional off-the-chip secondary cache **(L2)** may also interact with the CPU at a slower speed.

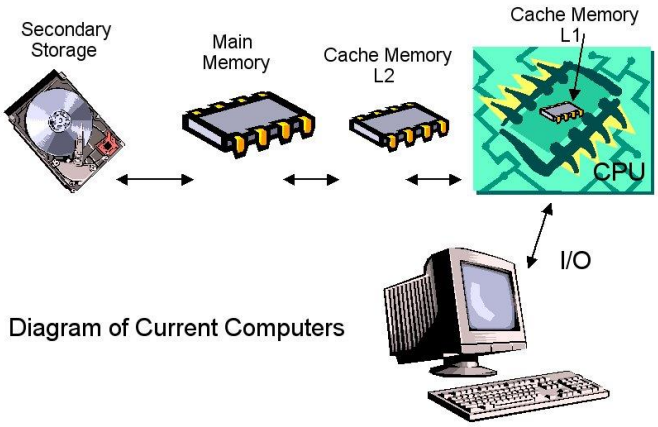
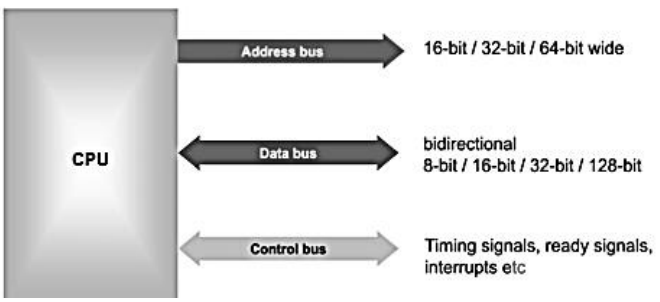
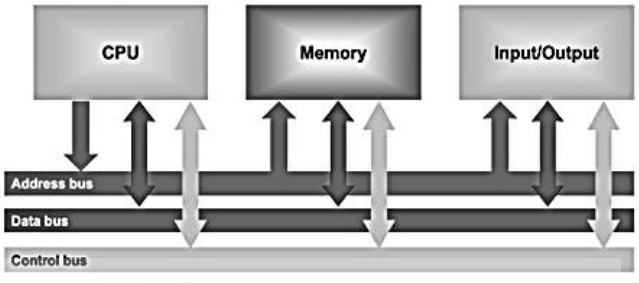
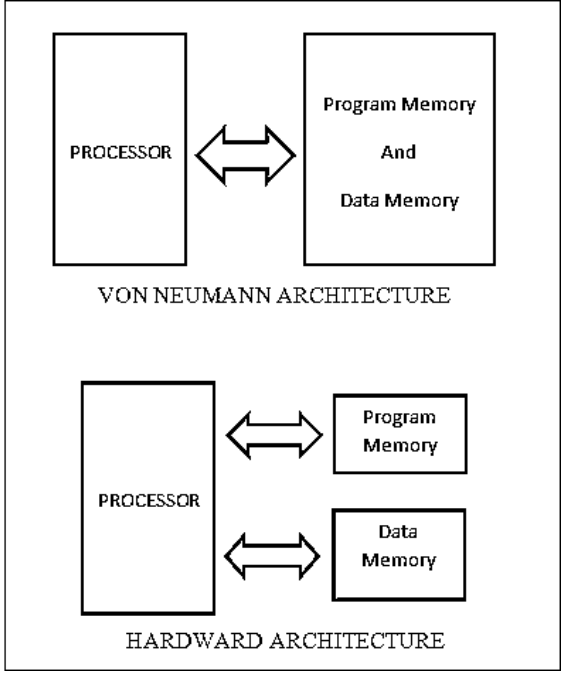


Diagram of Current Computers

Microprocessors are raw processors with minimal ALU+ registers without any peripheral components. You need to connect other chips to make it useful.







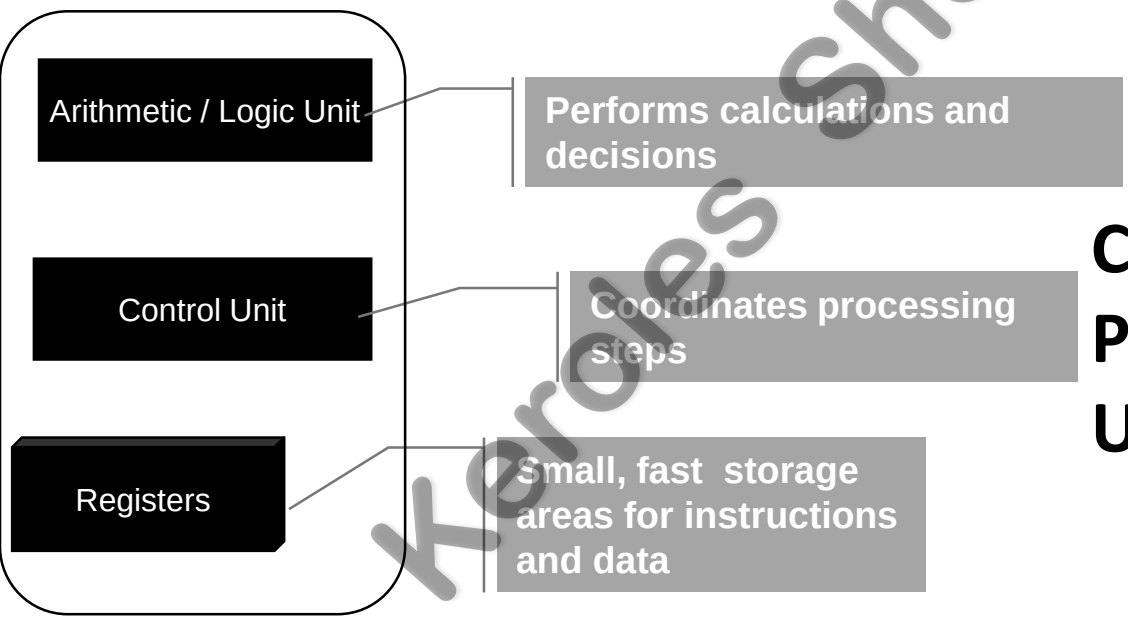
Von-Neuman Vs. Harvard Architecture

✓ ***Von-Neuman :***

1) Single common memory space where program instructions and data are stored
2) There is a single data bus fetches both instructions and data

✓ ***Harvard architecture***

1) Separate memory area for instructions and another are for data
2) One bus connects the CPU to the RAM and another connects the CPU to ROM



Central Processing Unit (CPU)

CISC	RISC
Used in laptops and desktop computers, made by Intel or AMD	Used in smartphones and tablets, based around ARM processor
Has more complex hardware	Has simpler hardware
Multiple machine cycles per instruction	Single machine cycle per instruction
Physically larger in size and require more silicon to make thus more expensive	Smaller in size as less complex circuity required, less silicon needed to make thus cheaper
Greater energy consumption	Lower energy requirements, and can go into "sleep mode" when not actively processing
More intensive tasks will do better with CISC	Run at lower clock speed, but can perform simpler tasks more quickly than CISC
Can't support pipelining	Can support pipelining

CPU Specific Registers

Location	Instruction
0	LOAD R0 1
1	ADD R0 1
2	WRITE 0 R0
3	READ R1 0
4	LOAD R2 4
5	COMPARE R0 R2
6	JUMPLT 2
7	EXIT
8	LOAD R1 4

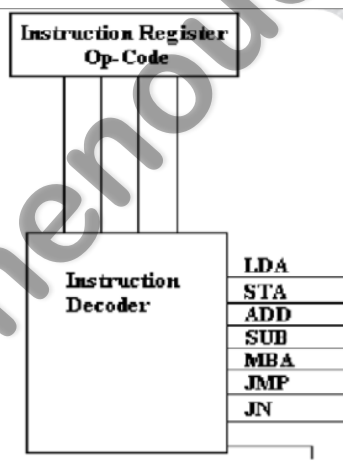
Program Counter	3

PC Program Counter Register

- Most important CPU register
- Holds the address of the next instruction in program memory space
- The size (width) of the program counter is directly related to the size of the µC's program memory

Instruction Register IR

- Contains the next instruction (Op-Code) to be decoded by the **Instruction Decoder**



Status Register (SREG)

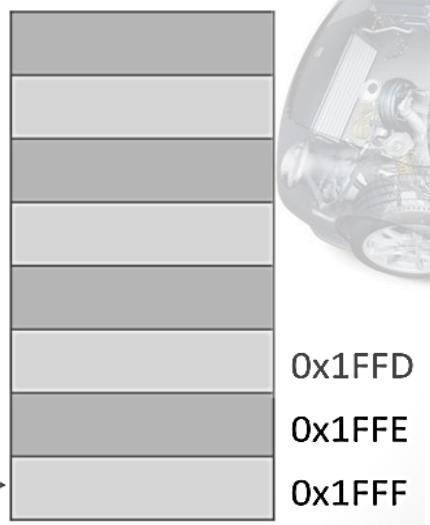
- Contains information about the result of the most recently executed instruction
  - Use to alter program flow on conditional operations
- NOT automatically stored when entering an interrupt routine
  - Must be handled by software

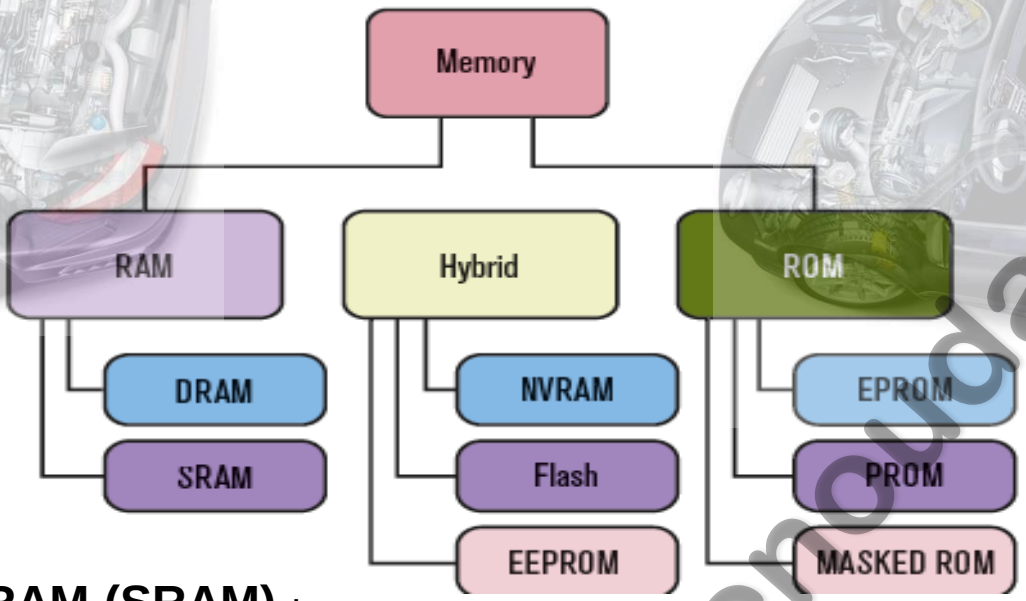
Instruction Decoder ID

- Takes Op-Code stored in the instruction register and decodes it then tells the CPU what to do for it and enable the components for this operation

STACK Pointer SP Register

- Used for storing temporary data
  - Local variables
  - Return addresses after interrupts or subroutine
- Implemented as growing from higher to lower address
  - Initial pointer set equal to last address of SRAM
- Push – decreases SP
- Pop – increases SP





- **Static RAM (SRAM)** :
  1) Storage cells are made of flip-flops and therefore don't require refreshing in order to keep their data
  2) The problem of flip-flops is that each cell requires at least 6 transistors to build and this cell hold only 1 bit
  3) The use of 4-transistor cells plus the use of CMOS technology give birth to a high-capacity SRAM but its capacity is so far below that of DRAM
- **Dynamic RAM** :
  1) It's lower than SRAM in price power consumption
  2) Using a capacitor to store data cuts down the number of transistors to build the cells
  3) The capacitors require constant refreshing due to charge leakage
  4) While DRAM is being refreshed , its data cannot be accessed in contrast to SRAM whose data can be accessed any time as it doesn't need refreshing
- **PROM(Programmable ROM):** It can be programmed only once.
  1) The kind of ROM that the user can burn information into
  2) For every bit , there is a fuse
  3) PROM is programmed by blowing the fuses
  4) The information can be burned into PROM only once , so it's called OTP(one-time programmable)
- **EPROM (Erasable ROM):** It can be programmed many times.An EPROM programmer is required to program the EPROM chip.

Can be programed and erased thousands of time
2) A widely used (EPROM) is called (UV-EPROM)
3) UV-EPROM has a window through which the programmer can shine ultra-violet radiation to erase its contents
4) To burn code into the UV-EPROM , the ROM burner uses 12.5 volts or higher
5) The major disadvantage with UV-EPROM is that it cannot be erased while it's in the system board

•Electrically Erasable Programmable ROM (EEPROM) :

1)It is similar to EPROM, but it can be erased electrically by applying an electrical signal to one of the pins.
2) In EEPROM , you can select the byte to be erased in contrast to UV-EPROM whose contents can be only entirely erased
3) It can be programmed while it's in the system board without the need of an external erasure or programming device
4) It's cost is higher than UV-EEPROM

•Non-Volatile RAM (NVRAM) :

It is a SRAM with battery backup so that the contents are not erased even if power is switched off. Its is very expensive but data access through it is fast.

1) It allows the CPU to read and write to it and when the power is off , the contents are not lost
2) It can retain its contents up to 10 years after turning off the power
3) It uses extremely power-efficient SRAM cells built out of CMOS
4) It uses internal lithium battery as a backup energy source
5) If the power to the Vcc pin falls bellow out of tolerance condition , the control circuitry switches automatically to its internal power source (the lithium battery)
6) Another type of the NVARM combines SRAM and EEPROM so that its content is written into the EEPROM when power is off and is read back from the EEPROM when power is restored.

•Flash Memory :

it is also a non - volatile memory, fast EEPROM. The main attraction of flash is that it can be erased one block at a time and programmed one bit at a time. Flash memory devices are high density, low cost, fast (to read but not to write), and electrically programmable. It is being extensively used for embedded systems that contain embedded OS and the application program such as handheld computers.

The erasure method is electrical so , it's referred to as flash EEPROM
2) In old flash EEPROM you can only erase the entire contents (not just specific byte)
3) In recent decades flash memory contents are divided into blocks where erasing is done block by block
4) It can be programmed while it's in the system board

Mask ROM

1) It's not a user programmable ROM
2) It's contents are only programmed by the IC-Manufacturer
3) Cheaper than other kinds of ROMs and is one-time programmable (OTP)

Static RAM	Dynamic RAM
➢ SRAM uses transistor to store a single bit of data	➢ DRAM uses a separate capacitor to store each bit of data
➢ SRAM does not need periodic refreshment to maintain data	➢ DRAM needs periodic refreshment to maintain the charge in the capacitors for data
➢ SRAM's structure is complex than DRAM	➢ DRAM's structure is simplex than SRAM
➢ SRAM are expensive as compared to DRAM	➢ DRAM's are less expensive as compared to SRAM
➢ SRAM are faster than DRAM	➢ DRAM's are slower than SRAM
➢ SRAM are used in Cache memory	➢ DRAM are used in Main memory

EPROM	EEPROM
✓ Exposure to ultraviolet light technique used to erase data.	✓ A voltage of 20V to 25V is applied to erase data.
✓ Selective erasing is not possible. All locations get erased.	✓ Selective erasing is possible. A particular locations can be erased.
✓ 10 to 15 mins. i.e. Long time required for erasing	✓ 10ms. i.e. A very short time required for erasing
✓ Less expensive	✓ More expensive

Memory type	Density	Speed	Size	Cost	Volatility
DRAM	**V.High**	Slow	**Small**	**V. Cheap**	Y
SRAM	Low	**V. fast**	Large	Costly	Y
ROM	**High**	**fast**	**Small**	**Cheap**	N
PROM	**High**	**fast**	moderate	**Cheap**	N
EPROM	**High**	V. Slow	Small	**Cheap**	N
EEPROM	Medium	V. Slow	Moderate	**Cheap**	N
Flash	**High**	**V. Slow**	**Small**	**Cheap**	N

Embedded System software developing Environment

✓ ***IDE which at least contains :***

1) Text editor to write and edit codes
2) Compiler , assembler and linker to build your code
3) Debugger to find and resolve errors
4) Corss compilation platform

✓ ***Simulator (SW)***

1) Takes (.hex) file and act as a specific ECU running this file
2) Some simulators can graphically simulate hardware such as proteus

✓ ***In-Circuit Emulator (ICE)***

1) HW device used to debug the embedded SW
2) Replace the ECU with a simulated equivalent providing full-control of all aspects of the ECU
3) An emulator can emulate a wide range of ECU families

✓ ***IN-Circuit Debugger (ICD)***

1) HW device that connects to the ECU via a JTAG interface
2) Allows the operation of the ECU to be monitored and controlled externally
3) Restricted to specific debugging capabilities in the ECU

Crystal

The CPU needs a clock source, and a crystal oscillator generates the clock. The Crystal is choose d based on the cock frequency of the processor. Micro-controllers provide an on chip oscillator and you connect an external crystal or ceramic resonator. The clock generation circuitry determines the various states of machine cycles.

Reset Circuit

It is generally built in the hardware to take care of any unforeseen problems. This circuit handles software handles software hang-ups, power supply failures, etc. The processor sends a status signal to this circuit periodically. If in case this signal is not received, it is an indicator that some thing is wrong, which is then reset by this circuit. Single chip solutions are also available.

Watchdog timer

Most of the embedded systems have no provision of resetting the processor in such cases a watchdog timer is used. It is set to a large value and is counted down. When value reaches zero, the processor resets. If things are fine and there is no need to reset the processor, the processor resets the watchdog timer to that large value again.