GND

C3 0.1uF C4 1.0uF

U3 RF System on Chip
1 GND
2 VDD
3 CE
4 CSN
5 SCK
6 MOSI/SIMO
7 MISO/SOMI
8 IRQ
VCC
U3 CE
U3 CSN
U3 CLK
U3 SIMO
U3 SOMI
U3 IRQ
RFM75

VCC
C1 Cap 0.1uF   C2 Cap 1uF
GND

U1
1 XOUT   CAP3.3 32
2 XIN   CAP/P3.2 31
3 DVSS   CAP3.1 30
4 DVCC   P2.7/CAP3.0 29
5 !RST   CAP2.3 28
6 TEST   CAP2.2 27
7 P1.4   CAP2.1 26
8 P1.5   CAP2.0 25
9 P1.6   VREG 24
10 P1.7   P2.6/CAP1.3 23
11 P1.0   P2.5/CAP1.2 22
12 P1.1   P2.4/CAP1.1 21
13 P1.2   P3.1/CAP1.0 20
14 P1.3   CAP0.3 19
15 P2.2   P2.3/CAP0.2 18
16 P3.0/CAP0.0 CAP0.1 17
MSP430FR2633IDA

!RST
TEST

U3 CE
U3 IRQ
U2 GSCLK
U3 CSN
U3 CLK
U3 SIMO
U3 SOMI

U2 SIMO
U2 SOMI
U2 CLK
U2 LAT

VCC
R6 Res1 47k
!RST
C6 Cap 0.1u
GND

captouch
B1 Captouch
(i) captouch

VCC
P0
1
2
3
4
Header 4
GND
!RST
TEST

VCC
C5 Cap 0.1uF
GND
GND
R2 Res3 ??K

U2 LED Controller
1 GND   VCC 24
2 SIN   IREF 23
3 SCLK   SOUT 22
4 LAT   GSCLK 21
5 OUT0   OUT15 20
6 OUT1   OUT14 19
7 OUT2   OUT13 18
8 OUT3   OUT12 17
9 OUT4   OUT11 16
10 OUT5   OUT10 15
11 OUT6   OUT9 14
12 OUT7   OUT8 13
TLC5948ADBQ

U2 SIMO
U2 CLK
U2 LAT

U2 SOMI
U2 GSCLK

VCC
DSR
10 g
9 f
7 a
6 b
5 DP
4 c
2 d
1 e
A 3
A 8
Dpy Yellow-CA

VCC
DSL
10 g
9 f
7 a
6 b
5 DP
4 c
2 d
1 e
A 3
A 8
Dpy Yellow-CA

VCC
R1 Res2 1
BT1 Battery
GND

Captouch

Title

Size A
Number
Revision
Date: 7/23/2023
File: D:\Dropbox\..\2023_Clippy.SchDoc
Sheet of
Drawn By:

Design Rules Verification Report

Filename : D:\Dropbox\PCB Projects\DEFCON2023\2023 Lanyard Clippy\PCB1.PcbDoc

Warnings 0
Rule Violations 1
Waived Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=200mil) (OnLayer('Mechanical 1')),(InNet('GND'))	0
Clearance Constraint (Gap=30mil) (HasFootprint('CAPHEART')),(InNet('GND'))	0
Clearance Constraint (Gap=10mil) (All),(All)	0
Clearance Constraint (Gap=20mil) (IsRegion),(All)	0
Clearance Constraint (Gap=30mil) ((InNamedPolygon('Bottom Layer-GND') OR InNamedPolygon('Top	0
Clearance Constraint (Gap=20mil) ((InNamedPolygon('Bottom Layer-GND') OR InNamedPolygon('Top	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=1mil) (Max=150mil) (Preferred=10mil) (InNet('No Net') And OnLayer('Top Layer'))	0
Width Constraint (Min=6mil) (Max=10mil) (Preferred=8mil) (InNetClass('captouch'))	0
Width Constraint (Min=1mil) (Max=200mil) (Preferred=10mil) (All)	0
SMD To Corner (Distance=6mil) (All)	0
SMD To Plane Constraint (Distance=0mil) (All)	0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Allowed) (Ignore First Corner = Allowed)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Power Plane Connect Rule(Relief Connect)(Expansion=10mil) (Conductor Width=60mil) (Air Gap=25mil) (Entries=4)	0
Hole Size Constraint (Min=11.811mil) (Max=100mil) (All)	1
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=50mil) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=10mil) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) ((OnLayer('Top Overlay') OR OnLayer('Bottom Overlay')))	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	1

Waived Violations	
Clearance Constraint (Gap=10mil) (All),(All)	1
Total	1

Hole Size Constraint (Min=11.811mil) (Max=100mil) (All)
Hole Size Constraint: (175mil > 100mil) Pad Free-0(-10mil,1720mil) on Multi-Layer Actual Hole Size = 175mil

Clearance Constraint (Gap=10mil) (All),(All)
Clearance Constraint: (8.642mil < 10mil) Between Arc (47.224mil,717.5mil) on Bottom Layer And Pad U2-2(121.221mil,692.5mil) on Bottom Layer Waived