



Welcome to the

Jülich Supercomputing Centre

N. Attig, D. Rohe Jülich Supercomputing Centre (JSC), Forschungszentrum Jülich



Schedule: Thursday, November 23

13:00 – 13:30	Welcome and Introduction of JSC Norbert Attig (JSC)
13:30 – 14:50	JURECA: An Overview – P. Thörnig, C. Paschoulas (JSC)
14:50 – 15:20	Break
15:20 – 16:00	JURECA – Tuning for the platform – part I F. Robel (ParTec)
16:00 – 16:30	Using GPU accelerators on JURECA W. Homberg (JSC)
16:30 – 17:30	JURECA – Tuning for the platform – part II Heinrich Bockhorst (Intel)
17:35	Bus SB20 from Seecasino to Rurtalbahn and Aachen/Jülich



Schedule: Friday, November 24 (morning)

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08:45 – 10:00 HPC Software – Compiler and Tools M. Knobloch (JSC)
10:00 – 10:15 Break
10:15 – 10:45 HPC Software – Math Libs & Application Software I. Gutheil (JSC)
10:45 – 11:15 Remote Visualization – H. Zilken (JSC)
11:15 – 12:00 Uniform Resource Access at JSC UNICORE – B. Hagemeier (JSC) LLView – C. Karbach (JSC)
12:00 – 13:00 Lunch break
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Schedule: Tuesday, May 23 (afternoon)

13:00 – 13:30	JURECA Booster – Intro, D. Krause (JSC)
13:30 – 14:45	JURECA Booster – Tuning and Tweaks
	Heinrich Bockhorst (Intel)
14:45 – 15:15	Break
15:15 – 16:30	Taming Wild Threads – Tips and Pitfalls in Hybrid
	Programming, Christoph Pospiech, Lenovo/IBM
16:30	End of Day 2
16:35	Bus 219 from Seecasino to Rurtalbahn
16:47	Bus SB 20 from Seecasino to Aachen/Jülich



Organisational Information

- List of participants -> after coffee break
- Slides of all talks are available after the course at
 - http://www.fz-juelich.de/jsc, English
 Expertise Services Documentation Presentations
- WLAN access
 - Eduroam
 - Temporary access, forms will be handed out
- More workshops and conferences on JSC website: www.fz-juelich.de/ias/jsc/events
- Twitter: @fzj_jsc, @fzj_jscuser





Jülich Supercomputing Centre

Introduction

N. Attig

Jülich Supercomputing Centre (JSC), Forschungszentrum Jülich



Jülich Supercomputing Centre

Supercomputer operation for:

- Centre FZJ
- Region RWTH Aachen University
- Germany Gauss Centre for Supercomputing
 John von Neumann Institute for Computing
- Europe PRACE, EU projects

Application support

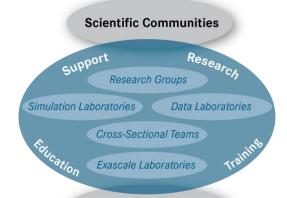
- Unique support & research environment at JSC
- Peer review support and coordination

R&D work

- Methods and algorithms, computational science, performance analysis and tools
- Scientific Big Data Analytics with HPC
- Computer architectures, Co-Design Exascale Labs together with IBM, Intel, NVIDIA

Education and training





Supercomputing Facility







Access to Supercomputing Resources at Jülich

- Access to JURECA via
 - JARA-HPC Vergabegremium (VGG) and/or Kommission zur Vergabe von SC Ressourcen (VSR) (for FZJ and RWTH staff members only; JARA-HPC Partition)
 - John von Neumann Institute for Computing (NIC)
- Access to JUQUEEN via
 - JARA-HPC Vergabegremium (VGG) and/or Kommission zur Vergabe von SC Ressourcen (VSR) (for FZJ and RWTH staff members only; JARA-HPC Partition)
 - Gauss Centre for Supercomputing (GCS)
 (JUQUEEN CPU time proposals are evaluated by NIC)
 - European Research Infrastructure PRACE
 - Project Access: Biannual CfPs since June 2010
 - Call for preparatory access open, no closing dates



Gauss Centre for Supercomputing (GCS)

A German Success Story:

GCS is the leading Tier-0 HPC centre in Europe

- Alliance of the three German Tier-1 centres
- Jülich Supercomting Centre (JSC)
- High Performance Computing Centre Stuttgart (HLRS)
- Leibniz Rechenzentrum (LRZ), Garching

Key Facts

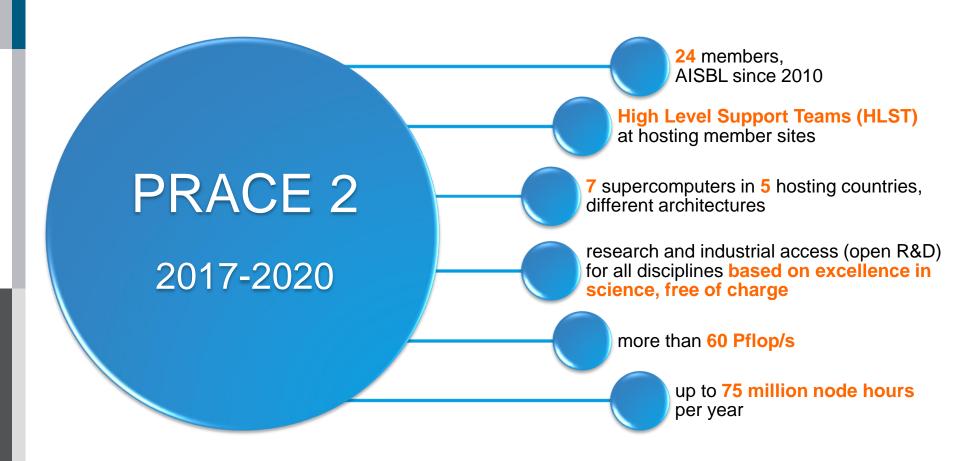
- To date in sum more than 20 Petaflops (continuously expanding)
- 400 people for Operation, HPC-research, Services, Training
- Extensive know-how in key scientific fields





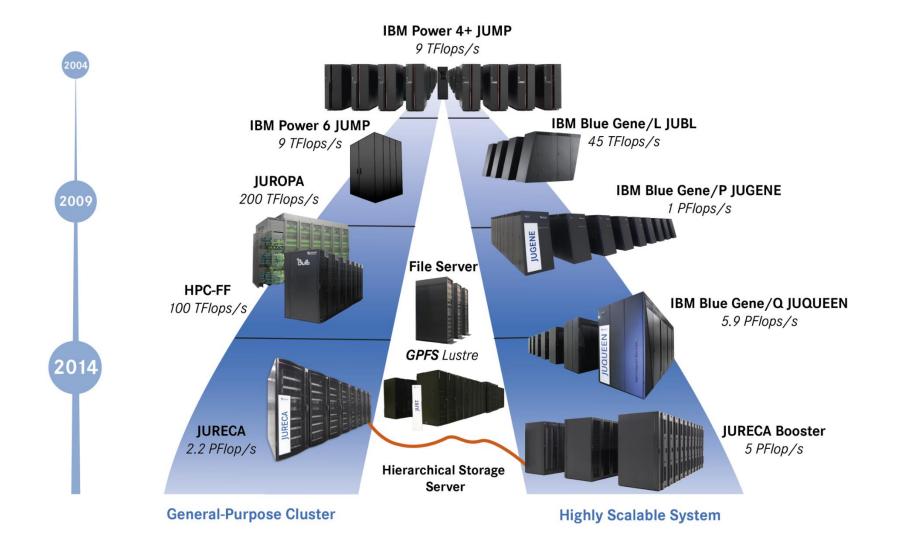


PRACE - Partnership for Advanced Computing in Europe The European HPC e-infrastructure (ESFRI)



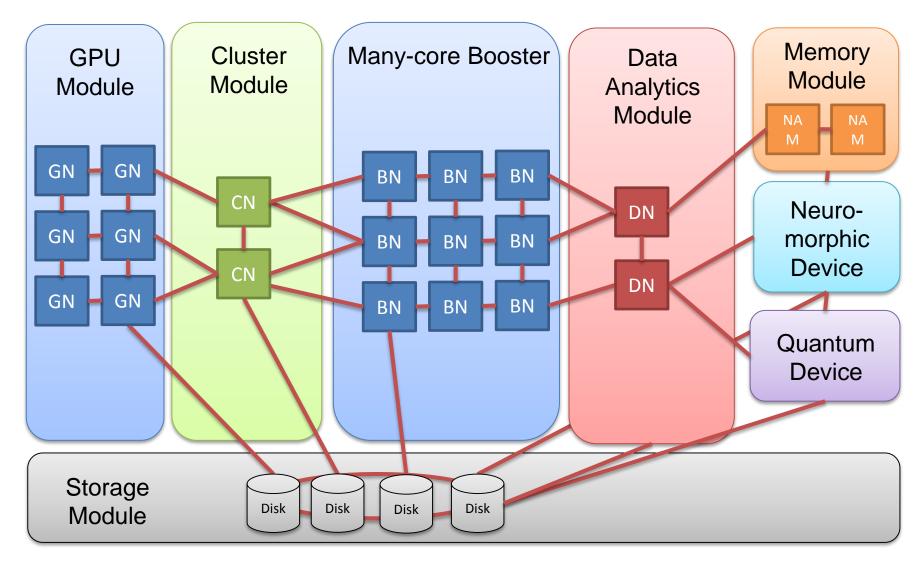


Dual Hardware Strategy at FZJ ...





... and Evolution to Modular Supercomputer Architecture





JUQUEEN: Jülich's Scalable Petaflop System

IBM Blue Gene/Q JUQUEEN

- IBM PowerPC® A2 1.6 GHz, 16 cores per node
- 28 racks, 458,752 cores
- 5,9 Petaflop/s peak5,0 Petaflop/s Linpack
- 448 TByte main memory



- 5D network
- Production start: Nov 5, 2012





JURECA: Jülich Research on Exascale Cluster Architectures

JURECA Cluster

- 2 Intel Haswell 12-core processors,
 2.5 GHz, SMT, 128 GB main memory
- 1,884 compute nodes or 45,216 cores, thereof
 75 nodes with 2 K80 NVIDIA graphics cards each and
 12 nodes with 512 GB main memory and 2 K40 NVIDIA graphics cards each for visualisation
- 2.245 Petaflop/s peak (with K80 graphics cards)
 1.425 Petaflop/s Linpack from CPUs (out of 1,693 Petaflop/s peak)
- 281 TByte memory
- Mellanox Infiniband EDR
- Connected to the GPFS file system on JUST



JURECA (II)

JURECA Booster

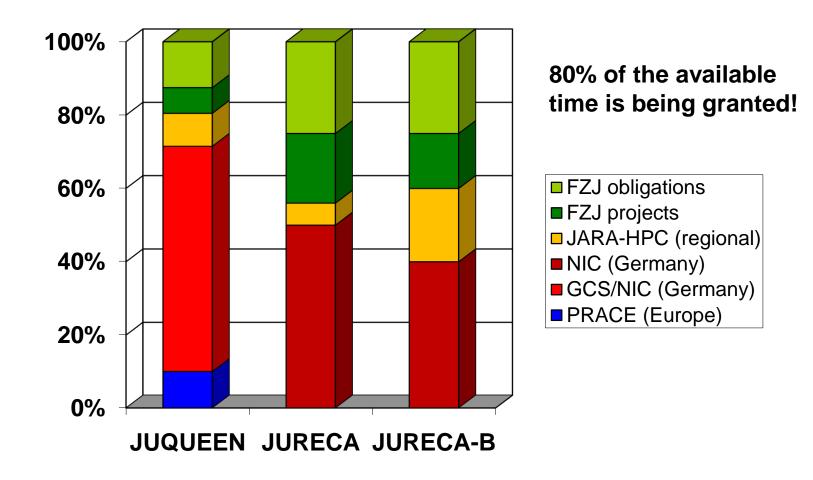
- Intel Xeon Knights Landing
- 1,640 compute nodes with 68 cores each
- 96 GiB memory per node plus 16 GiB MCDRAM high-bandwidth memory per node
- Shared login infrastructure with the cluster module
- Intel Omni-Path Architecture high-speed network with non-blocking fat tree topology
- 100+ GiB per second storage connection to JUST
- 5 Petaflop per second peak performance

JURECA Cluster & Booster: #29 worldwide (3,78 Petaflop/s Linpack)



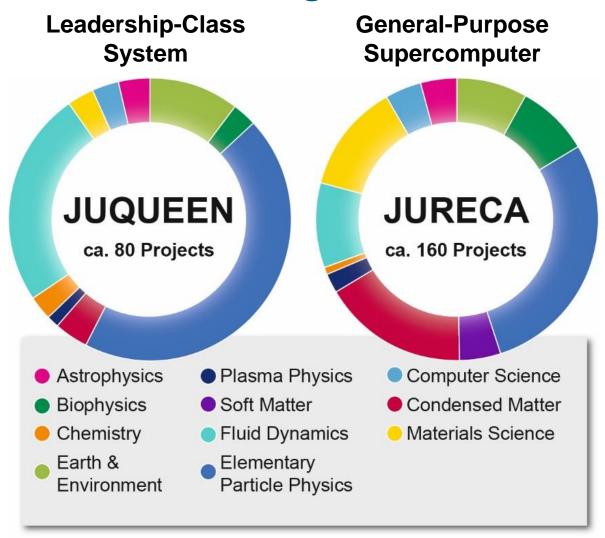


Stakeholder's Compute Time Shares





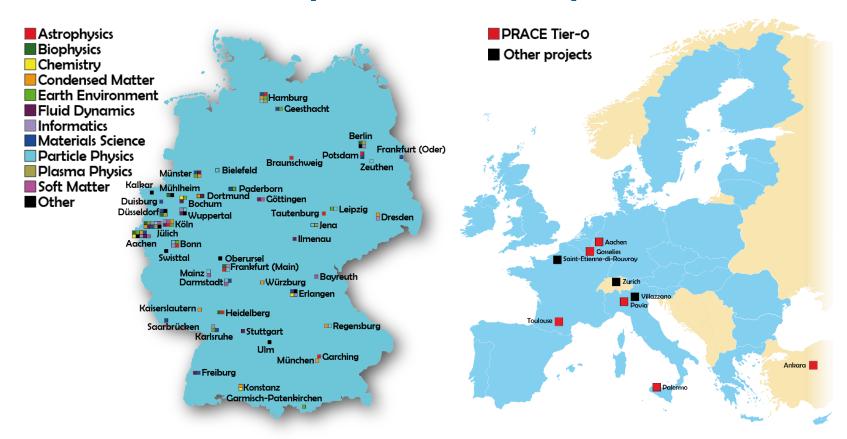
Research Field Usage 05/2017-04/2018



Granting periods 11/2017 – 10/2018 05/2017 – 04/2018



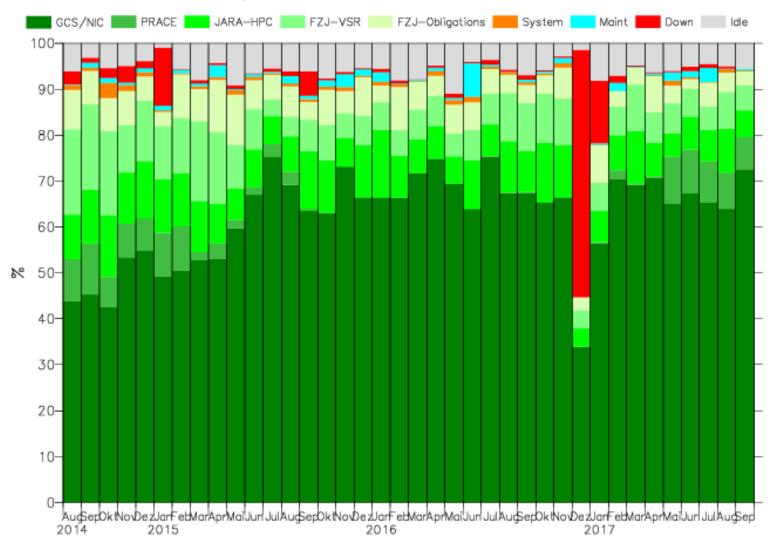
National and European User Groups



- Proposals for computer time accepted from Germany and Europe
- Peer review by international referees
- CPU time is granted by independent Scientific Councils

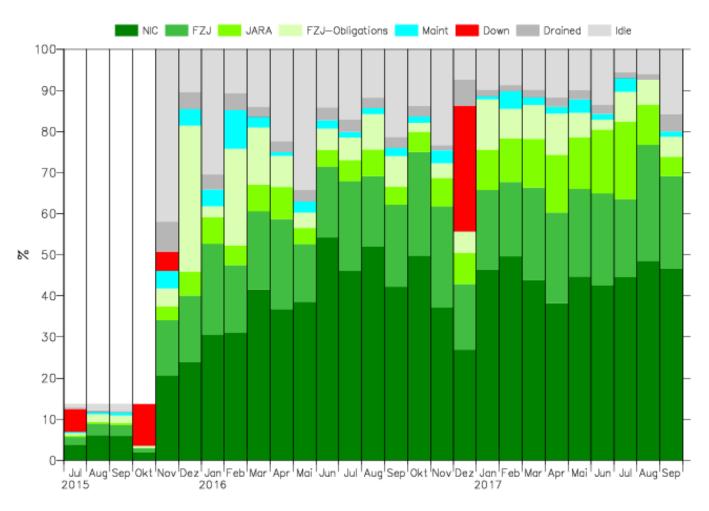


JUQUEEN Usage





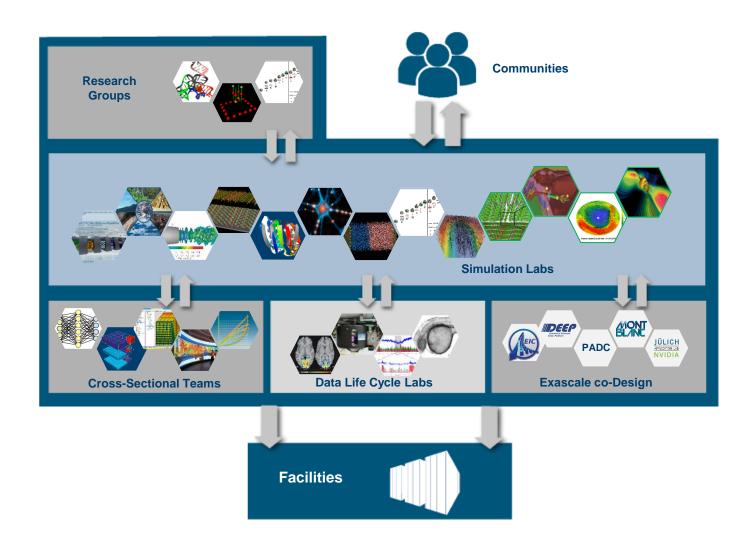
JURECA Usage



Launch of JURECA, phase 1, 260 nodes: Jul 13, 2015 phase 2, 1,884 nodes: Nov 02, 2015



Support and Research Landscape at JSC





Summary

- The Jülich Supercomputing Centre provides
 - Tier-0/1 HPC resources
 - high-end primary and domain-specific user support
 - · ...

to German and European research groups working in the computational sciences and in engineering

- JSC expects to see
 - breakthrough science
 - parallel applications, using a substantial number of processors simultaneously



End of Presentation