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An Ultra Low-Voltage and Low-Power OTA Using Bulk-Input Technique and Its Application in Active-RC Filters

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Abstract

This paper presents the design of a two-stage bulk-input pseudo-differential operational transconductance amplifier (OTA) and its application in active-RC filters. The OTA was designed in 90 nm CMOS process and operates at a single supply voltage of 0.5 V. Using a two-path bulk-driven OTA by the combination of two different amplifiers the DC gain and speed of the OTA is increased. Rail-to-rail input is made possible using the transistor's bulk terminal as in input. Also a Miller-Feed-forward (MFF) compensation is utilized which is improved the gain bandwidth (GBW) and phase margin of the OTA. In addition, a new merged cross-coupled self-cascode pair is used that can provide higher gain. Also, a novel cost-effective bulk-input common-mode feedback (CMFB) circuit has been designed. Simplicity and ability of using this new merged CMFB circuit is superior compared with state-of-the-art CMFBs. The OTA has a 70.2 dB DC gain, a 2.5 MHz GBW and a 70.8° phase margin for a 20 PF capacitive load whereas consumes only 25 μw. Finally, an 8th order Butterworth active Biquadrate RC filter has been designed and this OTA was checked by a typical switched-capacitor (SC) integrator with a 1 MHz clock-frequency.

Keywords: Operational Transconductance Amplifier (OTA), Common-Mode Feedback (CMFB), Bulk-Input, Switched-Capacitor (SC) Integrator, Miller-Feed-Forward (MFF)

1. Introduction

There are growing strong demands for low-voltage supply and low-power consumption circuits and systems. This is especially true for very high integration level and very large scale integrated (VLSI) mixed-signal chips and system-on-a-chip. In mixed-signal systems, the analog circuits are combined with digital circuits in order to get the best performance with low-voltage supply and low-power consumption. This combination should be in an optimal way and the optimization process is application dependent. Also modern portable applications such as medical devices and remote wireless sensors require extending the battery life as well. This trend has forced designers to develop new approaches more amenable to low-voltage and low-power integrated circuits and it poses lots of challenges for all involved such as processes, devices, circuits, and system architectures [1]. Operational transconductance amplifiers (OTAs) are the key active building blocks of continuous-time filters. They can be generally classified into single ended, fully differential and pseudo-differential OTAs. Fully differential OTAs are preferred because they provide larger signal swing, better distortion performance, better CM noise and supply noise rejection. The main drawback of using fully differential OTAs is that a common-mode feedback (CMFB) circuit must be added. The principle of the CM control circuit can be easily applied to the design of differential structures, and it is well suited for low-voltage pseudo-differential architectures. This extra circuit is used to establish the common-mode output voltage and suppress the common mode signal components [2]. The speed of the common-mode path should be comparable to that of the differential path; otherwise the common-mode noise may be significantly amplified such that the output signal becomes distorted. Also, the CMFB circuit is often a source of noise injection and increases the load capacitance that needs to be driven. Regardless of the limitations described above, fully differential OTAs work very well and can substantially im-

prove the system's quality, especially in very unfriendly environments such as mixed-mode applications. However, at lower supply voltages, pseudo differential OTAs could be used to avoid the voltage drop across the tail current source used in the fully differential structures. Taking the tail current source achieves a larger signal swing, but it also results in larger CM gain. So it requires to carefully controlling the CM response for pseudo differential OTAs. The reduced supply voltage will cause many problems when designing analog circuits due to the reduction in available signal swing. This problem is magnified due to the fact that the threshold voltage (V_T) of the transistors has been reduced at a slower rate than the supply voltage. In other words, the threshold-voltage with decreasing the Power supply never reduces linearly. If standard analog design techniques continue to be used, the dynamic range and SNR of the circuits will degrade. The gain of devices such as amplifiers will also decrease because cascode transistors can no longer be used since they limit the output swing. The design of rail-to-rail input circuits is also made more difficult due to the large V_T which must be overcome. One solution for designing low-voltage analog circuits is to operate the transistors in the weak inversion region. The drawbacks to this technique include a limited input signal swing, an increase in the mismatch between transistors, a low slew-rate due to the low bias current levels, and large transistor sizes [3-6]. In order to avoid these drawbacks a bulk-input technique can be used, which allows for operation in the moderate inversion region at supply voltages equal to the V_T of the technology. The voltage applied to the bulk actually reduces the threshold voltage of the transistor, which increases the inversion level. One drawback of the bulk input technique is that the input transistor must sit in an n-well or p-well, so that its bulk is separate from the bulk of the rest of the transistors. This is not a problem in advanced technologies, which make use of triple well structures. In triple-well processes both the NMOS and PMOS can have isolated bulk terminals [5]. This paper presents the design of a novel two-stage bulk-input pseudo differential OTA, which operates at a supply voltage of 0.5 V. The circuit was designed using the 90 nm process in digital CMOS technology. Design procedure for this new merged OTA structure such as main OTA, CMFB and bias circuits are introduced in Section 2. In Section 3, SC integrator and active RC filter design are described. Section 4 presents simulation results. Finally, conclusions and acknowledge are given in Section 5 and 6, respectively.

2. Bulk-Input OTA Circuit Design

2.1. Main Amplifier

A basic body-input stage, capable of operating with very low supply voltage is depicted in **Figure 1**. This structure is a two-path OTA built by the combination of the two different amplifiers. In this circuit a PMOS body-driven OTA is implemented due to the action of M_{1+}, M_{1-}, M_{4+} and M_{4-}, and also a current-mirror bulk-input OTA is composed by transistors M_{2+}, M_{2-}, M_{3-} and M_{3+}. The OTA input consists of two bulk-input split differential pairs; some of the ac current generated by the input transistors is injected to the output transistors, providing a fast path for the current. The other part of the current is delivered to the current mirrors of M_{3+} and M_{3-}. These are the main transistors which the main portion of the currents by the factor n transfer to output transistors of M_{4+} and M_{4-}. If we suppose M_{4+} and M_{4-} have equal effective voltage to M_{1+} and M_{1-}, their transconductances are very much greater than bulk- transconductance of M_{1+} and M_{1-} ($g_{m4} >> g_{mb1}$). It is possible to utilize common-source amplifier which is parallel and in same phase with M_1 when the input signal is implied to the gate of M_4 via feed-forward (FF) compensate capacitor C_{ff} (not shown in **Figure 1**). Moreover, the transistor of the active load current source operates like a common source amplifier. This structure increases the gain and speed of the OTA. M_{3+} and M_{3-} with diode connections utilize for M_{4+} and M_{4-} biasing and use in M_{2+} and M_{2-} as a differential loads.

To further improve the differential gain PMOS devices (M_{5+}, M_{6+} and M_{5-}, M_{6-}) are added. The body-inputs of them are a new merged cross-coupled self-cascode pairs that adds a negative resistance to the output in the form of g'_{mb6} and boosts the differential DC gain. The g'_{mb6} is the g_{mb} of the self-cascode configuration of M_5, M_6. Also, the gate inputs biased at 100 mV, which biases them in moderate inversion. Moreover, these transistors are a self-cascode active load for transistors M_{4+} and M_{4-} which are common source amplifiers.

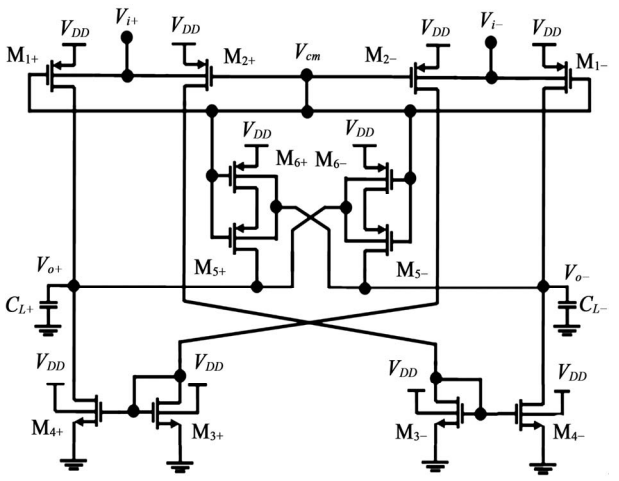

Figure 1. One stage of proposed bulk-input differential pair.

2.2. Bulk-Mode Common-Mode Feedback Circuit

The Fully differential OTAs require a common-mode feedback circuit. A CMFB circuit should behave linearly and only response to common-mode voltage. Lacking these features causes increase the THD of the circuit. Nowadays, designing a CMFB circuit which is able to operate under an ultra low-voltage supply is very difficult, mainly because of the difficulty of detecting of CM voltage. In Reference [5] a CMFB circuit which operated at 0.5 V by using two resistors to sense the output CM levels was designed. But this structure increases the die area and reduces the gain due to longer loads the OTA. To overcome some of these problems, a CMFB circuit has been reported [6]. This structure uses of four PMOS and two NMOS transistors. The NMOS devices is a bulk-input current mirror, which compares the current of the PMOS devices and then difference of these current is fed to the gate of the input transistors for controlling of the output CM voltages. This paper is given a novel continuous-time CMFB circuit that is able to operate with an ultra low-voltage supply. **Figure 2** shows the proposed CMFB circuit for each stage.

In this circuit, a combination of two complementary NMOS and PMOS transistors is used in a bulk-driven configuration. The output voltage of the CMFB circuit can be found using the KCL at the output node (V_{cm}). The difference between currents of PMOS and NMOS transistors is fed to the gate of the input transistors of OTA. The bulks of the PMOS devices M_{cp+} (M_{cp-}) connected to the NMOS devices M_{cn+} (M_{cn-}) and are utilized to maintain the output common voltage at the required level (250 mV), while maximizing the output swing of the OTA. In other words, the inputs to the CMFB circuit are the outputs of the OTA, V_{o+} and V_{o-}. The CMFB circuit amplifies the difference between the average of V_{o+} and V_{o-} and the desired common level V_{cm} (250 mV), and sends a feedback signal V_{cm} to set the bias voltage at the gates of input transistors of the OTA. This structure is able to operate with an ultra low supply voltage (as low as 0.3 V supply voltage).

In addition, this configuration with minimizing of the area cost and power consumption is a very cost-effective CMFB which is much more applicable regarding modern ultra low-voltage and low-power mixed-signal SoCs. Simplicity and ability of using this new merged CMFB circuit to set the output CM voltage of OTA is superior compared with state-of-the-art CMFB.

To obtain adequate gain, identical gain blocks can be cascaded so that a two-stage OTA is obtained. **Figure 3** show the proposed OTA structure in first and second stages without bias and CMFB circuits. In order to improve the phase margin and speed of amplifier, we were used Feed-forward compensation. Finally, the OTA was stabilized by adding Miller compensation capacitors Cc with series resistors Rc for right half-plane zero cancelation. The OTA was designed and classified into two kinds of compensations, such as only Miller compensation and Miller-Feed-forward (MFF) compensation. The comparison of two these methods of compensations are given in **Table 1**. As can be seen, the MFF compensation method increases the phase margin and enhances the open-loop GBW about two times as much.

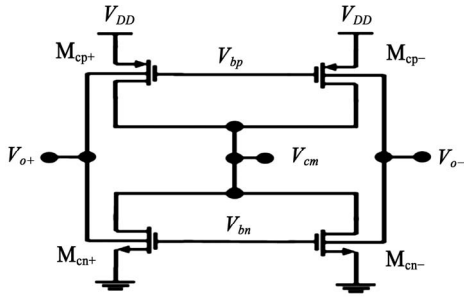

Figure 2. Ultra low-voltage bulk-mode CMFB circuit.

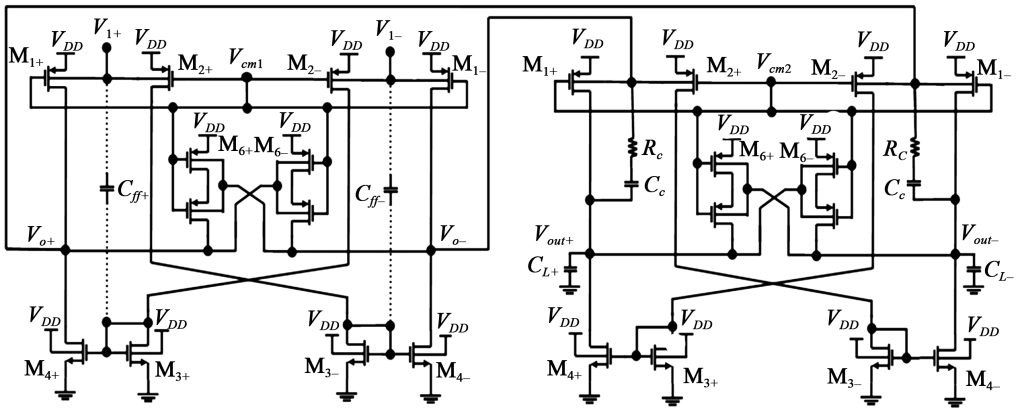

Figure 3. Two-stage bulk-input pseudo-differential OTA without bias and CMFB circuits.

Table 1. Comparison of two compensation methods.

Resistors and Capacitors	Miller-comp.	MFF-comp.
R_c	60 k	68 k
C_c	3 pf	1 pf
C_{ff}	-	3 pf
Open-loop GBW	962 KHz	2.5 MHz
Phase-Margin	65°	70.8°

2.3. Reference Current Generator and Bias Circuit

A low-sensitivity reference current generator and bias circuit are illustrated in **Figure 4**. Because the gate and source of M_{B3} and M_{B4} are common for both transistors, and the aspect ratios are equal, $I_{D\,MB3} = I_{D\,MB4}$. Also, note that $V_{GS\,MB2} = V_{GS\,MB1} + R_B \cdot I_{D\,MB1}$. Thus,

$$\sqrt{\frac{2I_{DM_{B3}}}{\mu_n \cdot C_{ox} \cdot (W/L)_{M_{B2}}}} = \sqrt{\frac{2I_{DM_{B3}}}{\mu_n \cdot C_{ox} \cdot K \cdot (W/L)_{M_{B2}}}} + R_B \cdot I_{DM_{B3}} \quad (1)$$

In the above mentioned equation, K is the ratio between the aspect ratios of M_{B1} and M_{B2}. Rearranging this expression,

$$I_{DM_{B3}} = \frac{1}{R_B^2} \frac{2}{\mu_n \cdot C_{ox}.K \cdot (W/L)_{M_{B2}}} \left(1 - \frac{1}{K}\right) \quad (2)$$

In the target circuit, k = 1.13 and R_B = 1 k, thus $I_{D\,MB3}$ = 1.25 uA. As expected, the circuit is independent of the supply voltage. Transistor M_{B5} mirrors this current to generate a stable 2 uA reference current, which is used in the bias of PMOS devices. In order to ensure that the all transistors operate in the saturation region, fixed bias voltages are applied either to the gate of the PMOS and NMOS transistors in the main OTA and CMFB circuits. The gate voltage all of the NMOS and PMOS transistors biased in about V_{bn} = 350 mV and V_{bp} = 100 mV, respectively.

3. SC Integrator and Active Filter Circuit

In order to show that the designed OTA will be useful in practical analog circuits, this structure was checked by a typical switched-capacitor (SC) integrator [7,8] with suitable input frequency 1 KHz and sampling frequency 1 MHz. **Figure 5** is shown schematic of this structure. In switched-capacitor integrator design, we utilized two clock-frequencies which have no overlap and used Bootstrapped switches in Reference [9].

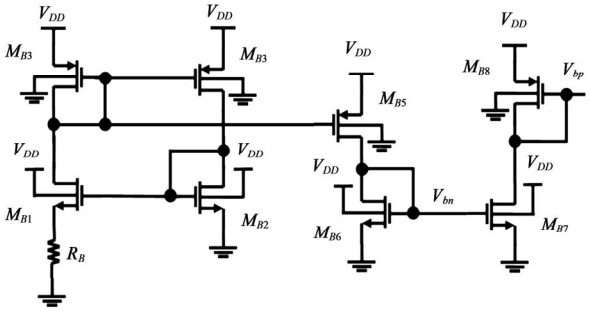

Figure 4. Reference current generator and bias circuit.

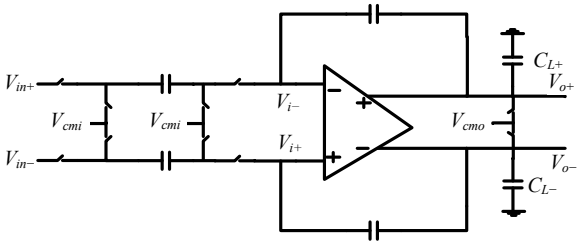

Figure 5. Fully differential switched-capacitor integrato.

Simulation result of this structure is depicted in **Figure 11**.

Filters are systems that can be used to manipulate the frequency spectrum of signals and they are essential in many different applications. The low-pass continuous-time filter is used to limit signal and noise bandwidth and provide anti-aliasing prior sampling. The analog-to- digital converter (ADC) digitizes the filtered output to take the advantages of the Digital Signal Processing (DSP) unit. The equalizer provides the equalization and the equalized signal goes to the decoder. The gain/timing control module is used to adjust the gain of the VGA. Although we are living in a digital age, many digital systems interfacing with the real analog world might use continuous-time filters. There are mainly two types of filters: digital filters and analog filters. While the data samples are discrete for digital filters, analog filters process continuous signals. Analog filters can be further divided into passive filters and active filters. While passive filters comprise passive components only such as resistors, capacitors, and inductors, active filters use active devices such as operational amplifiers and/or operational transconductance amplifiers (OTAs). Active filters can also be classified into Active-RC, Switched-Ca- pacitor (sampled-data filters), OTA-C/Gm-C, and LC filters. Passive filters do not employ amplifiers and usually they are off-chip filters and are not suitable for integrated circuits. But active-RC and SC filters are suitable for low to medium frequency applications.

This OTA was tested in an 8th order active Biquadrate RC filter for maximize the attainable swing. The filter was built by connecting four 2nd orders Thomas BiQuad stage to implement the Butterworth function, shown in **Figure 6**. The equations of the Two-Thomas biquad filter as follow:

$$\omega_{\circ}^2 = \frac{1}{R_{s2} \cdot R_{f2} \cdot C_{f1} \cdot C_{f2}}, Q = \frac{R_{f1}}{\sqrt{R_{s2} \cdot R_{f2}}} \sqrt{\frac{C_{f1}}{C_{f2}}}, A_{\circ} = \frac{R_{f2}}{R_{s1}} \tag{3}$$

where $A_{\circ}$ is the gain of integrator and $\omega_{\circ}$ and Q are the cut-off frequency and quality factor of integrator, respectively. Assume $R_{s2} = R_{f2}$, $C_{f1} = C_{f2}$, Equation (3) can be written as:

$$\omega_{\circ} = \frac{1}{R_{f2} \cdot C_{f1}}, Q = \frac{R_{f1}}{R_{f2}}, A_{\circ} = \frac{R_{f2}}{R_{s1}} \tag{4}$$

In the above mentioned equation, Q and $A_{\circ}$ are determined by the ratio of resistors and both Q and $\omega_{\circ}$ can be tuned independently [10]. This 8th order Butterworth filter consists of four cascaded Thomas biquads; and the cut-off frequency is about 400 KHz. The filter was simulated with components values given in **Table 2**. Also, a plot of the frequency response for input CM voltage from rail-to-rail of this filter is shown in **Figure 12**.

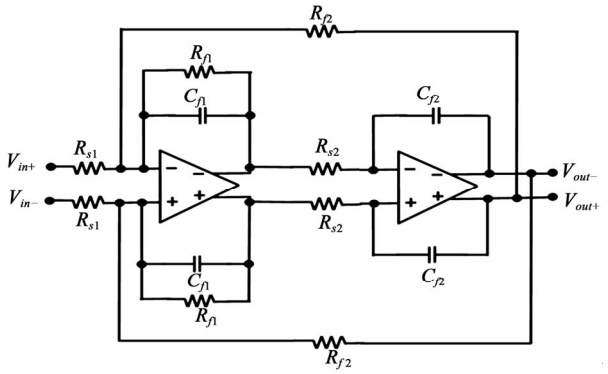

Figure 6. 2nd order Thomas Biquad filter stage.

Table 2. Filter component values.

Components	Stage (1)	Stage (2)	Stage (3)	Stage (4)
R_{s1}	56 k	39 k	47 k	56 k
R_{s2}	56 k	39 k	47 k	56 k
R_{f1}	30 k	87 k	87 k	30 k
R_{f2}	56 k	39 k	47 k	56 k
C_{f1}	10 pf	10 pf	10 pf	12 pf
C_{f2}	10 pf	8 pf	5.4 pf	10 pf

4. Simulation Results

To test op-amp's performance, various configurations were implemented to simulate application condition. Based on the analysis procedure described in the previous sections, an ultra low-voltage OTA at a single 0.5 V supply voltage was designed. The OTA has been designed in 90 nm CMOS process, and then simulated by Hspice. Then this structure was checked by a typical SC integrator with a 1 MHz clock frequency. Also a 8th order active RC-filter with a 400 KHz cut-off frequency was designed. The simulation results are shown in **Figures 7** to **12**. Furthermore, **Table 3** summarizes the simulated performance of this OTA and comparisons of characteristics of proposed OTA with state-of-the-art OTAs. The open-loop frequency response of the OTA for the common-mode input V_{cm} varying from rail-to-rail by a step 0.01 V was tested. The amplitudes and the phases of the proposed OTA were almost independent of the applied V_{cm}. **Figure 5** shows the frequency response of the OTA for V_{cm} = 0.25 V. The result showed a 70.2 dB DC gain, a 2.5 MHz bandwidth and a of 70.8° phase margin. For the closed-loop simulation, the OTA was configured in unity-gain with 1 pf capacitors.

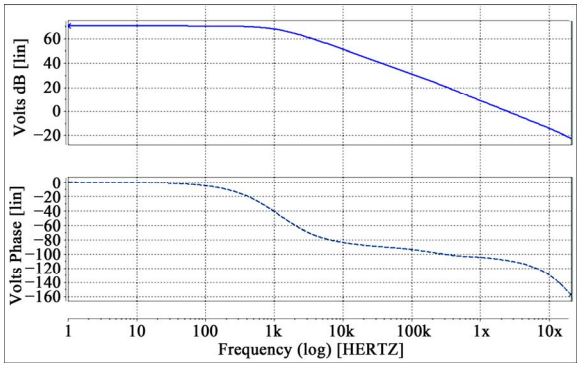

Figure 7. Open-loop frequency response of OTA for V_{cm} = 0.25 V.

Table 3. Comparison of characteristics of proposed OTA with state-of-the-art OTAs.

Parameters	This work	Ref. [5]	Ref. [6]
Technology	90 nm	0.18 µm	0.18 µm
Supply Voltage	0.5 V	0.5 V	0.5 V
Open-loop DC Gain	70.2 dB	62 dB	65 dB
Open-loop GBW	2.5 MHz	10 MHz	550 KHz
Closed-loop GBW	645 KHz	-	475 KHz
Phase-Margin	70.8°	60°	50°
Input ref. noise@1 KHz	139 nV/Hz$^{1/2}$	-	432 nV/Hz$^{1/2}$
FOM	100	133.3	19.6
THD@ 500 mV	0.119%	1%	0.13%
Load Capacitors	20 pf	20 pf	20 pf
Power Consumption	25 µw	110 µw	28 µw

The closed-loop frequency response of the OTA is shown in **Figure 8** for rail-to-rail input common-mod ranges by a step of 50 mV. It is obvious that the frequency responses of OTA have no peak and result a bandwidth of 645 KHz. This shows that the OTA function correctly for rail-to-rail input common-mode voltage values without any considerable decrease in gain.

The main optimization steps were done in transient tests because it is most important behavior. Two inputs were applied to see both small and large signal behavior of OTA in transient mode, when in closed-loop test; the OTA is configured in unity-gain with 1 pf capacitors. For an input common-mode voltage of 250 mV, when 0.1 V step was applied to inputs of OTA, the output voltage was settled to its final value in less than 735 ns (@ 0.01%). Identically, for large signal mode with a 0.3 V step and input common-mode voltage of 250 mV, output voltage was settled in less than 1500 ns for rising and less than 1170 ns for falling (@ 0.02%).

In this case, positive and negative slew-rates are 0.67 V/μs and 0.8 V/μs, respectively. **Figure 9** show transient response of OTA for 0.1 V and 0.3 V inputs, when input common-mode voltage varying from rail-to-rail by a step 50 mV. It is obvious that response has no ring or overshoot because of suitable bandwidth and phase margin.

The obtained total harmonic distortion of OTA with a 200 mV amplitude and 10 KHz input frequency sampled at 100 KHz is shown in **Figure 10**. The third harmonic is

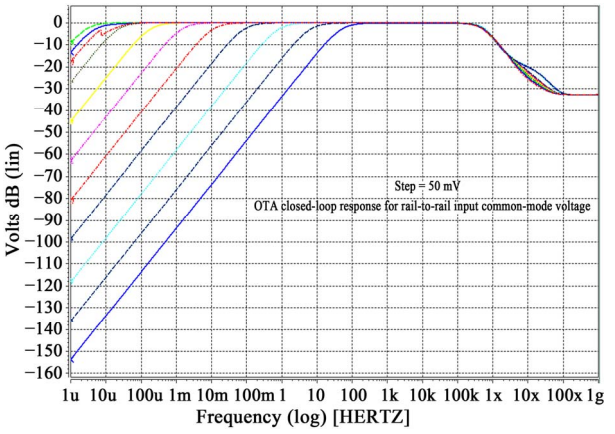

Figure 8. OTA closed-loop response for rail-to-rail common mode input value (Step = 50 mV).

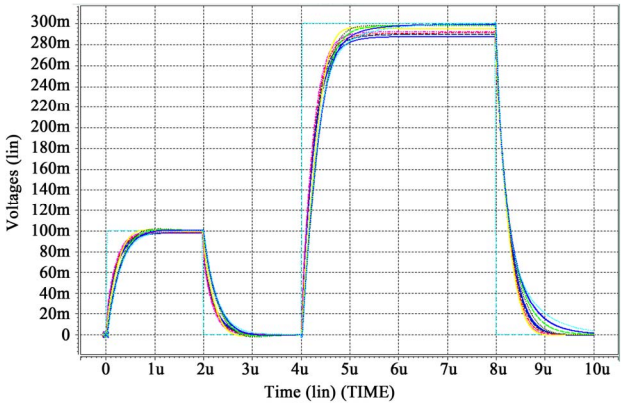

Figure 9. Settling simulated results of OTA for rail-to-rail input common-mode voltage (Step = 50 mV).

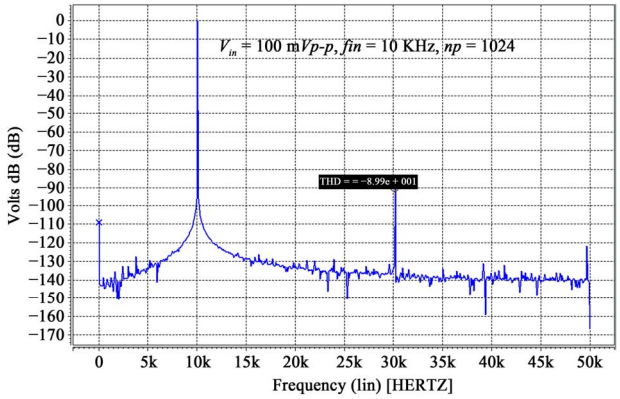

Figure 10. Total harmonic distortion of OTA with f_{in} = 10 KHz and V_{in} = 200 *mVp–p*.

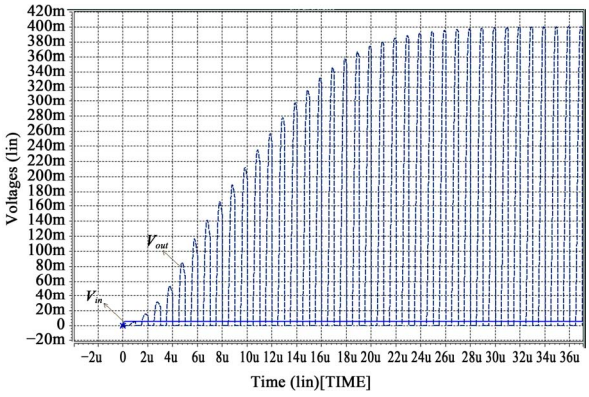

Figure 11. Integrated output voltage of OTA with f_s = 1 MHz and f_{in} = 1 KHz.

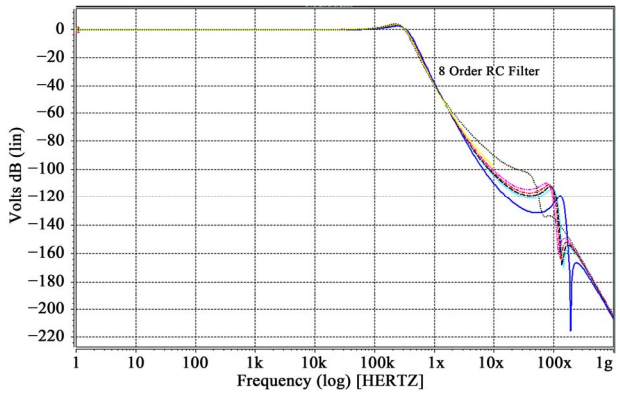

Figure 12. Filter frequency response of OTA v. s input CM voltage from rail-to-rail.

about 90 dB below the fundamental. Also, for 400 mV amplitude, the third harmonic is about −74.4 dB. As can be seen, the extra harmonics except main harmonic has been eliminated in this design.

5. Conclusions

In this paper a novel two-stage configuration of the ultra low-voltage and low-power bulk-input CMOS OTA in 90 nm CMOS process which is able to operate with a single supply voltage as low as 0.5 V has been presented. A new merged cross-coupled self-cascode pair was used and higher DC gain was achieved. In addition, a MFF compensation was utilized which has been improved the GBW and phase margin of the OTA. Also, a new bulk-mode CMFB circuit which no longer loads OTA has been discussed. A large linear signal swing has been achieved due to the well controlled CM behavior. Finally this structure was checked by a typical SC integrator and was tested in an 8th order active Biquadrate RC filter. Correct functionality for this configuration is verified from −30˚C to 70˚C. In addition, this structure can be used for modern ultra low-voltage and low-power mixed- signal SoCs.

6. Acknowledgements

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