

LECTURE 010 - INTRODUCTION TO CMOS ANALOG CIRCUIT DESIGN

LECTURE ORGANIZATION

Outline

- Introduction
- What is Analog Design?
- Skillset for Analog IC Circuit Design
- Trends in Analog IC Design
- Notation, Terminology and Symbols
- Summary

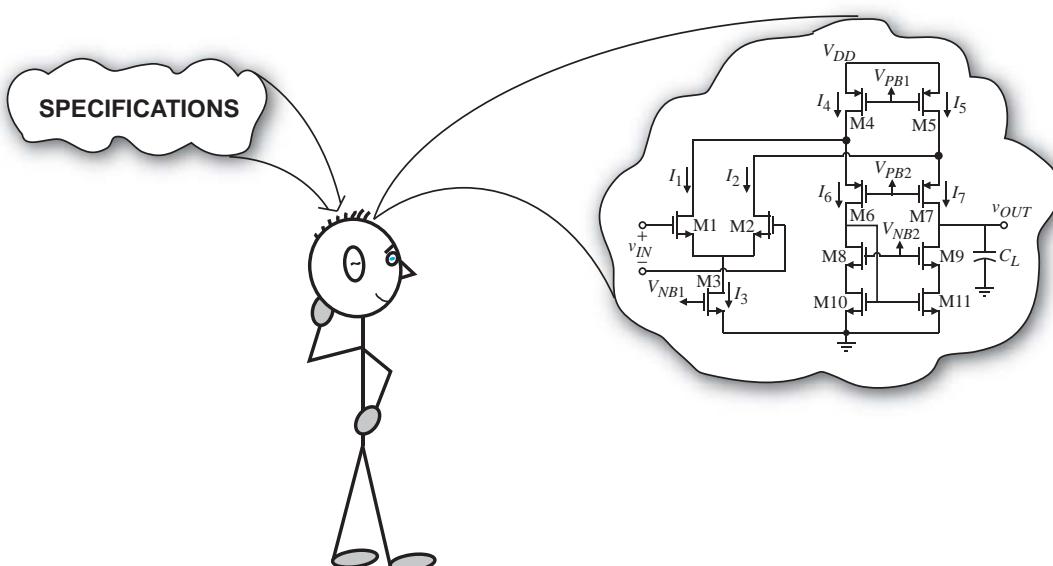
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 1-16

INTRODUCTION

Course Objective

This course teaches analog integrated circuit design using CMOS technology.

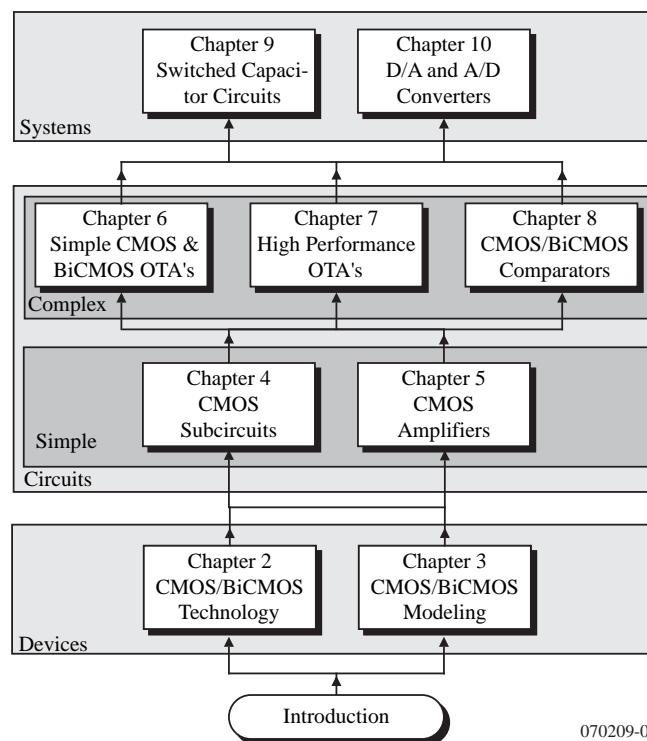


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Course Prerequisites

- Basic understanding of electronics
 - Active and passive components
 - Large and small signal models
 - Frequency response
- Circuit analysis techniques
 - Mesh and loop equations
 - Superposition, Thevenin and Norton's equivalent circuits
- Integrated circuit technology
 - Basics process steps
 - PN junctions

Course Organization – Based on 2nd Ed. of CMOS Analog Circuit Design



References

- 1.) P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design* – 2nd Ed., Oxford University Press, 2002.
- 2.) P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits* – 4th Ed., John Wiley and Sons, Inc., 2001.
- 3.) B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Inc., 2001.
- 4.) R.J. Baker, H.W. Li and D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, IEEE Press, 1998.
- 5.) D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley and Sons, Inc., 1997.
- 6.) K.R. Laker and W.M.C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Inc., 1994.
- 7.) R.L. Geiger, P.E. Allen and N.R. Strader, *VLSI Techniques for Analog and Digital Circuits*, McGraw-Hill, Inc., 1990.
- 8.) A. Hastings, *The Art of Analog Layout* – 2nd Ed., Prentice-Hall, Inc., 2005.
- 9.) J. Williams, Ed., *Analog Circuit Design - Art, Science, and Personalities*, Butterworth-Heinemann, 1991.
- 10.) R.A. Pease, *Troubleshooting Analog Circuits*, Butterworth-Heinemann, 1991.

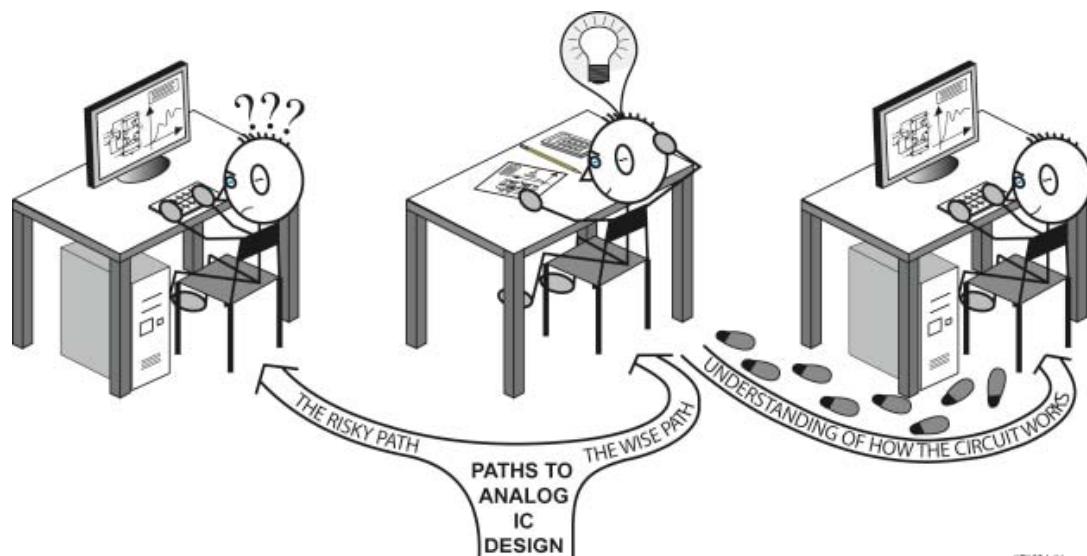
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Course Philosophy

This course emphasizes *understanding* of analog integrated circuit design.

Although simulators are very powerful, the designer must understand the circuit before using the computer to simulate a circuit.



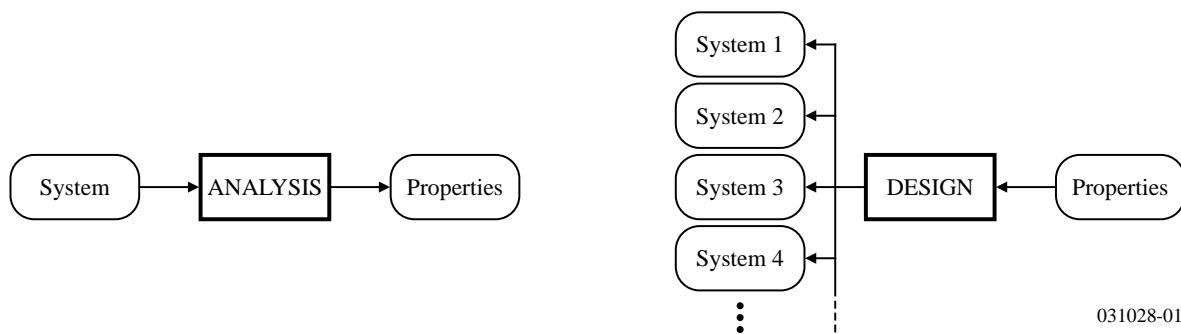
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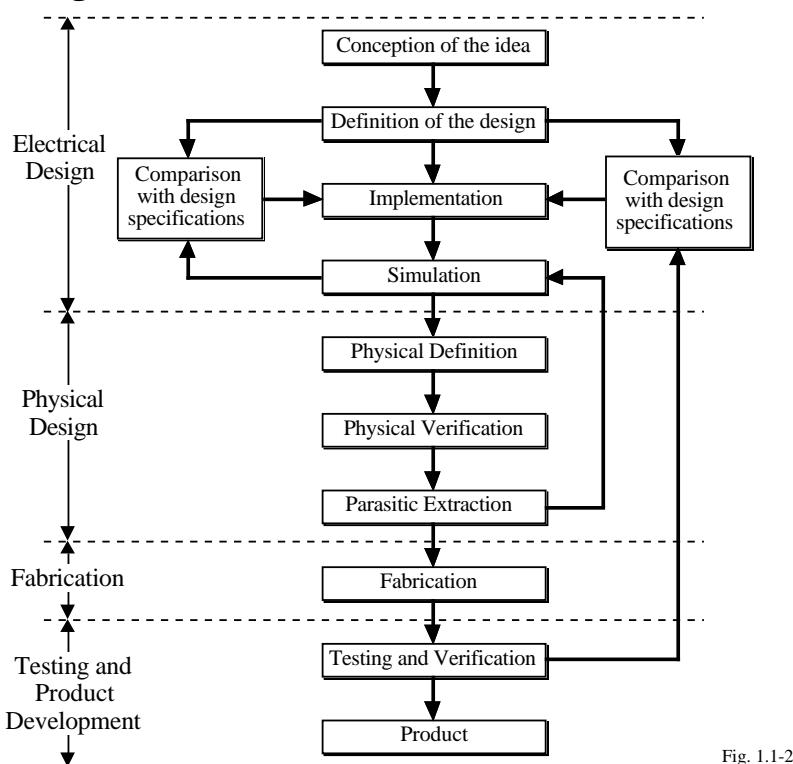
WHAT IS ANALOG DESIGN?

Analysis versus synthesis (design)



- Analysis: Given a system, find its properties. The solution is unique.
- Design: Given a set of properties, find a system possessing them. The solution is rarely unique.

The Analog IC Design Process



What is Electrical Design?

Electrical design is the process of going from the specifications to a circuit solution. The inputs and outputs of electrical design are:

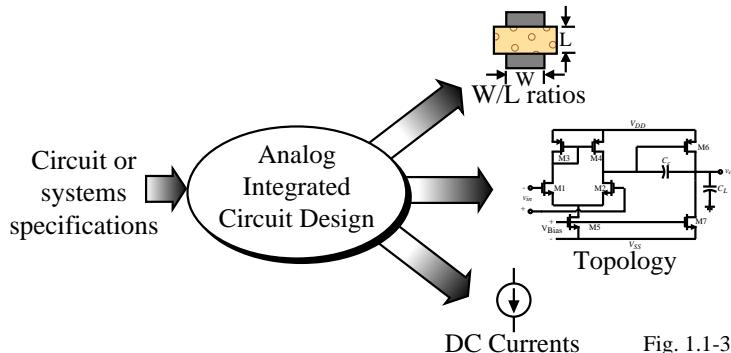


Fig. 1.1-3

The electrical design requires active and passive device electrical models for

- Creating the design
- Verifying the design
- Determining the robustness of the design

Steps in Electrical Design

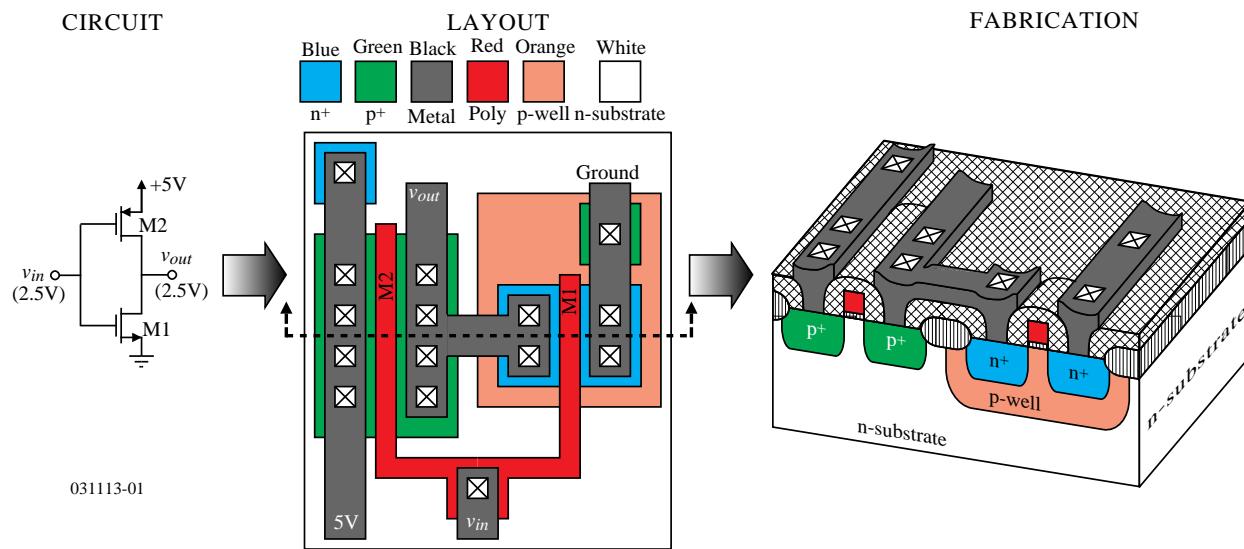
- 1.) Selection of a solution
 - Examine previous designs
 - Select a solution that is simple
- 2.) Investigate the solution
 - Analyze the performance (without a computer)
 - Determine the strengths and weaknesses of the solution
- 3.) Modification of the solution
 - Use the key principles, concepts and techniques to implement
 - Evaluate the modifications through analysis (still no computers)
- 4.) Verification of the solution
 - Use a simulator with precise models and verify the solution
 - Large disagreements with the hand analysis and computer verification should be carefully examined.



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What is Physical Design?

Physical design is the process of representing the electrical design in a layout consisting of many distinct geometrical rectangles at various levels. The layout is then used to create the actual, three-dimensional integrated circuit through a process called *fabrication*.



What is the Layout Process?

- 1.) The inputs are the W/L values and the schematic (generally from schematic entry used for simulation).
- 2.) A CAD tool is used to enter the various geometries. The designer must enter the location, shape, and level of the particular geometry.
- 3.) During the layout, the designer must obey a set of rules called *design rules*. These rules are for the purpose of ensuring the robustness and reliability of the technology.
- 4.) Once the layout is complete, then a process called *layout versus schematic* (LVS) is applied to determine if the physical layout represents the electrical schematic.
- 5.) The next step is now that the physical dimensions of the design are known, the parasitics can be extracted. These parasitics primarily include:
 - a.) Capacitance from a conductor to ground
 - b.) Capacitance between conductors
 - c.) Bulk resistance
- 6.) The extracted parasitics are entered into the simulated database and the design is re-simulated to insure that the parasitics will not cause the design to fail.

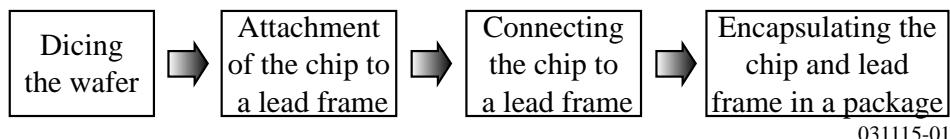
Packaging[†]

Packaging of the integrated circuit is an important part of the physical design process.

The function of packaging is:

- 1.) Protect the integrated circuit
- 2.) Power the integrated circuit
- 3.) Cool the integrated circuit
- 4.) Provide the electrical and mechanical connection between the integrated circuit and the outside world.

Packaging steps:



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Other considerations of packaging:

- Speed
- Parasitics (capacitive and inductive)

[†] Rao Tummala, "Fundamentals of Microsystems Packaging," McGraw-Hill, NY, 2001.
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What is Test Design?

Test design is the process of coordinating, planning and implementing the measurement of the analog integrated circuit performance.

Objective: To compare the experimental performance with the specifications and/or simulation results.

Types of tests:

- Functional – verification of the nominal specifications
- Parametric – verification of the characteristics to within a specified tolerance
- Static – verification of the static (AC and DC) characteristics of a circuit or system
- Dynamic – verification of the dynamic (transient) characteristics of a circuit or system

Additional Considerations:

Should the testing be done at the wafer level or package level?

How do you remove the influence (de-embed) of the measurement system from the measurement?

ANALOG INTEGRATED CIRCUIT DESIGN SKILLSET

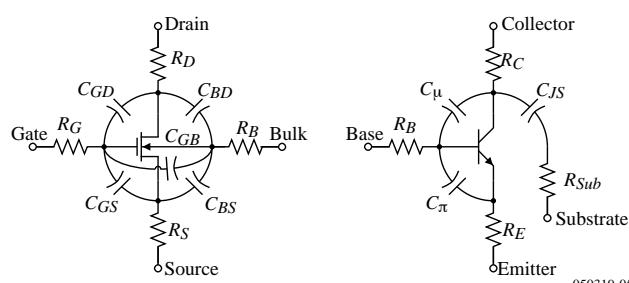
Characteristics of Analog Integrated Circuit Design

- Done at the circuits level
- Complexity is high
- Continues to provide challenges as technology evolves
- Demands a strong understanding of the principles, concepts and techniques
- Good designers generally have a good physics background
- Must be able to make appropriate simplifications and assumptions
- Requires a good grasp of both modeling and technology
- Have a wide range of skills - breadth (analog only is rare)
- Be able to learn from failure
- Be able to use simulation correctly

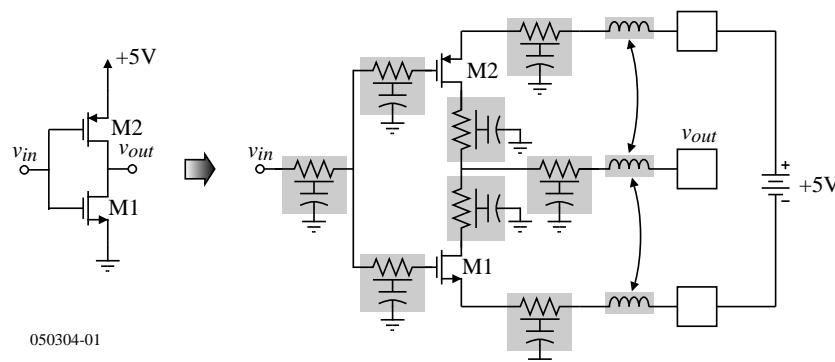
Understanding Technology

Understanding technology helps the analog IC designer to know the limits of the technology and the influence of the technology on the design.

Device Parasitics:



Connection Parasitics:



Implications of Smaller Technology on IC Design

The good:

- Smaller geometries
- Smaller parasitics
- Higher transconductance
- Higher bandwidths

The bad:

- Reduced voltages
- Smaller channel resistances (lower gain)
- More nonlinearity
- Deviation from square-law behavior

The challenging:

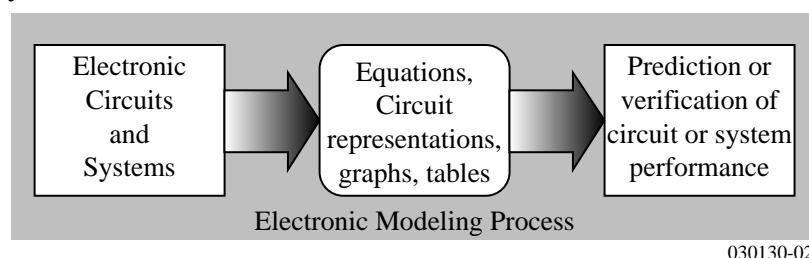
- Increased substrate noise in mixed signal applications
- Threshold voltages are not scaling with power supply
- Reduced dynamic range
- Poor matching at minimum channel length

Understanding Modeling

Modeling:

Modeling is the process by which the electrical properties of an electronic circuit or system are represented by means of mathematical equations, circuit representations, graphs or tables.

Models permit the predicting or verification of the performance of an electronic circuit or system.



Examples:

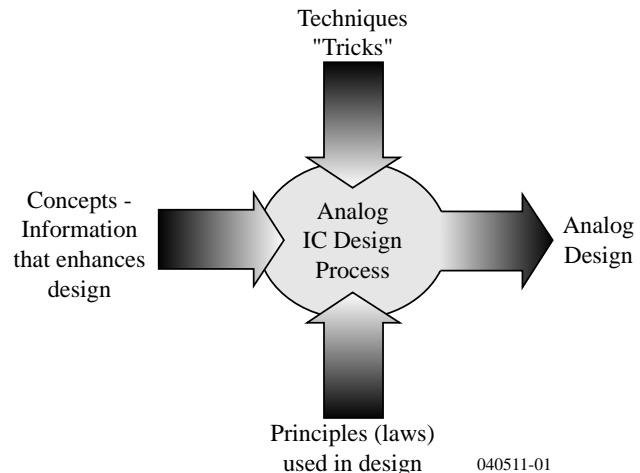
Ohm's law, the large signal model of a MOSFET, the I-V curves of a diode, etc.

Goal:

Models that are simple and allow the designer to understand the circuit performance.

Key Principles, Concepts and Techniques of Analog IC Design

- Principles mean *fundamental laws* that are precise and never change.
(Webster – A comprehensive and fundamental law, doctrine, or assumption. The laws or facts of nature underlying the working of an artificial device.)
- Concepts will include *relationships*, “soft-laws” (ones that are generally true), analytical tools, things worth remembering.
(Webster – An abstract idea generalized from particular instances.)
- Techniques will include the assumptions, “tricks”, tools, *methods* that one uses to simplify and understand.
(Webster – The manner in which technical details are treated, a method of accomplishing a desired aim or goal.)

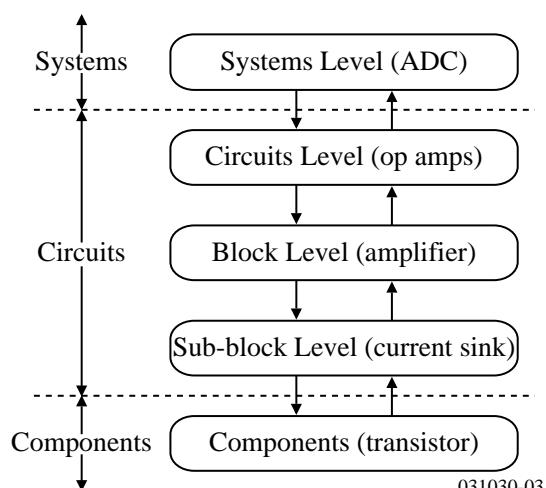


Complexity in Analog Design

Analog design is normally done in a non-hierarchical manner and makes little use of repeated blocks. As a consequence, analog design can become quite complex and challenging.

How do you handle the complexity?

- 1.) Use as much hierarchy as possible.
- 2.) Use appropriate organization techniques.
- 3.) Document the design in an efficient manner.
- 4.) Make use of assumptions and simplifications.
- 5.) Use simulators appropriately.



Assumptions

Assumptions:

An assumption is taking something to be true without formal proof. Assumptions in analog circuit design are used for simplifying the analysis or design. The goal of an assumption is to separate the essential information from the nonessential information of a problem.

The elements of an assumption are:

- 1.) Formulating the assumption to simplify the problem without eliminating the essential information.
- 2.) Application of the assumption to get a solution or result.
- 3.) Verification that the assumption was in fact appropriate.

Examples:

Neglecting a large resistance in parallel with a small resistance

Miller effect to find a dominant pole

Finding the roots of a second-order polynomial assuming the roots are real and separated

WHERE IS ANALOG IC DESIGN TODAY?

Analog IC Design has Reached Maturity

There are established fields of application:

- Digital-analog and analog-digital conversion
- Disk drive controllers
- Modems - filters
- Bandgap reference
- Analog phase lock loops
- DC-DC conversion
- Buffers
- Codecs
- Etc.

Existing philosophy regarding analog circuits:

“If it can be done economically by digital, don’t use analog.”

Consequently:

Analog finds applications where speed, area, or power have advantages over a digital approach.

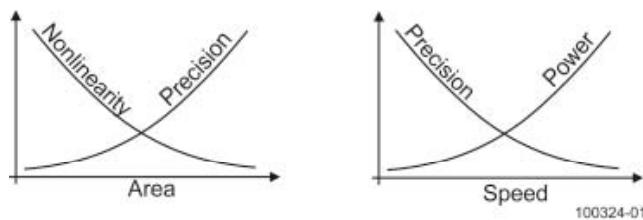
Analog IC Design Challenges

Technology:

- Digital circuits have scaled well with technology
- Analog does not benefit as much from smaller features
 - Speed increases
 - Gain decreases
 - Matching decreases
 - Nonlinearity increases
 - New issues appear such as gate current leakage

Analog Circuit Challenges:

- Trade offs are necessary between linearity, speed, precision and power



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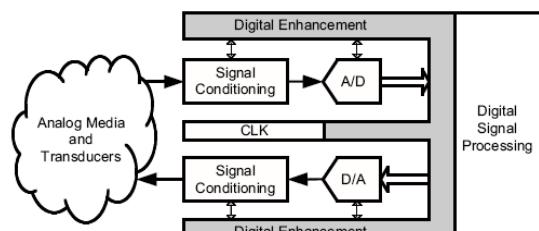
- As analog is combined with more digital, substrate interference will become worse

Digitally Assisted Analog Circuits

Use digital circuits which work better at scaled technologies to improve analog circuits that do not necessarily improve with technology scaling.

Principles and Techniques:

- Open-loop vs. closed loop
 - Open loop is less accurate but smaller \Rightarrow Faster, less power
 - Closed-loop is more accurate but larger \Rightarrow Slower, more power
- Averaging
 - Increase of accuracy \Rightarrow Smaller devices, more speed
- Calibration
 - Accuracy increases \Rightarrow Increased resolution with same area
- Dynamic Element Matching
 - Enhancement of component precision
- Doubly correlated sampling
 - Reduction of dc influences (noise, offset) \Rightarrow Smaller devices, more speed
- Etc.



What is the Future of Analog IC Design?

- More creative circuit solutions are required to achieve the desired performance.
- Analog circuits will continue to be a part of large VLSI digital systems
- Interference and noise will become even more serious as the chip complexity increases
- Packaging will be an important issue and offers some interesting solutions
- Analog circuits will always be at the cutting edge of performance
- Analog designer must also be both a circuit and systems designer and must know:
 - Technology and modeling
 - Analog circuit design
 - VLSI digital design
 - System application concepts
- There will be no significantly new and different technologies - innovation will combine new applications with existing or improved technologies
- Semicustom methodology will eventually evolve with CAD tools that will allow:
 - Design capture and reuse
 - Quick extraction of model parameters from new technology
 - Test design
 - Automated design and layout of simple analog circuits

NOTATION, TERMINOLOGY AND SYMBOLOGY

Definition of Symbols for Various Signals

Signal Definition	Quantity	Subscript	Example
Total instantaneous value of the signal	Lowercase	Uppercase	q_A
DC value of the signal	Uppercase	Uppercase	Q_A
AC value of the signal	Lowercase	Lowercase	q_a
Complex variable, phasor, or rms value of the signal	Uppercase	Lowercase	Q_a

Example:

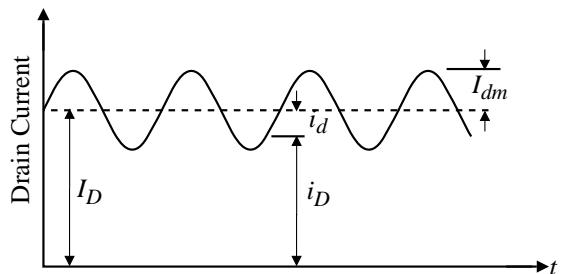
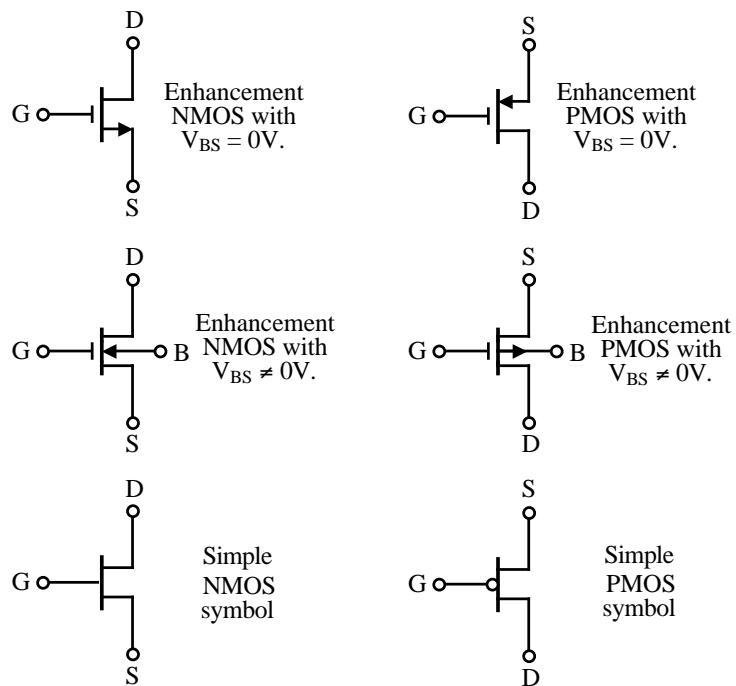
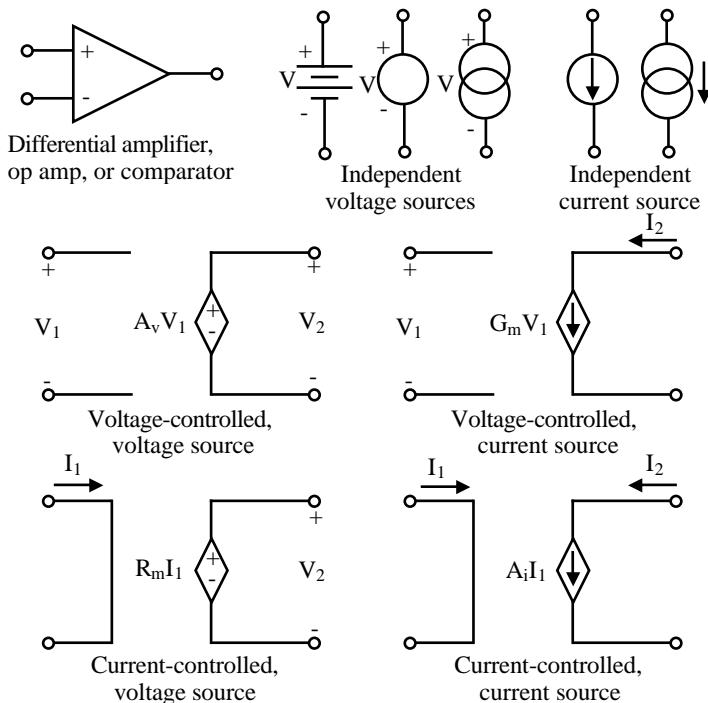


Fig. 1.4-1

MOS Transistor Symbols



Other Schematic Symbols



Three-Terminal Notation

QABC

A = Terminal with the larger magnitude of potential

B = Terminal with the smaller magnitude of potential

C = Condition of the remaining terminal with respect to terminal B

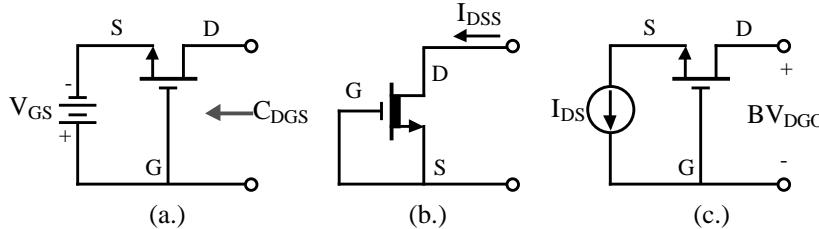
$C = 0 \Rightarrow$ There is an infinite resistance between terminal B and the 3rd terminal

$C = S \Rightarrow$ There is a zero resistance between terminal B and the 3rd terminal

$C = R \Rightarrow$ There is a finite resistance between terminal B and the 3rd terminal

$C = X \Rightarrow$ There is a voltage source in series with a resistor between terminal B and the 3rd terminal in such a manner as to reverse bias a PN junction.

Examples



(a.) Capacitance from drain to gate with the source shorted to the gate.

(b.) Drain-source current when gate is shorted to source (depletion device)

(c.) Breakdown voltage from drain to gate with the source is open- circuited to the gate.

SUMMARY

- Successful analog IC design proceeds with understanding the circuit before simulation.
- Analog IC design consists of three major steps:
 - 1.) Electrical design \Rightarrow Topology, W/L values, and dc currents
 - 2.) Physical design (Layout)
 - 3.) Test design (Testing)
- Analog designers must be flexible and have a skill set that allows one to simplify and understand a complex problem
- Analog IC design has reached maturity and is here to stay.
- The appropriate philosophy is “If it can be done economically by digital, don’t use analog”.
- As a result of the above, analog finds applications where speed, area, or power result in advantages over a digital approach.
- Deep-submicron technologies will offer exciting challenges to the creativity of the analog designer.

LECTURE 020 - SUBMICRON CMOS TECHNOLOGY

LECTURE ORGANIZATION

Outline

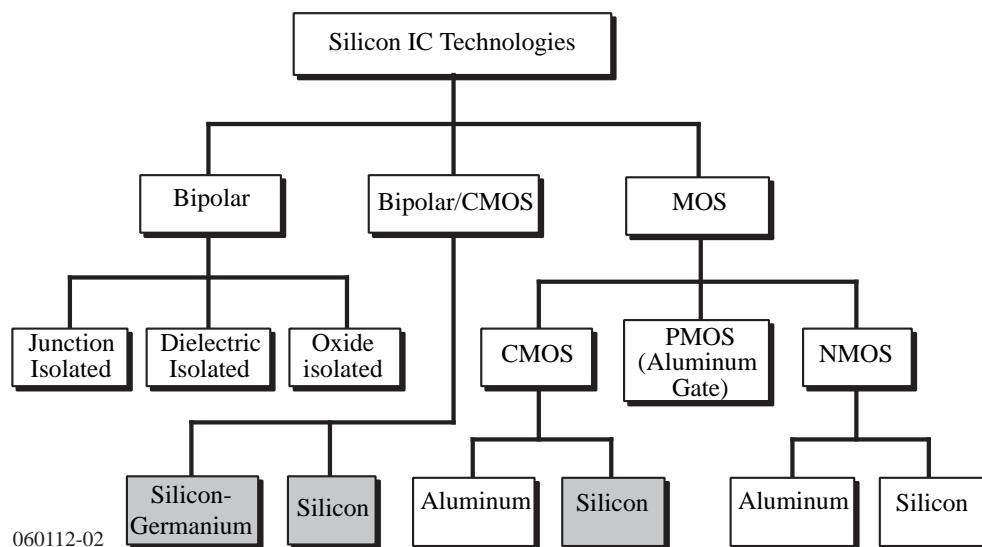
- CMOS Technology
- Fundamental IC Process Steps
- Typical Submicron CMOS Fabrication Process
- Summary

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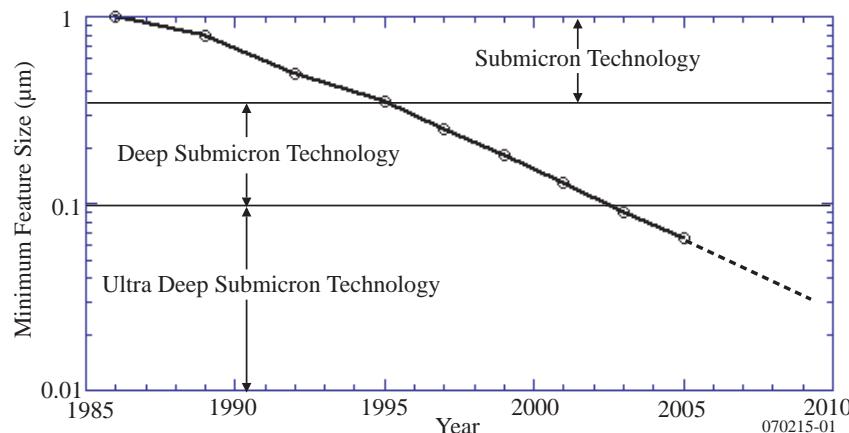
CMOS TECHNOLOGY

Classification of Silicon Technology



Categorization of CMOS Technology

- Minimum feature size as a function of time:



- Categories of CMOS technology:

- 1.) Submicron technology – $L_{min} \geq 0.35$ microns
- 2.) Deep Submicron technology (DSM) – 0.1 microns $\leq L_{min} \leq 0.35$ microns
- 3.) Ultra-Deep Submicron technology (UDSM) – $L_{min} \leq 0.1$ microns

Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

Comparison Feature	BJT	MOSFET
Cutoff Frequency(f_T)	100 GHz	50 GHz ($0.25\mu m$)
Noise (thermal about the same)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus v_{BE}	2-3 decades of square law behavior
Transconductance (Same current)	Larger by 10X	Smaller by 10X
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor	Voltage dependent	More options
Performance/Power Ratio	High	Low
Technology Improvement	Slower	Faster

Therefore,

- Almost every comparison favors the BJT, however a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume mixed-mode technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

How Does IC Technology Influence Analog IC Design?

Characteristics of analog IC design:

- Continuous in signal amplitude
- Discrete or continuous in time
- Signal processing primarily depends on ratios of values and time constants
 - Ratios are generally resistance, conductance, or capacitance
 - Time constants are generally products of resistance and capacitance
- Dynamic range is determined by the largest and smallest signals

Influence of IC Technology:

- Accuracy of signal processing depends on the accuracy of the ratios of values
- The dynamic range depends upon the linearity of the circuit elements and the noise
- The value of components is limited by area considerations
- IC technology introduces resistive, capacitive and inductive parasitics that cause deviation from desired behavior
- The analog circuit is subject to the influence of other circuits fabricated in the same substrate

FUNDAMENTAL IC PROCESS STEPS

Basic Steps

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Shallow trench isolation
- Epitaxy

Photolithography

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

Silicon Wafer

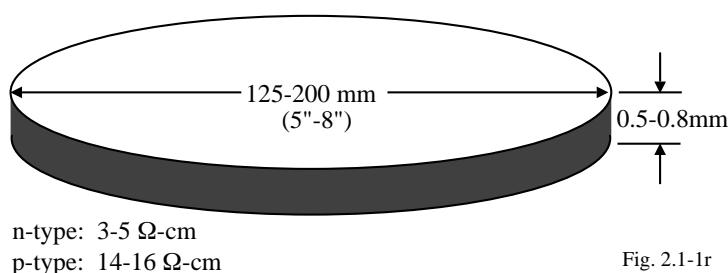


Fig. 2.1-1r

Oxidation

Description:

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

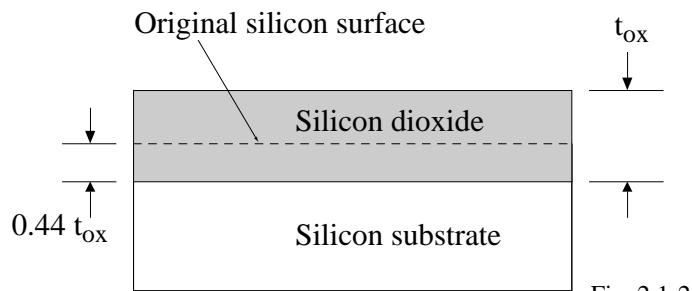


Fig. 2.1-2

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100\AA to 1000\AA) are grown using dry oxidation techniques. Thicker oxides ($>1000\text{\AA}$) are grown using wet oxidation techniques.

Diffusion

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

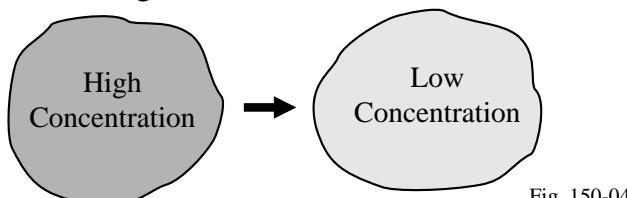
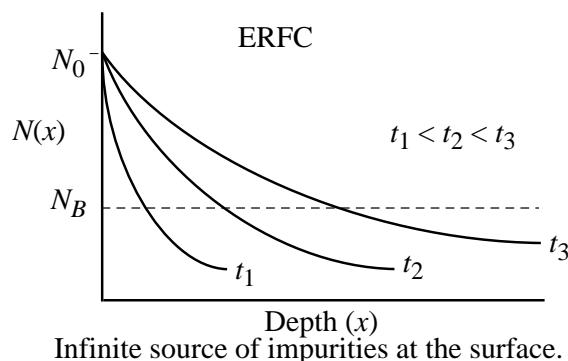
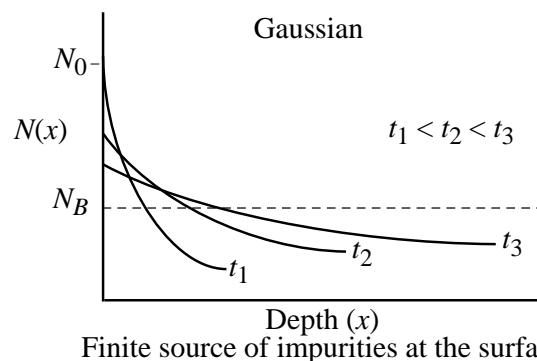


Fig. 150-04

Diffusion is typically done at high temperatures: 800 to 1400°C



Infinite source of impurities at the surface.

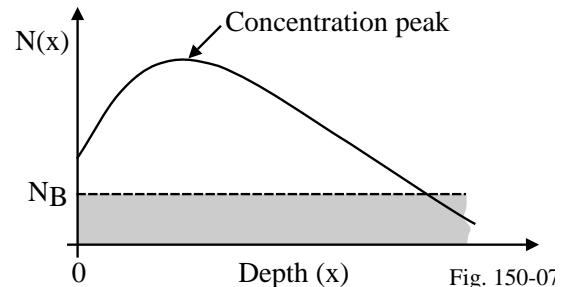
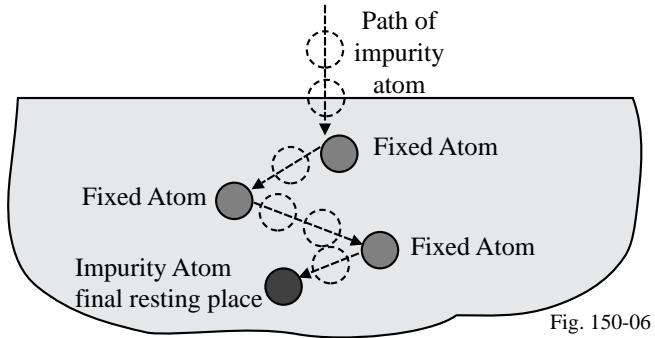


Finite source of impurities at the surface.

Ion Implantation

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

- Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.



Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon

There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

Material that is being deposited using these techniques covers the entire wafer and requires no mask.

Etching

Etching is the process of selectively removing a layer of material.

When etching is performed, the etchant may remove portions or all of:

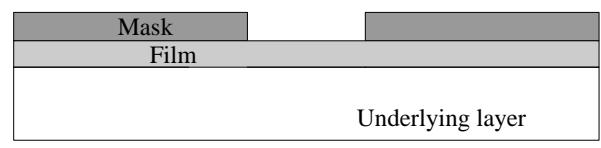
- The desired material
- The underlying layer
- The masking layer

Important considerations:

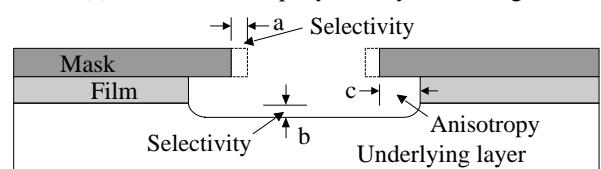
- *Anisotropy* of the etch is defined as,
 $A = 1 - (\text{lateral etch rate} / \text{vertical etch rate})$
- *Selectivity* of the etch (film to mask and film to substrate) is defined as,
 $S_{\text{film-mask}} = \frac{\text{film etch rate}}{\text{mask etch rate}}$
 $A = 1$ and $S_{\text{film-mask}} = \infty$ are desired.

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.



(a) Portion of the top layer ready for etching.



(b) Horizontal etching and etching of underlying layer.

Fig. 150-08

Epitaxy

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even opposite to the material on which it is grown
- It is accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns

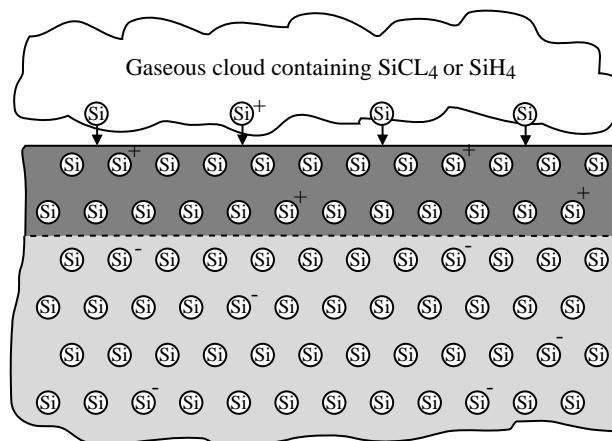


Fig. 150-09

Photolithography

Components

- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist

Areas exposed to UV light are soluble in the developer

Negative photoresist

Areas not exposed to UV light are soluble in the developer

Steps

1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake ($\approx 100^\circ\text{C}$)
6. Remove photoresist (solvents)

Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photo-mask is called *printing*.

Types of printing include:

- Contact printing
- Proximity printing
- Projection printing

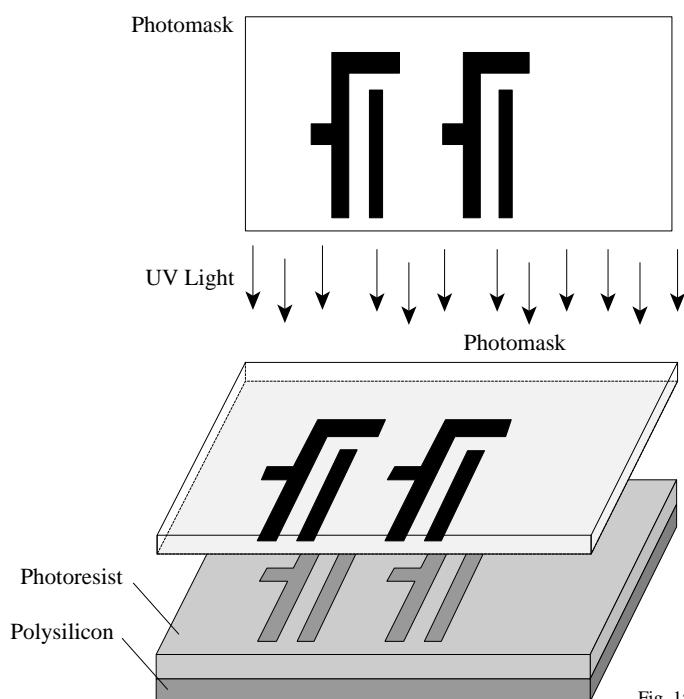


Fig. 150-10

Illustration of Photolithography - Positive Photoresist

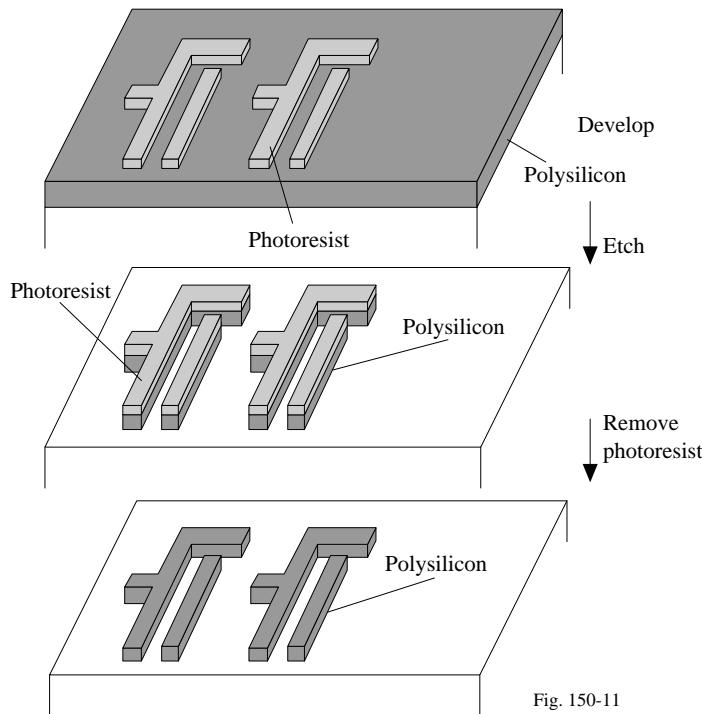


Fig. 150-11

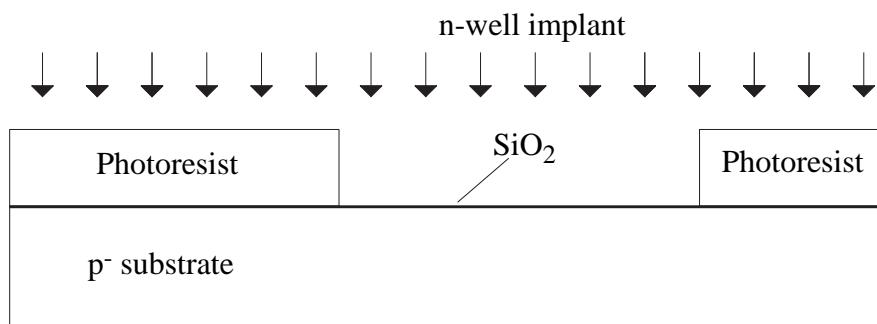
TYPICAL SUBMICRON CMOS FABRICATION PROCESS

N-Well CMOS Fabrication Major Steps

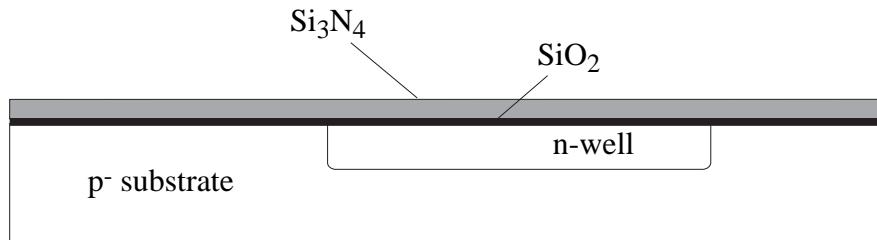
- 1.) Implant and diffuse the n-well
- 2.) Deposition of silicon nitride
- 3.) n-type field (channel stop) implant
- 4.) p-type field (channel stop) implant
- 5.) Grow a thick field oxide (FOX)
- 6.) Grow a thin oxide and deposit polysilicon
- 7.) Remove poly and form LDD spacers
- 8.) Implantation of NMOS S/D and n-material contacts
- 9.) Remove spacers and implant NMOS LDDs
- 10.) Repeat steps 8.) and 9.) for PMOS
- 11.) Anneal to activate the implanted ions
- 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
- 13.) Open contacts, deposit first level metal and etch unwanted metal
- 14.) Deposit another interlayer dielectric (CVD SiO₂), open vias, deposit 2nd level metal
- 15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



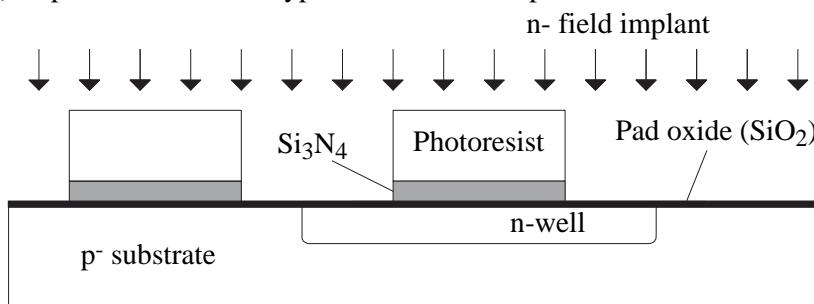
Step 2 - Growth of thin oxide and deposition of silicon nitride



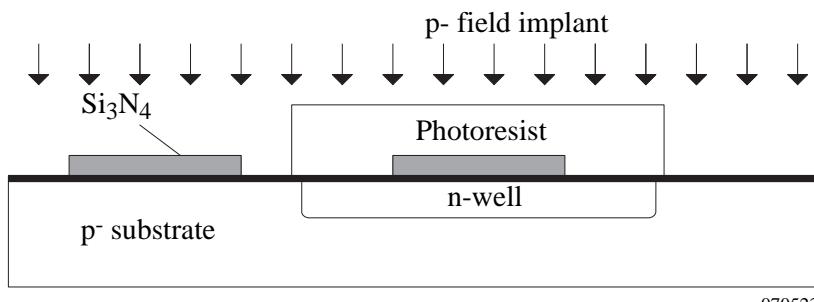
070523-01

Major CMOS Process Steps – Continued

Step 3.) Implantation of the n-type field channel stop



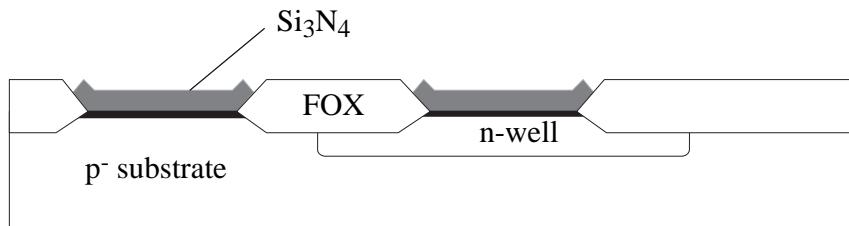
Step 4.) Implantation of the p-type field channel stop



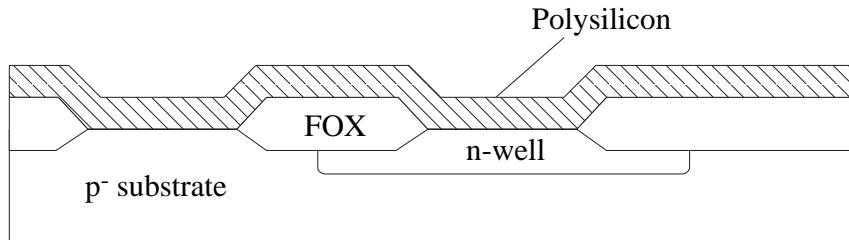
070523-02

Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - *localized oxidation of silicon*)



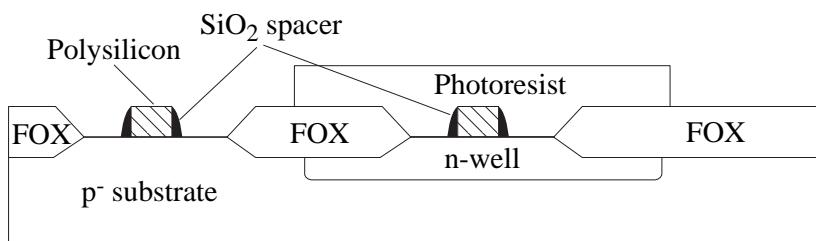
Step 6.) Growth of the gate thin oxide and deposition of polysilicon. The thresholds can be shifted by an implantation before the deposition of polysilicon.



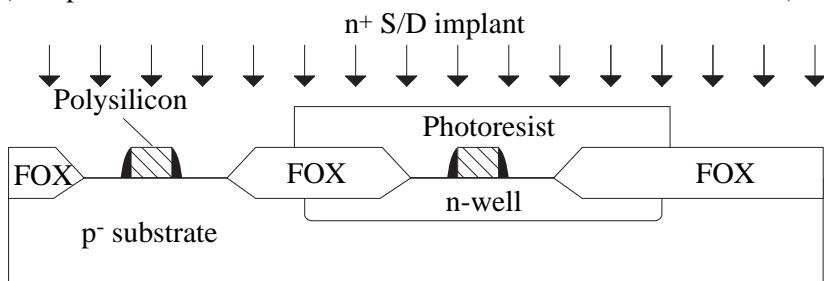
070523-03

Major CMOS Process Steps – Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



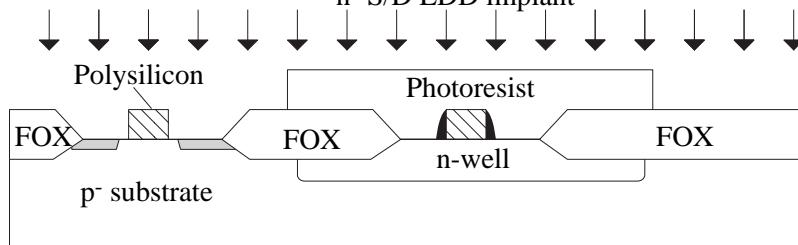
Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)



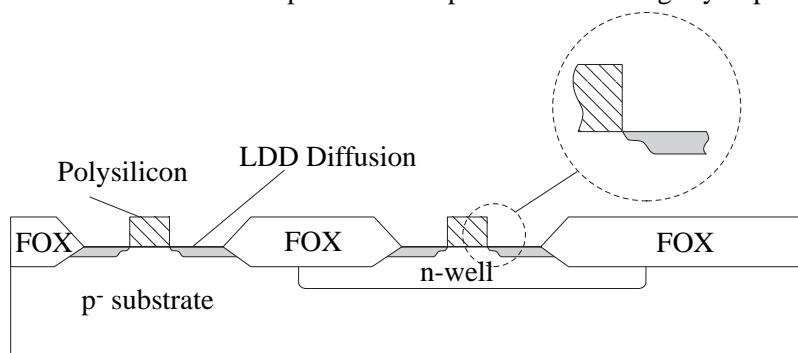
070523-04

Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drain
n- S/D LDD implant



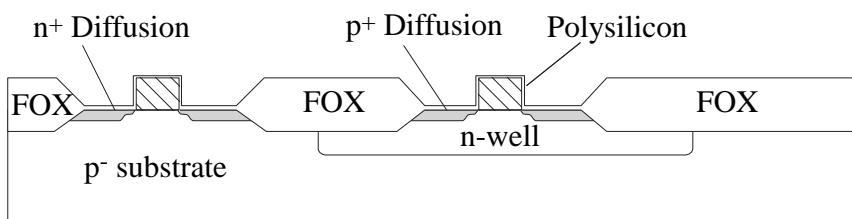
Step 10.) Implant the PMOS source/drain and contacts to the p- substrate (not shown),
remove the sidewall spacers and implant the PMOS lightly doped source/drain



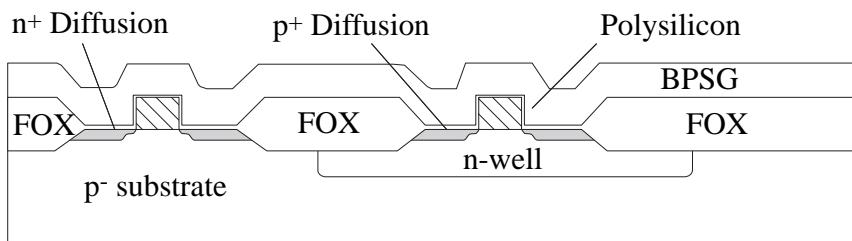
070209-03

Major CMOS Process Steps – Continued

Step 11.) Anneal to activate the implanted ions



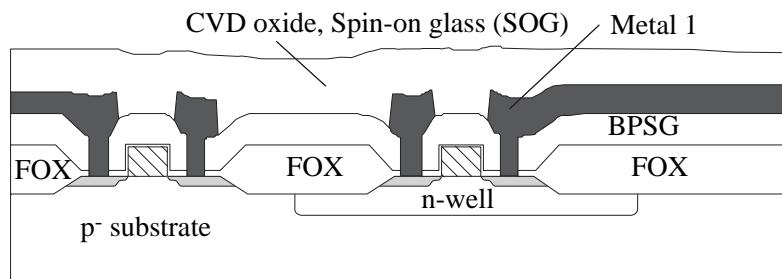
Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)



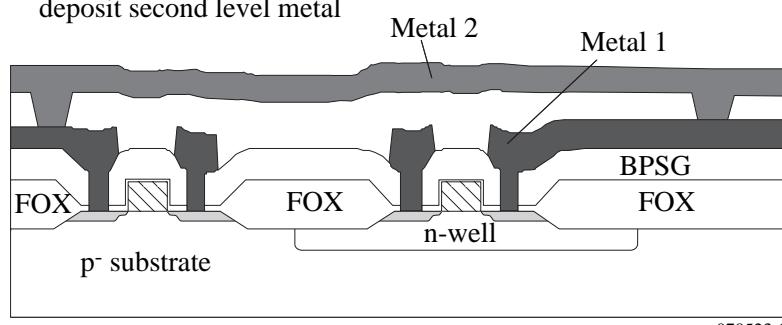
070523-05

Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



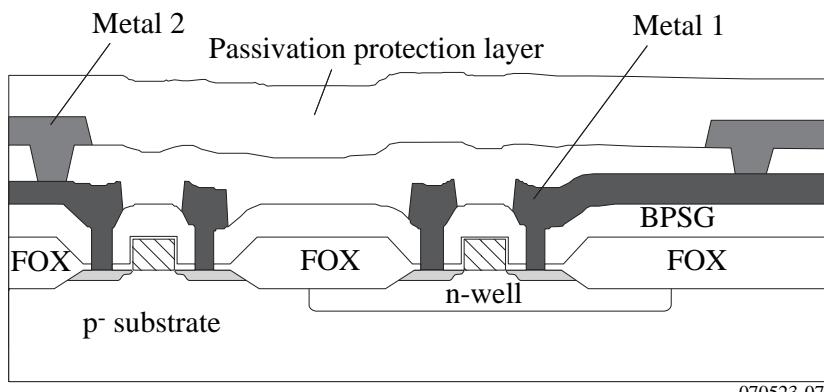
Step 14.) Deposit another interlayer dielectric (CVD SiO₂), open contacts, deposit second level metal



070523-06

Major CMOS Process Steps – Continued

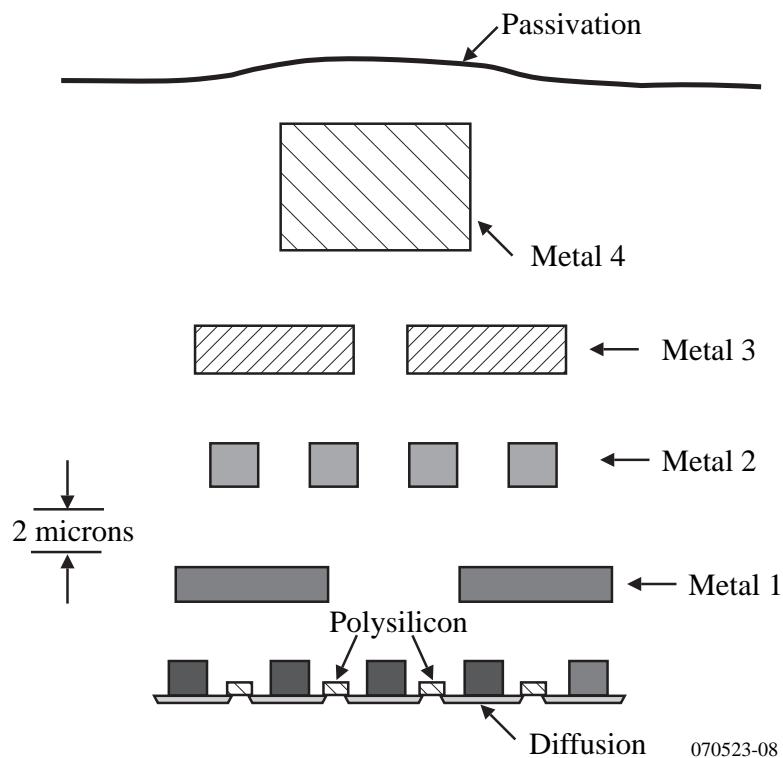
Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads



070523-07

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Approximate Side View of CMOS Fabrication

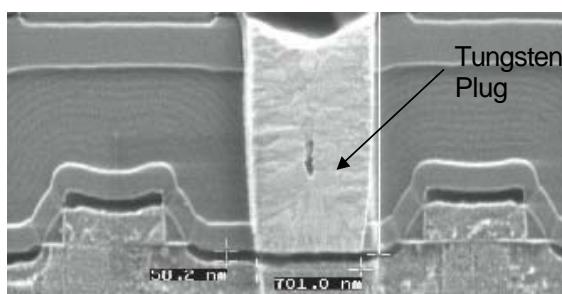


Planarization

Planarization attempts to minimize the variation in surface height of the wafer.

Planarization techniques

- Repeated applications of SOG
- Resist etch-back – highest areas of oxide are exposed longest to the etchant and therefore erode away the most.



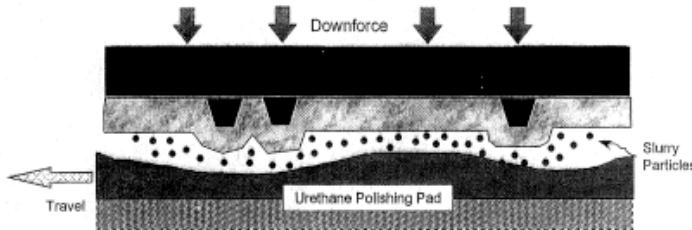
Influence of planarization on analog design:

- + Number of levels of metal and the metal integrity depends on planarization
- + Thin film components at the surface require good planarization
- + Without planarization, resistance of conductors increases
- + Planarization at the top level leads to less package induced stress (trimming?)
- + Planarized passivation helps printing when the depth of field is small.
- With planarization, the capacitance of the interdielectric isolation can vary (a good reason to extract capacitance!)
- Significant difference in contact aspect ratio (deep versus shallow contacts)

Chemical Mechanical Polishing

CMP produces the required degree of planarization for modern submicron technology.

Schematic diagram of the dielectric planarization process

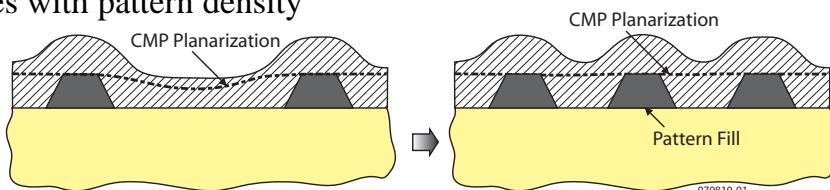


- Both chemical effect (slurry) and mechanical (pad pressure) take place.
- Although CMP is superior to SOG and resist etchback, large areas devoid of underlying metal or poly produce low regions in the final surface.
- Challenge: Achieve a highly planarized surface over a wide range of pattern density.

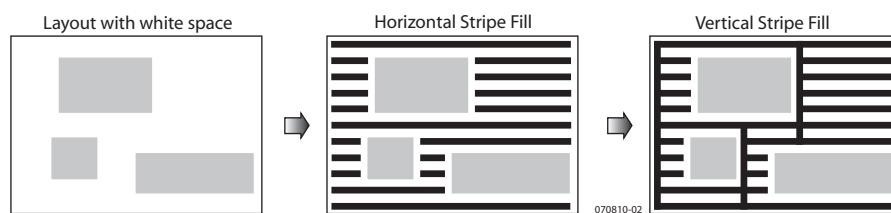
Chemical Mechanical Polishing – Continued

Impact on analog design:

- + Makes the surface flatter
- Vias and plugs can become longer adding resistance
- + More uniform surface giving better metal coverage and foundation for thin film components
- Thickness varies with pattern density



Examples of pattern fill:

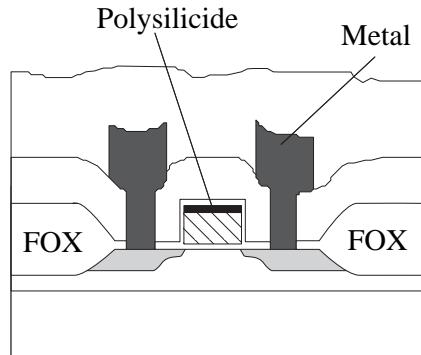


Pattern density design rules are both local and global.

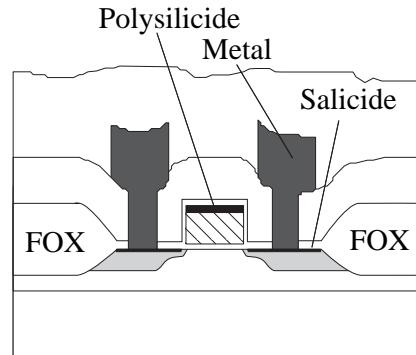
Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as TiSi_2 , WSi_2 , TaSi_2 , etc. on top of polysilicon

Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure



Salicide structure 070523-09

SUMMARY

- Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.
- Basic process steps include:

1.) Oxide growth	2.) Thermal diffusion	3.) Ion implantation
4.) Deposition	5.) Etching	6.) Epitaxy
- The complexity of a process can be measured in the terms of the number of masking steps or masks required to implement the process.
- Major CMOS Processing Steps:

1.) Well definition	2.) Definition of active areas and substrate/well contacts (SiNi_3)	3.) Thick field oxide (FOX)
4.) Thin field oxide and polysilicon	5.) Diffusion of the source and drains (includes the LDD)	6.) Dielectric layer/Contacts (planarization)
7.) Metallization	8.) Dielectric layer/Vias	

LECTURE 030 - DEEP SUBMICRON (DSM) CMOS TECHNOLOGY

LECTURE ORGANIZATION

Outline

- Characteristics of a deep submicron CMOS technology
- Typical deep submicron CMOS technology
- Summary

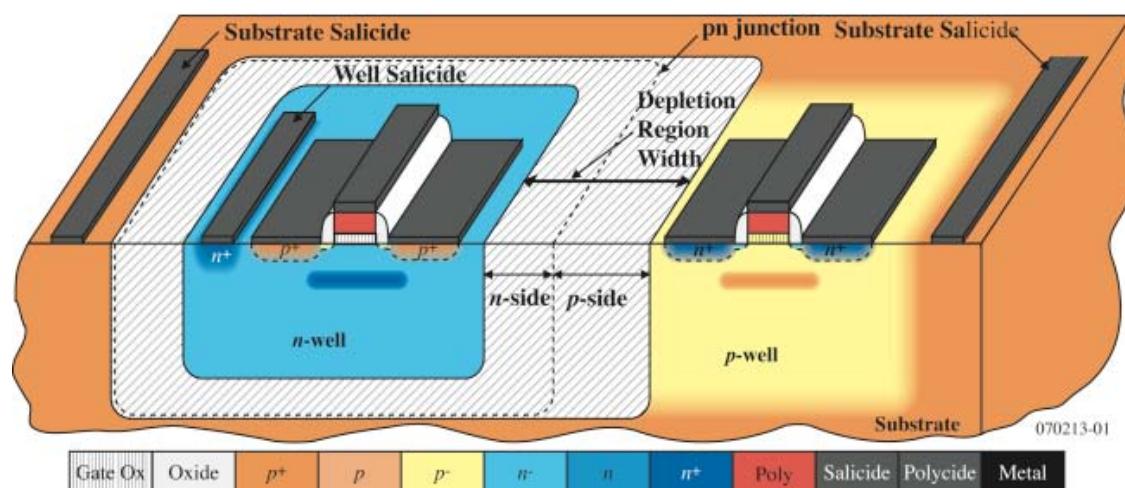
CMOS Analog Circuit Design, 2nd Edition Reference

New material

CHARACTERISTICS OF A DEEP SUBMICRON CMOS TECHNOLOGY

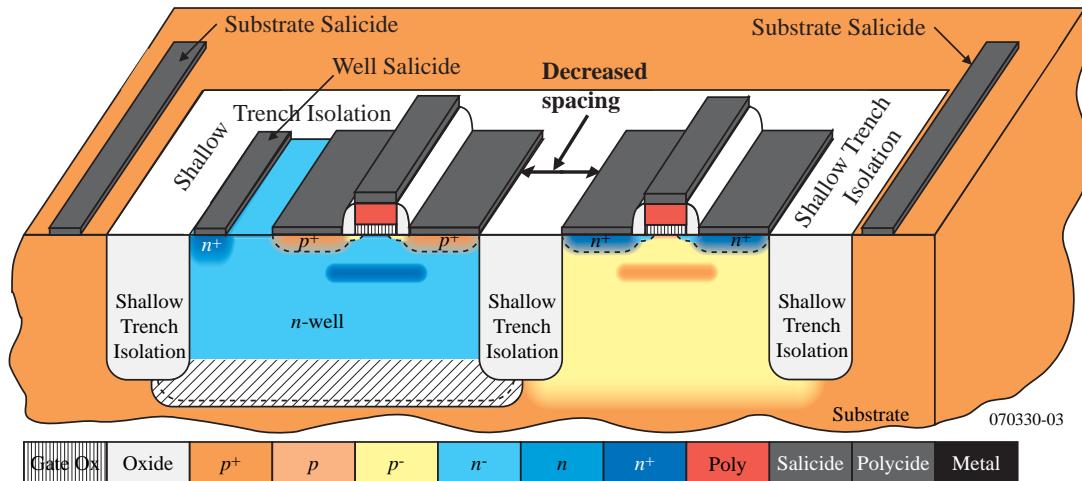
Isolation of Transistors

The use of reverse bias pn junctions to isolate transistors becomes impractical as the transistor sizes decrease.



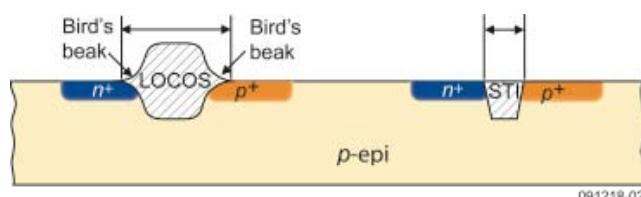
Use of Shallow Trench Isolation Technology

Shallow trench isolation (STI) allows closer spacing of transistors by eliminating the depletion region at the surface.



Comparison of STI and LOCOS

What are the differences between a LOCOS and STI technology?



Comments:

- If the n^+ to p^+ spacing is large, the Bird's beak can be compensated using techniques such as poly buffered LOCOS
- At some point as the n^+ to p^+ spacing gets smaller, the restricted bird's beak leads to undesirable stress effects in the transistor.
- An important advantage of STI is that it minimizes the heat cycle needed for n^+ or p^+ isolation compared to LOCOS. This is a significant advantage for any process where there are implants before STI.

Shallow Trench Isolation (STI)

- 1.) Cover the wafer with pad oxide and silicon nitride.
- 2.) First etch nitride and pad oxide. Next, an anisotropic etch is made in the silicon to a depth of 0.4 to 0.5 microns.
- 3.) Grow a thin thermal oxide layer on the trench walls.
- 4.) A CVD dielectric film is used to fill the trench.
- 5.) A chemical mechanical polishing (CMP) step is used to polish back the dielectric layer until the nitride is reached. The nitride acts like a CMP stop layer.
- 6.) Densify the dielectric material at 900°C and strip the nitride and pad oxide.

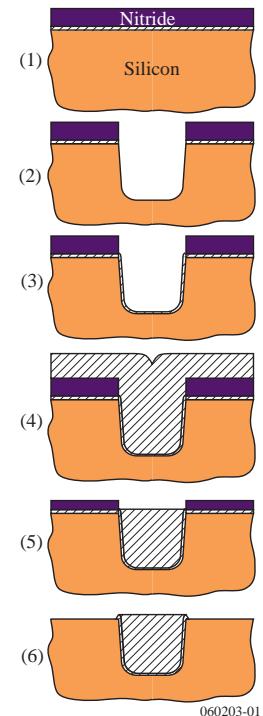
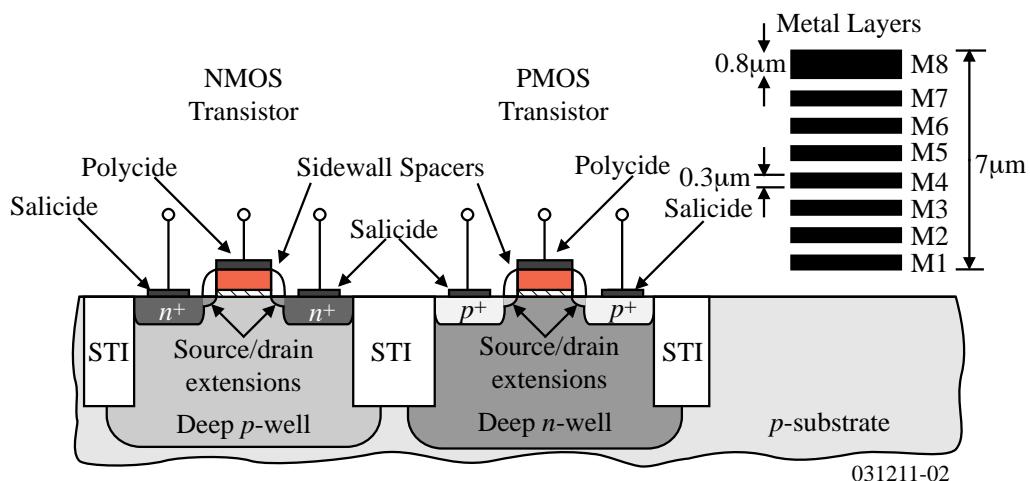


Illustration of a Deep Submicron (DSM) CMOS Technology

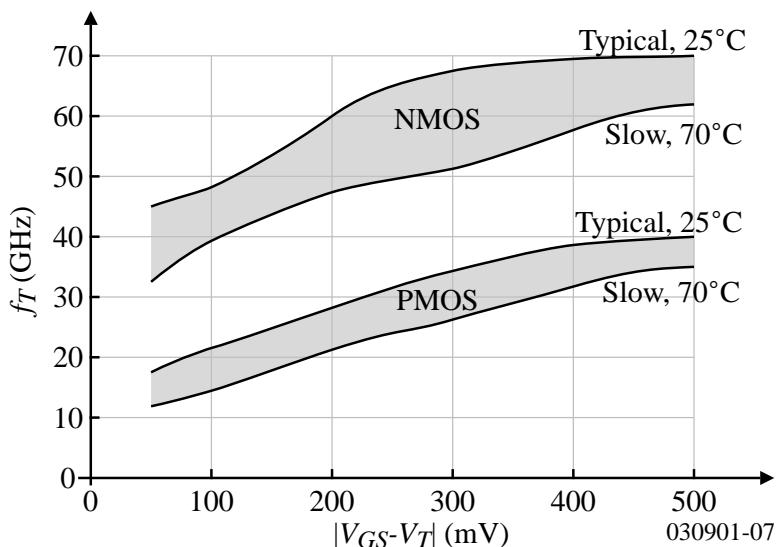


In addition to NMOS and PMOS transistors, the technology provides:

- 1.) A deep n -well that can be utilized to reduce substrate noise coupling.
- 2.) A MOS varactor that can serve in VCOs
- 3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

Transistors

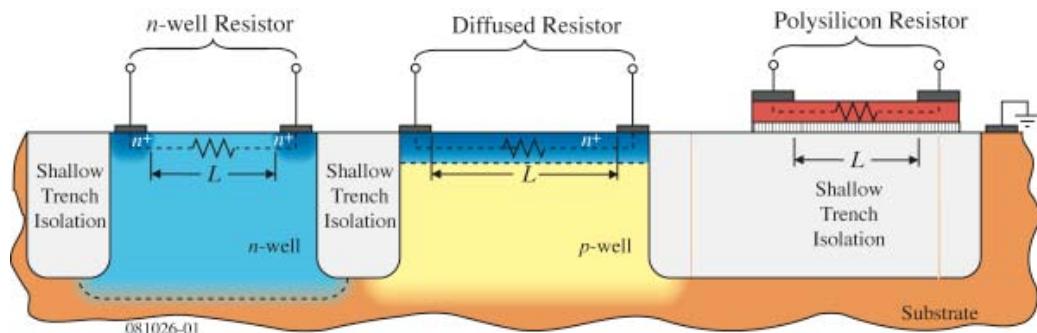
f_T as a function of gate-source overdrive, $V_{GS} - V_T$ ($0.13\mu\text{m}$):



The upper frequency limit is probably around 40 GHz for NMOS with an f_T in the vicinity of 60GHz with an overdrive of 0.5V and at the slow-high temperature corner.

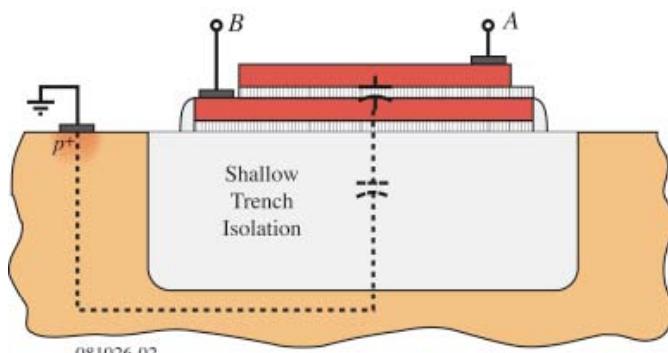
Resistors

- 1.) Diffused and/or implanted resistors.
- 2.) Well resistors.
- 3.) Polysilicon resistors.
- 4.) Metal resistors.

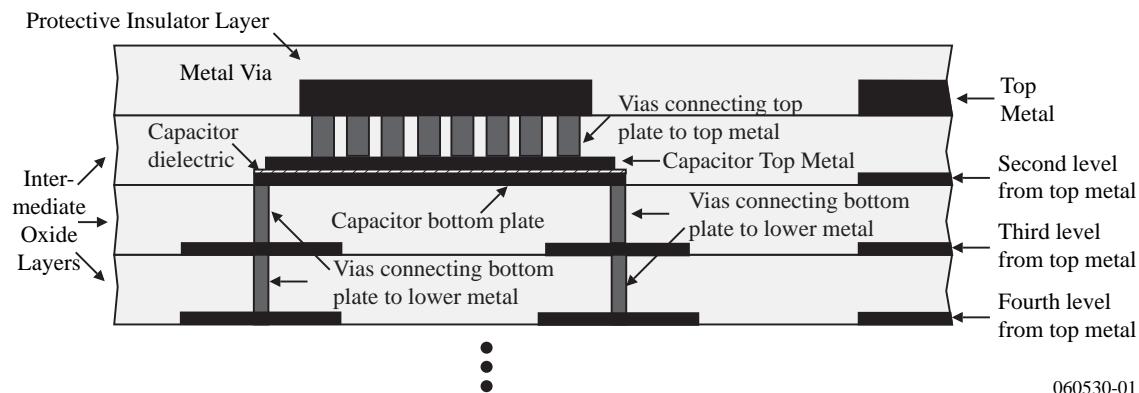


Capacitors

Polysilicon-polysilicon capacitors:

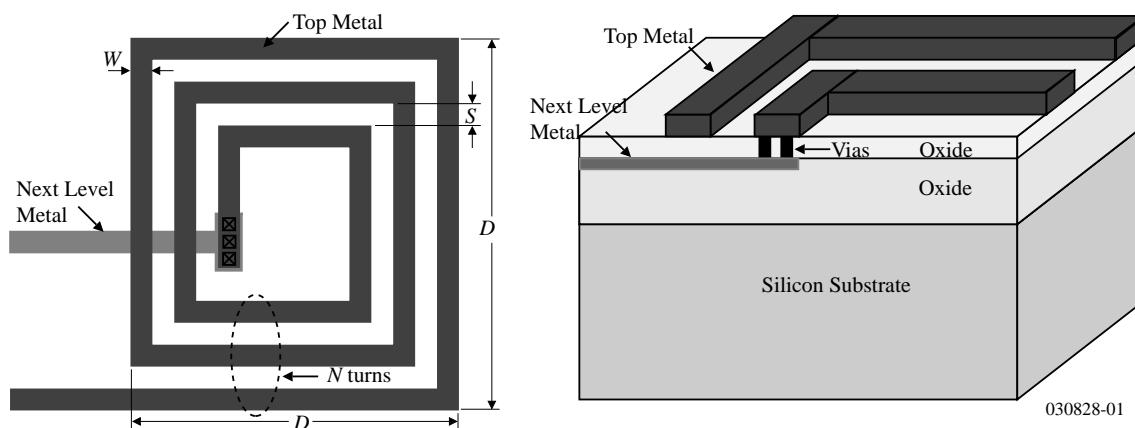


Metal-metal capacitors:



Inductors

Top view and cross-section of a planar inductor:



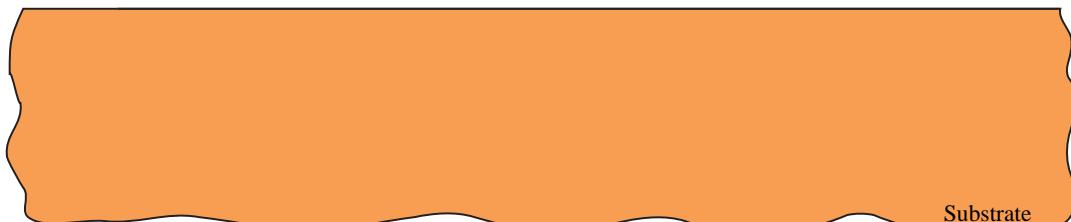
TYPICAL DEEP SUBMICRON (DSM) CMOS FABRICATION PROCESS

Major Fabrication Steps for a DSM CMOS Process

- 1.) p and n wells
- 2.) Shallow trench isolation
- 3.) Threshold shift and anti-punch through implants
- 4.) Thin oxide and gate polysilicon
- 5.) Lightly doped drains and sources
- 6.) Sidewall spacer
- 7.) Heavily doped drains and sources
- 8.) Siliciding (Salicide and Polycide)
- 9.) Bottom metal, tungsten plugs, and oxide
- 10.) Higher level metals, tungsten plugs/vias, and oxide
- 11.) Top level metal, vias and protective oxide

Starting Material

The substrate should be highly doped to act like a good conductor.

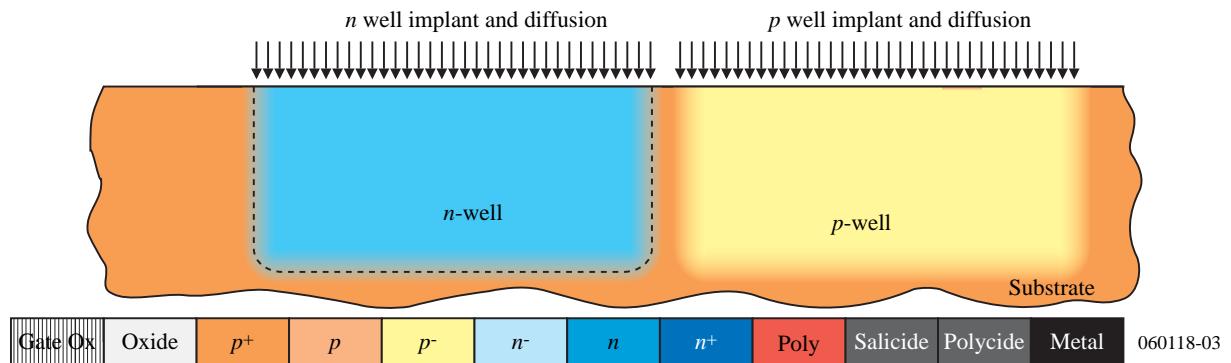


Gate Ox	Oxide	p^+	p	p^-	n^-	n	n^+	Poly	Salicide	Polycide	Metal	060118-02
---------	-------	-------	-----	-------	-------	-----	-------	------	----------	----------	-------	-----------

Step 1 - *n* and *p* wells

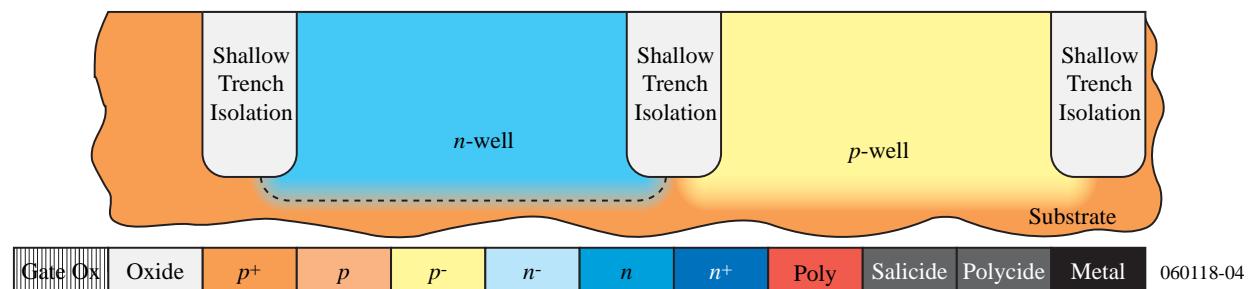
These are the areas where the transistors will be fabricated - NMOS in the *p*-well and PMOS in the *n*-well.

Done by implantation followed by a deep diffusion.



Step 2 – Shallow Trench Isolation

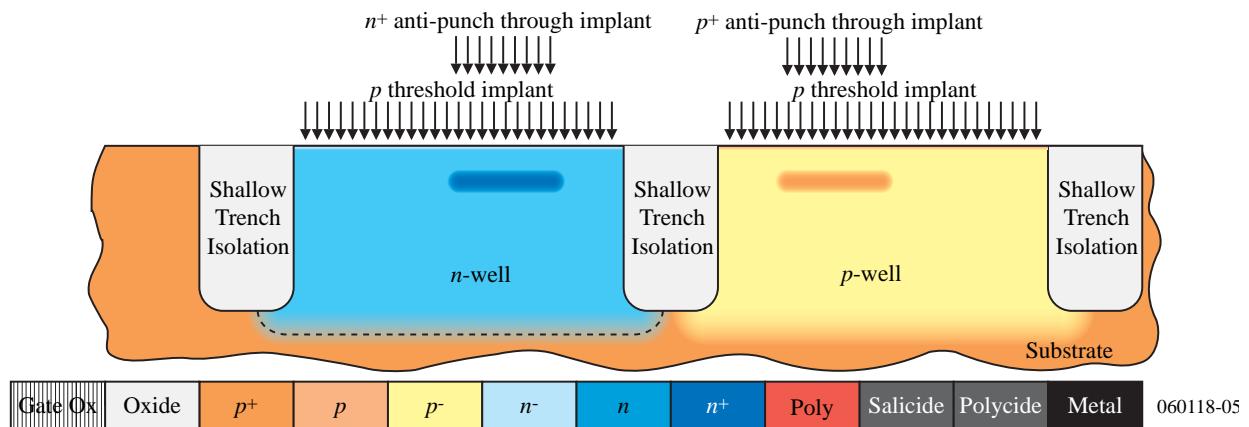
The shallow trench isolation (STI) electrically isolates one region/transistor from another.



Step 3 – Threshold Shift and Anti-Punch Through Implants

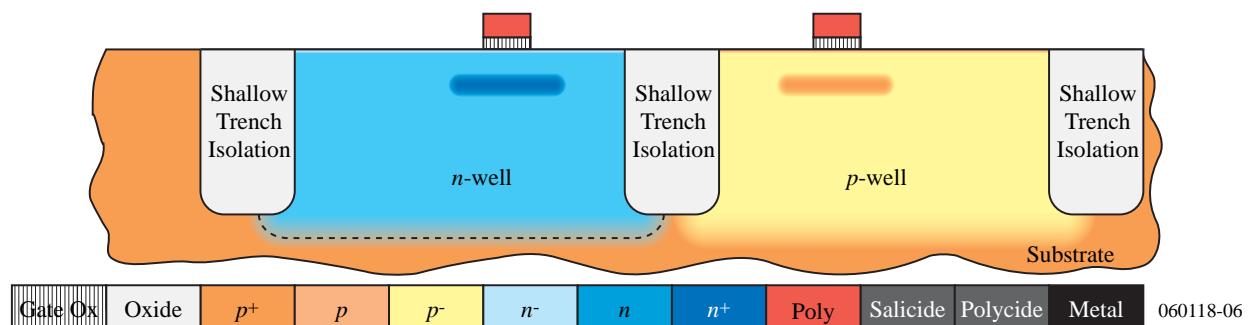
The natural thresholds of the NMOS is about 0V and of the PMOS is about -1.2V. An *p*-implant is used to make the NMOS harder to invert and the PMOS easier resulting in threshold voltages balanced around zero volts.

Also an implant can be applied to create a higher-doped region beneath the channels to prevent punch-through from the drain depletion region extending to source depletion region.



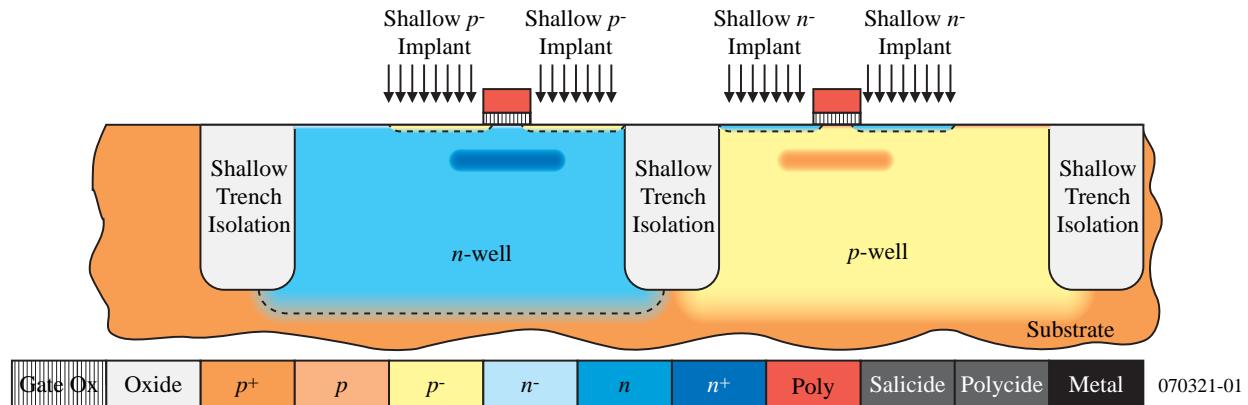
Step 4 – Thin Oxide and Polysilicon Gates

A thin oxide is deposited followed by polysilicon. These layers are removed where they are not wanted.



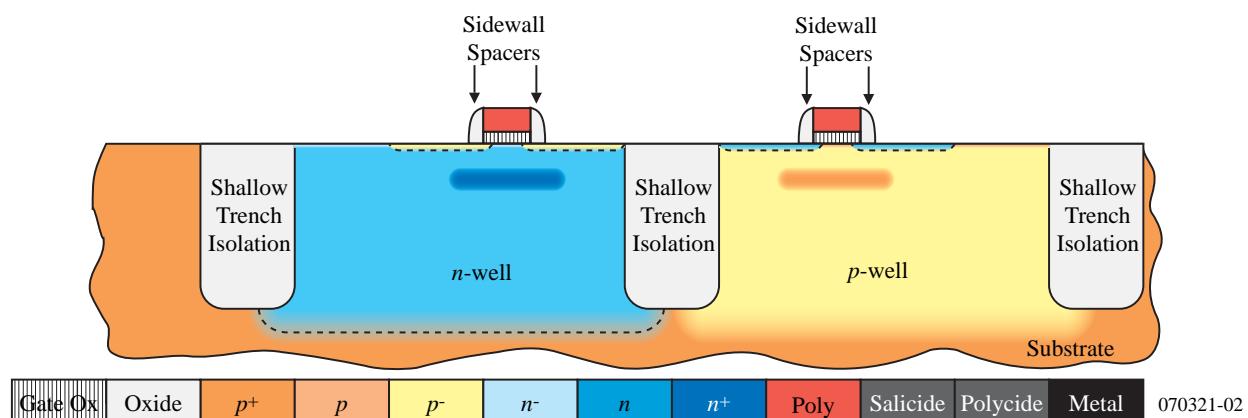
Step 5 – Lightly Doped Drains and Sources

A lightly-doped implant is used to create a lightly-doped source and drain next to the channel of the MOSFETs.



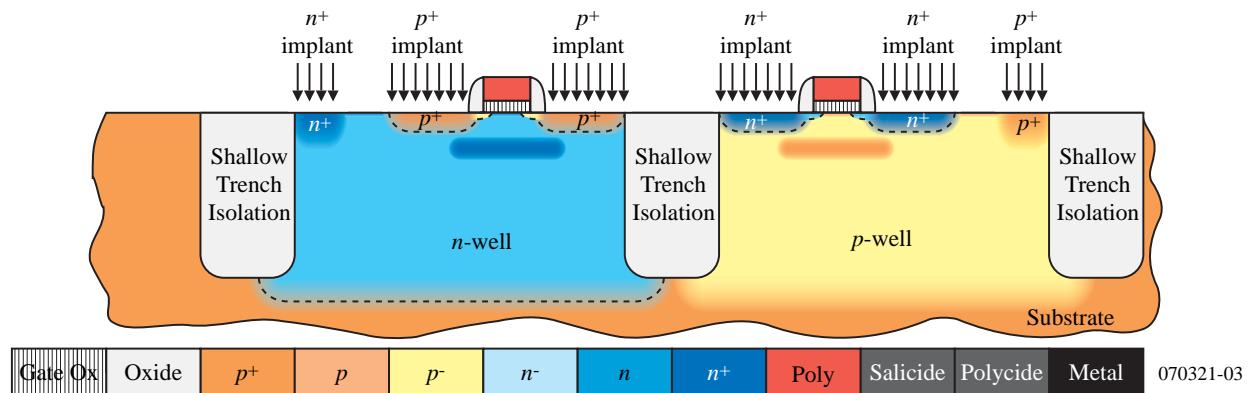
Step 6 – Sidewall Spacers

A layer of dielectric is deposited on the surface and removed in such a way as to leave “sidewall spacers” next to the thin-oxide-polysilicon-polycide sandwich. These sidewall spacers will prevent the part of the source and drain next to the channel from becoming heavily doped.



Step 7 – Implantation of the Heavily Doped Sources and Drains

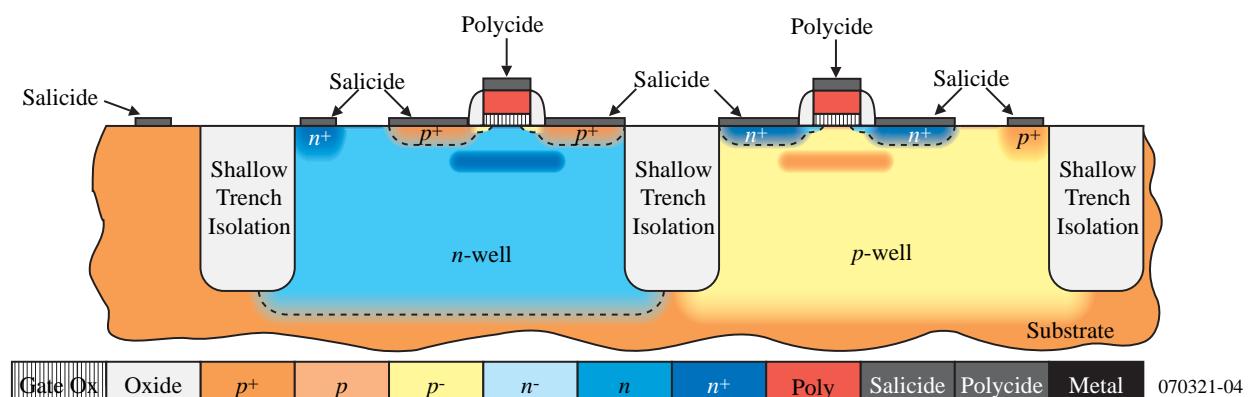
Note that not only does this step provide the completed sources and drains but allows for ohmic contact into the wells and substrate.



Step 8 – Siliciding (Salicide and Polycide)

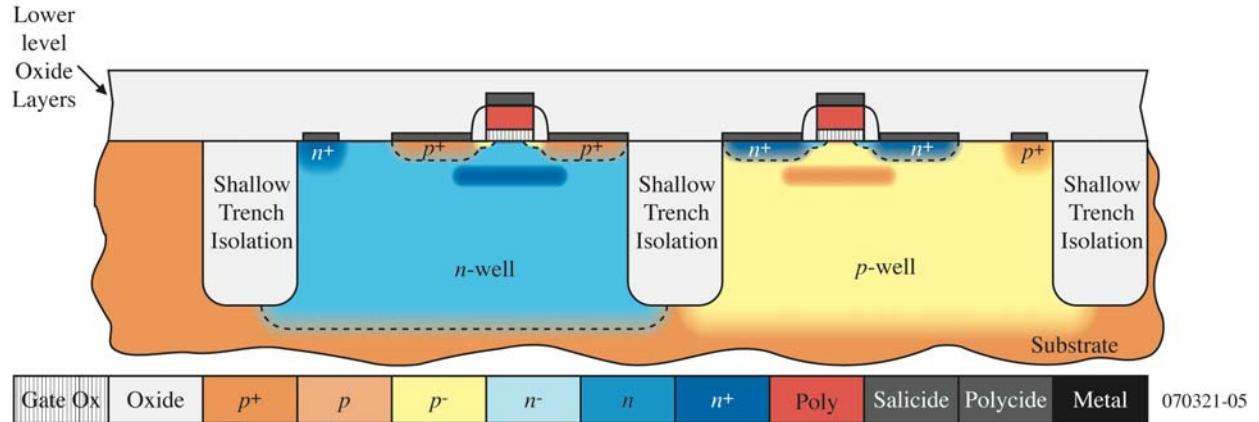
This step reduces the resistance of the bulk diffusions and polysilicon and forms an ohmic contact with material on which it is deposited.

Salicide = Self-aligned silicide



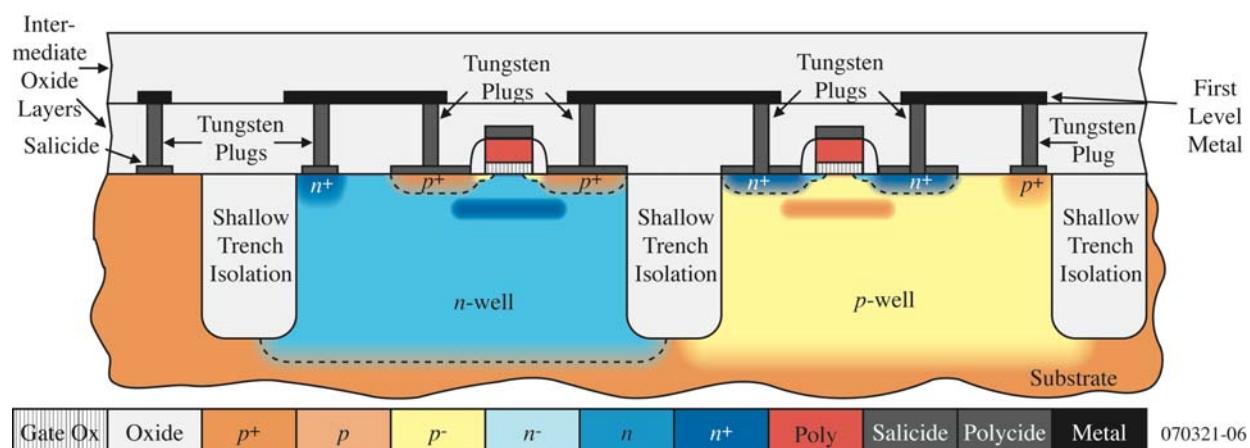
Step 9 – Intermediate Oxide Layer

An oxide layer is used to cover the transistors and to planarize the surface.



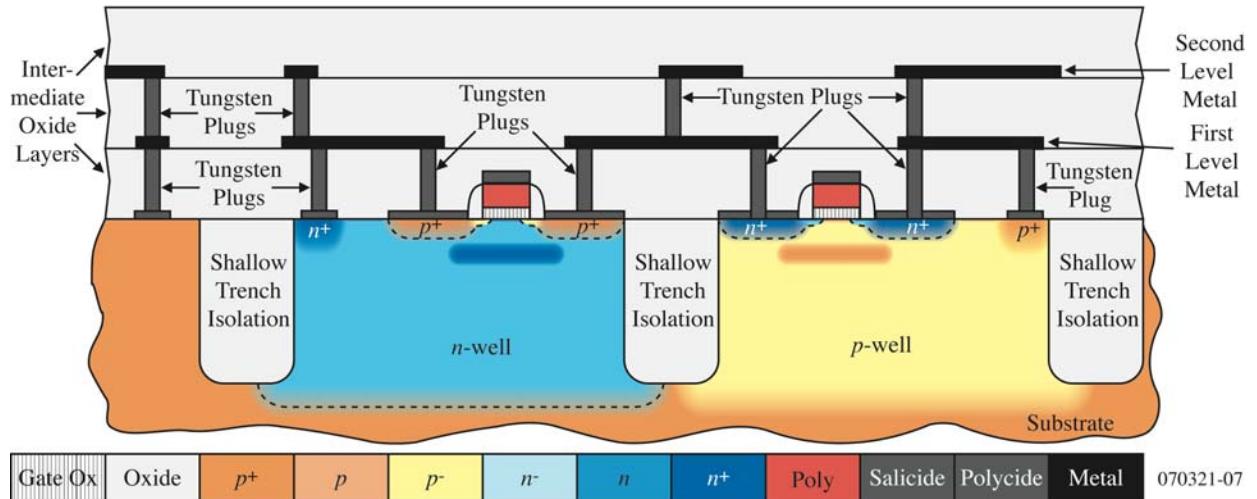
Step 10- First-Level Metal

Tungsten plugs are built through the lower intermediate oxide layer to provide contact between the devices, wells and substrate to the first-level metal.



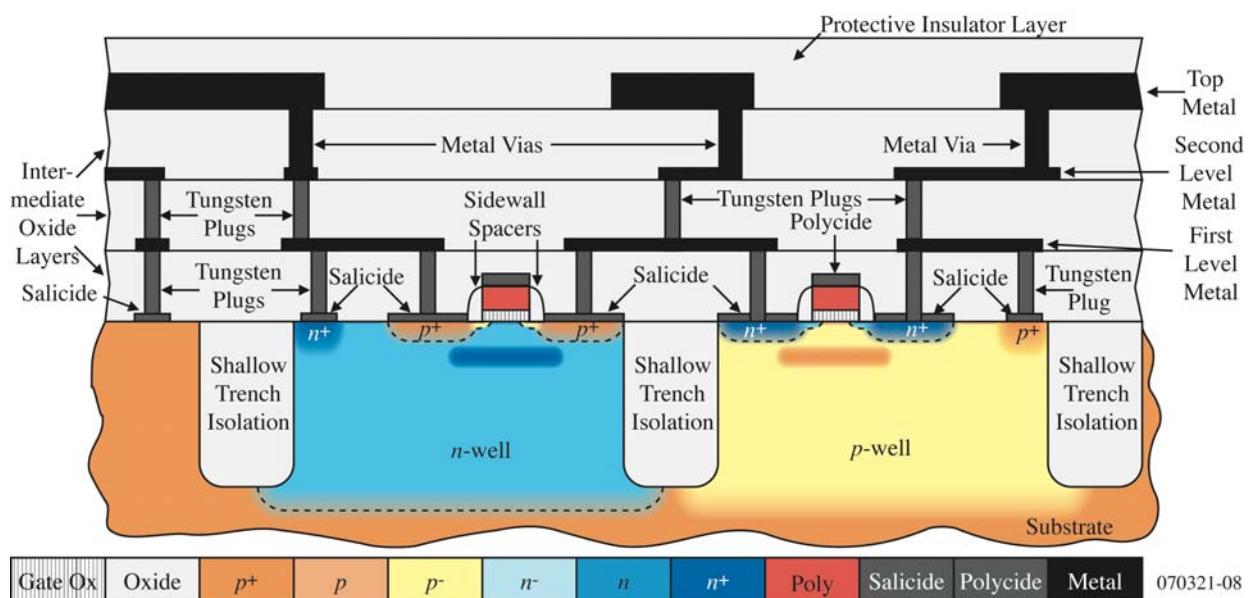
Step 11 – Second-Level Metal

The previous step is repeated for the second-level metal.



Completed Fabrication

After multiple levels of metal are applied, the fabrication is completed with a thicker top-level metal and a protective layer to hermetically seal the circuit from the environment. Note that metal is used for the upper level metal vias. The chip is electrically connected by removing the protective layer over large bonding pads.



Scanning Electron Microscope of a MOSFET Cross-section

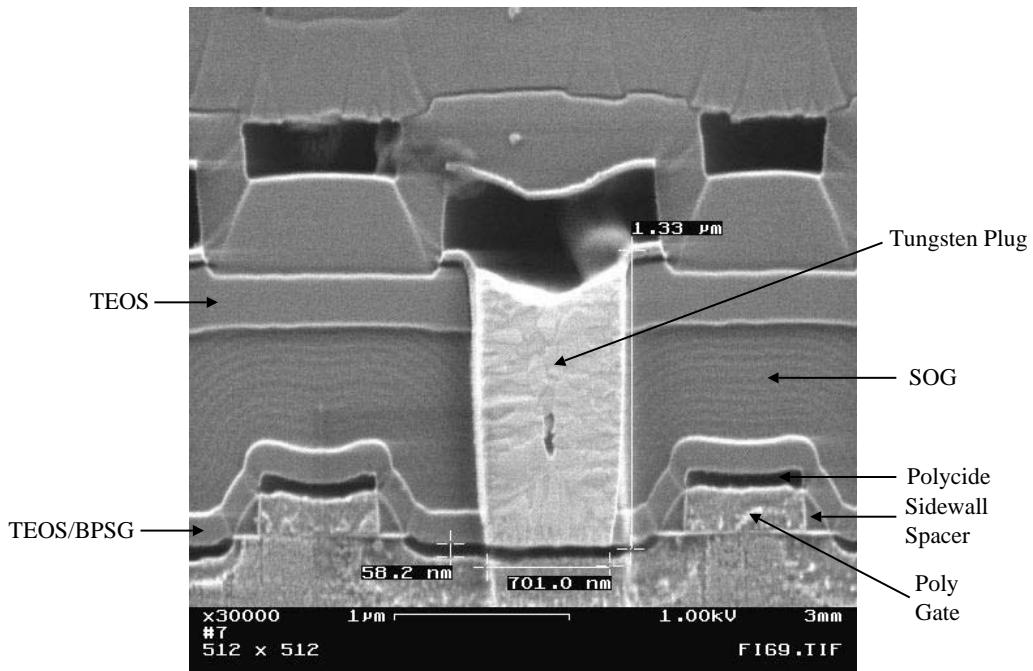


Fig. 2.8-20

Scanning Electron Microscope Showing Metal Levels and Interconnect

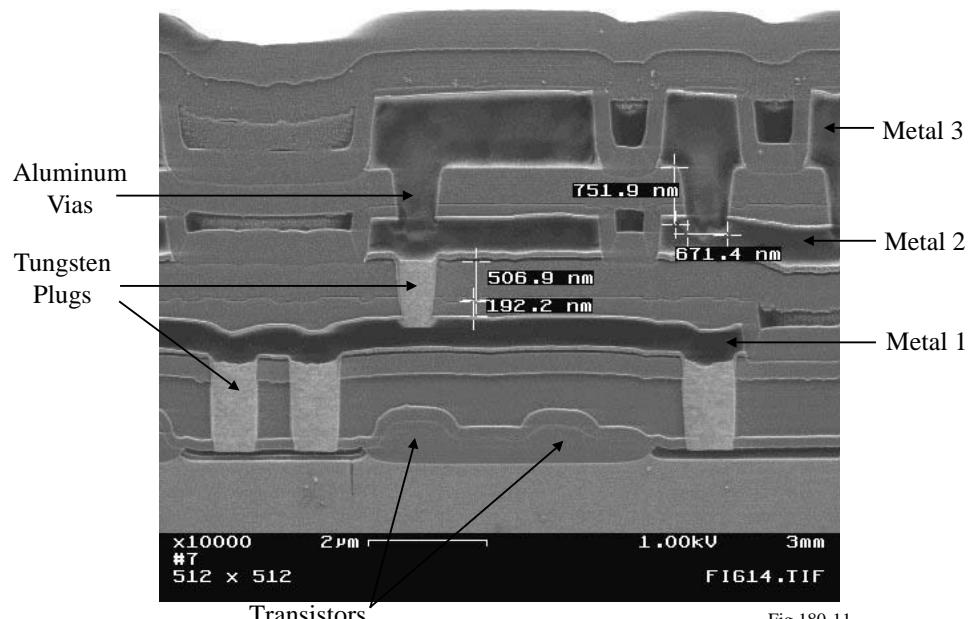


Fig.180-11

SUMMARY

- DSM technology typically has a minimum channel length between $0.35\mu\text{m}$ and $0.1\mu\text{m}$
- DSM technology addresses the problem of excessive depletion region widths in junction isolation techniques by using shallow trench isolation
- DSM technology may have from 4 to 8 levels of metal
- Lightly doped drains and sources are a key aspect of DSM technology

LECTURE 040 - ULTRA-DEEP SUBMICRON AND BiCMOS TECHNOLOGIES

LECTURE ORGANIZATION

Outline

- Ultra-deep submicron CMOS technology
 - Features
 - Advantages
 - Problems
- BiCMOS technology process flow
 - CMOS is typical submicron ($0.5 \mu\text{m}$)
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

New material

ULTRA-DEEP SUBMICRON (UDSM) CMOS TECHNOLOGY

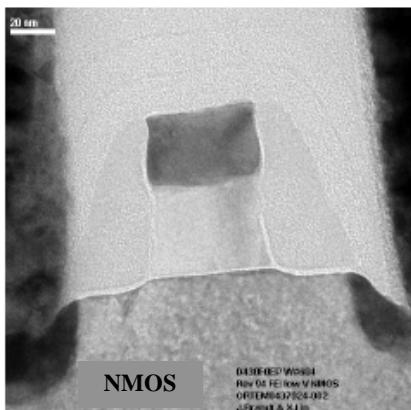
UDSM Technology

- $L_{min} \leq 0.1$ microns
- Minimum feature size less than 100 nanometers
- Today's state of the art:
 - 65 nm drawn length
 - 15 nm lateral diffusion (35 nm gate length)
 - 1.2 nm transistor gate oxide
 - 8 layers of copper interconnect
- Specialized processing is used to increase drive capability and maintain low off currents

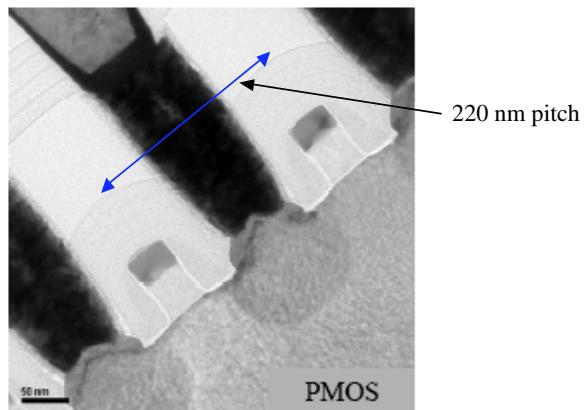
65 Nanometer CMOS Technology

TEM cross-section of a 35 nm NMOS and PMOS transistors.[†]

NMOS:



PMOS:



These transistors utilize enhanced channel strains to increase drive capability and to reduce off currents.

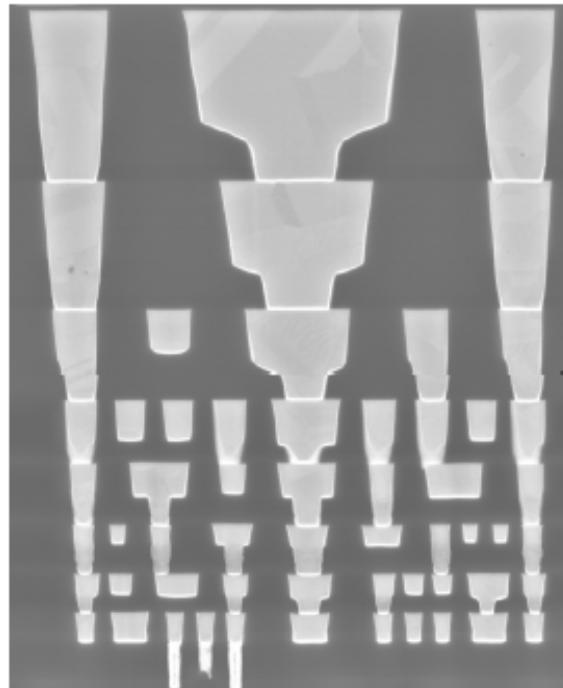
[†] P. Bai, et. Al., “A 65nm Lobic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell, *IEEE Inter. Electron Device Meeting*, Dec. 12-15, 2005.

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UDSM Metal and Interconnects

Physical aspects:

Layer	Pitch (nm)	Thickness (nm)	Aspect Ratio
Isolation	220	230	-
Polysilicon	220	90	-
Contacted Gate Pitch	220	-	-
Metal 1	210	170	1.6
Metal 2	210	190	1.8
Metal 3	220	200	1.8
Metal 4	280	250	1.8
Metal 5	330	300	1.8
Metal 6	480	430	1.8
Metal 7	720	650	1.8
Metal 8	1080	975	1.8



What are the Advantages of UDSM CMOS Technology?

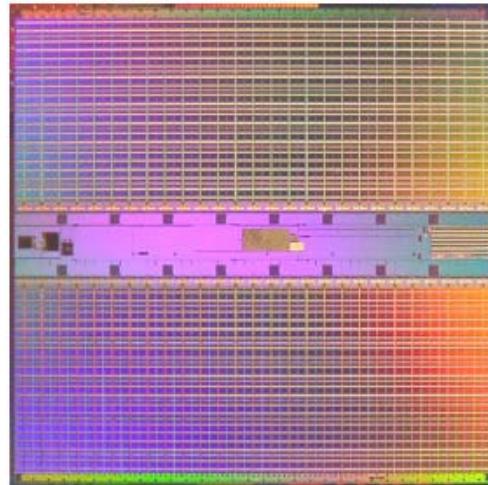
Digital Viewpoint:

- Improved I_{on}/I_{off}
- Reduced gate capacitance
- Higher drive current capability
- Reduced interconnect density
- Reduction of active power

Analog Viewpoint:

- More levels of metal
- Higher f_T
- Higher capacitance density
- Reduced junction capacitance per g_m

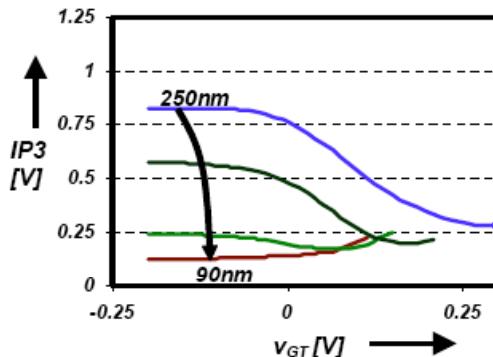
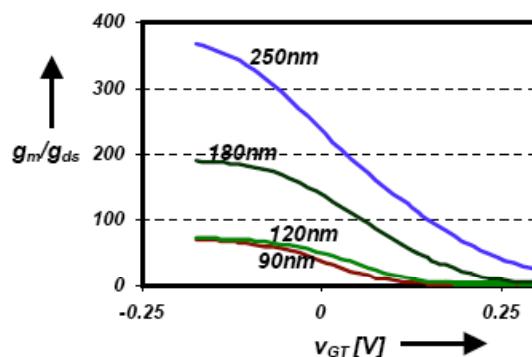
70 Mbit SRAM chip:



What are the Disadvantages of UDSM CMOS Technology (for Analog)?

- Reduction in power supply resulting in reduced headroom
- Gate leakage currents
- Reduced small-signal intrinsic gains
- Increased nonlinearity (IIP3)
- Noise and matching??

Intrinsic gain and IP3 as a function of the gate overdrive for decreasing V_{DS} :[†]



[†] Anne-Johan Annema, et. Al., "Analog Circuits in Ultra-Deep-Submicron CMOS," *IEEE J. of Solid-State Circuits*, Vol. 40, No. 1, Jan. 2005, pp. 132-143.

What is the Gate Leakage Problem?

Gate current occurs in thin oxide devices due to direct tunneling through the thin oxide.

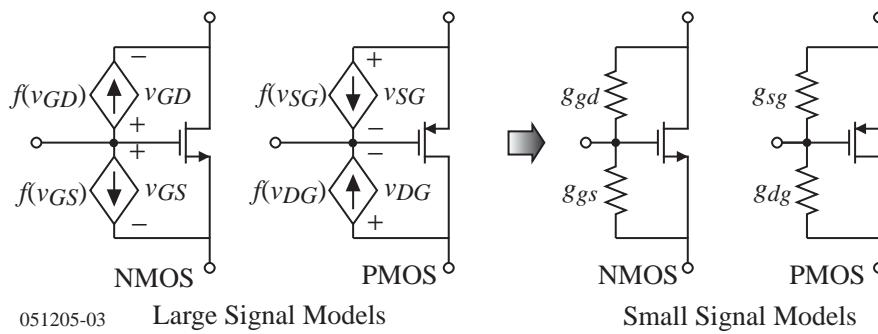
Gate current depends on:

- 1.) The gate-source voltage (and the drain-gate voltage)

$$i_{GS} = K_1 v_{GS} \exp(K_2 v_{GS}) \quad \text{and} \quad i_{GD} = K_3 v_{GD} \exp(K_4 v_{GD})$$

- 2.) Gate area – NMOS leakage $\approx 6\text{nA}/\mu\text{m}^2$ and PMOS leakage $\approx 3\text{nA}/\mu\text{m}^2$

Unfortunately, the gate leakage current is nonlinear with respect to the gate-source and gate-drain voltages. A possible model is:



051205-03 Large Signal Models

Small Signal Models

Base current cancellation schemes used for BJTs are difficult to apply to the MOSFET.

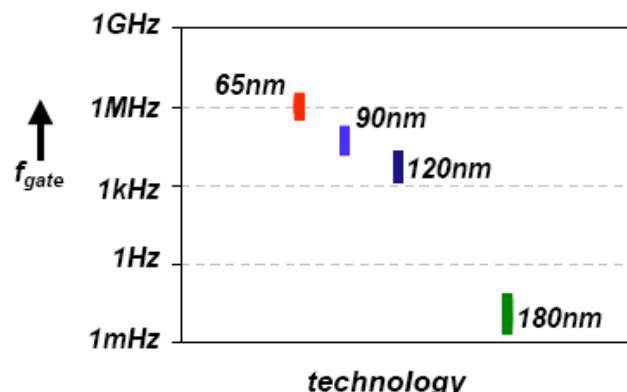
Gate Leakage and f_{gate}

The gate leakage can be represented by a conductance, g_{gate} , in parallel with the gate capacitance, C_{gate} . Since these two elements have identical area dependence, they result in a frequency, f_{gate} , that is fairly independent of the drain-source voltage, v_{ds} .

$$f_{gate} = \frac{g_{gate}}{2\pi C_{gate}} \approx \begin{cases} 1.5 \cdot 10^{16} v_{GS}^2 e^{t_{ox}(v_{GS}-13.6)} & (\text{NMOS}) \\ 0.5 \cdot 10^{16} v_{GS}^2 e^{t_{ox}(v_{GS}-13.6)} & (\text{PMOS}) \end{cases}$$

where t_{ox} is in nm and v_{GS} is in V.

For frequencies above f_{gate} the MOSFET looks capacitive and below f_{gate} , the MOSFET looks resistive (gate leakage).



UDSM CMOS Technology Summary

- Increased transconductance and frequency capability
- Low power supply voltages
- Reduced parasitics
- Gate leakage causes challenges for analog applications of UDSM technology
 - Can no longer use the MOSFET for capacitance
 - Conflict between matching and gate leakage
- Other issues
 - Noise
 - Zero temperature coefficient behavior
 - Etc.

BiCMOS TECHNOLOGY

Typical $0.5\mu\text{m}$ BiCMOS Technology

Masking Sequence:

- | | | |
|-----------------------|------------------------------|-------------------------|
| 1. Buried n^+ layer | 9. Base oxide/implant | 17. Contacts |
| 2. Buried p^+ layer | 10. Emitter implant | 18. Metal 1 |
| 3. Collector tub | 11. Poly 1 | 19. Via 1 |
| 4. Active area | 12. NMOS lightly doped drain | 20. Metal 2 |
| 5. Collector sinker | 13. PMOS lightly doped drain | 21. Via 2 |
| 6. n -well | 14. n^+ source/drain | 22. Metal 3 |
| 7. p -well | 15. p^+ source/drain | 23. Nitride passivation |
| 8. Emitter window | 16. Silicide protection | |

Notation used in the following slides:

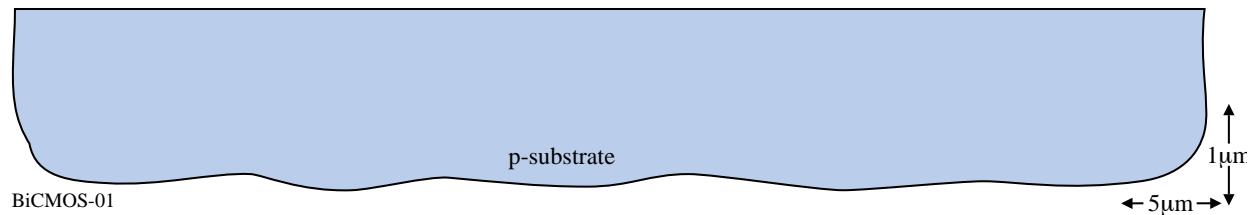
BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN₃ generated, during the field oxidation.

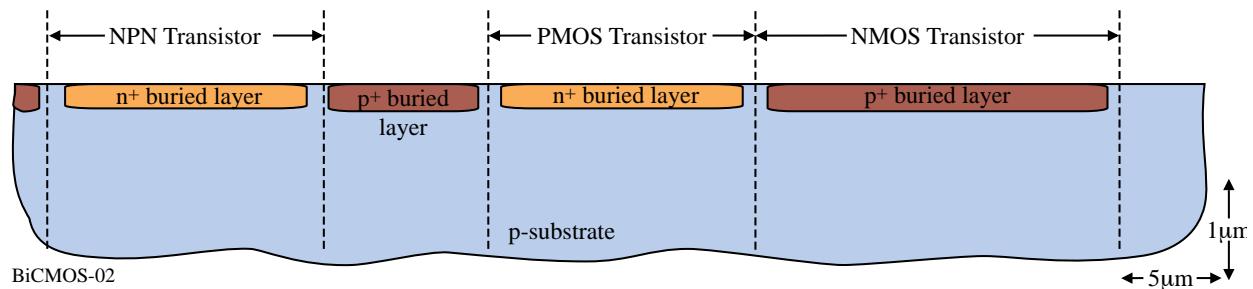
TEOS = Tetro-Ethyl-Ortho-Silicate. A chemical compound used to deposit conformal oxide films.

n⁺ and p⁺ Buried Layers

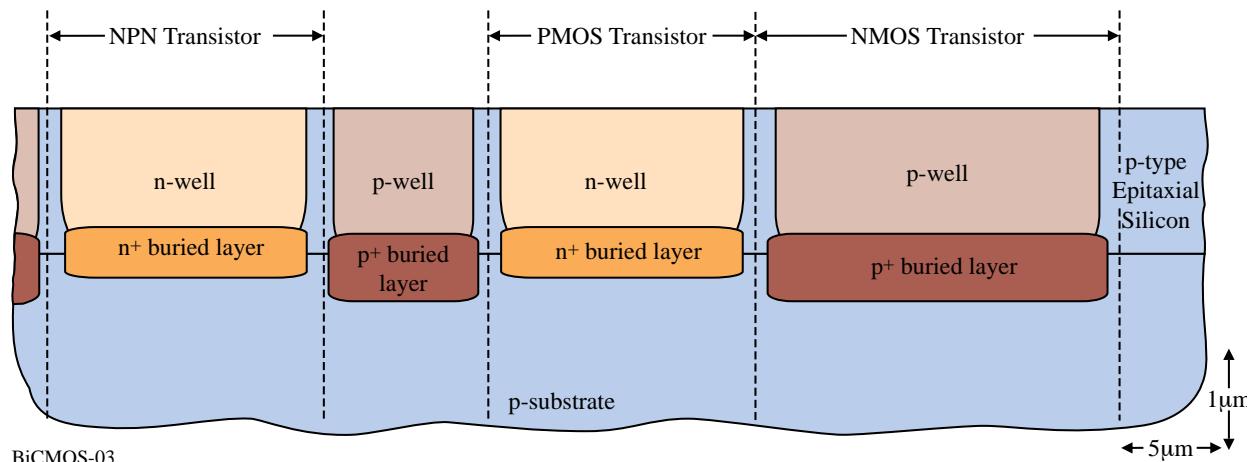
Starting Substrate:



n⁺ and p⁺ Buried Layers:



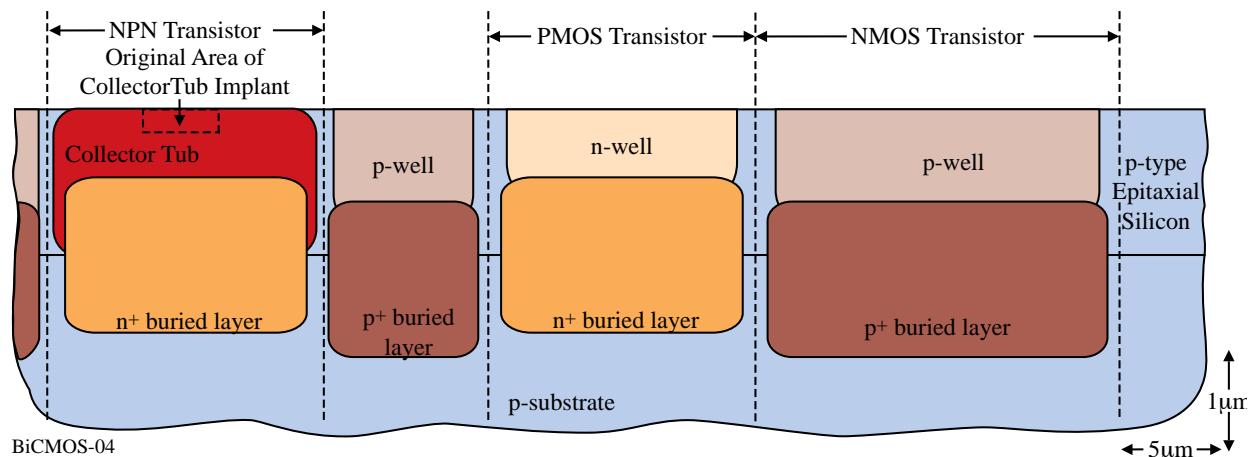
Epitaxial Growth



Comment:

- As the epi layer grows vertically, it assumes the doping level of the substrate beneath it.
- In addition, the high temperature of the epitaxial process causes the buried layers to diffuse upward and downward.

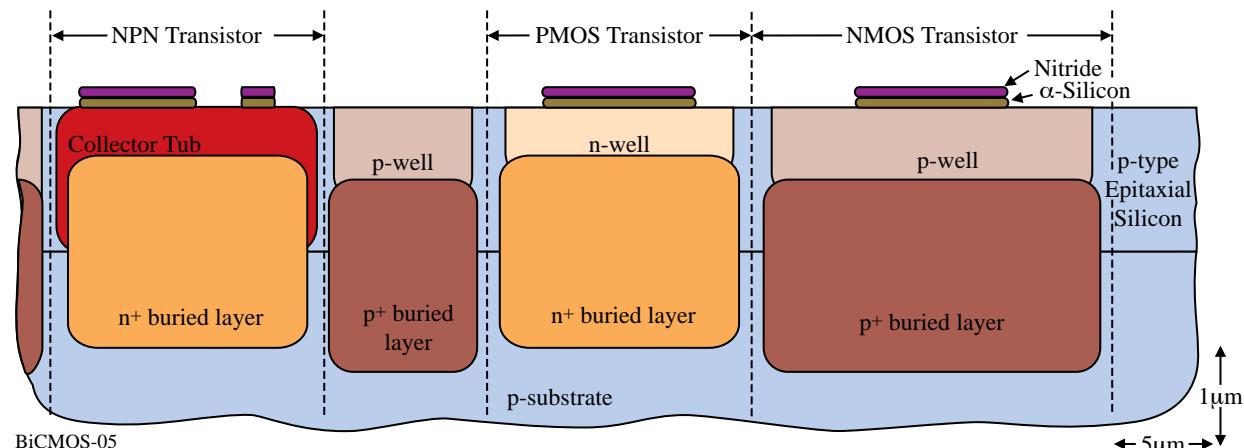
Collector Tub



Comment:

- The collector area is developed by an initial implant followed by a drive-in diffusion to form the collector tub.

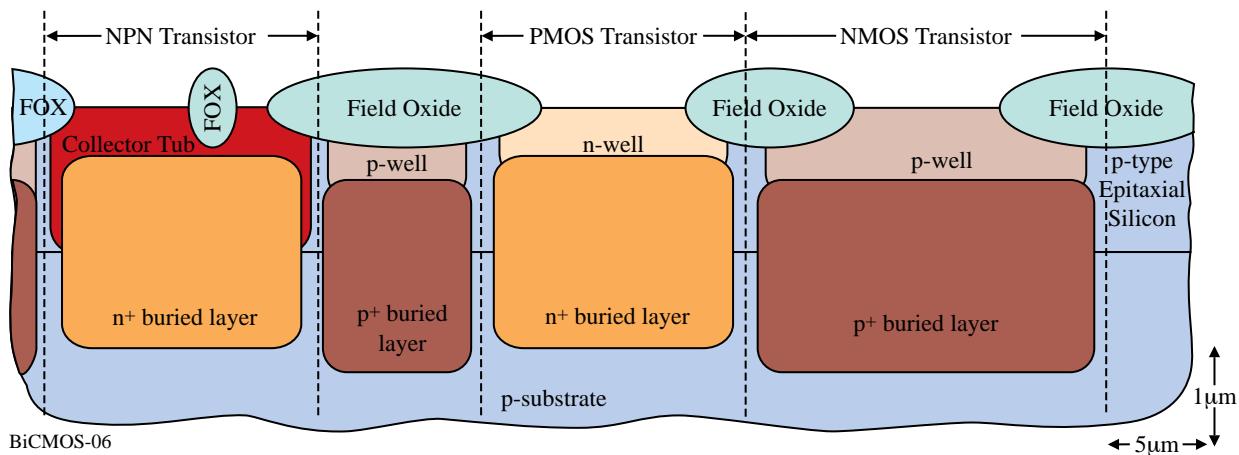
Active Area Definition



Comment:

- The silicon nitride is used to impede the growth of the thick oxide which allows contact to the substrate
- α -silicon is used for stress relief and to minimize the bird's beak encroachment

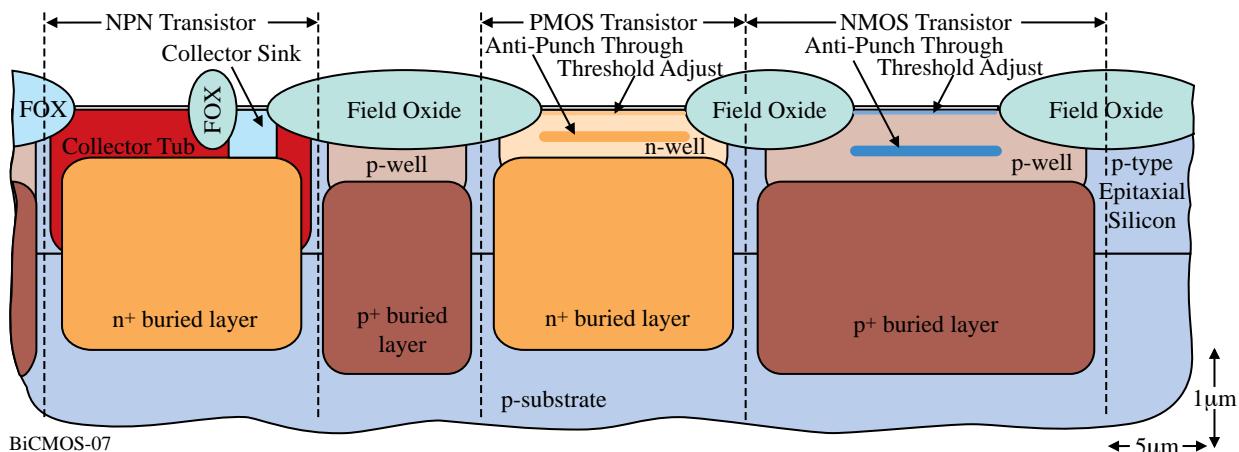
Field Oxide



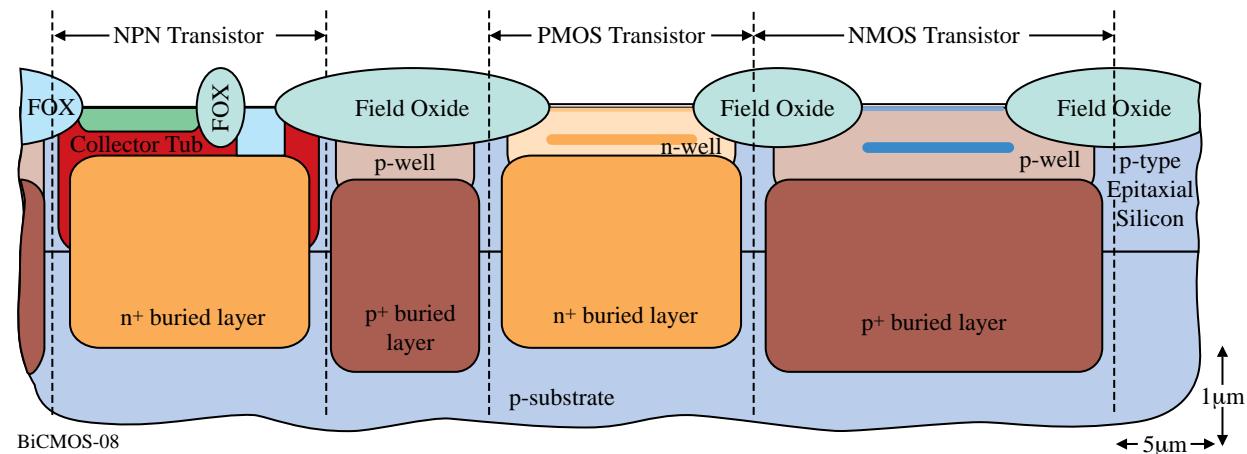
Comments:

- The field oxide is used to isolate surface structures (i.e. metal) from the substrate

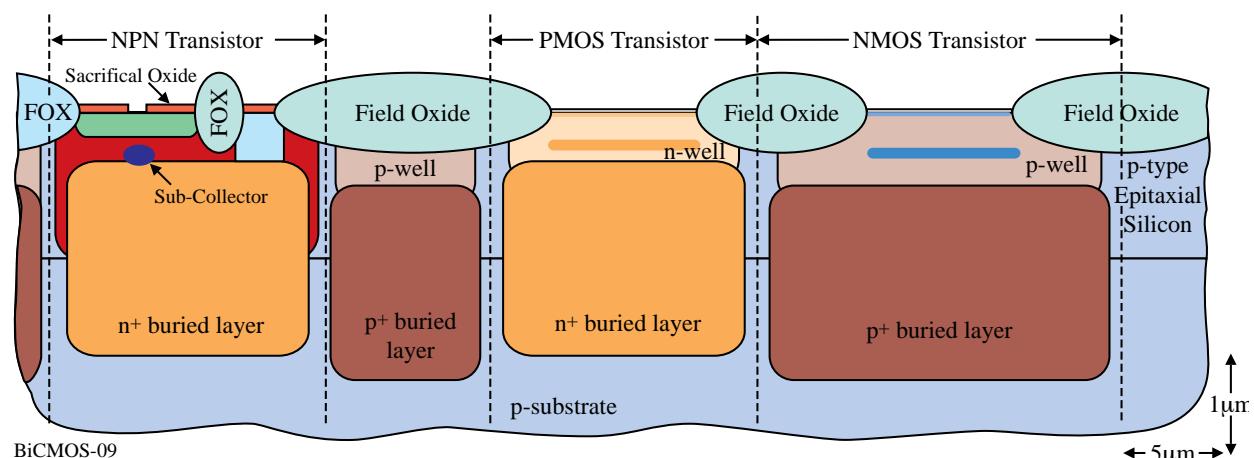
Collector Sink and n-Well and p-Well Definitions



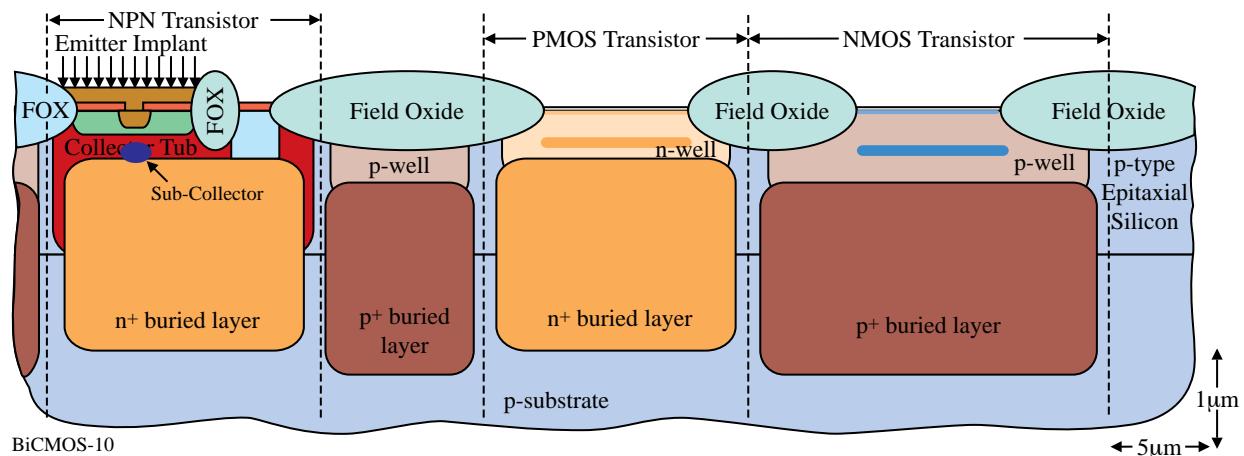
Base Definition



Definition of the Emitter Window and Sub-Collector Implant



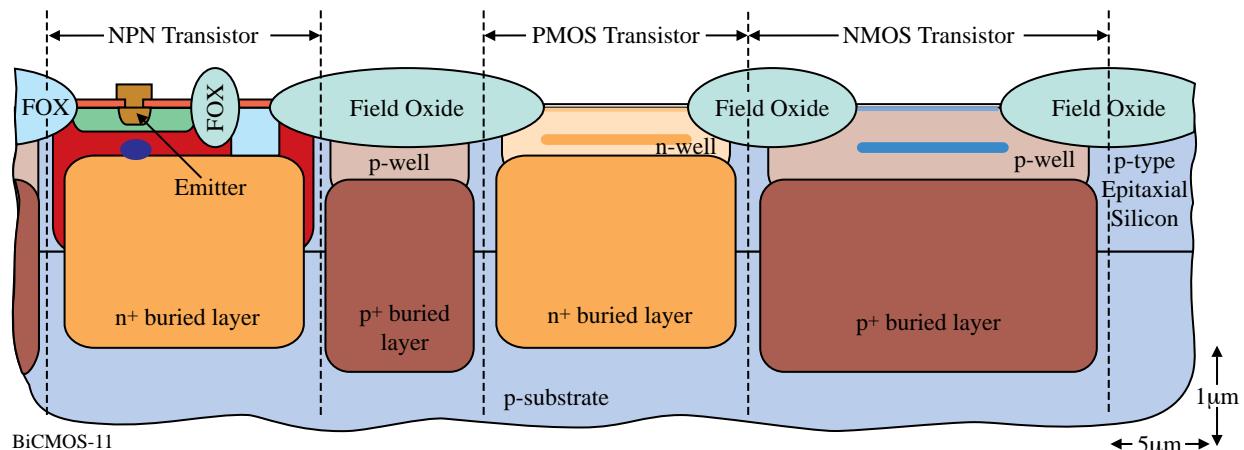
Emitter Implant



Comments:

- The polysilicon above the base is implanted with n-type carriers

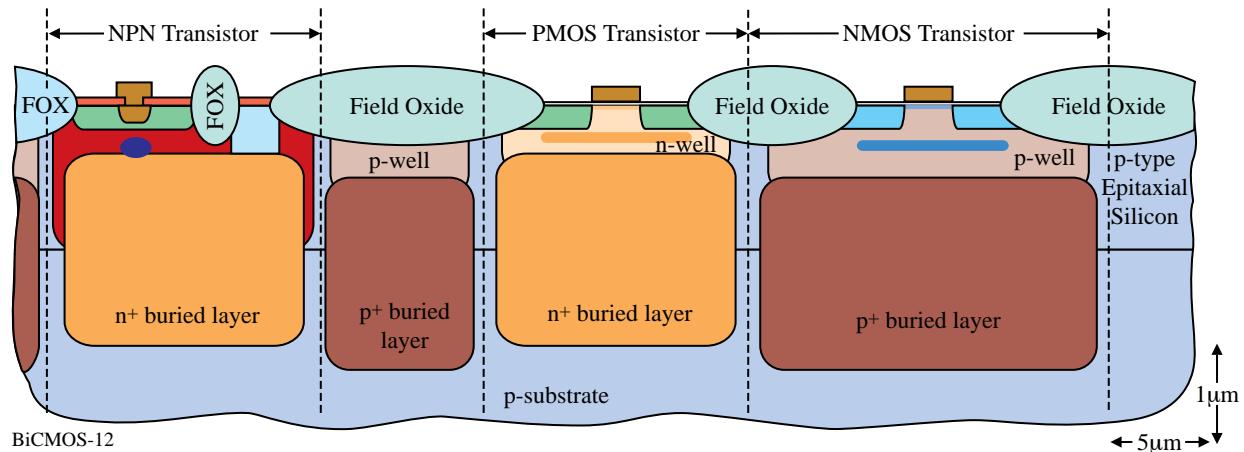
Emitter Diffusion



Comments:

- The polysilicon not over the emitter window is removed and the n-type carriers diffuse toward the base forming the emitter

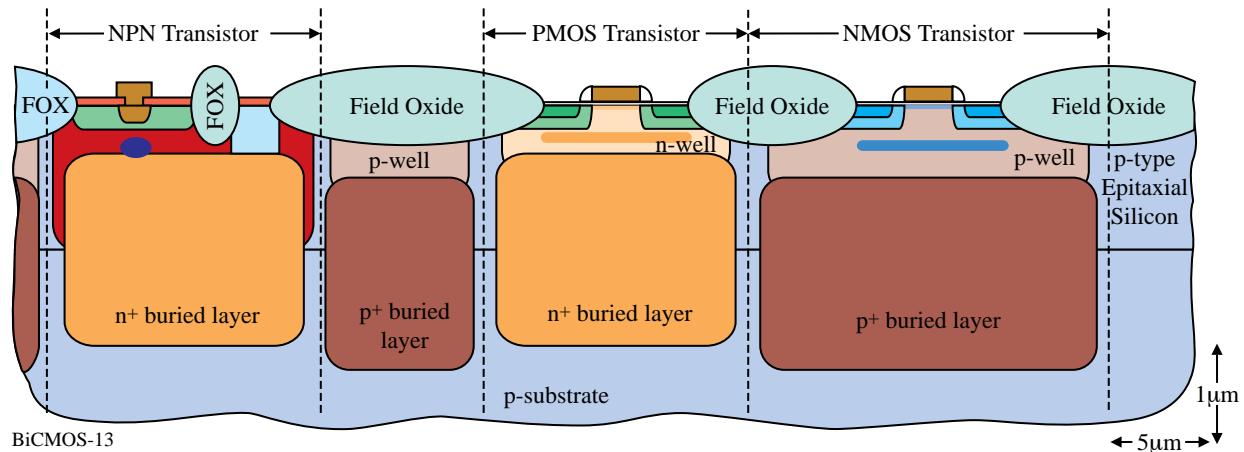
Formation of the MOS Gates and LD Drains/Sources



Comments:

- The surface of the region where the MOSFETs are to be built is cleared and a thin gate oxide is deposited with a polysilicon layer on top of the thin oxide
- The polysilicon is removed over the source and drain areas
- A light source/drain diffusion is done for the NMOS and PMOS (separately)

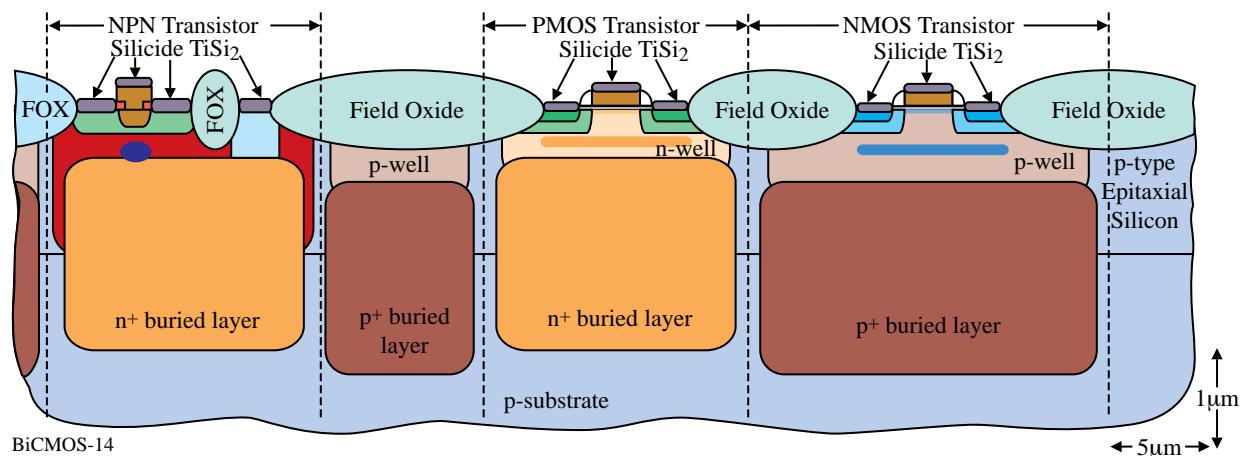
Heavily Doped Source/Drain



Comments:

- The sidewall spacers prevent the heavy source/drain doping from being near the channel of the MOSFET

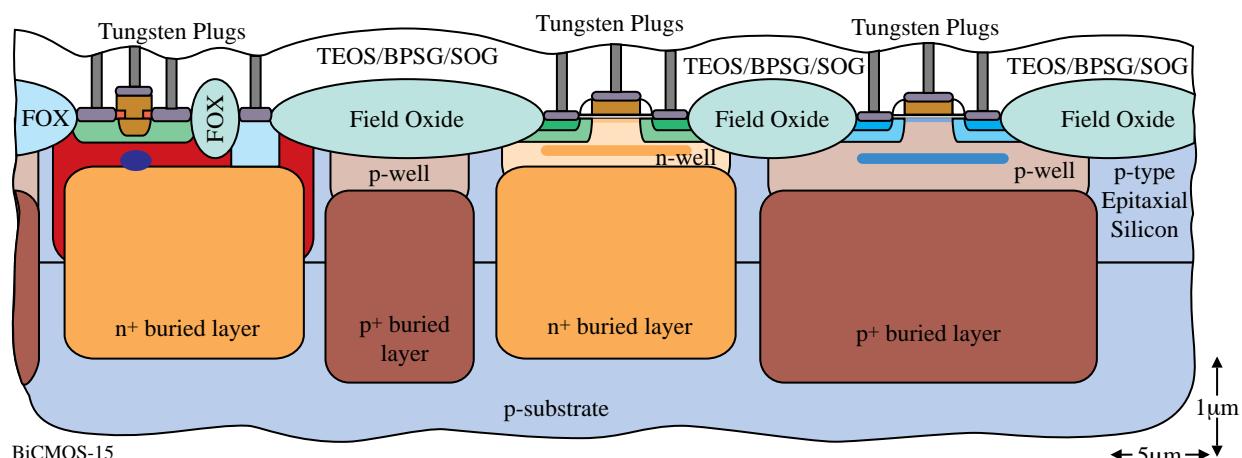
Siliciding



Comments:

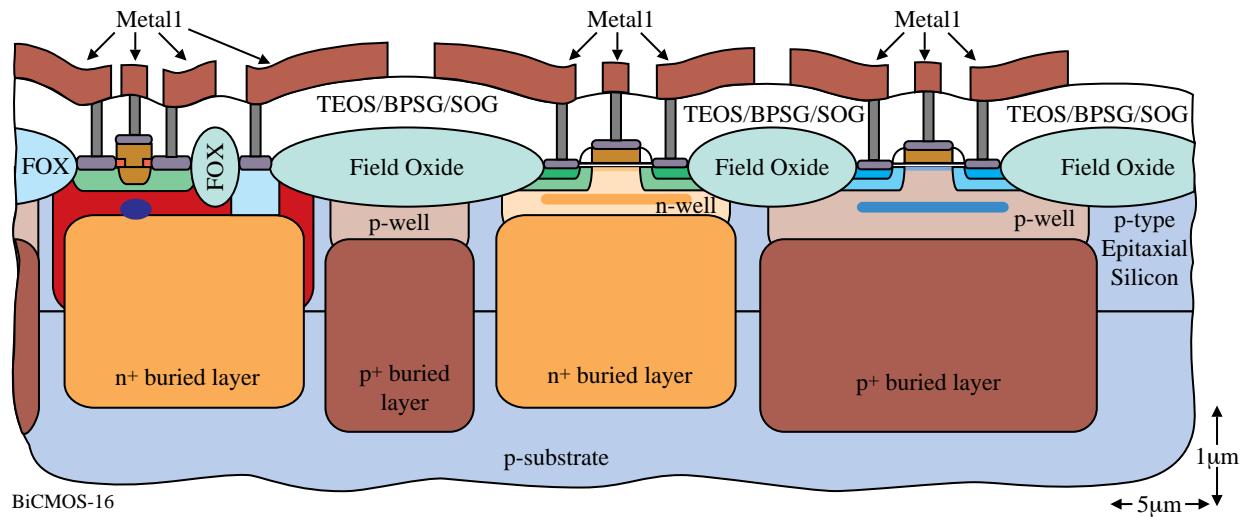
- Siliciding is used to reduce the resistance of the polysilicon and to provide ohmic contacts to the base, emitter, collector, sources and drains

Contacts

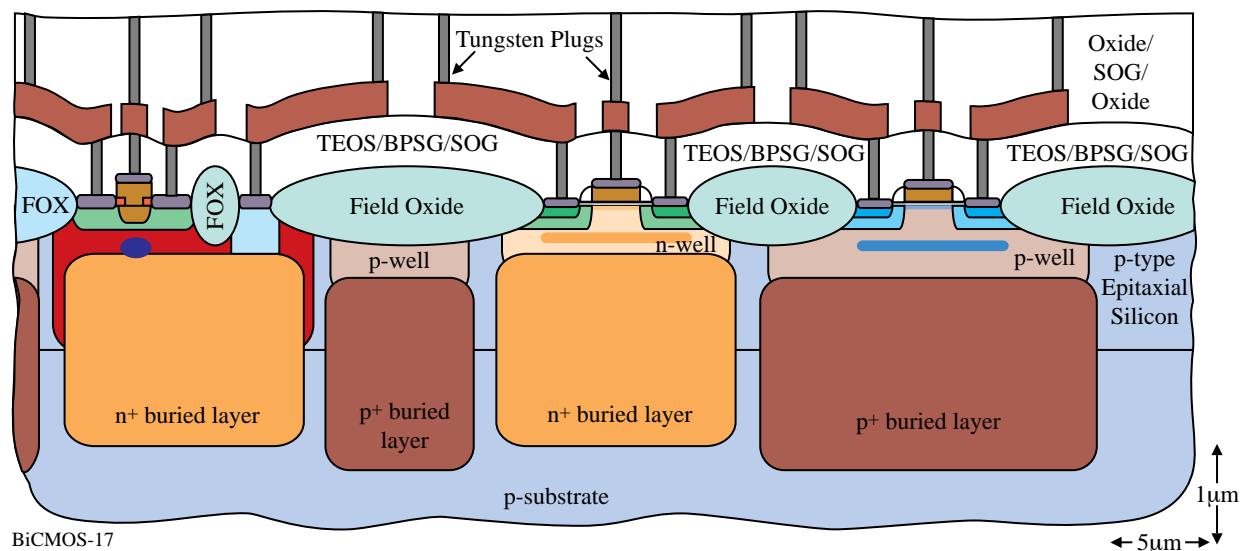


Comments:

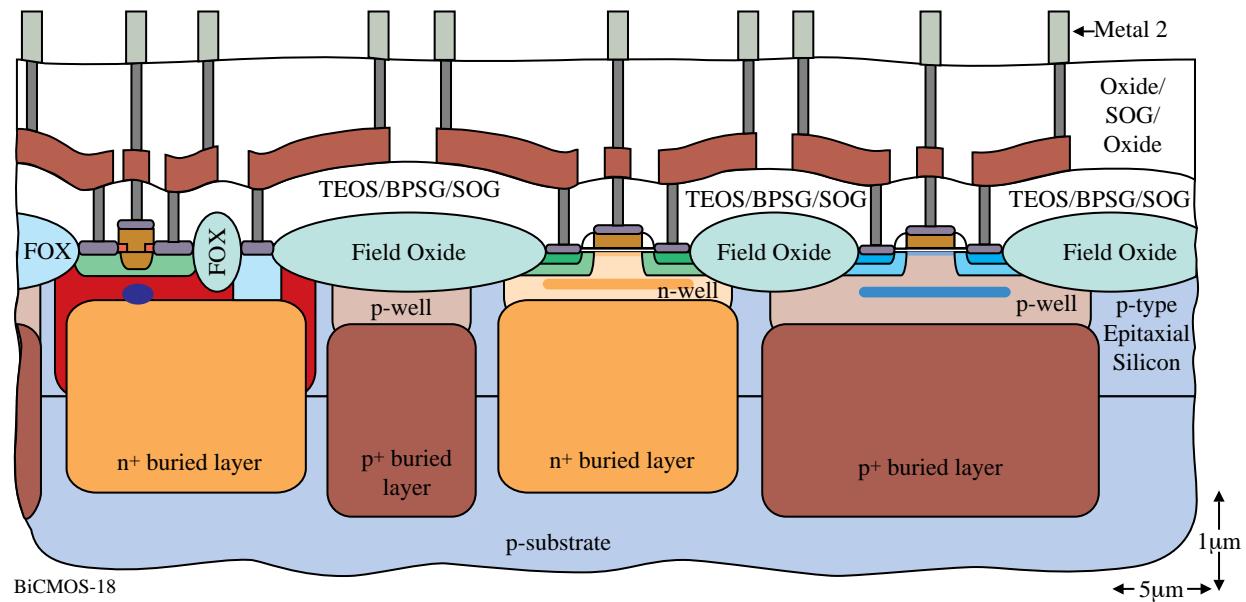
- A dielectric is deposited over the entire wafer
- One of the purposes of the dielectric is to smooth out the surface
- Tungsten plugs are used to make electrical contact between the transistors and metal1

Metal1

BiCMOS-16

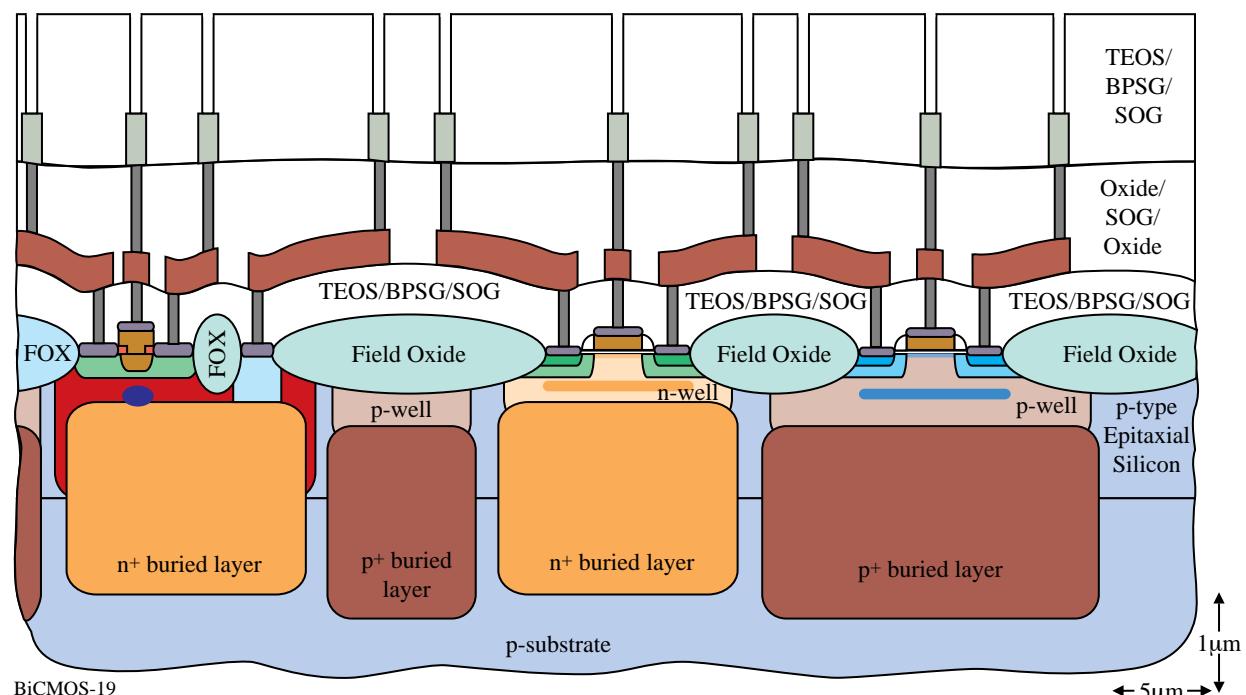
Metal1-Metal2 Vias

BiCMOS-17

Metal2

CMOS Analog Circuit Design

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Metal2-Metal3 Vias

BiCMOS-19

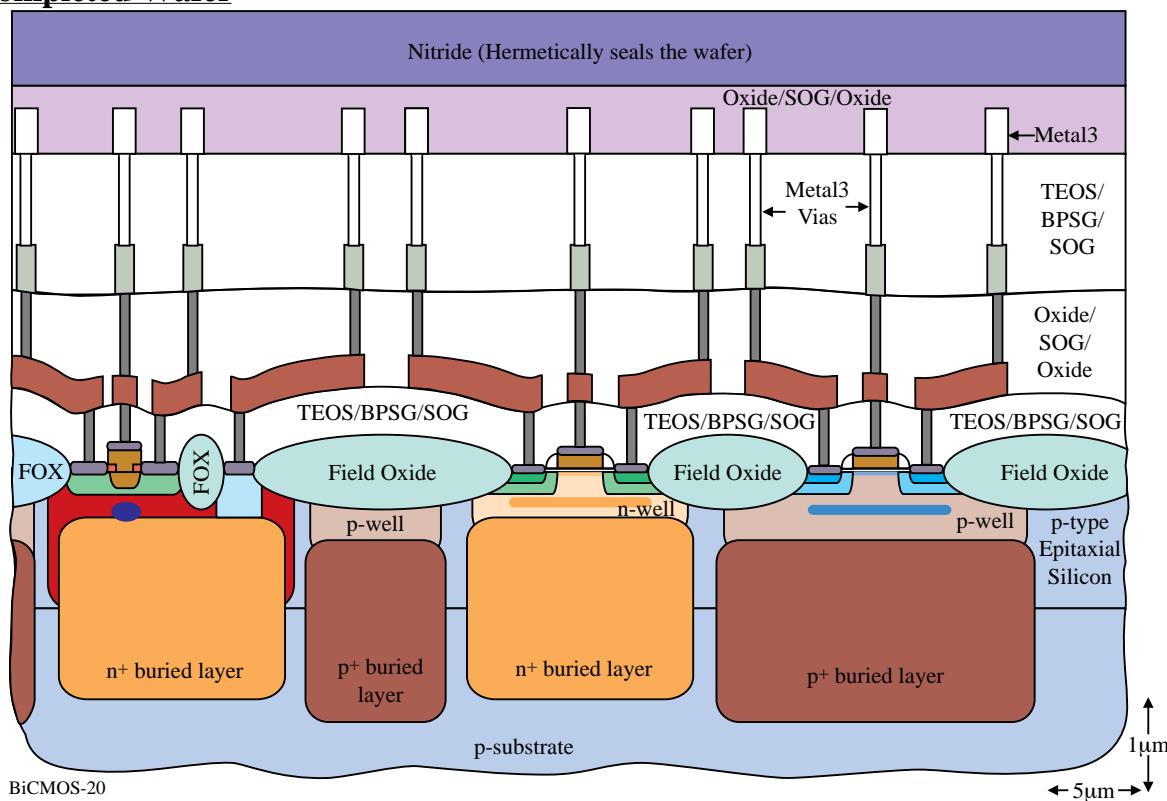
Comments:

- The metal2-metal3 vias will be filled with metal3 as opposed to tungsten plugs

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Completed Wafer



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SUMMARY

- UDSM technology typically has a minimum channel length less than $0.1\mu\text{m}$
- UDSM transistors utilize enhanced channel strains to increase drive capability and reduce off currents
- Advantages of UDSM technology include:
 - Smaller devices
 - Higher speeds and transconductances
 - Improved I_{on}/I_{off}
- Disadvantages of UDSM technology include:
 - Gate leakage currents
 - Reduced small signal gains
 - Increased nonlinearity
- BiCMOS technology
 - Offers both CMOS transistors and a high performance vertical BJT
 - CMOS is typically a generation behind
 - Silicon germanium can be used to enhance the BJT performance

LECTURE 050 - PN JUNCTIONS AND CMOS TRANSISTORS

LECTURE ORGANIZATION

Outline

- *pn* junctions
- MOS transistors
- Layout of MOS transistors
- Parasitic bipolar transistors in CMOS technology
- High voltage CMOS transistors
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 29-43

PN JUNCTIONS

How are PN Junctions used in CMOS?

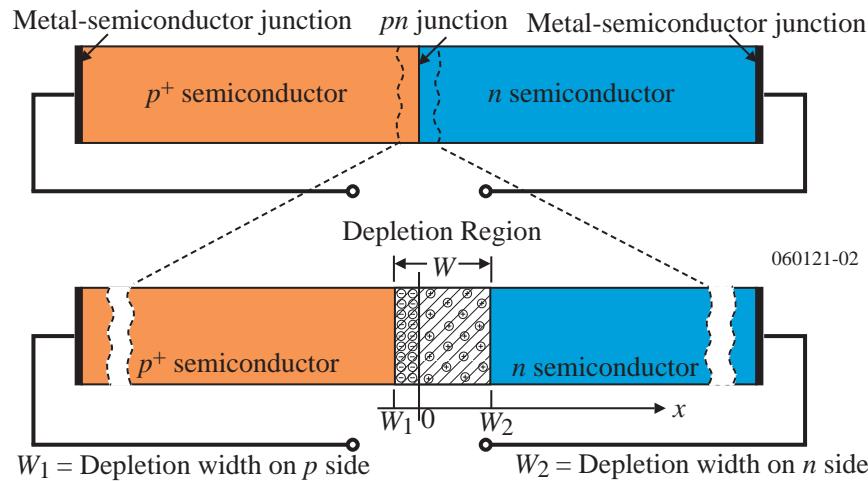
- *PN* junctions are used to electrically isolate one semiconductor region from another
- *PN* diodes
- ESD protection
- Creation of the thermal voltage for bandgap purposes
- Depletion capacitors – voltage variable capacitors (varactors)

Components of a *pn* junction:

1.) *p*-doped semiconductor – a semiconductor having atoms containing a lack of electrons (acceptors). The concentration of acceptors is N_A in atoms per cubic centimeter.

2.) *n*-doped semiconductor – a semiconductor having atoms containing an excess of electrons (donors). The concentration of these atoms is N_D in atoms per cubic centimeter.

Abrupt PN Junction



1. Doped atoms near the metallurgical junction lose their free carriers by diffusion.
2. As these fixed atoms lose their free carriers, they build up an electric field, which opposes the diffusion mechanism.
3. Equilibrium conditions are reached when:

$$\text{Current due to diffusion} = \text{Current due to electric field}$$

Influence of Doping Level on the Depletion Regions

Intuitively, one can see that the depletion regions are inversely proportional to the doping level. To achieve equilibrium, equal and opposite fixed charge on both sides of the junction are required. Therefore, the larger the doping the smaller the depletion region on that side of the junction.

The equations that result are:

$$W_1 = \sqrt{\frac{2\epsilon(\psi_o - v_D)}{qN_A\left(1 + \frac{N_A}{N_D}\right)}} \propto \sqrt{\frac{1}{N_A}}$$

and

$$W_2 = \sqrt{\frac{2\epsilon(\psi_o - v_D)}{qN_D\left(1 + \frac{N_D}{N_A}\right)}} \propto \sqrt{\frac{1}{N_D}}$$

Assume that $v_D = 0$, $\psi_o = 0.637V$ and $N_D = 10^{17}$ atoms/cm³. Find the p-side depletion region width if $N_A = 10^{15}$ atoms/cm³ and if $N_A = 10^{19}$ atoms/cm³:

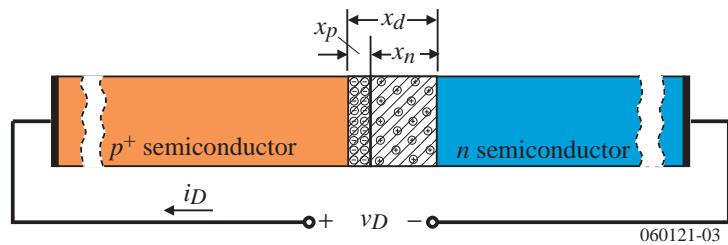
For $N_A = 10^{15}$ atoms/cm³ the p-side depletion width is $0.90 \mu\text{m}$.

For $N_A = 10^{19}$ atoms/cm³ the p-side depletion width is 0.9 nm .

Graphical Characterization of the Abrupt PN Junction

Assume the pn junction is open-circuited.

Cross-section of an ideal pn junction:



Symbol for the *pn* junction:

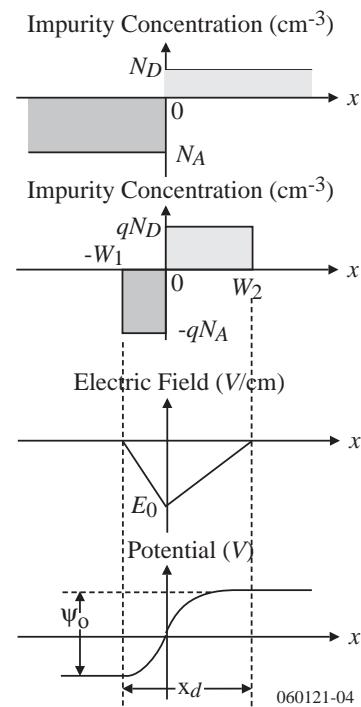
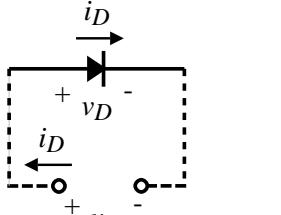
Built-in potential, ψ_0 :

$$\psi_0 = V_t \ln\left(\frac{N_A N_D}{n_i^2}\right),$$

where

$$V_t = \frac{kT}{q}$$

n_i is the intrinsic concentration of silicon.



Reverse-Biased PN Junctions

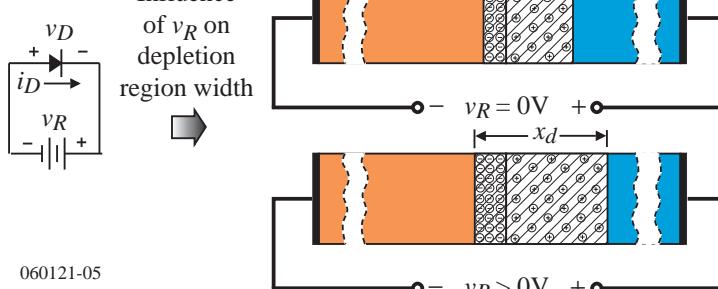
Depletion region:

$$x_d = x_p + x_n = W_1 + W_2$$

$$x_p = W_1 \propto \sqrt{v_R}$$

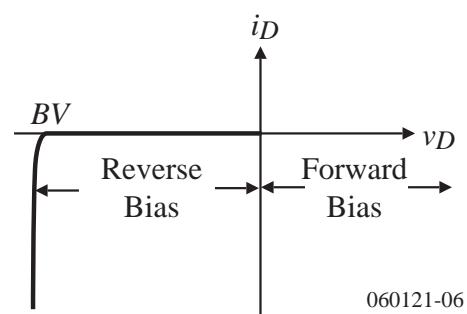
and

$$x_n = W_2 \propto \sqrt{v_R}$$



Breakdown voltage (BV):

If $v_R > BV$, avalanche multiplication will occur resulting in a high conduction state as illustrated.



Breakdown Voltage as a Function of Doping

It can be shown that[†]:

$$BV \approx \frac{\epsilon_{si}(N_A + N_D)}{2qNAN_D} E_{max}^2$$

where $E_{max} = 3 \times 10^5$ V/cm for silicon.

An example:

Assume that $N_D = 10^{17}$ atoms/cm³.

Find BV if $N_A = 10^{15}$ atoms/cm³ and if $N_A = 10^{19}$ atoms/cm³:

$N_A = 10^{15}$ atoms/cm³:

$$\text{If } N_A \ll N_D, \text{ then } BV \approx \frac{\epsilon_{si}}{2qN_A} E_{max}^2 = \frac{1.04 \times 10^{-12} \cdot 9 \times 10^{10}}{2 \cdot 1.6 \times 10^{-19} \cdot 10^{15}} = 291 \text{ V}$$

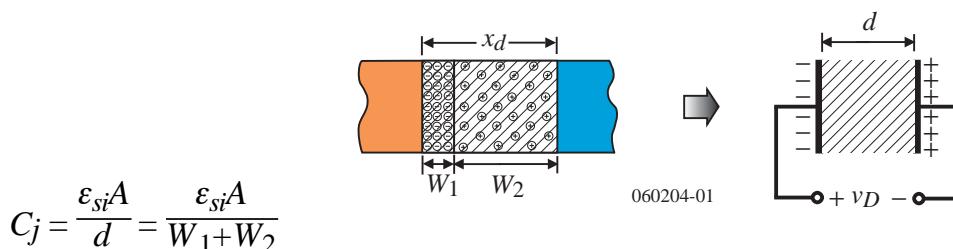
$N_A = 10^{19}$ atoms/cm³:

$$\text{If } N_A \gg N_D, \text{ then } BV \approx \frac{\epsilon_{si}}{2qN_D} E_{max}^2 = \frac{1.04 \times 10^{-12} \cdot 9 \times 10^{10}}{2 \cdot 1.6 \times 10^{-19} \cdot 10^{17}} = 2.91 \text{ V}$$

[†] P. Allen and D. Holberg, *CMOS Analog Circuit Design*, 2nd ed., Oxford University Press, 2002
CMOS Analog Circuit Design

Depletion Capacitance

Physical viewpoint of the depletion capacitance:

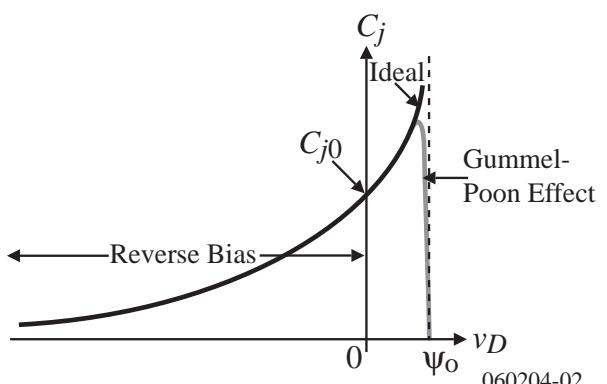


$$C_j = \frac{\epsilon_{si}A}{d} = \frac{\epsilon_{si}A}{W_1 + W_2}$$

$$= \frac{\epsilon_{si}A}{\sqrt{\frac{2\epsilon_{si}(\psi_o - vD)}{q(N_D + N_A)}} \left[\sqrt{\frac{N_D}{N_A}} + \sqrt{\frac{N_A}{N_D}} \right]}$$

$$= A \sqrt{\frac{\epsilon_{si} q N_A N_D}{2(N_A + N_D)}} \frac{1}{\sqrt{\psi_o - vD}}$$

$$= \frac{C_{j0}}{\sqrt{1 - \frac{vD}{\psi_o}}}$$

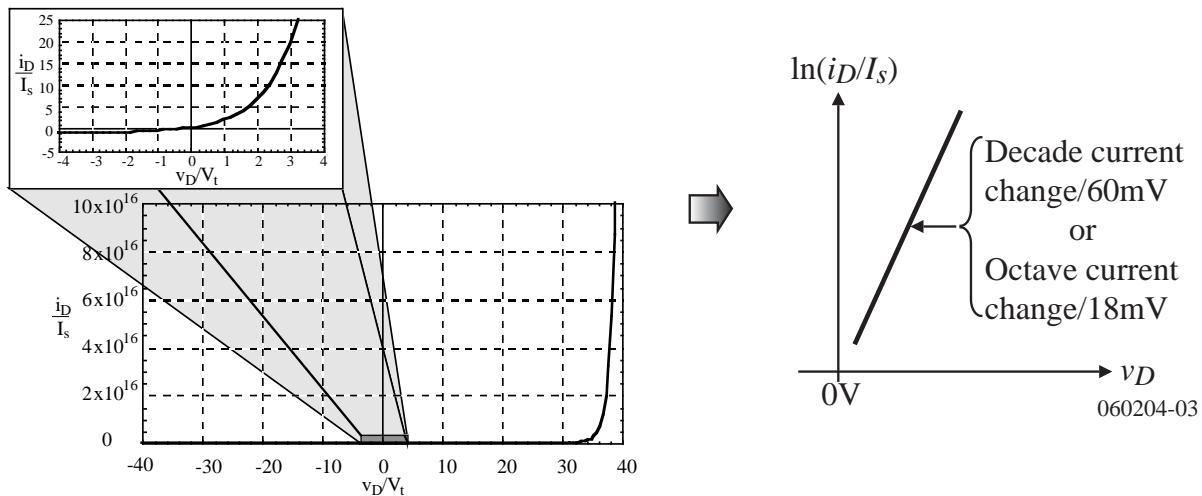


Forward-Biased PN Junctions

When the *pn* junction is forward-biased, the potential barrier is reduced and significant current begins to flow across the junction. This current is given by:

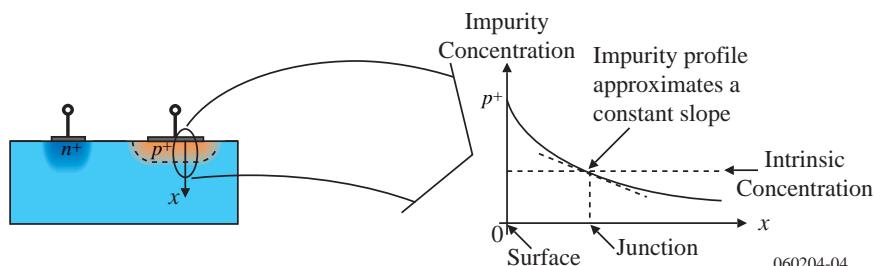
$$i_D = I_s \left[\exp\left(\frac{v_D}{V_t}\right) - 1 \right] \quad \text{where } I_s = qA \left[\frac{D_{ppno}}{L_p} + \frac{D_{nnpo}}{L_n} \right] \approx \frac{qAD}{L} \frac{n_i^2}{N} = KT^3 \exp\left(-\frac{V_{GO}}{V_t}\right)$$

Graphically, the i_D versus v_D characteristics are given as:



Graded PN Junctions

In practice, the *pn* junction is graded rather than abrupt.



The previous expressions become:

Depletion region widths-

$$\left. \begin{aligned} W_1 &= \left(\frac{2\epsilon_{si}(\psi_o - v_D)ND}{qNA(N_A + N_D)} \right)^m \\ W_2 &= \left(\frac{2\epsilon_{si}(\psi_o - v_D)N_A}{qND(N_A + N_D)} \right)^m \end{aligned} \right\} \quad W \propto \left(\frac{1}{N} \right)^m$$

Depletion capacitance-

$$\begin{aligned} C_j &= A \left(\frac{\epsilon_{si}qNAND}{2(N_A + N_D)} \right)^m \frac{1}{(\psi_o - v_D)^m} \\ &= \frac{C_{j0}}{\left(1 - \frac{v_D}{\psi_o} \right)^m} \end{aligned}$$

where $0.33 \leq m \leq 0.5$.

Metal-Semiconductor Junctions

Ohmic Junctions: A pn junction formed by a highly doped semiconductor and metal.

Energy band diagram

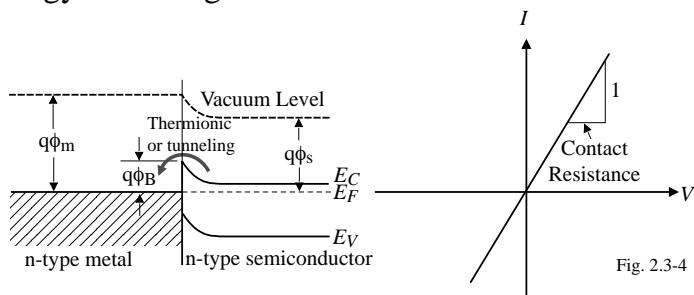


Fig. 2.3-4

Schottky Junctions: A pn junction formed by a lightly doped semiconductor and metal.

Energy band diagram

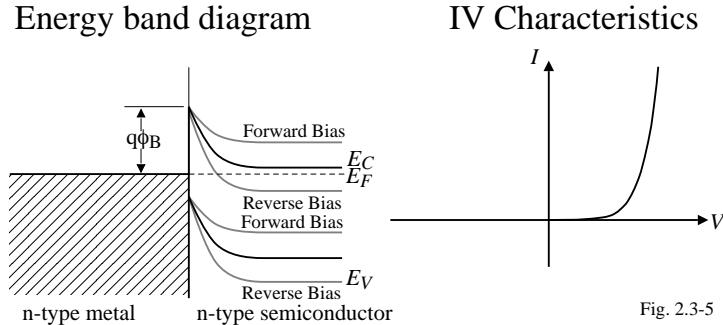
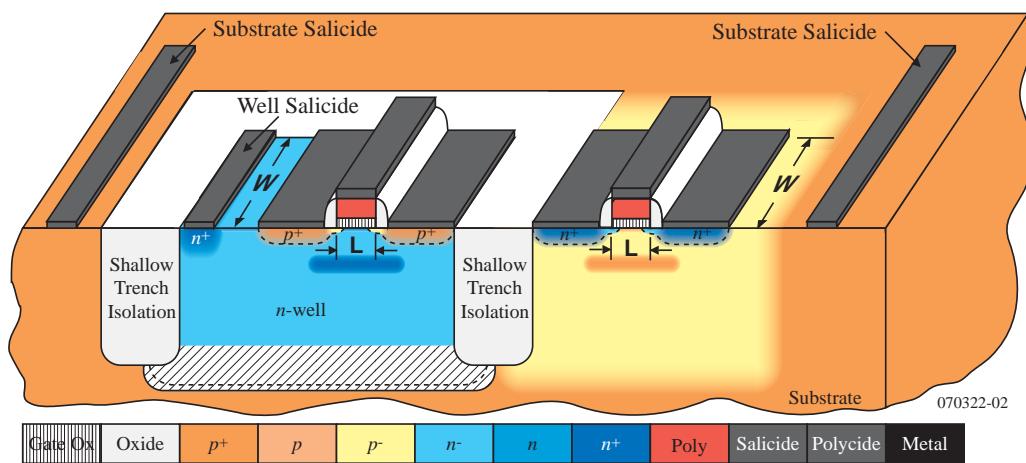


Fig. 2.3-5

MOS TRANSISTOR PHYSICAL ASPECTS OF MOS TRANSISTORS

Physical Structure of MOS Transistors in an n -well Technology



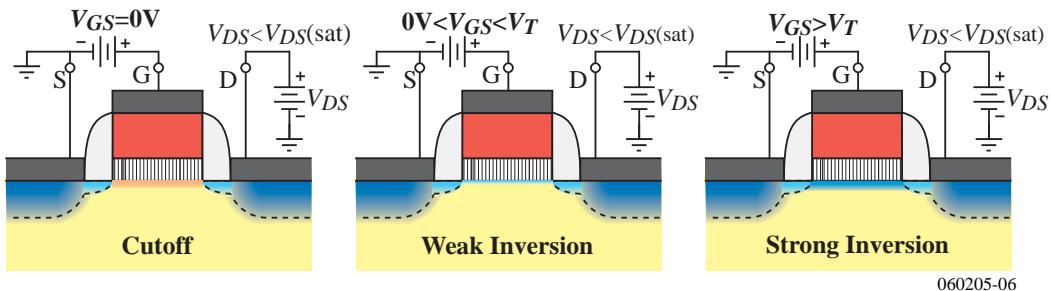
Width (W) of the MOSFET = Width of the source/drain diffusion

Length (L) of the MOSFET = Width of the polysilicon gate between the S/D diffusions

Note that the MOSFET is isolated from the well/substrate by reverse biasing the resulting pn junction

Enhancement MOSFETs

The channel of an enhancement MOSFET is formed when the proper potential is applied to the gate of the MOSFET. This potential inverts the material immediately below the gate to the same type of impurity as the source and drain forming the channel.



$$\begin{aligned} V_T = & \text{Gate-bulk work function } (\phi_{MS}) + \text{voltage to change the surface potential } (-2\phi_F) \\ & + \text{voltage to offset the channel-bulk depletion charge } (-Q_b/C_{ox}) \\ & + \text{voltage to compensate the undesired interface charge } (-Q_{ss}/C_{ox}) \end{aligned}$$

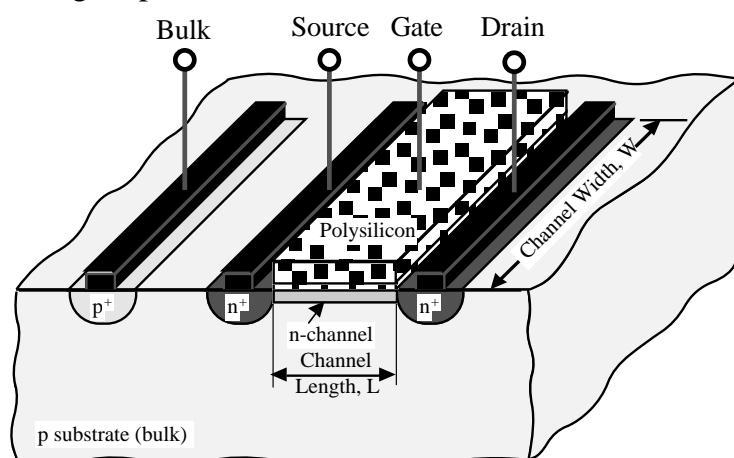
$$V_T = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_b - Q_{b0}}{C_{ox}} = V_{T0} + \gamma (\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|})$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}}, \quad \gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}} \quad \text{and} \quad Q_b \approx \sqrt{2qN_A\varepsilon_{si}(|-2\phi_F + v_{SB}|)}$$

Depletion Mode MOSFET

The channel is diffused into the substrate so that a channel exists between the source and drain with no external gate potential.



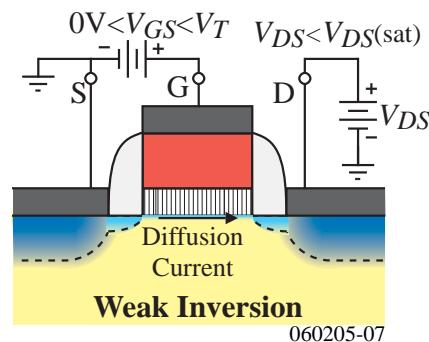
The threshold voltage for a depletion mode NMOS transistor will be negative (a negative gate potential is necessary to attract enough holes underneath the gate to cause this region to invert to p-type material).

Weak Inversion Operation

Weak inversion operation occurs when the applied gate voltage is below V_T and occurs when the surface of the substrate beneath the gate is weakly inverted.

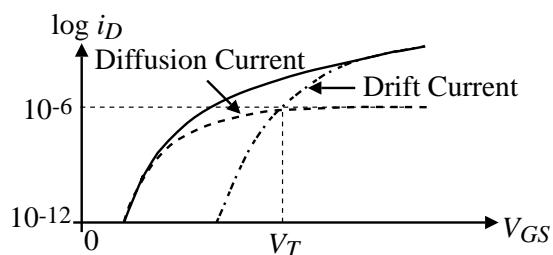
Regions of operation according to the surface potential, ϕ_s .

- $\phi_s < \phi_F$: Substrate not inverted
- $\phi_F < \phi_s < 2\phi_F$: Channel is weakly inverted
(diffusion current)
- $2\phi_F < \phi_s$: Strong inversion (drift current)



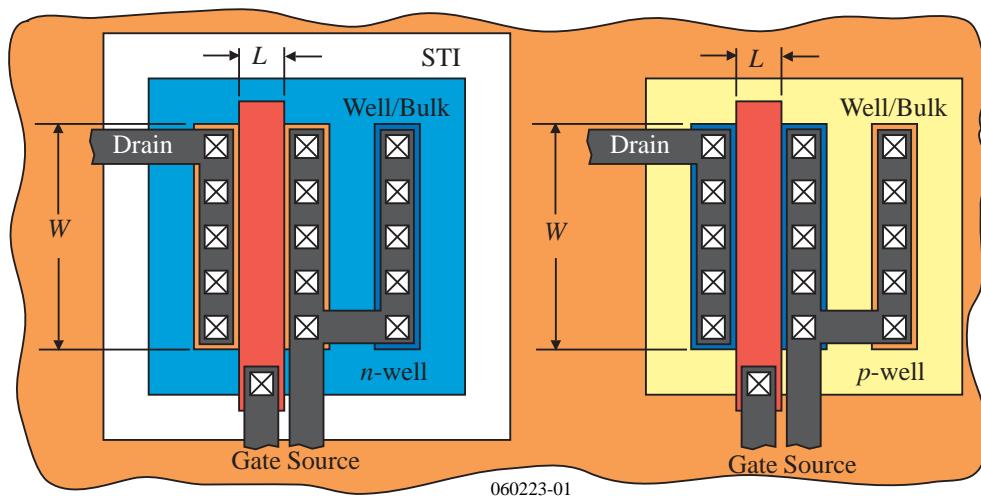
060205-07

Drift current versus diffusion current in a MOSFET:



LAYOUT OF MOS TRANSISTORS

Layout of a Single MOS transistor:



060223-01

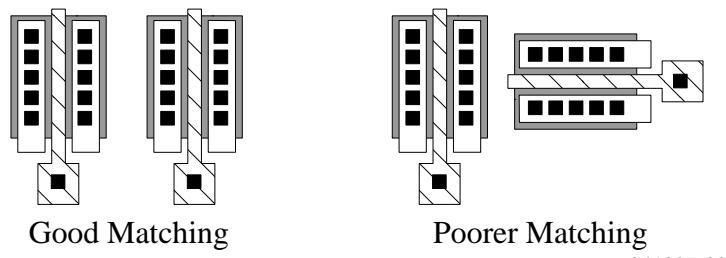
Comments:

- Make sure to contact the source and drain with multiple contacts to evenly distribute the current flow under the gate.
- Minimize the area of the source and drain to reduce bulk-source/drain capacitance.

Geometric Effects

Orientation:

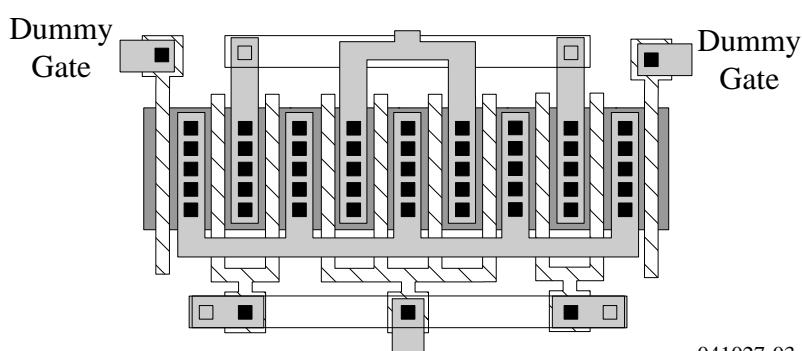
Devices oriented in the same direction match more precisely than those oriented in other directions.



041027-02

Diffusion and Etch Effects

- Poly etch rate variation – use dummy elements to prevent etch rate differences.



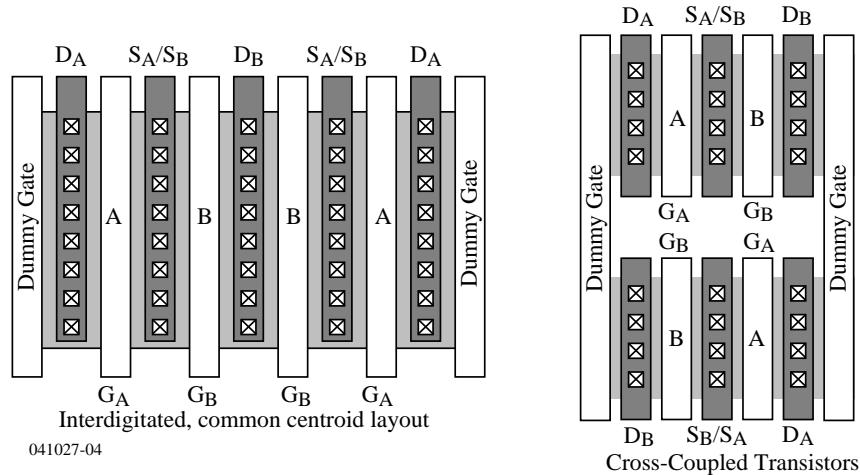
041027-03

- Do not put contacts on top of the gate for matched transistors.
- Be careful of diffusion interactions for diffusions near the channel of the MOSFET

Thermal and Stress Effects

- Oxide gradients – use common centroid geometry layout
- Stress gradients – use proper location and common centroid geometry layout
- Thermal gradients – keep transistors well away from power devices and use common centroid geometry layout with interdigitated transistors

Examples of Common Centroid Interdigitated transistor layout:

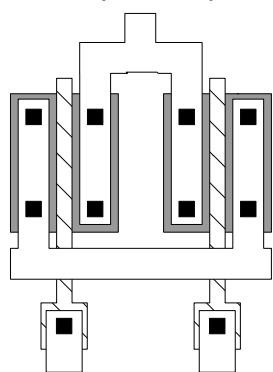


MOS Transistor Layout

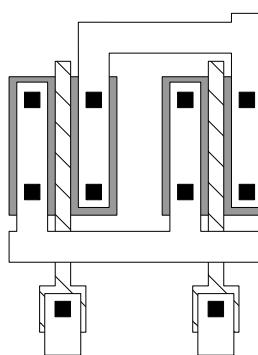
Photolithographic invariance (PLI) are transistors that exhibit identical orientation. PLI comes from optical interactions between the UV light and the masks.

Examples of the layout of matched MOS transistors:

- 1.) Examples of mirror symmetry and photolithographic invariance.



Mirror Symmetry



Photolithographic Invariance
Fig. 2.6-05

MOS Transistor Layout - Continued

- 2.) Two transistors sharing a common source and laid out to achieve both photolithographic invariance and common centroid.

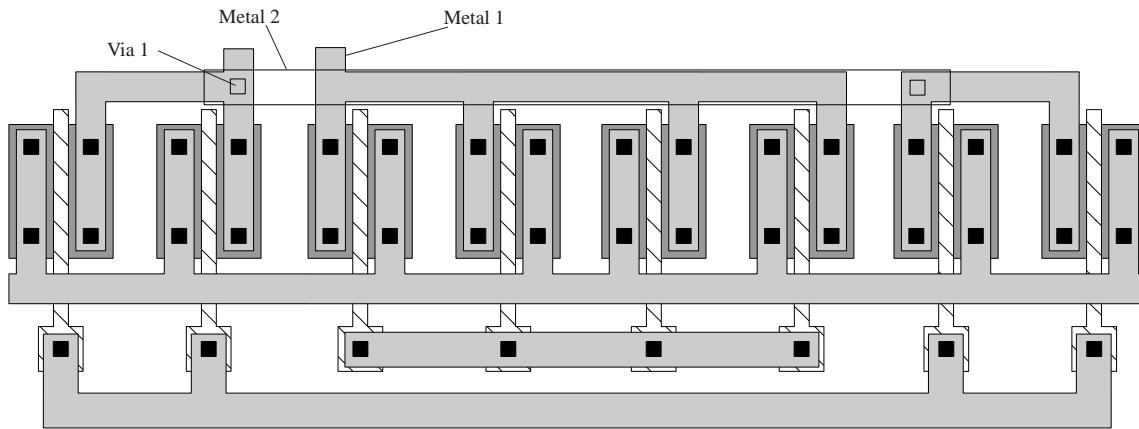


Fig. 2.6-06

MOS Transistor Layout - Continued

- 3.) Compact layout of the previous example.

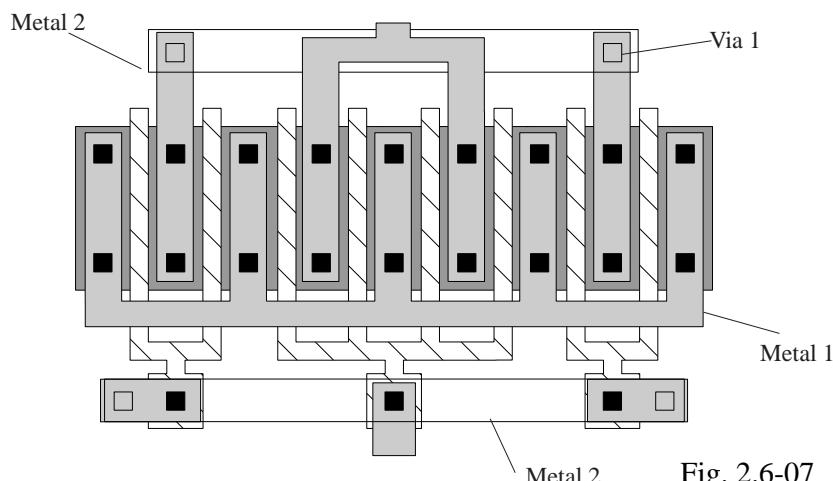


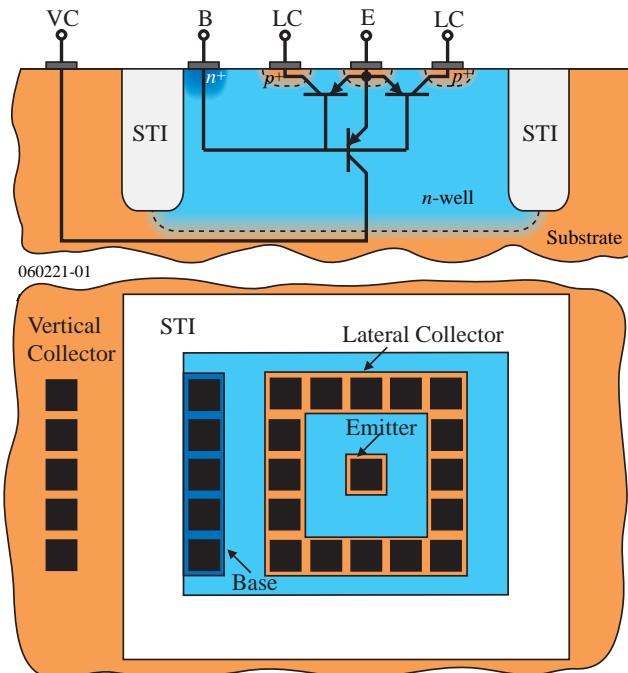
Fig. 2.6-07

PARASITIC BIPOLAR TRANSISTORS IN CMOS TECHNOLOGY

A Lateral Bipolar Transistor

n-well CMOS technology:

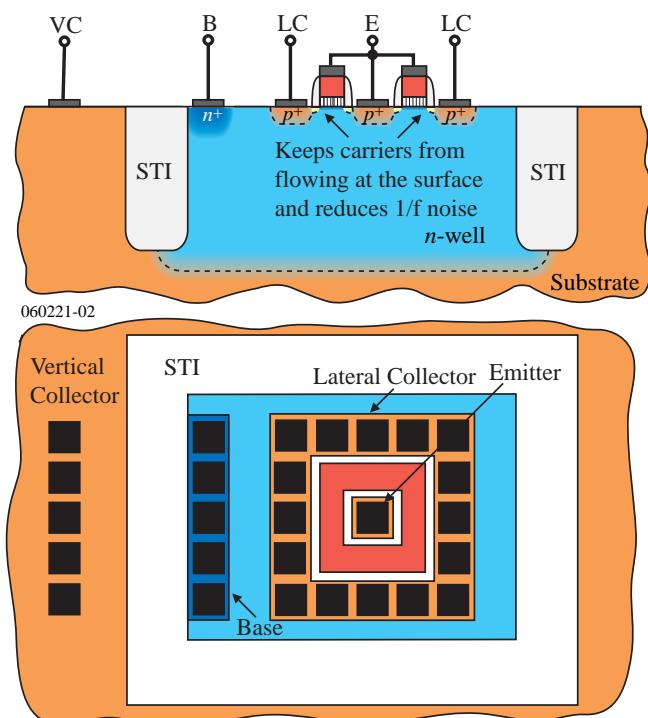
- It is desirable to have the lateral collector current much larger than the vertical collector current.
- Lateral BJT generally has good matching.
- The lateral BJT can be used as a photodetector with reasonably good efficiency.
- Triple well technology allows the current of the vertical collector to avoid the substrate.



A Field-Aided Lateral BJT

Use minimum channel length to enhance beta:

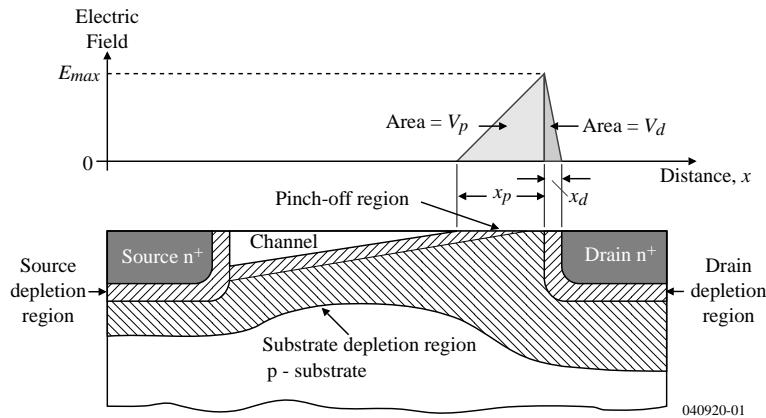
$\beta_F \approx 50$ to 100 depending on the process



HIGH VOLTAGE CMOS TRANSISTORS

Extended Voltage MOSFETs

The electric field from the source to drain in the channel is shown below.



The voltage drop from drain to source is,

$$V_{DS} = V_p + V_d = 0.5(E_{max}x_p + E_{max}x_d) = 0.5E_{max}(x_p + x_d)$$

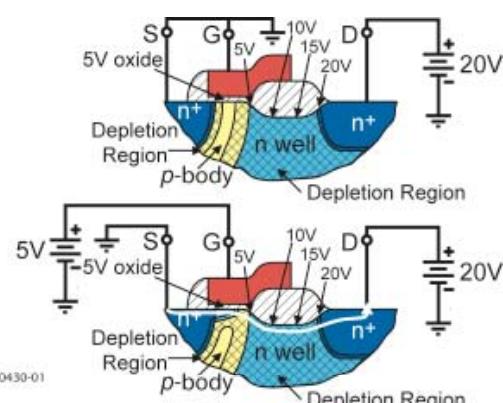
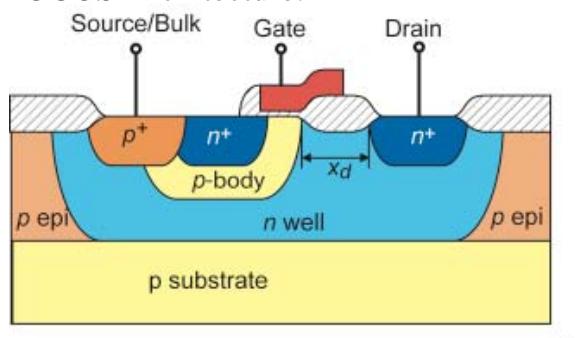
E_{max} and x_p are limited by hot carrier generation and channel length modulation requirements whereas these limitations do not exist for x_d .

Therefore, to get extended voltage transistors, make x_d larger.

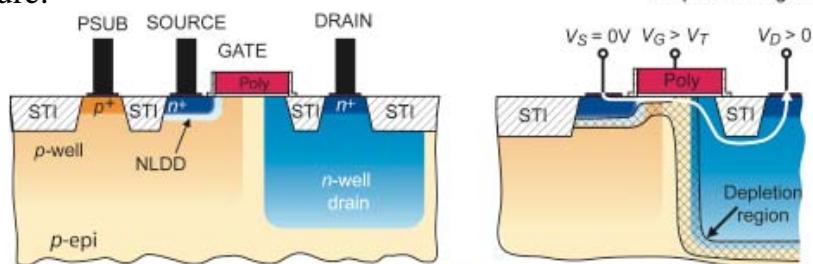
High Voltage Architectures

The objective is to create a lightly doped, extended drain region where the high voltage of the drain can drop down to a level that will not cause the gate oxide to breakdown.

LOCOS Architecture:



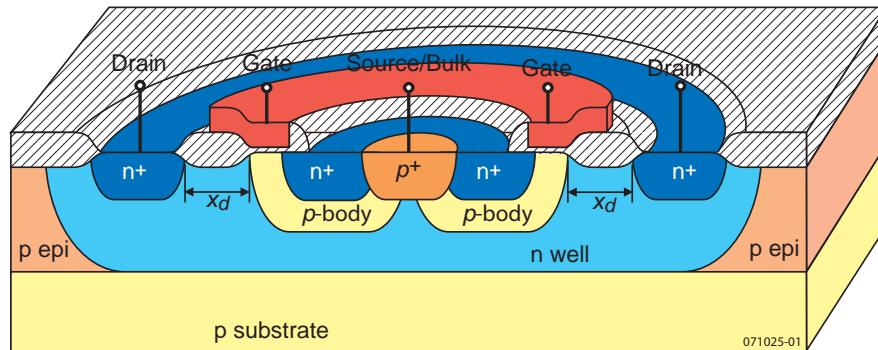
DSM Architecture:



Lateral DMOS (LDMOS) Using LOCOS CMOS Technology

The LDMOS structure is designed to provide sufficient lateral dimension and to prevent oxide breakdown by the higher drain voltages.

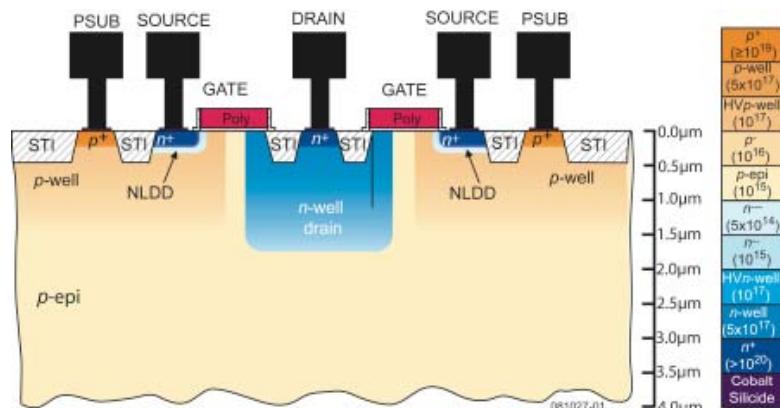
One possible implementation using LOCOS technology:



- Structure is symmetrical about the source/bulk contact
- Channel is formed in the p region under the gates
- The lightly doped n region between the drain side of the channel and the n⁺ drain contact (x_d) increases the depletion region width on the drain side of the channel/drain pn junction resulting in larger values of v_{DS} .
- Drain voltage can be 20-30V

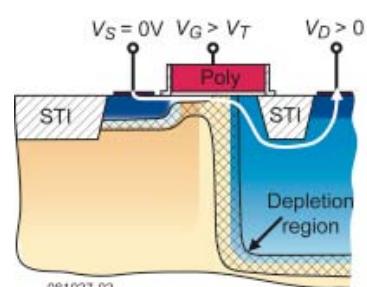
Lateral DMOS (LDMOS) Using DSM CMOS Technology

Cross-section of an NLDMOS using DSM technology:



Differences between an NLDMOS and NMOS:

- Asymmetry
- Non-uniform channel
- Current flow (not all at the surface)
- No self-alignment (larger drain-gate overlap capacitance)
- Note the extended drift region on the drain side of the channel



SUMMARY

- *pn* junction usage in CMOS include:
 - Electrical isolation, *pn* diodes, ESD protection, depletion capacitors
- Depletion region widths are inversely proportional to the doping
- Depletion region widths are proportional to the reverse bias voltage
- Ohmic metal-semiconductor junctions require a highly doped semiconductor
- MOSFETs can be:
 - Enhancement – the applied gate voltage forms the channel
 - Depletion – the channel is physically constructed in fabrication
- The threshold voltage of MOSFETs consists of the following components:
 - Gate bulk work function (ϕ_{MS})
 - Voltage to change the surface potential ($-2\phi_F$)
 - Voltage to offset the channel-bulk depletion charge ($-Q_b/C_{ox}$)
 - Voltage to compensate the undesired interface charge ($-Q_{ss}/C_{ox}$)
- Weak inversion is MOSFET operation with the gate-source voltage less than the threshold voltage
- Layout of the MOSFET is important to its performance and matching capabilities
- Extended drain regions lead to higher voltage capability MOSFETs

LECTURE 060 - CAPACITORS

LECTURE ORGANIZATION

Outline

- Introduction
- pN junction capacitors
- MOSFET gate capacitors
- Conductor-insulator-conductor capacitors
- Deviation from ideal behavior in capacitors
- Summary

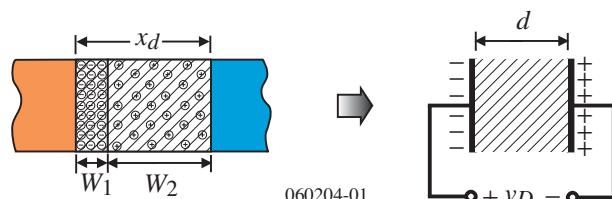
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 43-47, 58-59 and 63-64

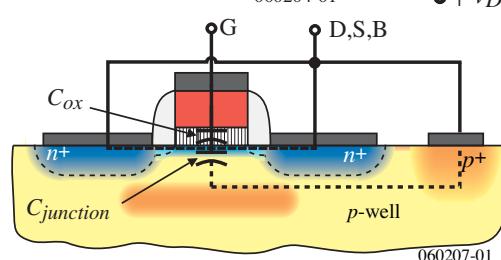
INTRODUCTION

Types of Capacitors for CMOS Technology

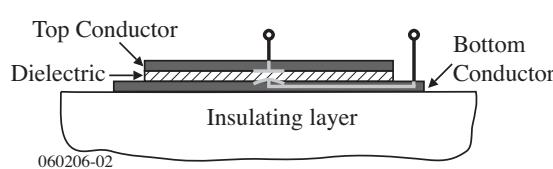
- 1.) PN junction (depletion) capacitors



- 2.) MOSFET gate capacitors



- 3.) Conductor-insulator-conductor capacitors



Characterization of Capacitors

What characterizes a capacitor?

- 1.) Dissipation (quality factor) of a capacitor is

$$Q = \omega C R_p = \frac{\omega C}{R_s}$$

where R_p is the equivalent resistance in parallel with the capacitor, C , and R_s is the electrical series resistance (ESR) of the capacitor, C .

- 2.) Parasitic capacitors to ground from each node of the capacitor.
- 3.) The density of the capacitor in Farads/area.
- 4.) The absolute and relative accuracies of the capacitor.
- 5.) The C_{max}/C_{min} ratio which is the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor (*varactor*).
- 6.) The variation of a variable capacitance with the control voltage.
- 7.) Linearity, $q = Cv$.

PN JUNCTION CAPACITORS

PN Junction Capacitors in a Well

Generally made by diffusion into the well.

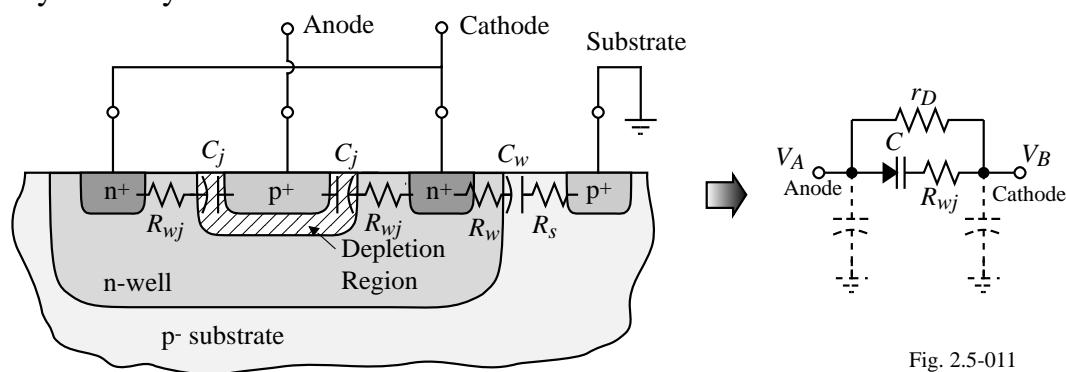


Fig. 2.5-011

Layout:

Minimize the distance between the p^+ and n^+ diffusions.

Two different versions have been tested.

- 1.) Large islands – $9\mu m$ on a side
- 2.) Small islands – $1.2\mu m$ on a side

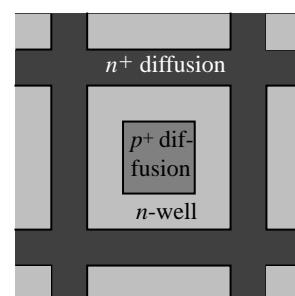
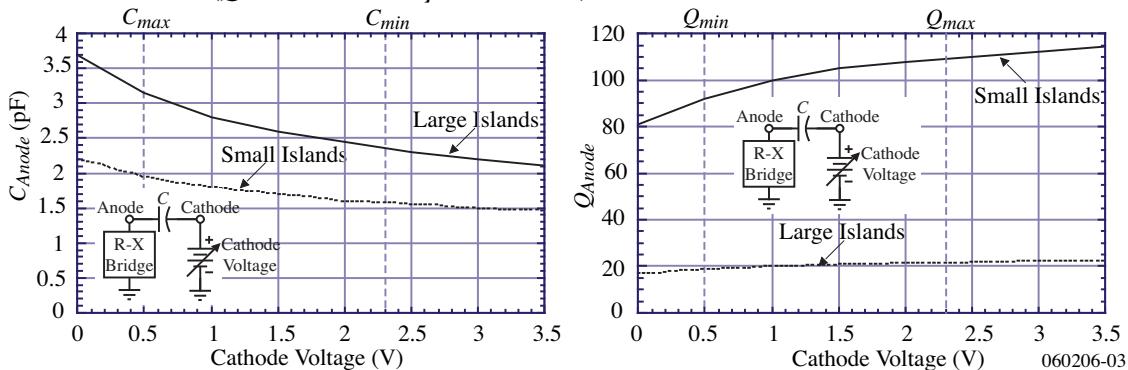


Fig. 2.5-1A

PN-Junction Capacitors – Continued

The anode should be the floating node and the cathode must be connected to ac ground. Experimental data (Q at 2GHz, 0.5 μ m CMOS)[†]:



Terminal Under Test	Small Islands (598 1.2 μ m x 1.2 μ m)			Large Islands (42 9 μ m x 9 μ m)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

Electrons as majority carriers lead to higher Q because of their higher mobility.

The resistance, R_{wj} , is reduced in small islands compared with large islands \Rightarrow higher Q

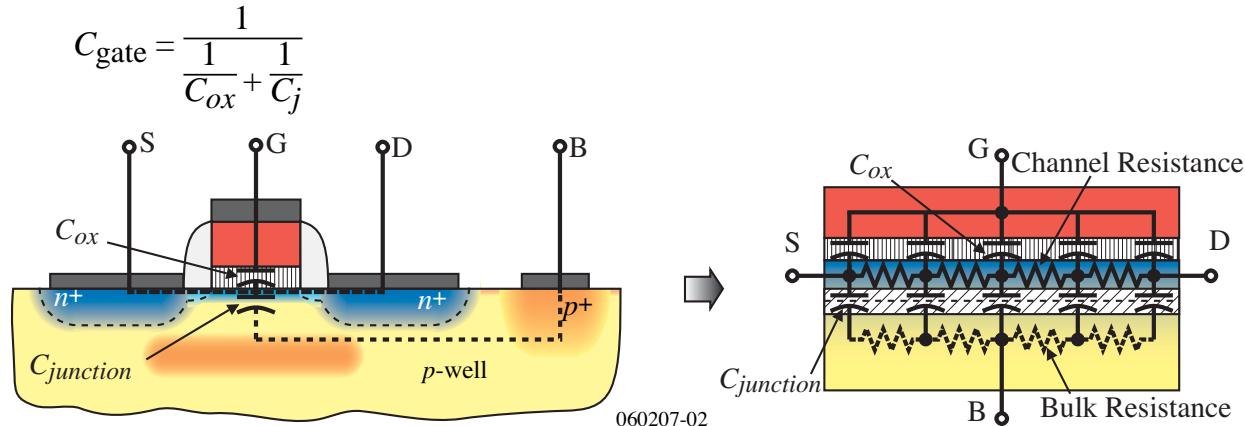
[†]E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001.
CMOS Analog Circuit Design
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MOSFET GATE CAPACITORS

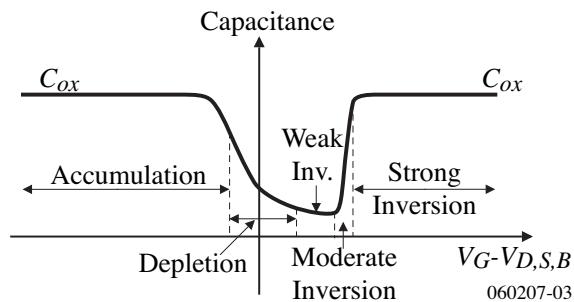
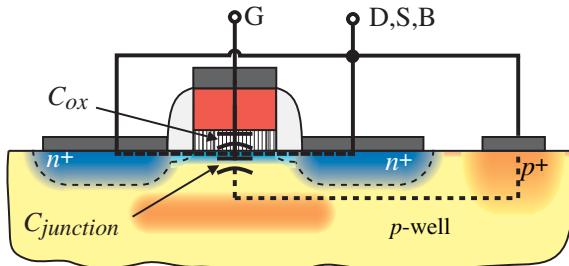
MOSFET Gate Capacitor Structure

The MOSFET gate capacitors have the gate as one terminal of the capacitor and some combination of the source, drain, and bulk as the other terminal.

In the model of the MOSFET gate capacitor shown below, the gate capacitance is really two capacitors in series depending on the condition of the channel.



MOSFET Gate Capacitor as a function of V_{GS} with D=S=B



Operation:

In this configuration, the MOSFET gate capacitor has 5 regions of operation as V_{GS} is varied. They are:

- 1.) Accumulation
- 2.) Depletion
- 3.) Weak inversion
- 4.) Moderate inversion
- 5.) Strong inversion

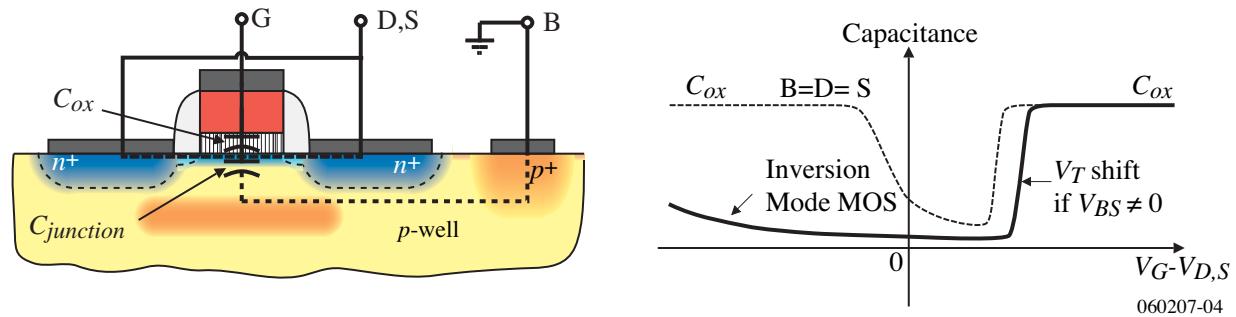
For the first four regions, the gate capacitance is the series combination of C_{ox} and C_j given as,

$$C_{\text{gate}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_j}}$$

Use of a 3 Segment Model to Explain the Gate Capacitor Variation

Region	Channel R	C_{ox} and C_j	C_{gate}	3-Segment Model
Accumulation	Large	In series and $C_j > C_{ox}$	$C_{\text{gate}} \approx C_{ox}$	 070218-01
Depletion	Large	In series and $C_j \approx C_{ox}$	$C_{\text{gate}} \approx 0.5C_{ox} \approx 0.5C_j$	 070218-02
Weak Inversion	Large	In series and $C_j < C_{ox}$	$C_{\text{gate}} \approx C_j$	 070218-03
Moderate Inversion	Moderate	In series and $C_j < C_{\text{gate}} < C_{ox}$	$C_j < C_{\text{gate}} < C_{ox}$	 070218-04
Strong Inversion	Small	In parallel and $C_j < C_{ox}$	$C_{\text{gate}} \approx C_{ox}$	 070218-05

MOSFET Gate Capacitor as a function of V_{GS} with Bulk Fixed (Inversion Mode)



Conditions:

- D = S, B = V_{SS}
- Accumulation region removed by connecting bulk to V_{DD}
- Nonlinear
- Channel resistance:

$$R_{on} = \frac{L}{12K_P'(V_{BG}-|V_T|)}$$

- LDD transistors will give lower Q because of the increased series resistance

Inversion Mode NMOS Capacitor

Best results are obtained when the drain-source are connected to ac ground.

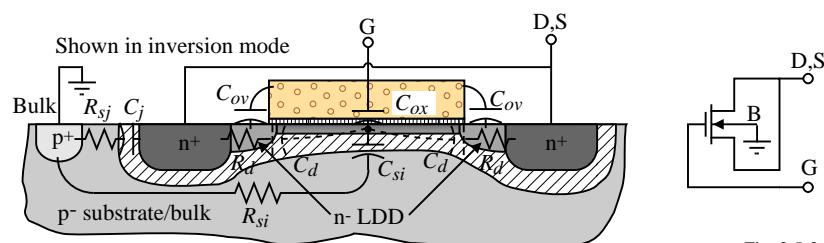
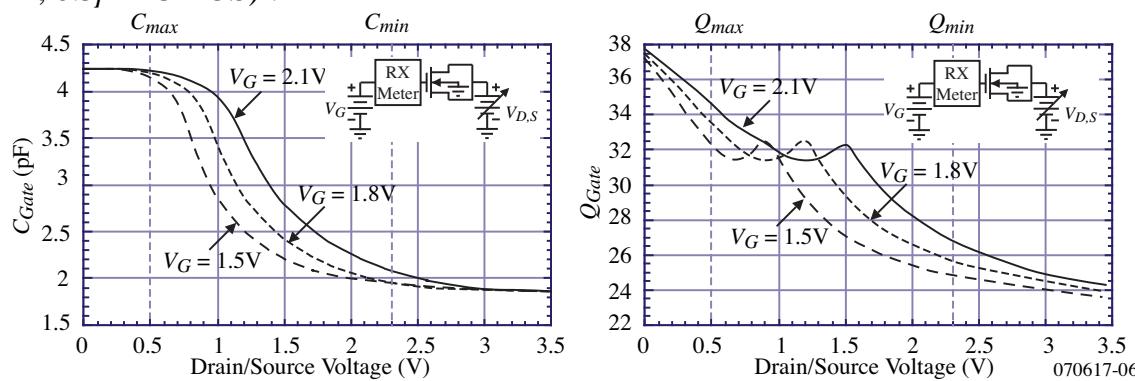


Fig. 2.5-2

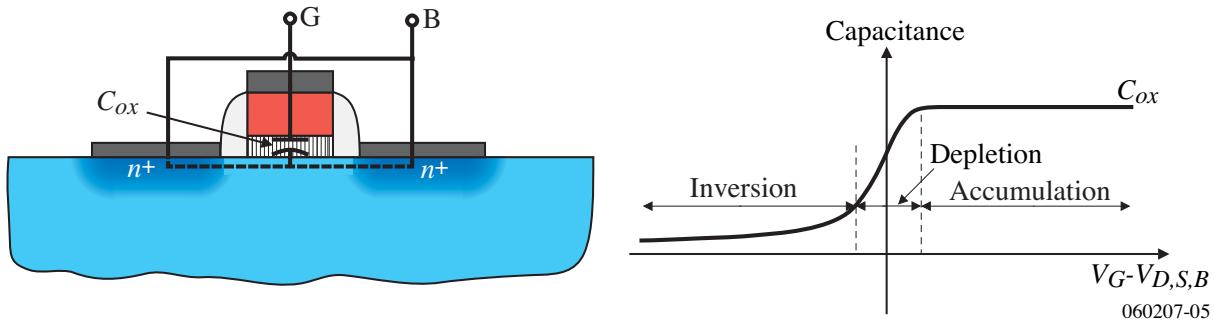
Experimental Results (Q at 2GHz, 0.5μm CMOS)[†]:



$V_G = 1.8V$: C_{max}/C_{min} ratio = 2.15 (1.91), $Q_{max} = 34.3$ (5.4), and $Q_{min} = 25.8$ (4.9)

[†] E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001.
CMOS Analog Circuit Design © P.E. Allen - 2010

Accumulation Mode NMOS Gate Capacitor



Conditions:

- Remove p⁺ drain and source and put n⁺ bulk contacts instead.
- Implements a variable capacitor with a larger transition region between the maximum and minimum values.
- Reasonably linear capacitor for values of $V_{GB} > 0$

Accumulation Mode Capacitor – Continued

Best results are obtained when the drain-source are on ac ground.

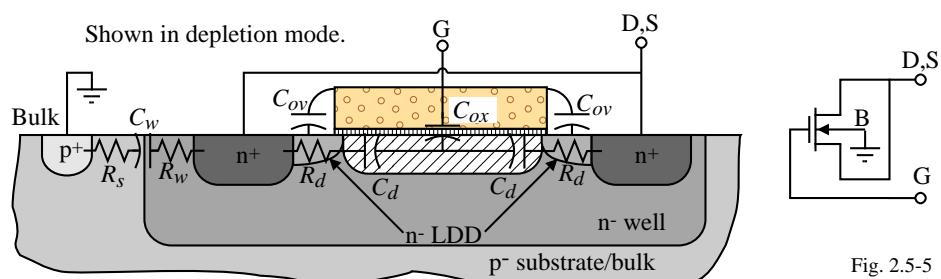
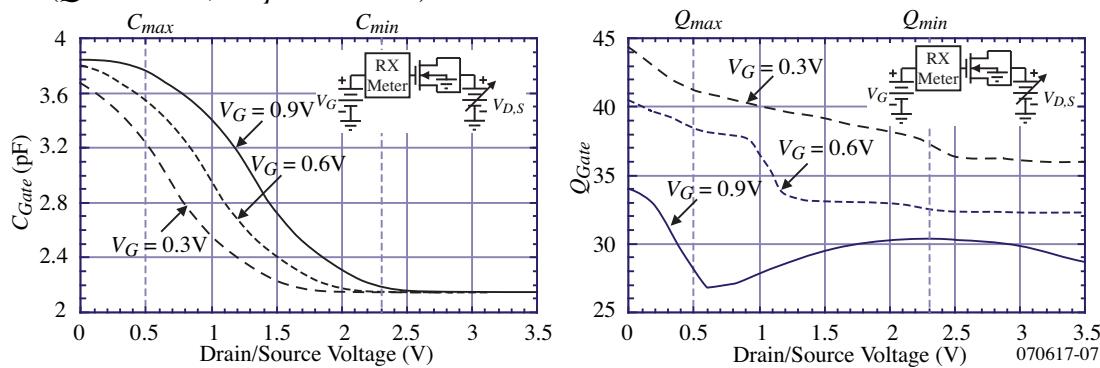


Fig. 2.5-5

Experimental Results (Q at 2GHz, 0.5μm CMOS)[†]:



$$V_G = 0.6V: C_{max}/C_{min} \text{ ratio} = 1.69 (1.61), Q_{max} = 38.3 (15.0), \text{ and } Q_{min} = 33.2 (13.6)$$

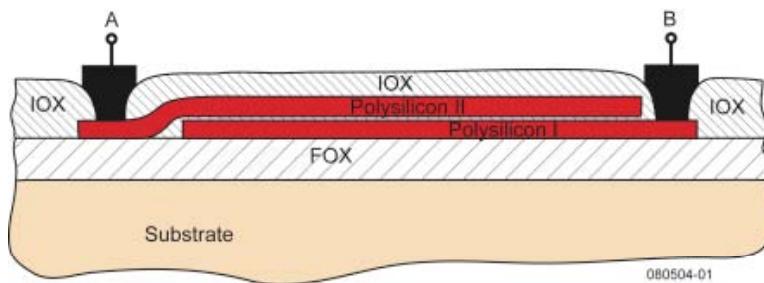
[†]E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001.
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CONDUCTOR-INSULATOR-CONDUCTOR CAPACITORS

Polysilicon-Oxide-Polysilicon (Poly-Poly) Capacitors

LOCOS Technology:

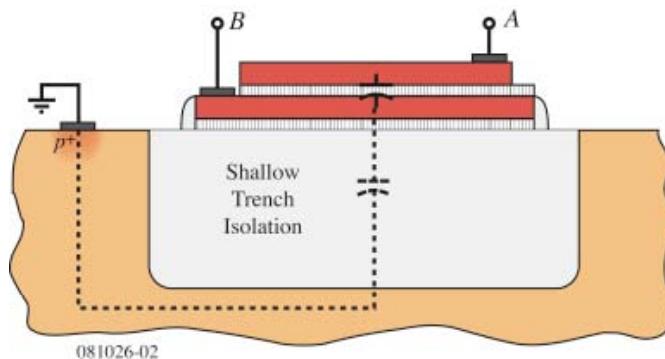
A very linear capacitor with minimum bottom plate parasitic.



080504-01

DSM Technology:

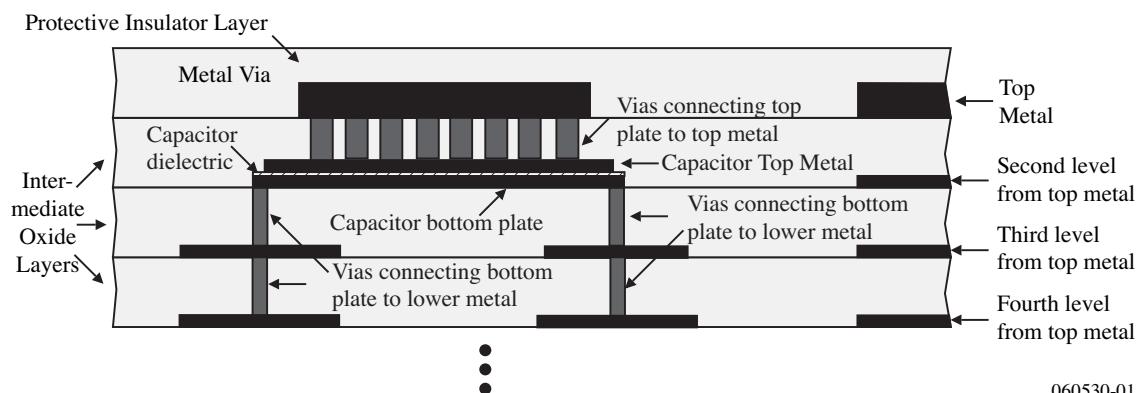
A very linear capacitor with small bottom plate parasitic.



081026-02

Metal-Insulator-Metal (MiM) Capacitors

In some processes, there is a thin dielectric between a metal layer and a special metal layer called “capacitor top metal”. Typically the capacitance is around $1\text{fF}/\mu\text{m}^2$ and is at the level below top metal.

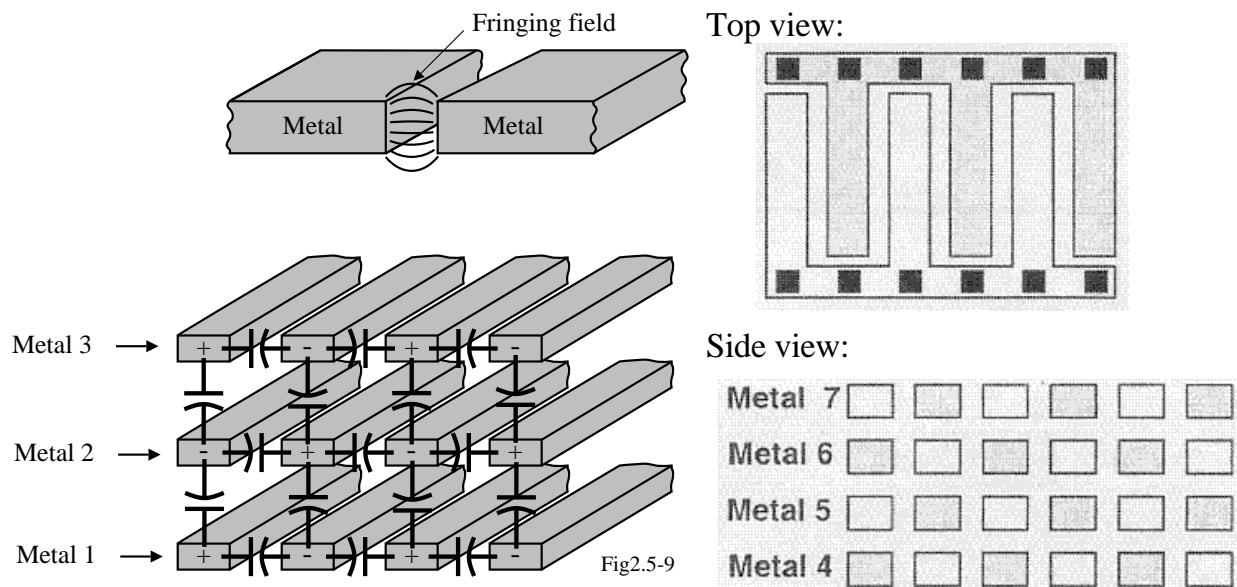


060530-01

Good matching is possible with low parasitics.

Metal-Insulator-Metal Capacitors – Lateral and Vertical Flux

Capacitance between conductors on the same level and use lateral flux.

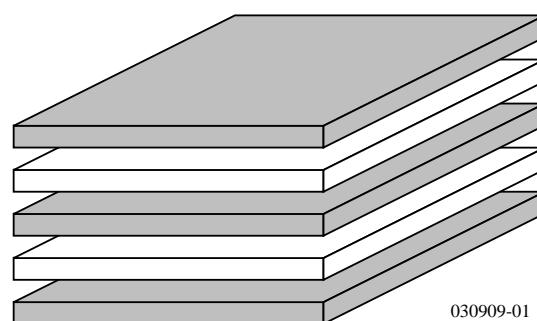


These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with a near-infinite perimeter.
The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

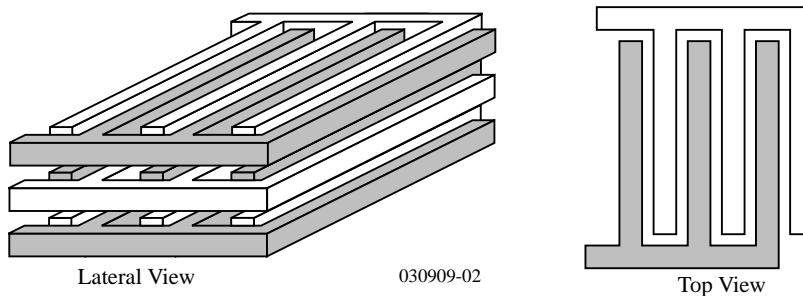
More Detail on Horizontal Metal Capacitors[†]

Some of the possible metal capacitor structures include:

- 1.) Horizontal parallel plate (HPP).



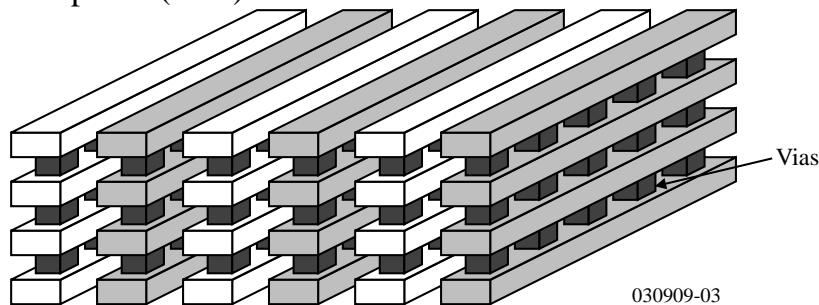
- 2.) Parallel wires (PW):



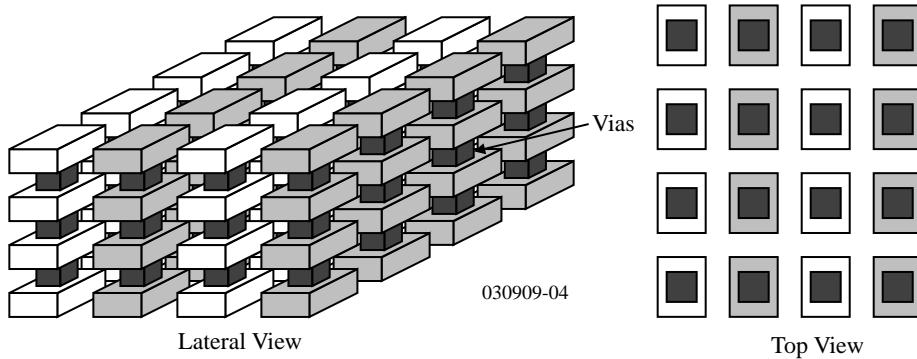
[†] R. Aparicio and A. Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors, *IEEE J. of Solid-State Circuits*, vol. 37, no. 3, March 2002, pp. 384-393.

Horizontal Metal Capacitors - Continued

3.) Vertical parallel plates (VPP):



4.) Vertical bars (VB):



Horizontal Metal Capacitors - Continued

Experimental results for a CMOS process with 3 layers of metal, $L_{min} = 0.5\mu\text{m}$, $t_{ox} = 0.95\mu\text{m}$ and $t_{metal} = 0.63\mu\text{m}$ for the bottom 2 layers of metal.

Structure	Cap. Density (aF/ μm^2)	$C_{aver.}$ (pF)	Std. Dev. (fF)	$\frac{\sigma}{C_{aver.}}$	$f_{res.}$ (GHz)	Q @ 1 GHz	R_s (Ω)	Break- down (V)
VPP	158.3	18.99	103	0.0054	3.65	14.5	0.57	355
PW	101.5	33.5	315	0.0094	1.1	8.6	0.55	380
HPP	35.8	6.94	427	0.0615	6.0	21	1.1	690

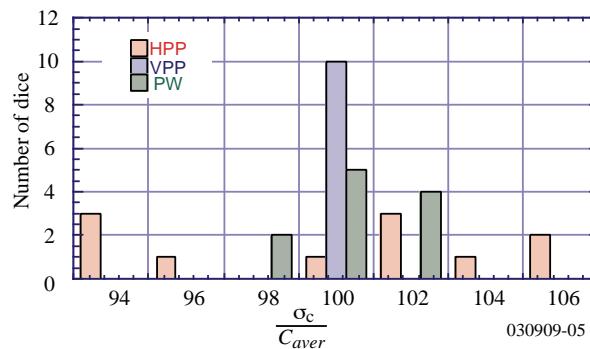
Experimental results for a digital CMOS process with 7 layers of metal, $L_{min} = 0.24\mu\text{m}$, $t_{ox} = 0.7\mu\text{m}$ and $t_{metal} = 0.53\mu\text{m}$ for the bottom 5 layers of metal. All capacitors = 1 pF.

Structure (1 pF)	Cap. Density (aF/ μm^2)	$C_{aver.}$ (pF)	Area (μm^2)	Cap. Enhanc- ement	Std. Dev. (fF)	$\frac{\sigma}{C_{aver.}}$	$f_{res.}$ (GHz)	Q @ 1 GHz	Break- down (V)
VPP	1512.2	1.01	670	7.4	5.06	0.0050	> 40	83.2	128
VB	1281.3	1.07	839.7	6.3	14.19	0.0132	37.1	48.7	124
HPP	203.6	1.09	5378	1.0	26.11	0.0239	21	63.8	500
MIM	1100	1.05	960.9	5.4	-	-	11	95	-

Horizontal Metal Capacitors - Continued

Histogram of the capacitance distribution for the above case (1 pF):

Experimental results for a digital CMOS process with 7 layers of metal, $L_{min} = 0.24\mu\text{m}$, $t_{ox} = 0.7\mu\text{m}$ and $t_{metal} = 0.53\mu\text{m}$ for the bottom 5 layers of metal (all capacitors = 10pF):



Structure (10 pF)	Cap. Density (aF/ μm^2)	C _{aver.} (pF)	Area (μm^2)	Cap. Enhancement	Std. Dev. (fF)	$\frac{\sigma}{C_{aver.}}$	f _{res.} (GHz)	Q @ 1 GHz	Break-down (V)
VPP	1480.0	11.46	7749	8.0	73.43	0.0064	11.3	26.6	125
VB	1223.2	10.60	8666	6.6	73.21	0.0069	11.1	17.8	121
HPP	183.6	10.21	55615	1.0	182.1	0.0178	6.17	23.5	495
MIM	1100	10.13	9216	6.0	-	-	4.05	25.6	-

DEVIATION FROM IDEAL BEHAVIOR IN CAPACITORS

Capacitor Errors

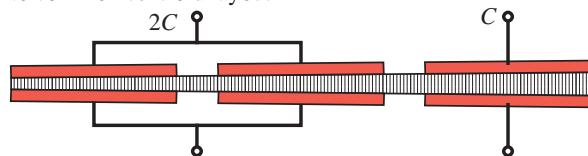
- 1.) Dielectric gradients
- 2.) Edge effects
- 3.) Process biases
- 4.) Parasitics
- 5.) Voltage dependence
- 6.) Temperature dependence

Capacitor Errors - Oxide Gradients

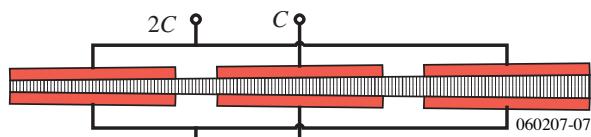
Error due to a variation in dielectric thickness across the wafer.

Common centroid layout - only good for one-dimensional errors:

No common centroid layout

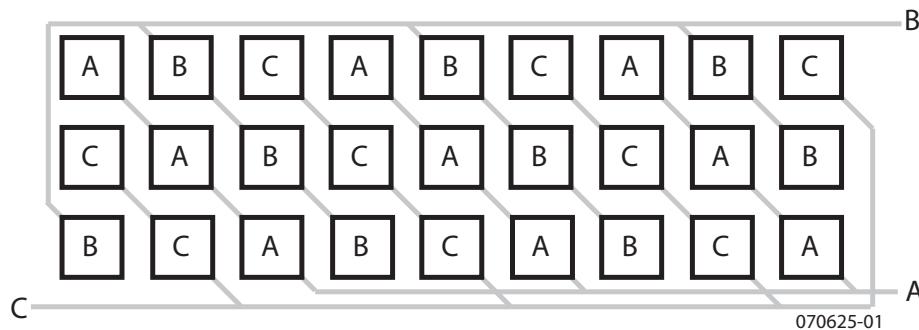


Common centroid layout



An alternate approach is to layout numerous repetitions and connect them randomly to achieve a statistical error balanced over the entire area of interest.

Improved matching of three components, A, B, and C:



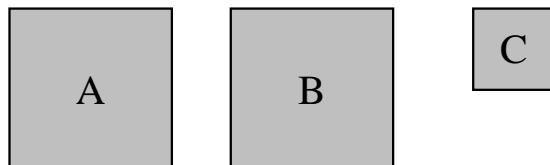
Capacitor Errors - Edge Effects

There will always be a randomness on the definition of the edge.

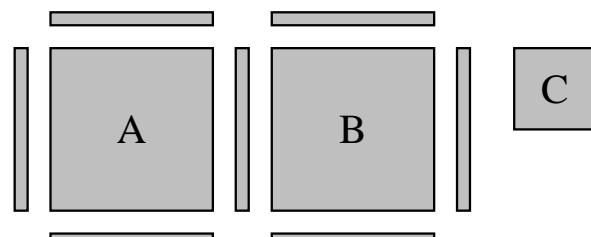
However, etching can be influenced by the presence of adjacent structures.

For example,

Matching of A and B are disturbed by the presence of C.

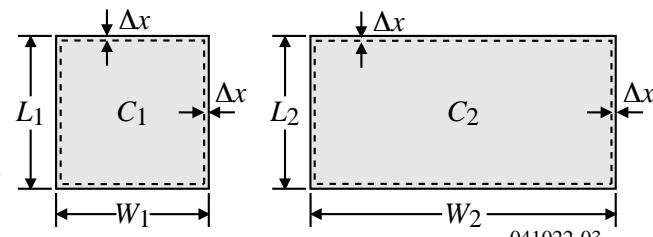


Improved matching achieve by matching the surroundings of A and B.



Process Bias on Capacitors

Consider the following two capacitors:



If $L_1 = L_2 = 2\mu\text{m}$, $W_2 = 2W_1 = 4\mu\text{m}$ and $\Delta x = 0.1\mu\text{m}$, the ratio of C_2 to C_1 can be written as,

$$\frac{C_2}{C_1} = \frac{(2-2)(4-2)}{(2-2)(2-2)} = \frac{3.8}{1.8} = 2.11 \rightarrow 5.6\% \text{ error in matching}$$

How can this matching error be reduced?

The capacitor ratios in general can be expressed as,

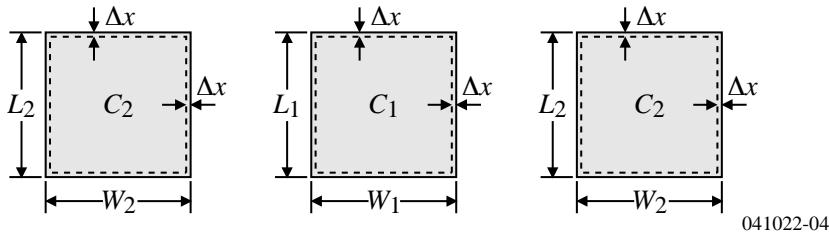
$$\frac{C_2}{C_1} = \frac{(L_2-2\Delta x)(W_2-2\Delta x)}{(L_1-2\Delta x)(W_1-2\Delta x)} = \frac{W_2}{W_1} \left(\frac{1 - \frac{2\Delta x}{W_2}}{1 - \frac{2\Delta x}{W_1}} \right) \approx \frac{W_2}{W_1} \left(1 - \frac{2\Delta x}{W_2} \right) \left(1 + \frac{2\Delta x}{W_1} \right) \approx \frac{W_2}{W_1} \left[1 - \frac{2\Delta x}{W_2} + \frac{2\Delta x}{W_1} \right]$$

Therefore, if $W_2 = W_1$, the matching error should be minimized. The best matching results between two components are achieved when their geometries are identical.

Replication Principle

Based on the previous result, a way to minimize the matching error between two or more geometries is to insure that the matched components have the same area to periphery ratio. Therefore, the replication principle requires that all geometries have the same area-periphery ratio.

Correct way to match the previous capacitors (the two C_2 capacitors are connected together):



If $L_1 = L_2 = 2\mu\text{m}$, $W_2 = 2W_1 = 2\mu\text{m}$ and $\Delta x = 0.1\mu\text{m}$, the ratio of C_2 to C_1 can be written as,

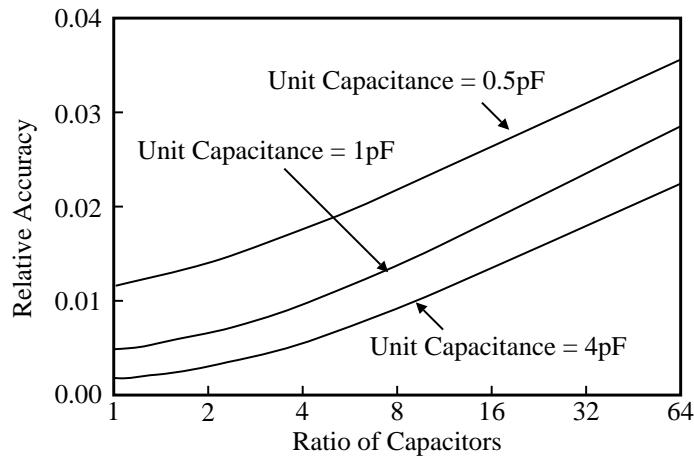
$$\frac{C_2}{C_1} = \frac{2(2-2)(2-2)}{(2-2)(2-2)} = \frac{2 \cdot 1.8}{1.8} = 2 \rightarrow 0\% \text{ error in matching}$$

The replication principle works for any geometry and includes transistors, resistors as well as capacitors.

Capacitor Errors - Relative Accuracy

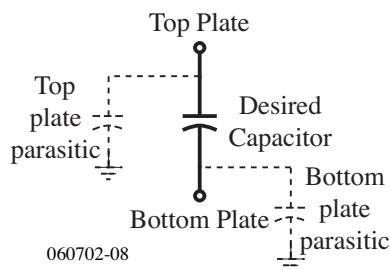
Capacitor relative accuracy is proportional to the area of the capacitors and inversely proportional to the difference in values between the two capacitors.

For example,



Capacitor Errors - Parasitics

Parasitics are normally from the top and bottom plate to ac ground which is typically the substrate.

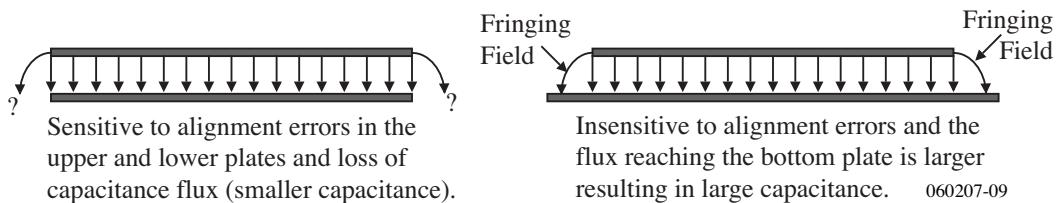


Top plate parasitic is 0.01 to 0.001 of $C_{desired}$

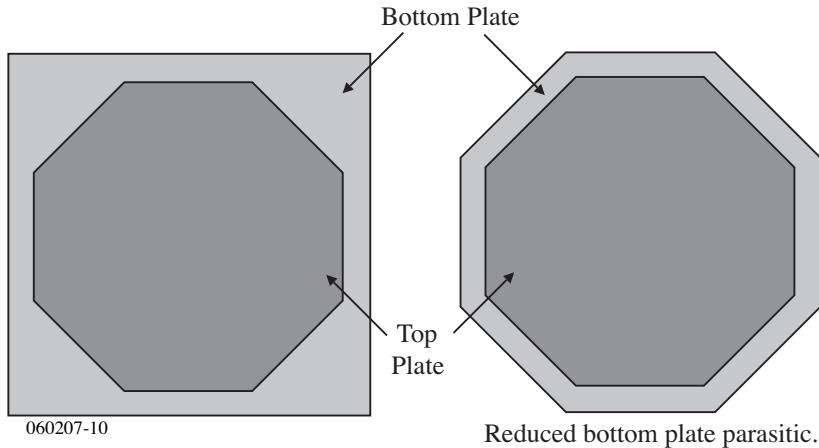
Bottom plate parasitic is 0.05 to 0.2 $C_{desired}$

Layout Considerations on Capacitor Accuracy

Decreasing Sensitivity to Edge Variation:



A structure that minimizes the ratio of perimeter to area (circle is best).

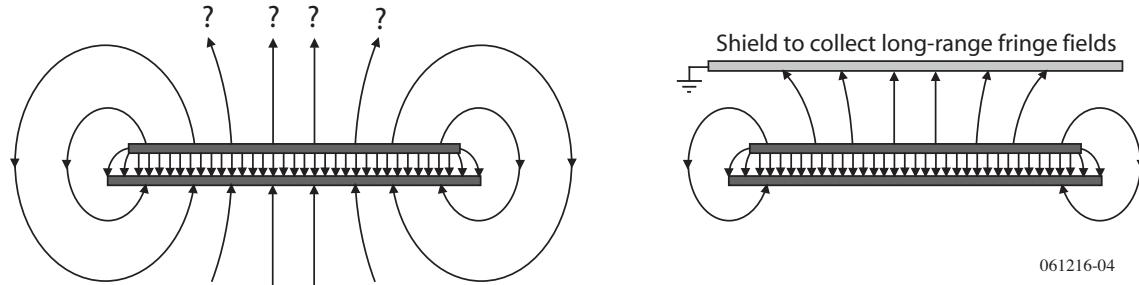


Accurate Matching of Capacitors[†]

Accurate matching of capacitors depends on the following influence:

- 1.) Mismatched perimeter ratios
- 2.) Proximity effects in unit capacitor photolithography
- 3.) Mismatched long-range fringe capacitance
- 4.) Mismatched interconnect capacitance
- 5.) Parasitic interconnect capacitance

Long-range fringe capacitance:



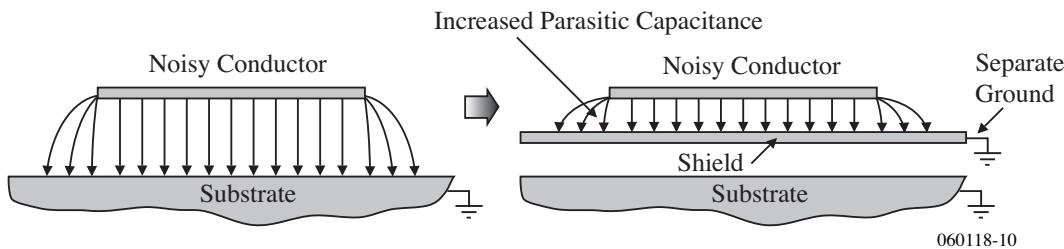
Obviously there will be a tradeoff between matching and speed.

[†] M.J. McNutt, S. LeMarquis and J.L. Dunkley, "Systematic Capacitance Matching Errors and Corrective Layout Procedures," *IEEE J. of Solid-State Circuit*, vo. 29, No. 5, May 1994, pp. 611-616.
CMOS Analog Circuit Design

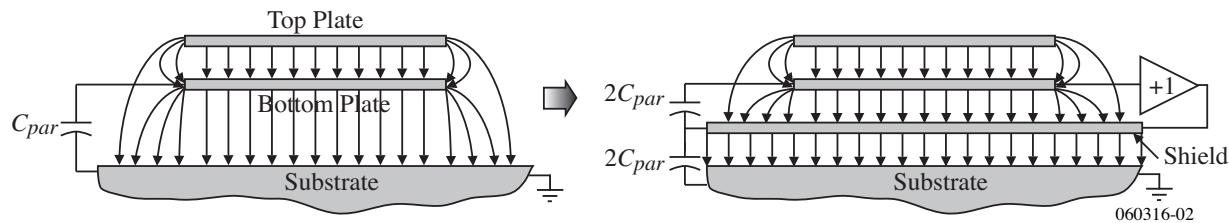
Shielding

The key to shielding is to determine and control the electric fields.

Consider the following noisy conductor and its influence on the substrate:



Use of bootstrapping to reduce capacitor bottom plate parasitic:



Definition of Temperature and Voltage Coefficients

In general a variable y which is a function of x , $y = f(x)$, can be expressed as a Taylor series,

$$y(x) \approx y(x_0) + a_1(x - x_0) + a_2(x - x_0)^2 + a_3(x - x_0)^3 + \dots$$

where the coefficients, a_i , are defined as,

$$a_1 = \frac{df(x)}{dx} \Big|_{x=x_0}, \quad a_2 = \frac{1}{2} \frac{d^2f(x)}{dx^2} \Big|_{x=x_0}, \dots$$

The coefficients, a_i , are called the first-order, second-order, temperature or voltage coefficients depending on whether x is temperature or voltage.

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called *fractional temperature coefficient*, TC_F , which is defined as,

$$TC_F(T=T_0) = \frac{1}{f(T=T_0)} \frac{df(T)}{dT} \Big|_{T=T_0} \text{ parts per million/}^\circ\text{C (ppm/}^\circ\text{C)}$$

or more simply,

$$TC_F = \frac{1}{f(T)} \frac{df(T)}{dT} \text{ parts per million/}^\circ\text{C (ppm/}^\circ\text{C)}$$

A similar definition holds for fractional voltage coefficient.

Capacitor Errors - Temperature and Voltage Dependence

MOSFET Gate Capacitors:

Absolute accuracy $\approx \pm 10\%$

Relative accuracy $\approx \pm 0.2\%$

Temperature coefficient $\approx +25 \text{ ppm/C}^\circ$

Voltage coefficient $\approx -50 \text{ ppm/V}$

Polysilicon-Oxide-Polysilicon Capacitors:

Absolute accuracy $\approx \pm 10\%$

Relative accuracy $\approx \pm 0.2\%$

Temperature coefficient $\approx +25 \text{ ppm/C}^\circ$

Voltage coefficient $\approx -20 \text{ ppm/V}$

Metal-Dielectric-Metal Capacitors:

Absolute accuracy $\approx \pm 10\%$

Relative accuracy $\approx \pm 0.6\%$

Temperature coefficient $\approx +40 \text{ ppm/C}^\circ$

Voltage coefficient $\approx -20 \text{ ppm/V}, 5 \text{ ppm/V}^2$

Accuracies depend upon the size of the capacitors.

Future Technology Impact on Capacitors

What will be the impact of scaling down in CMOS technology?

- The capacitance can be divided into gate capacitance and overlap capacitance.
 - Gate capacitance varies with external voltage changes
 - Overlap capacitances are constant with respect to external voltage changes
 - ∴ As the channel length decreases, the gate capacitance becomes less of the total capacitance and consequently the C_{max}/C_{min} will decrease. However, the Q of the capacitor will increase because the physical dimensions are getting smaller.
- For UDSM, the gate leakage current will eliminate gate capacitors from being useful.

Best capacitor for future scaled CMOS?

Polysilicon-polysilicon or metal-metal (too much leakage current in gate capacitors)

Best varactor for future scaled CMOS?

The standard mode CMOS depletion capacitor because C_{max}/C_{min} is larger than that for the accumulation mode and Q should be sufficient. The pn junction will be more useful for UDSM.

SUMMARY

- Capacitors are made from:
 - pn junctions (depletion capacitors)
 - MOSFET gate capacitors
 - Conductor-insulator-conductor capacitors
- Capacitors are characterized by:
 - Q , a measure of the loss
 - Density
 - Parasitics
 - Absolute and relative accuracies
- Deviations from ideal capacitor behavior include;
 - Dielectric gradients
 - Edge effects (etching)
 - Process biases
 - Parasitics
 - Voltage and temperature dependence

LECTURE 070 – RESISTORS AND INDUCTORS

LECTURE ORGANIZATION

Outline

- Resistors
- Inductors
- Summary

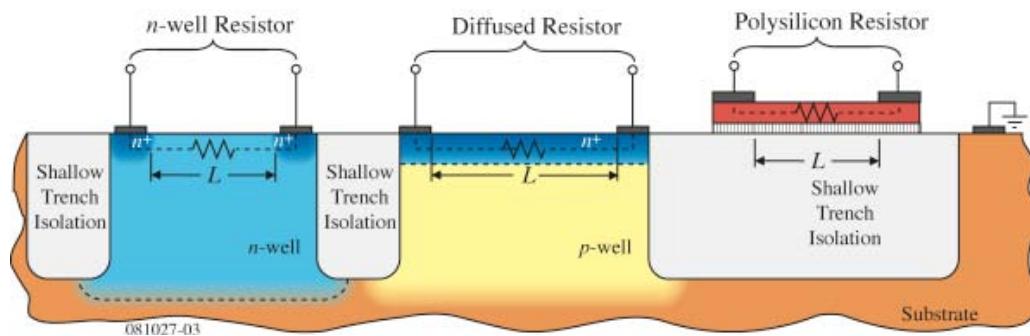
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 47-48, 60-63 and new material

RESISTORS

Types of Resistors Compatible with CMOS Technology

- 1.) Diffused and/or implanted resistors.
- 2.) Well resistors.
- 3.) Polysilicon resistors.
- 4.) Metal resistors.

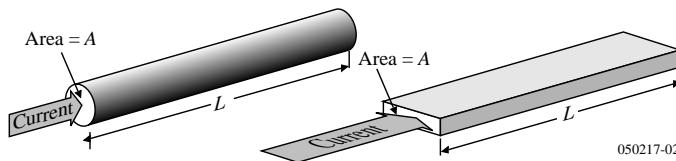


Characterization of Resistors

1.) Value

$$R = \frac{\rho L}{A}$$

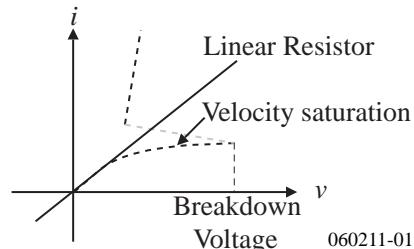
AC and DC resistance



2.) Linearity

Does $V = IR$?

Velocity saturation of carriers



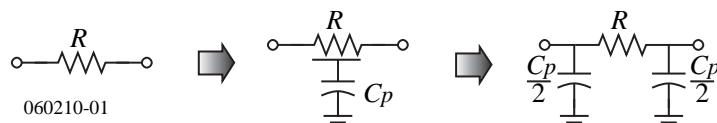
3.) Power

$$P = VI = I^2 R$$

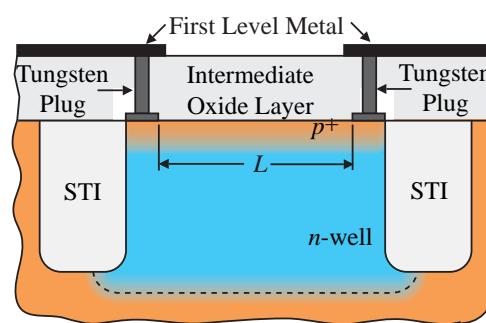
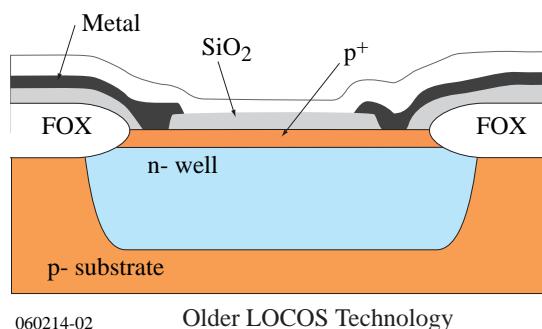
4.) Current

Electromigration

5.) Parasitics



MOS Resistors - Source/Drain Resistor



Diffusion:

10-100 ohms/square

Absolute accuracy = $\pm 35\%$

Relative accuracy = 2% ($5\mu\text{m}$), 0.2% ($50\mu\text{m}$)

Temperature coefficient = +1500 ppm/ $^\circ\text{C}$

Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square

Absolute accuracy = $\pm 15\%$

Relative accuracy = 2% ($5\mu\text{m}$), 0.15% ($50\mu\text{m}$)

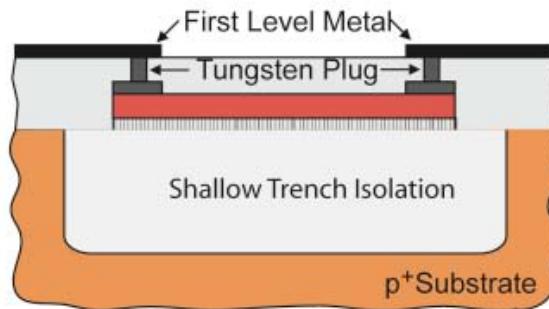
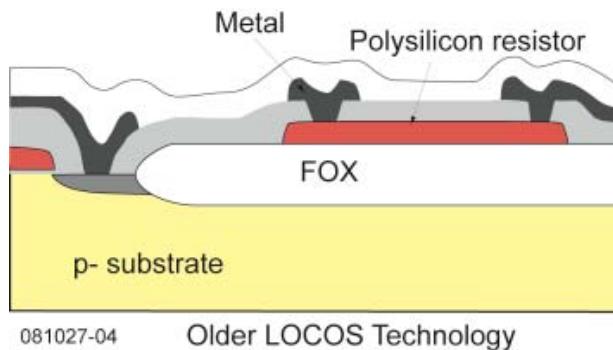
Temperature coefficient = +400 ppm/ $^\circ\text{C}$

Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor

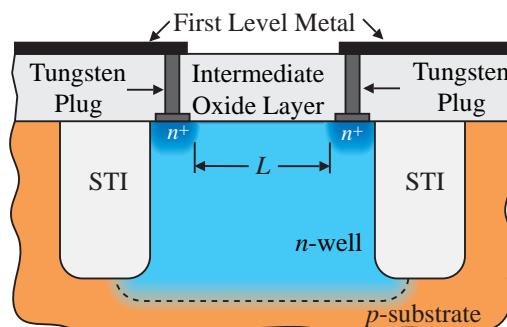
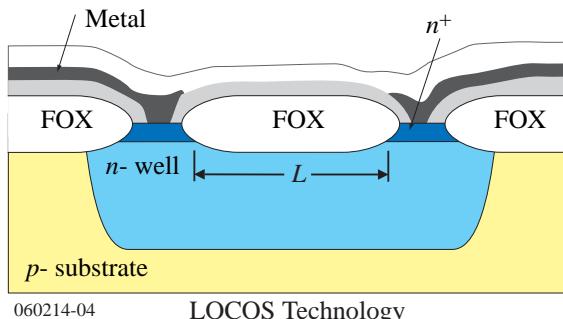


30-100 ohms/square (unshielded)
 100-500 ohms/square (shielded)
 Absolute accuracy = $\pm 3\%$
 Relative accuracy = 2% ($5 \mu\text{m}$)
 Temperature coefficient = 500-1000 ppm/ $^{\circ}\text{C}$
 Voltage coefficient $\approx 100 \text{ ppm/V}$

Comments:

- Used for fuzzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor



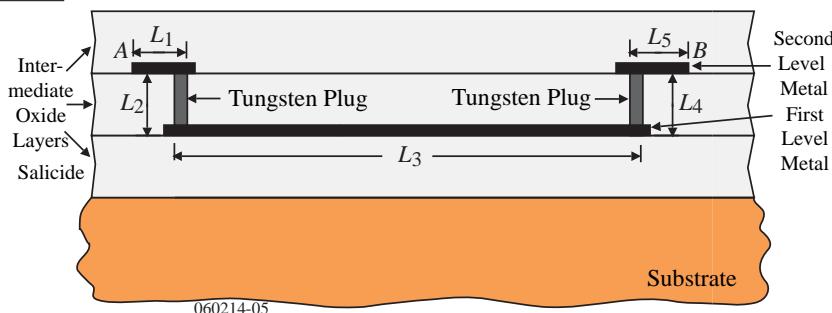
1000-5000 ohms/square
 Absolute accuracy = $\pm 40\%$
 Relative accuracy $\approx 5\%$
 Temperature coefficient = 4000 ppm/ $^{\circ}\text{C}$
 Voltage coefficient is large $\approx 8000 \text{ ppm/V}$

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent
- Could put a p^+ diffusion into the well to form a pinched resistor

Metal as a Resistor

Illustration:



Resistance from A to B = Resistance of segments L_1, L_2, L_3, L_4 , and L_5 with some correction subtracted because of corners.

Sheet resistance:

$50\text{-}70 \text{ m}\Omega/\square \pm 30\%$ for lower or middle levels of metal

$30\text{-}40 \text{ m}\Omega/\square \pm 15\%$ for top level metal

Watch out for the current limit for metal resistors.

Contact resistance varies from 5Ω to 10Ω .

Tempco $\approx +4000 \text{ ppm}/^\circ\text{C}$

Need to derate the current at higher temperatures:

$$I_{DC}(T_j) = D_t I_{DC}(T_r)$$

$T_j(\text{ }^\circ\text{C})$	$T_r(\text{ }^\circ\text{C})$	D_t
<85	85	1
100	85	0.63
110	85	0.48
125	85	0.32
150	85	0.18

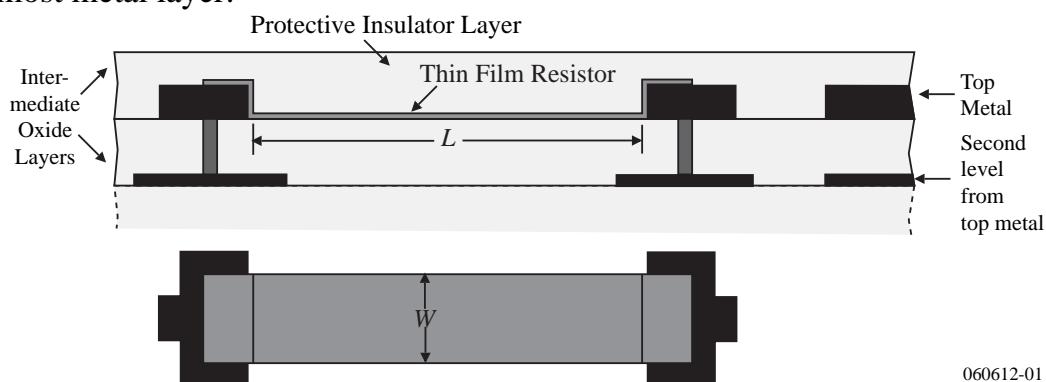
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Thin Film Resistors

A high-quality resistor fabricated from a thin nickel-chromium alloy or a silicon-chromium mixture.

Uppermost metal layer:



Performance:

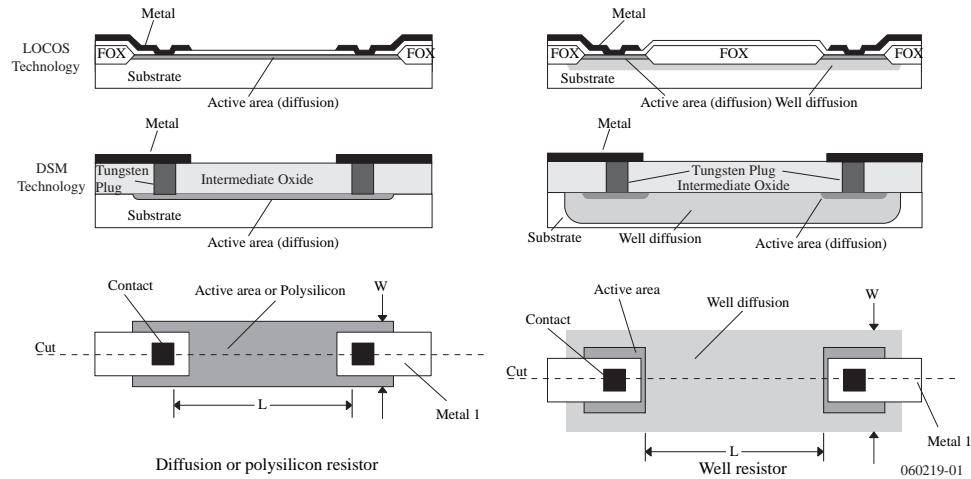
Sheet resistivity is approximately $5\text{-}10 \text{ ohms/square}$

Temperature coefficients of less than $100 \text{ ppm}/^\circ\text{C}$

Absolute tolerance of better than $\pm 0.1\%$ using laser trimming

Selectivity of the metal etch must be sufficient to ensure the integrity of the thin-film resistor beneath the areas where metal is etched away.

Resistor Layout Techniques



End structure calculations:

Diagram showing a resistor structure with contacts and silicon regions. Dimensions labeled are x_{con} , x_{c-r} , and W .

$$\Delta R_1 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh(sil)}} \left(\frac{X_{c-r} + 0.75 \cdot L_{\text{con}}}{W - 2 \cdot D W_{\text{sil}}} \right) \Delta R_{\text{total}} = \left(\frac{1}{\Delta R_1} + \frac{1}{\Delta R_2} + \dots \right)^{-1}$$

$(L_{\text{con}} = \text{width of the contact})$

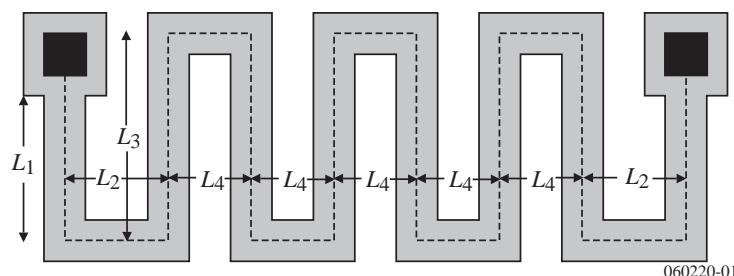
$$\Delta R_2 = \frac{R_{\text{cont}}}{N_{\text{cont}}} + R_{\text{sh(sil)}} \left(\frac{X_{c-r} + X_{\text{con}} + 1.75 \cdot L_{\text{con}}}{W - 2 \cdot \Delta W_{\text{sil}}} \right)$$

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Extending the Length of Resistors

Snaked Resistors:



Corner corrections:

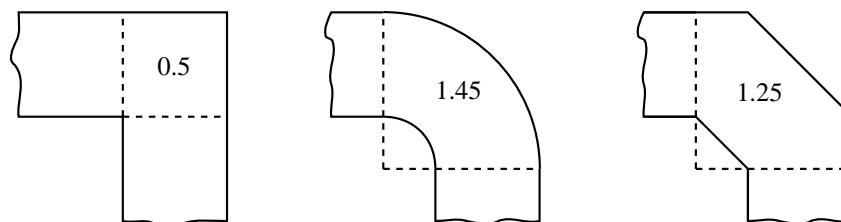
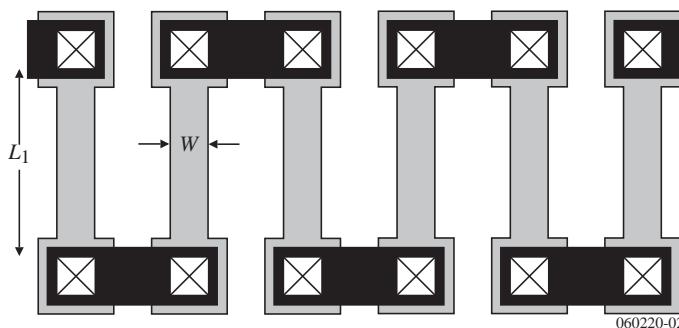


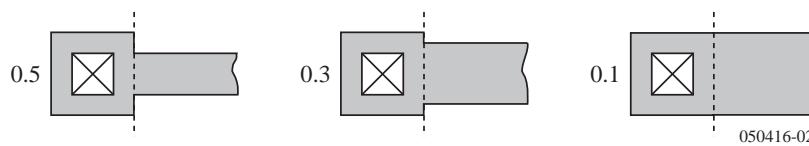
Fig. 2.6-16B

Extending the Length of Resistors

Series Resistors:



Resistor Ending



Influence:

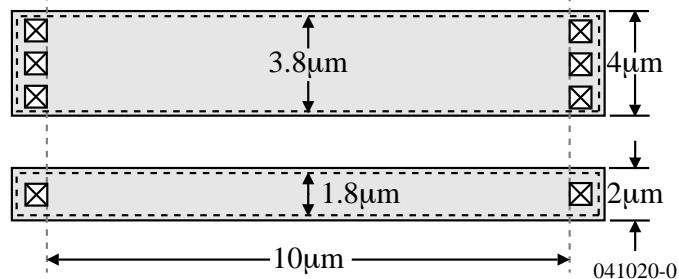
Process Bias Influence on Resistors

Process bias is where the dimensions of the fabricated geometries are not the same as the layout data base dimensions.

Process biases introduce systematic errors.

Consider the effect of over-etching-

Assume that etching introduces a process bias of $0.1\mu m$. Two resistors designed to have a ratio of 2:1 have equal lengths but the widths are different by a factor of two.



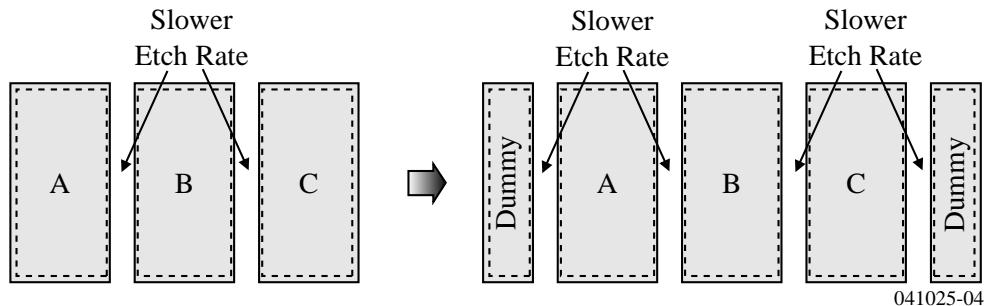
The actual matching ratio due to the etching bias is,

$$\frac{R_2}{R_1} = \frac{W_1}{W_2} = \frac{4-0.2}{2-0.2} = \frac{3.8}{1.8} = 2.11 \rightarrow 5.6\% \text{ error in matching}$$

Use the replication principle to eliminate this error.

Etch Rate Variations – Polysilicon Resistors

The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant. This is illustrated below:



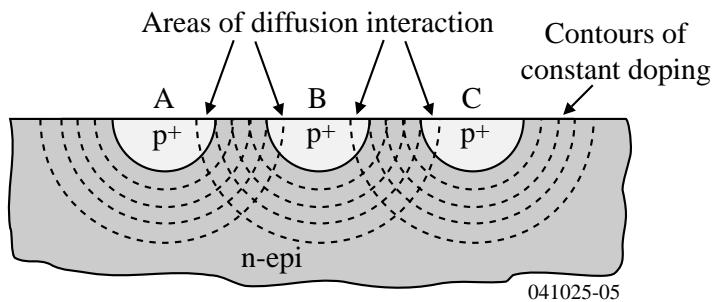
The objective is to make $A = B = C$. In the left-hand case, B is larger due to the slower etch rates on *both* sides of B. In the right-hand case, the dummy strips have caused the etch rates on both sides of A, B and C to be identical leading to better matching.

It may be advisable to connect the dummy strips to ground or some other low impedance node to avoid static electrical charge buildup.

Diffusion Interaction – Diffused Resistors

Problem:

Consider three adjacent p^+ diffusions into a n epitaxial region,



If A, B, and C are resistors that are to be matched, we see that the effective concentration of B is larger than A or C because of diffusion interaction. This would cause the B resistor to be smaller even though the geometry is identical.

Solution: Place identical dummy resistors to the left of A and right of C. Connect the dummy resistors to a low impedance to prevent the formation of floating diffusions that might increase the sensitivity to latchup.

Thermoelectric Effects

The thermoelectric effect, also called the Seebeck effect, is a potential difference that is developed between two dissimilar materials that are at different temperatures. The potential developed is given as,

$$V_\gamma = S \cdot \Delta T$$

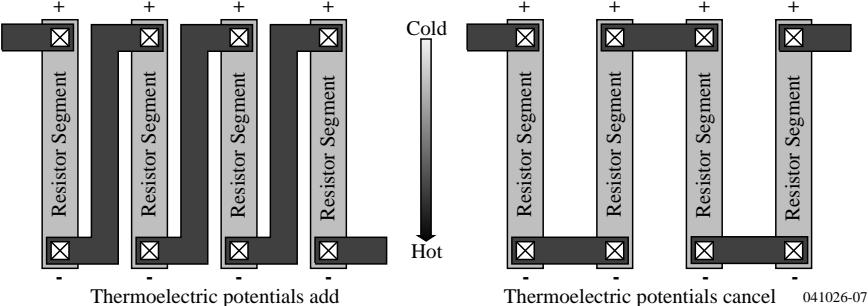
where,

S = Seebeck coefficient ($\approx 0.4\text{mV}/^\circ\text{C}$)

ΔT = temperature difference between the two metals

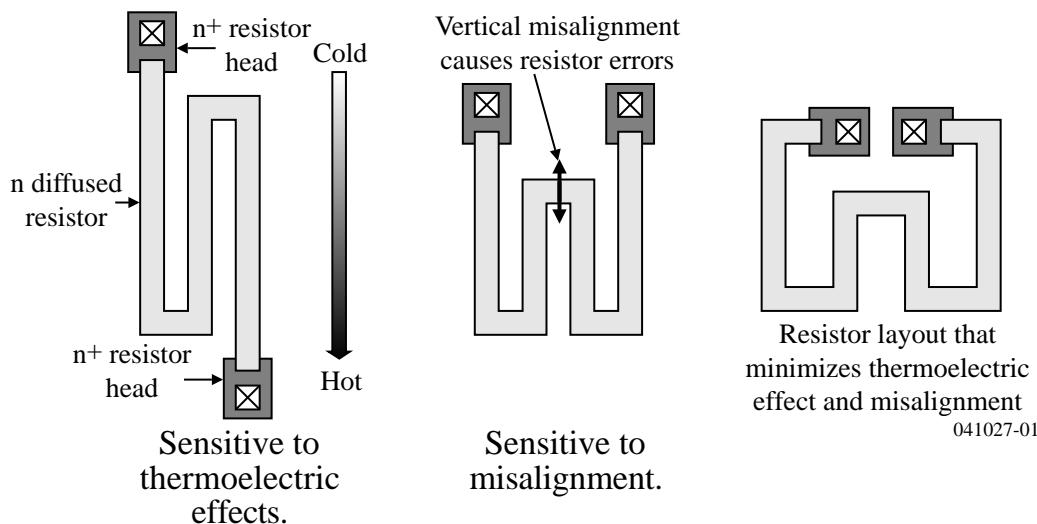
Thus, a temperature difference between the contacts to a resistor and the resistor of 1°C can generate a voltage of 0.4mV causing problems in certain circuits (bandgap).

Two possible resistor layouts with regard to the thermoelectric effect:



High Sheet Resistivity Resistor Layout

High sheet resistivity resistors must use p^+ or n^+ in order to make contacts to metal. Thus, there is plenty of opportunity for the thermoelectric effect to cause problems if care is not taken. Below are three high sheet resistor layouts with differing thermoelectric performance.



Future Technology Impact on Resistors

What will be the impact of scaling down in CMOS technology?

- If the size of the resistor remains the same, there will be little impact.
- If the size scales with the technology, the contacts and connections to the resistors will have more influence on the resistor.

MOS Passive RC Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOSFET gate Cap.	6-7 fF/ μm^2	10%	0.1%	20ppm/ $^\circ\text{C}$	$\pm 20\text{ppm/V}$
Poly-Poly Capacitor	0.3-0.4 fF/ μm^2	20%	0.1%	25ppm/ $^\circ\text{C}$	$\pm 50\text{ppm/V}$
Metal-Metal Capacitor	0.1-1fF/ μm^2	10%	0.6%	??	??
Diffused Resistor	10-100 $\Omega/\text{sq.}$	35%	2%	1500ppm/ $^\circ\text{C}$	200ppm/V
Ion Implanted Resistor	0.5-2 k $\Omega/\text{sq.}$	15%	2%	400ppm/ $^\circ\text{C}$	800ppm/V
Poly Resistor	30-200 $\Omega/\text{sq.}$	30%	2%	1500ppm/ $^\circ\text{C}$	100ppm/V
<i>n</i> -well Resistor	1-10 k $\Omega/\text{sq.}$	40%	5%	8000ppm/ $^\circ\text{C}$	10kppm/V
Top Metal Resistor	30 m $\Omega/\text{sq.}$	15%	2%	4000ppm/ $^\circ\text{C}$??
Lower Metal Resistor	70 m $\Omega/\text{sq.}$	28%	3%	4000ppm/ $^\circ\text{C}$??

INDUCTORS

Characterization of Inductors

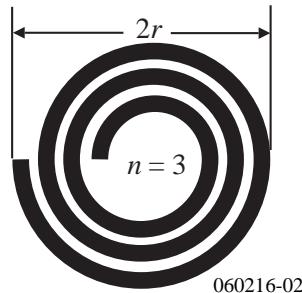
1.) Value of the inductor

Spiral inductor[†]:

$$L \approx \mu_0 n^2 r = 4\pi \times 10^{-7} n^2 r \approx 1.2 \times 10^{-6} n^2 r$$

2.) Quality factor, $Q = \frac{\omega L}{R}$

3.) Self-resonant frequency: $f_{self} = \frac{1}{\sqrt{LC}}$



060216-02

[†] H.M Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, and Packaging*, vol. 10, no. 2, June 1974, pp. 101-109.
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IC Inductors

What is the range of values for on-chip inductors?

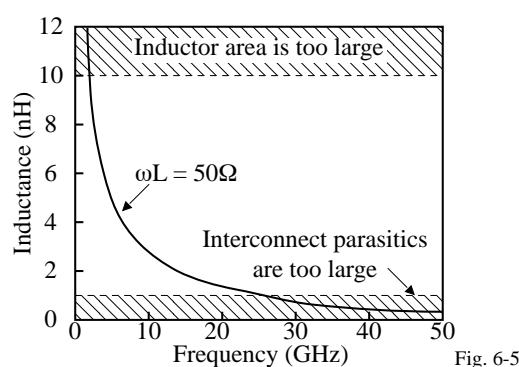


Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 5 \times 10^{-12}} = 5 \text{nH}$$

Note: Off-chip connections will result in inductance as well.

Candidates for inductors in CMOS technology are:

- 1.) Bond wires
- 2.) Spiral inductors
- 3.) Multi-level spiral
- 4.) Solenoid

Bond wire Inductors:

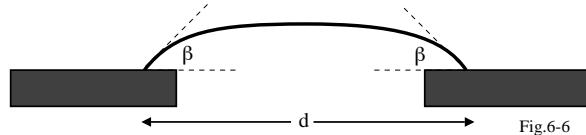


Fig.6-6

- Function of the pad distance d and the bond angle β
- Typical value is 1nH/mm which gives 2nH to 5nH in typical packages
- Series loss is 0.2 Ω/mm for 1 mil diameter aluminum wire
- $Q \approx 60$ at 2 GHz

Planar Spiral Inductors in CMOS Technology

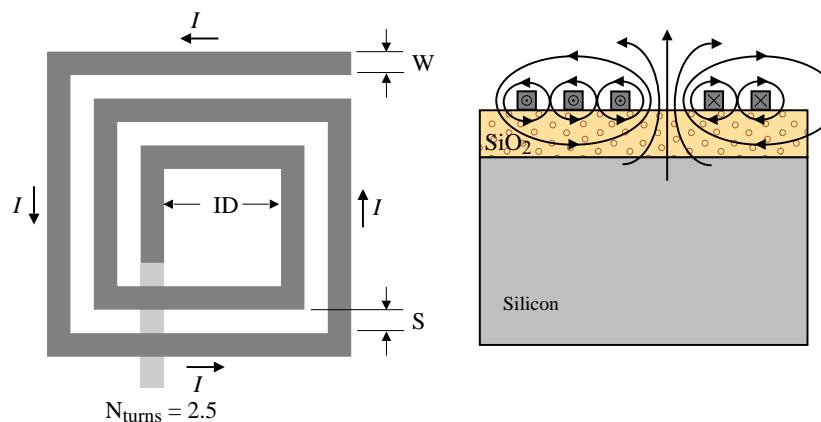


Fig. 6-9

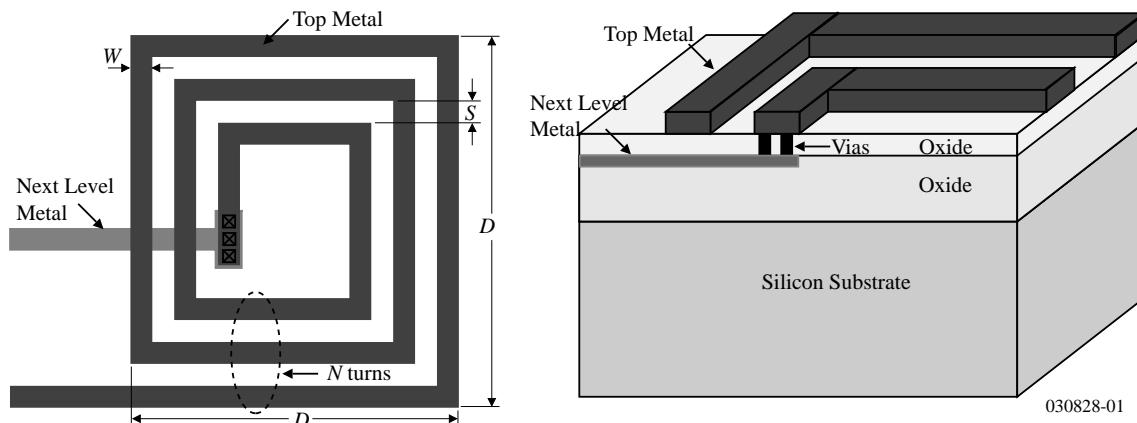
Typically: $3 < N_{\text{turns}} < 5$ and $S = S_{\min}$ for the given current

Select the OD, N_{turns} , and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

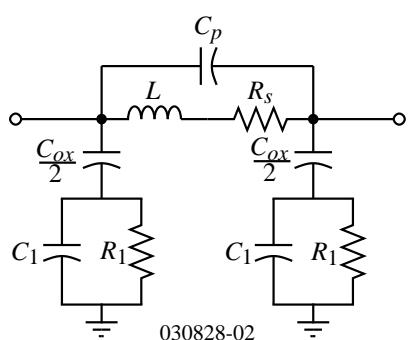
Planar Spiral Inductors on a Lossy Substrate



- Spiral inductor is implemented using metal layers in CMOS technology
- Topmost metal is preferred because of its lower resistivity
- More than one metal layer can be connected together to reduce resistance or area
- Accurate analysis of a spiral inductor requires complex electromagnetic simulation
- Optimize the values of W , S , and N to get the desired L , a high Q , and a high self-resonant frequency
- Typical values are $L = 1-8\text{nH}$ and $Q = 3-6$ at 2GHz

Inductor Modeling

Model:



$$L \approx \frac{37.5\mu_0 N^2 a^2}{11D-14a}$$

$$C_{ox} = W \cdot L \cdot \frac{\epsilon_{ox}}{t_{ox}}$$

$$R_s \approx \frac{L}{W\sigma\delta(1-e^{-t/\delta})}$$

$$R_1 \approx \frac{WLC_{sub}}{2}$$

$$C_p = NW^2 L \cdot \frac{\epsilon_{ox}}{t_{ox}}$$

$$C_1 \approx \frac{2}{WLC_{sub}}$$

where

$$\mu_0 = 4\pi \times 10^{-7} \text{ H/m} \text{ (vacuum permeability)}$$

σ = conductivity of the metal

a = distance from the center of the inductor to the middle of the windings

L = total length of the spiral

t = thickness of the metal

δ = skin depth given by $\delta = \sqrt{2/W\mu_0\sigma}$

$G_{sub}(C_{sub})$ is a process-dependent parameter

Inductor Modeling – Continued

Definition of the previous components:

R_s is the low frequency resistive loss of a metal and the skin effect

C_p arises from the overlap of the cross-under with the rest of the spiral. The lateral capacitance from turn-to-turn is also included.

C_{ox} is the capacitance between the spiral and the substrate

R_1 is the substrate loss due to eddy currents

C_1 is capacitance of the substrate

Design specifications:

L = desired inductance value

Q = quality factor

f_{SR} = self-resonant frequency. The resonant frequency of the LC tank represents the upper useful frequency limit of the inductor. Inductor operation frequency should be lower than f_{SR} , $f < f_{SR}$.

ASITIC: A software tool for analysis and simulation of CMOS spiral inductors and transformers.

<http://formosa.eecs.berkeley.edu/~niknejad/asitic.html>

Guidelines for Designing CMOS Sprial Inductors[†]

D – Outer diameter:

- As D increases, Q increases but the self-resonant frequency decreases
- A good design generally has $D < 200\mu\text{m}$

W – Metal width:

- Metal width should be as wide as possible
- As W increases, Q increases and R_s decreases
- However, as W becomes large, the skin effects are more significant, increasing R_s
- A good value of W is $10\mu\text{m} < W < 20\mu\text{m}$

S – Spacing between turns:

- The spacing should be as small as possible
- As S and L increase, the mutual inductance, M , decreases
- Use minimum metal spacing allowed in the technology but make sure the inter-winding capacitance between turns is not significant

N – Number of turns:

- Use a value that gives a layout convenient to work with other parts of the circuit

[†] Jaime Aguilera, et. al., "A Guide for On-Chip Inductor Design in a Conventional CMOS Process for RF Applications," *Applied Microwave & Wireless*, pp. 56-65, Oct. 2001.

Design Example

A 2GHz LC tank is to be designed as a part of LC oscillator. The C value is given as 3pF.

(a) Find value of L . (b) Design a spiral inductor with L value ($\pm 5\%$ range) from (a) using ASITIC. Optimize design parameters, W , S , D and N to get a high Q ($Q_{min} = 5$). Show L , Q , f_{SR} value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model.

Solution

(a) LC tank oscillation frequency is given as 2GHz.

$$\omega_{osc} = \frac{1}{\sqrt{LC}}, L = \frac{1}{\omega_{osc}^2 \cdot C} = \frac{1}{(2\pi \cdot 2 \times 10^9)^2 \cdot (3 \times 10^{-12})} = 2.11 \times 10^{-9}$$

$\therefore L = 2.11\text{nH}$ is desired.

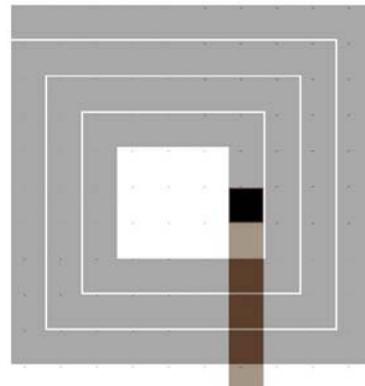
(b) $L = 2.11\text{nH} (\pm 5\%)$ is used as input parameter. Several design parameters are tried to get high Q and f_{SR} values. Final design has

- Parameters: $W = 19\text{um}$, $S = 1\text{um}$, $D = 200\text{um}$, $N = 3.5$
- Resulting inductor: $L = 2.06\text{nH}$, $Q = 7.11$, $f_{SR} = 9.99\text{GHz}$ @ 2GHz

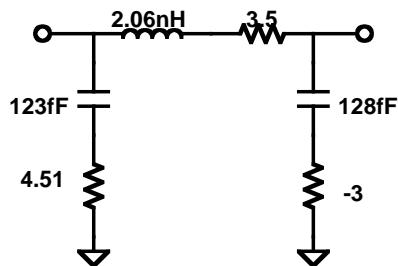
This design is acceptable as $Q > Q_{min}$ and $f < f_{SR}$.

Design Example-Continued

(c.) ASITIC generates a layout automatically. It can be saved and imported to use in other tools such as Cadence, ADS and Sonnet.



(d) Analysis in ASITIC gives the following π model.



The π model is usually not symmetrical and this can be used for differential configuration where none of the two ports are ac-grounded.

Reduction of Capacitance to Ground

Comments concerning implementation:

- 1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
 - Should be patterned so flux goes through but electric field is grounded
 - Metal strips should be orthogonal to the spiral to avoid induced loop current
 - The resistance of the shield should be low to terminate the electric field
- 2.) Avoid contact resistance wherever possible to keep the series resistance low.
- 3.) Use the metal with the lowest resistance and farthest away from the substrate.
- 4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example →

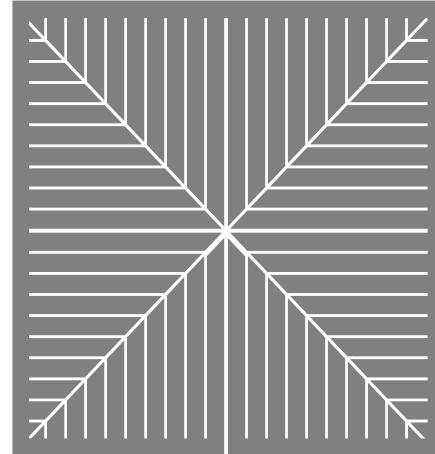
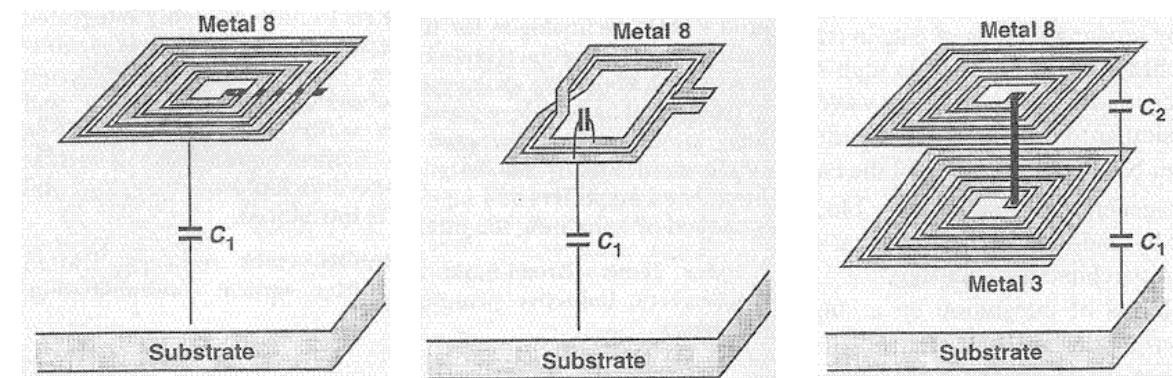


Fig. 2.5-12

Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately $4\mu\text{m}$ thick.

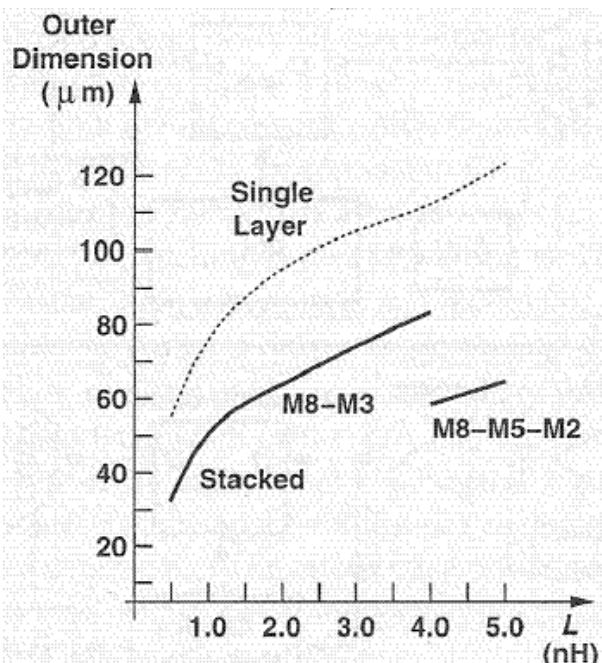
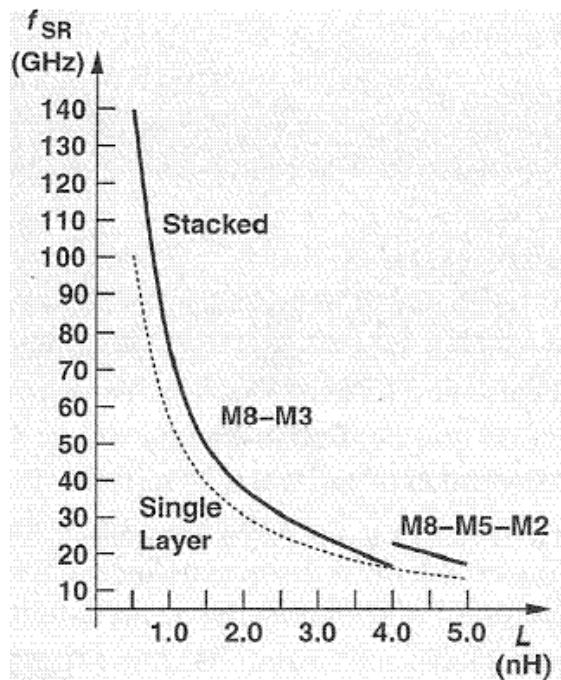


$Q = 5-6, f_{SR} = 30-40\text{GHz}$. $Q = 10-11, f_{SR} = 15-30\text{GHz}$ ¹. Good for high L in small area.

¹ The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.
CMOS Analog Circuit Design

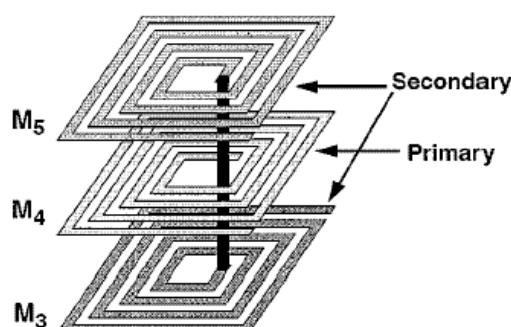
Inductors - Continued

Self-resonance as a function of inductance. Outer dimension of inductors.

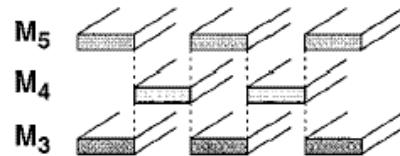


Transformers

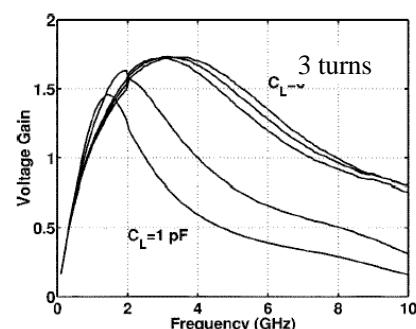
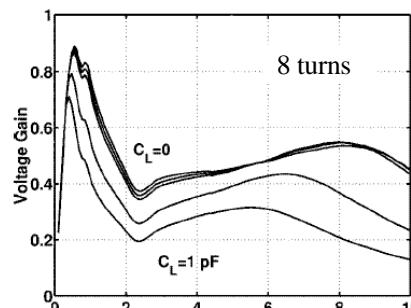
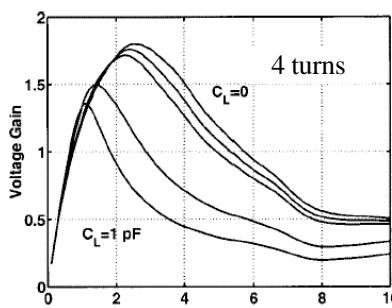
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.



Method of reducing the inter-winding capacitances.



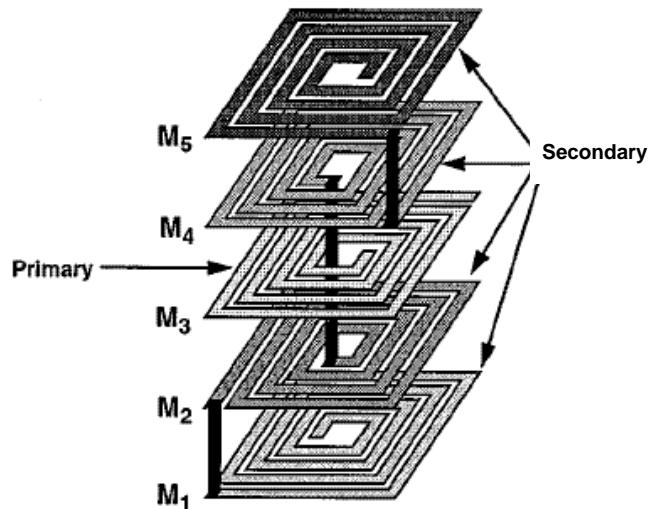
Measured 1:2 transformer voltage gains:



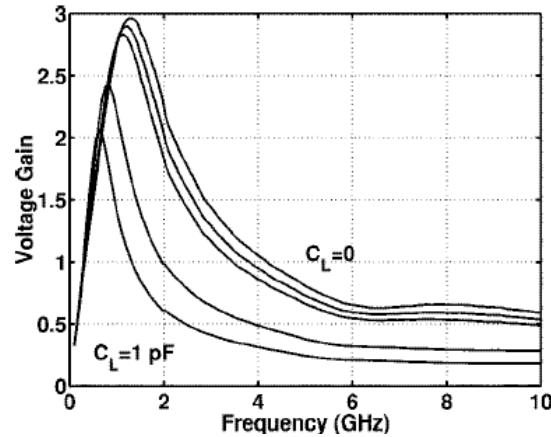
Transformers – Continued

A 1:4 transformer:

Structure-



Measured voltage gain-



($C_L = 0, 50\text{fF}, 100\text{fF}, 500\text{fF}$ and 1pF .
 C_L is the capacitive loading on the secondary.)

Summary of Inductors

Scaling? To reduce the size of the inductor would require increasing the flux density which is determined by the material the flux flows through. Since this material will not change much with scaling, the inductor size will remain constant.

Increase in the number of metal layers will offer more flexibility for inductor and transformer implementation.

Performance:

- Inductors
 - Limited to nanohenrys
 - Very low Q (3-5)
 - Not variable
- Transformers
 - Reasonably easy to build and work well using stacked inductors
- Matching
 - Not much data exists publicly – probably not good

SUMMARY

- Types of resistors include diffused, well, polysilicon and metal
- Resistors are characterized by:
 - Value
 - Linearity
 - Power
 - Parasitics
- Technology effects on resistors includes:
 - Process bias
 - Diffusion interaction
 - Thermoelectric effects
 - Piezoresistive effects
- Inductors are made by horizontal metal spirals, typically in top metal
- Inductors are characterized by:
 - Value
 - Losses
 - Self-resonant frequency
 - Parasitics
- RF transformers are reasonably easy to build and work well using stacked inductors

LECTURE 080 – LATCHUP AND ESD

LECTURE ORGANIZATION

Outline

- Latchup
- ESD
- Summary

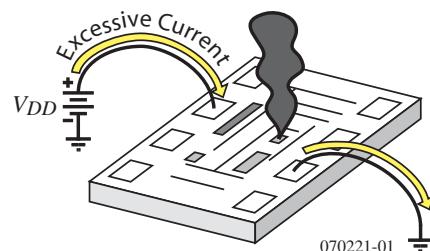
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 48-52 and new material

LATCHUP

What is Latchup?

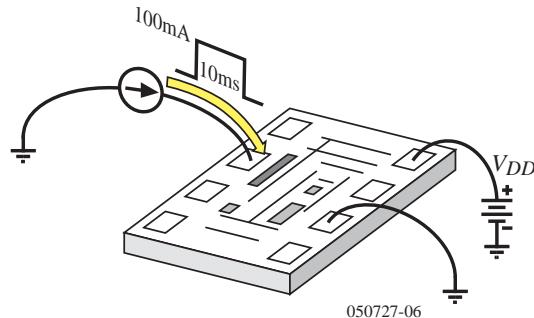
- Latchup is the creation of a low impedance path between the power supply rails.
- Latchup is caused by the triggering of parasitic bipolar structures within an integrated circuit when applying a current or voltage stimulus on an input, output, or I/O pin or by an over-voltage on the power supply pin.
- Temporary versus true latchup:
A temporary or transient latchup occurs only while the pulse stimulus is connected to the integrated circuit and returns to normal levels once the stimulus is removed.
A true latchup remains after the stimulus has been removed and requires a power supply shut down to remove the low impedance path between the power supply rails



Latchup Testing

The test for latchup defines how the designer must think about latchup.

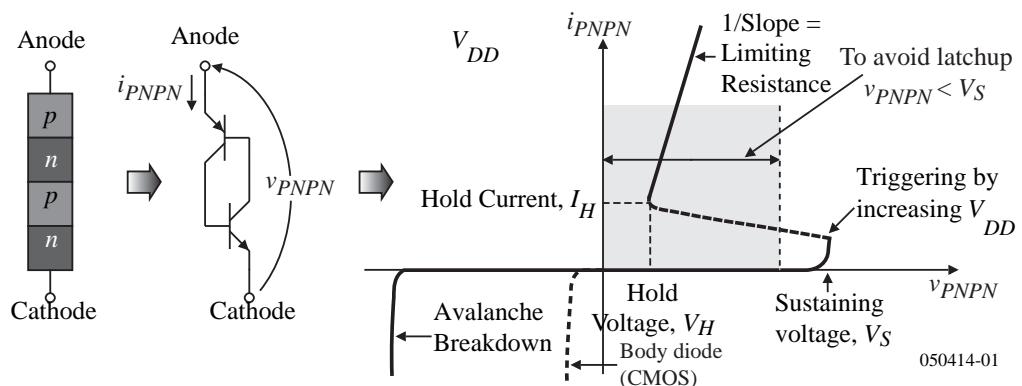
- For latchup prevention, you must consider where a current limited ($\geq 100\text{mA}$), 10ms pulse is going to go when applied to a pad when the voltage compliance of the pad is constrained to 50% above maximum power supply and to 2V below ground. (Higher temperatures, 85°C and 125°C , are more demanding, since V_{BE} is lower.)



- Latchup is sensitive to layout and is most often solved at the physical layout level.

How Does Latchup Occur?

Latchup is the regenerative process that can occur in a *pnpn* structure (SCR-silicon controlled rectifier) formed by a parasitic *npn* and a parasitic *pnp* transistor.



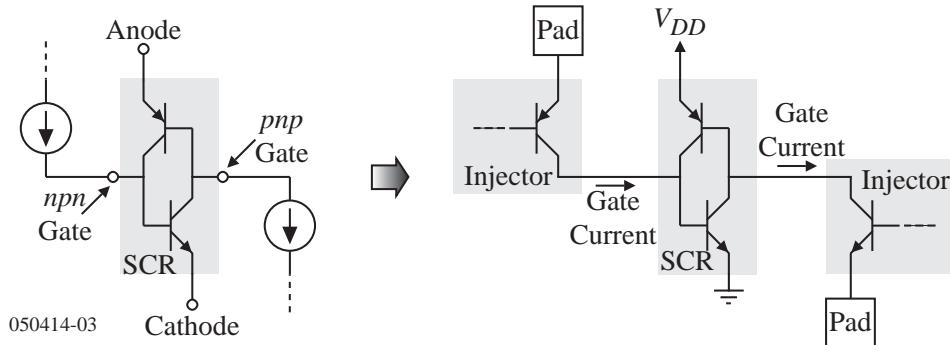
Important concepts:

- To avoid latchup, $v_{PNPN} \leq V_S$
- Once the *pnpn* structure has latched up, the large current required by the above $i-v$ characteristics must be provided externally to sustain latchup
- To remove latchup, the current must be reduced below the holding current

Latchup Triggering

Latchup of the SCR can be triggered by two different mechanisms.

- 1.) Allowing v_{PNPN} to exceed the sustaining voltage, V_S .
- 2.) Injection of current by a triggering device (gate triggered)



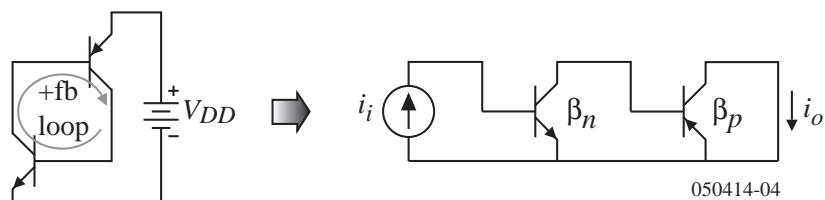
Note: The gates mentioned above are SCR junction gates, not MOSFET gates.

From the above considerations, latchup requires the following components:

- 1.) A four-layer structure (SCR) connected between V_{DD} and ground.
- 2.) An injector.
- 3.) A stimulus.

Necessary Conditions for Latchup

- 1.) The loop gain of the relevant BJT configuration must exceed unity.



Loop gain:

$$\frac{i_o}{i_i} \approx \beta_p \beta_n$$

- 2.) A bias condition must exist such that both bipolars are turned on long enough for current through the “SCR” to exceed its switching current.
- 3.) The bias supply and associated circuits must be capable of supplying the current at least equal to the switching current and at least equal to the holding current to maintain the latched state.

Latchup Trigger Modes

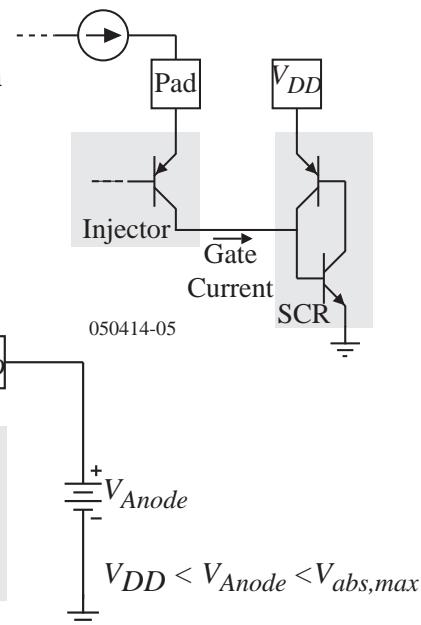
Current mode (Positive Injection Example):

When a current is applied to a pad, it can flow through an injector and trigger latchup of an SCR formed from parasitic bipolar transistors.

SCR gate current injection parasitic can occur in *p*-well or *n*-well technology.

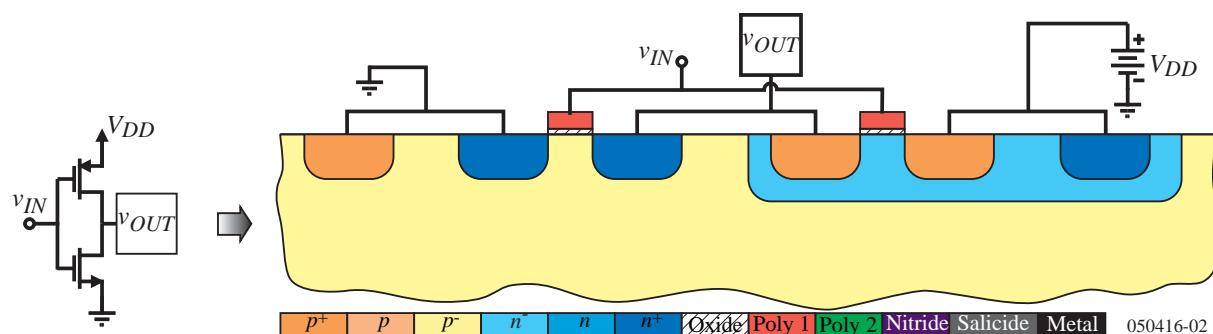
Voltage mode:

When the power supply is increased above the nominal value, the SCR formed from parasitic bipolar transistors can be triggered.



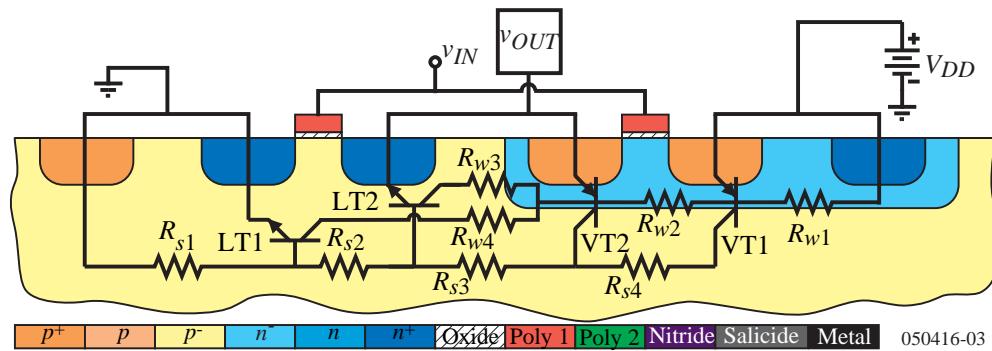
How does Latchup Occur in an IC?

Consider an output driver in CMOS technology:



Assume that the output is connected to a pad.

Parasitic Bipolar Transistors for the n-well CMOS Inverter



Parasitic components:

Lateral BJTs LT1 and LT2

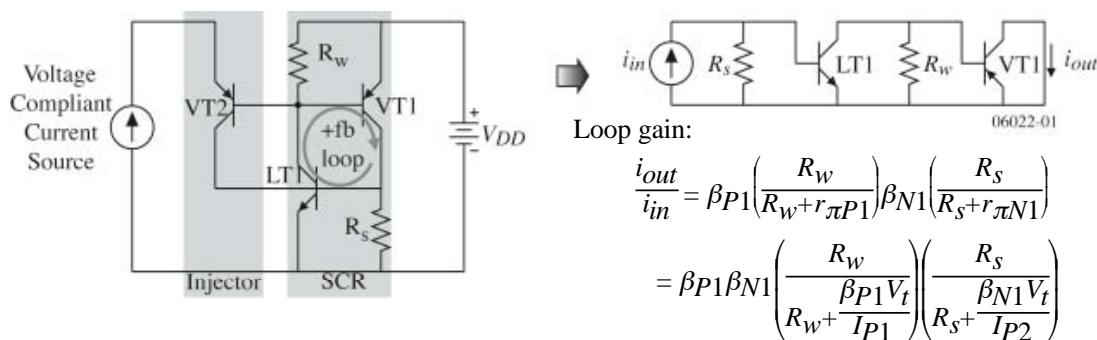
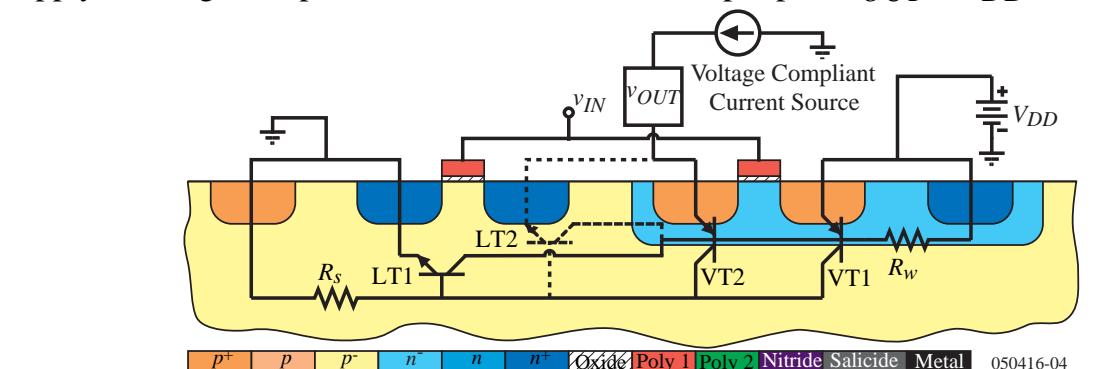
Vertical BJTs VT1 and VT2

Bulk substrate resistances R_{s1}, R_{s2}, R_{s3} , and R_{s4}

Bulk well resistances R_{w1}, R_{w2}, R_{w3} , and R_{w4}

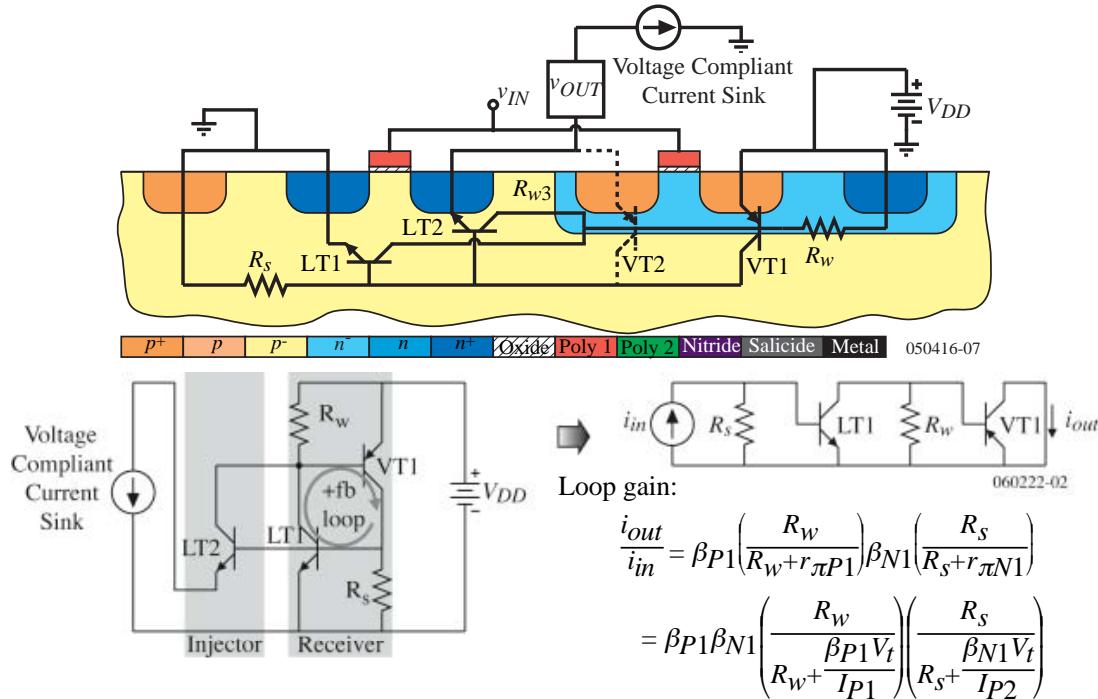
Current Source Injection

Apply a voltage compliant current source to the output pad ($v_{OUT} > V_{DD}$).



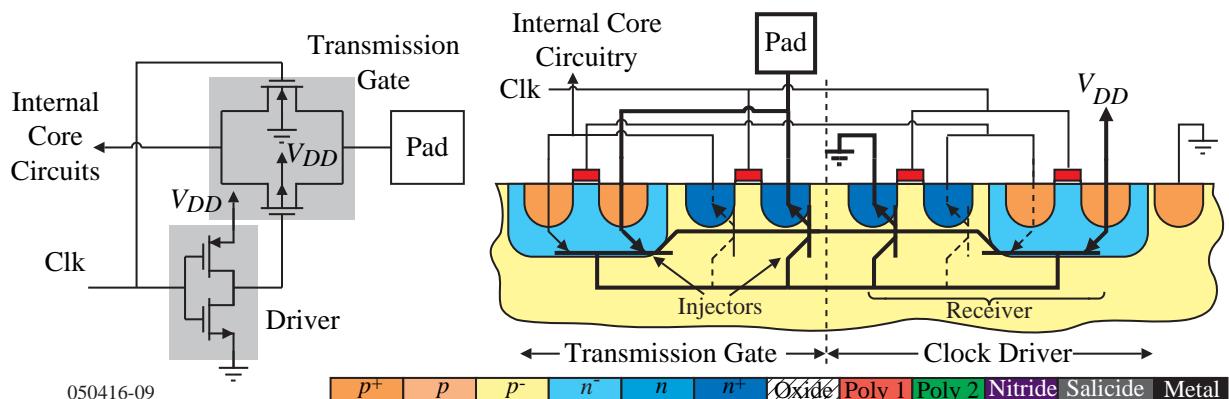
Current Sink Injection

Apply a voltage compliant current sink to the output pad ($v_{OUT} < 0$).



Latchup from a Transmission Gate

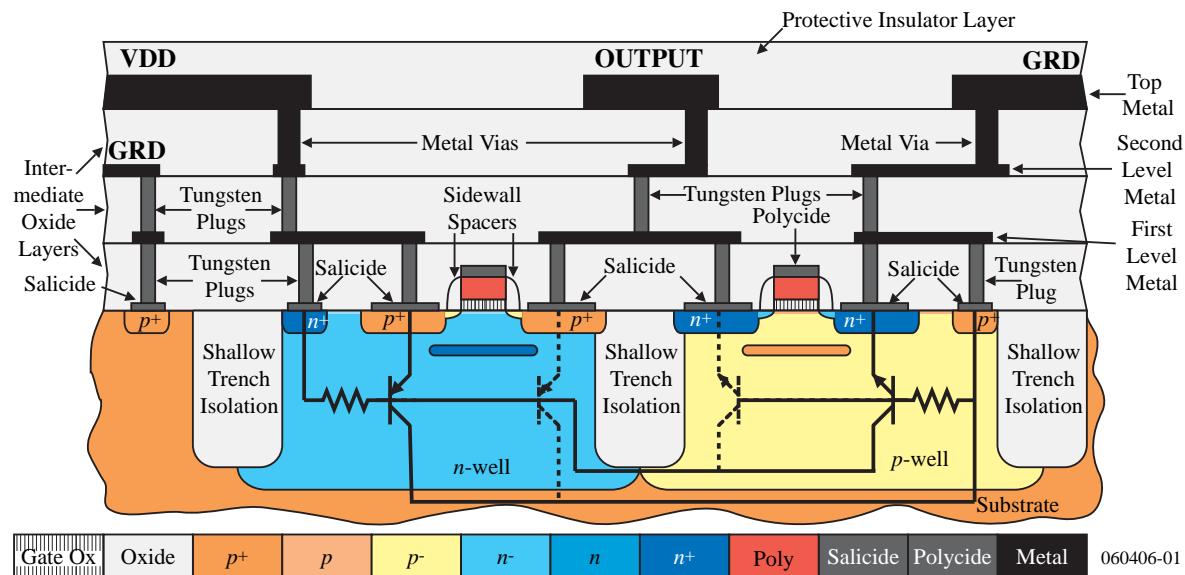
The classical push-pull output stage is only one of the many configurations that can lead to latchup. Here is another configuration:



The two bold solid bipolar transistors in the transmission gate act as injectors to the $npn-pnp$ parasitic bipolars of the clock driver and cause these transistors to latchup. The injector sites are the diffusions connected to the pad.

The Influence of Shallow Trench Isolation on Latchup

As seen below, the STI causes the parasitic betas to be smaller.



Preventing Latch-Up

- 1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.
- 2.) Reduce the values of R_{N^-} and R_{P^-} . This requires more current before latch-up can occur.
- 3.) Surround the transistors with guard rings. Guard rings reduce transistor betas and divert collector current from the base of SCR transistors.

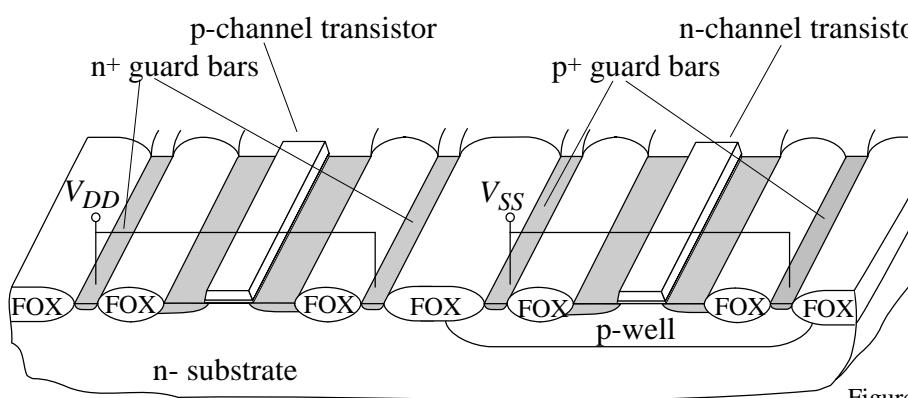
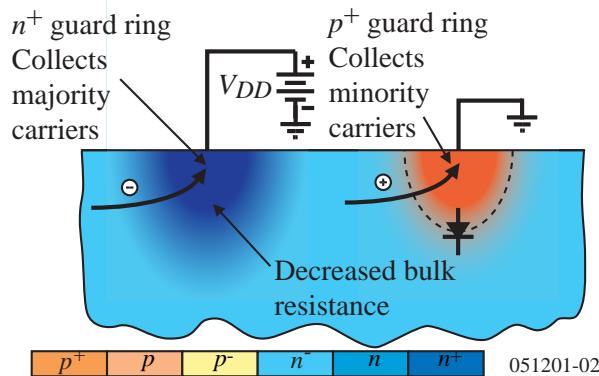


Figure 190-10

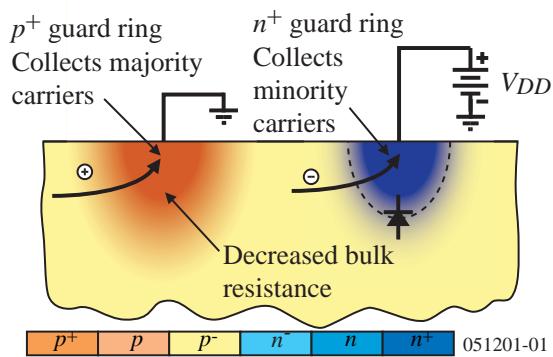
What are Guard Rings?

Guard rings are used to collect carriers flowing in the silicon. They can be designed to collect either majority or minority carriers.

Guard rings in n -material:



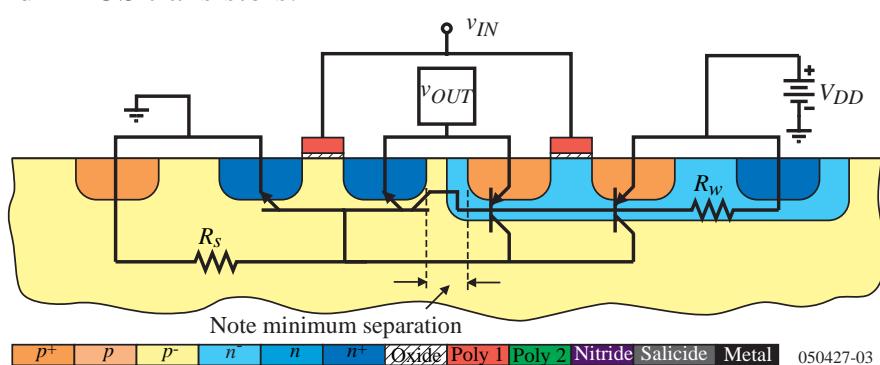
Guard rings in p -material:



Also, the increased doping level of the n^+ (p^+) guard ring in n (p) material decreases the resistance in the area of the guard ring.

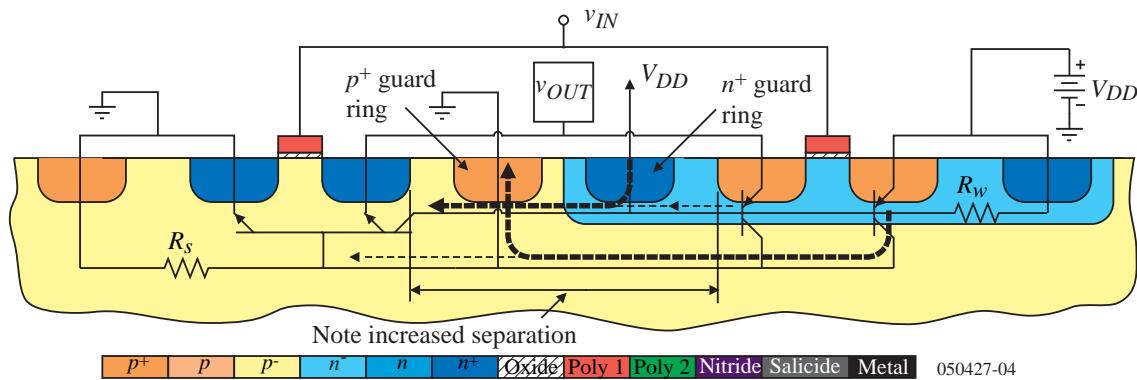
Example of Reducing the Sensitivity to Latchup

Start with an inverter with no attempt to minimize latchup and minimum spacing between the NMOS and PMOS transistors.



Example of Reducing the Sensitivity to Latchup by using Guard Rings

Next, place guard rings around the NMOS and PMOS transistors (both I/O and logic) to collect most of the parasitic NPN and PNP currents locally and prevent turn-on of adjacent devices.

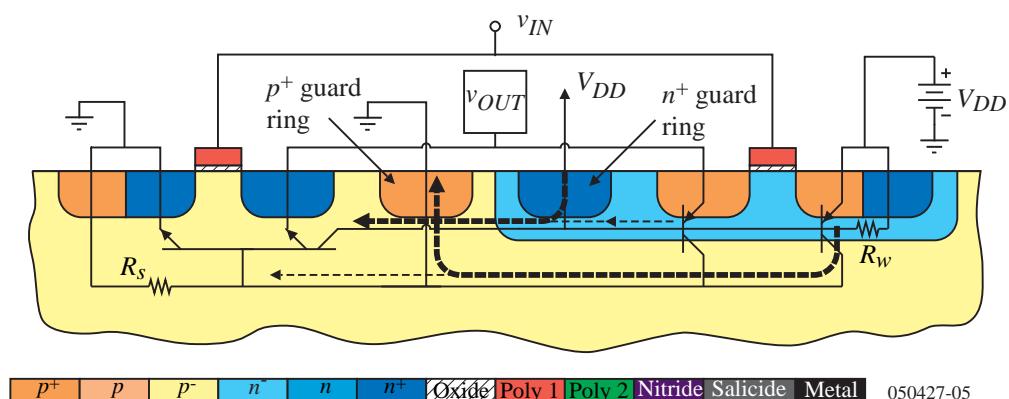


- The guard rings also help to reduce the effective well and substrate resistance.
- The guard rings reduce the lateral beta

Key: The guard rings should act like collectors

Example of Reducing the Sensitivity to Latchup by using Butted Contacts

Finally, use butted source contacts to further reduce the well resistance and reduce the substrate resistance.



Guidelines for Guard Rings

- Guard rings should be low resistance paths.
- Guard rings should utilize continuous diffusion areas.
- More than one transistor of the same type can be placed inside the same well inside the same guard ring as long as the design rules for spacing are followed.
- Only 2 guard rings are required between adjacent PMOS and NMOS transistors
- The well taps and/or the guard ring should be laid out as close to the MOSFET source as possible.
- I/O output NMOSFET should use butted composite for source to bulk connections when the source is electrically connected to the *p*-well tap. If separate well tap and source connections are required due to substrate noise injection problems, minimize the source-well tap spacing. This will minimize latch up and early snapback of the output MOSFETs with the drain diffusion tied directly (in metal) to the bond pad.

ESD IN CMOS TECHNOLOGY

What is Electrostatic Discharge?

Triboelectric charging happens when 2 materials come in contact and then are separated.

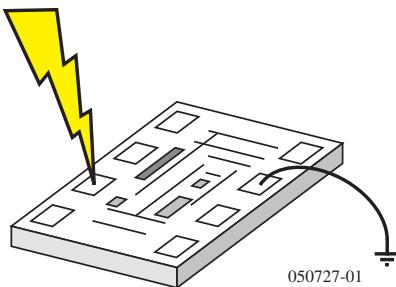


An ESD event occurs when the stored charge is discharged.



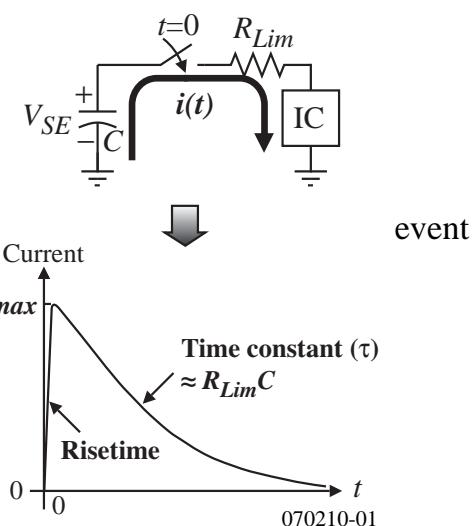
ESD and Integrated Circuits

- ICs consist of components that are very sensitive to excess current and voltage above the nominal power supply.
- Any path to the outside world is susceptible to ESD
- ESD damage can occur at any point in the IC assembly and packaging, the packaged part handling or the system assembly process.
- Note that power is normally not on during an ESD event



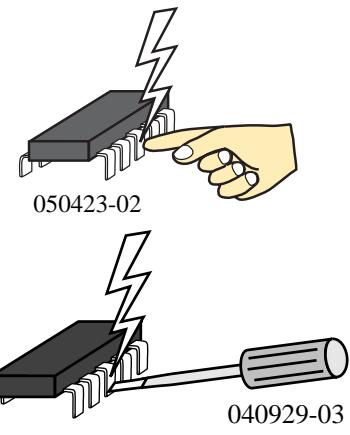
ESD Models and Standards

- Standard tests give an indication of the ICs robustness to withstand ESD stress.
- Increased robustness:
 - Reduces field failures due to ESD
 - Demanded by customers
- Simple ESD model:
 - V_{SE} = Charging Voltage
 - Key parameters of the model:
 - o Maximum current flow
 - o Time constant or how fast the ESD discharges
 - o Risetime of the pulse

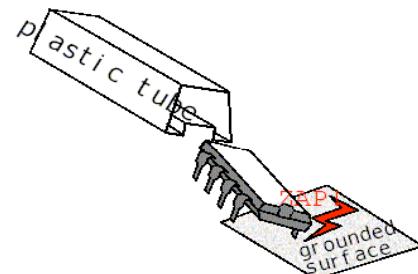


ESD Models

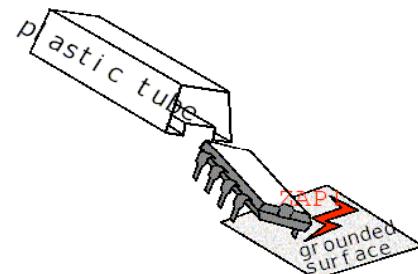
- Human body model (HBM): Representative of an ESD event between a human and an electronic component.



- Machine model (MM): Simulates the ESD event when a charged “machine” discharges through a component.



- Charge device model (CDM): Simulates the ESD event when the component is charged and then discharges through a pin. The substrate of the chip becomes charged and discharges through a pin.



ESD Influence on Components

An ESD event typically creates very high values of current (1-10A) for very short periods of time (150 ns) with very rapid rise times (1ns).

Therefore, components experience extremely high values of current with very little power dissipation or thermal effects.

Resistors – become nonlinear at high currents and will breakdown

Capacitors – become shorts and can breakdown from overvoltage (pad to substrate)

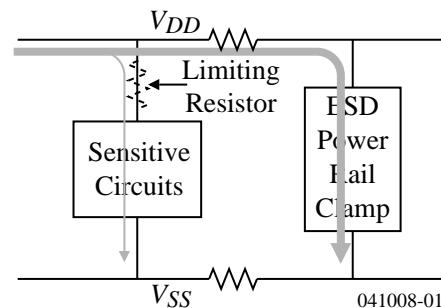
Diodes – current no longer flows uniformly (the connections to the diodes represent the ohmic resistance limit)

Transistors – ESD event is only a two terminal event, the third terminal is influenced by parasitics and many of the transistor parameters are poorly controlled.

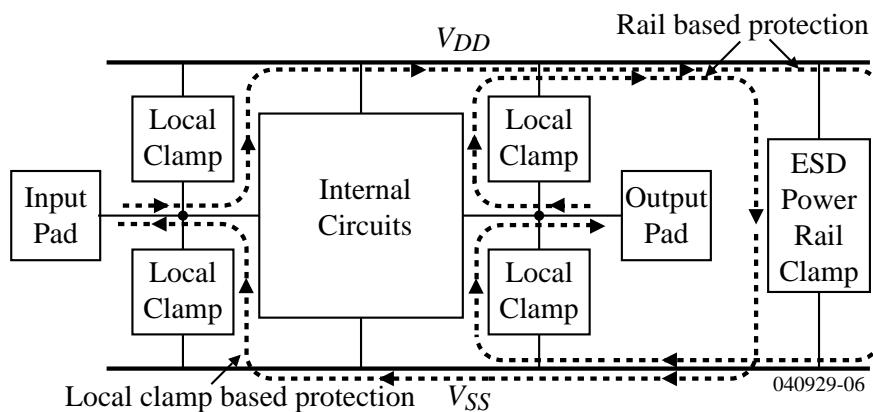
- MOSFETs – the parasitic bipolar experiences snapback under an ESD event
- BJTs – will experience snapback under ESD event

Objective of ESD Protection

- There must be a safe low impedance path between every combination of pins to sink the ESD current (i.e. 1.5A for 2kV HBM)
- The ESD device should clamp the voltage below the breakdown voltage of the internal circuitry
- The metal busses must be designed to survive 1.5A (fast transient) without building up excessive voltage drop
- ESD current must be steered away from sensitive circuits
- ESD protection will require area on the chip (busses and timing components)



ESD Protection Architecture



Local clamps – Conducts ESD current without loading the internal (core) circuits

ESD power rail clamps – Conducts a large amount of current with a small voltage drop

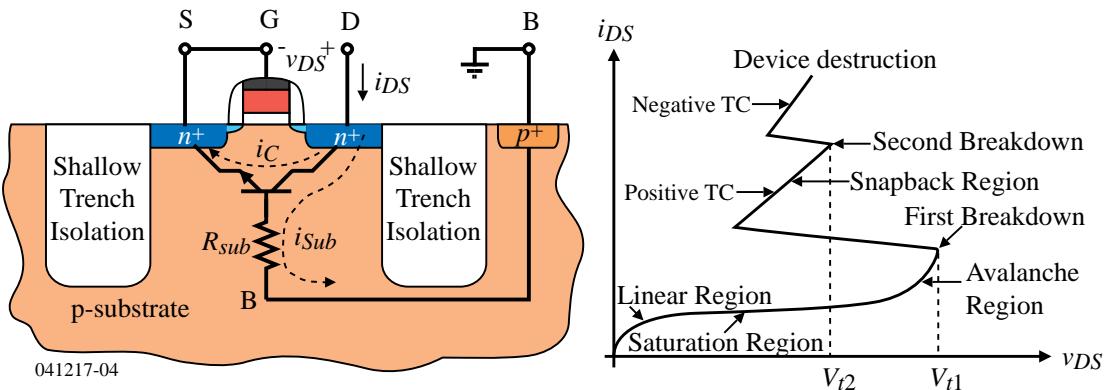
ESD Events:

Pad-to-rail (uses local clamps only)

Pad-to-pad (uses either local or local and ESD power rail clamps)

Example of an ESD Breakdown Clamp

A normal MOSFET that uses the parasitic lateral BJT to achieve a snapback clamp. Normally, the MOSFET has the gate shorted to the source so that drain current is zero.

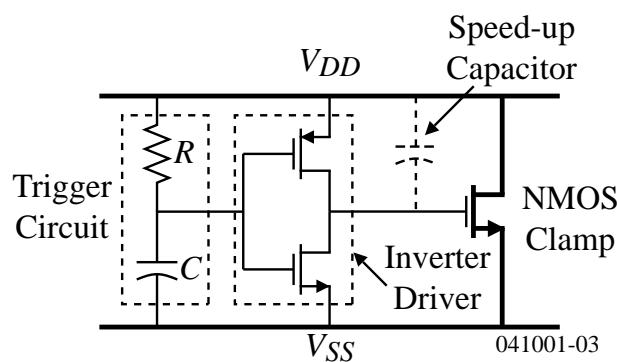


Issues:

- If the drain voltage becomes too large, the gate oxide may breakdown
- If the transistor has multiple fingers, the layout should ensure that the current is distributed evenly.

Example of a Non-Breakdown Clamp

NMOS Clamp:



Operation:

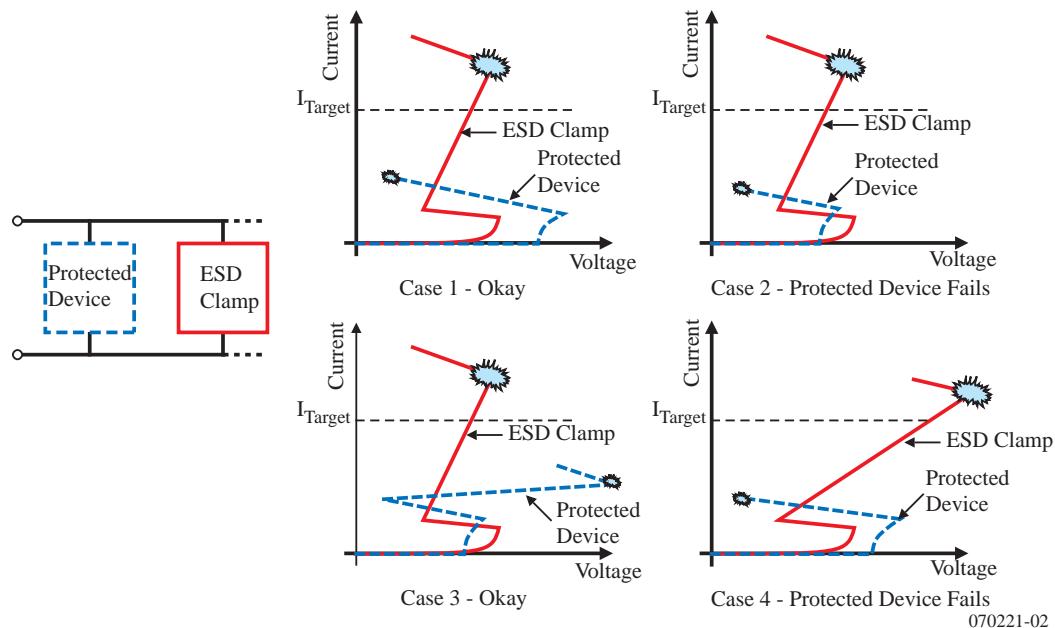
- Normally, the input to the trigger circuit is low, the output low and the NMOS clamp off
- For a positive ESD event, the voltage increases across R causing the inverter to turn on the NMOS clamp providing a low impedance path between the rails
- Cannot be used for pads that go above power supply or are active when powered up
- For power supply turn-on, the circuit should not trigger (C holds the clamp off during turn-on)

the driver is

Also, forward biased diodes serve as non-breakdown clamps.

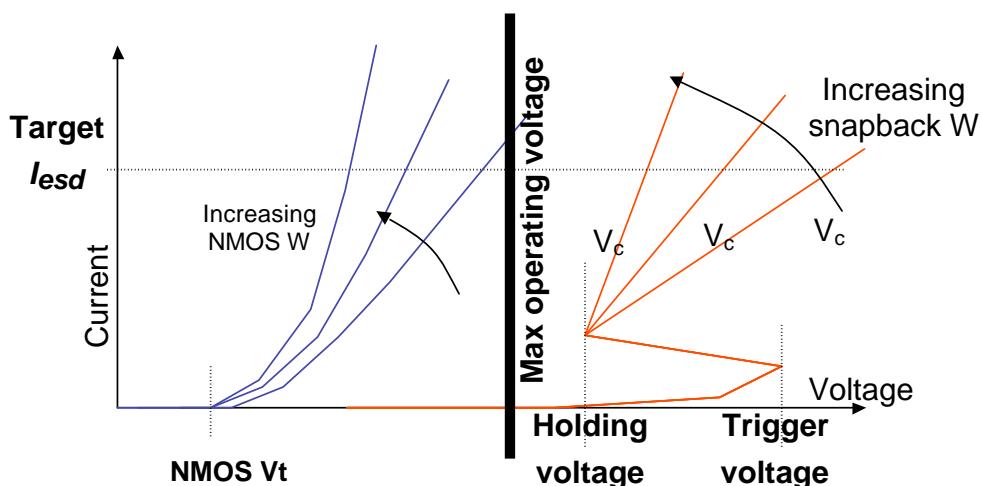
IV Characteristics of Good ESD Protection

Goal: Sink the ESD current and clamp the voltage.



Comparison Between the NMOS Clamp and the Snapback Clamp

Increasing the width of the NMOS clamp will reduce the clamp voltage.



Note that the NMOS clamp does not normally exceed the absolute maximum voltage. NMOS clamps should be used with EPROMs to avoid reprogramming during an ESD event.

ESD Practice

General Guidelines:

- Understand the current flow requirements for an ESD event
- Make sure the current flows where desired and is uniformly distributed
- Series resistance is used to limit the current in the protected devices
- Minimize the resistance in protecting devices
- Use distributed (smaller) active clamps to minimize the effect of bus resistance
- Understand the influence of packaging on ESD
- Use guard rings to prevent latchup

Check list:

- Check the ESD path between every pair of pads
- Check for ESD protection between the pad and internal circuitry
- Check for low bus resistance
 - Current: Minimum metal for ESD $\approx 40 \times$ Electromigration limit
 - Voltage: 1.5A in a metal bus of $0.03\Omega/\text{square}$ of $1000\mu\text{m}$ long and $30\mu\text{m}$ wide gives a voltage drop of 1.5V
- Check for sufficient contacts and vias in the ESD path (uniform current distribution)

SUMMARY

- Latchup is the creation of a low impedance path between the power supply rails resulting in excessive current.
- The conditions for latchup are:
 - A four-layer, *pnpn* structure connected between power supply rails
 - An injector (any diffusion connected to a pad)
 - A stimulus
- Latchup is prevented by:
 - Keeping the NMOS and PMOS transistors separated
 - Reducing the well resistance with appropriate well ties
 - Surrounding the transistors with guard rings
- ESD is caused by triboelectric charging which discharges through the IC when the power is off
- The current produced by an ESD event must be controlled – uniform current flow, minimum voltage drop, and must not flow through sensitive circuitry
- An ESD event turns on very quickly (<1ns), has a high peak current (1A), and lasts for approximately 100 ns.
- ESD clamps consist of breakdown clamps (snapback) and non-breakdown clamps.

LECTURE 090 – LARGE SIGNAL MOSFET MODEL

LECTURE ORGANIZATION

Outline

- Introduction to modeling
- Operation of the MOS transistor
- Simple large signal model (SAH model)
- Subthreshold model
- Short channel, strong inversion model
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 73-78 and 97-99

INTRODUCTION TO MODELING

Models Suitable for Understanding Analog Design

The model required for analog design with CMOS technology is one that leads to understanding and insight as distinguished from accuracy.

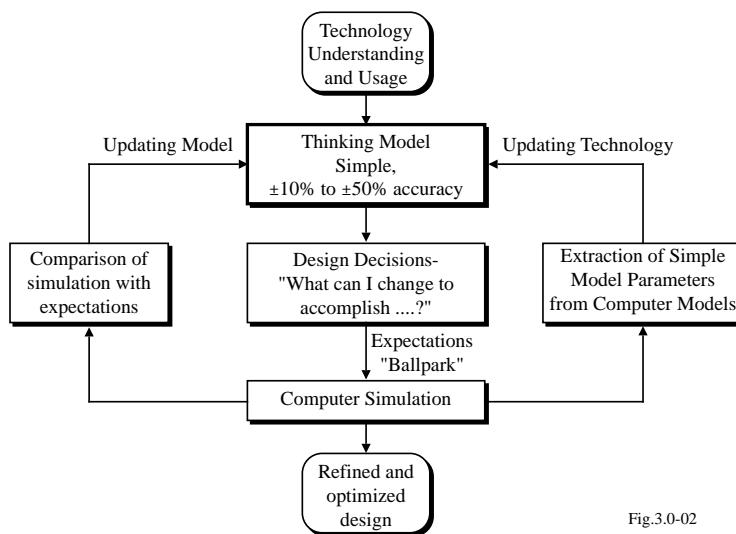


Fig.3.0-02

This lecture is devoted to the simple model suitable for design *not* using simulation.

Categorization of Electrical Models

		Time Dependence	
		Time Independent	Time Dependent
Linearity	Linear	Small-signal, midband R_{in}, A_v, R_{out} (.TF)	Small-signal frequency response- poles and zeros (.AC)
	Nonlinear	DC operating point $i_D = f(v_D, v_G, v_S, v_B)$ (.OP)	Large-signal transient response - Slew rate (.TRAN)

Based on the simulation capabilities of SPICE.

OPERATION OF THE MOS TRANSISTOR

Formation of the Channel for an Enhancement MOS Transistor

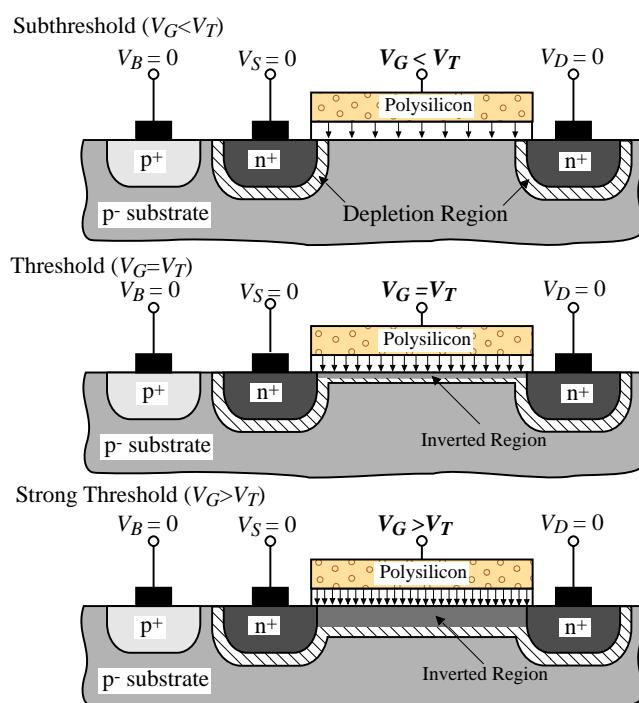


Fig.3.1-02

Transconductance Characteristics of an Enhancement NMOSFET when $V_{DS} = 0.1V$

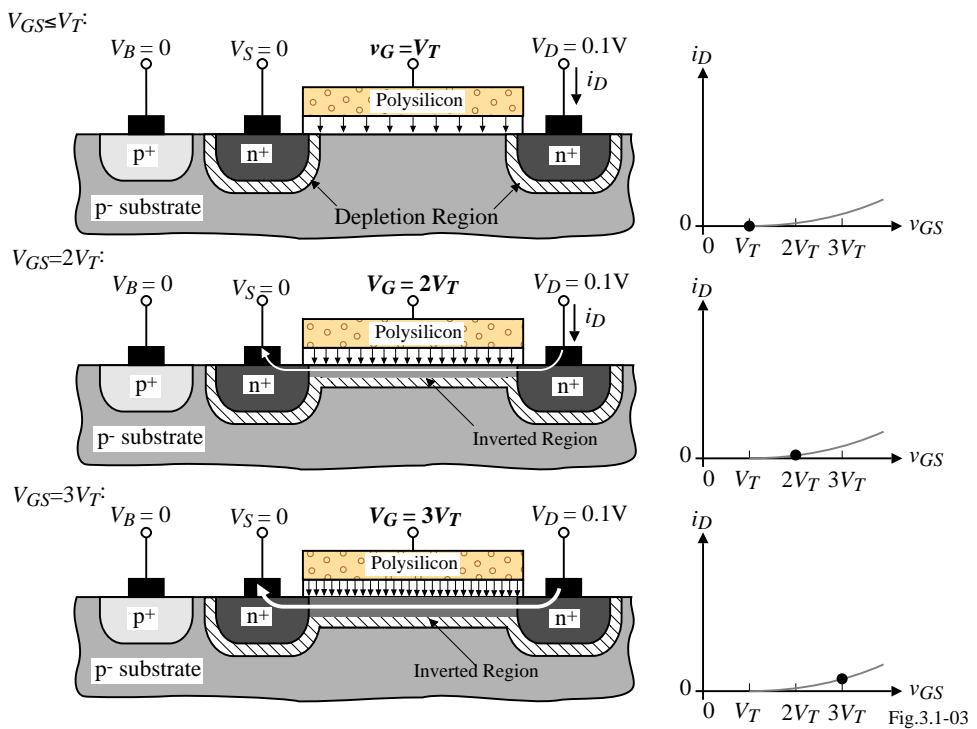


Fig.3.1-03

Output Characteristics of the Enhancement NMOS Transistor for $V_{GS} = 2V_T$

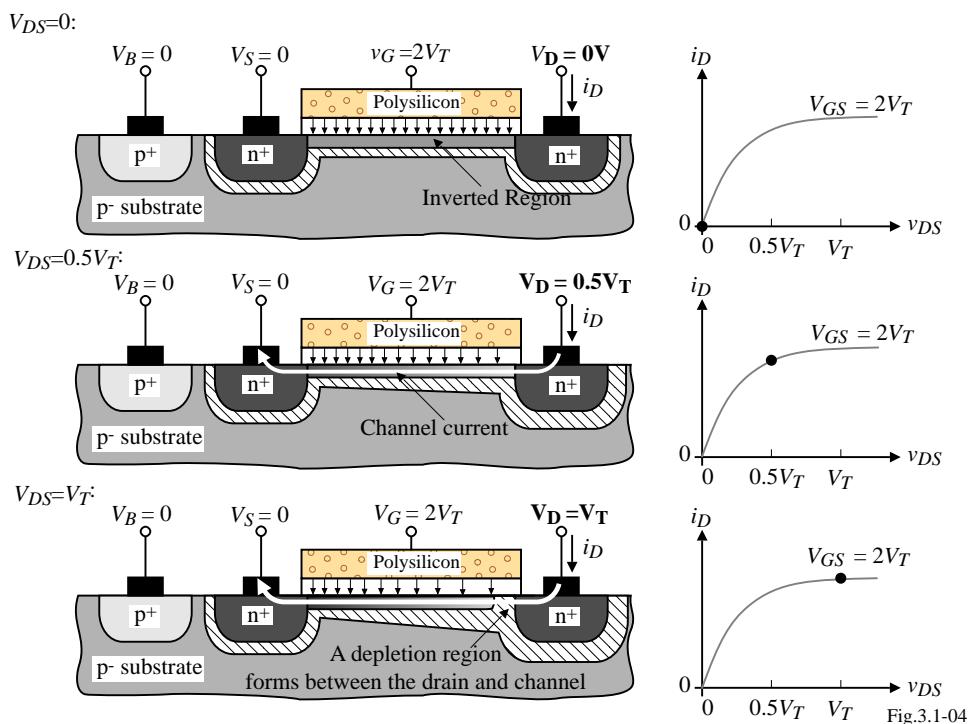


Fig.3.1-04

Output Characteristics of the Enhanced NMOS when $v_{DS} = 2V_T$

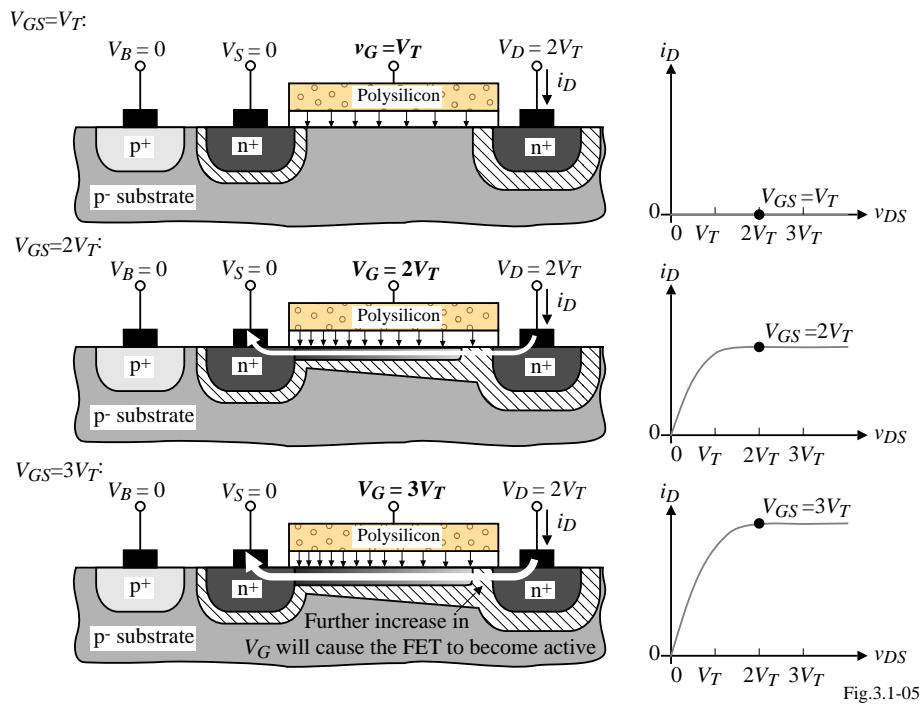


Fig.3.1-05

Output Characteristics of an Enhancement NMOS Transistor

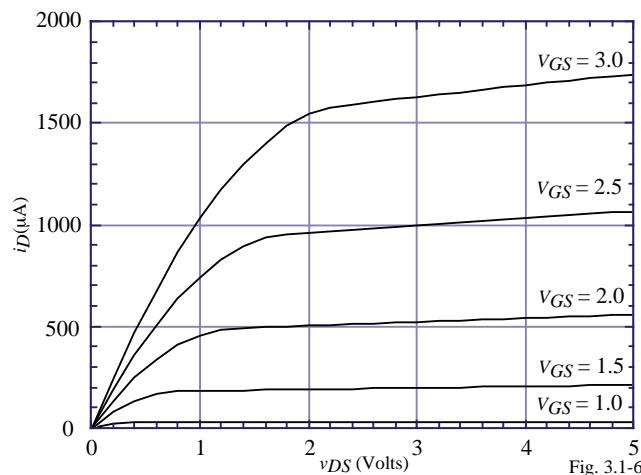


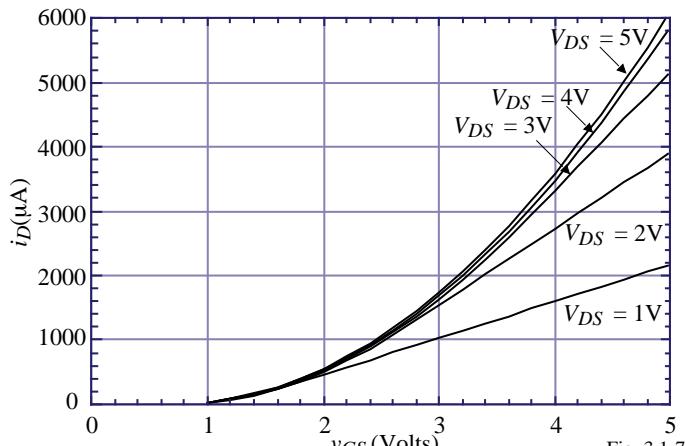
Fig. 3.1-6

SPICE Input File:

```
Output Characteristics for NMOS
M1 6 1 0 0 MOS1 w=5u l=1.0u
VGS1 1 0 1.0
M2 6 2 0 0 MOS1 w=5u l=1.0u
VGS2 2 0 1.5
M3 6 3 0 0 MOS1 w=5u l=1.0u
VGS3 3 0 2.0
M4 6 4 0 0 MOS1 w=5u l=1.0u
VGS4 4 0 2.5
```

```
M5 6 5 0 0 MOS1 w=5u l=1.0u
VGS5 5 0 3.0
VDS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 +lambda=.04 phi=.7)
.dc vds 0 .5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.end
```

Transconductance Characteristics of an Enhancement NMOS Transistor



SPICE Input File:

```

Transconductance Characteristics for NMOS
M1 1 6 0 0 MOS1 w=5u l=1.0u
VDS1 1 0 1.0
M2 2 6 0 0 MOS1 w=5u l=1.0u
VDS2 2 0 2.0
M3 3 6 0 0 MOS1 w=5u l=1.0u
VDS3 3 0 3.0
M4 4 6 0 0 MOS1 w=5u l=1.0u
VDS4 4 0 4.0
M5 5 6 0 0 MOS1 w=5u l=1.0u
VDS5 5 0 5.0
VGS 6 0 5
.model mos1 nmos (vto=0.7 kp=110u
+gamma=0.4 lambda=.04 phi=.7)
.dc vgs 0 5 .2
.print dc ID(M1), ID(M2), ID(M3), ID(M4),
ID(M5)
.probe
.end

```

SIMPLE LARGE SIGNAL MODEL (SAH MODEL)

Large Signal Model Derivation

- 1.) Let the charge per unit area in the channel inversion layer be

$$Q_l(y) = -C_{ox}[v_{GS} - v(y) - V_T] \text{ (coul./cm}^2\text{)}$$

- 2.) Define sheet conductivity of the inversion layer per square as

$$\sigma_S = \mu_o Q_l(y) \left(\frac{\text{cm}^2}{\text{v}\cdot\text{s}} \right) \left(\frac{\text{coulombs}}{\text{cm}^2} \right) = \frac{\text{amps}}{\text{volt}} = \frac{1}{\Omega/\text{sq.}}$$

- 3.) Ohm's Law for current in a sheet is

$$J_S = \frac{i_D}{W} = -\sigma_S E_y = -\sigma_S \frac{dv}{dy} \rightarrow dv = \frac{-i_D}{\sigma_S W} dy = \frac{-i_D dy}{\mu_o Q_l(y) W} \rightarrow i_D dy = -W \mu_o Q_l(y) dv$$

- 4.) Integrating along the channel for 0 to L gives

$$\int_0^L i_D dy = - \int_0^{v_{DS}} W \mu_o Q_l(y) dv = \int_0^{v_{DS}} W \mu_o C_{ox} [v_{GS} - v(y) - V_T] dv$$

- 5.) Evaluating the limits gives

$$i_D = \frac{W \mu_o C_{ox}}{L} \left[(v_{GS} - V_T) v_{DS} - \frac{v_{DS}^2}{2} \right]$$

Saturation Voltage - $V_{DS}(\text{sat})$

Interpretation of the large signal model:

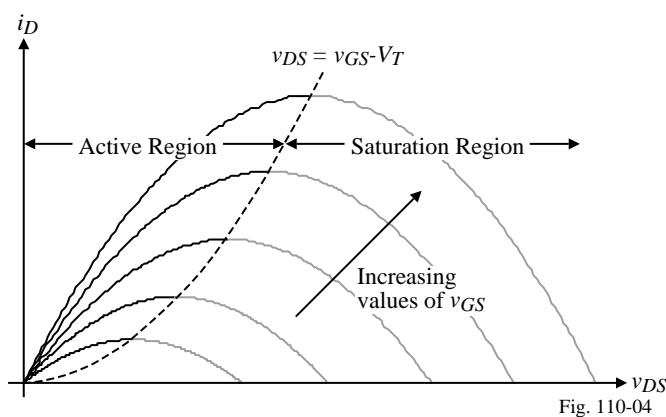


Fig. 110-04

The saturation voltage for MOSFETs is the value of drain-source voltage at the peak of the inverted parabolas.

$$\frac{di_D}{dv_{DS}} = \frac{\mu_o C_{ox} W}{L} [(v_{GS} - V_T) - v_{DS}] = 0$$

$$v_{DS}(\text{sat}) = v_{GS} - V_T$$

Useful definitions:

$$\frac{\mu_o C_{ox} W}{L} = \frac{K' W}{L} = \beta$$

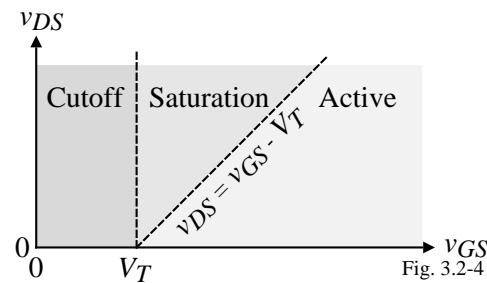


Fig. 3.2-4

The Simple Large Signal MOSFET Model

Regions of Operation of the MOS Transistor:

1.) Cutoff Region:

$$v_{GS} - V_T < 0$$

$$i_D = 0$$

(Ignores subthreshold currents)

2.) Active Region

$$0 < v_{DS} < v_{GS} - V_T$$

$$i_D = \frac{\mu_o C_{ox} W}{2L} [2(v_{GS} - V_T) - v_{DS}] v_{DS}$$

3.) Saturation Region

$$0 < v_{GS} - V_T < v_{DS}$$

$$i_D = \frac{\mu_o C_{ox} W}{2L} (v_{GS} - V_T)^2$$

Output Characteristics of the MOSFET:

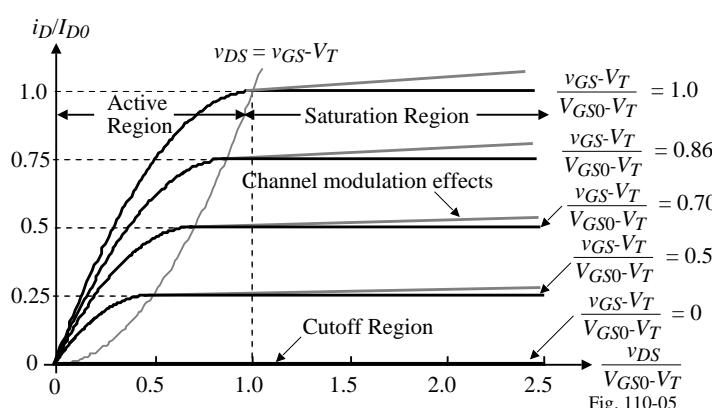
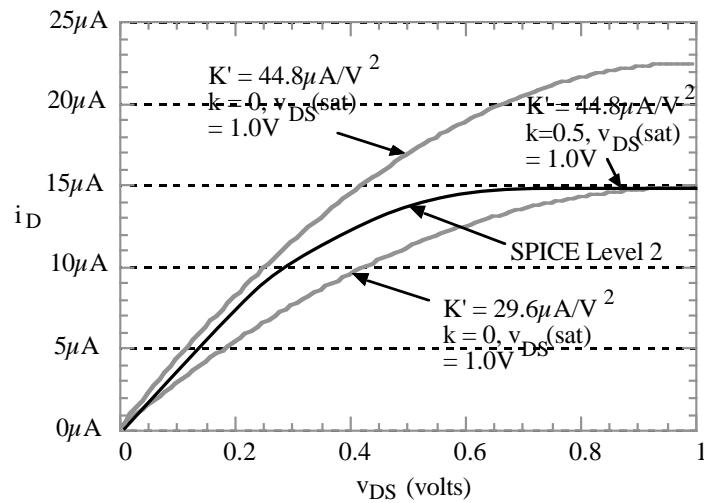


Fig. 110-05

Illustration of the Need to Account for the Influence of v_{DS} on the Simple Sah Model

Compare the Simple Sah model to SPICE level 2:



$V_{GS} = 2.0V$, $W/L = 100\mu m/100\mu m$, and no mobility effects.

Modification of the Previous Model to Include the Effects of v_{DS} on V_T

From the previous derivation:

$$\int_0^L i_D dy = - \int_0^{v_{DS}} W \mu_o Q_l(y) dv = \int_0^{v_{DS}} W \mu_o C_{ox} [v_{GS} - v(y) - V_T] dv$$

Assume that the threshold voltage varies across the channel in the following way:

$$V_T(y) = V_T + kv(y)$$

where V_T is the value of V_T at the source end of the channel and k is a constant.

Integrating the above gives,

$$i_D = \frac{W \mu_o C_{ox}}{L} \left[(v_{GS} - V_T)v(y) - (1+k) \frac{v^2(y)}{2} \right]_0^{v_{DS}}$$

or

$$i_D = \frac{W \mu_o C_{ox}}{L} \left[(v_{GS} - V_T)v_{DS} - (1+k) \frac{v^2_{DS}}{2} \right]$$

To find $v_{DS}(\text{sat})$, set the di_D/dv_{DS} equal to zero and solve for $v_{DS} = v_{DS}(\text{sat})$,

$$v_{DS}(\text{sat}) = \frac{v_{GS} - V_T}{1 + k}$$

Therefore, in the saturation region, the drain current is

$$i_D = \frac{W \mu_o C_{ox}}{2(1+k)L} (v_{GS} - V_T)^2$$

For $k = 0.5$ and $K' = 44.8 \mu A/V^2$, excellent correlation is achieved with SPICE 2

Influence of v_{DS} on the Output Characteristics

Channel modulation effect:

As the value of v_{DS} increases, the effective L decreases causing the current to increase.

Illustration:

Note that $L_{\text{eff}} = L - X_d$

Therefore the model in saturation becomes,

$$i_D = \frac{K'W}{2L_{\text{eff}}} (v_{GS} - V_T)^2 \rightarrow \frac{di_D}{dv_{DS}} = -\frac{K'W}{2L_{\text{eff}}^2} (v_{GS} - V_T)^2 \frac{dL_{\text{eff}}}{dv_{DS}} = \frac{i_D}{L_{\text{eff}}} \frac{dX_d}{dv_{DS}} = \lambda i_D$$

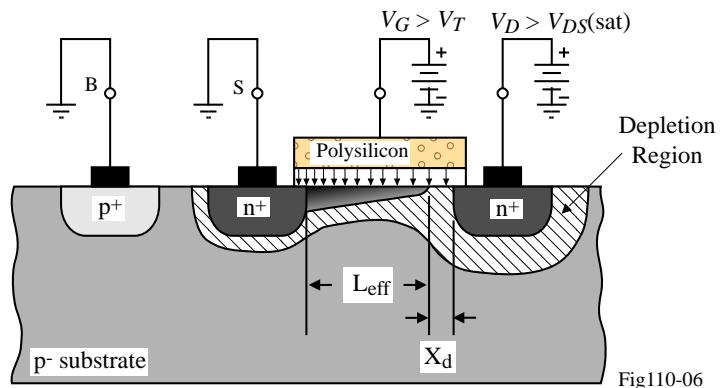


Fig110-06

Therefore, a good approximation to the influence of v_{DS} on i_D is

$$i_D \approx i_D(\lambda = 0) + \frac{di_D}{dv_{DS}} v_{DS} = i_D(\lambda = 0)(1 + \lambda v_{DS}) = \frac{K'W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

Channel Length Modulation Parameter, λ

Assume the MOS is transistor is saturated-

$$\therefore i_D = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

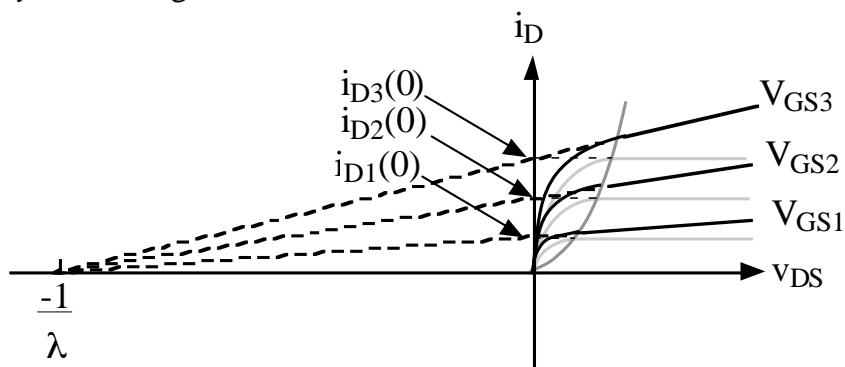
Define $i_D(0) = i_D$ when $v_{DS} = 0V$.

$$\therefore i_D(0) = \frac{\mu C_{ox} W}{2L} (v_{GS} - V_T)^2$$

Now,

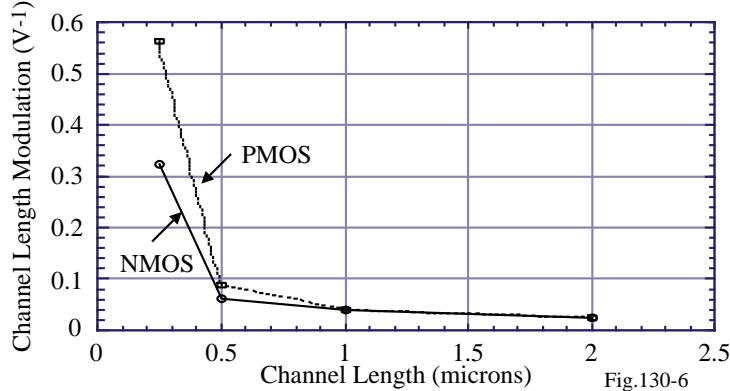
$$i_D = i_D(0)[1 + \lambda v_{DS}] = i_D(0) + \lambda i_D(0) v_{DS}$$

Matching with $y = mx + b$ gives the value of λ



Influence of Channel Length on λ

Note that the value of λ varies with channel length, L . The data below is from a $0.25\mu\text{m}$ CMOS technology.



Most analog designers stay away from minimum channel length to get better gains and matching at the sacrifice of speed.

Influence of the Bulk Voltage on the Large Signal MOSFET Model

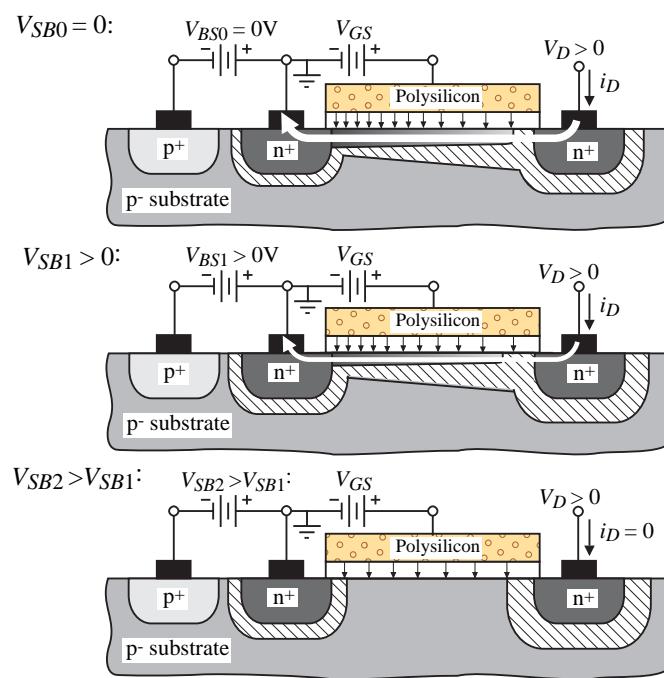
The components of the threshold voltage are:

- V_T = Gate-bulk work function (ϕ_{MS})
 - + voltage to change the surface potential ($-2\phi_F$)
 - + voltage to offset the channel-bulk depletion charge ($-Q_b/C_{ox}$)
 - + voltage to compensate the undesired interface charge ($-Q_{ss}/C_{ox}$)

We know that

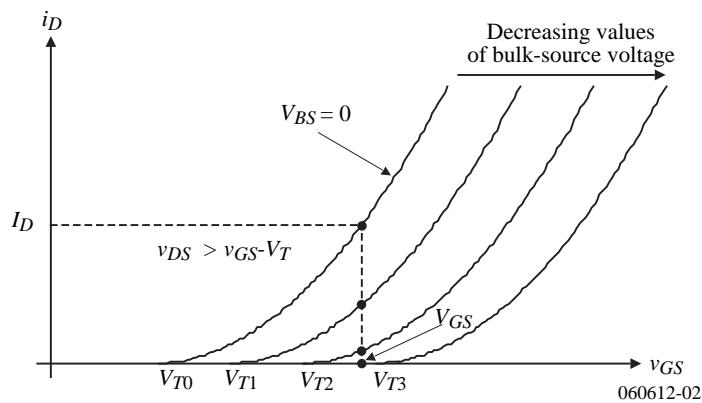
$$Q_b = \gamma \sqrt{|2\phi_F| + |v_{BS}|}$$

Therefore, as the bulk becomes more reverse biased with respect to the source, the threshold voltage must increase to offset the increased channel-bulk depletion charge.



Influence of the Bulk Voltage on the Large Signal MOSFET Model - Continued

Bulk-Source (v_{BS}) influence on the transconductance characteristics-



In general, the simple model incorporates the bulk effect into V_T by the previously developed relationship:

$$V_T(v_{BS}) = V_{T0} + \gamma \sqrt{2|\phi_f| + |v_{BS}|} - \gamma \sqrt{2|\phi_f|}$$

Summary of the Simple Large Signal MOSFET Model

N-channel reference convention:

Non-saturation-

$$i_D = \frac{W\mu_oC_{ox}}{L} \left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda v_{DS})$$

Saturation-

$$i_D = \frac{W\mu_oC_{ox}}{L} \left[(v_{GS} - V_T)v_{DS(\text{sat})} - \frac{v_{DS(\text{sat})}^2}{2} \right] (1 + \lambda v_{DS}) = \frac{W\mu_oC_{ox}}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

where:

μ_o = zero field mobility ($\text{cm}^2/\text{volt}\cdot\text{sec}$)

C_{ox} = gate oxide capacitance per unit area (F/cm^2)

λ = channel-length modulation parameter (volts^{-1})

$V_T = V_{T0} + \gamma (\sqrt{2|\phi_f| + |v_{BS}|} - \sqrt{2|\phi_f|})$

V_{T0} = zero bias threshold voltage

γ = bulk threshold parameter ($\text{volts}^{-0.5}$)

$2|\phi_f|$ = strong inversion surface potential (volts)

For p-channel MOSFETs, use n-channel equations with p-channel parameters and invert the current.

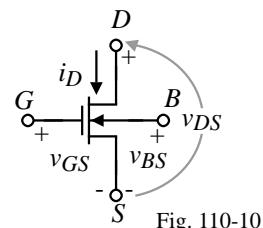


Fig. 110-10

Silicon Constants

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann's constant	1.381x10 ⁻²³	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45x10 ¹⁰	cm ⁻³
ϵ_o	Permittivity of free space	8.854x10 ⁻¹⁴	F/cm
ϵ_{si}	Permittivity of silicon	11.7 ϵ_o	F/cm
ϵ_{ox}	Permittivity of SiO ₂	3.9 ϵ_o	F/cm

MOSFET Parameters

Model Parameters for a Typical CMOS Bulk Process (0.25 μ m CMOS n -well):

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		N-Channel	P-Channel	
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.5 ± 0.15	-0.5 ± 0.15	V
K'	Transconductance Parameter (in saturation)	120.0 ± 10%	25.0 ± 10%	μ A/V ²
γ	Bulk threshold parameter	0.4	0.6	(V) ^{1/2}
λ	Channel length modulation parameter	0.32 ($L=L_{min}$) 0.06 ($L \geq 2L_{min}$)	0.56 ($L=L_{min}$) 0.08 ($L \geq 2L_{min}$)	(V) ⁻¹
$2 \phi_F $	Surface potential at strong inversion	0.7	0.8	V

SUBTHRESHOLD MODEL

Large-Signal Model for Weak Inversion

The electrons in the substrate at the source side can be expressed as,

$$n_p(0) = n_{po} \exp\left(\frac{\phi_s}{V_t}\right)$$

The electrons in the substrate at the drain side can be expressed as,

$$n_p(L) = n_{po} \exp\left(\frac{\phi_s - v_{DS}}{V_t}\right)$$

Therefore, the drain current due to diffusion is,

$$i_D = qAD_n \left(\frac{n_p(L) - n_p(0)}{L} \right) = \frac{W}{L} qXD_n n_{po} \exp\left(\frac{\phi_s}{V_t}\right) \left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right) \right]$$

where X is the thickness of the region in which i_D flows.

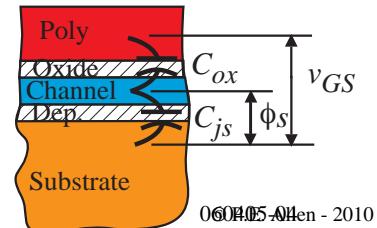
In weak inversion, the changes in the surface potential, $\Delta\phi_s$ are controlled by changes in the gate-source voltage, Δv_{GS} , through a voltage divider consisting of C_{ox} and C_{js} , the depletion region capacitance.

$$\therefore \frac{d\phi_s}{dv_{GS}} = \frac{C_{ox}}{C_{ox} + C_{js}} = \frac{1}{n} \rightarrow \phi_s = \frac{v_{GS} - V_T}{n} + k_1 = \frac{v_{GS} - V_T}{n} + k_2$$

where

$$k_2 = k_1 + \frac{V_T}{n}$$

CMOS Analog Circuit Design



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Large-Signal Model for Weak Inversion – Continued

Substituting the above relationships back into the expression for i_D gives,

$$i_D = \frac{W}{L} qXD_n n_{po} \exp\left(\frac{k_2}{V_t}\right) \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) \left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right) \right]$$

Define I_t as

$$I_t = qXD_n n_{po} \exp\left(\frac{k_2}{V_t}\right)$$

to get,

$$i_D = \frac{W}{L} I_t \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) \left[1 - \exp\left(-\frac{v_{DS}}{V_t}\right) \right]$$

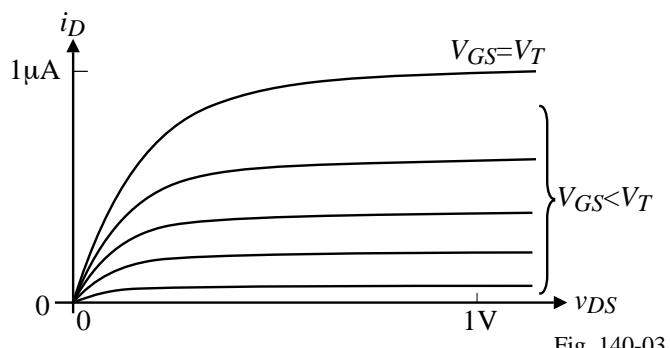
where $n \approx 1.5 - 3$

If $v_{DS} > 0$, then

$$i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS} - V_T}{nV_t}\right) \left(1 + \frac{v_{DS}}{V_A} \right)$$

The boundary between nonsaturated and saturated is found as,

$$V_{ov} = V_{DS(sat)} = V_{ON} = V_{GS} - V_T = 2nV_t$$



SHORT CHANNEL, STRONG INVERSION MODEL

What is Velocity Saturation?

The most important short-channel effect in MOSFETs is the velocity saturation of carriers in the channel. A plot of electron drift velocity versus electric field is shown below.

An expression for the electron drift velocity as a function of the electric field is,

$$v_d \approx \frac{\mu_n E}{1 + E/E_c}$$

where

v_d = electron drift velocity (m/s)

μ_n = low-field mobility ($\approx 0.07 \text{ m}^2/\text{V}\cdot\text{s}$)

E_c = critical electrical field at which velocity saturation occurs

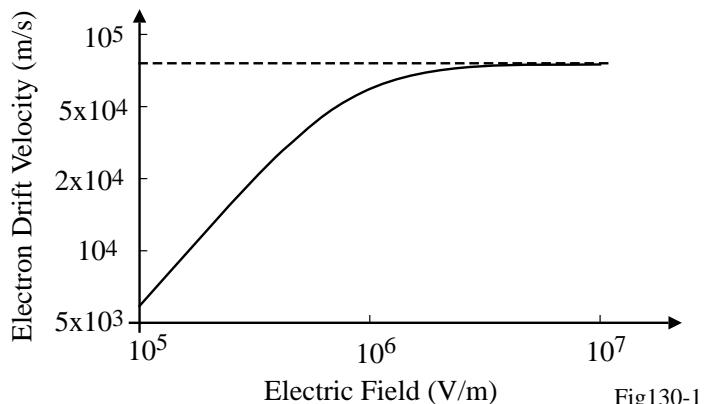


Fig130-1

Short-Channel Model Derivation

As before,

$$J_D = J_S = \frac{i_D}{W} = Q_I(y)v_d(y) \rightarrow i_D = WQ_I(y)v_d(y) = \frac{WQ_I(y)\mu_n E}{1 + E/E_c} \rightarrow i_D \left(1 + \frac{E}{E_c}\right) = WQ_I(y)\mu_n E$$

Replacing E by dv/dy gives,

$$i_D \left(1 + \frac{1}{E_c} \frac{dv}{dy}\right) = WQ_I(y)\mu_n dv$$

Integrating along the channel gives,

$$\int_0^L i_D \left(1 + \frac{1}{E_c} \frac{dv}{dy}\right) dy = \int_0^{v_{DS}} WQ_I(y)\mu_n dv$$

The result of this integration is,

$$i_D = \frac{\mu_n C_{ox}}{2 \left(1 + \frac{1}{E_c} \frac{v_{DS}}{L}\right)} \frac{W}{L} [2(v_{GS} - V_T)v_{DS} - v_{DS}^2] = \frac{\mu_n C_{ox}}{2(1 + \theta v_{DS})} \frac{W}{L} [2(v_{GS} - V_T)v_{DS} - v_{DS}^2]$$

where $\theta = 1/(E_c L)$ with dimensions of V^{-1} .

Saturation Voltage

Differentiating i_D with respect to v_{DS} and setting equal to zero gives,

$$V'_{DS}(\text{sat}) = \frac{1}{\theta} (\sqrt{1 + 2\theta(V_{GS} - V_T)} - 1) \approx (V_{GS} - V_T) \left(1 - \frac{\theta(V_{GS} - V_T)}{2} + \dots \right)$$

if

$$\frac{\theta(V_{GS} - V_T)}{2} < 1$$

Therefore,

$$V'_{DS}(\text{sat}) \approx V_{DS}(\text{sat}) \left(1 - \frac{\theta(V_{GS} - V_T)}{2} + \dots \right)$$

Note that the transistor will enter the saturation region for $v_{DS} < v_{GS} - V_T$ in the presence of velocity saturation.

Large Signal Model for the Saturation Region

Assuming that

$$\frac{\theta(V_{GS} - V_T)}{2} < 1$$

gives

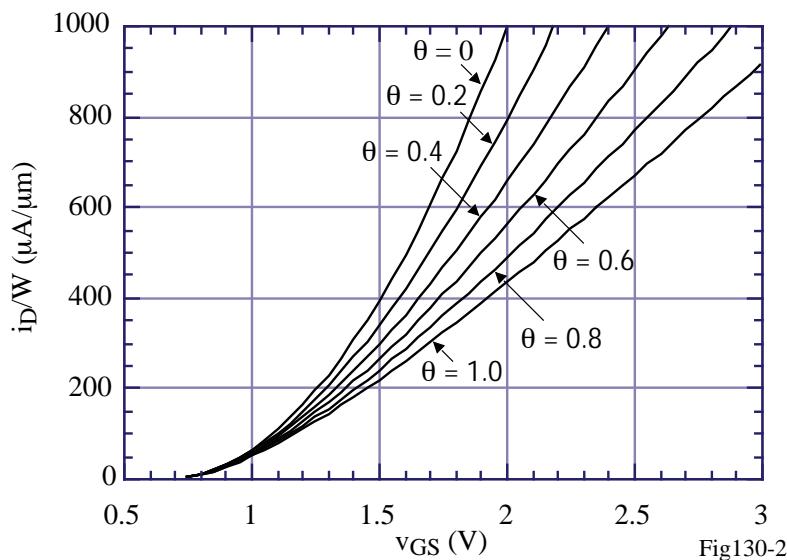
$$V'_{DS}(\text{sat}) \approx (V_{GS} - V_T)$$

Therefore the large signal model in the saturation region becomes,

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]} \frac{W}{L} [v_{GS} - V_T]^2, \quad v_{DS} \geq (V_{GS} - V_T) \left(1 - \frac{\theta(V_{GS} - V_T)}{2} + \dots \right)$$

The Influence of Velocity Saturation on the Transconductance Characteristics

The following plot was made for $K' = 110\mu\text{A/V}^2$ and $W/L = 1$:



Note as the velocity saturation effect becomes stronger, that the drain current-gate voltage relationship becomes linear.

Circuit Model for Velocity Saturation

A simple circuit model to include the influence of velocity saturation is shown:

We know that

$$i_D = \frac{K'W}{2L} (v_{GS}' - V_T)^2 \quad \text{and} \quad v_{GS} = v_{GS}' + i_D R_{SX}$$

or

$$v_{GS}' = v_{GS} - i_D R_{SX}$$

Substituting v_{GS}' into the current relationship gives,

$$i_D = \frac{K'W}{2L} (v_{GS} - i_D R_{SX} - V_T)^2$$

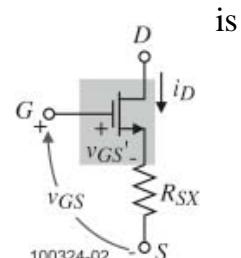
Solving for i_D results in,

$$i_D = \frac{K'}{2 \left[1 + K' \frac{W}{L} R_{SX} (v_{GS} - V_T) \right]} \frac{W}{L} (v_{GS} - V_T)^2$$

Comparing with the previous result, we see that

$$\theta = K' \frac{W}{L} R_{SX} \rightarrow R_{SX} = \frac{\theta L}{K' W} = \frac{1}{E_c K' W}$$

Therefore for $K' = 110\mu\text{A/V}^2$, $W = 1\mu\text{m}$ and $E_c = 1.5 \times 10^6 \text{V/m}$, we get $R_{SX} = 6.06\text{k}\Omega$.



SUMMARY

- The modeling of this lecture is devoted to understanding how the circuit works
- The two primary current-voltage characteristics of the MOSFET are the transconductance characteristic and the output characteristic
- The simple Sah large signal model is good enough for most applications and technology
- The Sah model can be improved in the region of the knee and for the weak dependence of drain current on drain-source voltage in the saturation region
- Most designers do not work at minimum channel length because of the channel length modulation effect and because worse matching occurs for small areas
- The threshold voltage is increased as the bulk-source is reverse biased
- The subthreshold model accounts for very small currents that flow in the channel when the gate-source voltage is smaller than the threshold voltage
- The subthreshold current is exponentially related to the gate-source voltage
- Velocity saturation occurs at minimum channel length and can be modeled by including a source degeneration resistor with the simple large signal model

LECTURE 100 – MOS CAPACITOR MODEL AND LARGE SIGNAL MODEL DEPENDENCE

LECTURE ORGANIZATION

Outline

- MOSFET capacitor model
- Dependence of the large signal model on process
- Dependence of the large signal model on voltage
- Dependence of the large signal model on temperature
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 79-86

MOSFET CAPACITOR MODEL

Submicron Technology

Physical perspective:

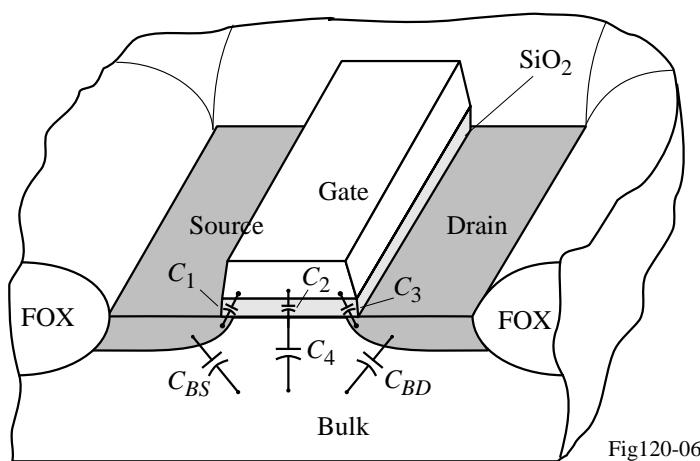


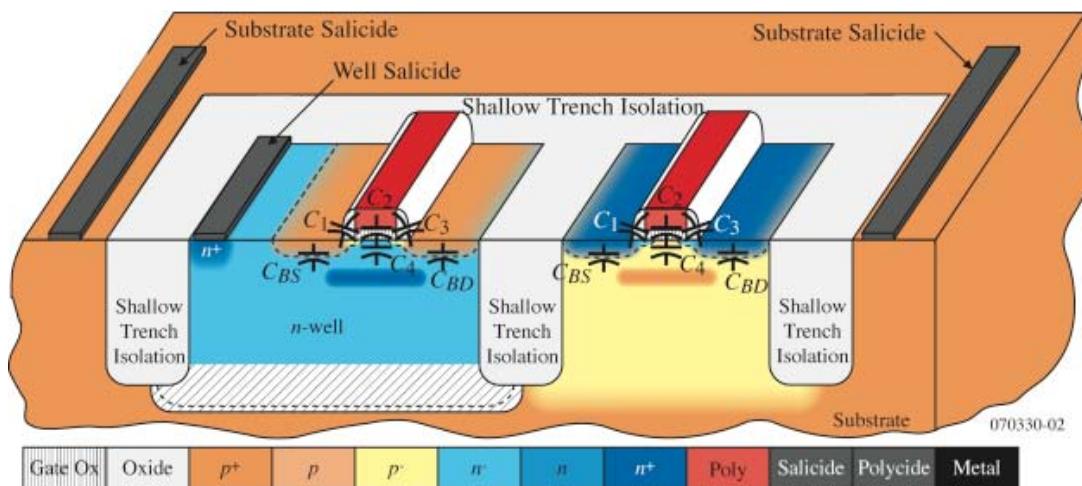
Fig120-06

MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

Deep Submicron Technology

Physical perspective:



MOSFET capacitors consist of:

- Depletion capacitances
- Charge storage or parallel plate capacitances

MOSFET Depletion Capacitors

Model:

$$1.) \quad v_{BS} \leq FC \cdot PB$$

$$C_{BS} = \frac{CJ \cdot AS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PS}{\left(1 - \frac{v_{BS}}{PB}\right)^{MJSW}},$$

and

$$2.) \quad v_{BS} > FC \cdot PB$$

$$C_{BS} = \frac{CJ \cdot AS}{(1 - FC)^{1+MJ}} \left(1 - (1+MJ)FC + MJ \frac{V_{BS}}{PB}\right)$$

$$+ \frac{CJSW \cdot PS}{(1 - FC)^{1+MJSW}} \left(1 - (1+MJSW)FC + MJSW \frac{V_{BS}}{PB}\right)$$

where

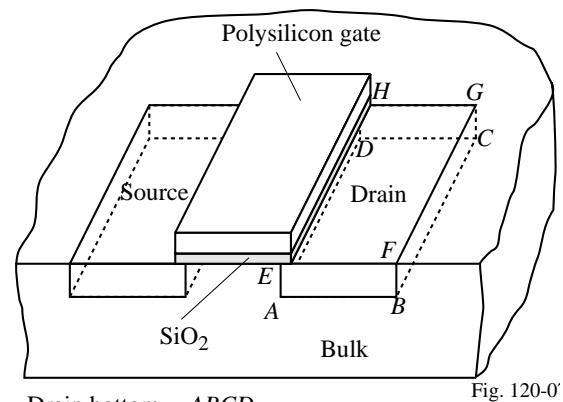
AS = area of the source

PS = perimeter of the source

$CJSW$ = zero bias, bulk source sidewall capacitance

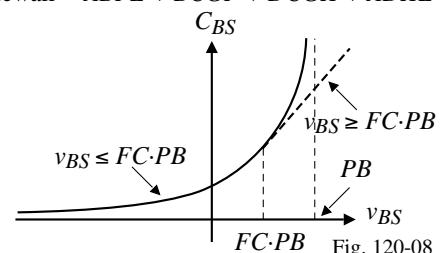
$MJSW$ = bulk-source sidewall grading coefficient

For the bulk-drain depletion capacitance replace "S" by "D" in the above.

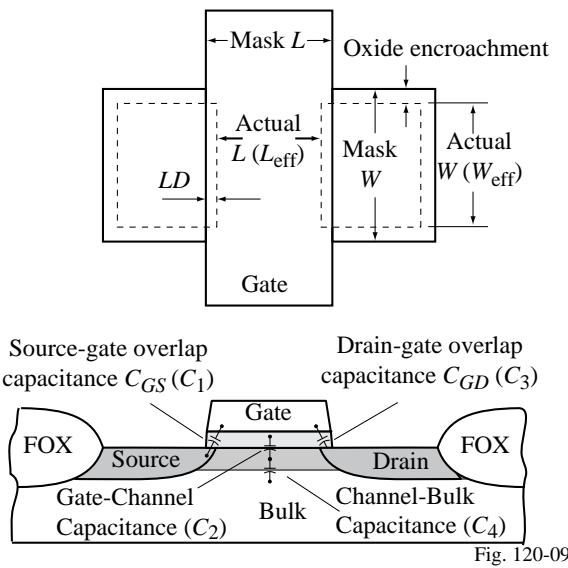


Drain bottom = ABCD

Drain sidewall = ABFE + BCGF + DCGH + ADHE



SM Charge Storage (Parallel Plate) MOSFET Capacitances - C_1, C_2, C_3 and C_4



Overlap capacitances:

$$C_1 = C_3 = LD \cdot W_{\text{eff}} \cdot C_{ox} = CGSO \text{ or } CGDO$$

($LD \approx 0.015 \mu\text{m}$ for LDD structures)

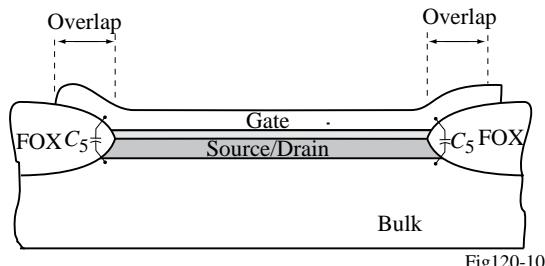
Channel capacitances:

$$C_2 = \text{gate-to-channel} = C_{ox} W_{\text{eff}} \cdot (L - 2LD) = C_{ox} W_{\text{eff}} \cdot L_{\text{eff}}$$

$C_4 = \text{voltage dependent channel-bulk/substrate capacitance}$

SM Charge Storage (Parallel Plate) MOSFET Capacitances - C_5

View looking down the channel from source to drain

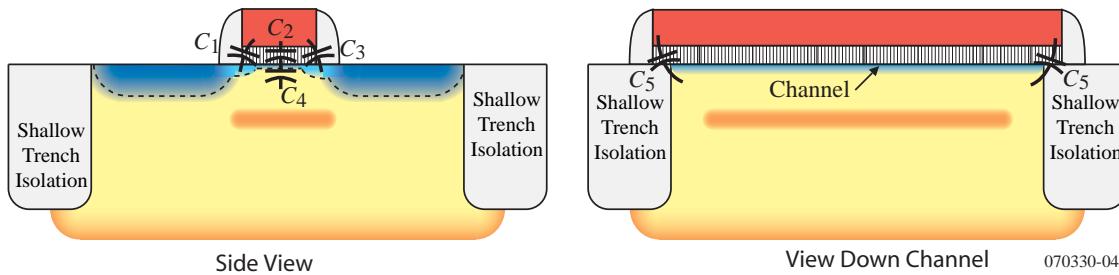


$$C_5 = CGBO$$

Capacitance values based on an oxide thickness of 140 Å or $C_{ox} = 24.7 \times 10^{-4} \text{ F/m}^2$:

Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m ²
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

DSM Charge Storage MOSFET Capacitances - C_1, C_2, C_3, C_4 and C_5



C_1 and C_3 are overlap capacitors due to lateral diffusion of the source and drain

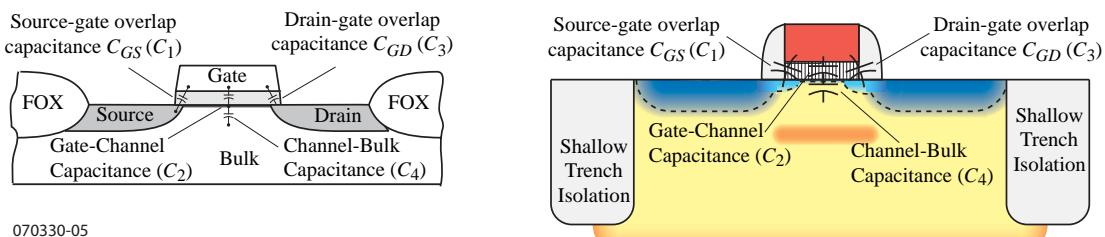
C_2 is the gate to channel capacitance

C_4 is the depletion capacitance between the channel and the bulk

C_5 is the fringing capacitance between the gate and the bulk around the edges of the channel

MOSFET Capacitors for the Cutoff Region

Side view:



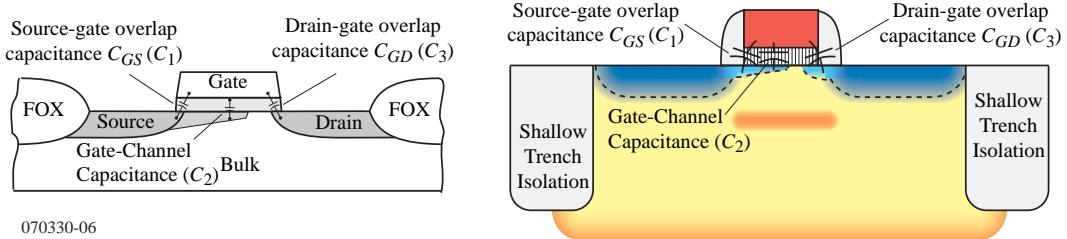
As the gate-source voltage varies from 0 to V_T , the channel-bulk capacitor varies from a very large capacitor (because of a very small depletion region) to a capacitor much smaller than C_2 .

Capacitors in Cutoff:

C_{GS}	$C_1 = C_{ox} \cdot LD \cdot W = CGSO \cdot W$
C_{GD}	$C_3 = C_{ox} \cdot LD \cdot W = CGDO \cdot W$
C_{GB}	C_2 varies from $C_{ox} \cdot L \cdot W$ to $2C_5$
C_{BD}	$C_{BD} = (CJ \cdot AD) / [1 - (v_{BD}/PB)]^{MJ} + (CJSW \cdot PD) / [1 - (v_{BD}/PB)]^{MJSW}$
C_{BS}	$C_{BS} = (CJ \cdot AS) / [1 - (v_{BS}/PB)]^{MJ} + (CJSW \cdot PS) / [1 - (v_{BS}/PB)]^{MJSW}$

MOSFET Capacitors for the Saturation Region

Side view:



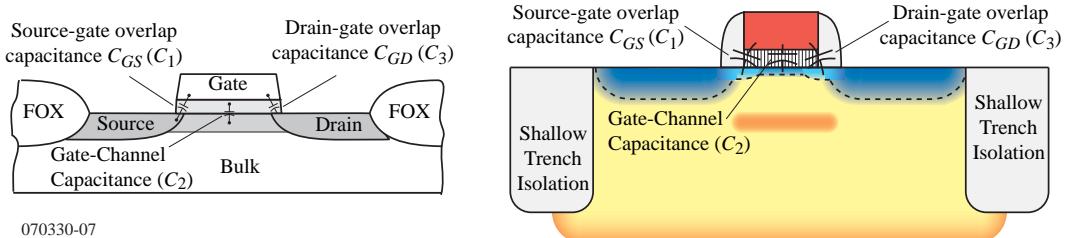
In the saturation region, C_4 , becomes small and is not shown above.

Capacitors in Saturation:

C_{GS}	$C_1 = C_{ox} \cdot LD \cdot W + (2/3)C_{ox} \cdot L \cdot W = [CGSO + (2/3)C_{ox} \cdot L]W$
C_{GD}	$C_3 = C_{ox} \cdot LD \cdot W = CGDO \cdot W$
C_{GB}	$2C_5 = 2 \cdot CGBO \cdot W$
C_{BD}	$C_{BD} = (CJ \cdot AD)/[1 - (v_{BD}/PB)]^{MJ} + (CJSW \cdot PD)/[1 - (v_{BD}/PB)]^{MJSW}$
C_{BS}	$C_{BS} = (CJ \cdot AS)/[1 - (v_{BS}/PB)]^{MJ} + (CJSW \cdot PS)/[1 - (v_{BS}/PB)]^{MJSW}$

MOSFET Capacitors for the Active Region

Side view:



In the saturation region, C_4 , becomes small and is not shown above.

Capacitors in Active:

C_{GS}	$C_1 = C_{ox} \cdot LD \cdot W + (1/2)C_{ox} \cdot L \cdot W = [CGSO + (1/2)C_{ox} \cdot L]W$
C_{GD}	$C_3 = C_{ox} \cdot LD \cdot W + (1/2)C_{ox} \cdot L \cdot W = [CGSO + (1/2)C_{ox} \cdot L]W$
C_{GB}	$2C_5 = 2 \cdot CGBO \cdot W$
C_{BD}	$C_{BD} = (CJ \cdot AD)/[1 - (v_{BD}/PB)]^{MJ} + (CJSW \cdot PD)/[1 - (v_{BD}/PB)]^{MJSW}$
C_{BS}	$C_{BS} = (CJ \cdot AS)/[1 - (v_{BS}/PB)]^{MJ} + (CJSW \cdot PS)/[1 - (v_{BS}/PB)]^{MJSW}$

Illustration of C_{GD} , C_{GS} and C_{GB}

Comments on the variation of C_{BG} in the cutoff region:

$$C_{BG} = \frac{1}{\frac{1}{C_2} + \frac{1}{C_4}} + 2C_5$$

- 1.) For $v_{GS} \approx 0$, $C_{GB} \approx C_2 + 2C_5$

(C_4 is large because of the thin inversion layer in weak inversion where V_{GS} is slightly less than V_T)

- 2.) For $0 < v_{GS} \leq V_T$, $C_{GB} \approx 2C_5$
(C_4 is small because of the thicker inversion layer in strong inversion)

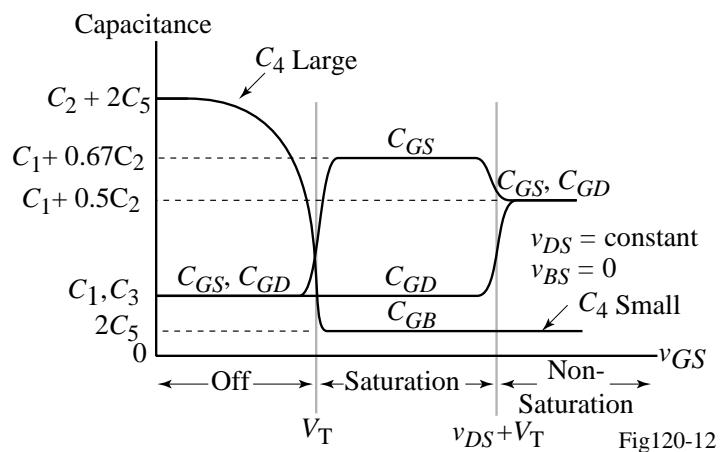
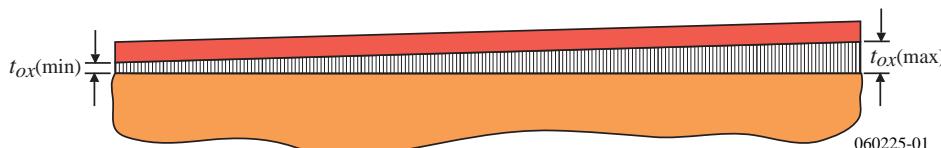


Fig120-12

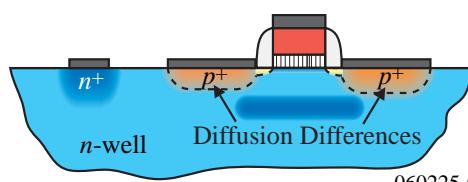
DEPENDENCE OF THE LARGE SIGNAL MODEL ON PROCESS

How Does Technology Vary?

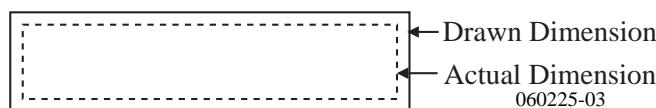
- 1.) Thickness variations in layers (dielectrics and metal)



- 2.) Doping variations



- 3.) Process biases – differences between the drawn and actual dimensions due to process (etching, lateral diffusion, etc.)



Large Signal Model Dependence on Process Variations

1.) Threshold voltage

$$V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + v_{SB}|} - \sqrt{|-2\phi_F|})$$

where

$$V_{T0} = \phi_{MS} - 2\phi_F - \frac{Q_{b0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} \quad \text{and} \quad \gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}}$$

If $V_{BS} = 0$, then V_T is dependent on doping and oxide thickness because

$$\phi_F = \frac{kT}{q} \ln \left(\frac{N_{SUB}}{n_i} \right) \quad \text{and} \quad C_{ox} \propto \frac{1}{t_{ox}}$$

(Recall that the threshold is also determined by the threshold implant during processing)

2.) Transconductance parameter

$$K' = \mu_o C_{ox} \propto \frac{1}{t_{ox}}$$

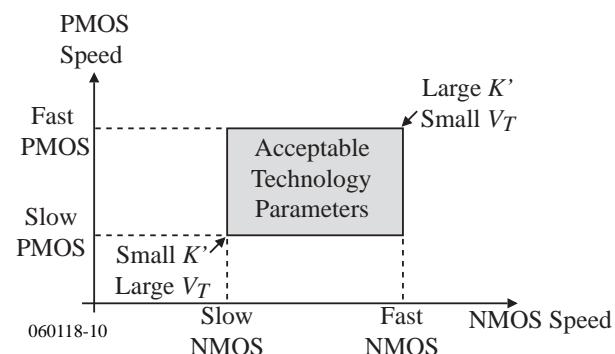
For short channel devices, the mobility is degraded as given by

$$\mu_{eff} = \frac{\mu_o}{1 + \theta(V_{GS} - V_T)} \quad \text{and} \quad \theta \approx \frac{2 \times 10^{-9} \text{ m/V}}{t_{ox}}$$

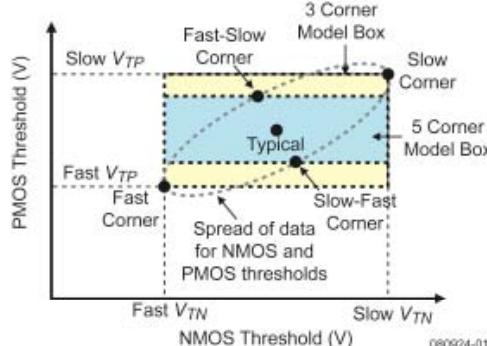
Process Variation “Corners”

For strong inversion operation, the primary influence is the oxide thickness, t_{ox} . We see that K' will tend to increase with decreasing oxide thickness whereas V_T tends to decrease.

If the “speed” of a transistor is increased by increasing K' and decreasing V_T , then the variation of technology can be expressed on a two-dimensional graph resulting in a rectangular area of “acceptable” process limitation.



Three corner versus five corner models



DEPENDENCE OF THE LARGE SIGNAL MODEL ON VOLTAGE

What is Voltage Variation?

Voltage variation is the influence of power supply voltage on the component.

(There is also power supply influence on the circuit called power supply rejection ratio, PSRR. We will deal with this much later.)

Power supply variation comes from:

- 1.) Influence of depletion region widths on components.
- 2.) Nonlinearity
- 3.) Breakdown voltage

Note: Because the large-signal model for the MOSFET includes all the influences of voltage on the transistor, we will focus on passive components except for breakdown.

Models for Voltage Dependence of a Component

1.) *i*th-order Voltage Coefficients

In general a variable $y = f(v)$ which is a function of voltage, v , can be expressed as a Taylor series,

$$y(v = V_0) \approx y(V_0) + a_1(v - V_0) + a_2(v - V_0)^2 + a_3(v - V_0)^3 + \dots$$

where the coefficients, a_i , are defined as,

$$a_1 = \frac{df(v)}{dv} \Big|_{v=V_0}, a_2 = \frac{1}{2} \frac{d^2f(v)}{dv^2} \Big|_{v=V_0}, \dots$$

The coefficients, a_i , are called the first-order, second-order, voltage coefficients.

2.) Fractional Voltage Coefficient or Voltage Coefficient

Generally, only the first-order coefficients are of interest.

In the characterization of temperature dependence, it is common practice to use a term called *fractional voltage coefficient*, VC_F , which is defined as,

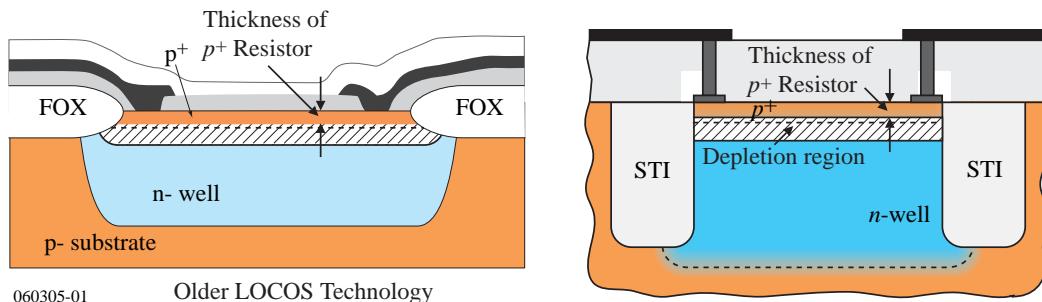
$$VC_F(v = V_0) = \frac{1}{f(v = V_0)} \frac{df(v)}{dv} \Big|_{v=V_0} \text{ parts per million/V (ppm/V)}$$

or more simply,

$$VC_F = \frac{1}{f(v)} \frac{df(v)}{dv} \text{ parts per million/V (ppm/V)}$$

Influence of Voltage on a Diffused Resistor – Depletion Region

Influence of the depletion region on the p^+ resistor:



As the voltage at the terminals of the resistor become smaller than the n -well potential, the depletion region will widen causing the thickness of the resistor to decrease.

$$R = \frac{\rho L}{t W} \propto \sqrt{V_R}$$

where V_R is the reverse bias voltage from the resistor to the well.

This effect is worse for well resistors because the doping concentration of the resistor is smaller.

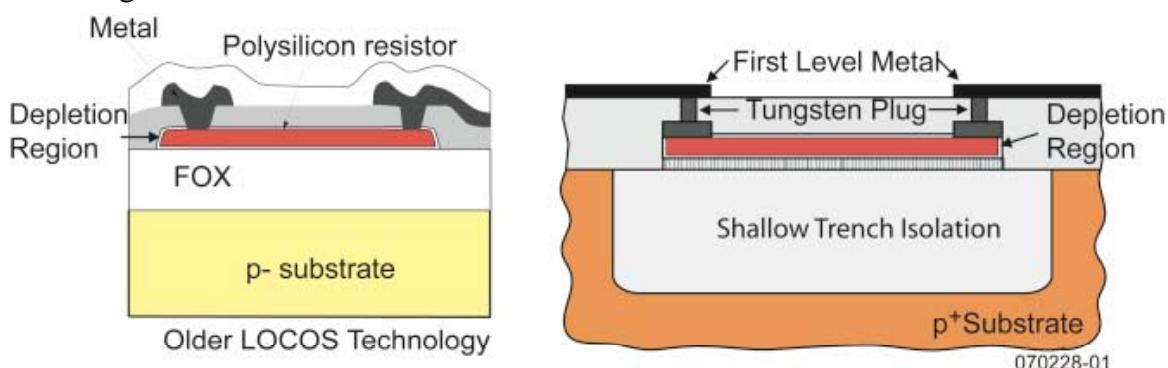
Voltage coefficient for diffused resistors $\approx 200\text{-}800 \text{ ppm/V}$

Voltage coefficient for well resistors $\approx 8000 \text{ ppm/V}$

Voltage Coefficient of Polysilicon Resistors

Why should polysilicon resistors be sensitive to voltage?

There is a small depletion region between the polysilicon and its surrounding material that has a very small dependence on the voltage between the polysilicon and the surrounding material.

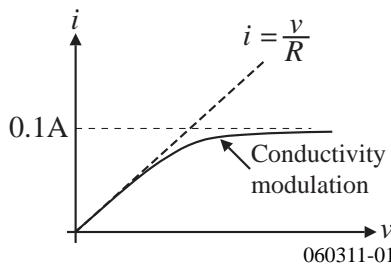


Voltage Nonlinearity and Breakdown Voltage

Conductivity modulation:

As the current in a resistor increases, the conductivity becomes modulated and the resistance increases.

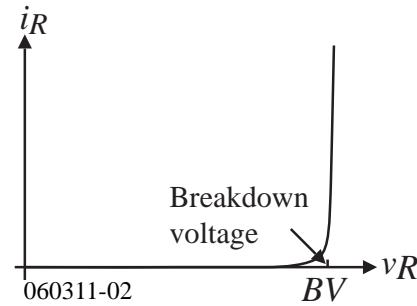
Example of a *n*-well resistor:



As the reverse bias voltage across a *pn* junction becomes large, at some point, called the breakdown voltage, the current will rapidly increase. Both transistors, diodes and depletion capacitors experience this breakdown.

Model for current multiplication factor:

$$M = \frac{1}{1 + \left(\frac{vR}{BV}\right)^n}$$



DEPENDENCE OF THE LARGE SIGNAL MODEL ON TEMPERATURE

Temperature Dependence of the MOSFET

Transconductance parameter:

$$K'(T) = K'(T_0) (T/T_0)^{-1.5} \quad (\text{Exponent becomes } +1.5 \text{ below } 77^\circ\text{K})$$

Threshold Voltage:

$$V_T(T) = V_T(T_0) + \alpha(T-T_0) + \dots$$

Typically $\alpha_{NMOS} = -2\text{mV}/^\circ\text{C}$ to $-3\text{mV}/^\circ\text{C}$ from 200°K to 400°K (PMOS has a + sign)

Example

Find the value of I_D for a NMOS transistor at 27°C and 100°C if $V_{GS} = 2\text{V}$ and $W/L = 5\mu\text{m}/1\mu\text{m}$ if $K'(T_0) = 110\mu\text{A}/\text{V}^2$ and $V_T(T_0) = 0.7\text{V}$ and $T_0 = 27^\circ\text{C}$ and $\alpha_{NMOS} = -2\text{mV}/^\circ\text{C}$.

Solution

At room temperature, the value of drain current is,

$$I_D(27^\circ\text{C}) = \frac{110\mu\text{A}/\text{V}^2 \cdot 5\mu\text{m}}{2 \cdot 1\mu\text{m}} (2 - 0.7)^2 = 465\mu\text{A}$$

At $T = 100^\circ\text{C}$ (373°K), $K'(100^\circ\text{C}) = K'(27^\circ\text{C}) (373/300)^{-1.5} = 110\mu\text{A}/\text{V}^2 \cdot 0.72 = 79.3\mu\text{A}/\text{V}^2$
and $V_T(100^\circ\text{C}) = 0.7 - (.002)(73^\circ\text{C}) = 0.554\text{V}$

$$\therefore I_D(100^\circ\text{C}) = \frac{79.3\mu\text{A}/\text{V}^2 \cdot 5\mu\text{m}}{2 \cdot 1\mu\text{m}} (2 - 0.554)^2 = 415\mu\text{A} \quad (\text{Repeat with } V_{GS} = 2.0855\text{V})$$

Zero Temperature Coefficient (ZTC) Point for MOSFETs

For a given value of gate-source voltage, the drain current of the MOSFET will be independent of temperature. Consider the following circuit:

Assume that the transistor is saturated and that:

$$\mu = \mu_0 \left(\frac{T}{T_0} \right)^{-1.5} \quad \text{and} \quad V_T(T) = V_{T0} + \alpha(T - T_0)$$

where $\alpha = -0.0023 \text{V}/\text{°C}$ and $T_0 = 27^\circ\text{C}$

$$\therefore I_D(T) = \frac{\mu_0 C_{ox} W}{2L} \left(\frac{T}{T_0} \right)^{-1.5} [V_{GS} - V_{T0} - \alpha(T - T_0)]^2$$

$$\frac{dI_D}{dT} = \frac{-1.5 \mu_0 C_{ox}}{2T_0} \left(\frac{T}{T_0} \right)^{-2.5} [V_{GS} - V_{T0} - \alpha(T - T_0)]^2 + \alpha \mu_0 C_{ox} \left(\frac{T}{T_0} \right)^{-1.5} [V_{GS} - V_{T0} - \alpha(T - T_0)] = 0$$

$$\therefore V_{GS} - V_{T0} - \alpha(T - T_0) = \frac{-4T\alpha}{3} \quad \Rightarrow \quad V_{GS(\text{ZTC})} = V_{T0} - \alpha T_0 - \frac{\alpha T}{3}$$

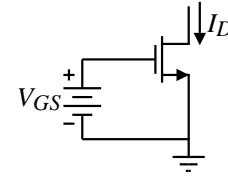


Fig. 4.5-12

Let $K' = 10 \mu\text{A}/\text{V}^2$, $W/L = 5$ and $V_{T0} = 0.71\text{V}$.

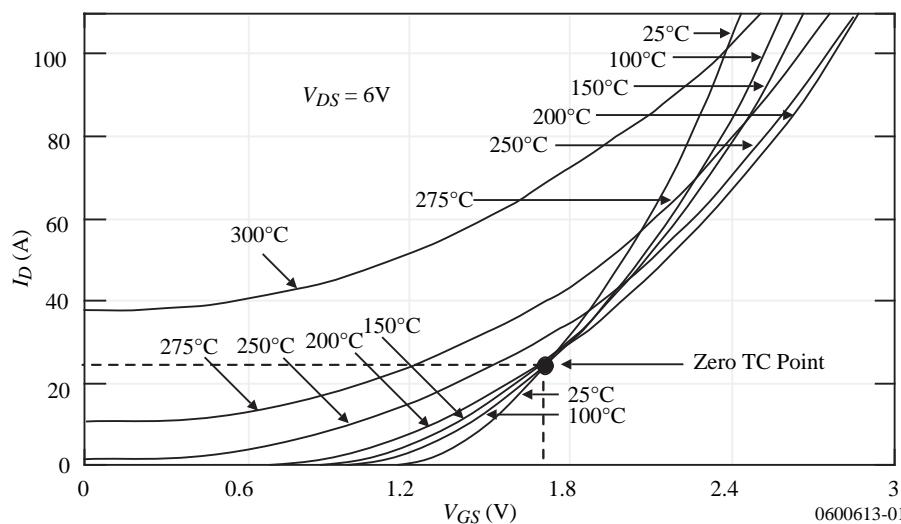
At $T=27^\circ\text{C}(300^\circ\text{K})$, $V_{GS(\text{ZTC})}=0.71-(-0.0023)(300^\circ\text{K})-(0.333)(-0.0023)(300^\circ\text{K})=1.63\text{V}$

At $T=27^\circ\text{C}$ (300°K), $I_D = (10 \mu\text{A}/\text{V}^2)(5/2)(1.63-0.71)^2 = 21.2 \mu\text{A}$

At $T=200^\circ\text{C}(473^\circ\text{K})$, $V_{GS(\text{ZTC})}=0.71-(-0.0023)(300^\circ\text{K})-(0.333)(-0.0023)(473^\circ\text{K})=1.76\text{V}$

Experimental Verification of the ZTC Point

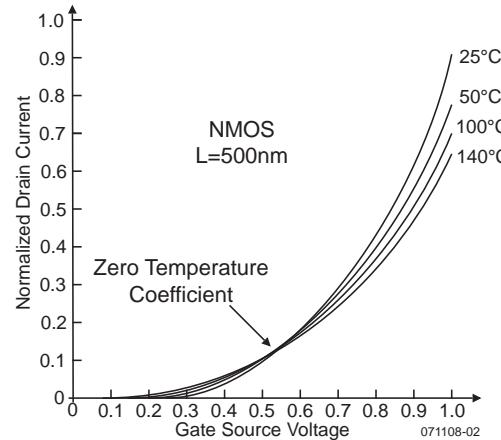
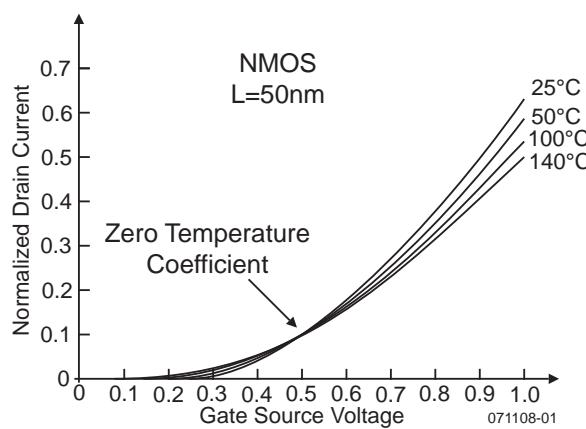
The data below is for a $5\mu\text{m}$ n-channel MOSFET with $W/L=50\mu\text{m}/10\mu\text{m}$, $N_A=10^{16} \text{ cm}^{-3}$, $t_{ox} = 650\text{\AA}$, $\mu_0 C_{ox} = 10 \mu\text{A}/\text{V}^2$, and $V_{T0} = 0.71\text{V}$.



A similar result holds for the p-channel MOSFET.

ZTC Point for UDSM Technology

50 nm CMOS:



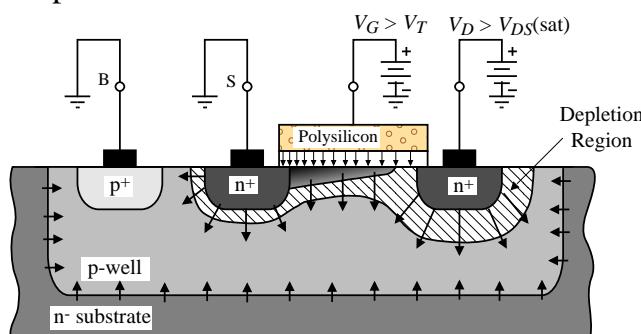
Note that the ZTC point is close to V_{DD} .

PMOS will have similar characteristics.

Bulk-Drain (Bulk-Source) Leakage Currents

Cross-section of a NMOS in a p-well:

$V_{GS} > V_T$:



$V_{GS} < V_T$:

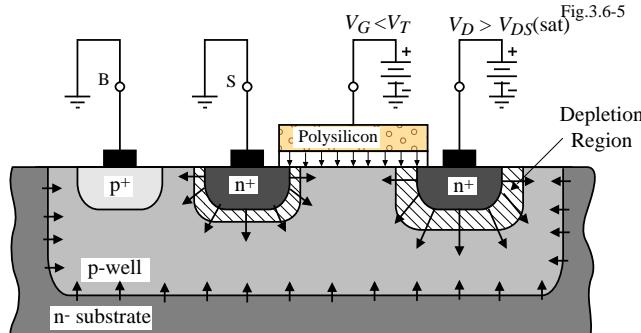


Fig.3.6-5

Temperature Modeling of the PN Junction

PN Junctions (Reverse-biased only):

$$-i_D \approx I_s = qA \left[\frac{D_{ppno}}{L_p} + \frac{D_{nnpo}}{L_n} \right] \approx \frac{qAD}{L} \frac{n_i^2}{N} = KT^3 \exp\left(\frac{-V_{Go}}{V_t}\right)$$

Differentiating with respect to temperature gives,

$$\frac{dI_s}{dT} = \frac{3KT^2}{T} \exp\left(\frac{-V_{Go}}{V_t}\right) + \frac{qKT^3 V_{Go}}{KT^2} \exp\left(\frac{-V_{Go}}{V_t}\right) = \frac{3I_s}{T} + \frac{I_s}{T} \frac{V_{Go}}{V_t}$$

$$TC_F = \frac{dI_s}{I_s dT} = \frac{3}{T} + \frac{1}{T} \frac{V_{Go}}{V_t}$$

Example

Assume that the temperature is 300°K (room temperature) and calculate the reverse diode current change and the TC_F for a 5°K increase.

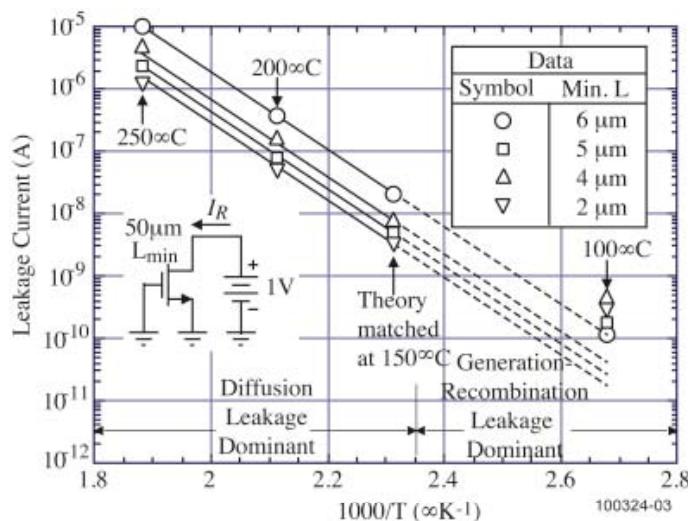
Solution

The TC_F can be calculated from the above expression as $TC_F = 0.01 + 0.155 = 0.165$.

Since the TC_F is change per degree, the reverse current will increase by a factor of 1.165 for every degree K (or °C) change in temperature. Multiplying by 1.165 five times gives an increase of approximately 2. Thus, the reverse saturation current approximately doubles for every 5°C temperature increase.

Experimentally, the reverse current doubles for every 8°C increase in temperature because the reverse current is in part leakage current.

Experimental Verification of the PN Junction Temperature Dependence



Theory:

$$I_s(T) \propto T^3 \exp\left(\frac{V_G(T)}{kT}\right)$$

Temperature Modeling of the PN Junction – Continued

PN Junctions (Forward biased – v_D constant):

$$i_D \cong I_s \exp\left(\frac{v_D}{V_t}\right)$$

Differentiating this expression with respect to temperature and assuming that the diode voltage is a constant ($v_D = V_D$) gives

$$\frac{di_D}{dT} = \frac{i_D}{I_s} \frac{dI_s}{dT} - \frac{1}{T} \frac{V_D}{V_t} i_D$$

The fractional temperature coefficient for i_D is

$$\frac{1}{i_D} \frac{di_D}{dT} = \frac{1}{I_s} \frac{dI_s}{dT} - \frac{V_D}{TV_t} = \frac{3}{T} + \left[\frac{V_{Go} - V_D}{TV_t} \right]$$

If V_D is assumed to be 0.6 volts, then the fractional temperature coefficient is equal to $0.01 + (0.155 - 0.077) = 0.0879$. The forward diode current will approx. double for a 10°C .

PN Junctions (Forward biased – i_D constant):

$$V_D = V_t \ln(I_D/I_s)$$

Differentiating with respect to temperature gives

$$\frac{dv_D}{dT} = \frac{v_D}{T} - V_t \left(\frac{1}{I_s} \frac{dI_s}{dT} \right) = \frac{v_D}{T} - \frac{3V_t}{T} - \frac{V_{Go}}{T} = - \left[\frac{V_{Go} - v_D}{T} \right] - \frac{3V_t}{T}$$

Assuming that $v_D = V_D = 0.6$ V the temperature dependence of the forward diode voltage at room temperature is approximately -2.3 mV/ $^\circ\text{C}$.

Resistor Dependence on Temperature

Diffused Resistors:

The temperature dependence of resistors depends mostly on the doping level of diffused and implanted resistors. As the doping level or sheet resistance increases from $100 \Omega/\square$ to $400 \Omega/\square$, the temperature coefficient varies from about $+1000$ ppm/ $^\circ\text{C}$ to $+4000$ ppm/ $^\circ\text{C}$. Diffused and implanted resistors have good thermal conduction to the substrate or well.

Polysilicon Resistors:

Typically has a sheet resistance of $20 \Omega/\square$ to $80 \Omega/\square$ and has poor thermal conduction because it is electrically isolated by oxide layers.

Metal:

Metal is often used for resistors and has a positive temperature coefficient.

Temperature Coefficients of Resistors:

n -well = 4000 ppm/ $^\circ\text{C}$

Diffusion = $+1500$ ppm/ $^\circ\text{C}$

Polysilicon = 500 - 2000 ppm/ $^\circ\text{C}$

Ion implanted = $+400$ ppm/ $^\circ\text{C}$

Metal = $+3800$ ppm/ $^\circ\text{C}$ (aluminum)

SUMMARY

- The large signal capacitance model includes depletion and parallel plate capacitors
- The depletion capacitors C_{BD} and C_{BS} vary with their reverse bias voltage
- The capacitors C_{GD} , C_{GS} , and C_{GB} have different values for the regions of cutoff, active and saturated
- The large signal model varies with process primarily through μ_o and t_{ox}
- Voltage dependence of resistors and capacitors is primarily due to the influence of depletion regions
- The temperature dependent large signal model of the MOSFET yields a gate-source voltage where the derivative of drain current with respect to temperature is zero
- Other MOSFET temperature dependence comes from the leakage currents across reverse biased pn junctions

LECTURE 110 – LINEAR CIRCUIT MODELS

LECTURE ORGANIZATION

Outline

- Frequency independent small signal transistor models
- Frequency dependent small signal transistor model
- Noise models
- Passive component models
- Interconnects
- Substrate interference
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 86-91 and new material

FREQUENCY INDEPENDENT SMALL SIGNAL TRANSISTOR MODELS

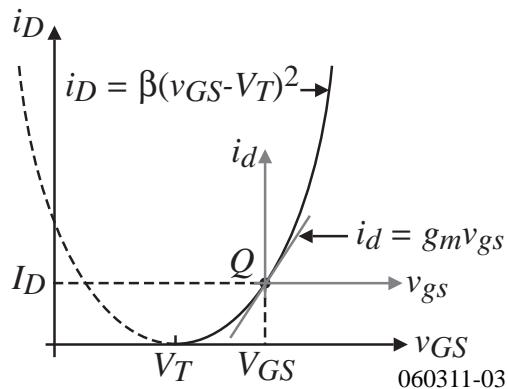
What is a Small Signal Model?

The small signal model is a linear approximation of a nonlinear model.

Mathematically:

$$i_D = \frac{\beta}{2} (v_{GS} - V_T)^2 \xrightarrow{\text{Large Signal to Small Signal}} i_d = g_m v_{gs}$$

Graphically:



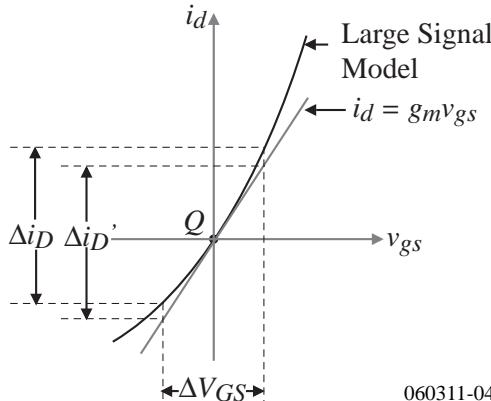
The large signal curve at point Q has been approximated with a small signal model going through the point Q and having a slope of g_m .

Why Small Signal Models?

The small signal model is a linear approximation to the large signal behavior.

- 1.) The transistor is biased at given DC operating point (Point Q above)
- 2.) Voltage changes are made about the operating point.
- 3.) Current changes result from the voltage changes.

If the designer is interested in only the current changes and not the DC value, then the small signal model is a fast and simple way to find the current changes given the voltage changes.



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How Good is the Small Signal Model?

It depends on how large are the changes and how nonlinear is the large signal model.

- The parameters of the small signal model will depend on the values of the large signal model.
- The model is a tradeoff in complexity versus accuracy (we will choose simplicity and give up accuracy).
- What does a simulator do? Exactly the same thing when it makes an ac analysis (i.e. frequency response)
- Regardless of the approximate nature of the small signal model, it is the primary model used to predict the signal performance of an analog circuit.

Small-Signal Model for the Saturation Region

The small-signal model is a linearization of the large signal model about a quiescent or operating point.

Consider the large-signal MOSFET in the saturation region ($v_{DS} \geq v_{GS} - V_T$) :

$$i_D = \frac{W\mu_o C_{ox}}{2L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$

The small-signal model is the linear dependence of i_d on v_{gs} , v_{bs} , and v_{ds} . Written as,

$$i_d \approx g_m v_{gs} + g_{mbs} v_{bs} + g_{ds} v_{ds}$$

where

$$g_m \equiv \left. \frac{di_D}{dv_{GS}} \right|_Q = \beta(V_{GS} - V_T) = \sqrt{2\beta I_D}$$

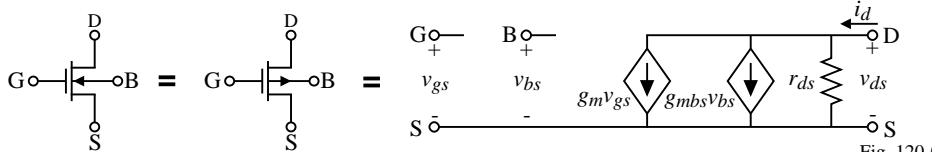
$$g_{ds} \equiv \left. \frac{di_D}{dv_{DS}} \right|_Q = \frac{\lambda I_D}{1 + \lambda V_{DS}} \approx \lambda I_D$$

and

$$g_{mbs} \equiv \left. \frac{di_D}{dv_{BS}} \right|_Q = \left(\frac{di_D}{dv_{GS}} \right) \left(\frac{dv_{GS}}{dv_{BS}} \right) \Big|_Q = \left(- \frac{di_D}{dV_T} \right) \left(\frac{dV_T}{dv_{BS}} \right) \Big|_Q = \frac{g_m \gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Small-Signal Model – Continued

Complete schematic model:



where

$$g_m \equiv \left. \frac{di_D}{dv_{GS}} \right|_Q =$$

$$\beta(V_{GS} - V_T) = \sqrt{2\beta I_D}$$

$$g_{ds} \equiv \left. \frac{di_D}{dv_{DS}} \right|_Q = \frac{\lambda I_D}{1 + \lambda v_{DS}} \approx \lambda I_D$$

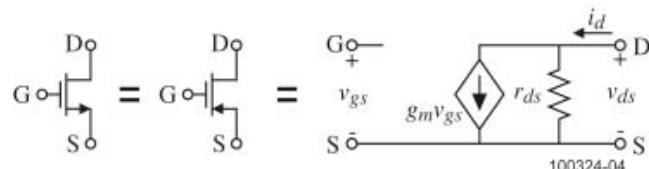
and

$$g_{mbs} \equiv \left. \frac{di_D}{dv_{BS}} \right|_Q = \left(\frac{\partial i_D}{\partial v_{GS}} \right) \left(\frac{\partial v_{GS}}{\partial v_{BS}} \right) \Big|_Q = \left(- \frac{\partial i_D}{\partial v_T} \right) \left(\frac{\partial v_T}{\partial v_{BS}} \right) \Big|_Q = \frac{g_m \gamma}{2\sqrt{2|\phi_F| - V_{BS}}} = \eta g_m$$

Simplified schematic model:

A very useful assumption:

$$g_m \approx 10g_{mbs} \approx 100g_{ds}$$



Small-Signal Model for other Regions

Active region:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \Big|_Q = \frac{K'WV_{DS}}{L} (1 + \lambda V_{DS}) \approx \left(\frac{K'W}{L} \right) V_{DS}$$

$$g_{mbs} = \frac{\partial i_D}{\partial v_{BS}} \Big|_Q = \frac{K'W\gamma V_{DS}}{2L\sqrt{2\phi_F - V_{BS}}}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \Big|_Q = \frac{K'W}{L} (V_{GS} - V_T - V_{DS})(1 + \lambda V_{DS}) + \frac{I_D \lambda}{1 + \lambda V_{DS}} \approx \frac{K'W}{L} (V_{GS} - V_T - V_{DS})$$

Note:

While the small-signal model analysis is independent of the region of operation, the evaluation of the small-signal performance is not.

Weak inversion region:

If $v_{DS} > 0$, then

$$i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \left(1 + \frac{v_{DS}}{V_A}\right)$$

Small-signal model:

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \Big|_Q = I_t \frac{W}{L} \frac{I_t}{nV_t} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \left(1 + \frac{v_{DS}}{V_A}\right) = \frac{I_D}{nV_t} = \frac{qI_D}{nkT} = \frac{I_D}{V_t} \frac{C_{ox}}{C_{ox} + C_{js}}$$

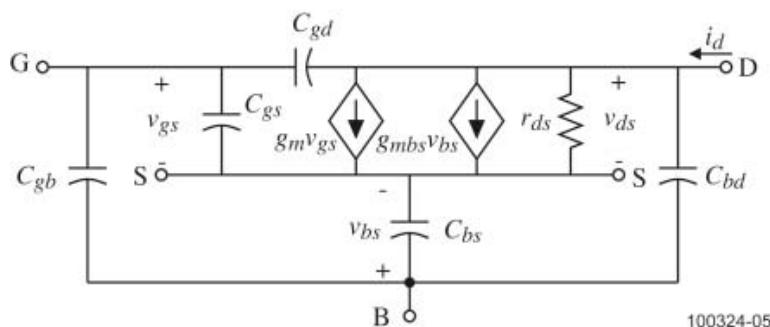
$$g_{ds} = \frac{\partial i_D}{\partial v_{DS}} \Big|_Q \approx \frac{I_D}{V_A}$$

FREQUENCY DEPENDENT SMALL SIGNAL MODEL

Small-Signal Frequency Dependent Model

The depletion capacitors are found by evaluating the large signal capacitors at the DC operating point.

The charge storage capacitors are constant for a specific region of operation.

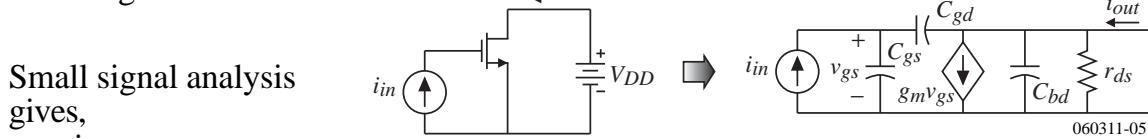


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Gain-bandwidth of the MOSFET (f_T)

The short-circuit current gain is measure of the frequency capability of the MOSFET.

Small signal model:



Small signal analysis gives,

$$i_{out} = g_m v_{gs} -$$

$$sC_{gd}v_{gs} \text{ and } v_{gs} = \frac{i_{in}}{s(C_{gs} + C_{gd})}$$

Therefore,

$$\frac{i_{out}}{i_{in}} = \frac{g_m - sC_{gd}}{s(C_{gs} + C_{gd})} \approx \frac{g_m}{s(C_{gs} + C_{gd})}$$

Assume $V_{SB} = 0$ and the MOSFET is in saturation,

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{1}{2\pi} \frac{g_m}{C_{gs}}$$

Recalling that

$$C_{gs} \approx \frac{2}{3} C_{ox} WL \quad \text{and} \quad g_m = \mu_o C_{ox} \frac{W}{L} (V_{GS} - V_T) \quad \rightarrow \quad f_T = \frac{3}{4\pi} \frac{\mu_o}{L^2} (V_{GS} - V_T)$$

For velocity saturation, $f_T \propto 1/L$.

NOISE MODELS

Derivation of the Thermal Noise Model

The noise model for the MOSFET is developed for the active region as follows:

In the active region, the channel resistance of the MOSFET is given from the simple large signal model as,

$$R_{channel} = \frac{1}{\left| \frac{\partial i_D}{\partial v_{DS}} \right|} = \frac{1}{\frac{K'W}{L} (V_{GS} - V_T - V_{DS})} \approx \frac{1}{\frac{K'W}{L} (V_{GS} - V_T)} = \frac{1}{g_m(\text{sat})}$$

In the saturation region, approximate the channel resistance as $2/3$ the value in the active region giving,

$$R_{channel}(\text{sat}) = \frac{2}{3g_m(\text{sat})} = \frac{2}{3g_m}$$

We know the current thermal noise spectral density of a resistor of value R is given as

$$i_n^2 = \frac{4kT}{R} (\text{A}^2/\text{Hz})$$

Substituting R by $R_{channel}(\text{sat})$ gives the drain current MOSFET thermal noise model as,

$$i_n^2 = \frac{8kTg_m}{3} (\text{A}^2/\text{Hz})$$

Translating this drain current noise to the gate voltage noise by dividing by g_m^2 gives

$$e_n^2 = \frac{8kT}{3g_m} (\text{V}^2/\text{Hz})$$

The Influence of the Back Gate on Thermal Noise

Using the derivation above, we can include the influence of the bulk-source voltage on the thermal noise as follows

$$R_{channel}(\text{sat}) = \frac{2}{3g_m(\text{eff})} = \frac{2}{3(g_m + g_{mbs})} = \frac{2}{3g_m(1 + \eta)}$$

where

$$\eta = \frac{g_{mbs}}{g_m}$$

Substituting R with $R_{channel}(\text{sat})$ gives the voltage and current noise spectral densities as,

$$e_n^2 = \frac{8kT}{3(g_m + g_{mbs})} (\text{V}^2/\text{Hz}) = \frac{8kT}{3g_m(1 + \eta)} (\text{V}^2/\text{Hz})$$

or

$$i_n^2 = \frac{8kT(g_m + g_{mbs})}{3} (\text{A}^2/\text{Hz}) = \frac{8kTg_m(1 + \eta)}{3} (\text{A}^2/\text{Hz})$$

1/f Noise Model

Another significant noise contribution to MOSFETs is a noise that is typically inversely proportional to frequency called the 1/f noise.

This 1/f noise spectral density is given as,

$$e_n^2 = \frac{KF}{2f^s C_{ox} W L K} \quad \text{or} \quad i_n^2 = \left[\frac{KF I_D}{f^s C_{ox} L^2} \right]$$

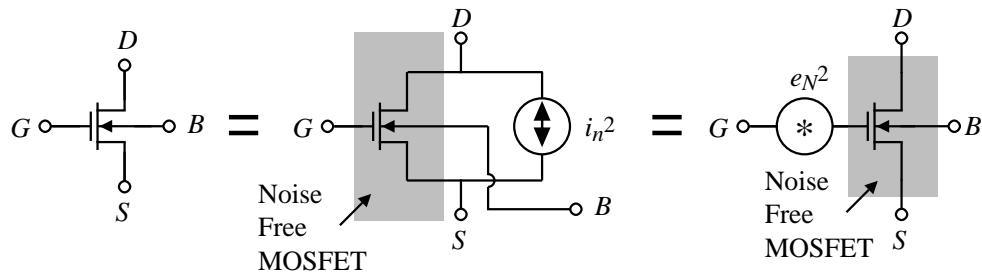
where

KF = Flicker noise coefficient

S = Slope factor of the 1/f noise

Although we do not have a good explanation for the reason why, the value of KF for a PMOS transistor is smaller than the value of KF for a NMOS transistor with the same current and W/L . The current will also influence the comparative 1/f noise of the NMOS and PMOS.

MOS Device Noise at Low Frequencies



where

$$i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{KF I_D}{f^s C_{ox} L^2} \right] \text{ (amperes}^2/\text{Hz)}$$

$$\eta = \frac{g_{mbs}}{g_m}$$

k = Boltzmann's constant

KF = Flicker noise coefficient

S = Slope factor of the 1/f noise

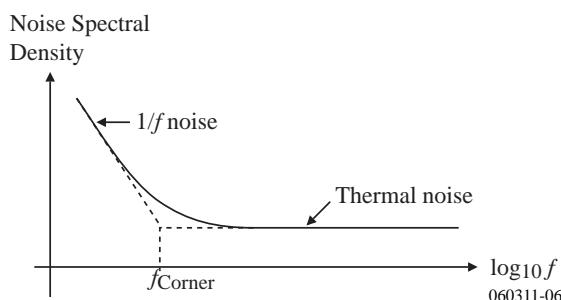
Reflecting the MOSFET Noise to the Gate

Dividing i_n^2 by g_m^2 gives the voltage noise spectral density as

$$e_n^2 = \frac{i_n^2}{g_m^2} = \left[\frac{8kT}{3g_m(1+\eta)} + \frac{KF}{2f^s C_{ox} W L K'} \right] \text{ (volts}^2/\text{Hz)}$$

It will be convenient to use $B = \frac{KF}{2C_{ox}K'}$ to simplify the notation.

Frequency response of MOSFET noise:



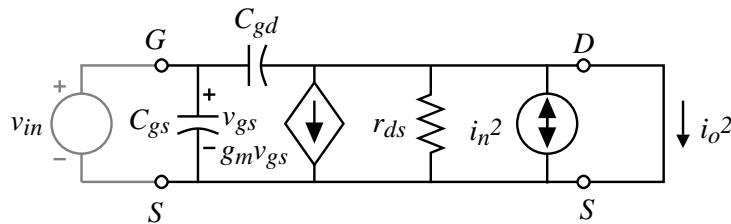
The 1/f corner frequency is:

$$\frac{8kT}{3g_m(1+\eta)} = \frac{KF}{2f^s C_{ox} W L K'} \Rightarrow f_{corner} \approx \frac{3g_m B}{8kT W L} \text{ if } g_{mbs} = 0$$

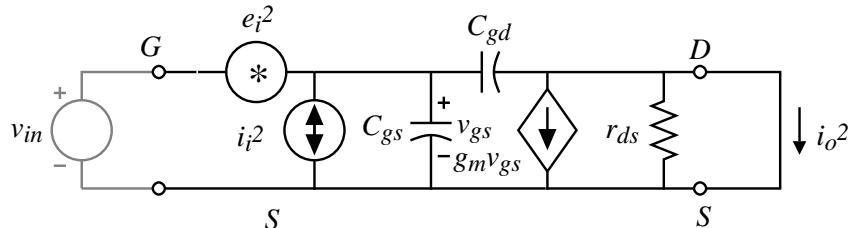
MOSFET Noise Model at High Frequencies

At high frequencies, the source resistance can no longer be assumed to be small. Therefore, a noise current generator at the input results.

MOSFET Noise Models:



Circuit 1: Frequency Dependent Noise Model



Circuit 2: Input-referenced Noise Model

MOSFET Noise Model at High Frequencies – Continued

To find e_i^2 and i_i^2 , we will perform the following calculations:

e_i^2 :

Short-circuit the input and find i_o^2 of both models and equate to get $\overline{e_i^2}$.

$$\begin{aligned} \text{Ckt. 1: } i_o^2 &= i_n^2 \\ \text{Ckt. 2: } i_o^2 &= g_m^2 e_i^2 + (\omega C_{gd})^2 e_i^2 \end{aligned} \quad \left\{ e_i^2 = \frac{i_n^2}{g_m^2 + (\omega C_{gd})^2} \right.$$

i_i^2 :

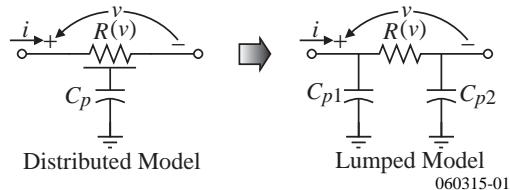
Open-circuit the input and find i_o^2 of both models and equate to get $\overline{i_i^2}$.

$$\text{Ckt. 1: } i_o^2 = i_n^2$$

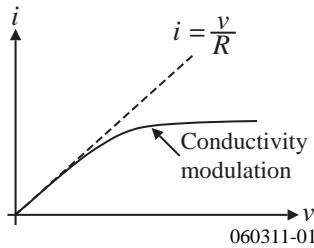
$$\begin{aligned} \text{Ckt. 2: } i_o^2 &= \left(\frac{(1/C_{gs})}{(1/C_{ds}) + (1/C_{gs})} \right)^2 i_i^2 + \frac{g_m^2 i_i^2}{\omega^2 (C_{gs} + C_{ds})^2} \\ &\approx \frac{g_m^2}{\omega^2 C_{gs}^2} i_n^2 \text{ if } C_{gd} < C_{gs} \Rightarrow i_i^2 = \frac{\omega^2 C_{gs}^2}{g_m^2} i_n^2 \end{aligned}$$

PASSIVE COMPONENT MODELS

Resistor Models



1.) Large signal



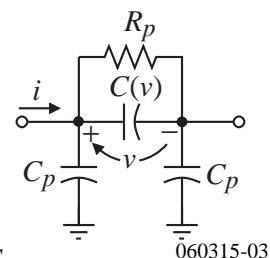
2.) Small signal

$$v = Ri$$

3.) Noise

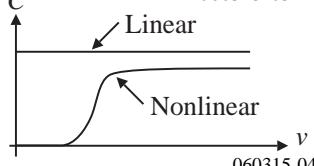
$$e_n^2 = 4kTR \quad \text{or} \quad i_n^2 = 4kTG$$

Capacitor Models



One of the parasitic capacitors is the top plate and the other is associated with the bottom plate.

1.) Large signal



2.) Small signal

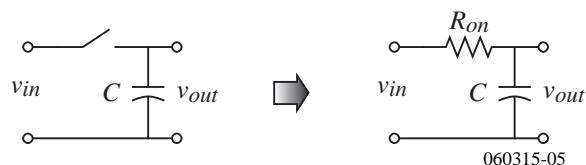
$$q = Cv \rightarrow i = C(dv/dt)$$

3.) Do capacitors have noise? See next page.

Switched Capacitor Circuits - kT/C Noise

Capacitors and switches generate an inherent thermal noise given by kT/C . This noise is verified as follows.

An equivalent circuit for a switched capacitor:



The noise voltage spectral density of switched capacitor above is given as

$$e_{R_{on}}^2 = 4kTR_{on} \text{ Volts}^2/\text{Hz} = \frac{2kTR_{on}}{\pi} \text{ Volt}^2/\text{Rad./sec.}$$

The rms noise voltage is found by integrating this spectral density from 0 to ∞ to give

$$v_{R_{on}}^2 = \frac{2kTR_{on}}{\pi} \int_0^{\infty} \frac{\omega_1^2 d\omega}{\omega_1^2 + \omega^2} = \frac{2kTR_{on}}{\pi} \left(\frac{\pi\omega_1}{2} \right) = \frac{kT}{C} \text{ Volts(rms)}^2$$

where $\omega_1 = 1/(R_{on}C)$. Note that the switch has an effective noise bandwidth of

$$f_{sw} = \frac{1}{4R_{on}C} \text{ Hz}$$

which is found by dividing the second relationship by the first.

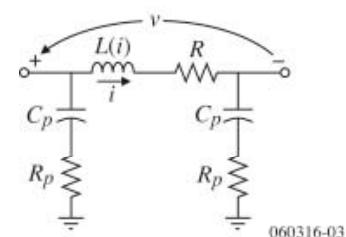
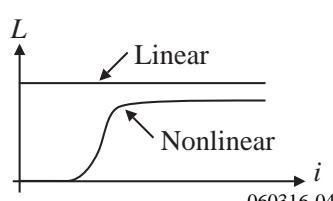
Inductor Models

R = losses of the inductor

C_p = parasitic capacitance to ground

R_p = losses due to eddy currents caused by magnetic flux

1.) Large Signal



2.) Small signal

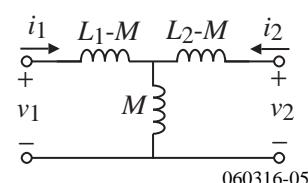
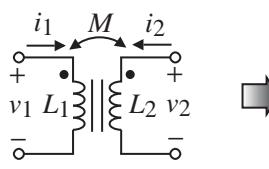
$$\psi = Li \rightarrow \frac{d\psi}{dt} = v = L \frac{di}{dt}$$

3.) Mutual inductance

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

$$k = \frac{M}{\sqrt{L_1 L_2}}$$



INTERCONNECTS

Types of “Wires”

1.) Metal

Many layers are available in today's technologies:

- Lower level metals have more resistance ($70 \text{ m}\Omega/\text{sq.}$)
- Upper level metal has the less resistance because it is thicker ($50 \text{ m}\Omega/\text{sq.}$)

2.) Polysilicon

Better resistor than conductor (unpolysicided) ($135\Omega/\text{sq.}$)

Silicided polysilicon has a lower resistance ($5\Omega/\text{sq.}$)

3.) Diffusion

Reasonable for connections if silicided ($5\Omega/\text{sq.}$)

Unsilicided ($55\Omega/\text{sq.}$)

4.) Vias

Vias are vertical metal (tungsten plugs or aluminum)

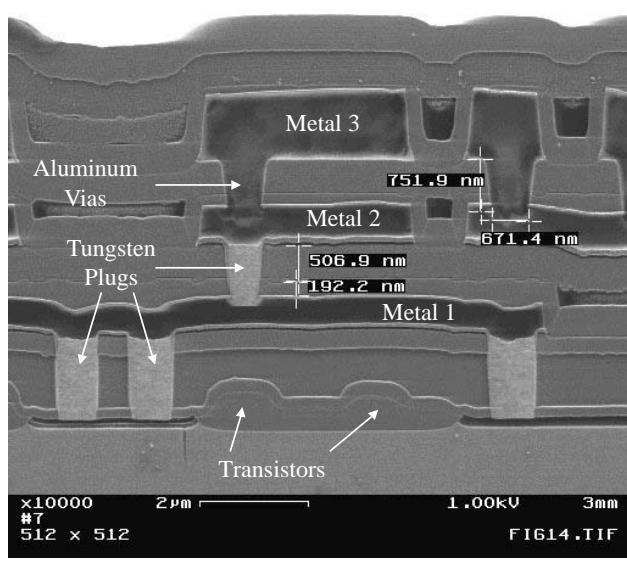
- Connect metal layer to metal layer ($3.5\Omega/\text{via}$)
- Connect metal to silicon or polysilicon contact resistance ($5\Omega/\text{contact}$)

Ohmic Contact Resistance

The metal to silicon contact generates resistance because of the presence of a potential barrier between the metal and the silicon.

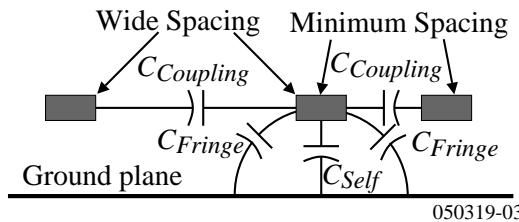
Contact and Via Resistance:

Contact System	Contact Resistance ($\Omega/\mu\text{m}^2$)
Al-Cu-Si to $160\Omega/\text{sq.}$ base	750
Al-Cu-Si to $5\Omega/\text{sq.}$ emitter	40
Al-Cu/Ti-W/PtSi to $160\Omega/\text{sq.}$ base	1250
Al-Cu/Al-Cu (Via)	5
Al-Cu/Ti-W/Al-Cu (Via)	5



Capacitance of Wires

Self, fringing and coupling capacitances:



Capacitance	Typical Value	Units
Metal to diffusion, Self capacitance	33	aF/ μm^2
Metal to diffusion, Fringe capacitance, minimum spacing	7	aF/ μm
Metal to diffusion, Fringe capacitance, wide spacing	40	aF/ μm
Metal to metal, Coupling capacitance, minimum spacing	85	aF/ μm
Metal to substrate, Self capacitance	28	aF/ μm^2
Metal to substrate, Fringe capacitance, minimum spacing	4	aF/ μm
Metal to substrate, Fringe capacitance, wide spacing	39	aF/ μm

Electromigration

Electromigration occurs if the current density is too large and the pressure of carrier collisions on the metal atoms causes a slow displacement of the metal.

Black's law:

$$\text{MTF} = \frac{1}{AJ^2} e^{(E_a/kT_j)}$$

Where

A = rate constant ($\text{cm}^4/\text{A}^2/\text{hr}$)

J = current density (A/cm^2)

E_a = activation energy in electron volts (0.5eV for Al and 0.7eV for Cu doped Al)

k = Boltzmann's constant (8.6×10^{-5} eV/K)

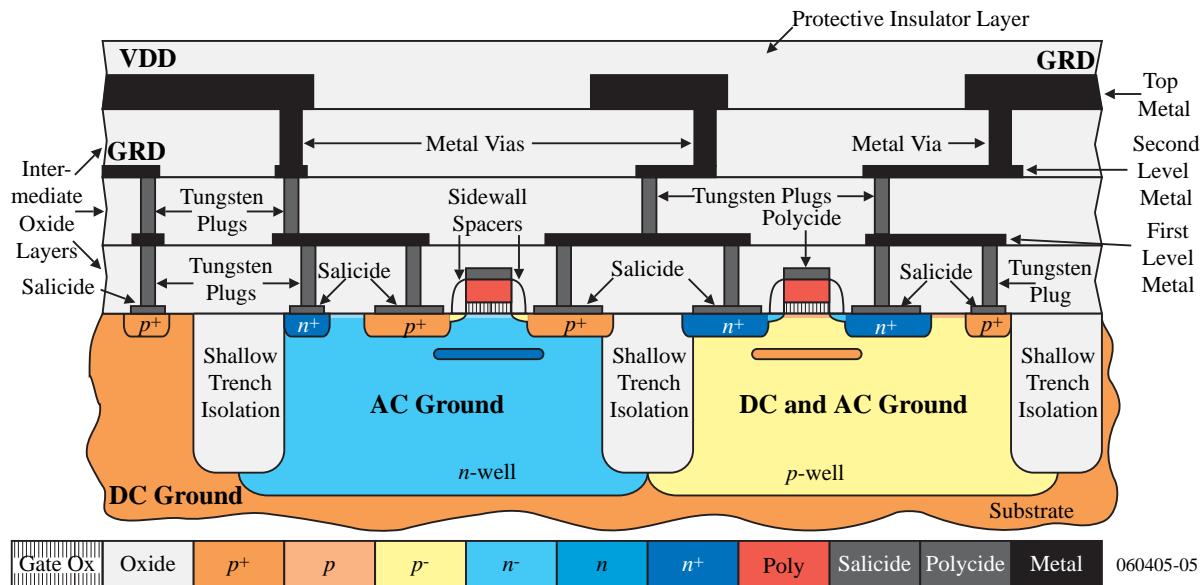
Electromigration leads to a maximum current density, J_{max} . J_{max} for copper doped aluminum is $5 \times 10^5 \text{ A}/\text{cm}^2$ at 85°C .

If $t = 10,000$ Angstroms and $J_{max} = 5 \times 10^5 \text{ A}/\text{cm}^2$, then a $10\mu\text{m}$ wide lead can conduct no more than 50mA at 85°C .



Where is AC Ground on the Chip?

AC grounds on the chip are any area tied to a fixed potential. This includes the substrate and the wells. *All parasitic capacitances are in reference to these points.*

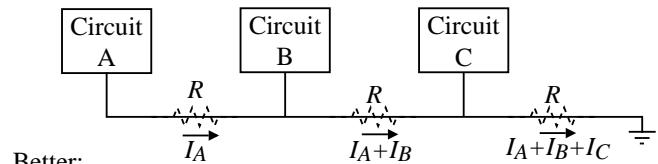


Grounds that are Not Grounds

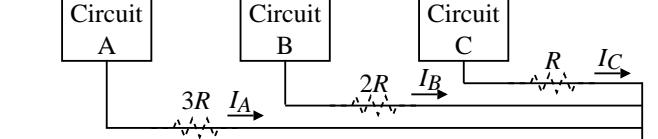
Because of the resistance of “wires”, current flowing through a wire can cause a voltage drop.

An example of good and bad practice:

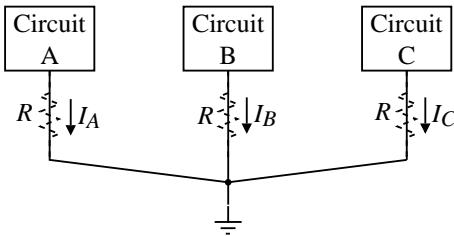
Bad:



Better:

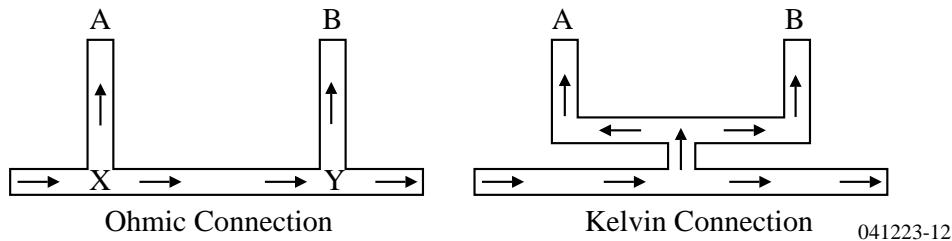


Best:



Kelvin Connections

Avoid unnecessary ohmic drops.



In the left-hand connection, an *IR* drop is experienced between *X* and *Y* causing the potentials at *A* and *B* to be slightly different.

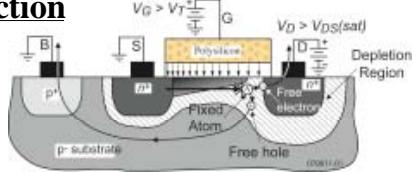
For example, let the current be $100\mu\text{A}$ and the metal be $30\text{m}\Omega/\text{sq}$. Suppose that the distance between X and Y is 100 squares. Therefore, the IR drop is

$$100\mu\text{A} \times 30\text{m}\Omega/\text{sq.} \times 100\text{sq.} = 0.3\text{mV}$$

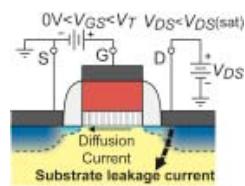
SUBSTRATE NOISE INTERFERENCE

Methods of Substrate Injection

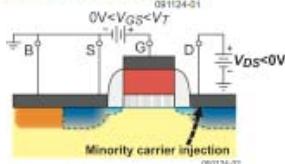
- Hot carrier



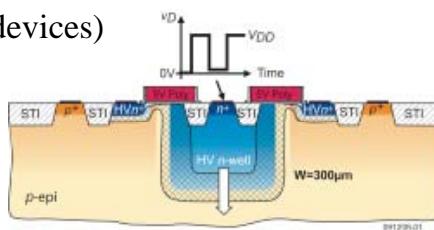
- Leakage



- Minority Carrier



- Displacement Current (large devices)



Other Methods of Substrate Injection

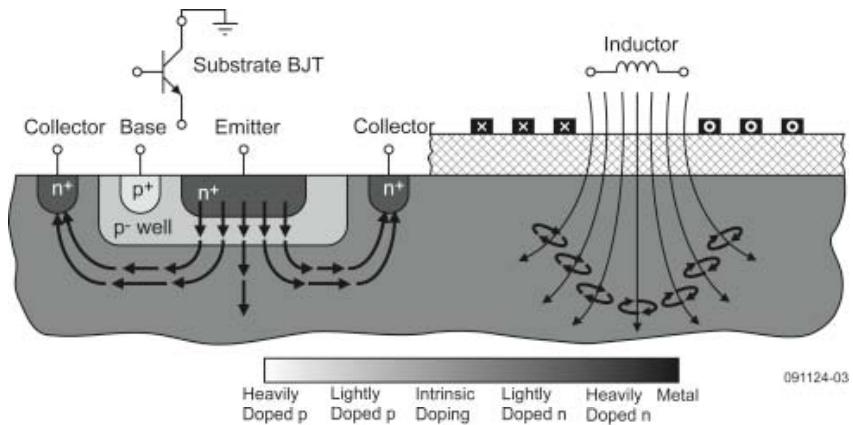


Illustration of Noise Interference Mechanism – No Epi

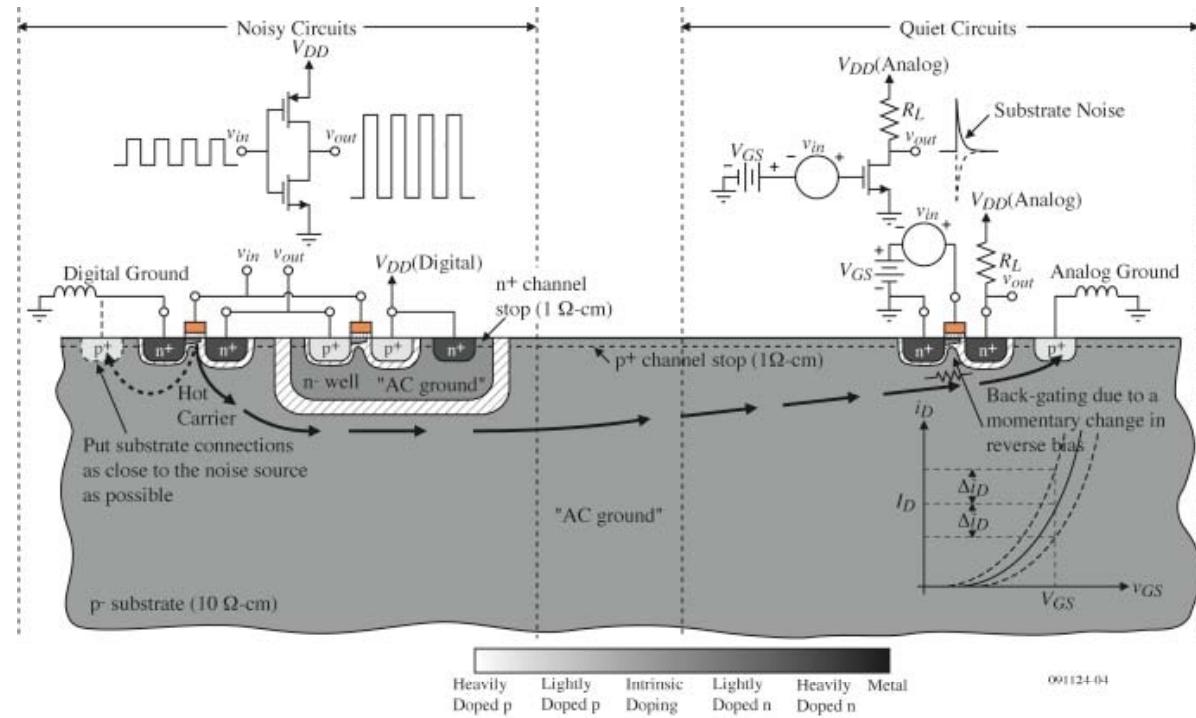
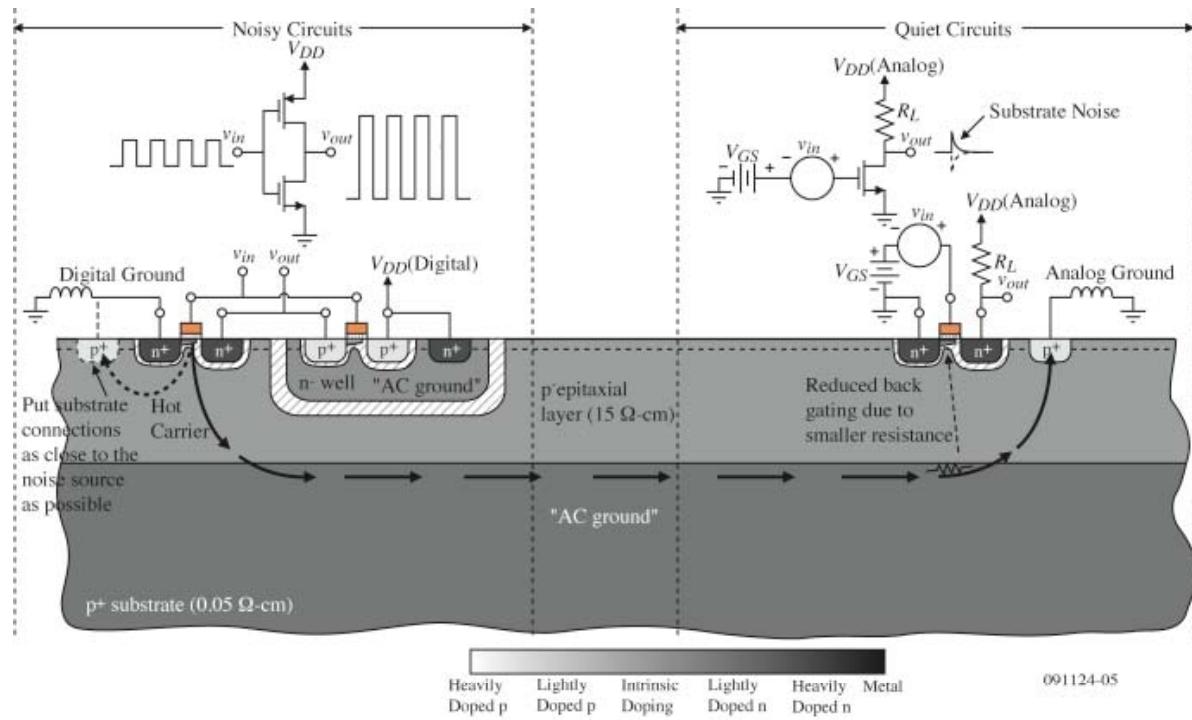


Illustration of Noise Interference Mechanism – With Epi



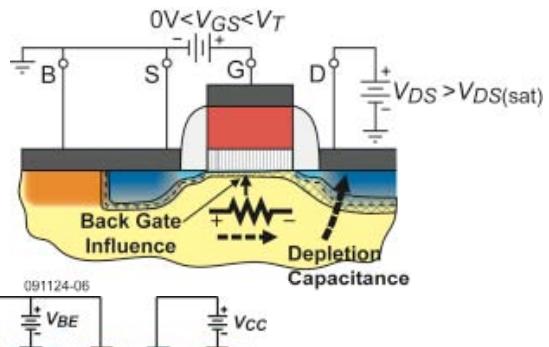
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How is Noise Injected into Components?

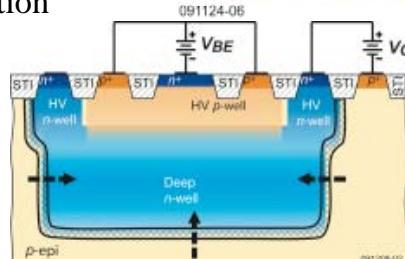
MOSFETs:

Injection occurs by the bulk effect on the threshold and across the depletion capacitance.

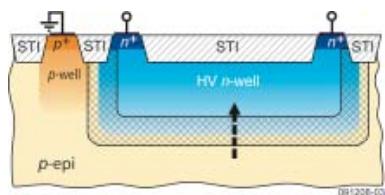


BJTs:

Injection primarily across the depletion capacitance.



Passives:

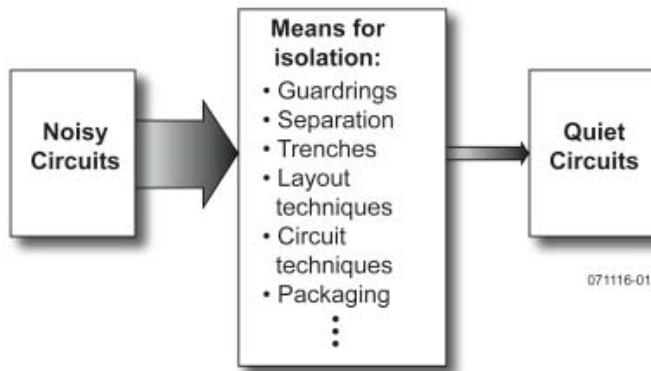


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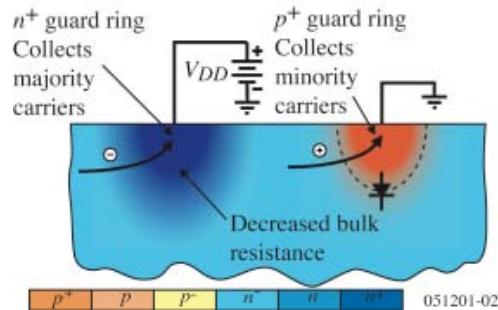
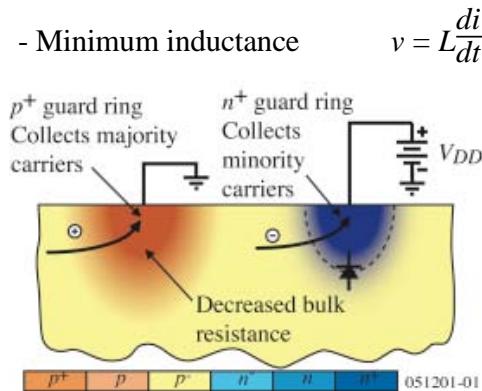
Isolation Techniques

Isolation techniques include both layout and circuit approaches to isolating quiet from noisy circuits.



Isolation Techniques – Guard Rings

- Collect the majority/minority carriers in the substrate
- Connect the guard rings to external potentials through conductors with
 - Minimum resistance
 - Minimum inductance



Isolation Techniques - Layout

Separation:

Physical separation – works well for non-epi, less for epi

Trenches:

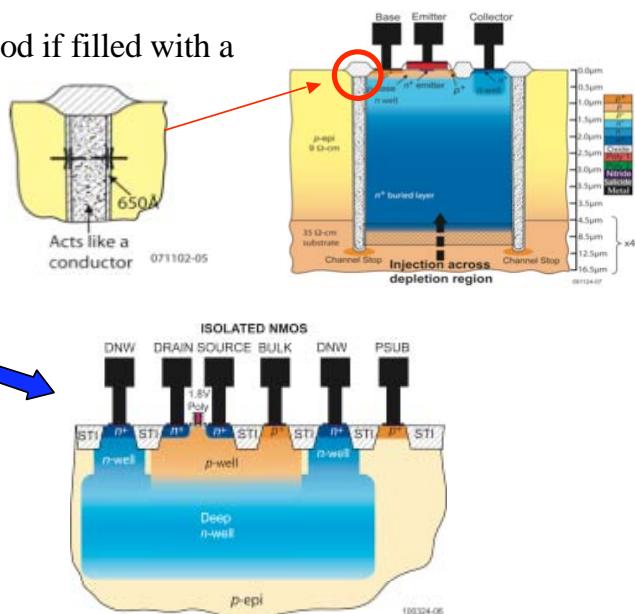
Good if filled with a dielectric, not good if filled with a conductor.

Layout:

Common centroid geometry does not help.

Keep contact and via resistance to a minimum.

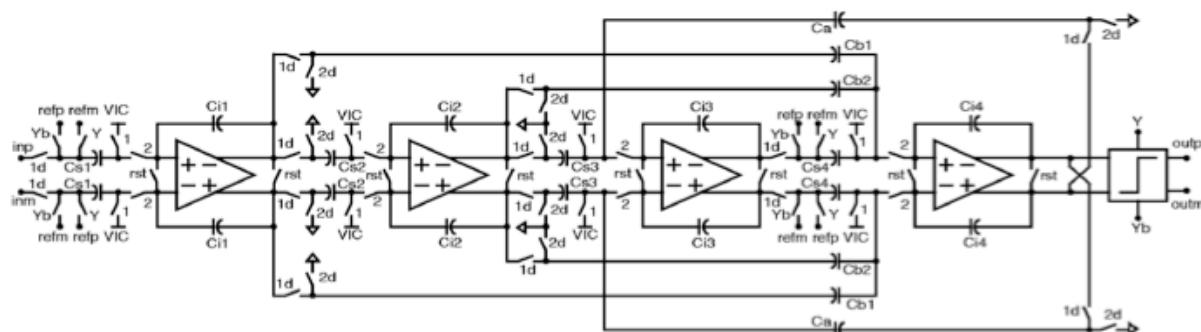
Wells help to isolate (deep n -well)



Isolation Techniques - Noise Insensitive Circuit Design

- Design for high power supply rejection ratio (PSRR)
- Correlated sampling techniques – eliminate low frequency noise
- Use “quiet” digital logic (power supply current remains constant)
- Use differential signal processing techniques.

Example of a 4th order Sigma Delta modulator using differential circuits:

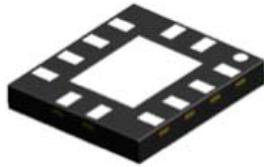


Noise Isolation Techniques - Reduction of Package Parasitics

- Keep the lead inductance to a minimum (multiple bond wires)
- Package selection

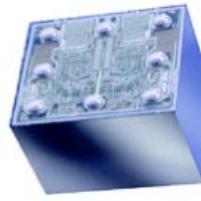
Package	Body Size (mm)	Lead Count	R (ohms)		L (nH)		M (nH)				C (pF)		C_{M12} (pF)	
			Corner	Center	Corner	Center	Corner	M12	M13	Center	Corner	Center	Corner	Center
QFP	28x28	208	0.90	0.65	12.00	8.00	8.00	6.50	5.50	4.50	0.20	0.06	1.00	0.60
	20x14	128	1.2	0.8	4.50	2.40	2.80	2.20	1.40	1.10	0.10	0.05	0.45	0.20
	12x12	80	0.36	0.28	2.90	2.40	2.30	1.60	1.30	0.90	0.15	0.10	0.27	0.20
LLP	All sizes	All	0.001	0.001	0.008	0.008	0.001	0.001	0.001	0.001	0.03	0.03	0.03	0.03
Mini SOIC	5x3	8	0.015	0.015	0.45	0.45	0.15	0.08	0.15	0.08	0.05	0.05	0.04	0.04
SC-70	2x1.25	5	0.015	-	0.045	-	0.08	0.05	-	-	0.06	-	0.06	-
SSOP	5.3x10.2	28	0.3	0.25	2.9	1.3	1.45	0.85	0.6	0.35	0.2	0.08	0.27	0.1
MDIP	19x6.35	14	0.15	0.05	7.0	3.0	2.5	1.8	1.0	0.7	0.65	0.25	1.1	0.4
μ SMD (small bumps)	All sizes	All	0.003	-	0.011	-	0.002	-	-	-	0.016	-	0.012	-
μ SMD (large bumps)	All sizes	All	0.002	-	0.013	-	0.002	-	-	-	0.016	-	0.012	-

Leadless lead frame:



Still has bond wires

Micro surface mount device:



Minimum inductance package

Summary of Substrate Interference

- Methods to reduce substrate noise
 - 1.) Physical separation
 - 2.) Guard rings placed close to the sensitive circuits with dedicated package pins.
 - 3.) Reduce the inductance in power supply and ground leads (best method)
 - 4.) Connect regions of constant potential (wells and substrate) to metal with as many contacts as possible.
- Noise Insensitive Circuit Design Techniques
 - 1.) Design for a high power supply rejection ratio (PSRR)
 - 2.) Use multiple devices spatially distinct and average the signal and noise.
 - 3.) Use “quiet” digital logic (power supply current remains constant)
 - 4.) Use differential signal processing techniques.
- Some references
 - 1.) D.K. Su, M.J. Loinaz, S. Masui and B.A. Wooley, “Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal IC’s,” *J. of Solid-State Circuits*, vol. 28, No. 4, April 1993, pp. 420-430.
 - 2.) K.M. Fukuda, T. Anbo, T. Tsukada, T. Matsuura and M. Hotta, “Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal ICs,” *J. of Solid-State Circuits*, vol. 31, No. 5, May 1996, pp. 726-731.
 - 3.) X. Aragones, J. Gonzalez and A. Rubio, *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs*, Kluwer Academic Publishers, Boston, MA, 1999.

SUMMARY

- Small signal models are a linear representation of the transistor electrical behavior
- Including the transistor capacitors in the small signal model gives frequency dependence
- Noise models include thermal and $1/f$ noise voltage or current spectral density models
- Passive component models include the nonlinearity, small signal and noise models
- Interconnects include metal, polysilicon, diffusion and vias
- Electromigration occurs if the current density is too large causing a displacement of metal
- Substrate interference is due to interaction between various parts of an integrated circuit via the substrate
- Method to reduce substrate interference include:
 - Physical separation
 - Guard rings
 - Reduced inductance in the power supply and ground leads
 - Appropriate contacts to the regions of constant potential
 - Reduce the source of interfering noise
 - Use differential signal processing techniques

LECTURE 120 – COMPONENT MATCHING

LECTURE ORGANIZATION

Outline

- Introduction
- Electrical matching
- Physical matching
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 56-59 and new material

INTRODUCTION

What is Accuracy and Matching?

The *accuracy* of a quantity specifies the difference between the actual value of the quantity and the ideal or true value of the quantity.

The *mismatch* between two quantities is the difference between the actual ratio of the quantities and the desired ratio of the two quantities.

Example:

x_1 = actual value of one quantity

x_2 = actual value of a second quantity

X_1 = desired value of the first quantity

X_2 = desired value of the second quantity

The accuracy of a quantity can be expressed as,

$$\text{Accuracy} = \frac{x - X}{X} = \frac{\Delta X}{X}$$

The mismatch, δ , can be expressed as,

$$\delta = \frac{\frac{x_2}{x_1} - \frac{X_2}{X_1}}{\frac{X_2}{X_1}} = \frac{\frac{X_1 x_2}{X_2 X_1} - 1}{\frac{X_2}{X_1}}$$

Relationship between Accuracy and Matching

Let:

$$\Delta X_1 = |x_1 - X_1| \rightarrow x_1 = X_1 \pm \Delta X_1$$

and

$$\Delta X_2 = |x_2 - X_2| \rightarrow x_2 = X_2 \pm \Delta X_2$$

Therefore, the mismatch can be expressed as,

$$\delta = \frac{X_1(X_2 \pm \Delta X_2)}{X_2(X_1 \pm \Delta X_1)} - 1 = \frac{1 \pm \frac{\Delta X_2}{X_2}}{1 \pm \frac{\Delta X_1}{X_1}} - 1 \approx \left(1 \pm \frac{\Delta X_2}{X_2}\right) \left(1 \mp \frac{\Delta X_1}{X_1}\right) - 1$$

$$\delta \approx 1 \pm \frac{\Delta X_2}{X_2} \mp \frac{\Delta X_1}{X_1} - 1 = \pm \frac{\Delta X_2}{X_2} + \frac{\Delta X_1}{X_1}$$

Thus, the mismatch is approximately equal to the difference in the accuracies of x_1 and x_2 assuming the deviations (ΔX) are small with respect to X .

Characterization of the Mismatch

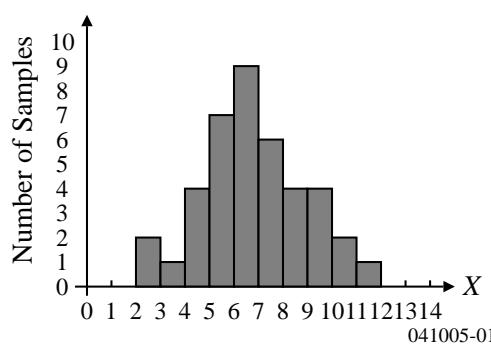
Mean of the mismatch for N samples-

$$m_\delta = \frac{1}{N} \sum_{i=1}^N \delta_i$$

Standard deviation of the mismatch for N samples-

$$s_\delta = \sigma = \sqrt{\frac{1}{N-1} \sum_{i=1}^N (\delta_i - m_\delta)^2}$$

Example:



$$m_\delta = \frac{253}{40} = 6.325$$

$$s_\delta = 2.115$$

Motivation for Matching of Components

The accuracy of analog signal processing is determined by the accuracy of gains and time constants. These accuracies are dependent upon:

Gain \propto Ratios of components or areas

Time constants \propto Products of components or areas

Ratio Accuracy?

$$\text{Actual Ratio} = \frac{X_1 \pm \Delta X_1}{X_2 \pm \Delta X_2} = \frac{X_1}{X_2} \left(\frac{1 \pm \frac{\Delta X_1}{X_1}}{1 \pm \frac{\Delta X_2}{X_2}} \right) \approx \frac{X_1}{X_2} \left(1 \pm \frac{\Delta X_1}{X_1} \right) \left(1 \pm \frac{\Delta X_2}{X_2} \right) \approx \frac{X_1}{X_2} \left(1 \pm \frac{\Delta X_1}{X_1} \mp \frac{\Delta X_2}{X_2} \right)$$

If X_1 and X_2 match ($\Delta X_1/X_1 \approx \Delta X_2/X_2$), then the actual ratio becomes the ideal ratio.

Product Accuracy?

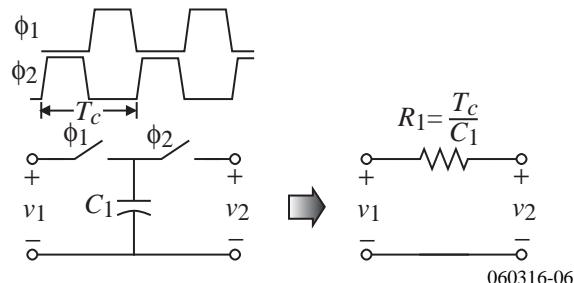
$$\text{Product accuracy} = (X_1 \pm \Delta X_1)(X_2 \pm \Delta X_2) = X_1 X_2 \left(1 \pm \frac{\Delta X_1}{X_1} \right) \left(1 \pm \frac{\Delta X_2}{X_2} \right) \approx X_1 X_2 \left(1 \pm \frac{\Delta X_1 \Delta X_2}{X_1 X_2} \right)$$

Unfortunately, the product cannot be accurately maintained in integrated circuits.

Switched Capacitor Circuits

Switched capacitor circuits offer a solution to the product accuracy problem.

A switched capacitor replacement of a resistor:



The product of a resistor, R_1 , and a capacitor, C_2 , now become,

$$R_1 C_2 = \left(\frac{T_c}{C_1} \right) C_2 = \left(\frac{1}{f_c C_1} \right) C_2 = \frac{C_2}{f_c C_1}$$

The accuracy of the time constant (product) now becomes,

$$\frac{C_2}{f_c C_1} \left(1 \pm \frac{\Delta C_2}{C_2} \mp \frac{\Delta C_1}{C_1} \mp \frac{\Delta f_c}{f_c} \right)$$

Assuming the clock frequency is accurate and larger than the signal bandwidth, then time constants in analog signal processing can be accurately matched by ratios of elements.

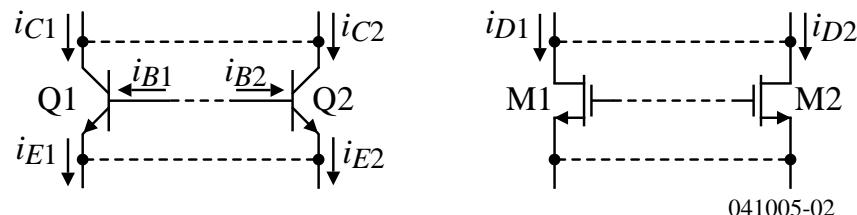
Types of Mismatches

- 1.) Those controlled or influenced by electrical design
 - Transistor operation
 - Circuit techniques
 - Correction/calibration techniques
- 2.) Those controlled or influenced by physical design
 - Random statistical fluctuations (microscopic fluctuations and irregularities)
 - Process bias (geometric variations)
 - Pattern shift (misalignment)
 - Diffusion interactions
 - Stress gradients and package shifts
 - Temperature gradients and thermoelectrics
 - Electrostatic interactions

ELECTRICAL MATCHING

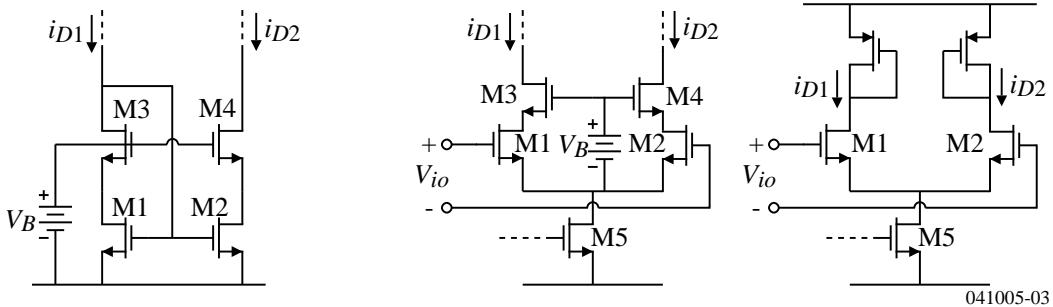
Matching Principle

Assume that two transistors are matched (large signal model parameters are equal). Then if all terminal voltages of one transistor are equal to the terminal voltages of the other transistor, then the terminal currents will be matched.



Note that the terminals may be physically connected together or at the same potential but not physically connected together.

Examples of the Matching Principle



Cascode current mirror:

The key transistors are M1 and M2. The gates and sources are physically connected and the drains are equal due to M3 and M4 gate-source drops. As a result, i_{D1} will be very close to i_{D2} .

Differential amplifier:

When i_{D1} and i_{D2} are equal, the fact that the drains of M1 and M2 are equal should give the smallest value of the input offset voltage, V_{io} .

Note: Since the drain voltages of M3 and M4 in both circuits are not necessarily equal, the gate-source voltages of M3 and M4 are not exactly equal which cause the drain voltages of M1 and M2 to not be exactly equal.

Gate-Source Matching

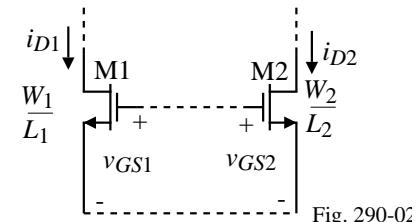
Not as precise as the previous principle but useful for biasing applications.

A. If the gate-source voltages of two or more FETs are equal and the FETs are matched and operating in the saturation region, then the currents are related by the W/L ratios of the individual FETs. The gate-source voltages may be directly or indirectly connected.

$$i_{D1} = \frac{K'W_1}{2L_1} (v_{GS1} - V_{T1})^2 \rightarrow (v_{GS1} - V_{T1})^2 = \frac{2K'i_{D1}}{(W_1/L_1)}$$

$$i_{D2} = \frac{K'W_2}{2L_2} (v_{GS2} - V_{T2})^2 \rightarrow (v_{GS2} - V_{T2})^2 = \frac{2K'i_{D2}}{(W_2/L_2)}$$

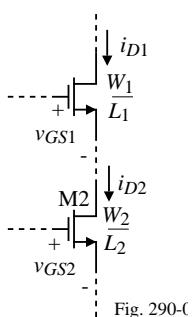
If $v_{GS1} = v_{GS2}$, then $\left(\frac{W_2}{L_2}\right) i_{D1} = \left(\frac{W_1}{L_1}\right) i_{D2}$ or $i_{D1} = \left(\frac{W_1/L_1}{W_2/L_2}\right) i_{D2}$



B. If the drain currents of two or more transistors are equal and the transistors are matched and operating in the saturation region, then the gate-source voltages are related by the W/L ratios (ignoring bulk effects).

If $i_{D1} = i_{D2}$, then

$$v_{GS1} = V_{T1} + \sqrt{\frac{W_2/L_2}{W_1/L_1}} (v_{GS2} - V_{T2}) \quad \text{or} \quad v_{GS1} = v_{GS2} \text{ if } \frac{W_2}{L_2} = \frac{W_1}{L_1}$$



Process Independent Biasing - MOSFET

The sensitivity of the bias points of all transistors depend on both the variation of the technological parameters and the accuracy of the biasing circuits.

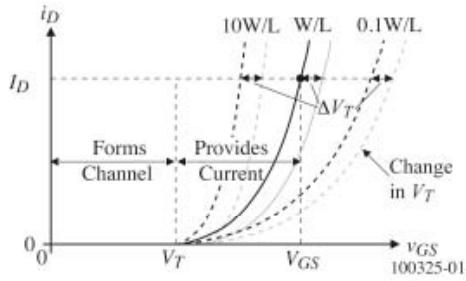
Gate-source voltage decomposition:

The gate-source voltage of the MOSFET can be divided into two parts:

- 1.) The part necessary to form or enhance the channel, V_T
- 2.) The part necessary to cause current to flow, $V_{GS} - V_T = V_{ON}$, called the overdrive.

This overdrive can be expressed,

$$V_{ON} = V_{DS(\text{sat})} = \sqrt{\frac{2I_D}{K'(W/L)}}$$



The dependence of the bias point on the technology, V_T , can be reduced by making $V_{ON} = V_{DS(\text{sat})} \gg V_T$.

This implies that small values of W/L are preferable. Unfortunately, this causes the transconductance to become small if the current remains the same.

Doubly Correlated Sampling

Illustration of the use of chopper stabilization to remove the undesired signal, v_u , from the desired signal, v_{in} . In this case, the undesired signal is the gate leakage current.

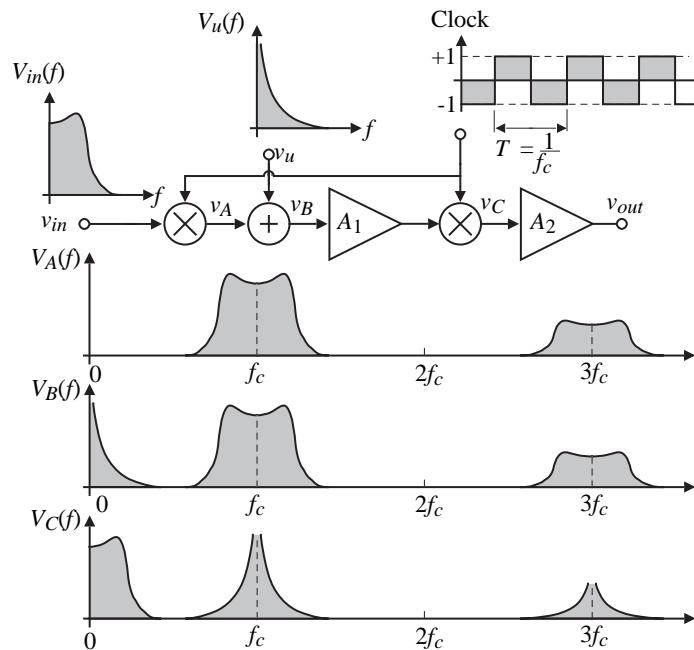
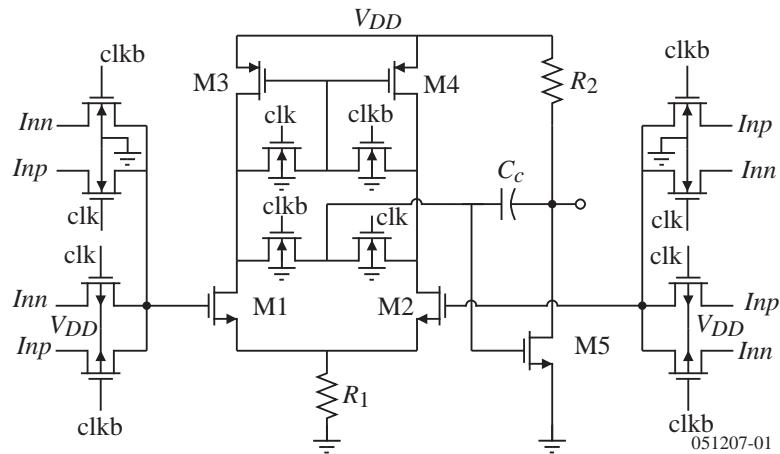


Fig. 7.5-8

An Op Amp Using Doubly Correlated Sampling to Remove DC Offsets



- Chopping with 50% duty cycle
- All switches use thick oxide devices to reduce gate leakage
- Gain $\approx g_m 1(r_{ds2} \parallel r_{ds4}) g_m 5 R_2$

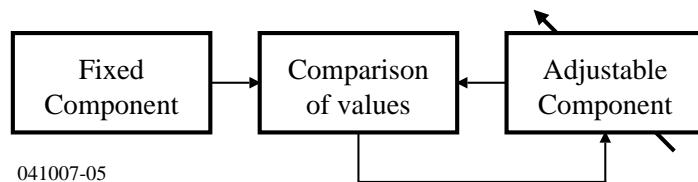
Will examine further in low noise op amps.

Self-Calibration Techniques

The objective of self-calibration is to increase the matching between two or more components (generally passive).

The requirements for self-calibration:

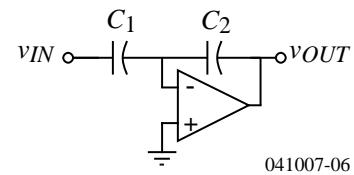
- 1.) A time interval in which to perform the calibration
- 2.) A means of adjusting the value of one or more of the components.



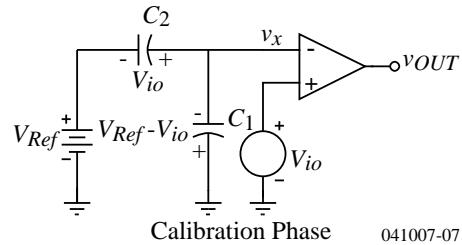
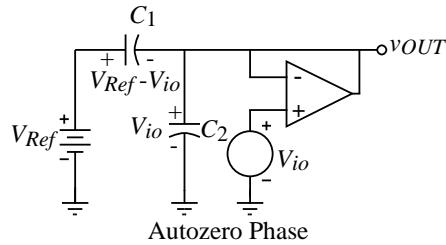
Self-calibration can typically improve the matching by a factor of 2-3 bits (4-8).

Example of Capacitor Self-Calibration

Consider the charge amplifier below that should have a gain of unity.



Assume the amplifier has a DC input offset voltage of V_{io} . The following shows how to calibrate one (or both) of the capacitors.



In the calibration phase, v_x , is:

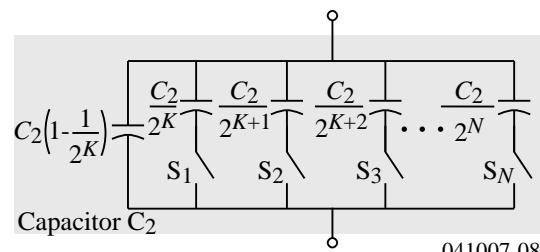
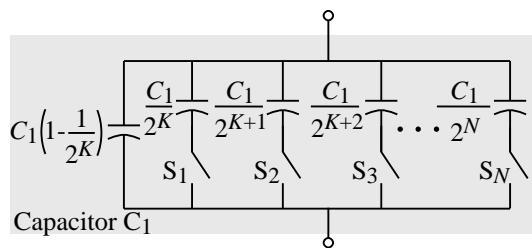
$$v_x = (V_{REF} - V_{io}) \left(\frac{C_2}{C_1 + C_2} \right) - (V_{REF} - V_{io}) \left(\frac{C_1}{C_1 + C_2} \right) = (V_{REF} - V_{io}) \left(\frac{C_2 - C_1}{C_1 + C_2} \right)$$

The correction circuitry varies C_1 or C_2 until $v_x = 0$ as observed by v_{OUT} .

Variable Components

The correction circuitry should be controlled by logic circuits so that the correction can be placed into memory to maintain the calibration of the circuit during application.

Implementation for C_1 and C_2 of the previous example:



K is selected to achieve the desired tolerance or variation

N is selected to achieve the desired resolution ($N > K$)

Additional circuitry:

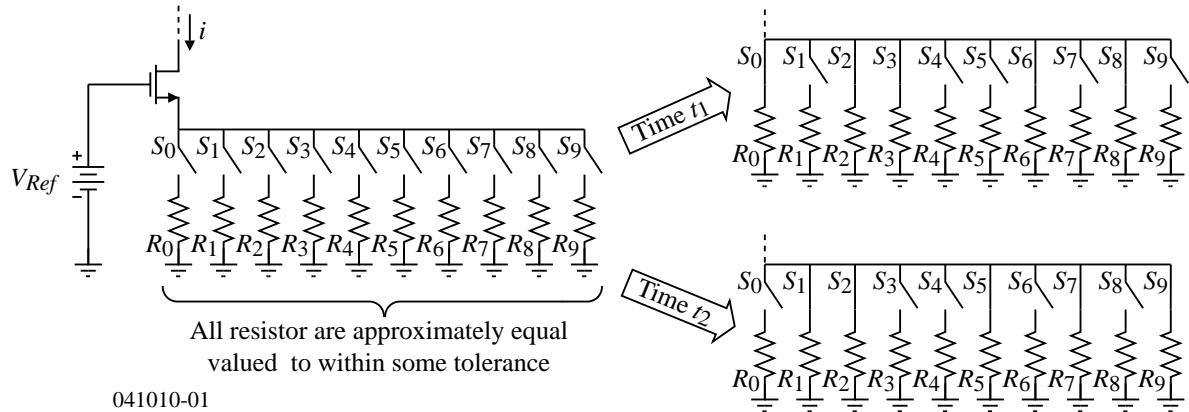
Every self-calibration system will need additional logic circuits to sense when the value of v_x changes from positive to negative (or vice versa) and to store the switch settings in memory to maintain the calibration.

Basics of Dynamic Element Matching[†]

Dynamic element matching chooses different, approximately equal-valued elements to represent a more precise value of a component as a function of time.

Goal of dynamic element matching:

Convert the error due to element mismatch from a dc offset into an ac signal of equivalent power which can be removed by the appropriate means (doubly-correlated sampling, highpass filtering of a sigma-delta modulator, etc.)



[†] L. R. Carley, "A Noise-Shaping Coder Topology for 15+ Bit Converters, *IEEE J. of Solid-State Circuits*, vol. 24, no. 2, April 1989, pp. 267-273.
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How Dynamic Element Matching Works

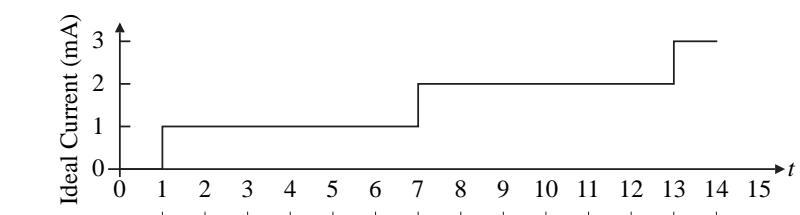
Assume that we have three approximately equal elements with the following currents:

Element 1 = 0.99mA

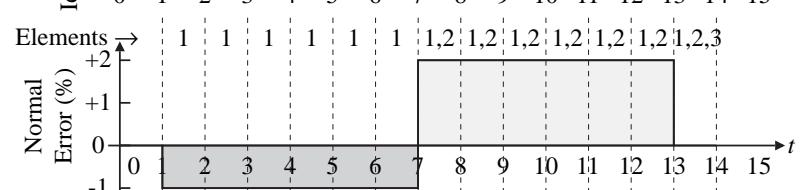
Element 2 = 1.03mA

Element 3 = 0.98mA

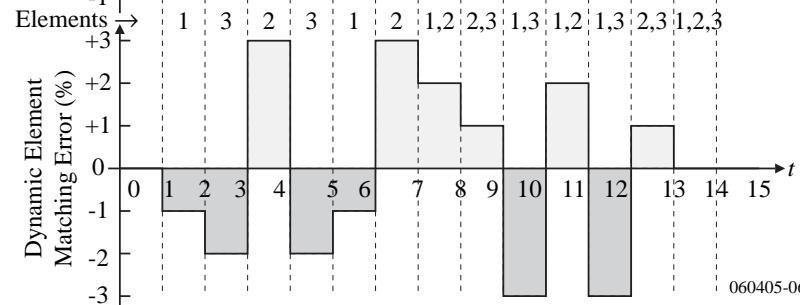
Ideal current output level →



Error when dynamic element matching is not → used

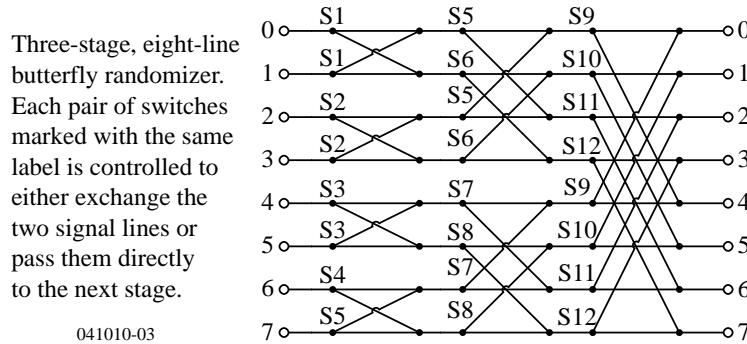


Error when dynamic element matching is used →



Issues of Dynamic Element Matching

- The selection of the elements must be truly random for the maximum benefit to occur.
- If the number of elements is large this can be an overwhelming task to implement. An approximation to random selection is the butterfly-type randomizer below:



- When using the dynamic element technique, one needs to be careful that the averaging activity of the dynamic element matching process does not interfere with other averaging processes that might be occurring simultaneously (i.e. $\Sigma\Delta$ modulators).
- Other references:
 - 1.) B.H. Leung and s. Sutarja, "Multibit $\Sigma\Delta$ A/D Converter Incorporating A Novel Class of Dynamic Element Matching Techniques," *IEEE Trans. on Circuits and Systems-II*, vol. 39, no. 1, Jan. 1992, pp. 35-51.
 - 2.) R. Baird and T. Fiez, "Linearity Enhancement of Multibit $\Delta\text{-}\Sigma$ A/D and D/A Converters Using Data Weighted Averaging," *IEEE Trans. on Circuits and Systems-II*, vol. 42, no. 12, Dec. 1995, pp. 753-762.

PHYSICAL MATCHING

Review of Physical Matching

We have examined these topics in previous lectures. To summarize, the sources of physical mismatch are:

- Random statistical fluctuations (microscopic fluctuations and irregularities)
- Process bias (geometric variations)
- Pattern shift (misalignment)
- Diffusion interactions
- Stress gradients and package shifts
- Temperature gradients and thermoelectrics
- Electrostatic interactions

Rules for Resistor Matching[†]

- 1.) Construct matched resistors from the same material.
- 2.) Make matched resistors the same width.
- 3.) Make matched resistors sufficiently wide.
- 4.) Where practical, use identical geometries for resistors (replication principle)
- 5.) Orient resistors in the same direction.
- 6.) Place matched resistors in close physical proximity.
- 7.) Interdigitate arrayed resistors.
- 8.) Place dummy resistors on either end of a resistor array.
- 9.) Avoid short resistor segments.
- 10.) Connect matched resistors in order to cancel thermoelectrics.
- 11.) If possible place matched resistors in a low stress area (minimize piezoresistance).
- 12.) Place matched resistors well away from power devices.
- 13.) Place precisely matched resistors on the axes of symmetry of the die.
- 14.) Consider the influence of tank modulation for HSR resistors (the voltage modulation of the reverse-biased depletion region changes the sheet resistivity).
- 15.) Sectioned resistors are superior to serpentine resistors.

[†] Alan Hastings, *Art of Analog Layout*, 2nd ed, 2006, Pearson Prentice Hall, New Jersey
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Rules for Resistor Matching – Continued

- 16.) Use poly resistors in preference to diffused resistors.
- 17.) Do not allow the buried layer shadow to intersect matched diffused resistors.
- 18.) Use electrostatic shielding where necessary.
- 19.) Do not route unconnected metal over matched resistors.
- 20.) Avoid excessive power dissipation in matched resistors.

Rules for Capacitor Matching[†]

- 1.) Use identical geometries for matched capacitors (replication principle).
- 2.) Use square or octagonal geometries for precisely matched capacitors.
- 3.) Make matched capacitors as large as possible.
- 4.) Place matched capacitors adjacent to one another.
- 5.) Place matched capacitors over field oxide.
- 6.) Connect the upper electrode of a matched capacitor to the higher-impedance node.
- 7.) Place dummy capacitors around the outer edge of the array.
- 8.) Electrostatically shield matched capacitors.
- 9.) Cross-couple arrayed matched capacitors.
- 10.) Account for the influence of the leads connecting to matched capacitors.
- 11.) Do not run leads over matched capacitors unless they are electrostatically shielded.
- 12.) Use thick-oxide dielectrics in preference to thin-oxide or composite dielectrics.
- 13.) If possible, place matched capacitors in areas of low stress gradients.
- 14.) Place matched capacitors well away from power devices.
- 15.) Place precisely matched capacitors on the axes of symmetry for the die.

[†] Alan Hastings, *Art of Analog Layout*, 2nd ed., 2006, Pearson Prentice Hall, New Jersey
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Mismatched Transistors

Assume two transistors have $v_{DS1} = v_{DS2}$, $K_1' \neq K_2'$ and $V_{T1} \neq V_{T2}$. Therefore we have

$$\frac{i_O}{i_I} = \frac{K_2'(v_{GS} - V_{T2})^2}{K_1'(v_{GS} - V_{T1})^2}$$

How do you analyze the mismatch? Use plus and minus worst case approach. Define $\Delta K' = K_2' - K_1'$ and $K' = 0.5(K_2' + K_1')$ $\Rightarrow K_1' = K' - 0.5\Delta K'$ and $K_2' = K' + 0.5\Delta K'$
 $\Delta V_T = V_{T2} - V_{T1}$ and $V_T = 0.5(V_{T1} + V_{T2}) \Rightarrow V_{T1} = V_T - 0.5\Delta V_T$ and $V_{T2} = V_T + 0.5\Delta V_T$

Substituting these terms into the above equation gives,

$$\frac{i_O}{i_I} = \frac{(K' + 0.5\Delta K')(v_{GS} - V_T - 0.5\Delta V_T)^2}{(K' - 0.5\Delta K')(v_{GS} - V_T + 0.5\Delta V_T)^2} = \frac{\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}$$

Assuming that the terms added to or subtracted from “1” are smaller than unity gives

$$\frac{i_O}{i_I} \approx \left(1 + \frac{\Delta K'}{2K'}\right)\left(1 + \frac{\Delta K'}{2K'}\right)\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2\left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2 \approx 1 + \frac{\Delta K'}{K'} - \frac{2\Delta V_T}{(v_{GS} - V_T)}$$

If $\Delta K'/K' = \pm 5\%$ and $\Delta V_T/(v_{GS} - V_T) = \pm 10\%$, then $i_O/i_I \approx 1 \pm 0.05 \pm (-0.20) = 1 \pm (0.25)$

Geometric Effects

How does the size and shape of the transistor effect its matching?

Gate Area:

$$\sigma_{V_{th}} = \frac{C_{V_{th}}}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{K_p} = K' \frac{C_{K_p}}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{\Delta W/W} = \frac{C_{\Delta W/W}}{\sqrt{W_{eff}L_{eff}}}$$

where $C_{V_{th}}$, C_{K_p} and $C_{\Delta W/W}$ are constants determined by measurement.

Values from a $0.35\mu m$ CMOS technology:

$$\sigma_{V_{th,NMOS}} = \frac{10.6 \text{mV}\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}} \quad \sigma_{V_{th,PMOS}} = \frac{8.25 \text{mV}\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}}$$

and

$$\sigma\left(\frac{\Delta W}{W}\right)_{NMOS} = \frac{0.0056\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}} \quad \sigma\left(\frac{\Delta W}{W}\right)_{PMOS} = \frac{0.0011\cdot\mu\text{m}}{\sqrt{W_{eff}L_{eff}}}$$

The above results suggest that PMOS devices would be better matched than NMOS devices in this technology.

Pelgrom's Law

Spatial Averaging: Local and random variations decrease as the device size increases, since the parameters “average out” over a greater area.

Pelgrom's Law:

$$s^2(\Delta P) = \frac{A_p^2}{WL} + S_p^2 D_x^2$$

where,

ΔP = mismatch in a parameter, P

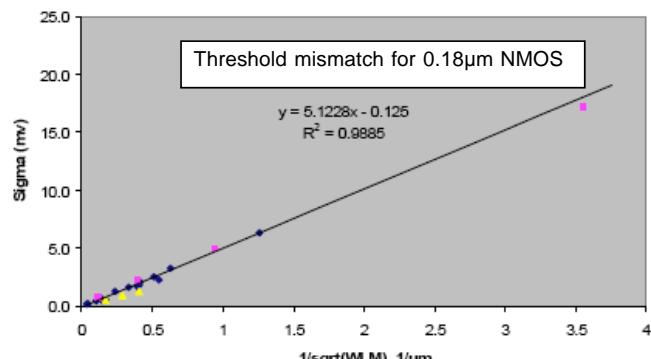
WL = width times the length of the device (effective Pelgrom area)

A_p = proportionality constant between the standard deviation of ΔP and the area of the device

D_x = distance between the matched devices

S_p = proportionality constant between the standard deviation of ΔP and D_x

As D_x becomes large, the standard deviation tends to infinity which is not realistic.



Rules for Transistor Matching[†]

- 1.) Use identical finger geometries.
- 2.) Use large active areas.
- 3.) For voltage matching, keep $V_{GS} - V_T$, small (i.e. 0.1V).
- 4.) For current matching, keep $V_{GS} - V_T$, large (i.e. 0.5V).
- 5.) Orient the transistors in the same direction.
- 6.) Place the transistors in close proximity to each other.
- 7.) Keep the layout of the matched transistors as compact as possible.
- 8.) Where practical use common centroid geometry layouts.
- 9.) Place dummy segments on the ends of arrayed transistors.
- 10.) Avoid using very short or narrow transistors.
- 11.) Place transistors in areas of low stress gradients.
- 12.) Do not place contacts on top of active gate area.
- 13.) Keep junctions of deep diffusions as far away from the active gate area as possible.
- 14.) Do not route metal across the active gate region.
- 15.) Place precisely matched transistors on the axes of symmetry of the die.
- 16.) Do not allow the buried layer shadow to intersect the active gate area.
- 17.) Connect gate fingers using metal connections.

[†] Alan Hastings, *Art of Analog Layout*, 2nd ed., 2006, Pearson Prentice Hall, New Jersey
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SUMMARY

- IC technology offers poor absolute values but good relative values or matching
- In analog circuits, gains are determined by ratios (good matching) and time constants are determined by products (poor matching)
- Electrical matching is determined in the electrical design phase
 - Matching due to equal terminal voltages
 - Matching due to process independent biasing
 - Doubly correlated sampling
 - Self-calibration techniques
 - Dynamic element matching
- Physical matching is determined in the physical design phase
 - Random statistical fluctuations (microscopic fluctuations and irregularities)
 - Process bias (geometric variations)
 - Pattern shift (misalignment)
 - Diffusion interactions
 - Stress gradients and package shifts
 - Temperature gradients and thermoelectrics
 - Electrostatic interactions

LECTURE 130 – COMPUTER MODELS AND EXTRACTION OF THE SIMPLE LARGE SIGNAL MODEL

LECTURE ORGANIZATION

Outline

- Computer Models
- Extraction of a large signal model for hand calculations
- Extraction of the simple model for short channel MOSFETs
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 92-97 and 744-753

COMPUTER MODELS

FET Model Generations

- First Generation – Physically based analytical model including all geometry dependence.
- Second Generation – Model equations became subject to mathematical conditioning for circuit simulation. Use of empirical relationships and parameter extraction.
- Third Generation – A return to simpler model structure with reduced number of parameters which are physically based rather than empirical. Uses better methods of mathematical conditioning for simulation including more specialized smoothing functions.

Performance Comparison of Models (from Cheng and Hu, *MOSFET Modeling & BSIM: Users Guide*)

Model	Minimum L (μm)	Minimum Tox (nm)	Model Continuity	i_D Accuracy in Strong Inversion	i_D Accuracy in Subthreshold	Small signal parameter	Scalability
MOS1	5	50	Poor	Poor	Not Modeled	Poor	Poor
MOS2	2	25	Poor	Poor	Poor	Poor	Fair
MOS3	1	20	Poor	Fair	Poor	Poor	Poor
BSIM1	0.8	15	Fair	Good	Fair	Poor	Fair
BSIM2	0.35	7.5	Fair	Good	Good	Fair	Fair
BSIM3v2	0.25	5	Fair	Good	Good	Good	Good
BSIM3v3	0.15	4	Good	Good	Good	Good	Good

First Generation Models

Level 1 (MOS1)

- Basic square law model based on the gradual channel approximation and the square law for saturated drain current.
- Good for hand analysis.
- Needs improvement for deep-submicron technology (must incorporate the square law to linear shift)

Level 2 (MOS2)

- First attempt to include small geometry effects
- Inclusion of the channel-bulk depletion charge results in the familiar 3/2 power terms
- Introduced a simple subthreshold model which was not continuous with the strong inversion model.
- Model became quite complicated and probably is best known as a “developing ground” for better modeling techniques.

Level 3 (MOS3)

- Used to overcome the limitations of Level 2. Made use of a semi-empirical approach.
- Added DIBL and the reduction of mobility by the lateral field.
- Similar to Level 2 but considerably more efficient.
- Used binning but was poorly implemented.

Second Generation Models

BSIM (Berkeley Short-Channel IGFET Model)

- Emphasis is on mathematical conditioning for circuit simulation
- Short channel models are mostly empirical and shifts the modeling to the parameter extraction capability
- Introduced a more detailed subthreshold current model with good continuity
- Poor modeling of channel conductance

HSPICE Level 28

- Based on BSIM but has been extensively modified.
- More suitable for analog circuit design
- Uses model binning
- Model parameter set is almost entirely empirical
- User is locked into HSPICE
- Model is proprietary

BSIM2

- Closely based on BSIM
- Employs several expressions developed from two dimensional analysis
- Makes extensive modifications to the BSIM model for mobility and the drain current
- Uses a new subthreshold model
- Output conductance model makes the model very suitable for analog circuit design

Third Generation Models

BSIM2 – Continued

- The drain current model is more accurate and provides better convergence
- Becomes more complex with a large number of parameters
- No provisions for variations in the operating temperature

BSIM3

- This model has achieved stability and is being widely used in industry for deep submicron technology.
- Initial focus of simplicity was not realized.

MOS Model 9

- Developed at Philips Laboratory
- Has extensive heritage of industrial use
- Model equations are clean and simple – should be efficient

Other Candidates

- EKV (Enz-Krummenacher-Vittoz) – fresh approach well suited to the needs of analog circuit design

BSIM2 Model

Generic composite expression for the model parameters:

$$X = X_0 + \frac{LX}{L_{eff}} + \frac{WX}{W_{eff}}$$

where

X_0 = parameter for a given W and L

LX (WX) = first-order dependence of X on L (W)

Modeling features of BSIM2:

Mobility

- Mobility reduction by the vertical and the lateral field

Drain Current

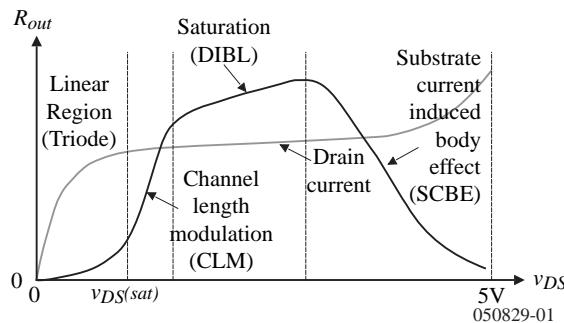
- Velocity saturation
- Linear region drain current
- Saturation region drain current
- Subthreshold current

$$i_{DS} = \frac{\mu_0 C_{ox} W_{eff}}{L_{eff}} \cdot \left(\frac{kT}{q} \right) \frac{e^{v_{GS} - V_t - V_{off}}}{n} \cdot [1 - e^{qV_{DS}/kT}]$$

where

$$V_{off} = V_{OF} + V_{OFB} \cdot v_{BS} + V_{OFD} \cdot v_{DS} \quad \text{and} \quad n = NO + \frac{NB}{\sqrt{PHI - v_{BS}}} + ND \cdot v_{DS}$$

BSIM2 Output Conductance Model



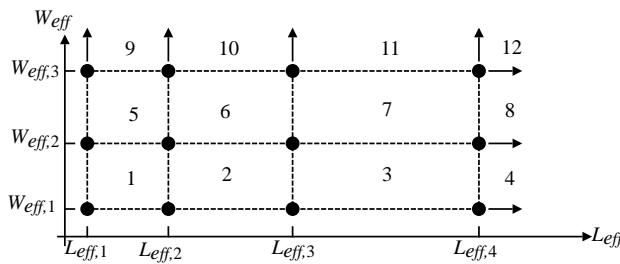
- Drain-Induced Barrier Lowering (DIBL) – Lowering of the potential barrier at the source-bulk junction allowing carriers to traverse the channel at a lower gate bias than would otherwise be expected.
- Substrate Current-Induced Body Effect (SCBE) – The high field near the drain accelerates carriers to high energies resulting in impact ionization which generates a hole-electron pair (hot carrier generation). The opposite carriers are swept into the substrate and have the effect of slightly forward-biasing the source-substrate junction. This reduces the threshold voltage and increases the drain current.

Charge Model

- Eliminates the partitioning choice (50%/50% is used)
- BSIM charge model better documented with more options

BSIM2 Basic Parameter Extraction

- A number of devices with different W/L are fabricated and measured



- A long, wide device is used as the base to add geometry effects as corrections.
- Procedure:
 - 1.) Oxide thickness and the differences between the drawn and effective channel dimensions are provided as process input.
 - 2.) A long, wide device is used to determine some base parameters which are used as the starting point for each individual device extraction in the second phase.
 - 3.) In the second phase, a set of parameters is extracted independently for each device. This phase represents the fitting of the data for each independent device to the intrinsic equation structure of the model
 - 4.) In the third phase, the compiled parameters from the second phase are used to determine the geometry parameters. This represents the imposition of the extrinsic structure onto the model.

BSIM3 Model

The background for the BSIM3 model and the equations are given in detail in the text *MOSFET Modeling & BSIM3 User's Guide*, by Y. Cheng and C. Hu, Kluwer Academic Publishers, 1999.

The short channel effects included in the BSIM3 model are:

- Normal and reverse short-channel and narrow-width effects on the threshold.
 - Channel length modulation (*CLM*).
 - Drain induced barrier lowering (*DIBL*).
 - Velocity saturation.
 - Mobility degradation due to the vertical electric field.
 - Impact ionization.
 - Band-to-band tunneling.
 - Velocity overshoot.
 - Self-heating.
- 1.) Channel quantization.
 - 2.) Polysilicon depletion.

BSIM3v3 Model Equations for Hand Calculations

In strong inversion, approximate hand equations are:

$$i_{DS} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \frac{1}{1 + \frac{v_{DS}}{E_{sat} L_{eff}}} \left(v_{GS} - V_{th} - \frac{A_{bulk} v_{DS}}{2} \right) v_{DS}, \quad v_{DS} < V_{DS}(\text{sat})$$

$$i_{DS} = W_{eff} v_{sat} C_{ox} [v_{GS} - V_{th} - A_{bulk} V_{DS}(\text{sat})] \left(1 + \frac{v_{DS} - V_{DS}(\text{sat})}{V_A} \right), \quad v_{DS} > V_{DS}(\text{sat})$$

where

$$V_{DS}(\text{sat}) = \frac{E_{sat} L_{eff} (v_{GS} - V_{th})}{A_{bulk} E_{sat} L_{eff} + (v_{GS} - V_{th})}$$

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

E_{sat} = Electric field where the drift velocity (v) saturates

v_{sat} = saturation velocity of carriers in the channel

$$\mu = \frac{\mu_{eff}}{1 + (E_y/E_{sat})} \Rightarrow \mu_{eff} = \frac{2v_{sat}}{E_{sat}}$$

Note: Assume $A_{bulk} \approx 1$ and extract V_{th} and V_A .

MOSIS Parametric Test Results

<http://www.mosis.org/>

RUN: T02D
TECHNOLOGY: SCN025

VENDOR: TSMC
FEATURE SIZE: 0.25 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: TSMC 025P5M.

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.36/0.24			
Vth		0.54	-0.50	volts
SHORT	20.0/0.24			
Idss		557	-256	uA/um
Vth		0.56	-0.56	volts
Vpt		7.6	-7.2	volts
WIDE	20.0/0.24			
Ids0		6.6	-1.5	pA/um
LARGE	50.0/50.0			
Vth		0.47	-0.60	volts
Vjbd		5.8	-7.0	volts
Ijk		-25.0	-1.1	pA
Gamma		0.44	0.61	V ^{0.5}
K' (Uo*Cox/2)		112.0	-23.0	uA/V ²

0.25μm BSIM3v3.1 NMOS Parameters

```

MODEL CMOSN NMOS (
  LEVEL = 49
  +VERSION = 3.1    TNOM = 27      TOX = 5.7E-9
  +XJ = 1E-7      NCH = 2.3549E17   VTH0 = 0.4273342
  +K1 = 0.3922983  K2 = 0.0185825  K3 = 1E-3
  +K3B = 2.0947677 W0 = 2.171779E-7  NLX = 1.919758E-7
  +DVT0W = 0       DVT1W = 0      DVT2W = 0
  +DVT0 = 7.137212E-3  DVT1 = 6.066487E-3  DVT2 = -0.3025397
  +U0 = 403.1776038 UA = -3.60743E-12 UB = 1.323051E-18
  +UC = 2.575123E-11 VSAT = 1.616298E5 A0 = 1.4626549
  +AGS = 0.3136349 B0 = 3.080869E-8 B1 = -1E-7
  +KETA = 5.462411E-3 A1 = 4.653219E-4 A2 = 0.6191129
  +RDSW = 345.624986 PRWG = 0.3183394 PRWB = -0.1441065
  +WR = 1          WINT = 8.107812E-9 LINT = 3.375523E-9
  +XL = 3E-8      XW = 0        DWG = 6.420502E-10
  +DWB = 1.042094E-8 VOFF = -0.1083577 NFACTOR = 1.1884386
  +CIT = 0         CDSC = 2.4E-4 CDSRD = 0
  +CDSCB = 0      ETA0 = 4.914545E-3 ETAB = 4.215338E-4
  +DSUB = 0.0313287 PCLM = 1.2088426 PDIBLC1 = 0.7240447
  +PDIBLC2 = 5.120303E-3 PDIBLCB = -0.0443076 DROUT = 0.7752992
  +PSCBE1 = 4.451333E8 PSCBE2 = 5E-10 PVAG = 0.2068286
  +DELTA = 0.01 MOBMOD = 1 PRT = 0
  +UTE = -1.5     KT1 = -0.11   KT1L = 0
  +KT2 = 0.022    UA1 = 4.31E-9 UB1 = -7.61E-18
  +UC1 = -5.6E-11 AT = 3.3E4   WL = 0
  +WLN = 1        WW = -1.22182E-16 WWN = 1.2127
  +WWL = 0        LL = 0      LLN = 1
  +LW = 0         LWN = 1     LWL = 0
  +CAPMOD = 2    XPART = 0.4   CGDO = 6.33E-10
  +CGSO = 6.33E-10 CGBO = 1E-11 CJ = 1.766171E-3
  +PB = 0.9577677 MJ = 0.4579102 CJSW = 3.931544E-10
  +PBSW = 0.99   MJSW = 0.2722644 CF = 0
  +PVTH0 = -2.126483E-3 PRDSW = -24.2435379 PK2 = -4.788094E-4
  +WKETA = 1.430792E-3 LKETA = -6.548592E-3 )

```

0.25µm BSIM3v3.1 PMOS Parameters

```

MODEL CMOSP PMOS (          LEVEL = 49
+VERSION = 3.1      TNOM  = 27      TOX   = 5.7E-9
+XJ   = 1E-7      NCH   = 4.1589E17    VTH0  = -0.6193382
+K1   = 0.5275326    K2   = 0.0281819    K3   = 0
+K3B  = 11.249555     W0   = 1E-6      NLX   = 1E-9
+DVT0W = 0      DVT1W = 0      DVT2W = 0
+DVT0  = 3.1920483    DVT1  = 0.4901788    DVT2  = -0.0295257
+U0   = 185.1288894    UA   = 3.40616E-9    UB   = 3.640498E-20
+UC   = -6.35238E-11    VSAT  = 1.975064E5    A0   = 0.4156696
+AGS  = 0.0702036    B0   = 3.111154E-6    B1   = 5E-6
+KETA = 0.0253118    A1   = 2.421043E-4    A2   = 0.6754231
+RDSW = 866.896668    PRWG  = 0.0362726    PRWB = -0.293946
+WR   = 1      WINT  = 6.519911E-9    LINT  = 2.210804E-8
+XL   = 3E-8      XW   = 0      DWG   = -2.423118E-8
+DWB  = 3.052612E-8    VOFF  = -0.1161062    NFACTOR = 1.2546896
+CIT  = 0      CDSC  = 2.4E-4      CDSCD = 0
+CDSCB = 0      ETA0  = 0.7241245    ETAB  = -0.3675267
+DSUB = 1.1734643    PCLM  = 1.0837457    PDIBLC1 = 9.608442E-4
+PDIBLC2 = 0.0176785    PDIBLCB = -9.605935E-4    DROUT = 0.0735541
+PSCBE1 = 1.579442E10    PSCBE2 = 6.707105E-9    PVAG  = 0.0409261
+DELTA = 0.01      MOBMOD = 1      PRT   = 0
+UTE  = -1.5      KT1   = -0.11      KT1L  = 0
+KT2  = 0.022     UA1   = 4.31E-9      UB1   = -7.61E-18
+UC1  = -5.6E-11    AT   = 3.3E4      WL   = 0
+WLN  = 1      WW   = 0      WWN   = 1
+WWL  = 0      LL   = 0      LLN   = 1
+LW   = 0      LWN  = 1      LWL   = 0
+CAPMOD = 2      XPART = 0.4      CGDO  = 5.11E-10
+CGSO = 5.11E-10    CGBO  = 1E-11    CJ   = 1.882953E-3
+PB   = 0.99      MJ   = 0.4690946    CJSW = 3.018356E-10
+PBSW = 0.8137064    MJSW  = 0.3299497    CF   = 0
+PVTH0 = 5.268963E-3    PRDSW = -2.2622317    PK2  = 3.952008E-3
+WKETA = -7.69819E-3    LKETA = -0.0119828    )
)

```

EXTRACTION OF A LARGE SIGNAL MODEL FOR HAND CALCULATIONS

Objective

Extract a simple model that is useful for design from the computer models such as BSIM3.

Extraction for Short Channel Models

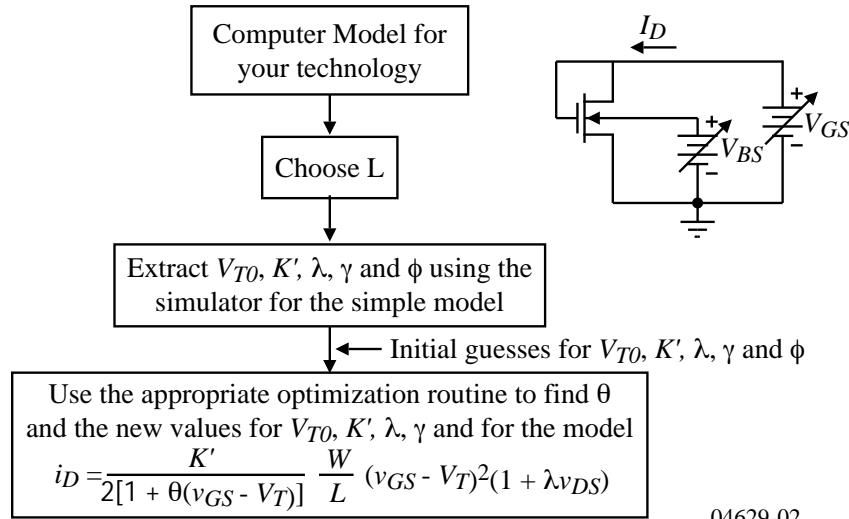
Procedure for extracting short channel models:

- 1.) Extract the square-law model parameters for a transistor with length at least 10 times L_{min} .
- 1.) Using the values of K' , V_T , λ , and γ extract the model parameters for the following model:

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]} \frac{W}{L} [v_{GS} - V_T]^2 (1 + \lambda v_{DS})$$

Adjust the values of K' , V_T , and λ as needed.

Illustration of the Extraction Procedure



04629-02

EXTRACTION OF THE SIMPLE, SQUARE-LAW MODEL

Characterization of the Simple Square-Law Model

Equations for the MOSFET in strong inversion:

$$i_D = K' \left(\frac{W_{\text{eff}}}{2L_{\text{eff}}} \right) (v_{GS} - V_T)^2 (1 + \lambda v_{DS}) \quad (1)$$

$$i_D = K' \left(\frac{W_{\text{eff}}}{L_{\text{eff}}} \right) \left[(v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2} \right] (1 + \lambda v_{DS}) \quad (2)$$

where

$$V_T = V_{T0} + \gamma [\sqrt{2|\phi_F| + v_{SB}} - \sqrt{2|\phi_F|}] \quad (3)$$

Extraction of Model Parameters:

First assume that v_{DS} is chosen such that the λv_{DS} term in Eq. (1) is much less than one and v_{SB} is zero, so that $V_T = V_{T0}$.

Therefore, Eq. (1) simplifies to

$$i_D = K' \left(\frac{W_{\text{eff}}}{2L_{\text{eff}}} \right) (v_{GS} - V_{T0})^2 \quad (4)$$

This equation can be manipulated algebraically to obtain the following

$$i_D^{1/2} = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2} v_{GS} = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2} V_{T0} \quad (5)$$

which has the form

$$y = mx + b \quad (6)$$

This equation is easily recognized as the equation for a straight line with m as the slope and b as the y -intercept. Comparing Eq. (5) to Eq. (6) gives

$$y = i_D^{1/2} \quad (7)$$

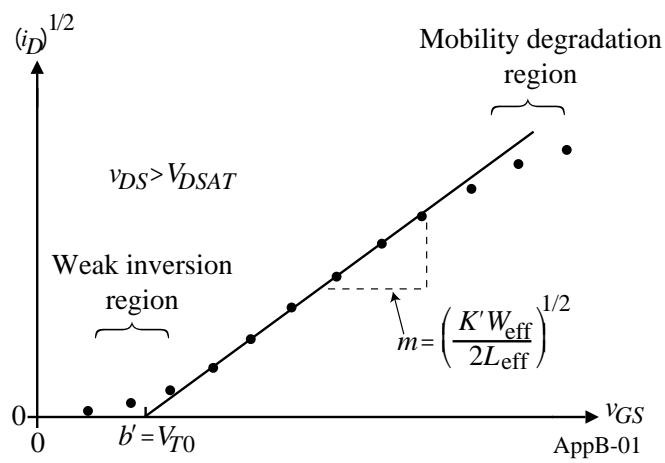
$$x = v_{GS} \quad (8)$$

$$m = \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2}$$

and

$$b = - \left(\frac{K' W_{\text{eff}}}{2L_{\text{eff}}} \right)^{1/2} V_{T0}$$

Illustration of K' and V_T Extraction



Comments:

- Stay away from the extreme regions of mobility degradation and weak inversion
- Use channel lengths greater than L_{min}

Example 130-1 – Extraction of K' and V_T Using Linear Regression

Given the following transistor data shown in Table 1 and linear regression formulas based on the form,

$$y = mx + b \quad (11)$$

and

$$m = \frac{\sum x_i y_i - (\sum x_i \sum y_i)/n}{\sum x_i^2 - (\sum x_i)^2/n} \quad (12)$$

determine V_{T0} and $K'W/2L$. The data in Table 1 also give $I_D^{1/2}$ as a function of V_{GS} .

Table 1 Data for Example 130-1

V_{GS} (V)	I_D (μ A)	$\sqrt{I_D}$ (μ A) $^{1/2}$	V_{SB} (V)
1.000	0.700	0.837	0.000
1.200	2.00	1.414	0.000
1.500	8.00	2.828	0.000
1.700	13.95	3.735	0.000
1.900	22.1	4.701	0.000

Example 130-1 – Continued

Solution

The data must be checked for linearity before linear regression is applied. Checking slopes between data points is a simple numerical technique for determining linearity. Using the formula that

$$\text{Slope } m = \frac{\Delta y}{\Delta x} = \frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{V_{GS2} - V_{GS1}}$$

Gives

$$m_1 = \frac{1.414 - 0.837}{0.2} = 2.885$$

$$m_2 = \frac{2.828 - 1.414}{0.3} = 4.713$$

$$m_3 = \frac{3.735 - 2.828}{0.2} = 4.535$$

$$m_4 = \frac{4.701 - 3.735}{0.2} = 4.830$$

These results indicate that the first (lowest value of V_{GS}) data point is either bad, or at a point where the transistor is in weak inversion. This data point will not be included in subsequent analysis. Performing the linear regression yields the following results.

$$V_{T0} = 0.898 \text{ V} \quad \text{and} \quad \frac{K'W_{\text{eff}}}{2L_{\text{eff}}} = 21.92 \mu\text{A/V}^2$$

Extraction of the Bulk-Threshold Parameter γ

Using the same techniques as before, the following equation

$$V_T = V_{T0} + \gamma [\sqrt{2|\phi_F|} + v_{SB} - \sqrt{2|\phi_F|}]$$

is written in the linear form where

$$y = V_T$$

$$x = \sqrt{2|\phi_F|} + v_{SB} - \sqrt{2|\phi_F|}$$

$$m = \gamma$$

$$b = V_{T0}$$

The term $2|\phi_F|$ is unknown but is normally in the range of 0.6 to 0.7 volts.

Procedure:

1.) Pick a value for $2|\phi_F|$.

2.) Extract a value for γ .

3.) Calculate N_{SUB} using the relationship, $\gamma = \frac{\sqrt{2\varepsilon_{si}qN_{SUB}}}{C_{ox}}$

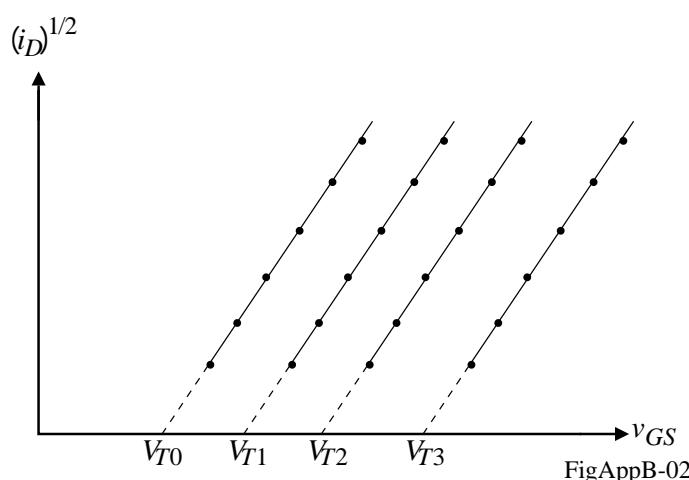
4.) Calculate ϕ_F using the relationship, $\phi_F = -\frac{kT}{q} \ln \left(\frac{N_{SUB}}{n_i} \right)$

5.) Iterative procedures can be used to achieve the desired accuracy of γ and $2|\phi_F|$.

Generally, an approximate value for $2|\phi_F|$ gives adequate results.

Illustration of the Procedure for Extracting γ

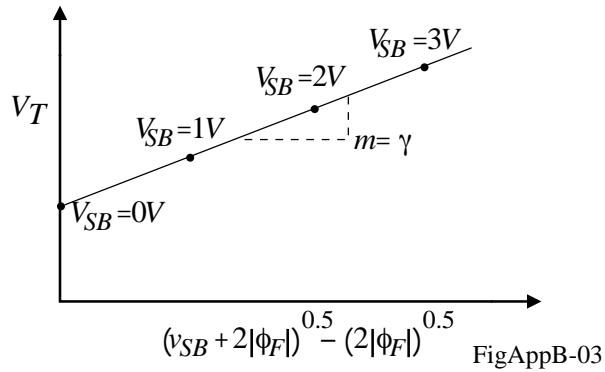
A plot of $\sqrt{i_D}$ versus v_{GS} for different values of v_{SB} used to determine γ is shown below.



By plotting V_T versus x of Eq. (13) one can measure the slope of the best fit line from which the parameter γ can be extracted. In order to do this, V_T must be determined at various values of v_{SB} using the technique previously described.

Illustration of the Procedure for Extracting γ - Continued

Each V_T determined above must be plotted against the v_{SB} term. The result is shown below. The slope m , measured from the best fit line, is the parameter γ .



FigAppB-03

Example 130-2 – Extraction of the Bulk Threshold Parameter

Using the results from Ex. 130-1 and the following transistor data, determine the value of γ using linear regression techniques. Assume that $2|\phi_F|$ is 0.6 volts.

Table 2 Data for Example 130-2.

V_{SB} (V)	V_{GS} (V)	I_D (μ A)
1.000	1.400	1.431
1.000	1.600	4.55
1.000	1.800	9.44
1.000	2.000	15.95
2.000	1.700	3.15
2.000	1.900	7.43
2.000	2.10	13.41
2.000	2.30	21.2

Solution

Table 2 shows data for $V_{SB} = 1$ volt and $V_{SB} = 2$ volts. A quick check of the data in this table reveals that $\sqrt{I_D}$ versus V_{GS} is linear and thus may be used in the linear regression analysis. Using the same procedure as in Ex. 1, the following thresholds are determined: $V_{T0} = 0.898$ volts (from Ex. 1), $V_T = 1.143$ volts (@ $V_{SB} = 1$ V), and $V_T = 1.322$ V (@ $V_{SB} = 2$ V). Table 3 gives the value of V_T as a function of $[(2|\phi_F| + V_{SB})^{1/2} - (2|\phi_F|)^{1/2}]$ for the three values of V_{SB} .

Example 130-2 - Continued

Table 3 Data for Example 130-2.

V_{SB} (V)	V_T (V)	$[\sqrt{2 \phi_F + V_{SB}} - \sqrt{2 \phi_F }] (V^{1/2})$
0.000	0.898	0.000
1.000	1.143	0.490
2.000	1.322	0.838

With these data, linear regression must be performed on the data of V_T versus $[(2|\phi_F| + V_{SB})^{0.5} - (2|\phi_F|)^{0.5}]$. The regression parameters of Eq. (12) are

$$\sum x_i y_i = 1.668$$

$$\sum x_i \sum y_i = 4.466$$

$$\sum x_i^2 = 0.9423$$

$$(\sum x_i)^2 = 1.764$$

These values give $m = 0.506 = \gamma$.

Extraction of the Channel Length Modulation Parameter, λ

The channel length modulation parameter λ should be determined for all device lengths that might be used. For the sake of simplicity, Eq. (1) is rewritten as

$$i_D = i'_D \lambda' v_{DS} + i'_D$$

which is in the familiar linear form where

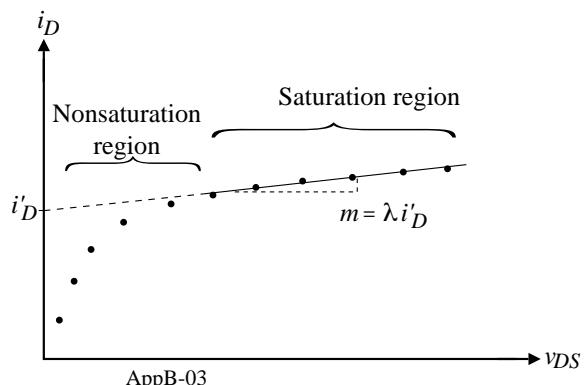
$$y = i_D \quad (\text{Eq. (1)})$$

$$x = v_{DS}$$

$$m = \lambda i'_D$$

$$b = i'_D \quad (\text{Eq. (1) with } \lambda = 0)$$

By plotting i_D versus v_{DS} , measuring the slope of the data in the saturation region, and dividing that value by the y -intercept, λ can be determined. The procedure is illustrated in the figure shown.



Example 130-3 – Extraction of the Channel Length Modulation Parameter

Given the data of I_D versus V_{DS} in Table 4, determine the parameter λ .

Table 4 Data for Example 130-3.

I_D (μA)	39.2	68.2	86.8	94.2	95.7	97.2	98.8	100.3
V_{DS} (V)	0.500	1.000	1.500	2.000	2.50	3.00	3.50	4.00

Solution

We note that the data of Table 4 covers both the saturation and nonsaturation regions of operation. A quick check shows that saturation is reached near $V_{DS} = 2.0$ V. To calculate λ , we shall use the data for V_{DS} greater than or equal to 2.5 V. The parameters of the linear regression are

$$\sum x_i y_i = 1277.85 \quad \sum x_i \sum y_i = 5096.00$$

$$\sum x_i^2 = 43.5 \quad (\sum x_i)^2 = 169$$

These values result in $m = \lambda I'_D = 3.08$ and $b = I'_D = 88$, giving $\lambda = 0.035$ V $^{-1}$.

The slope in the saturation region is typically very small, making it necessary to be careful that two data points taken with low resolution are not subtracted (to obtain the slope) resulting in a number that is of the same order of magnitude as the resolution of the data point measured. If this occurs, then the value obtained will have significant and unacceptable error.

EXTRACTION OF THE SIMPLE MODEL FOR SHORT CHANNEL MOSFETS

Extraction for Short Channel MOSFETS

The model proposed is the following one which is the square-law model modified by the velocity saturation influence.

$$i_D = \frac{K'}{2[1 + \theta(v_{GS} - V_T)]} \frac{W}{L} [v_{GS} - V_T]^2 (1 + \lambda v_{DS})$$

Using the values of K' , V_T , λ , and γ extracted previously, use an appropriate extraction procedure to find the value of θ adjusting the values of K' , V_T , and λ as needed.

Comments:

- We will assume that the bulk will be connected to the source or the standard relationship between V_T and V_{BS} can be used.
- The saturation voltage is still given by

$$V_{DS}(\text{ sat}) = V_{GS} - V_T$$

Example of a Genetic Algorithm[†]

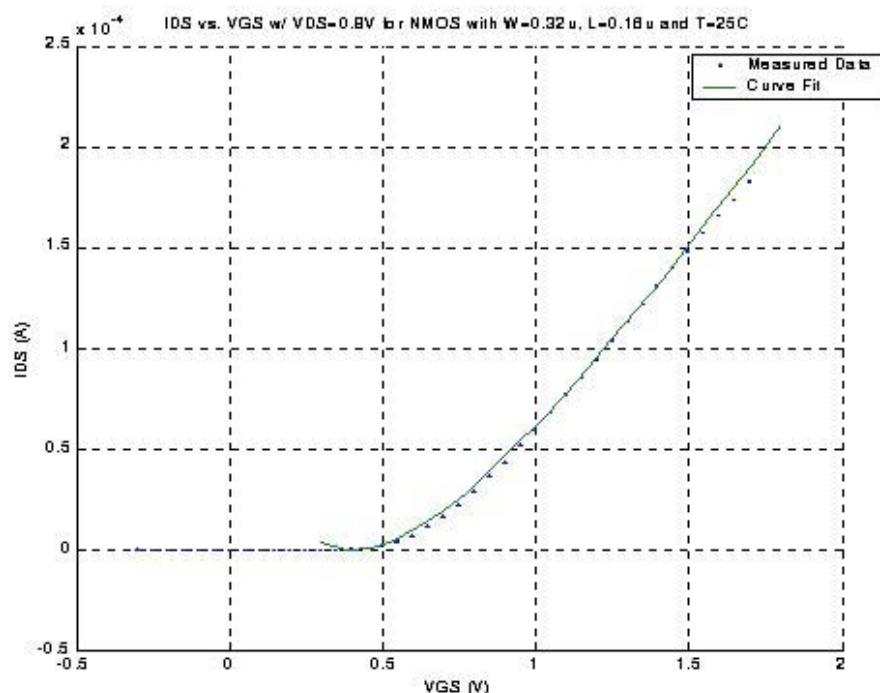
- 1.) To use this algorithm or any other, use the simulator and an appropriate short-channel model (BSIM3) to generate a set of data for the transconductance (i_D vs. v_{GS}) and output characteristics (i_D vs. v_{DS}) of the transistor with the desired W and L values.
 - 2.) The best fit to the data is found using a genetic algorithm. The constraints on the parameters are obtained from experience with prior transistor parameters and are:
 $10E-6 < \beta < 610E-6$, $1 < \theta < 5$, $0 < V_T < 1$, and $0 < \lambda < 0.5$
 - 3.) The details of the genetic algorithm are:
Gene structure is $A = [\beta, \theta, V_T, \text{fitness}]$. A mutation was done by varying all four parameters. A weighted sum of the least square errors of the data curves was used as the error function. The fitness of a gene was chosen as 1/error.
 - 4.) The results for an extraction run of 8000 iterations for an NMOS transistor is shown below.
- | $\beta(A/V^2)$ | θ | $V_T(V)$ | $\lambda(V^{-1})$ |
|------------------------|----------|----------|-------------------|
| 294.1×10^{-6} | 1.4564 | 0.4190 | 0.1437 |
- 5.) The results for a NMOS and PMOS transistor are shown on the following pages.

[†] Anurag Kapilash, "Parameter Optimization of Deep Submicron MOSFETs Using a Genetic Algorithm," May 4, 2000, Special Project Report, School of ECE, Georgia Tech.
CMOS Analog Circuit Design

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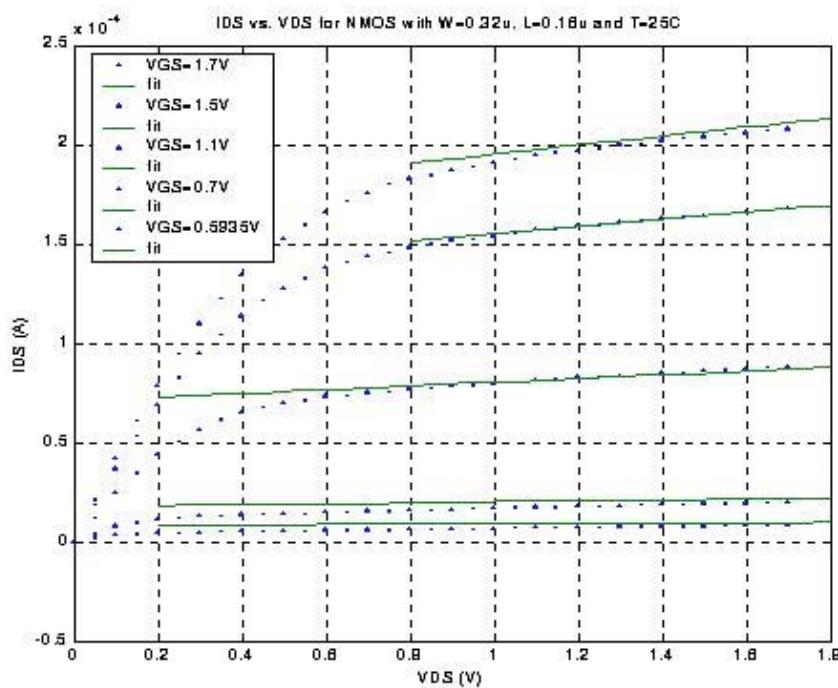
Extraction Results for an NMOS Transistor with $W = 0.32\mu\text{m}$ and $L = 0.18\mu\text{m}$

Transconductance:



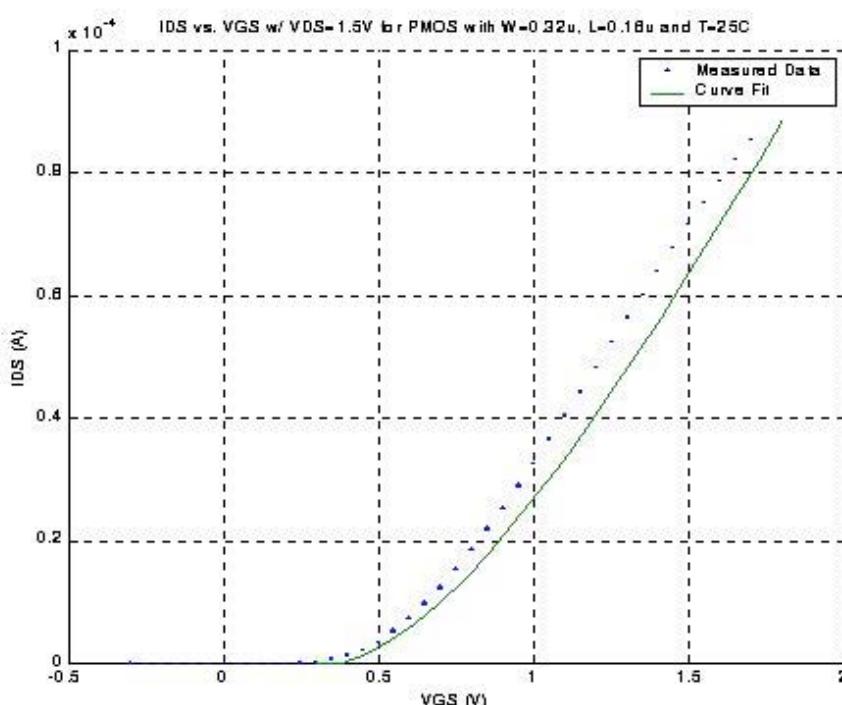
Extraction Results for an NMOS Transistor with $W = 0.32\mu\text{m}$ and $L = 0.18\mu\text{m}$

Output:



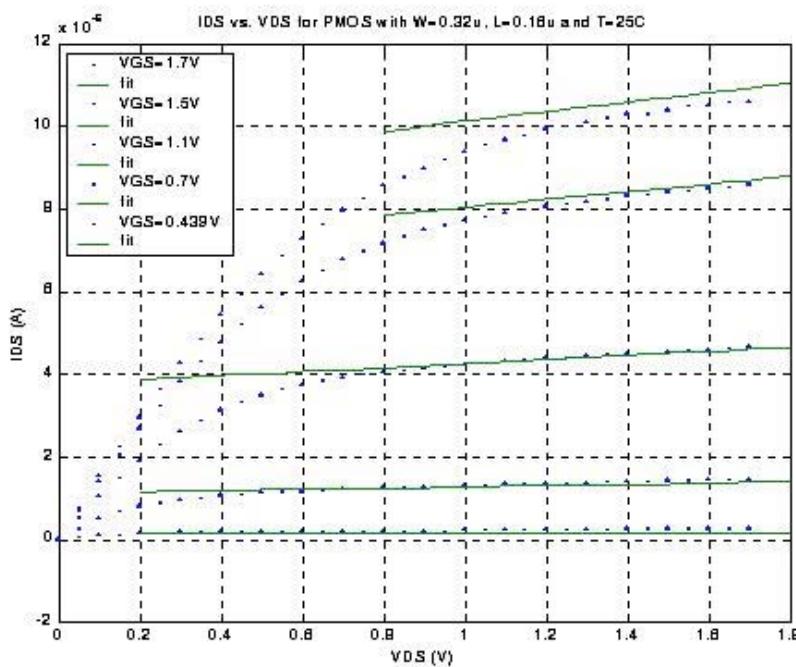
Extraction Results for an PMOS Transistor with $W = 0.32\mu\text{m}$ and $L = 0.18\mu\text{m}$

Transconductance:



Extraction Results for an PMOS Transistor with $W = 0.32\mu\text{m}$ and $L = 0.18\mu\text{m}$

Output:



SUMMARY

- Models are much improved for efficient computer simulation
- Output conductance model is greatly improved
- Narrow channel transistors have difficulty with modeling
- Can have discontinuities at bin boundaries
- The BSIM model is a complex model, difficult to understand in detail
- The simple large signal model can be extracted from any computer model
- Extract the model at the desired channel length for the design
- Short channel technology can be modeled by finding the θ by any optimization routine

LECTURE 140 – THE MOS SWITCH AND MOS DIODE

LECTURE ORGANIZATION

Outline

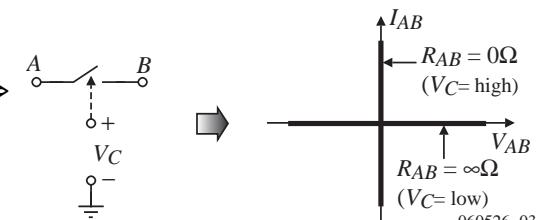
- MOSFET as a switch
- Influence of the switch resistance
- Influence of the switch capacitors
 - Channel injection
 - Clock feedthrough
- Using switches at reduced values of V_{DD}
- MOS Diode
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 113-124

Switch Model

- An ideal switch is a short-circuit when ON and an open-circuit when OFF. $V_C =$ controlling terminal for the switch (V_C high \Rightarrow switch ON, V_C low \Rightarrow switch OFF)



- Actual switch:

r_{on} = resistance of the switch when ON

r_{off} = resistance of the switch when OFF

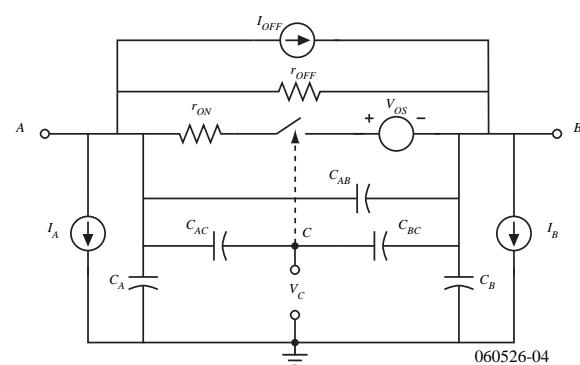
V_{OS} = offset voltage when the switch is ON

I_{off} = offset current when the switch is OFF

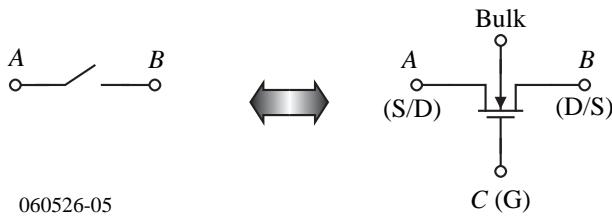
I_A and I_B are leakage currents to ground

C_A and C_B are capacitances to ground

C_{AC} and C_{BC} = parasitic capacitors between the control terminal and switch terminals



MOS Transistor as a Switch



On Characteristics of a MOS Switch

Assume operation in active region ($v_{DS} < v_{GS} - V_T$) and v_{DS} small.

$$i_D = \frac{\mu C_{ox} W}{L} \left[(v_{GS} - V_T) - \frac{v_{DS}}{2} \right] v_{DS} \approx \frac{\mu C_{ox} W}{L} (v_{GS} - V_T) v_{DS}$$

Thus,

$$R_{ON} \approx \frac{v_{DS}}{i_D} = \frac{1}{\frac{\mu C_{ox} W}{L} (v_{GS} - V_T)}$$

OFF Characteristics of a MOS Switch

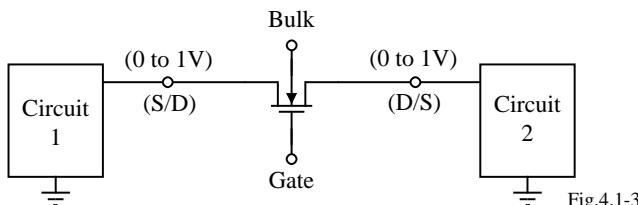
If $v_{GS} < V_T$, then $i_D = I_{OFF} = 0$ when $v_{DS} \approx 0V$.

If $v_{DS} > 0$, then

$$R_{OFF} \approx \frac{1}{i_D \lambda} = \frac{1}{I_{OFF} \lambda} \approx \infty$$

MOS Switch Voltage Ranges

If a MOS switch is used to connect two circuits that can have analog signal that vary from 0 to 1V, what must be the value of the bulk and gate voltages for the switch to work properly?



- To insure that the bulk-source and bulk-drain *pn* junctions are reverse biased, the bulk voltage must be less than the minimum analog signal for a NMOS switch.
- To insure that the switch is on, the gate voltage must be greater than the maximum analog signal plus the threshold for a NMOS switch.

Therefore:

$$V_{Bulk} \leq 0V$$

$$V_{Gate(on)} > 1V + V_T$$

$$V_{Gate(off)} \leq 0V$$

Unfortunately, the large value of reverse bias bulk voltage causes the threshold voltage to increase.

Current-Voltage Characteristics of a NMOS Switch

The following simulated output characteristics correspond to triode operation of the MOSFET.

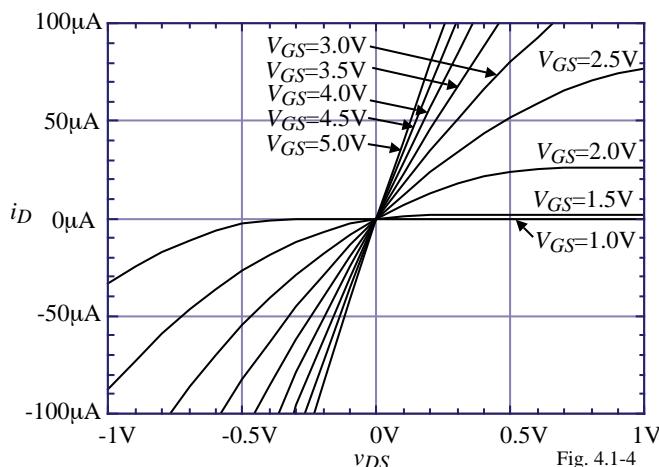


Fig. 4.1-4

SPICE Input File:

```
MOS Switch On Characteristics
M1 1 2 0 3 MNMOS W=1U L=1U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4 PHI=0.7
VDS 1 0 DC 0.0
```

```
VGS 2 0 DC 0.0
VBS 3 0 DC -5.0
.DC VDS -1 1 0.1 VGS 1 5 0.5
.PRINT DC ID(M1)
.PROBE
.END
```

MOS Switch ON Resistance as a Function of Gate-Source Voltage

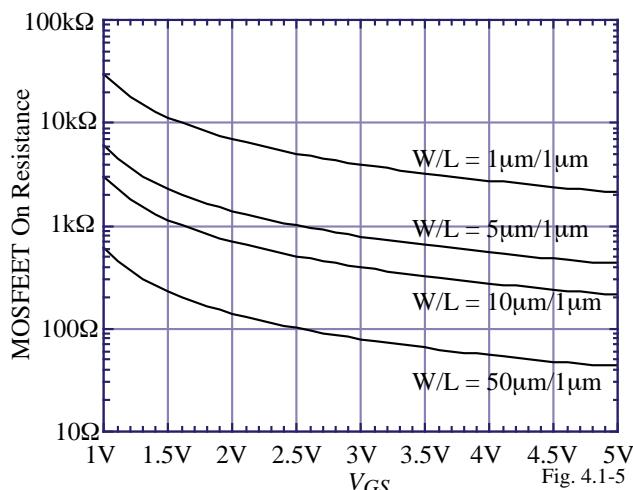


Fig. 4.1-5

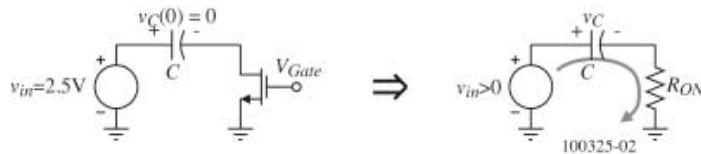
SPICE Input File:

```
MOS Switch On Resistance as a f(W/L)
M1 1 2 0 0 MNMOS W=1U L=1U
M2 1 2 0 0 MNMOS W=5U L=1U
M3 1 2 0 0 MNMOS W=10U L=1U
M4 1 2 0 0 MNMOS W=50U L=1U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
```

```
+LAMBDA=0.04, GAMMA=0.4, PHI=0.7
VDS 1 0 DC 0.001V
VGS 2 0 DC 0.0
.DC VGS 1 5 0.1
.PRINT DC ID(M1) ID(M2) ID(M3) ID(M4)
.PROBE
.END
```

Influence of the ON Resistance on MOS Switches

Finite ON Resistance:



Example

Initially assume the capacitor is uncharged. If $V_{Gate}(\text{ON})$ is 5V and is high for $0.1\mu\text{s}$, find the W/L of the MOSFET switch that will charge a capacitance of 10pF in five time constants.

Solution

The time constant must be $100\text{ns}/5 = 20\text{ns}$. Therefore R_{ON} must be less than $20\text{ns}/10\text{pF} = 2\text{k}\Omega$. The ON resistance of the MOSFET (for small v_{DS}) is

$$R_{ON} = \frac{1}{K_N'(W/L)(V_{GS}-V_T)} \Rightarrow \frac{W}{L} = \frac{1}{R_{ON} \cdot K_N'(V_{GS}-V_T)} = \frac{1}{2\text{k}\Omega \cdot 110\mu\text{A/V}^2 \cdot 4.3} = 1.06$$

Comments:

- It is relatively easy to charge on-chip capacitors with minimum size switches.
- Switch resistance is really not constant during switching and the problem is more complex than above.

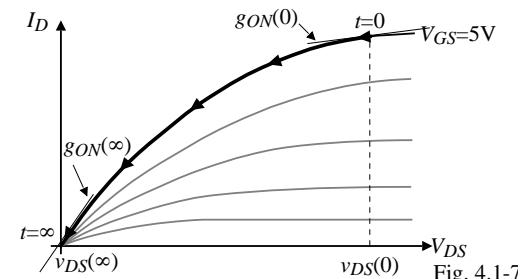
Including the Influence of the Varying On Resistance

Gate-source Constant

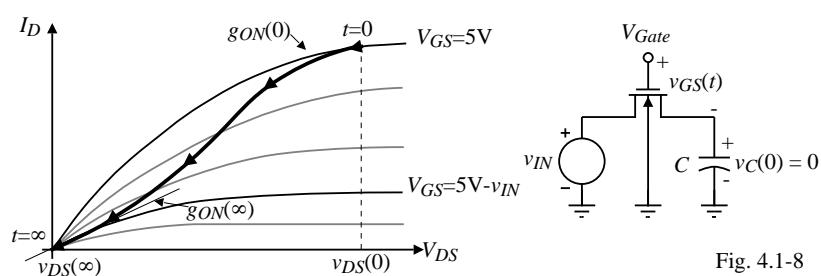
$$g_{ON}(t) = \frac{K'W}{L} [(v_{GS}(t)-V_T) - 0.5v_{DS}(t)]$$

$$g_{ON}(\text{aver.}) = \frac{1}{r_{ON}(\text{aver.})} \approx \frac{g_{ON}(0) + g_{ON}(\infty)}{2}$$

$$\begin{aligned} &= \frac{K'W}{2L} (V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L} + \frac{K'W}{2L} (V_{GS}-V_T) \\ &= \frac{K'W}{L} (V_{GS}-V_T) - \frac{K'WV_{DS}(0)}{4L} \end{aligned}$$



Gate-source Varying



$$g_{ON} = \frac{K'W}{2L} [V_{GS}(0)-V_T] - \frac{K'WV_{DS}(0)}{4L} + \frac{K'W}{2L} [V_{GS}(\infty)-v_{IN}-V_T]$$

Example 1 - Switch ON Resistance

Assume that at $t = 0$, the gate of the switch shown is taken to 5V. Design the W/L value of the switch to discharge the C_1 capacitor to within 1% of its initial charge in 10ns. Use the MOSFET parameters of Table 3.1-2.

Solution

Note that the source of the NMOS is on the right and is always at ground potential so there is no bulk effect as long as the voltage across C_1 is positive. The voltage across C_1 can be expressed as

$$v_{C1}(t) = 5 \exp\left(\frac{-t}{R_{ON}C_1}\right)$$

At 10ns, v_{C1} is 5/100 or 0.05V. Therefore,

$$\begin{aligned} 0.05 &= 5 \exp\left(\frac{-10^{-8}}{R_{ON}10^{-11}}\right) = 5 \exp\left(\frac{-10^3}{R_{ON}}\right) \Rightarrow \exp(G_{ON}10^3) = 100 \Rightarrow G_{ON} = \frac{\ln(100)}{10^3} \\ &= 0.0046 \text{S} \end{aligned}$$

$$\therefore 0.0046 = \frac{K'W}{L}(V_{GS} - V_T) - \frac{K'WV_{DS}(0)}{4L} = \left(110 \times 10^{-6} \cdot 4.3 - \frac{110 \times 10^{-6} \cdot 5}{4}\right) \frac{W}{L} = 356 \times 10^{-6} \frac{W}{L}$$

$$\text{Thus, } \frac{W}{L} = \frac{0.0046}{356 \times 10^{-6}} = 13.71 \approx 14$$

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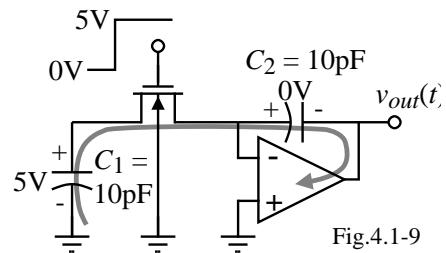


Fig.4.1-9

Influence of the OFF State on MOS Switches

The OFF state influence is primarily in any current that flows from the terminals of the switch to ground.

An example might be:

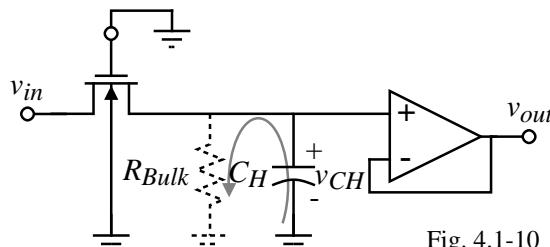


Fig. 4.1-10

Typically, no problems occur unless capacitance voltages are held for a long time. For example,

$$v_{out}(t) = v_{CH} e^{-t/(R_{Bulk}C_H)}$$

If $R_{Bulk} \approx 10^9 \Omega$ and $C_H = 10 \text{ pF}$, the time constant is $10^9 \cdot 10^{-11} = 0.01 \text{ seconds}$

Influence of Parasitic Capacitances

The parasitic capacitors have two influences:

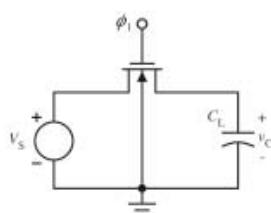
- Parasitics to ground at the switch terminals (C_{BD} and C_{BS}) add to the value of the desired capacitors.

This problem is solved by the use of stray-insensitive switched capacitor circuits

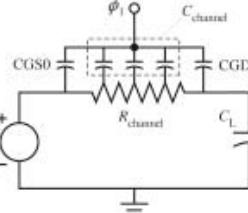
- Parasitics from gate to source and drain cause *charge injection* and *clock feedthrough* onto or off the desired capacitors.

This problem can be minimized but not eliminated.

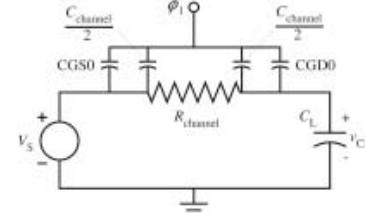
Model for studying gate capacitance:



A simple switch circuit useful for studying charge injection.



A distributed model of the transistor switch.



A lumped model of the transistor switch. 100325-03

Channel Charge Injection

Consider the simple switch configuration shown:

When the switch is ON, a charge is stored in the channel which is equal to,

$$Q_{ch} = -WLC_{ox}(V_H - v_{in} - V_T)$$

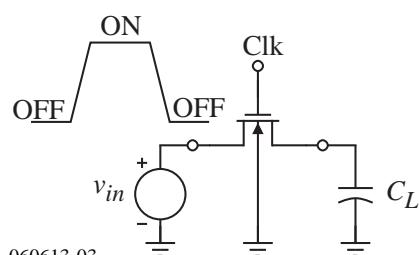
where V_H is the value of the clock waveform when the switch is on ($V_H \approx V_{DD}$)

When the switch turns OFF, this charge is injected into the source and drain terminals as shown.

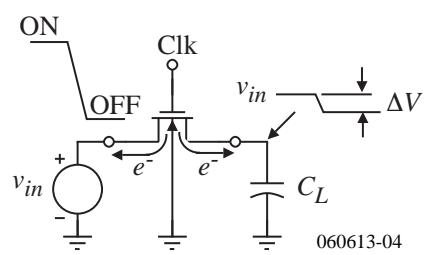
Assuming the charge splits evenly, then the change of voltage across the capacitor, C_L , is

$$\Delta V = \frac{Q_{ch}}{2C_L} = \frac{-WLC_{ox}(V_H - v_{in} - V_T)}{2C_L}$$

The charge injection does not influence v_{in} because it is a voltage source.



060613-03

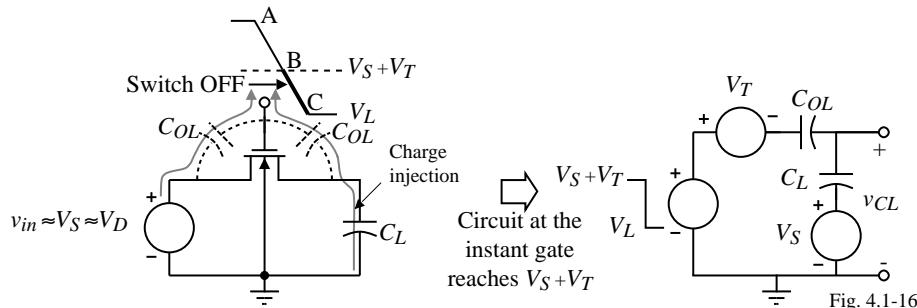


060613-04

Clock Feedthrough

In addition to the charge injection, the overlap capacitors of the MOSFET couple the turning off part of the clock to the load capacitor. This is called *clock feedthrough*.

The model for this case is given as:



The gate decrease from B to C is modeled as a negative step of magnitude $V_S + V_T - V_L$. The output voltage on the capacitor after opening the switch is,

$$v_{CL} = \left(\frac{C_L}{C_{OL} + C_L} \right) V_S - \left(\frac{C_{OL}}{C_{OL} + C_L} \right) V_T - (V_S + V_T - V_L) \left(\frac{C_{OL}}{C_{OL} + C_L} \right) \approx V_S - (V_S + 2V_T - V_L) \left(\frac{C_{OL}}{C_L} \right)$$

if $C_{OL} < C_L$.

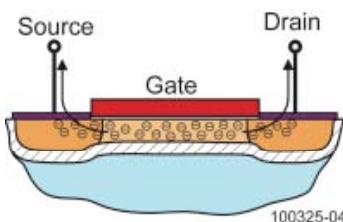
Therefore the error voltage is,

$$V_{error} \approx -(V_S + 2V_T - V_L) \left(\frac{C_{OL}}{C_L} \right) = -(v_{in} + 2V_T - V_L) \left(\frac{C_{OL}}{C_L} \right)$$

Modeling the Influence of Charge Injection and Clock Feedthrough

The influence of charge injection and clock feedthrough on a switch is a complex analysis which is better suited for computer analysis. Here we will attempt to develop an understanding sufficient to show ways of reducing these effects.

To begin the model development, there are two cases of charge injection depending upon the transition rate when the switch turns off.



- 1.) Slow transition time – the charge in the channel can react instantaneously to changes in the turning-off, gate-source voltage.
- 2.) Fast transition time – the charge in the channel cannot react fast enough to respond to the changes in the turning-off, gate-source voltage.

Slow Transition Time

Consider the following switch circuit:

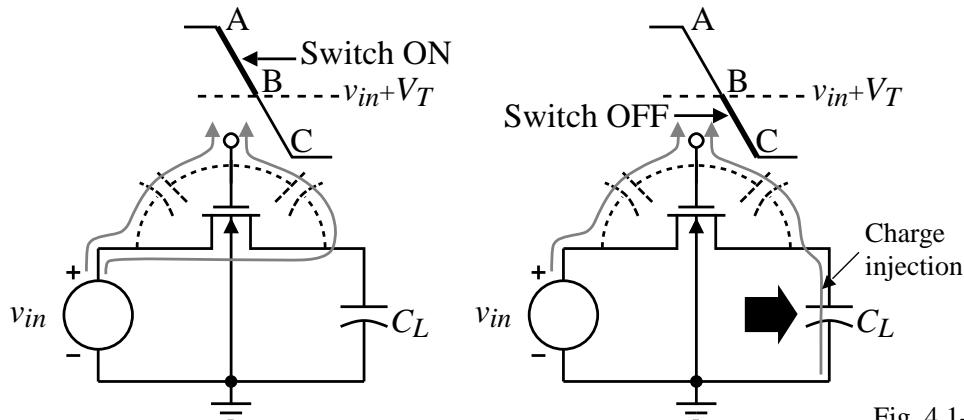


Fig. 4.1-13

- 1.) During the on-to-off transition time from A to B, the charge injection is absorbed by the low impedance source, v_{in} .
- 2.) The switch turns off when the gate voltage is $v_{in} + V_T$ (point B).
- 3.) From B to C the switch is off but the gate voltage is changing. As a result charge injection occurs to C_L .

Fast Transition Time

For the fast transition time, the rate of transition is faster than the channel time constant so that some of the charge during the region from point A to point B is injected onto C_L even though the transistor switch has not yet turned off.

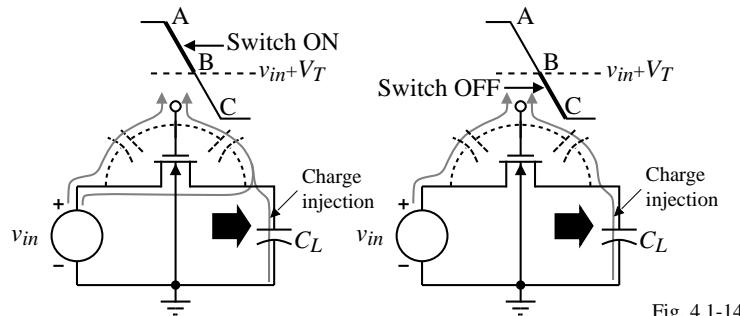


Fig. 4.1-14

A Quantized Model of Charge Injection/Clock Feedthrough[†]

Approximate the gate transition as a staircase and discretized in voltage as follows:

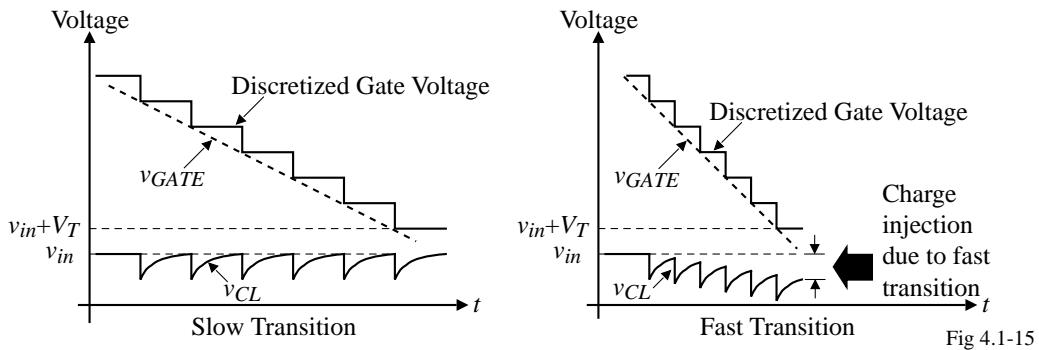


Fig 4.1-15

The time constant of the channel, $R_{channel}C_{channel}$, determines whether or not the capacitance, C_L , fully charges during each voltage step.

[†] B.J. Sheu and C. Hu, "Switched-Induced Error Voltage on A Switched Capacitor," *IEEE J. Solid-State Circuits*, Vol. SC-19, No. 4, pp. 519-525, August 1984.

Analytical Expressions to Approximate Charge Injection/Clock Feedthrough

Assume the gate voltage is making a transition from high, V_H , to low, V_L .

$$\therefore v_{Gate} = v_G(t) = V_H - Ut \quad \text{where } U = \text{magnitude of the slope of } v_G(t)$$

$$\text{Define } V_{HT} = V_H - V_S - V_T \text{ and } \beta = \frac{K'W}{L}$$

The error in voltage across C_L , V_{error} , is given below in two terms. The first term corresponds to the feedthrough that occurs while the switch is still on and the second term corresponds to feedthrough when the switch is off.

$$1.) \text{ Slow transition occurs when } \frac{\beta V_{HT}}{2C_L} \gg U.$$

$$V_{error} = -\left(\frac{W \cdot CGD0 + \frac{C_{channel}}{2}}{C_L}\right) \sqrt{\frac{\pi U C_L}{2\beta}} - \frac{W \cdot CGD0}{C_L} (V_S + 2V_T - V_L)$$

$$2.) \text{ Fast transition occurs when } \frac{\beta V_{HT}}{2C_L} \ll U.$$

$$V_{error} = -\left(\frac{W \cdot CGD0 + \frac{C_{channel}}{2}}{C_L}\right) \left(V_{HT} - \frac{\beta V_{HT}^3}{6U \cdot C_L}\right) - \frac{W \cdot CGD0}{C_L} (V_S + 2V_T - V_L)$$

Example 2 - Calculation of Charge Feedthrough Error

Calculate the effect of charge feedthrough on the previous circuit where $V_S = 1V$, $C_L = 1\text{pF}$, $W/L = 0.8\mu\text{m}/0.8\mu\text{m}$, and V_G is given below for the two cases. Use model parameters from Tables 3.1-2 and 3.2-1. Neglect ΔL and ΔW effects.

Solution

Case 1:

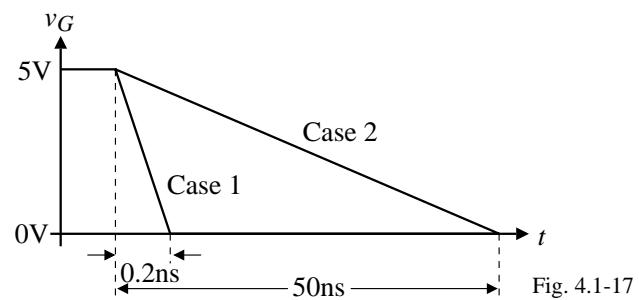


Fig. 4.1-17

The value of U is equal to $5V/0.2\text{nS}$ or 25×10^9 . Next we must test to see if the slow or fast transition time is appropriate. First calculate the value of V_T as

$$V_T = V_{T0} + \gamma\sqrt{2|\phi_F| - V_{BS}} - \gamma\sqrt{2|\phi_F|} = 0.7 + 0.4\sqrt{0.7+1} - 0.4\sqrt{0.7} = 0.887\text{V}$$

Therefore,

$$V_{HT} = V_H - V_S - V_T = 5 - 1 - 0.887 = 3.113\text{V} \Rightarrow \frac{\beta V_{HT}}{2C_L} = \frac{110 \times 10^{-6} \cdot 3.113^2}{2 \cdot 1\text{pF}} = 5.32 \times 10^8 < 25 \times 10^9$$

which corresponds to the fast transition case. Using the previous expression gives,

$V_{error} =$

$$-\left(\frac{176 \times 10^{-18} + 0.5(1.58 \times 10^{-15})}{1 \times 10^{-12}}\right) \left(3.113 - \frac{3.32 \times 10^{-3}}{30 \times 10^{-3}}\right) - \frac{176 \times 10^{-18}}{1 \times 10^{-12}}(1 + 1.774 - 0) = -3.39\text{mV}$$

Example 2 - Continued

Case 2:

In this case U is equal to $5V/50\text{ns}$ or 1×10^8 which means that the slow transition case is valid ($1 \times 10^8 < 5.32 \times 10^8$).

Using the previous expression gives,

$$V_{error} = -\left(\frac{176 \times 10^{-18} + 0.5(1.58 \times 10^{-15})}{1 \times 10^{-12}}\right) \left(\sqrt{\frac{314 \times 10^{-6}}{220 \times 10^{-6}}} - \frac{176 \times 10^{-18}}{1 \times 10^{-12}}(1 + 1.774 - 0)\right) \\ = -1.64\text{mV}$$

Comment:

These results are not expected to give precise answers regarding the amount of charge feedthrough one should expect in an actual circuit. Rather, they are a guide to understand the effects of various circuit elements and terminal conditions in order to minimize unwanted behavior by design techniques.

Solutions to Charge Injection

- 1.) Use minimum size switches to reduce the overlap capacitances and/or increase C_L .
- 2.) Use a dummy compensating transistor.

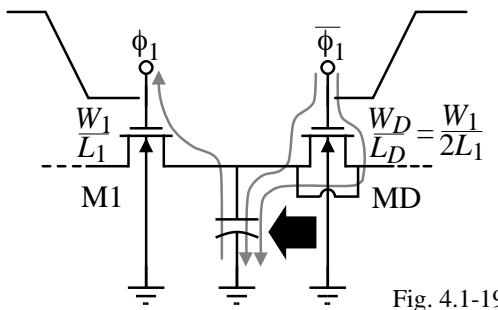


Fig. 4.1-19

- Requires complementary clocks
 - Complete cancellation is difficult and may in fact make the feedthrough worse
- 3.) Use complementary switches (transmission gates)
 - 4.) Use differential implementation of switched capacitor circuits (probably the best solution)

Input-Dependent Charge Injection

Examination of the error voltage reveals that,

$$\text{Error voltage} = \text{Component independent of input} + \text{Component dependent on input}$$

This only occurs for switches that are floating and is due to the fact that the input influences the voltage at which the transistor switches ($v_{in} \approx V_S \approx V_D$). Leads to spurious responses and other undesired results.

Solution:

Use delayed clocks to remove the input-dependence by removing the path for injection from the floating switches.

Assume that C_s is charged to V_{in} (both ϕ_1 and ϕ_{1d} are high):

- 1.) ϕ_1 opens, no input-dependent feedthrough because switch terminals (S3) are at ground potential.
- 2.) ϕ_{1d} opens, no feedthrough occurs because there is no current path (except through small parasitic capacitors).

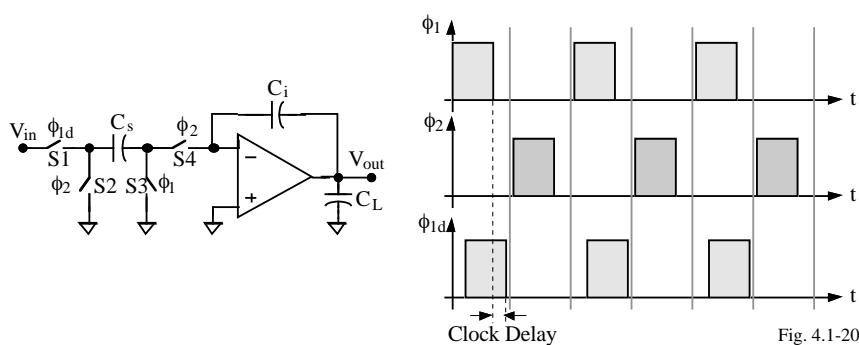


Fig. 4.1-20

CMOS Switches (Transmission Gate)

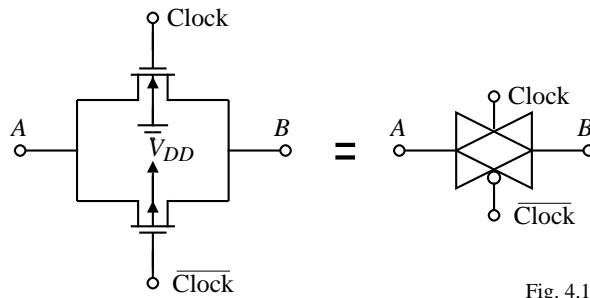


Fig. 4.1-21

Advantages:

- Feedthrough somewhat diminished
- Larger dynamic range
- Lower ON resistance

Disadvantages:

- Requires a complementary clock
- Requires more area

Example 3 - Charge Injection for a CMOS Switch

Calculate the effect of charge feedthrough on the circuit shown below. Assume that $U = 5V/50ns = 10^8V/s$, $v_{in} = 2.5V$ and ignore the bulk effect. Use the model parameters from Tables 3.1-2 and 3.2-1.

Solution

First we must identify the transition behavior. For the NMOS transistor we have

$$\frac{\beta_N V_{HTN}}{2C_L} = \frac{110 \times 10^{-6} \cdot (5-2.5-0.7)^2}{2 \cdot 10^{-12}} = 1.78 \times 10^8$$

For the PMOS transistor, noting that

$$V_{HTP} = V_S - |V_{TP}| - V_L = 2.5 - 0.7 - 0 = 1.8$$

we have $\frac{\beta_P V_{HTP}}{2C_L} = \frac{50 \times 10^{-6} \cdot (1.8)^2}{2 \cdot 10^{-12}} = 8.10 \times 10^7$. Thus, the NMOS transistor is in the slow transition and the PMOS transistor is in the fast transition regimes.

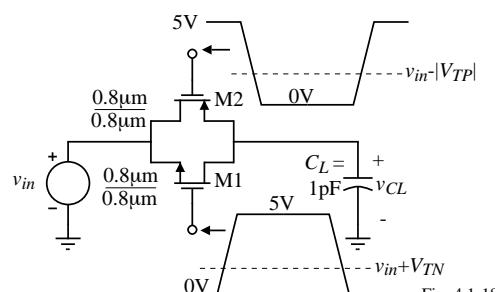


Fig. 4.1-18

Example 3 - Continued

Error due to NMOS (slow transition):

$$V_{error}(\text{NMOS}) = -\left(\frac{176 \times 10^{-18} + 0.5(1.58 \times 10^{-15})}{10^{-12}}\right) \sqrt{\frac{\pi \cdot 108 \cdot 10^{-12}}{2 \cdot 110 \cdot 10^{-6}}} - \frac{176 \times 10^{-18}}{10^{-12}} (2.5 + 1.4 - 0)$$

$$= -1.840 \text{ mV}$$

Error due to PMOS (fast transition):

$$V_{error}(\text{PMOS}) = \left(\frac{176 \times 10^{-18} + 0.5(1.58 \times 10^{-15})}{10^{-12}}\right) \left(1.8 - \frac{50 \times 10^{-6}(1.8)^3}{6 \cdot 108 \cdot 10^{-12}}\right) + \frac{176 \times 10^{-18}}{10^{-12}} (5 + 1.4 - 2.5)$$

$$= 1.956 \text{ mV}$$

Net error voltage due to charge injection is $116 \mu\text{V}$. This will vary with V_S .

Dynamic Range of the CMOS Switch

The switch dynamic range is the range of voltages at the switch terminals ($V_A \approx V_B = V_{A,B}$) over which the ON resistance is small.

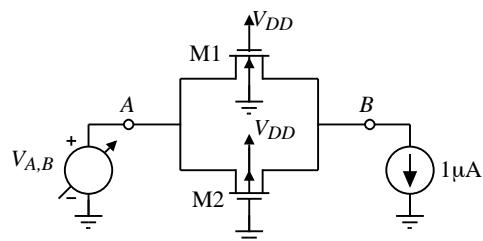


Fig. 4.1-22

Spice File:

```
Simulation CMOS transmission switch resistance
M1 1 3 2 0 MNMOS L=1U W=10U
M2 1 0 2 3 MPMOS L=1U W=10U
.MODEL MNMOS NMOS VTO=0.7, KP=110U,
+LAMBDA=0.04, GAMMA=0.4, PHI=0.7
.MODEL MPMOS PMOS VTO=-0.7, KP=50U,
+ LAMBDA=0.05, GAMMA=0.5, PHI=0.8
```

Result:

Low ON resistance over a wide voltage range is difficult as the power supply decreases.

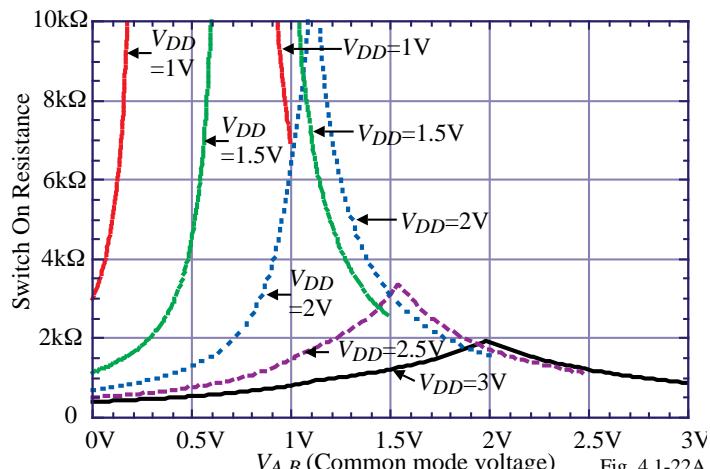


Fig. 4.1-22A

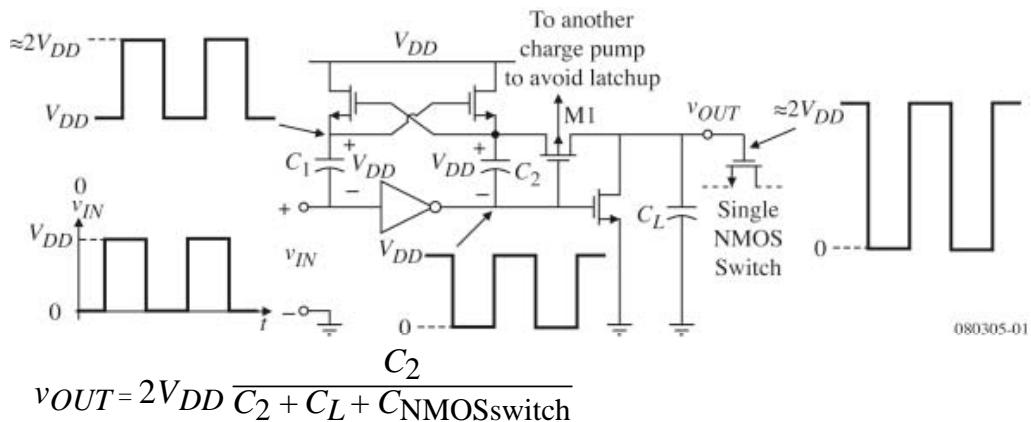
```
VDD 3 0
VAB 1 0
IA 2 0 DC 1U
.DC VAB 0 3 0.02 VDD 1 3 0.5
.PRINT DC V(1,2)
.END
```

Charge Pumps for Switches with Low Power Supply Voltages

As power supply voltages decrease below 2V, it becomes difficult to keep the switch on at a low value of on-resistance over the range of the power supply. The result is that r_{ON} becomes a function of the signal amplitude and produces harmonics.

Consequently, charge pumps are used to provide a gate voltage above power supply.

Principle of a charge pump:



Simulation of the Charge Pump Circuit[†]

Circuit:

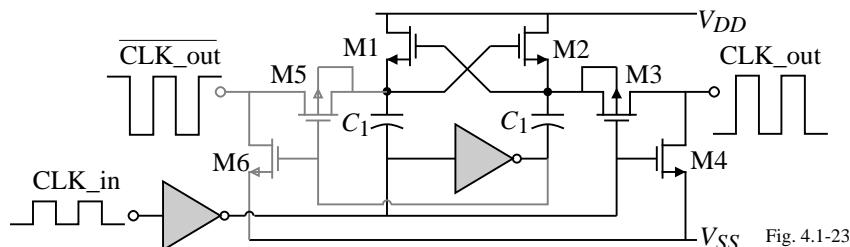


Fig. 4.1-23

Simulation:

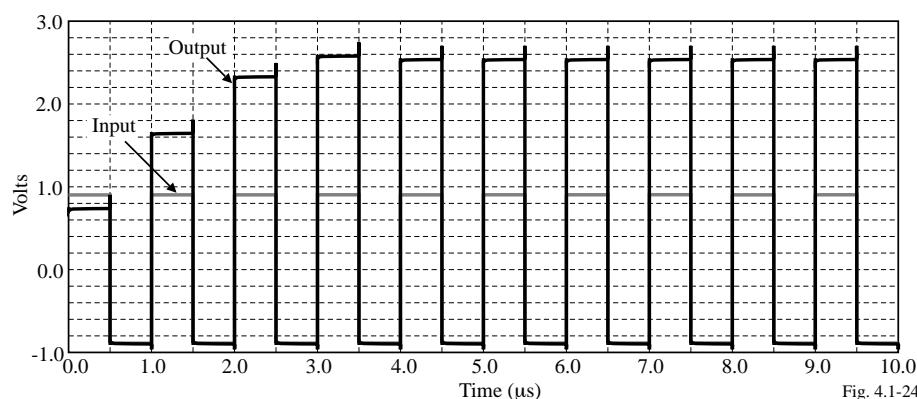


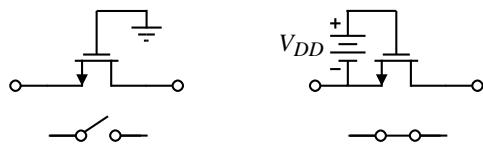
Fig. 4.1-24

[†] T.B. Cho and R.R. Gray, "A 10b, 20 Msample/s, 35mW Pipeline A/D Converter," *IEEE J. of Solid-State Circuits*, Vol. 30, No. 3m March 1995, pp. 166-172.

Bootstrapped Switches with High Reliability[†]

In the previous charge pump switch driver, the amount of gate-source drive depends upon the input signal and can easily cause reliability problems because it becomes too large for low values of input signal.

The solution to this problem is a → bootstrapped switch as shown.



Actual bootstrap switch:

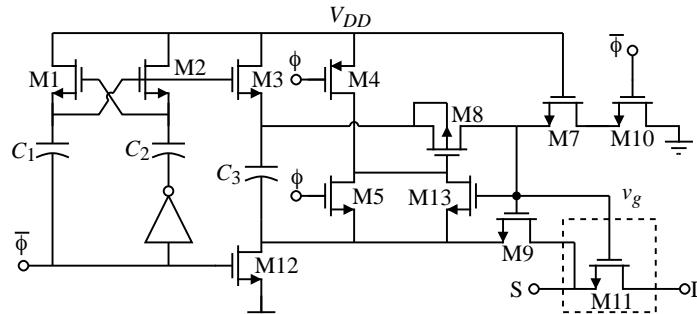


Fig. 4.1-25

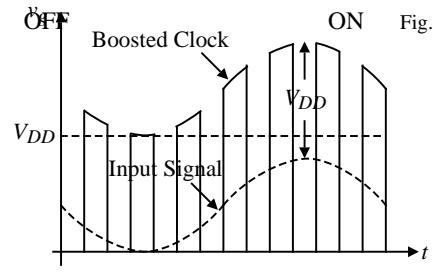


Fig. 4.1-26

ϕ low: M7 and M10 make $v_g=0$ and C_3 charges to V_{DD} , ϕ high: C_3 connected to v_{GS11} .

M7 reduces the v_{DS} and v_{GS} of M10 when $\phi = 0$. M13 ensures that $v_{GS8} \leq V_{DD}$.

The parasitics at the source of M11 require this node to be driven from a low impedance.

[†] A.M. Abo and P.R. Gray, "A 1.5V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter, *IEEE J. of Solid-State Circuits*, Vol. 34, No. 5, May 1999, pp. 599-605.
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MOSFET DIODE

MOS Diode

When the MOSFET has the gate connected to the drain, it acts like a diode with characteristics similar to a pn-junction diode.

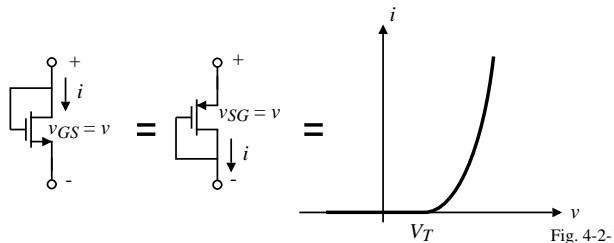


Fig. 4-2-

Note that when the gate is connected to the drain of an enhancement MOSFET, the MOSFET is *always* in the saturation region.

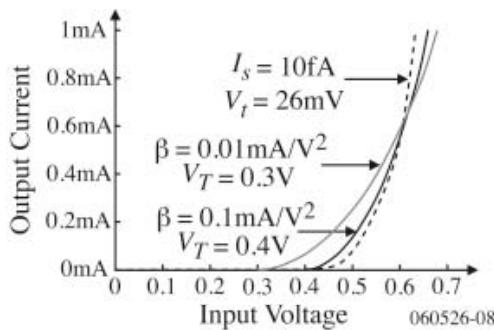
$$v_{DS} \geq v_{GS} - V_T \quad \Rightarrow \quad v_D - v_S \geq v_G - v_S - V_T \Rightarrow \quad v_D - v_G \geq -V_T \quad \Rightarrow \quad v_{DG} \geq -V_T$$

Since V_T is always greater than zero for an enhancement device, then $v_{DG} = 0$ satisfies the conditions for saturation.

- Works for NMOS or PMOS
 - Note that the drain could be V_T less than the gate and still be in saturation

How Does the MOS Diode Compare with a *pn* Diode?

The comparison is basically the difference between an exponential and a square-law function. However, if the designer is willing to spend W/L , the comparison becomes more interesting as shown below.



If the threshold voltage is less than 0.4V, the MOS diode is a clear winner over the *pn* junction diode even for modest W/L ratios.

SUMMARY

- Symmetrical switching characteristics
- High OFF resistance
- Moderate ON resistance (OK for most applications)
- Clock feedthrough is proportional to size of switch (W) and inversely proportional to switching capacitors.
- Output offset due to clock feedthrough has 2 components:
 - Input dependent
 - Input independent
- Complementary switches help increase dynamic range.
- Fully differential operation should minimize the clock feedthrough.
- As power supply reduces, floating switches become more difficult to fully turn on.
- Switches contribute a kT/C noise which can get folded back into the baseband.
- The gate-drain connected MOSFET can make a good diode realization

LECTURE 150 – RESISTOR IMPLEMENTATIONS AND CURRENT SINKS AND SOURCES

LECTURE ORGANIZATION

Outline

- Resistor implementations
- Simple current sinks and sources
- Improved performance current sinks and sources
- Summary

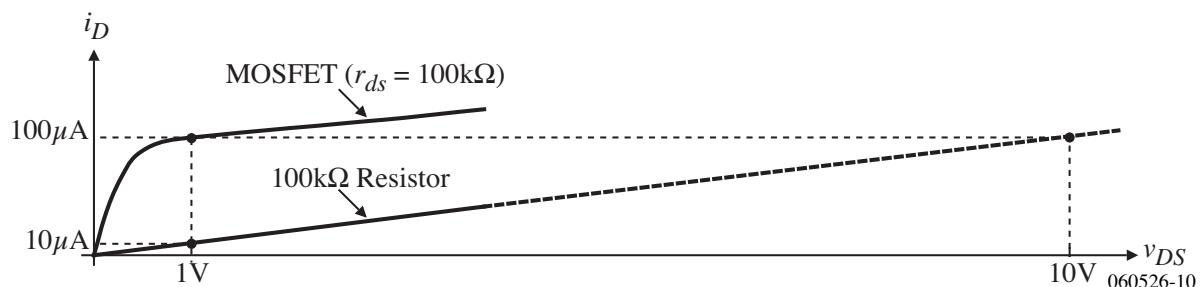
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 126-134

RESISTOR IMPLEMENTATION USING MOSFETS

Real Resistors versus MOSFET Resistors

- Smaller in area than actual resistors
- Can pass a large current through a large resistance without a large voltage drop



$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_{ds}}$$

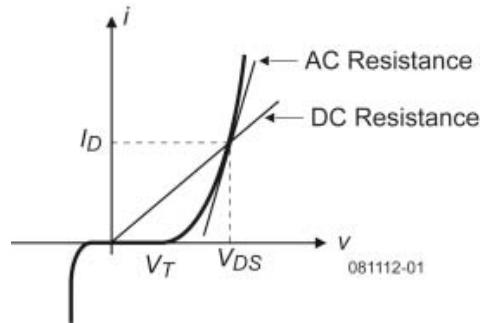
where

$$g_{ds} \approx \frac{\beta}{2} (V_{GS} - V_T)^2 \lambda = I_D \lambda$$

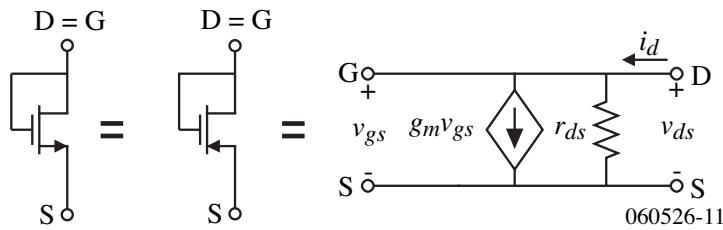
MOS Diode as a Resistor

AC and DC resistance:

$$\text{DC resistance} = \frac{V_{DS}}{I_D} = \frac{V_T}{I_D} + \sqrt{\frac{2}{\beta I_D}}$$



Small-Signal Load (AC resistance):



$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m}$$

where

$$g_m = \beta(V_{GS} - V_T) = \sqrt{2\beta I_D}$$

Use of the MOSFET to Implement a Floating Resistor

In many applications, it is useful to implement a resistance using a MOSFET. First, consider the simple, single MOSFET implementation.

$$R_{AB} = \frac{L}{K'W(V_{GS} - V_T)}$$

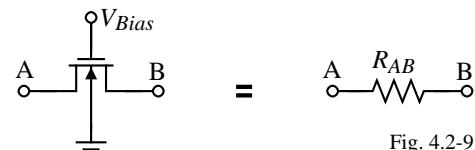


Fig. 4.2-9

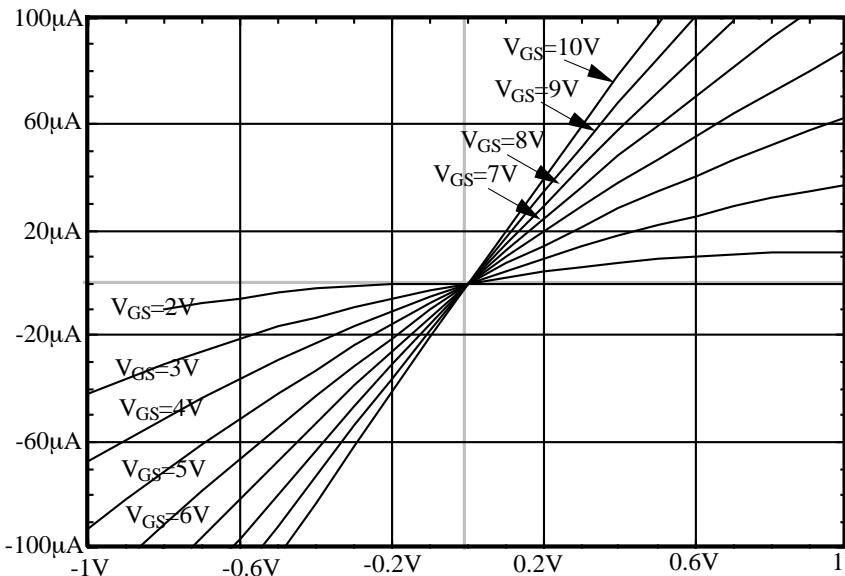
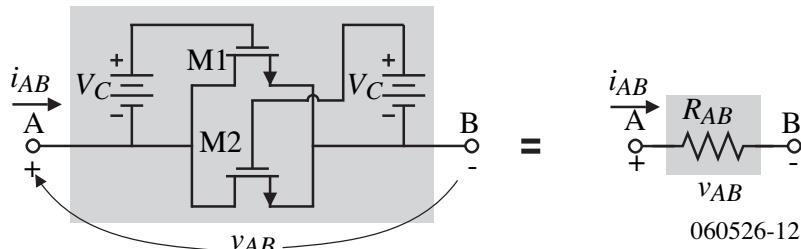


Fig. 4.2-95

Cancellation of Second-Order Voltage Dependence – Parallel MOSFETs

Circuit:

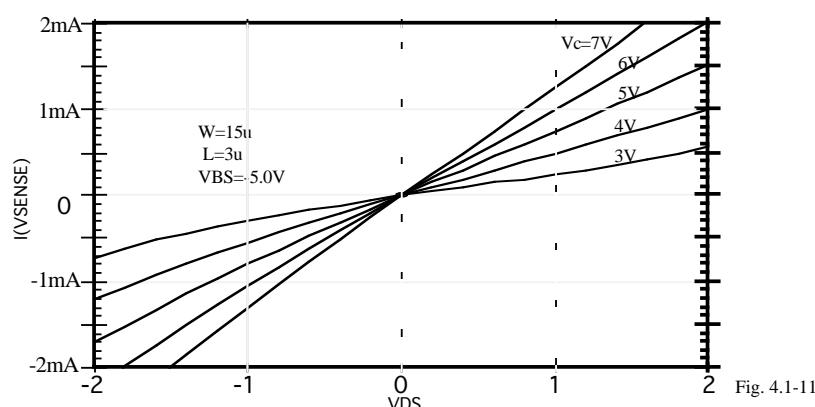


Assume both devices are non-saturated

$$\begin{aligned} i_{D1} &= \beta_1 \left[(v_{AB} + V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2} \right] \\ i_{D2} &= \beta_2 \left[(V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2} \right] \\ i_{AB} &= i_{D1} + i_{D2} = \beta \left[v_{AB}^2 + (V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2} + (V_C - V_T)v_{AB} - \frac{v_{AB}^2}{2} \right] \\ i_{AB} &= 2\beta(V_C - V_T)v_{AB} \quad \Rightarrow \quad R_{AB} = \frac{1}{2\beta(V_C - V_T)} \end{aligned}$$

Parallel MOSFET Performance

Voltage-Current Characteristic:



SPICE Input File:

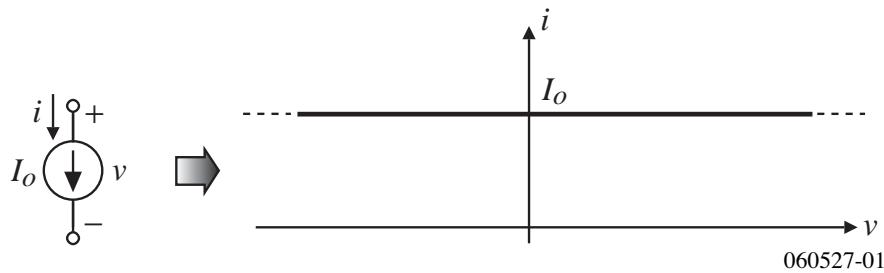
```
NMOS parallel transistor realization
M1 2 1 0 5 MNMOS W=15U L=3U
M2 2 4 0 5 MNMOS W=15U L=3U
.MODEL MNMOS NMOS VTO=0.75, KP=25U, +LAMBDA=0.01,
GAMMA=0.8 PHI=0.6
VC 1 2
E1 4 0 1 2 1.0
VSENSE 10 2 DC 0
```

```
VDS 10 0
VSS 5 0 DC -5
.DC VDS -2.0 2.0 .2 VC 3 7 1
.PRINT DC I(VSENSE)
.PROBE
.END
```

SIMPLE CURRENT SINKS AND SOURCES

Ideal Current Sinks and Sources

What is an ideal current sink or source?



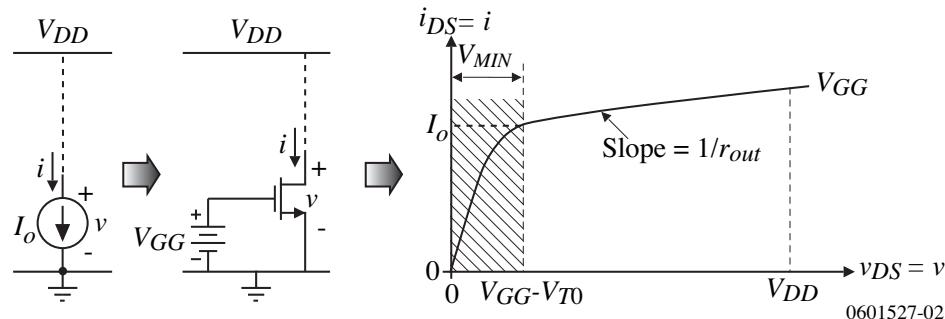
- Current is fixed at a value of I_o
- Voltage can be any value from $+\infty$ to $-\infty$
- Be careful when using a current sink or source to replace a MOSFET sink/source in simulation

Characterization of MOSFET Sinks and Sources

A sink/source is characterized by two quantities:

- r_{out} - a measure of the “flatness” of the current sink/source (its independence of voltage)
- V_{MIN} - the min. across the sink or source for which the current is no longer constant

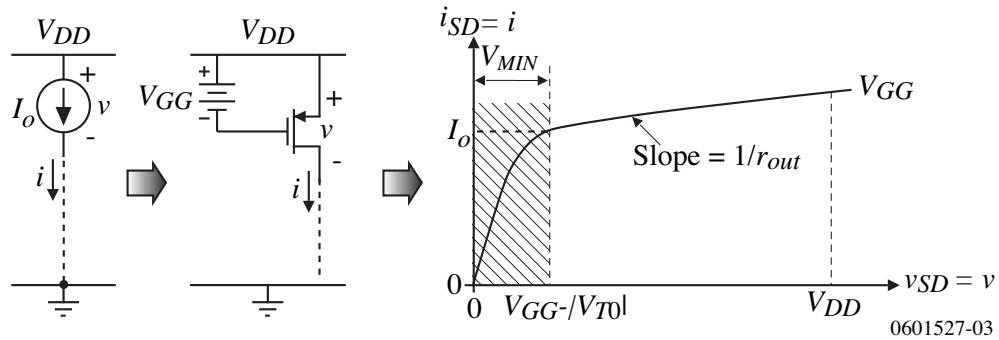
NMOS Current Sink:



$$r_{out} = \frac{1}{di_D/dv_{DS}} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D} \quad \text{and} \quad V_{MIN} = V_{DS(\text{sat})} = V_{GS} - V_{T0} = V_{GG} - V_{T0}$$

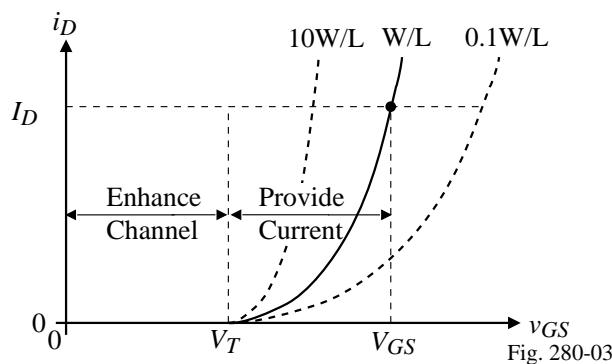
Note: The NMOS current sink can only have positive values of v .

PMOS Current Source



Gate-Source Voltage Components

It is important to note that the gate-source voltage consists of two parts as illustrated below:



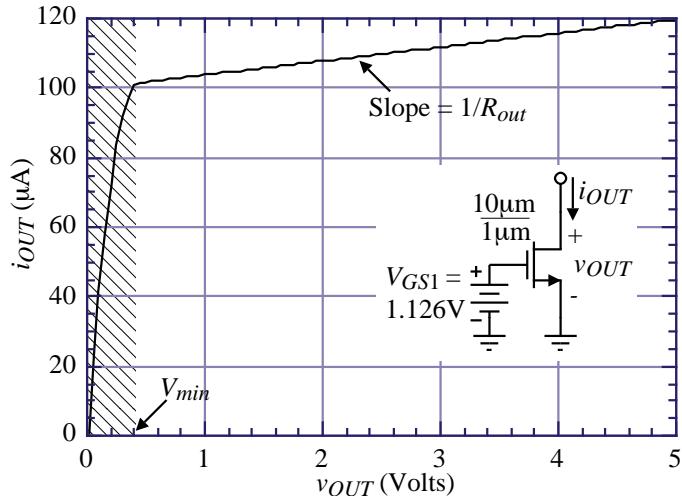
$V_{GS} = V_{T0} + V_{ON}$ = Part to enhance the channel + Part to cause current flow
where

$$V_{ON} = V_{DS(\text{sat})} = V_{GS} - V_{T0}$$

$$\therefore V_{MIN} = V_{ON} = V_{DS(\text{sat})} = \sqrt{\frac{2I_D}{K'(W/L)}} \quad \text{for the simple current sink.}$$

Note that V_{MIN} can be reduced by using large values of W/L.

Simulation of a Simple MOS Current Sink



Comments:

V_{MIN} is too large - desire V_{MIN} to approach zero, at least approach $V_{CE}(\text{sat})$

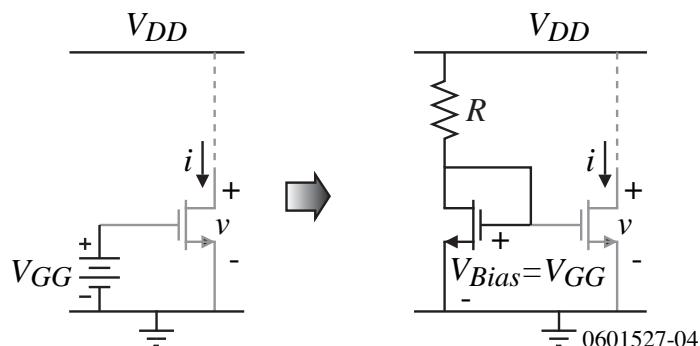
Slope too high - desire the characteristic to be flat implying very large output resistance

$$(K_N' = 110 \mu\text{A}/\text{V}^2, V_T = 0.7\text{V} \text{ and } \lambda = 0.04\text{V}^{-1}) \Rightarrow r_{ds} = 250\text{k}\Omega$$

How is V_{GG} Implemented?

The only voltage source assumed available is V_{DD} .

Therefore, V_{GG} , can be implemented in many ways with the example below being one way.



Better and more stable implementations of V_{GG} will be shown later.

IMPROVED PERFORMANCE CURRENT SINKS

Improving the Performance of the Simple NMOS Current Sink

The simple NMOS current sink shown previously had two problems.

- 1.) The value of V_{MIN} may be too large.
- 2.) The output resistance ($250\text{k}\Omega$) was too small.

How can the designer solve these problems?

- 1.) The first problem can be solved by increasing the W/L value of the NMOS transistor.

$$V_{MIN} = V_{ON} = V_{DS(\text{sat})} = \sqrt{\frac{2I_D}{K'(W/L)}}$$

In the simulation shown previously,

$$V_{MIN} = \sqrt{\frac{2 \cdot 100\mu\text{A}}{110\mu\text{A}/\text{V}^2 \cdot 10}} = 0.426\text{V}$$

We could decrease this to 0.1V with a $W/L = 182$.

- 2.) How can the small output resistance be increased? Answer is feedback.

Blackman's Formula for Finding the Resistance at a Port with Feedback[†]

Blackman's formula to find the resistance at a port X , is based on the following circuit:

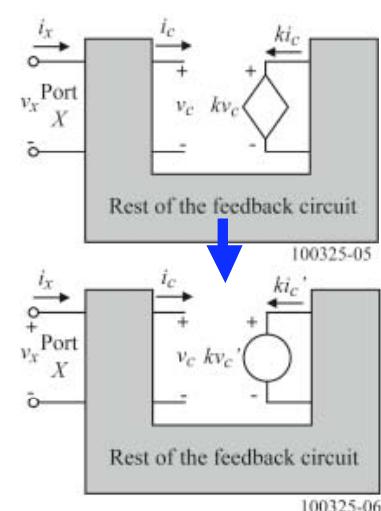
The resistance seen looking into port X is given as,

$$R_x = R_x(k=0) \left[\frac{1 + RR(\text{port shorted})}{1 + RR(\text{port opened})} \right]$$

The return ratio, RR , is found by changing the dependent source to an independent source as shown:

Therefore, the return ratio is defined as,

$$RR = -\frac{v_c}{v_c'} = -\frac{i_c}{i_c'}$$



The key is to find a feedback circuit that when we calculate the RR , it is non-zero when port X is shorted and zero when port X is opened. In this case, the resistance at port X is

$$R_x = R_x(k=0)[1 + RR(\text{port shorted})]$$

[†] R.B. Blackman, "Effect of Feedback on Impedance," *Bell Sys. Tech.J.*, Vol. 23, pp. 269-277, October 1943.

Identification of the Proper Type of Feedback

For the port X , the circuit variables associated with the input port should be able to be expressed as,

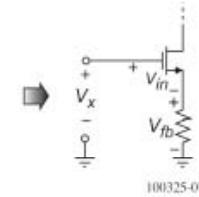
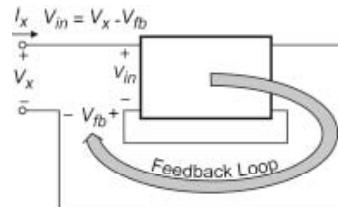
Input Variable to Port X = Signal variable to the circuit – Feedback variable

where the variables can be voltage or current.

- 1.) Series feedback (variables are voltage):

$$RR(V_x = 0) \neq 0$$

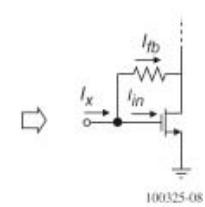
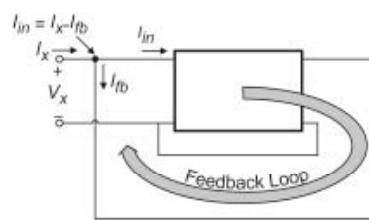
$RR(I_x = 0) = 0$ (V_{in} is disconnected from V_{fb})



- 2.) Shunt feedback (variables are current):

$$RR(V_x = 0) = 0 \quad (I_{in} \text{ is disconnected from } I_{fb})$$

$$RR(I_x = 0) \neq 0$$



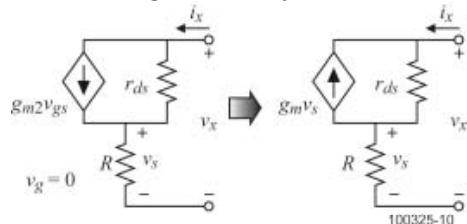
We see that for series feedback RR (port opened) will be zero and for shunt feedback that RR (port shorted) will be zero.

Increasing the Output Resistance of the Simple Current Sink

Choosing series feedback, we select the following circuit to boost the output resistance of the simple current sink:

Assume that we can neglect the bulk effect and find the input resistance by 1.) small-signal analysis and 2.) return ratio method.

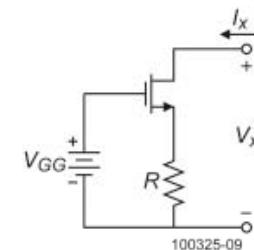
- 1.) Small-signal Analysis:



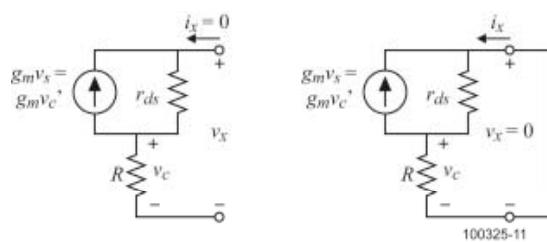
$$v_x = (i_x + g_m v_s) r_{ds} + i_x R$$

$$v_x = (i_x + g_m i_x R) r_{ds} + i_x R = i_x (1 + R + g_m r_{ds} R)$$

$$\therefore R_x = \frac{v_x}{i_x} = 1 + R + g_m r_{ds} R \approx g_m r_{ds} R$$



- 2.) Return Ratio:



$$R_x(k=0) = R_x(g_m=0) = r_{ds} + R$$

$$RR(v_x = 0) = -\frac{v_c}{v_c} = g_m \left(\frac{r_{ds} R}{r_{ds} + R} \right)$$

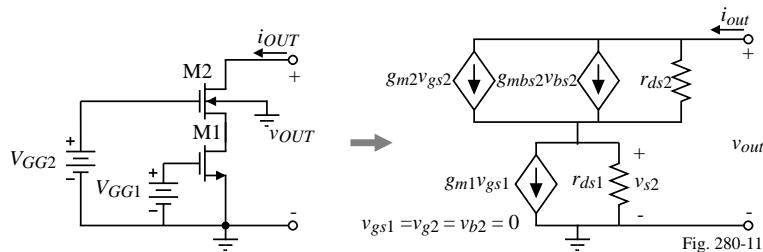
$$RR(i_x = 0) = 0$$

$$\therefore R_x = (r_{ds} + R) \left[1 + g_m \left(\frac{r_{ds} R}{r_{ds} + R} \right) \right]$$

$$= 1 + R + g_m r_{ds} R \approx g_m r_{ds} R$$

Cascode Current Sink

Replacing R with the simple current sink leads to a practical implementation shown as:



Small signal output resistance:

Noting that $v_{gs1} = v_{g2} = v_{b2} = 0$ and writing a loop equation we get,

$$v_{out} = (i_{out} - g_{m2}v_{gs2} - g_{mbs2}v_{bs2})r_{ds2} + r_{ds1}i_{out}$$

However,

$$v_{gs2} = 0 - v_{s2} = -i_{out}r_{ds1} \quad \text{and} \quad v_{bs2} = 0 - v_{s2} = -i_{out}r_{ds1}$$

Therefore,

$$v_{out} = i_{out}[r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2} + g_{mbs2}r_{ds1}r_{ds2}]$$

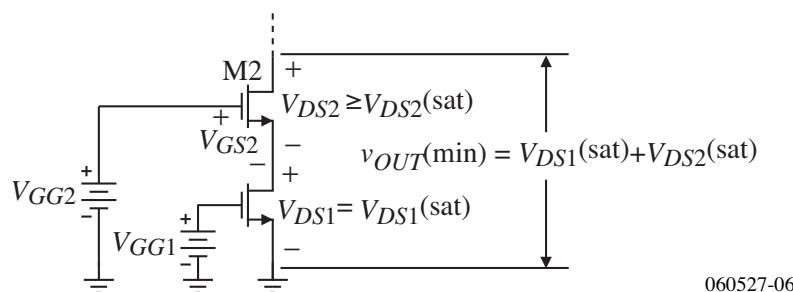
or

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2} + g_{mbs2}r_{ds1}r_{ds2} \approx g_{m2}r_{ds1}r_{ds2}$$

A general principle is beginning to emerge:

The output resistance of a cascode circuit $\approx R \times (\text{Common source voltage gain of the cascading transistor})$

Design of V_{GG1} and V_{GG2}



- 1.) V_{GG1} is selected to provide the desired current. M1 is assumed to be in saturation.
- 2.) V_{GG2} is selected to keep V_{DS1} as small as possible and still be in saturation.

$$V_{GG2} = V_{DS1}(\text{sat}) + V_{GS2} = V_{DS1}(\text{sat}) + V_T + V_{DS2}(\text{sat})$$

$$\text{If } W_1/L_1 = W_2/L_2, \text{ then } V_{GG2} = 2V_{DS}(\text{sat}) + V_T = 2V_{ON} + V_T$$

Thus, for the previous NMOS current sink, V_{GG2} would be equal to,

$$V_{GG2} = 2(0.426) + 0.7 = 1.552\text{V}$$

Simulation of the Cascode CMOS Current Sink

Example

Use the model parameters $K_N = 110 \mu\text{A/V}^2$, $V_T = 0.7$ and $\lambda_N = 0.04 \text{V}^{-1}$ to calculate (a) the small-signal output resistance for the simple current sink if $I_{OUT} = 100 \mu\text{A}$ and (b) the small-signal output resistance for the cascode current sink with $I_{OUT} = 100 \mu\text{A}$. Assume that all W/L values are 1.

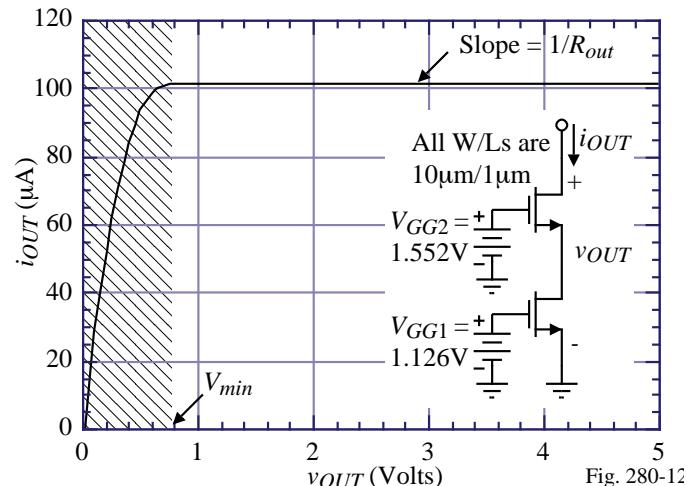


Fig. 280-12

Solution

(a) Using $\lambda = 0.04 \text{ V}^{-1}$ and $I_{OUT} = 100\mu\text{A}$ gives $r_{ds1} = 250\text{k}\Omega = r_{ds2}$. (b) Ignoring the bulk effect, we find that $g_{m1} = g_{m2} = 469\mu\text{S}$ which gives $r_{out} = (250\text{k}\Omega)(469\mu\text{S})(250\text{k}\Omega) = 29.32\text{M}\Omega$.

High-Swing Cascode Current Sink

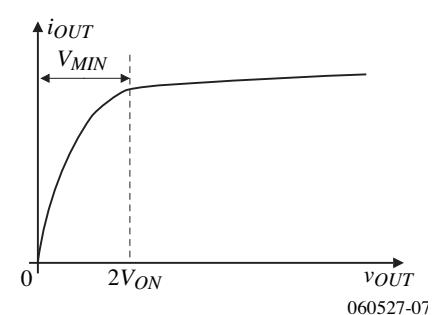
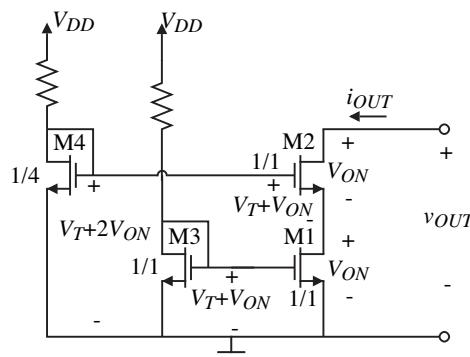
This current sink achieves the smallest possible V_{MIN} .

Since

$$V_{ON} = \sqrt{\frac{2I_D}{K'(W/L)}}$$

,
then if L/W of M4
is quadrupled, then
 V_{ON} is doubled.

$$\therefore V_{MIN} \equiv 2V_{ON}$$



060527-07

Example

Use the cascode current sink configuration above to design a current sink of $100\mu\text{A}$ and a $V_{MIN} = 1\text{V}$. Assume the device parameters of Table 3.1-2.

Solution

With $V_{MIN} = 1V$, choose $V_{ON} = 0.5V$. Assuming M1 and M2 are identical gives

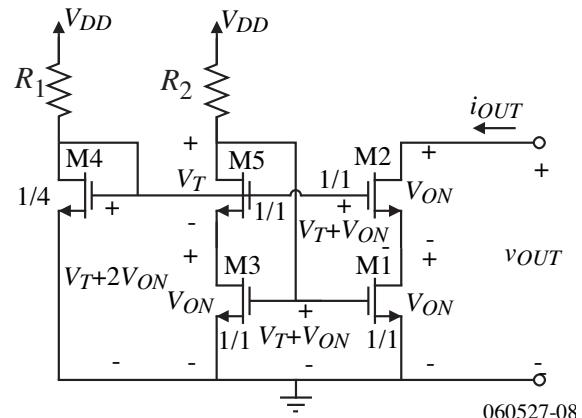
$$\frac{W}{L} = \frac{2 \cdot I_{OUT}}{K' \cdot V_{ON}^2} = \frac{2 \cdot 100 \times 10^{-6}}{110 \times 10^{-6} \times 0.25} = 7.27 \Rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \underline{\underline{7.27}} \text{ and } \frac{W_4}{L_4} = \underline{\underline{1.82}}$$

Improved High-Swing Cascode Current Sink

Because the drain-source voltages of the matching transistors, M1 and M3 are not equal, $i_{OUT} \neq I_{REF}$.

To circumvent this problem the cascode current sink shown is utilized:

Note that the drain-source voltage of M1 and M3 are identical causing i_{OUT} to be a replication of I_{REF} .



Design Procedure

- 1.) Since $V_{MIN} = 2V_{ON} = 2V_{DS(\text{sat})}$, let $V_{ON} = 0.5V_{MIN}$.
 - 2.) $V_{ON} = \sqrt{\frac{2I_{REF}}{K'(W/L)}}$ $\Rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{2I_{REF}}{K'V_{ON}^2} = \frac{8I_{REF}}{K'V_{MIN}^2}$
 - 3.) $\frac{W_4}{L_4} = \frac{2I_{REF}}{K'(V_{GS4}-V_T)^2} = \frac{2I_{REF}}{K'(2V_{ON})^2} = \frac{I_{REF}}{2K'V_{ON}^2}$

Signal Flow in Transistors

The last example brings up an interesting and important point. This point is illustrated by the following question, "How does I_{REF} flow into the M3-M5 combination of transistors since there is no path to the gate of M5?"

Consider how signals flow in transistors:

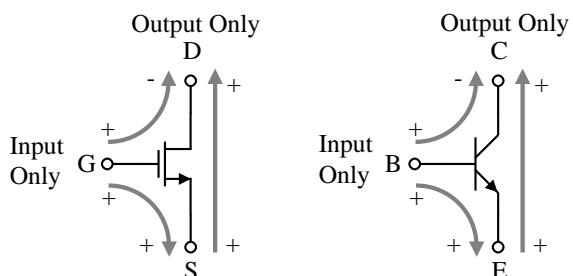


Fig. 4.3-12E

Answer to the above question:

As V_{DD} increases (i.e. the circuit begins to operate), I_{REF} cannot flow into the drain of M5, so it flows through the path indicated by the arrow to the gate of M3. It charges the stray capacitance and causes the gate-source voltage of M3 to increase to the exact value necessary to cause I_{REF} to flow through the M3-M5 combination.

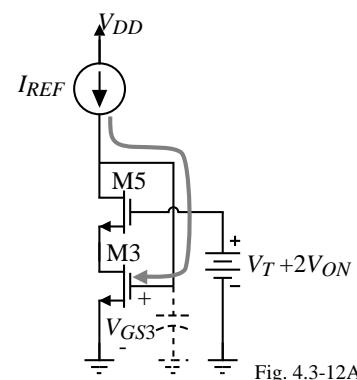


Fig. 4.3-12A

Example 150-1 - Design of a Minimum V_{MIN} Current Sink

Assume $I_{REF} = 100\mu A$ and design a cascode current sink with a $V_{MIN} = 0.3V$ using the following parameters: VTO=0.7, KP=110U, LAMBDA=0.04, GAMMA=0.4, PHI=0.7

Solution

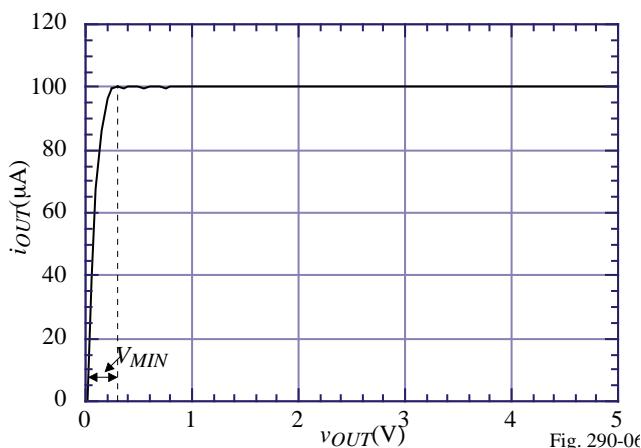
From the previous equations, we get

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{W_3}{L_3} = \frac{W_5}{L_5} = \frac{8I_{REF}}{K'V_{MIN}^2} = \frac{8 \cdot 100}{110 \cdot (0.3V)^2} = 80.8 \text{ and}$$

$$\frac{W_4}{L_4} = \frac{I_{REF}}{2K'V_{ON}^2} = \frac{100}{2 \cdot 110 \cdot 0.15^2} = 20.2$$

Simulation Results:

```
Low Vmin Cascade Current Sink - Method No. 2
M1 5 1 0 0 MNMOS W=81U L=1U
M2 2 3 5 5 MNMOS W=81U L=1U
M3 4 1 0 0 MNMOS W=81U L=1U
M4 3 3 0 0 MNMOS W=20U L=1U
M5 1 3 4 4 MNMOS W=81U L=1U
.MODEL MNMOS NMOS VTO=0.7 KP=110U
+LAMBDA=0.04 GAMMA=0.4 PHI=0.7
VDD 6 0 DC 5V
IIN1 6 1 DC 100U
IIN2 6 3 DC 100U
VOUT 2 0 DC 5.0
.OP
.DC VOUT 5 0 0.05
.PRINT DC ID(M2)
.END
```



Self-Biased Cascode Current Sink[†]

The $V_T + 2V_{ON}$ bias voltage is developed through a series resistor.

Design procedure:

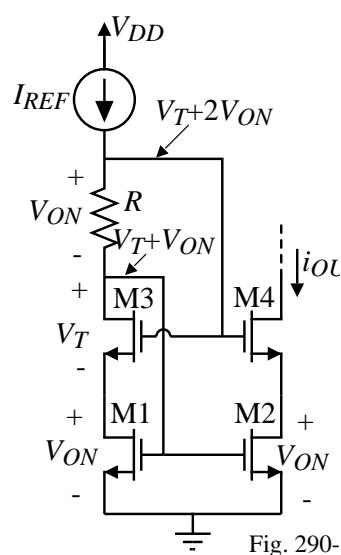
Same as the previous except

$$R = \frac{V_{ON}}{I_{REF}} = \frac{V_{MIN}}{2I_{REF}}$$

For the previous example,

$$R = \frac{0.3V}{2 \cdot 100\mu A} = 1.5k\Omega$$

If the reference current is small, R can become large.



[†] T.L. Brooks and A.L. Westwick, "A Low-Power Differential CMOS Bandgap Reference," Proc. of IEEE Inter. Solid-State Circuits Conf., Feb. 1994, pp. 248-249.

MOS Regulated Cascode Sink[†]

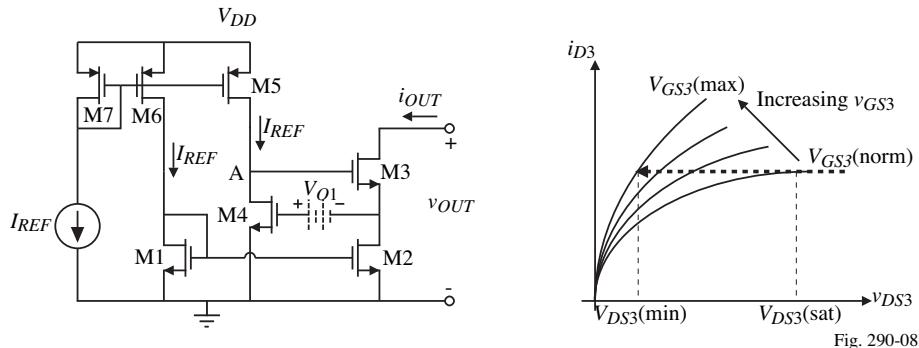


Fig. 290-08

Comments:

- Achieves very high output resistance by increasing the loop gain (return-ratio) due to the M4-M5 inverting amplifier.
- $$\text{LG} = g_{m3}r_{ds2} \frac{\left(\frac{g_{m4}}{g_{ds4}+g_{ds5}} \right)}{g_{ds4}+g_{ds5}} \approx \frac{g_{m3}r_{ds2}g_{m4}r_{ds4}}{2} \quad \text{If } r_{ds4} \approx r_{ds5}, \text{ then } r_{out}$$
- $$\approx \frac{r_{ds3}g_{m3}r_{ds2}g_{m4}r_{ds4}}{2}$$
- M3 maintains “constant” current even though it is no longer in the saturation region.

[†] E. Sackinger and W. Guggenbuhl, “A Versatile Building Block: The CMOS Differential Difference Amplifier,” *IEEE J. of Solid-State Circuits*, vol. SC-22, no. 2, pp. 287-294, April 1987.

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Regulated Cascode Current Sink - Continued

Small signal model:

Solving for the output resistance:

$$i_{out} = g_{m3}v_{gs3} + g_{ds3}(v_{out} - v_{gs4})$$

But

$$v_{gs4} = i_{out}r_{ds2}$$

and

$$v_{gs3} = v_{g3} - v_{s3} = -g_{m4}(r_{ds4}\parallel r_{ds5})v_{gs4} - v_{gs4} = -r_{ds2}[1 + g_{m4}(r_{ds4}\parallel r_{ds5})]i_{out}$$

$$\therefore i_{out} = -g_{m3}r_{ds2}[1 + g_{m4}(r_{ds4}\parallel r_{ds5})]i_{out} + g_{ds3}v_{out} - g_{ds3}r_{ds2}i_{out}$$

$$v_{out} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}\parallel r_{ds5})]i_{out}$$

$$\therefore r_{out} = \frac{v_{out}}{i_{out}} = r_{ds3}[1 + g_{m3}r_{ds2} + g_{ds3}r_{ds2} + g_{m3}r_{ds2}g_{m4}(r_{ds4}\parallel r_{ds5})]$$

$$\approx r_{ds3}g_{m3}r_{ds2}g_{m4}(r_{ds4}\parallel r_{ds5})$$

If $I_{REF} = 100\mu\text{A}$, all W/Ls are $10\mu\text{m}/1\mu\text{m}$ we get $r_{ds} = 0.25\text{M}\Omega$ and $g_m = 469\mu\text{S}$ which gives

$$r_{out} \approx (0.25\text{M}\Omega)(469\mu\text{S})(0.25\text{M}\Omega)(469\mu\text{S})(0.125\text{M}\Omega) = 1.72\text{G}\Omega$$

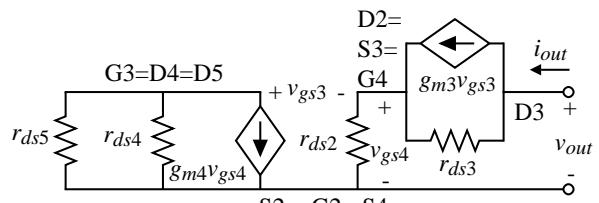


Fig. 290-09

Can $1G\Omega$ Output Resistance Really be Achieved?

No, because of substrate currents. Substrate currents are caused by impact ionization due to high electric fields cause an impact which generates a hole-electron pair. The electrons flow out the drain and the holes flow into the substrate causing a substrate current flow.

Illustration:

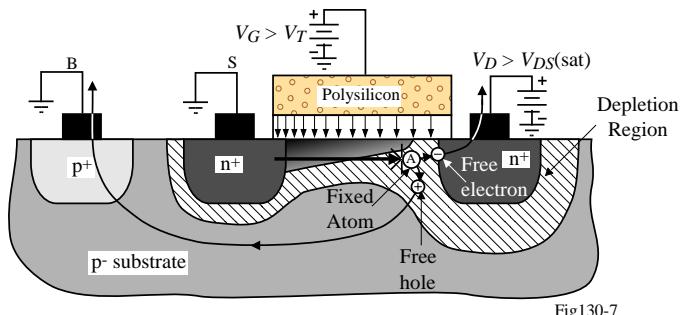


Fig130-7

Maximum output resistance $\approx 500M\Omega$ - $1G\Omega$

Model of Substrate Current Flow

Substrate current:

$$i_{DB} = K_1(v_{DS} - v_{DS(\text{sat})})i_D e^{-[K_2/(v_{DS}-v_{DS(\text{sat})})]}$$

where

K_1 and K_2 are process-dependent parameters (typical values: $K_1 = 5V^{-1}$ and $K_2 = 30V$)

Schematic model:

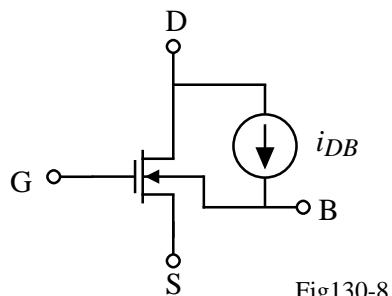


Fig130-8

Small-signal model:

$$g_{db} = \frac{\partial i_{DB}}{\partial v_{DB}} = K_2 \frac{I_{DB}}{V_{DS} - V_{DS(\text{sat})}} \approx 1nS$$

This conductance will prevent the realization of high-output resistance current sinks/sources such as the regulated cascode current sink.

Minimizing the V_{MIN} of the Regulated Cascode Current Sink

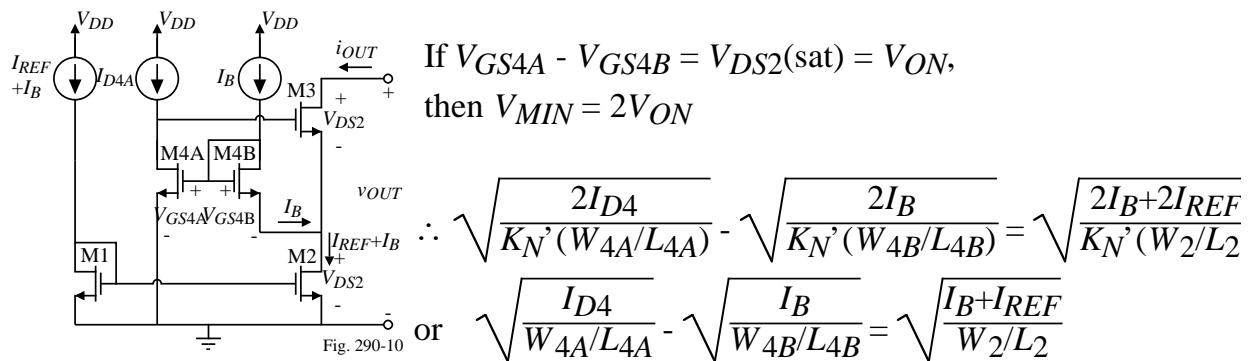
V_{MIN} :

Without the use of the V_{O1} battery shown, V_{MIN} is pretty bad. It is,

$$V_{MIN} = V_{GS4} + V_{DS3(\text{sat})} = V_T + 2V_{ON}$$

Minimizing V_{MIN} :

If $V_{O1} = V_T$, then $V_{MIN} = 2V_{ON}$. This is accomplished by the following circuit:



A number of solutions exist. For example, let $I_B = I_{REF}$. This gives $I_{D4A} = 5.824I_{REF}$ assuming all W/L ratios are identical.

Example 150-2 - Design of a Minimum V_{MIN} Regulated Cascode Current Sink

Design a regulated cascode current sink for $100\mu\text{A}$ and minimum voltage of $V_{MIN} = 0.3\text{V}$.

Solution

Let the W/L ratios of M1 through M5 be equal and let $I_B = 10\mu\text{A}$. Therefore,

$$V_{MIN} = 0.3\text{V} = V_{ON3} + V_{ON2} = \sqrt{\frac{2 \cdot 100\mu\text{A}}{110\mu\text{A}/\text{V}^2(W/L)}} + \sqrt{\frac{2 \cdot 110\mu\text{A}}{110\mu\text{A}/\text{V}^2(W/L)}}$$

$$= \sqrt{\frac{2 \cdot 100\mu\text{A}}{110\mu\text{A}/\text{V}^2(W/L)}} (\sqrt{1} + \sqrt{1.1})$$

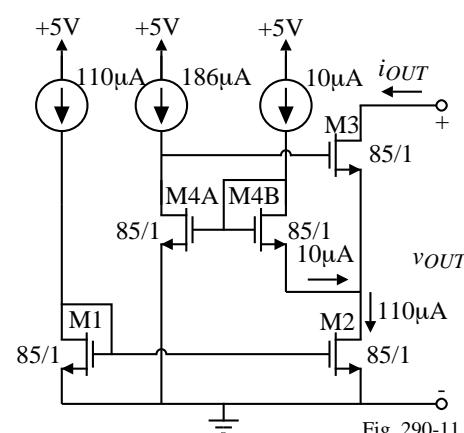
Therefore,

$$0.3\text{V} = \sqrt{\frac{2 \cdot 100\mu\text{A}}{110\mu\text{A}/\text{V}^2(W/L)}} (2.049)$$

$$\frac{W}{L} = \frac{2 \cdot 100\mu\text{A} \cdot 2.049^2}{110\mu\text{A}/\text{V}^2 \cdot 0.32} = 84.8 \approx 85.$$

With $I_B = 10\mu\text{A}$, then $I_{D4A} =$

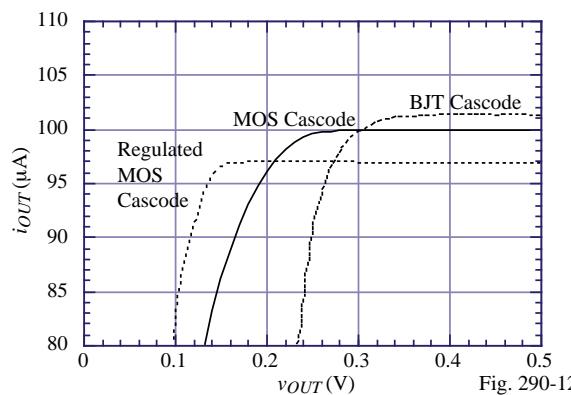
$$(\sqrt{10} + \sqrt{110})^2 = 186\mu\text{A}$$



Comparison of the MOS Cascode and Regulated Cascode Current Sink

Close examination in the knee area reveals interesting differences.

Simulation results:



Comments:

- The regulated cascode current is smaller than the cascode current because the drain-source voltages of M1 and M2 are not equal.
- The regulated cascode current sink has a smaller V_{MIN} due to the fact that M3 can have a drain-source voltage smaller than $V_{DS}(\text{sat})$

SUMMARY

Summary of Both BJT and MOS Current Sinks/Sources

Current Sink/Source	r_{OUT}	V_{MIN}
Simple MOS Current Sink	$r_{ds} = \frac{1}{\lambda I_D}$	$V_{DS}(\text{sat}) = V_{ON}$
Simple BJT Current Sink	$r_o = \frac{V_A}{I_C}$	$V_{CE}(\text{sat}) \approx 0.2V$
Cascode MOS	$\approx g_m 2 r_{ds2} r_{ds1}$	$2V_{ON}$
Cascode BJT	$\approx \beta r_o$	$2V_{CE}(\text{sat})$
Regulated Cascode Current Sink	$\approx r_{ds3} g_m 3 r_{ds2} g_m 4 (r_{ds4} r_{ds5})$	$\approx V_T + V_{ON}$
Minimum V_{MIN} Regulated Cascode Current Sink	$\approx r_{ds3} g_m 3 r_{ds2} g_m 4 (r_{ds4} r_{ds5})$	$\approx V_{ON}$

Resistor Implementations

- MOSFET resistors may use less area than actual resistors
- Linearity is the primary issue for MOSFET resistor realizations

LECTURE 160 – CURRENT MIRRORS AND SIMPLE REFERENCES

LECTURE ORGANIZATION

Outline

- MOSFET current mirrors
- Improved current mirrors
- Voltage references with power supply independence
- Current references with power supply independence
- Temperature behavior of voltage and current references

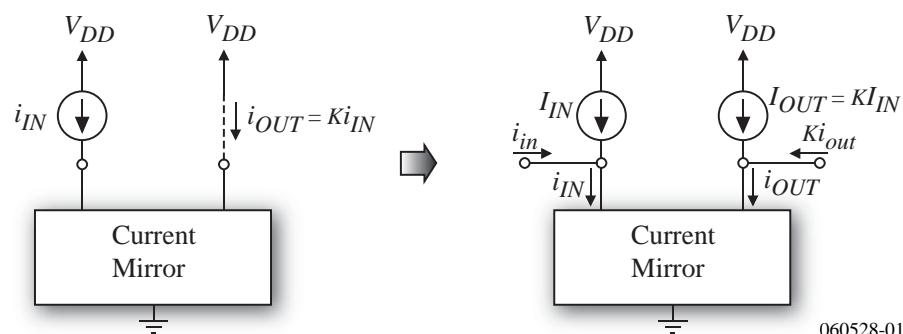
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 134-153

MOSFET CURRENT MIRRORS

What is a Current Mirror?

A current mirror replicates the input current of a current sink or current source as an output current. The output current may be identical to the input current or can be a scaled version of it.



The above current mirrors are referenced with respect to ground. Current mirrors can also be referenced with respect to V_{DD} and current sink inputs and outputs.

Characterization of Current Mirrors

A current mirror is basically nothing more than a current amplifier. The ideal characteristics of a current amplifier are:

- Output current linearly related to the input current, $i_{out} = A_i i_{in}$
- Input resistance is zero
- Output resistance is infinity

Also, the characteristic V_{MIN} applies not only to the output but also the input.

- $V_{MIN}(\text{in})$ is the range of v_{in} over which the input resistance is not small
- $V_{MIN}(\text{out})$ is the range of v_{out} over which the output resistance is not large

Graphically:

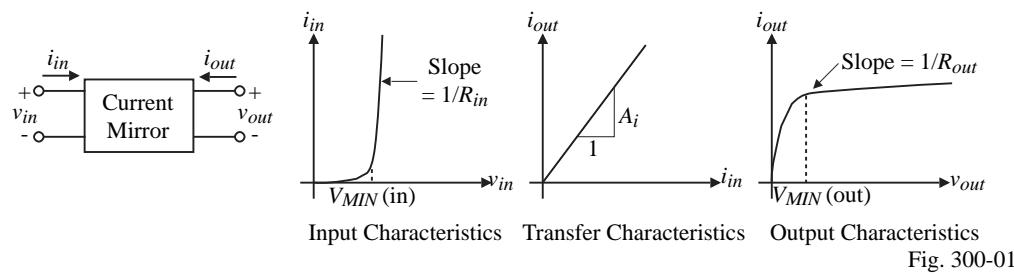


Fig. 300-01

Therefore, R_{out} , R_{in} , $V_{MIN}(\text{out})$, $V_{MIN}(\text{in})$, and A_i will characterize the current mirror.

Simple MOS Current Mirror

Circuit:

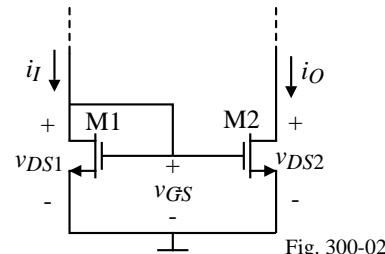


Fig. 300-02

Assume that $v_{DS2} > v_{GS} - V_{T2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2} \right) \left(\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}} \right) 2 \left[\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \left(\frac{K_2'}{K_1'} \right) \right]$$

If the transistors are matched, then $K_1' = K_2'$ and $V_{T1} = V_{T2}$ to give,

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2} \right) \left(\frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \right)$$

If $v_{DS1} = v_{DS2}$, then

$$\frac{i_O}{i_I} = \left(\frac{L_1 W_2}{W_1 L_2} \right)$$

Therefore the sources of error are:

- 1.) $v_{DS1} \neq v_{DS2}$
- 2.) M1 and M2 are not matched.

Influence of the Channel Modulation Parameter, λ

If the transistors are matched and the W/L ratios are equal, then

$$\frac{i_O}{i_I} = \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}$$

if the channel modulation parameter is the same for both transistors ($L_1 = L_2$).

Ratio error (%) versus drain voltage difference:

Note that one could use this effect to measure λ .

Measure V_{DS1}, V_{DS2} , i_I and i_O and solve the above equation for the channel modulation parameter, λ .

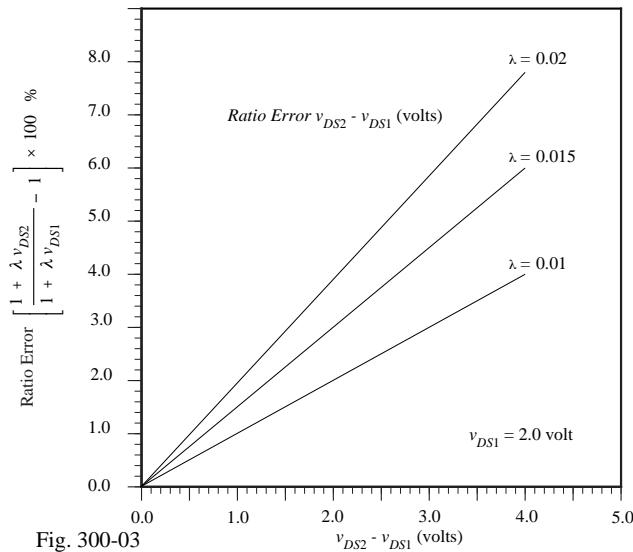


Fig. 300-03

Illustration of the Offset Voltage Error Influence

Assume that $V_T1 = 0.7V$ and $K'W/L = 110\mu A/V^2$.

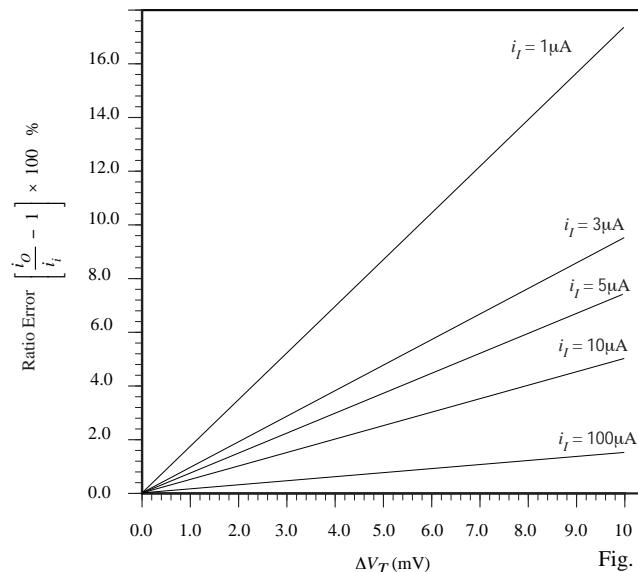


Fig. 300-4

Key: Make the part of V_{GS} causing the current to flow, V_{ON} , more significant than V_T .

Influence of Error in Aspect Ratio of the Transistors

Example 160-1 - Aspect Ratio Errors in Current Mirrors

A layout is shown for a one-to-four current amplifier. Assume that the lengths are identical ($L_1 = L_2$) and find the ratio error if $W_1 = 5 \pm 0.1 \mu\text{m}$. The actual widths of the two transistors are

$$W_1 = 5 \pm 0.1 \mu\text{m} \text{ and } W_2 = 20 \pm 0.1 \mu\text{m}$$

Solution

We note that the tolerance is not multiplied by the nominal gain factor of 4.

The ratio of

W_2 to W_1 and consequently the gain of the current amplifier is

$$\frac{i_O}{i_I} = \frac{W_2}{W_1} = \frac{20 \pm 0.1}{5 \pm 0.1} = 4 \left(\frac{1 \pm (0.1/20)}{1 \pm (0.1/5)} \right) \approx 4 \left(1 \pm \frac{0.1}{20} \right) \left(1 - \frac{\pm 0.1}{5} \right) \approx 4 \left(1 \pm \frac{0.1}{20} - \frac{\pm 0.4}{20} \right) = 4 - (\pm 0.03)$$

where we have assumed that the variations would both have the same sign (correlated). It is seen that this ratio error is 0.75% of the desired current ratio or gain.

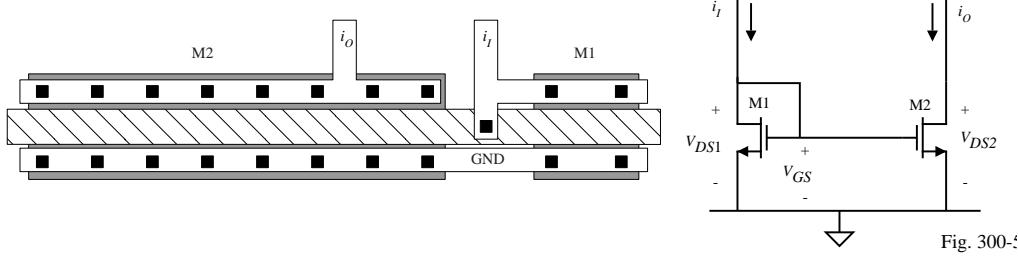


Fig. 300-4

Influence of Error in Aspect Ratio of the Transistors-Continued

Example 160-2 - Reduction of the Aspect Ratio Errors in Current Mirrors

Use the layout technique illustrated below and calculate the ratio error of a current amplifier having the specifications of the previous example.

Solutions

The actual widths of M1 and M2 are

$$W_1 = 5 \pm 0.1 \mu\text{m} \text{ and } W_2 = 4(5 \pm 0.1) \mu\text{m}$$

The ratio of W_2 to W_1 and consequently the current gain is given below and is for all practical purposes independent of layout error.

$$\frac{i_O}{i_I} = \frac{4(5 \pm 0.1)}{5 \pm 0.1} = 4$$

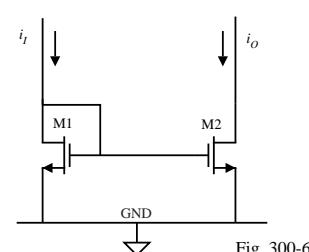
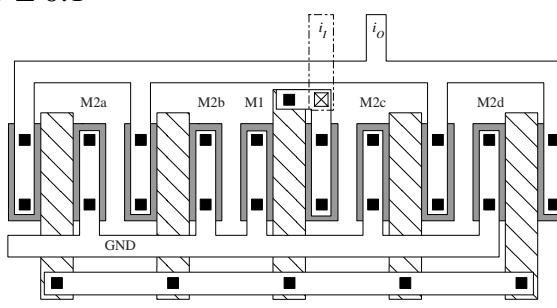


Fig. 300-6

Summary of the Simple MOS Current Mirror/Amplifier

- Minimum input voltage is $V_{MIN(in)} = V_T + V_{ON}$
Okay, but could be reduced to V_{ON} .
Principle:

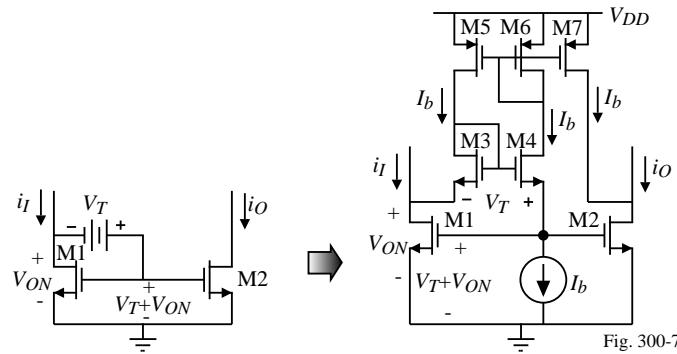


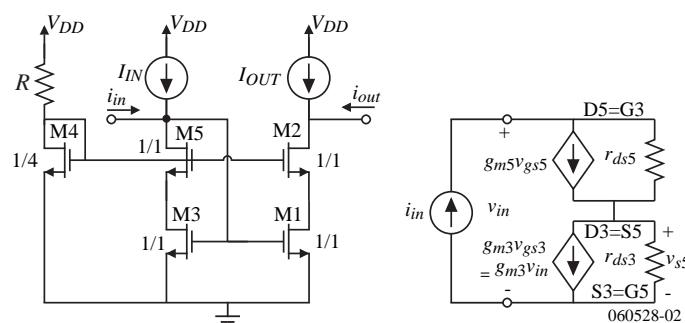
Fig. 300-7

Will deal with later in low voltage op amps.

- Minimum output voltage is $V_{MIN(out)} = V_{ON}$
- Output resistance is $R_{out} = \frac{1}{\lambda I_D}$
- Input resistance is $R_{in} \approx \frac{1}{g_m}$
- Current gain accuracy is poor because $v_{DS1} \neq v_{DS2}$

IMPROVED CURRENT MIRRORS

Large Output Swing Cascode Current Mirror



- $R_{out} \approx g_m 2 r_{ds2} r_{ds1}$
- $R_{in} = ?$ $v_{in} = r_{ds5}(i_{in} - g_{m5}v_{gs5}) + v_{s5} = r_{ds5}(i_{in} + g_{m5}v_{s5}) + v_{s5} = r_{ds5}i_{in} + (1 + g_{m5}r_{ds5})v_{s5}$
But, $v_{s5} = r_{ds3}(i_{in} - g_{m3}v_{in})$
 $\therefore v_{in} = r_{ds5}i_{in} + (1 + g_{m5}r_{ds5})r_{ds3}i_{in} - g_{m3}r_{ds3}(1 + g_{m5}r_{ds5})v_{in}$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{ds5} + r_{ds3} + r_{ds3}g_{m5}r_{ds5}}{g_{m3}r_{ds3}(1 + g_{m5}r_{ds5})} \approx \frac{1}{g_{m3}}$$

- $V_{MIN(out)} = 2V_{ON}$
- $V_{MIN(in)} = V_T + V_{ON}$
- Current gain is excellent because $v_{DS1} = v_{DS3}$.

Self-Biased Cascode Current Mirror

- $R_{in} = ?$

$$v_{in} = i_{in}R + r_{ds3}(i_{in} - g_{m3}v_{gs3}) + r_{ds1}(i_{in} - g_{m1}v_{gs1})$$

But,

$$v_{gs1} = v_{in} - i_{in}R$$

and

$$\begin{aligned} v_{gs3} &= v_{in} - r_{ds1}(i_{in} - g_{m1}v_{gs1}) \quad \text{Self-biased, cascode current mirror} \\ &= v_{in} - r_{ds1}i_{in} + g_{m1}r_{ds1}(v_{in} - i_{in}R) \end{aligned}$$

$$\therefore v_{in} = i_{in}R + r_{ds3}i_{in} - g_{m3}r_{ds3}[v_{in} - r_{ds1}i_{in} + g_{m1}r_{ds1}(v_{in} - i_{in}R)] + r_{ds1}[i_{in} - g_{m1}(v_{in} + i_{in}R)]$$

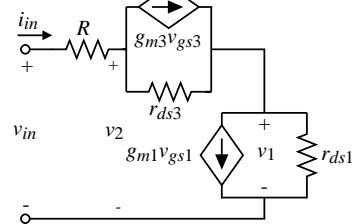
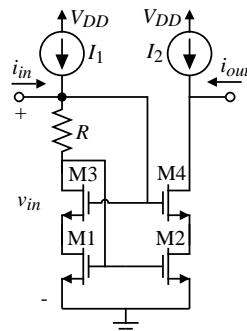
$$v_{in}[1 + g_{m3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3} + g_{m1}r_{ds1}]$$

$$= i_{in}[R + r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1} + g_{m1}r_{ds1}g_{m3}r_{ds3}R]$$

$$R_{in} = \frac{R + r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1} + g_{m1}r_{ds1}g_{m3}r_{ds3}R}{1 + g_{m3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3} + g_{m1}r_{ds1}} \approx \frac{1}{g_{m1}} + R$$

- $R_{out} \approx g_{m4}r_{ds4}r_{ds2}$

- $V_{MIN}(\text{in}) = V_T + 2V_{ON}$
- $V_{MIN}(\text{out}) = 2V_{ON}$
- Current gain matching is excellent



Small-signal model to calculate R_{in} .
Fig. 310-03

MOS Regulated Cascode Current Mirror

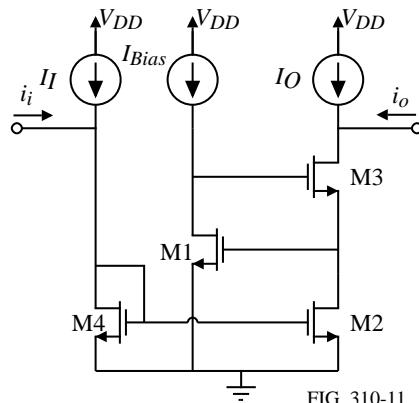


FIG. 310-11

- $R_{out} \approx g_m^2 r_{ds3}$
- $R_{in} \approx \frac{1}{g_{m4}}$
- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$ (Can be reduced to $2V_{ON}$)
- $V_{MIN}(\text{in}) = V_T + V_{ON}$ (Can be reduced to V_{ON})
- Current gain matching - good as long as $v_{DS4} = v_{DS2}$

Summary of MOS Current Mirrors

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	r_{ds}	$\frac{1}{g_m}$	V_{ON}	$V_T + V_{ON}$
Wide Output Swing Cascode	Excellent	$g_m r_{ds}^2$	$\frac{1}{g_m}$	$2V_{ON}$	$V_T + V_{ON}$
Self-biased Cascode	Excellent	$g_m r_{ds}^2$	$R + \frac{1}{g_m}$	$2V_{ON}$	$V_T + 2V_{ON}$
Regulated Cascode	Good-Excellent	$g_m^2 r_{ds}^3$	$\frac{1}{g_m}$	$V_T + 2V_{ON}$ (Can be $2V_{ON}$)	$V_T + V_{ON}$ (Can be $\approx V_{ON}$)

VOLTAGE REFERENCES WITH POWER SUPPLY INDEPENDENCE

Power Supply Independence

How do you characterize power supply independence?

Use the concept of:

$$S_{V_{DD}}^{V_{REF}} = \frac{\partial V_{REF}/V_{REF}}{\partial V_{DD}/V_{DD}} = \frac{V_{DD}}{V_{REF}} \left(\frac{\partial V_{REF}}{\partial V_{DD}} \right)$$

Application of sensitivity to determining power supply dependence:

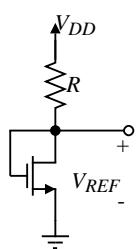
$$\frac{\partial V_{REF}}{V_{REF}} = \left(S_{V_{DD}}^{V_{REF}} \right) \frac{\partial V_{DD}}{V_{DD}}$$

Thus, the fractional change in the reference voltage is equal to the sensitivity times the fractional change in the power supply voltage.

For example, if the sensitivity is 1, then a 10% change in V_{DD} will cause a 10% change in V_{REF} .

Ideally, we want $S_{V_{DD}}^{V_{REF}}$ to be zero for power supply independence.

MOSFET-Resistance Voltage References



$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD}-V_{REF})}{\beta R}}$$

or

$$V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD}-V_T)}{\beta R} + \frac{1}{(\beta R)^2}}$$

$$S_{V_{DD}}^{V_{REF}} = \left(\frac{1}{\sqrt{1+2\beta(V_{DD}-V_T)R}} \right) \left(\frac{V_{DD}}{V_{REF}} \right)$$

Assume that $V_{DD}=5V$, $W/L=100$ and $R=100k\Omega$,

$$\text{Thus, } V_{REF} \approx 0.7875V \text{ and } S_{V_{DD}}^{V_{REF}} = 0.0653$$

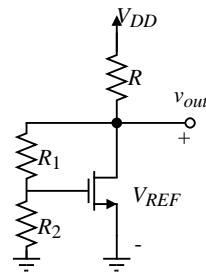
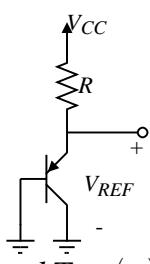


Fig. 370-03

This circuit allows V_{REF} to be larger. If the current in R_1 (and R_2) is small compared to the current flowing through the transistor, then

$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_2} \right) V_{GS}$$

Bipolar-Resistance Voltage References



$$V_{REF} = V_{EB} = \frac{kT}{q} \ln \left(\frac{I}{I_s} \right)$$

$$\text{and } I = \frac{V_{CC} - V_{EB}}{R} \approx \frac{V_{CC}}{R}$$

$$\text{give } V_{REF} \approx \frac{kT}{q} \ln \left(\frac{V_{CC}}{RI_s} \right)$$

$$S_{V_{CC}}^{V_{REF}} = \frac{1}{\ln[V_{CC}/(RI_s)]} = \frac{1}{\ln(I/I_s)}$$

If $V_{CC} = 5V$, $R = 4.3k\Omega$ and $I_s = 1fA$, then $V_{REF} = 0.719V$.

$$\text{Also, } S_{V_{CC}}^{V_{REF}} = 0.0362$$

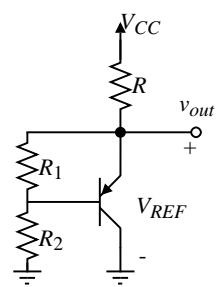


Fig. 370-04

If the current in R_1 (and R_2) is small compared to the current flowing through the transistor, then

$$V_{REF} \approx \left(\frac{R_1 + R_2}{R_1} \right) V_{EB}$$

Can use diodes in place of the BJTs.

CURRENT REFERENCES WITH POWER SUPPLY INDEPENDENCE

Power Supply Independence

Again, we want

$$S_{V_{DD}} = \frac{\partial I_{REF}/I_{REF}}{\partial V_{DD}/V_{DD}} = \frac{V_{DD}}{I_{REF}} \left(\frac{\partial I_{REF}}{\partial V_{DD}} \right)$$

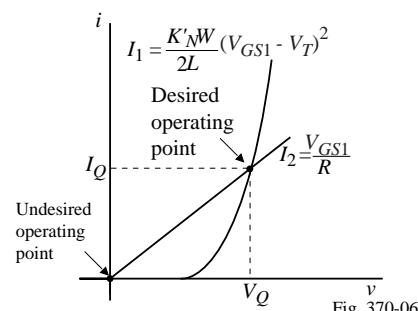
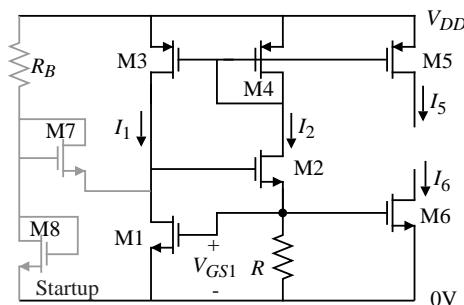
to approach zero.

Therefore, as $S_{V_{DD}}$ approaches zero, the change in I_{REF} as a function of a change in V_{DL} approaches zero.

Gate-Source Referenced Current Reference

The circuit below uses both positive and negative feedback to accomplish a current reference that is reasonably independent of power supply.

Circuit:



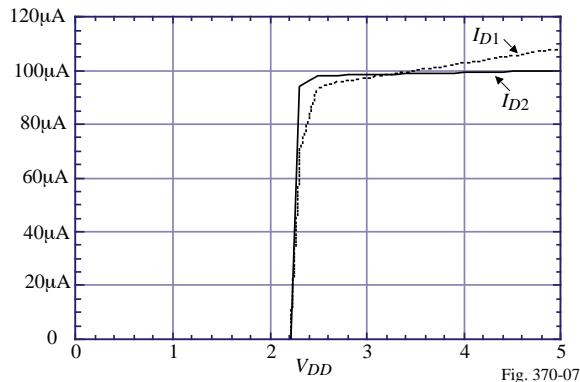
Principle:

If $M3 = M4$, then $I_1 \approx I_2$. However, the M1-R loop gives $V_{GS1} = V_{T1} + \sqrt{\frac{2I_1}{K_N'(W_1/L_1)}}$

Solving these two equations gives $I_2 = \frac{V_{GS1}}{R} = \frac{V_{T1}}{R} + \left(\frac{1}{R}\right) \sqrt{\frac{2I_1}{K_N'(W_1/L_1)}}$

The output current, $I_{out} = I_1 = I_2$ can be solved as $I_{out} = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R} \sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{(\beta_1 R)^2}}$

Simulation Results for the Gate-Source Referenced Current Reference



Simple, Bootstrap Current Reference

```
VDD 1 0 DC 5.0
VSS 9 0 DC 0.0
M1 5 7 9 9 N W=20U L=1U
M2 3 5 7 9 N W=20U L=1U
M3 5 3 1 1 P W=25U L=1U
M4 3 3 1 1 P W=25U L=1U
M5 9 3 1 1 P W=25U L=1U
R 7 9 10KIOHM
M8 6 6 9 9 N W=1U L=1U
M7 6 6 5 9 N W=20U L=1U
```

```
RB 1 6 100KIOHM
.OP
.DC VDD 0 5 0.1
.MODEL N NMOS VTO=0.7 KP=110U
GAMMA=0.4 +PHI=0.7 LAMBDA=0.04
.MODEL P PMOS VTO=-0.7 KP=50U
GAMMA=0.57 PHI=0.8 LAMBDA=0.05
.PRINT DC ID(M1) ID(M2) ID(M5)
.PROBE
.END
```

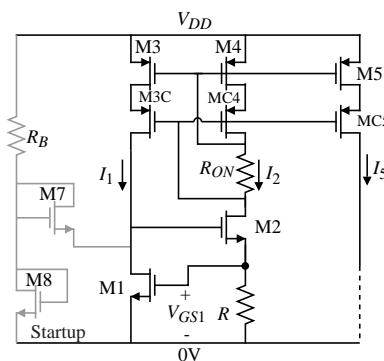
The current ID_2 appears to be okay, why is ID_1 increasing?

Apparently, the channel modulation on the current mirror M3-M4 is large.

At $V_{DD} = 5V$, $V_{SD3} = 2.83V$ and $V_{SD4} = 1.09V$ which gives $ID_3 = 1.067ID_4 \approx 107\mu A$

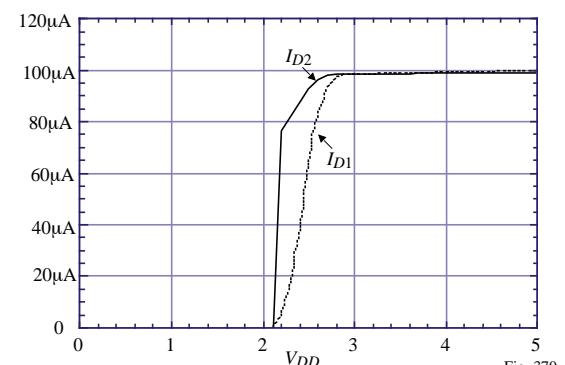
Need to cascode the upper current mirror.
SPICE Input File:

Cascoded Gate-Source Referenced Current Reference



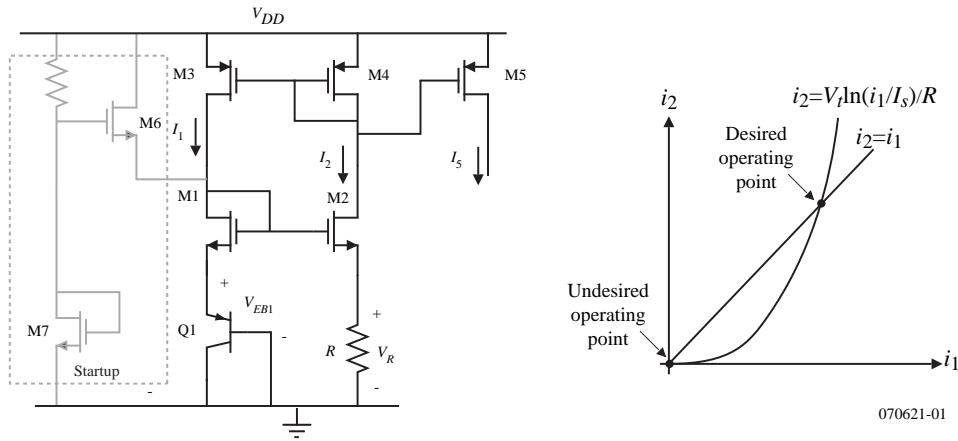
SPICE Input File:

```
Cascade, Bootstrap Current Reference
VDD 1 0 DC 5.0
VSS 9 0 DC 0.0
M1 5 7 9 9 N W=20U L=1U
M2 4 5 7 9 N W=20U L=1U
M3 2 3 1 1 P W=25U L=1U
M4 8 3 1 1 P W=25U L=1U
M3C 5 4 2 1 P W=25U L=1U
MC4 3 4 8 1 P W=25U L=1U
RON 3 4 4KIOHM
M5 9 3 1 1 P W=25U L=1U
R 7 9 10KIOHM
M8 6 6 9 9 N W=1U L=1U
```



```
M7 6 6 5 9 N W=20U L=1U
RB 1 6 100KIOHM
.OP
.DC VDD 0 5 0.1
.MODEL N NMOS VTO=0.7 KP=110U
GAMMA=0.4 PHI=0.7 LAMBDA=0.04
.MODEL P PMOS VTO=-0.7 KP=50U
GAMMA=0.57 PHI=0.8 LAMBDA=0.05
.PRINT DC ID(M1) ID(M2) ID(M5)
.PROBE
.END
```

Base-Emitter Referenced Circuit



070621-01

$$I_{out} = I_2 = \frac{V_{EB1}}{R}$$

BJT can be a MOSFET in weak inversion.

Low Voltage Gate-Source Referenced MOS Current Reference

The previous gate-source referenced circuits required at least 2 volts across the power supply before operating.

A low-voltage gate-source referenced circuit:

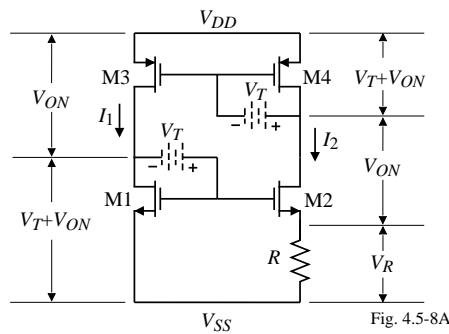


Fig. 4.5-8A

Without the batteries, V_T , the minimum power supply is $V_T + 2V_{ON} + V_R$.

With the batteries, V_T , the minimum power supply is $2V_{ON} + V_R \approx 0.5V$

Summary of Power-Supply Independent References

- Reasonably good, simple voltage and current references are possible
- Best power supply sensitivity is approximately 0.01
(10% change in power supply causes a 0.1% change in reference)

Type of Reference	$\frac{V_{REF}}{S V_{PP}}$ or $\frac{I_{REF}}{S V_{PP}}$
Voltage division	1
Simple Current Reference	1
MOSFET-R	<1
BJT-R	<<1
Gate-source Referenced	<<1
Base-emitter Referenced	<<1

TEMPERATURE BEHAVIOR OF VOLTAGE AND CURRENT REFERENCES

Characterization of Temperature Dependence

The objective is to minimize the fractional temperature coefficient defined as,

$$TC_F = \frac{1}{V_{REF}} \left(\frac{\partial V_{REF}}{\partial T} \right) = \frac{1}{T} S \frac{V_{REF}}{T} \text{ parts per million per } ^\circ\text{C or ppm/}^\circ\text{C}$$

Temperature dependence of PN junctions:

$$\left. \begin{aligned} i &\approx I_s \exp\left(\frac{v}{V_t}\right) \\ I_s &= KT^3 \exp\left(\frac{-V_{GO}}{V_t}\right) \end{aligned} \right\} \quad \frac{1}{I_s} \left(\frac{\partial I_s}{\partial T} \right) = \frac{\partial (\ln I_s)}{\partial T} = \frac{3}{T} + \frac{V_{GO}}{TV_t} \approx \frac{V_{GO}}{TV_t}$$

$$\frac{dv_{BE}}{dT} \approx \frac{V_{BE} - V_{GO}}{T} = -2 \text{ mV/}^\circ\text{C at room temperature}$$

($V_{GO} = 1.205$ V at room temperature and is called the bandgap voltage)

Temperature dependence of MOSFET in strong inversion:

$$\left. \begin{aligned} \frac{dv_{GS}}{dT} &= \frac{dV_T}{dT} + \sqrt{\frac{2L}{WC_{ox}}} \frac{d}{dT} \left(\sqrt{\frac{i_D}{\mu_o}} \right) \\ \mu_o &= KT^{-1.5} \\ V_T(T) &= V_T(T_0) - \alpha(T-T_0) \end{aligned} \right\} \quad \frac{dv_{GS}}{dT} \approx -\alpha \approx -2.3 \frac{\text{mV}}{^\circ\text{C}}$$

Resistors: $(1/R)(dR/dT)$ ppm/°C

Bipolar-Resistance Voltage References

From previous work we know that,

$$V_{REF} = \frac{kT}{q} \ln \left(\frac{V_{DD} - V_{REF}}{RI_s} \right)$$

However, not only is V_{REF} a function of T , but R and I_s are also functions of T .

$$\therefore \frac{dV_{REF}}{dT} = \frac{k}{q} \ln \left(\frac{V_{DD} - V_{REF}}{RI_s} \right) + \frac{kT}{q} \left(\frac{RI_s}{V_{DD} - V_{REF}} \right) \left[-\frac{1}{RI_s} \frac{dV_{REF}}{dT} - \left(\frac{V_{DD} - V_{REF}}{RI_s} \right) \left(\frac{dR}{RdT} + \frac{dI_s}{I_s dT} \right) \right]$$

$$\begin{aligned} &= \frac{V_{REF}}{T} - \frac{V_t}{V_{DD} - V_{REF}} \frac{dV_{REF}}{dT} - V_t \left(\frac{dR}{RdT} + \frac{dI_s}{I_s dT} \right) = \frac{V_{REF} - V_{GO}}{T} - \frac{V_t}{V_{DD} - V_{REF}} \frac{dV_{REF}}{dT} - \frac{3V_t}{T} - \frac{V_t}{R} \frac{dR}{dT} \\ \therefore \frac{dV_{REF}}{dT} &= \frac{\frac{V_{REF} - V_{GO}}{T} - V_t \frac{dR}{RdT} - \frac{3V_t}{T}}{1 + \frac{V_t}{V_{DD} - V_{REF}}} \approx \frac{V_{REF} - V_{GO}}{T} - V_t \frac{dR}{RdT} - \frac{3V_t}{T} \\ TC_F &= \frac{1}{V_{REF}} \frac{dV_{REF}}{dT} = \frac{V_{REF} - V_{GO}}{V_{REF} \cdot T} - \frac{V_t}{V_{REF}} \frac{dR}{RdT} - \frac{3V_t}{V_{REF} \cdot T} \end{aligned}$$

If $V_{REF} = 0.6V$, $V_t = 0.026V$, and the R is polysilicon, then at $27^\circ K$ the TC_F is

$$TC_F = \frac{0.6 - 1.205}{0.6 \cdot 300} - \frac{0.026 \cdot 0.0015}{0.6} - \frac{3 \cdot 0.026}{0.6 \cdot 300} = 33110^{-6} - 65 \times 10^{-6} - 433 \times 10^{-6} = -3859 \text{ ppm}/^\circ C$$

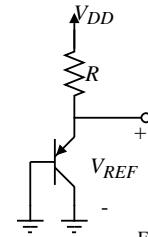


Fig. 380-1

MOSFET Resistor Voltage Reference

From previous results we know that

$$V_{REF} = V_{GS} = V_T + \sqrt{\frac{2(V_{DD} - V_{REF})}{\beta R}}$$

$$\text{or } V_{REF} = V_T - \frac{1}{\beta R} + \sqrt{\frac{2(V_{DD} - V_T)}{\beta R} + \frac{1}{(\beta R)^2}}$$

Note that V_{REF} , V_T , β , and R are all functions of temperature.

It can be shown that the TC_F of this reference is

$$\begin{aligned} \frac{dV_{REF}}{dT} &= \frac{-\alpha + \sqrt{\frac{V_{DD} - V_{REF}}{2\beta R} \left(\frac{1.5}{T} - \frac{1}{R} \frac{dR}{dT} \right)}}{1 + \sqrt{2\beta R (V_{DD} - V_{REF})}} \\ \therefore TC_F &= \frac{-\alpha + \sqrt{\frac{V_{DD} - V_{REF}}{2\beta R} \left(\frac{1.5}{T} - \frac{1}{R} \frac{dR}{dT} \right)}}{V_{REF} \left(1 + \sqrt{2\beta R (V_{DD} - V_{REF})} \right)} \end{aligned}$$

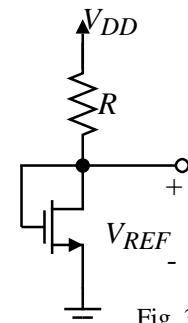


Fig. 380-02

Example 160-3 - Calculation of MOSFET-Resistor Voltage Reference TC_F

Calculate the temperature coefficient of the MOSFET-Resistor voltage reference where $W/L=2$, $V_{DD}=5V$, $R=100k\Omega$ using the parameters of Table 3.1-2. The resistor, R, is polysilicon and has a temperature coefficient of 1500 ppm/ $^{\circ}C$.

Solution

First, calculate V_{REF} . Note that $\beta R = 220 \times 10^{-6} \times 10^5 = 22$ and $\frac{dR}{RdT} = 1500 \text{ ppm}/^{\circ}C$

$$\therefore V_{REF} = 0.7 - \frac{1}{22} + \sqrt{\frac{2(5 - 0.7)}{22} + \left(\frac{1}{22}\right)^2} = 1.281V$$

$$\text{Now, } \frac{dV_{REF}}{dT} = \frac{-2.3 \times 10^{-3} + \sqrt{\frac{5 - 1.281}{2(22)} \left(\frac{1.5}{300} - 1500 \times 10^{-6}\right)}}{1 + \frac{1}{\sqrt{2(22)(5 - 1.281)}}} = -1.189 \times 10^{-3}V/^{\circ}C$$

The fractional temperature coefficient is given by

$$TC_F = -1.189 \times 10^{-3} \left(\frac{1}{1.281}\right) = -928 \text{ ppm}/^{\circ}C$$

Gate-Source and Base-Emitter Referenced Current Source/Sinks

Gate-source referenced source:

The output current was given as, $I_{out} = \frac{V_{T1}}{R} + \frac{1}{\beta_1 R^2} + \frac{1}{R} \sqrt{\frac{2V_{T1}}{\beta_1 R} + \frac{1}{(\beta_1 R)^2}}$

Although we could grind out the derivative of I_{out} with respect to T , the temperature performance of this circuit is not that good to spend the time to do so. Therefore, let us assume that $V_{GS1} \approx V_{T1}$ which gives

$$I_{out} \approx \frac{V_{T1}}{R} \Rightarrow \frac{dI_{out}}{dT} = \frac{1}{R} \frac{dV_{T1}}{dT} - \frac{1}{R^2} \frac{dR}{dT}$$

In the resistor is polysilicon, then

$$TC_F = \frac{1}{I_{out}} \frac{dI_{out}}{dT} = \frac{1}{V_{T1}} \frac{dV_{T1}}{dT} - \frac{1}{R} \frac{dR}{dT} = \frac{-2.3 \times 10^{-3}}{V_{T1}} - \frac{1}{R} \frac{dR}{dT} = \frac{-2.3 \times 10^{-3}}{0.7} - 1.5 \times 10^{-3} = -4786 \text{ ppm}/^{\circ}C$$

Base-emitter referenced source:

The output current was given as, $I_{out} = I_2 = \frac{V_{BE1}}{R}$

$$\text{The } TC_F = \frac{1}{V_{BE1}} \frac{dV_{BE1}}{dT} - \frac{1}{R} \frac{dR}{dT}$$

If $V_{BE1} = 0.6V$ and R is poly, then the $TC_F = \frac{1}{0.6} (-2 \times 10^{-3}) - 1.5 \times 10^{-3} = -4833 \text{ ppm}/^{\circ}C$.

Technique to Make g_m Dependent on a Resistor

Consider the following circuit with all transistors having a $W/L = 10$. This is a bootstrapped reference which creates a V_{bias} independent of V_{DD} . The two key equations are:

$$I_3 = I_4 \Rightarrow I_1 = I_2$$

and

$$V_{GS1} = V_{GS2} + I_2 R$$

Solving for I_2 gives:

$$I_2 = \frac{V_{GS1} - V_{GS2}}{R} = \frac{1}{R} \left(\sqrt{\frac{2I_1}{\beta_1}} - \sqrt{\frac{2I_2}{\beta_2}} \right) = \frac{\sqrt{2I_1}}{R\sqrt{\beta_1}} \left(1 - \frac{1}{2} \right)$$

$$\therefore \sqrt{I_2} = \frac{1}{R\sqrt{2\beta_1}} \Rightarrow I_2 = I_1 = \frac{1}{2\beta_1 R^2} = \frac{1}{2 \cdot 110 \times 10^{-6} \cdot 10 \cdot 25 \times 10^6} = 18.18 \mu A$$

Now, V_{bias} can be written as

$$V_{bias} = V_{GS1} = \sqrt{\frac{2I_2}{\beta_1}} + V_{TN} = \frac{1}{\beta_1 R} + V_{TN} = \frac{1}{110 \times 10^{-6} \cdot 10 \cdot 5 \times 10^3} + 0.7 = 0.1818 + 0.7 = 0.8818 V$$

Any transistor with $V_{GS} = V_{bias}$ will have a current flow that is given by $1/2\beta R^2$.

Therefore,
$$g_m = \sqrt{2I\beta} = \sqrt{\frac{2\beta}{2\beta R^2}} = \frac{1}{R} \Rightarrow g_m = \frac{1}{R}$$

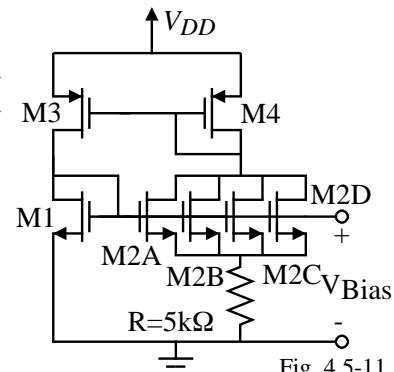


Fig. 4.5-11

Summary of Reference Performance

Type of Reference	$S_{V_{DD}}^{V_{REF}}$	TC_F	Comments
MOSFET-R	<1	>1000ppm/°C	
BJT-R	<<1	>1000ppm/°C	
Gate-Source Referenced	Good if currents are matched	>1000ppm/°C	Requires start-up circuit
Base-emitter Referenced	Good if currents are matched	>1000ppm/°C	Requires start-up circuit

- A MOSFET can have zero temperature dependence of i_D for a certain v_{GS}
- If one is careful, very good independence of power supply can be achieved
- None of the above references have really good temperature independence

Consider the following example:

A 10 bit ADC has a reference voltage of 1V. The LSB is approximately 0.001V. Therefore, the voltage reference must be stable to within 0.1%. If a 100°C change in temperature is experienced, then the TC_F must be 0.001%/C or multiplying by 10^4 requires a $TC_F = 10$ ppm/°C.

LECTURE 170 – TEMPERATURE STABLE REFERENCES

LECTURE ORGANIZATION

Outline

- Principles of temperature stable references
- Examples of temperature stable references
- Design of bias voltages for a chip
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 153-159

PRINCIPLES OF TEMPERATURE STABLE REFERENCES

Temperature Stable References

- The previous reference circuits failed to provide small values of temperature coefficient although sufficient power supply independence was achieved.
- This section introduces a temperature stable reference that cancels a positive temperature coefficient with a negative temperature coefficient. The technique is sometimes called the *bandgap reference* although it has nothing to do with the bandgap voltage.

Principle

$$V_{REF}(T) = V_{PTAT}(T) + K \cdot V_{CTAT}(T)$$

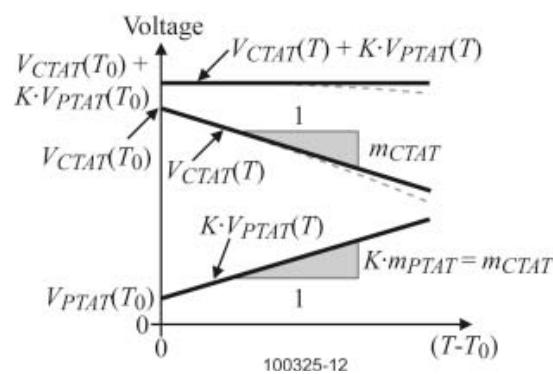
where

$V_{PTAT}(T)$ is a voltage that is *proportional to absolute temperature* (PTAT)

$V_{CTAT}(T)$ is a voltage that is *complementary to absolute temperature* (CTAT)

and

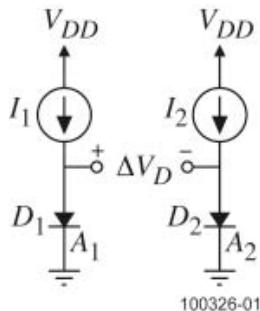
K is a temperature independent constant that makes $V_{REF}(T)$ independent of temperature



PTAT Voltage

The principle illustrated on the last slide requires perfectly linear positive and negative temperature coefficients to work properly. We will now show a technique of generating PTAT voltages that are linear with respect to temperature.

Implementation of a PTAT voltage:



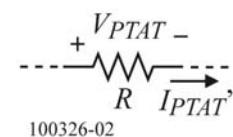
$$\begin{aligned}
 V_{PTAT} &= \Delta V_D = V_{D1} - V_{D2} = V_t \ln\left(\frac{I_1}{I_{s1}}\right) - V_t \ln\left(\frac{I_2}{I_{s2}}\right) \\
 &= V_t \ln\left(\frac{I_1}{I_2} \frac{I_{s2}}{I_{s1}}\right) = V_t \ln\left(\frac{I_{s2}}{I_{s1}}\right) = V_t \ln\left(\frac{A_2}{A_1}\right) = \frac{kT}{q} \ln\left(\frac{A_2}{A_1}\right) \\
 &\text{if } I_1 = I_2.
 \end{aligned}$$

Therefore, if $A_2 = 10A_1$, ΔV_D at room temperature becomes,

$$\begin{aligned}
 \Delta V_D &= \left[\frac{k}{q} \ln\left(\frac{A_2}{A_1}\right) \right] T = \left[\frac{1.381 \times 10^{-23} \text{ J/K}}{1.6 \times 10^{-19} \text{ Coul}} \ln(10) \right] T = (+0.086 \text{ mV/C})T \\
 \therefore V_{PTAT} &= V_t \ln\left(\frac{A_2}{A_1}\right)
 \end{aligned}$$

Pseudo-PTAT Currents

In developing temperature independent voltages, it is useful to show how to generate PTAT currents. A straight-forward method is to superimpose V_{PTAT} across a resistor as shown:



Because R is always dependent on temperature, this current is called a *pseudo-PTAT current* and is designated by I_{PTAT} .

When a pseudo-PTAT current flows through a second resistor with the same temperature characteristics as the first, it creates a new V_{PTAT} voltage.

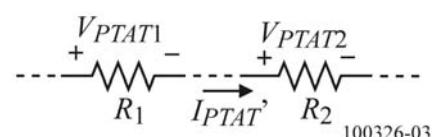
The new V_{PTAT} voltage, V_{PTAT2} is equal to,

$$V_{PTAT2} = \frac{R_2}{R_1} V_{PTAT1}$$

Differentiating with respect to temperature gives

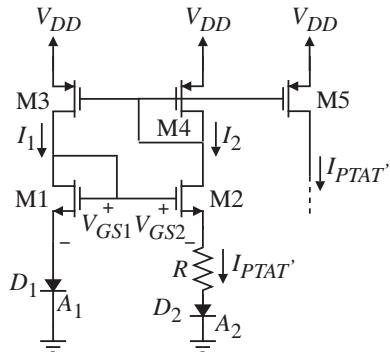
$$\frac{dV_{PTAT2}}{dT} = \frac{R_2}{R_1} \left(\frac{dR_2}{R_2 dT} - \frac{dR_1}{R_1 dT} \right) + \frac{dV_{PTAT1}}{dT}$$

Therefore, if the temperature coefficient of R_1 and R_2 are equal, then the temperature dependence of V_{PTAT2} is the same as V_{PTAT1} .

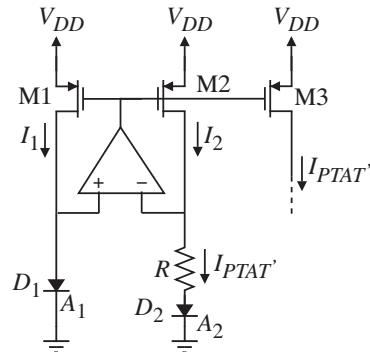


Pseudo-PTAT Currents - Continued

This can be done through the circuits below which use only MOSFETs and *pn* junctions or MOSFETs, an op amp and *pn* junctions.



Pseudo-PTAT current generator using only MOSFETs and pn junctions.



Pseudo-PTAT current generator using MOSFETs, an op amp and pn junctions.

100326-04

In these circuits, $I_1 = I_2$ and the voltage across D_1 is made equal to the voltage across the series combination of R and D_2 to create the pseudo-PTAT current,

$$I_{PTAT'} = \frac{V_{D1} - V_{D2}}{R} = \frac{kT}{Rq} \ln\left(\frac{A_2}{A_1}\right)$$

where $V_{GS1} = V_{GS2}$ for the MOSFET only version.

CTAT Voltage

This becomes more challenging because a true CTAT voltage does not exist. The best approach is to examine the *pn* junction (can be a diode or BJT).

The current through a *pn* junction shown can be written as,

$$J_D = \left[\frac{qD_n n_i^2}{L_n N_A} + \frac{qD_p p_{no}}{L_p} \right] \left(\frac{(v_D - V_{G0})}{V_t} \right) = AT^\gamma \exp\left(\frac{v_D - V_{G0}}{V_t}\right)$$

Consider the circuit shown. It can be shown, that $v_D(T)$ can be given as,

$$v_D(T) = V_{GO} \left(1 - \frac{T}{T_0} \right) + v_{D0} \left(\frac{T}{T_0} \right) + \frac{\gamma kT}{q} \ln\left(\frac{T_0}{T}\right) + \frac{kT}{q} \ln\left(\frac{J_D}{J_{D0}}\right)$$

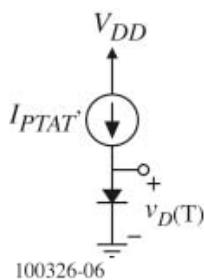
where,

V_{GO} = bandgap voltage of silicon (1.205V)

T_0 = a reference temperature about which T varies

γ = a temperature coefficient for the *pn* junction saturation current ($\gamma \approx 3$)

J_D = *pn* junction current density



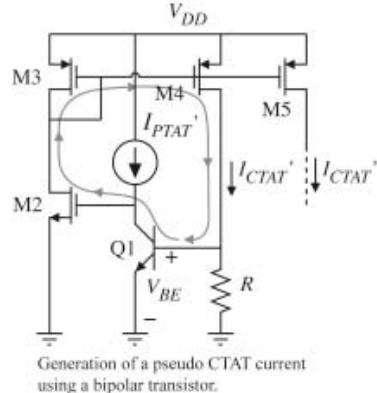
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In the above expression for $v_D(T)$ the term $\frac{\gamma kT}{q} \ln\left(\frac{T_0}{T}\right)$ is not linear with T !!

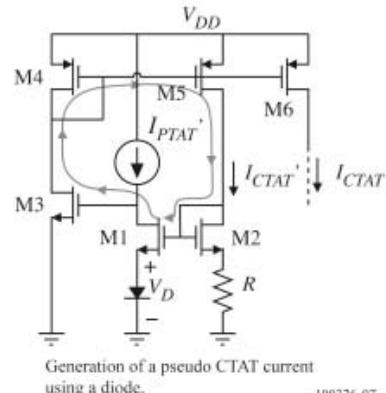
This term will create a problem called “bandgap curvature problem” because a perfectly linear PTAT function cannot be cancelled by a term that is not truly CTAT.

Pseudo CTAT Currents

The circuits below show two ways of creating a pseudo CTAT current using negative feedback:[†]



Generation of a pseudo CTAT current using a bipolar transistor.



Generation of a pseudo CTAT current using a diode.

100326-07

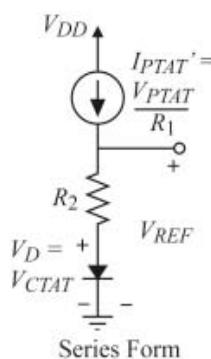
The negative feedback loop shown causes the current designated as I_{CTAT}' to be,

$$I_{CTAT}' = \frac{V_{BE}}{R} = \frac{V_D}{R}$$

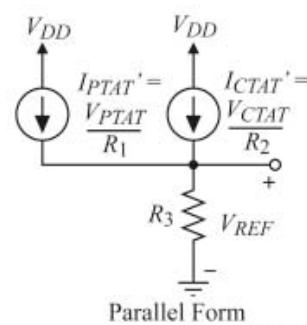
[†] I.M. Gunawan, G.C.M. Jeijer, J. Fonderie, and J.H. Huijsing, "A Curvature-Corrected Low-Voltage Bandgap Reference, *IEEE J. Solid-state Circuits*, vol. SC-28, No. 6, June 1993, pp. 677-670.

Temperature Independent Voltage References

Basic structures:



Series Form



Parallel Form

100326-08

Series form:

$$V_{REF} = I_{PTAT}' R_2 + V_D = \left(\frac{R_2}{R_1} \right) V_{PTAT} + V_{CTAT}$$

Parallel form:

$$V_{REF} = (I_{PTAT}' + I_{CTAT}') R_3 + V_D = \left(\frac{R_3}{R_1} \right) V_{PTAT} + \left(\frac{R_3}{R_2} \right) V_{CTAT} = \left(\frac{R_3}{R_2} \right) \left[\left(\frac{R_2}{R_1} \right) V_{PTAT} + V_{CTAT} \right]$$

To achieve temperature independence, V_{REF} must be differentiated with respect to temperature and set equal to zero. The resistor ratios and other parameters can be used to achieve temperature independence.

Conditions for Temperature Independence

Differentiating either the series or parallel form with respect to temperature and equating to zero gives,

$$K = \frac{R_2}{R_1} = -\frac{dV_{CTAT}/dT}{dV_{PTAT}/dT}$$

The slopes of V_{CTAT} and V_{PTAT} at a given temperature, T_0 , are:

$$m_{CTAT} = \left. \frac{dV_{CTAT}}{dT} \right|_{T=T_0} = \frac{V_D - V_{GO}}{T_0} + (\alpha - \gamma) \left(\frac{k}{q} \right) = \frac{V_{CTAT} - V_{GO}}{T_0} + (\alpha - \gamma) \left(\frac{V_{t0}}{T_0} \right)$$

where α = temperature dependence of J_D [$J_D(T) \propto T^\alpha$, where $\alpha = 1$ for PTAT current flowing through the pn junction]

and

$$m_{PTAT} = \left. \frac{dV_{PTAT}}{dT} \right|_{T=T_0} = \frac{k}{q} \ln \left(\frac{J_{D2}}{J_{D1}} \right) = \frac{k}{q} \ln \left(\frac{A_2}{A_1} \right) = \frac{V_{t0}}{T_0} \ln \left(\frac{A_2}{A_1} \right) = \frac{V_{PTAT}}{T_0}$$

Therefore, the temperature independent constant multiplying V_{PTAT} is

$$\text{Temp. independent constant} = K = \frac{R_2}{R_1} = \frac{V_{GO} - V_{CTAT} + (\gamma - \alpha)V_{t0}}{V_{PTAT}}$$

Therefore,

$$V_{REF} = V_{GO} - V_{CTAT} + (\gamma - \alpha)V_{t0} + V_{CTAT} = V_{GO} + (\gamma - \alpha)V_{t0} \approx 1.205V + 0.057 = 1.262V$$

Example 170-1 – Temp. Independent Constant for Series and Parallel References

(a.) Design the ratio of R_2/R_1 for the series configuration if $V_{CTAT} = 0.6V$ and $A_2/A_1 = 10$ for room temperature ($V_t = 0.026V$). Assume $\gamma = 3.2$ and $\alpha = 1$. Find the value of V_{REF} .

$$\frac{R_2}{R_1} = \frac{V_{GO} - V_{CTAT} + (\gamma - \alpha)V_{t0}}{V_{PTAT}} = \frac{1.205 - 0.6 + 2.2(0.026)}{0.026(2.3026)} = 11.06$$

$$V_{REF} = 1.205 + 2.2(0.026) = 1.262V$$

(b.) For the parallel configuration find the values of R_2/R_1 and R_3/R_2 if $V_{REF} = 0.5V$.

From (a.) we know that $R_2/R_1 = 11.05$. We also know that,

$$\begin{aligned} V_{REF} &= \left(\frac{R_3}{R_1} \right) V_{PTAT} + \left(\frac{R_3}{R_2} \right) V_{CTAT} = \left(\frac{R_3}{R_2} \right) \left[\left(\frac{R_2}{R_1} \right) V_{PTAT} + V_{CTAT} \right] \\ &= (R_3/R_2)[11.05 \ln(10)(0.026) + 0.6] = (R_3/R_2)1.262 = 0.5 \end{aligned}$$

$$\therefore (R_3/R_2) = 0.3963$$

If $R_1 = 1k\Omega$, then $R_2 = 11.05k\Omega$ and $R_3 = 4.378k\Omega$

A Series Temperature Independent Voltage Reference

An early realization of the series form is shown below[†]:

Assuming $V_{OS} = 0$, then V_{R1} is

$$\begin{aligned} V_{R1} &= V_{EB2} - V_{EB1} = V_t \ln\left(\frac{J_2}{J_{s2}}\right) - V_t \ln\left(\frac{J_1}{J_{s1}}\right) \\ &= V_t \ln\left(\frac{I_2 A_{E1}}{I_1 A_{E2}}\right) = V_t \ln\left(\frac{R_2 A_{E1}}{R_1 A_{E2}}\right) \end{aligned}$$

The op amp forces the relationship $I_1 R_2 = I_2 R_3$

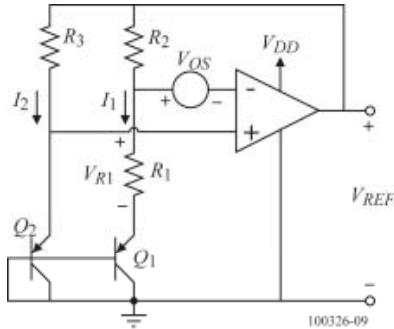
$$\therefore V_{REF} = V_{EB2} + I_2 R_3 = V_{EB2} + V_{R1} \frac{(R_2)}{(R_1)} = V_{EB2} + \left(\frac{R_2}{R_1}\right) V_t \ln\left(\frac{R_2 A_{E1}}{R_1 A_{E2}}\right) = V_{CTAT} + \left(\frac{R_2}{R_1}\right) \ln\left(\frac{R_2 A_{E1}}{R_1 A_{E2}}\right) V_t$$

Differentiating the above with respect to temperature and setting the result to zero, gives

$$\left(\frac{R_2}{R_1}\right) \ln\left(\frac{R_2 A_{E1}}{R_1 A_{E2}}\right) = \frac{V_{GO} - V_{CTAT} + (\gamma - \alpha) V_{t0}}{V_t}$$

If $V_{OS} \neq 0$, then V_{REF} becomes,

$$V_{REF} = V_{EB2} - \left(1 + \frac{R_2}{R_1}\right) V_{OS} + \frac{R_2}{R_1} V_t \ln\left[\frac{R_2 A_{E1}}{R_1 A_{E2}} \left(1 - \frac{V_{OS}}{I_1 R_2}\right)\right]$$



100326-09

[†] K.E. Kujik, "A Precision Reference Voltage Source," *IEEE Journal of Solid-State Circuits*, Vol. SC-8, No. 3 (June 1973) pp. 222-226.

Example 170-2 – Design of the Previous Temperature Independent Reference

Assume that $A_{E1} = 10 A_{E2}$, $V_{EB2} = 0.7$ V, $R_2 = R_3$, and $V_t = 0.026$ V at room temperature for temperature independent reference on the previous slide. Find R_2/R_1 to give a zero temperature coefficient at room temperature. If $V_{OS} = 10$ mV, find the change in V_{REF} . Note that $I_1 R_2 = V_{REF} - V_{EB2} - V_{OS}$.

Evaluating the temperature independent constant gives

$$\left(\frac{R_2}{R_1}\right) \ln\left(\frac{R_2 A_{E1}}{R_3 A_{E2}}\right) = \frac{V_{GO} - V_{CTAT} + (\gamma - \alpha) V_{t0}}{V_{PTAT}} = \frac{1.205 - 0.7 + (2.2)(0.026)}{0.026} = 21.62$$

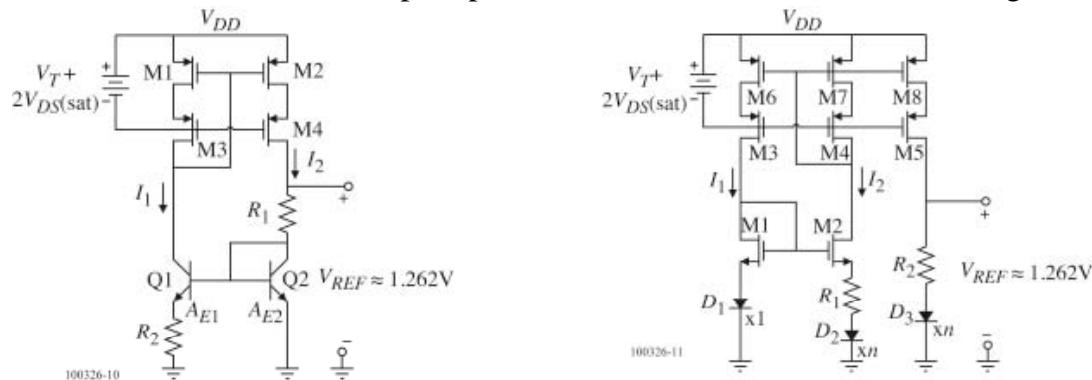
Therefore, $R_2/R_1 = 9.39$. In order to use the equation for V_{REF} with $V_{OS} \neq 0$, we must know the approximate value of V_{REF} and iterate if necessary because I_1 is a function of V_{REF} . Assuming V_{REF} to be 1.262, we obtain from

$$V_{REF} = V_{EB2} - \left(1 + \frac{R_2}{R_1}\right) V_{OS} + \frac{R_2}{R_1} V_t \ln\left[\frac{R_2 A_{E1}}{R_1 A_{E2}} \left(1 - \frac{V_{OS}}{V_{REF} - V_{EB2} - V_{OS}}\right)\right]$$

a new value $V_{REF} = 1.153$ V. The second iteration makes little difference on the result because V_{REF} is in the argument of the logarithm

Series Temperature Independent Voltage References

The references shown do not use an op amp and avoid the issues with offset voltage and PSRR.



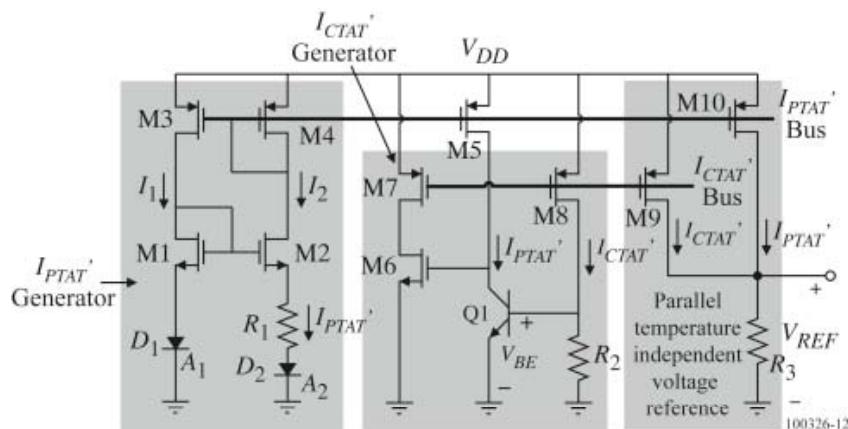
$$I_1 = I_{PTAT'} = \frac{V_{BE2} - V_{BE1}}{R_2} = \frac{V_t}{R_2} \left[\ln\left(\frac{I_2}{I_{s2}}\right) - \ln\left(\frac{I_1}{I_{s1}}\right) \right] \\ = \frac{V_t}{R_2} \ln\left(\frac{I_{s1}}{I_{s2}}\right) = \frac{V_t}{R_2} \ln\left(\frac{A_{E1}}{A_{E2}}\right)$$

$$\text{Since } I_1 = I_2, V_{REF} = V_{BE1} + I_1 R_1 = V_{BE1} + \left(\frac{R_1}{R_2} \ln\left(\frac{A_{E1}}{A_{E2}}\right) \right) V_t \\ = V_{CTAT} + \left(\frac{R_1}{R_2} \ln\left(\frac{A_{E1}}{A_{E2}}\right) \right) V_{PTAT}$$

$$V_{D1} = I_2 R_1 + V_{D2} \\ I_3 = I_2 = I_{PTAT'} = \frac{V_t}{R} \ln(n) \\ V_{REF} = V_{D3} + I_3(kR) = V_{D3} + kV_t \ln(n) \\ = V_{CTAT} + k \ln(n) V_{PTAT}$$

Parallel Temperature Independent Voltage Reference

A parallel form of the temperature independent voltage reference is shown below:



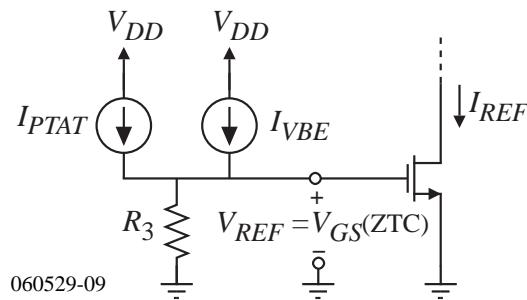
$$V_{REF} = \left(\frac{R_3}{R_1} \right) V_{PTAT} + \left(\frac{R_3}{R_2} \right) V_{CTAT}$$

Comments:

- The BJT of the I_{CTAT}' generator can be replaced with an MOSFET-diode equivalent
- Any value of V_{REF} can be achieved
- Part (b.) of Example 170-1 showed how to design the resistors of this implementation

How Can a Bandgap “Current” Reference be Obtained?

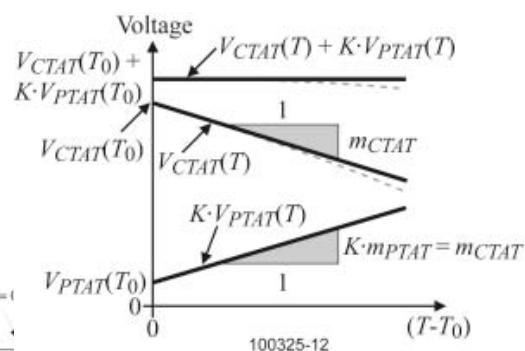
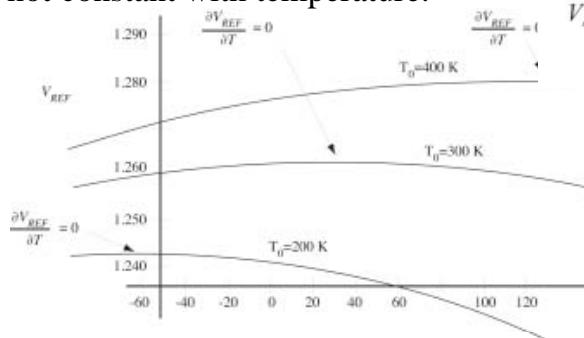
Use a MOSFET under ZTC operation and design the parallel form of the bandgap voltage reference to give a value of V_{ZTC} .



Bandgap Curvature Problem

Unfortunately, the $\frac{\gamma kT}{q} \ln\left(\frac{T_0}{T}\right)$ term of the pn junction contributed a nonlinearity to the CTAT realization. This is illustrated by the dashed lines in the plot shown.

The result is shown below where the reference voltage is not constant with temperature.



Comments:

- True temperature independence is only achieved over a small range of temperatures
- References that do not correct this problem have a temperature dependence of 10 ppm/ $^{\circ}$ C to 50 ppm/ $^{\circ}$ C over 0 $^{\circ}$ C to 70 $^{\circ}$ C.

Some Curvature Correction Techniques

- Squared PTAT Correction:
Temperature coefficient $\approx 1\text{-}20 \text{ ppm}/^\circ\text{C}$

- V_{BE} loop

M. Gunaway, et. al., "A Curvature-Corrected Low-Voltage Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 6, pp. 667-670, June 1993.

- β compensation

I. Lee et. al., "Exponential Curvature-Compensated BiCMOS Bandgap References," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 11, pp. 1396-1403, Nov. 1994.

- Nonlinear cancellation

G.M. Meijer et. al., "A New Curvature-Corrected Bandgap Reference," *IEEE Journal of Solid-State Circuits*, vol. 17, no. 6, pp. 1139-1143, December 1982.

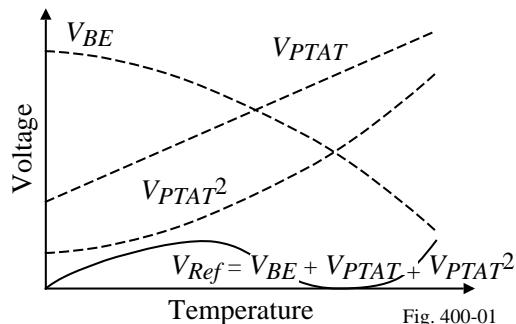
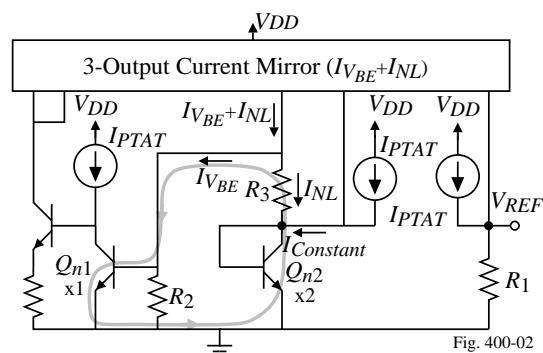


Fig. 400-01

V_{BE} Loop Curvature Correction Technique

Circuit:



Operation:

$$\begin{aligned} I_{NL} &= \frac{V_{BE1}-V_{BE2}}{R_3} = \frac{V_t}{R_3} \ln \left(\frac{I_{c1}A_2}{A_1I_{c2}} \right) \\ &= \frac{V_t}{R_3} \ln \left(\frac{2I_{PTAT}}{I_{NL}+I_{Constant}} \right) \end{aligned}$$

where

$$\begin{aligned} I_{constant} &= I_{NL} + I_{PTAT} + I_{VBE} \\ &\approx I_{NL} + \frac{V_t}{R_x} + \frac{V_{BE}}{R_2} \end{aligned}$$

(a quasi-temperature independent current subject to the TC_F of the resistors)
where

$$V_t = kT/q$$

I_{c1} and I_{c2} are the collector currents of Q_{n1} and Q_{n2} , respectively

R_x = a resistor used to define I_{PTAT}

$$\therefore V_{REF} = \left[\frac{V_{BE}}{R_2} + \frac{V_t}{R_3} \ln \left(\frac{2I_{PTAT}}{I_{NL}+I_{constant}} \right) + I_{PTAT} \right] R_1$$

Temperature coefficient $\approx 3 \text{ ppm}/^\circ\text{C}$ with a total quiescent current of $95\mu\text{A}$.

β Compensation Curvature Correction Technique

Circuit:

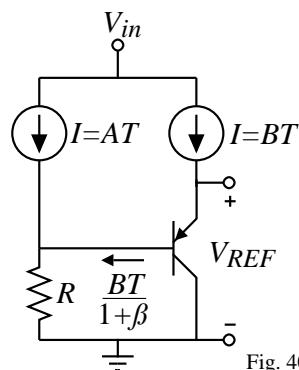


Fig. 400-0

Operation:

$$V_{REF} = V_{BE} + \left(AT + \frac{BT}{(1+\beta)} \right) R \approx V_{BE} + \left(AT + \frac{BT}{\beta} \right) R$$

where

 A and B are constant T = temperatureThe temperature dependence of β is

$$\beta(T) \propto e^{-1/T} \Rightarrow \beta(T) = C e^{-1/T}$$

Not good for small values of V_{in} .

$$V_{in} \geq V_{REF} + V_{sat.} = V_{GO} + V_{sat.} = 1.4V$$

Series Temperature Independent Voltage Reference with Curvature Correction

Objective: Eliminate nonlinear term from V_{CTAT} .Result: 0.5 ppm/ $^{\circ}\text{C}$ from -25°C to 85°C .

Operation:

$$V_{REF} = V_{PTAT} + 3V_{CTAT} - 2V_{Constant}$$

Note that, $I_{PTAT} \Rightarrow I_c \propto T^1 \Rightarrow \alpha = 1$ and $I_{Constant} \Rightarrow I_c \propto T^0 \Rightarrow \alpha = 0$,

Previously we found,

$$V_{CTAT}(T) \approx V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] - (\gamma - \alpha) V_t \ln\left(\frac{T}{T_0}\right)$$

so that

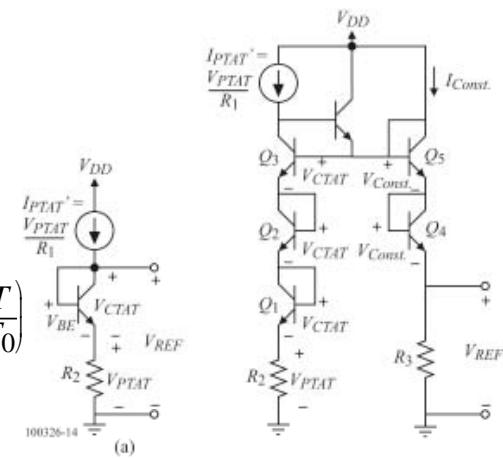
$$V_{CTAT}(I_{PTAT}) = V_{GO} - \frac{T}{T_0} [V_{GO} - V_{BE}(T_0)] - (\gamma - 1) V_t \ln\left(\frac{T}{T_0}\right)$$

and

$$V_{CTAT}(I_{Constant}) = V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] - \gamma V_t \ln\left(\frac{T}{T_0}\right)$$

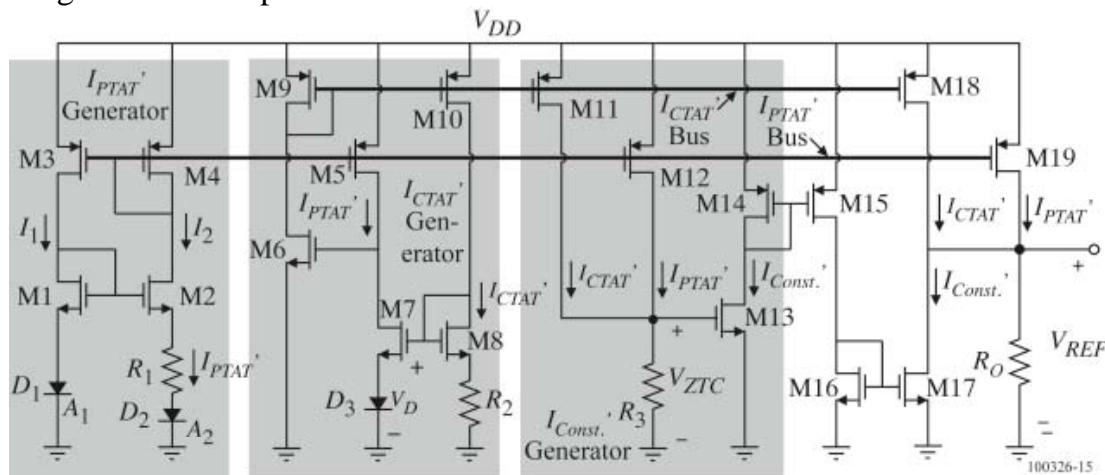
Combining the above relationships gives,

$$V_{REF}(T) = V_{PTAT} + V_{GO} - (T/T_0) [V_{GO} - V_{CTAT}(T_0)] - [\gamma - 3] V_t \ln(T/T_0)$$

If $\gamma \approx 3$, then $V_{REF}(T) \approx V_{PTAT} + V_{GO}(1 - (T/T_0)) + V_{CTAT}(T_0)(T/T_0)$ 

A Parallel Version of the Nonlinear Curvature Correction Technique

The last idea was good in concept but not appropriate for CMOS implementation. The following is a better implementation.



$$V_{REF} = R_0[I_{PTAT'} + I_{CTAT'} - I_{const.}] = \frac{R_0}{R_1} V_{PTAT} + \frac{R_0}{R_2} V_{CTAT} - \frac{R_0}{R_3} V_{const.}$$

Use the resistor ratios to eliminate the nonlinear term given γ and α .

Parallel Curvature Correction Reference - Continued

Substitute for V_{CTAT} and $V_{const.}$ in the expression for V_{REF} .

$$V_{REF} = \frac{R_0}{R_1} V_{PTAT} + \frac{R_0}{R_2} \left[V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] - (\gamma-1) V_t \ln\left(\frac{T}{T_0}\right) \right] - \frac{R_0}{R_3} \left[V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] - \gamma V_t \ln\left(\frac{T}{T_0}\right) \right]$$

To cancel the nonlinear CTAT term, we want the following relationship to hold:

$$\frac{R_0}{R_2} (\gamma-1) = \frac{R_0}{R_3} \gamma \Rightarrow \frac{R_2}{R_3} = \frac{(\gamma-1)}{\gamma} \quad (\text{Fortunately } \gamma \text{ is always greater than 1})$$

With these constraints, we find the voltage reference to be,

$$\begin{aligned} V_{REF} &= \frac{R_0}{R_1} V_{PTAT} + \left(\frac{R_0}{R_2} - \frac{R_0}{R_3} \right) \left[V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] \right] \\ &= \frac{R_0}{R_1} V_{PTAT} + \frac{1}{\gamma} \frac{R_0}{R_2} \left[V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] \right] \\ &= \frac{R_0}{\gamma R_2} \left\{ \frac{\gamma R_2}{R_1} V_{PTAT} + \left[V_{GO} - \frac{T}{T_0} [V_{GO} - V_{CTAT}(T_0)] \right] \right\} = \frac{R_0}{\gamma R_2} \left[\frac{\gamma R_2}{R_1} V_{PTAT} + V_{CTAT}(T_0) \right], \quad (T = T_0) \end{aligned}$$

Design $\gamma R_2 / R_1$ to achieve temperature independence and R_0 / R_2 to get V_{REF} .

Example 170-3 – Design of a Zero Temperature Coefficient Voltage Reference

Assume that $V_{CTAT} = 0.7$ V, $R_3 = 10k\Omega$, $\gamma = 3.2$, $A_2 = 10A_1$, and $V_t = 0.026$ V at room temperature for the parallel curvature correction circuit. Find R_2 and R_3 to give a zero temperature coefficient at room temperature and a reference voltage of 1.0V.

To eliminate the nonlinear CTAT term,

$$\frac{R_2}{R_3} = \frac{(\gamma-1)}{\gamma} = \frac{(2.2)}{3.2} = 0.6875 \quad \Rightarrow \quad R_2 = 6.88k\Omega$$

To cancel the temperature dependence,

$$\text{Temp. independent constant } K = \frac{\gamma R_2}{R_1} = \frac{V_{GO} - V_{CTAT} + (\gamma-\alpha)V_{t0}}{V_{PTAT}}$$

or

$$\frac{\gamma R_2}{R_1} = \frac{V_{GO} - V_{CTAT} + (\gamma-\alpha)V_{t0}}{V_{PTAT}} = \frac{(1.205 - 0.7 + (3.2-1)(0.026))}{(0.026)(2.3026)} = 9.3907 \Rightarrow R_1 = 2.34k\Omega$$

The reference voltage can be written as,

$$V_{REF} = \frac{R_0}{\gamma R_2} \left[\frac{\gamma R_2}{R_1} V_{PTAT} + V_{CTAT}(T_0) \right] = \frac{R_0}{\gamma R_2} [9.3907(0.026)(2.3026) + 0.7]$$

$$\frac{R_0}{R_2} = \frac{(3.2)}{1.262} = 2.535 \quad \Rightarrow \quad R_0 = 2.535R_2 = 17.44k\Omega$$

Other Characteristics of Bandgap Voltage References

Noise

Voltage references for high-resolution ADCs are particularly sensitive to noise.

Noise sources: Op amp, resistors, switches, etc.

PSRR

Maximize the PSRR of the op amp.

Offset Voltages

Becomes a problem when op amps are used.

$$V_{BE2} = V_{BE1} + V_{R1} + V_{OS}$$

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_{R1} + V_{OS} = V_t \ln \left(\frac{i_{C2} A_{E1}}{i_{C1} A_{E2}} \right)$$

$$\text{Since } i_{C2} R_3 = i_{C1} R_2 - V_{OS}$$

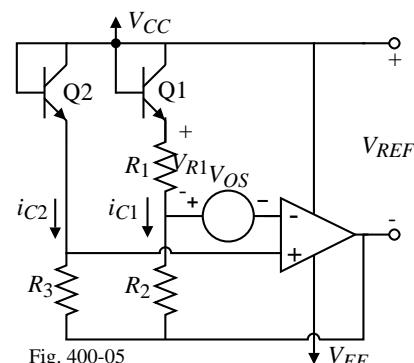
$$\text{then } \frac{i_{C2}}{i_{C1}} = \frac{R_2}{R_3} - \frac{V_{OS}}{i_{C1} R_3} = \frac{R_2}{R_3} \left(1 + \frac{V_{OS}}{i_{C1} R_2} \right)$$

Therefore,

$$V_{R1} = -V_{OS} + V_t \ln \left[\frac{R_2 A_{E1}}{R_3 A_{E2}} \left(1 + \frac{V_{OS}}{i_{C1} R_2} \right) \right]$$

$$V_{REF} = V_{BE2} - V_{OS} + i_{C1} R_2 = V_{BE2} - V_{OS} + \left(\frac{V_{R1}}{R_1} \right) R_2 = V_{BE2} - V_{OS} + \left(\frac{R_2}{R_1} \right)$$

$$\therefore V_{REF} = V_{BE2} - V_{OS} \left(1 + \frac{R_2}{R_1} \right) + \frac{R_2}{R_1} V_t \ln \left[\frac{R_2 A_{E1}}{R_3 A_{E2}} \left(1 - \frac{V_{OS}}{i_{C1} R_2} \right) \right]$$



Noise Analysis of a Bandgap Reference

Consider the simple classical BG reference shown ($R_2 = 10 R_1 = 10\text{k}\Omega$):

The open-circuit output noise voltage squared is found as,

$$\begin{aligned} e_{no}^2 &= [e_{n1}^2/R_1^2 + e_{n2}^2/R_1^2 + g_{m5}^2 e_{n3}^2 \\ &+ g_{m5}^2 e_{n4}^2 + g_{m5}^2 e_{n5}^2 + i_{nd1}^2/(g_{m1}^2 R_1^2) \\ &+ i_{nd2}^2 + i_{nd3}^2 + i_{nr1}^2 + i_{nr2}^2] R_2^2 \end{aligned}$$

Assuming the MOSFETs are matched and the dc currents in D_1 , D_2 , and D_3 are equal gives,

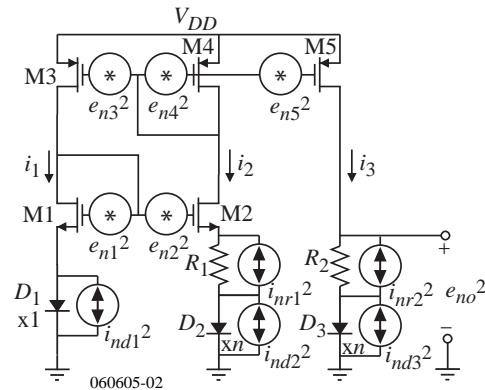
$$e_{no}^2 \approx [g_{m5}^2(e_{n3}^2 + e_{n4}^2 + e_{n5}^2) + i_{nd2}^2 + i_{nd3}^2 + i_{nr1}^2 + i_{nr2}^2] R_2^2$$

Thermal noise gives ($g_{m5} = 400\mu\text{S}$),

$$e_{no}^2 = 8kT g_{m5}^2 R_2^2 + 4qI_1 \left(\frac{4kT}{R_1} + \frac{4kT}{R_2} \right) R_2^2 \approx 5.3 \times 10^{-19} + 6.4 \times 10^{-23} + 1.7 \times 10^{-15} (\text{V}^2/\text{Hz})$$

$1/f$ noise gives,

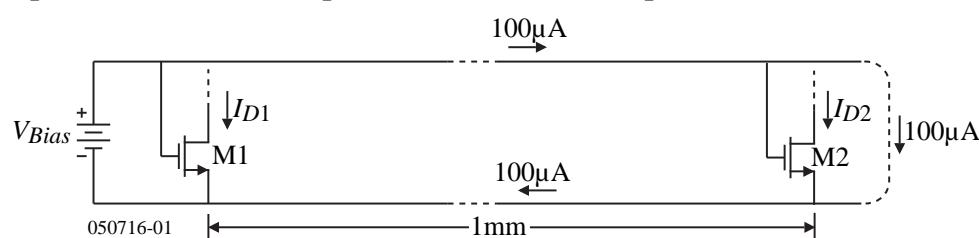
$$e_{no}^2 = 3g_{m5}^2 \frac{KF}{2fC_{ox}WLK},$$



DESIGN OF BIAS VOLTAGES FOR A CHIP

Distributing Bias Voltages over a Distance

The major problem is the IR drops in busses. For example,



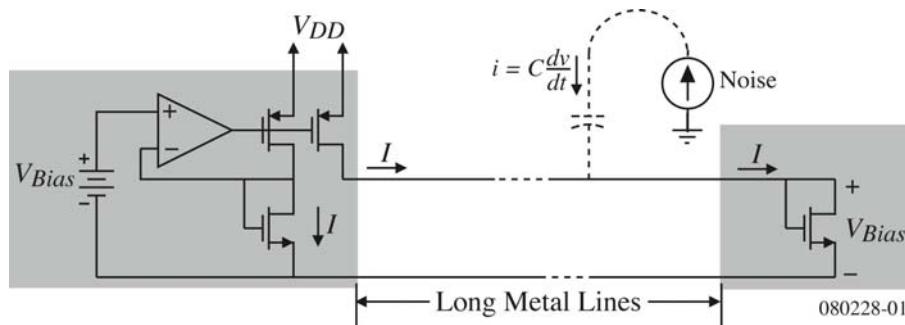
If the bus metal is $50\text{m}\Omega/\text{sq}$. and is $5\mu\text{m}$ wide, the resistance of the bus in one direction is $(50\text{m}\Omega/\text{sq.}) \times (1000\mu\text{m}/5\mu\text{m}) = 10\Omega$. The difference in drain currents for an overdrive of 0.1V is,

$$V_{GS1} = 1\text{mV} + V_{GS2} + 1\text{mV} = V_{GS2} + 2\text{mV}$$

$$\frac{I_{D1}}{I_{D2}} = \frac{(V_{GS1}-V_{TN})^2}{(V_{GS2}-V_{TN})^2} = \frac{(V_{GS2}-V_{TN}+2\text{mV})^2}{(V_{GS2}-V_{TN})^2} = \left(\frac{0.1+0.002}{0.1} \right)^2 = 1.04$$

Use Current to Avoid *IR* Drops in Long Metal Lines

Example:

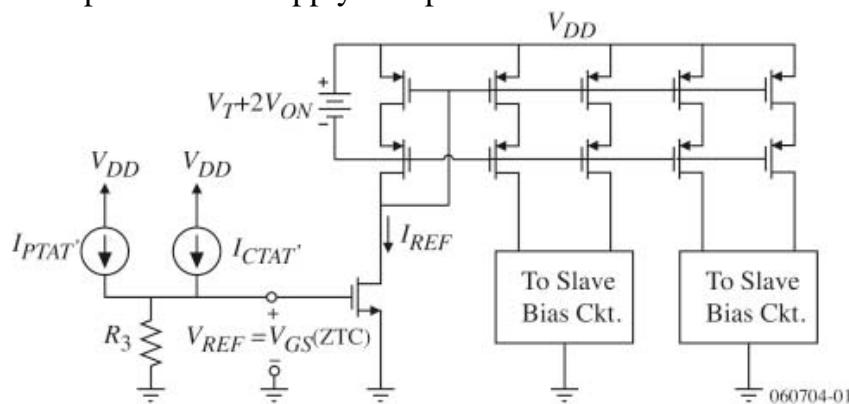


CMOS Analog Circuit Design

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Practical Aspects of Temperature-Independent and Supply-Independent Biasing

A temperature-independent and supply-independent current source and its distribution:



The currents are used to distribute the bias voltages to remote sections of the chip.

Practical Aspects of Bias Distribution Circuits - Continued

Distribution of the current avoids change in bias voltage due to IR drop in bias lines.

Slave bias circuit:

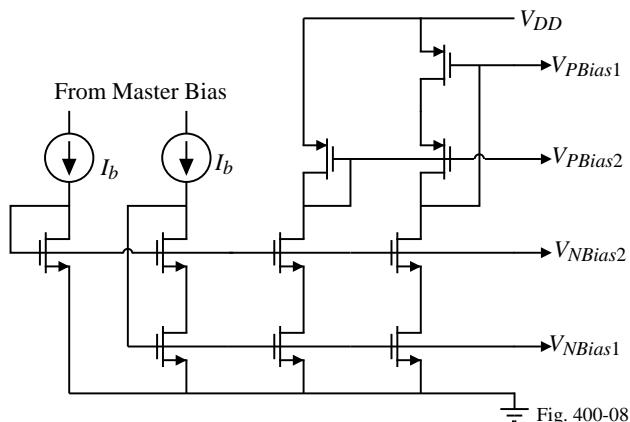


Fig. 400-08

From here on out in these notes,

$$V_{PBias1} = V_{PB1} = V_{DD} - |V_{TP}| - V_{SD}(\text{sat}) \quad V_{PBias2} = V_{PB2} = V_{DD} - |V_{TP}| - 2V_{SD}(\text{sat})$$

and

$$V_{NBias1} = V_{NB1} = V_{TN} + V_{DS}(\text{sat}) \quad V_{NBias2} = V_{NB2} = V_{TN} + 2V_{DS}(\text{sat})$$

SUMMARY OF TEMPERATURE STABLE REFERENCES

- The classical form of the temperature stable reference has a value of voltage close to the bandgap voltage and is called the “bandgap voltage reference”.
- Bandgap voltage references can achieve temperature dependence less than 50 ppm/ $^{\circ}\text{C}$
- Correction of second-order effects in the bandgap voltage reference can achieve very stable (1 ppm/ $^{\circ}\text{C}$) voltage references.
- Watch out for second-order effects such as noise when using the bandgap voltage reference in sensitive applications.
- Distribution of bias voltages over a long distance should be done by current rather than voltage.

LECTURE 180 – INVERTING AMPLIFIERS

LECTURE ORGANIZATION

Outline

- Introduction
- Active Load Inverting Amplifier
- Current Source Load Inverting Amplifier
- Push-Pull Inverting Amplifier
- Noise Analysis of Inverting Amplifiers
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 168-180

INTRODUCTION

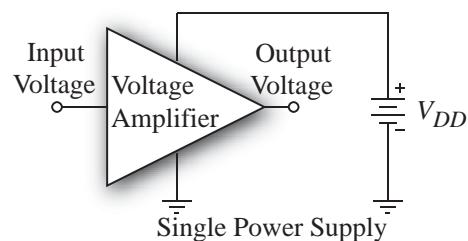
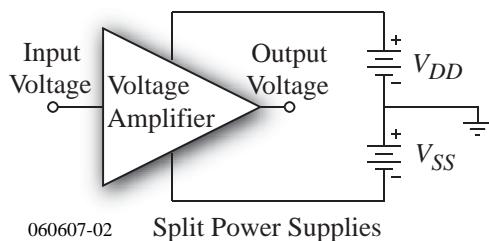
Types of Amplifiers

Type of Amplifier	Gain = $\frac{\text{Output}}{\text{Input}}$	Ideal Input Resistance	Ideal Output Resistance
Voltage	$A_v = \frac{\text{Output Voltage}}{\text{Input Voltage}}$	Infinite	Zero
Current	$A_i = \frac{\text{Output Current}}{\text{Input Current}}$	Zero	Infinite
Transconductance	$G_m = \frac{\text{Output Current}}{\text{Input Voltage}}$	Infinite	Infinite
Transresistance	$R_m = \frac{\text{Output Voltage}}{\text{Input Current}}$	Zero	Zero

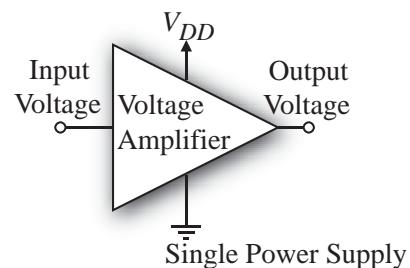
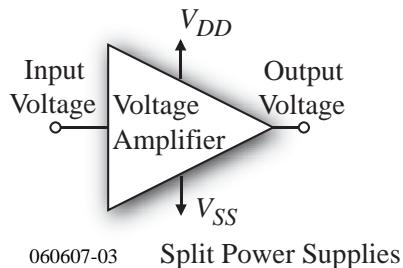
Most CMOS amplifiers fit naturally into the transconductance amplifier category as they have large input resistance and fairly large output resistance.

If the load resistance is high, the CMOS transconductance amplifier is essentially a voltage amplifier.

Amplifier Notation



Simpler notation:



Characterization of an Amplifier

1.) Large signal static characterization:

- Plot of output versus input (transfer curve)
- Large signal gain
- Output and input swing limits

2.) Small signal static characterization:

- AC gain
- AC input resistance
- AC output resistance

3.) Small signal dynamic characterization:

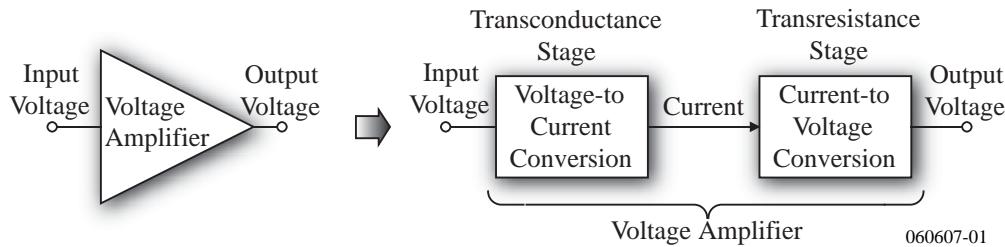
- Bandwidth
- Noise
- Power supply rejection

4.) Large signal dynamic characterization:

- Slew rate
- Nonlinearity

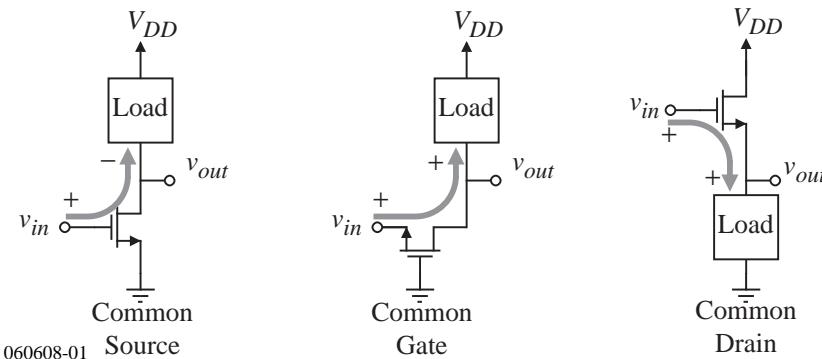
Components of a CMOS Voltage/Transconductance Amplifier

- 1.) A transconductance stage that converts the input voltage to current.
- 2.) A transresistance stage (load) that converts the current from the transconductance stage back to voltage.



Inverting and Noninverting Amplifiers

The types of amplifiers are based on the various configurations of the actual transistors. If we assume that one terminal of the transistor is grounded, then three possibilities result:

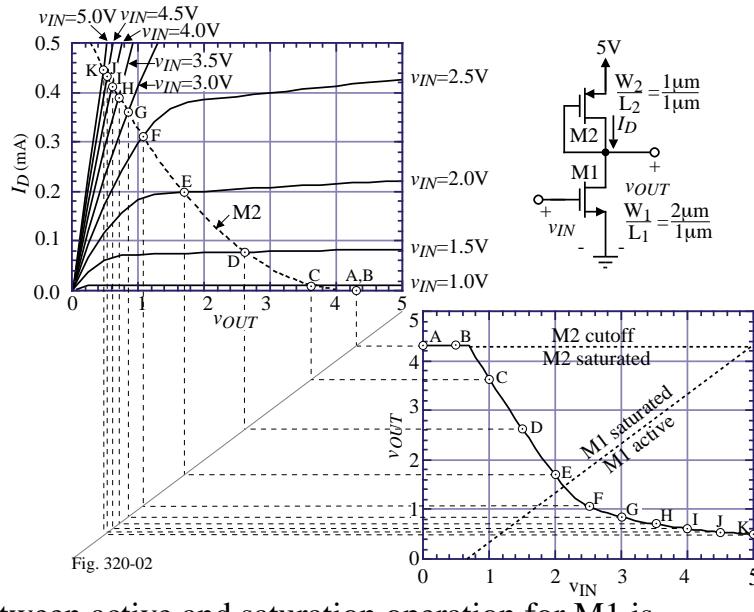


Note that there are two categories of amplifiers:

- 1.) Noninverting - Those whose input and output are in phase (common gate and common drain)
- 2.) Inverting - Those whose input and output are out of phase (common source)

ACTIVE LOAD INVERTING AMPLIFIER

Voltage Transfer Characteristic of the Active Load Inverter



The boundary between active and saturation operation for M1 is

$$v_{DS1} \geq v_{GS1} - V_{TN} \rightarrow v_{OUT} \geq v_{IN} - 0.7V$$

Large-Signal Voltage Swing Limits of the Active Load Inverter

Maximum output voltage, $v_{OUT(max)}$:

$$v_{OUT(max)} \approx V_{DD} - |V_{TP}|$$

(ignores subthreshold current influence on the MOSFET)

Minimum output voltage, $v_{OUT(min)}$:

Assume that M1 is nonsaturated and that $V_{T1} = |V_{T2}| = V_T$.

$$v_{DS1} \geq v_{GS1} - V_{TN} \rightarrow v_{OUT} \geq v_{IN} - 0.7V$$

The current through M1 is

$$i_D = \beta_1 \left((v_{GS1} - V_T)v_{DS1} - \frac{v_{DS1}^2}{2} \right) = \beta_1 \left((V_{DD} - V_T)(v_{OUT}) - \frac{(v_{OUT})^2}{2} \right)$$

and the current through M2 is

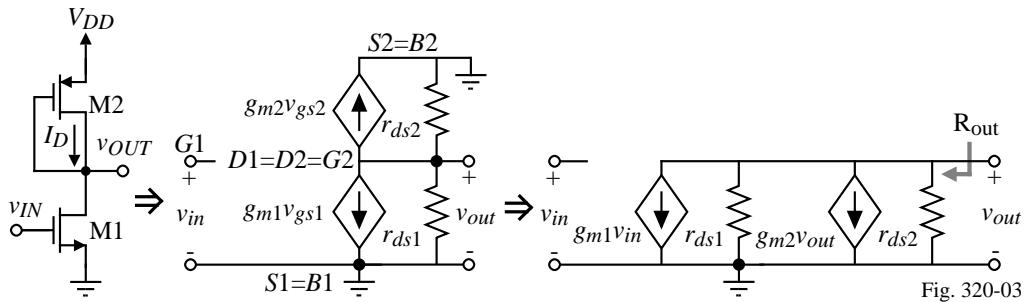
$$i_D = \frac{\beta_2}{2} (v_{SG2} - V_T)^2 = \frac{\beta_2}{2} (V_{DD} - v_{OUT} - V_T)^2 = \frac{\beta_2}{2} (v_{OUT} + V_T - V_{DD})^2$$

Equating these currents gives the minimum v_{OUT} as,

$$v_{OUT(min)} = V_{DD} - V_T - \frac{V_{DD} - V_T}{\sqrt{1 + (\beta_2/\beta_1)}}$$

Small-Signal Midband Performance of the Active Load Inverter

The development of the small-signal model for the active load inverter is shown below:



Sum the currents at the output node to get,

$$g_{m1}v_{in} + g_{ds1}v_{out} + g_{m2}v_{out} + g_{ds2}v_{out} = 0$$

Solving for the voltage gain, v_{out}/v_{in} , gives

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \cong -\frac{g_{m1}}{g_{m2}} = -\left(\frac{K'N W_1 L_2}{K' P L_1 W_2}\right)^{1/2}$$

The small-signal output resistance can also be found from the above by letting $v_{in} = 0$ to get,

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \cong \frac{1}{g_{m2}}$$

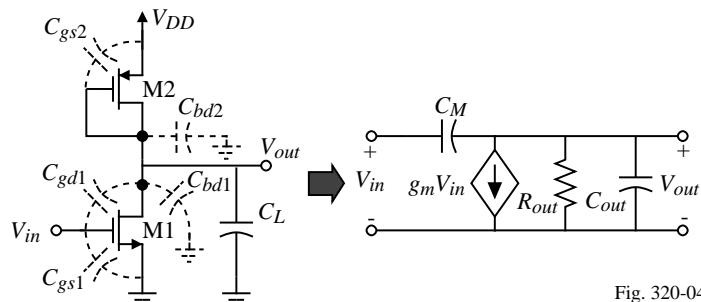
Frequency Response of the Active Load Inverter

Incorporation of the parasitic capacitors into the small-signal model:

If we assume the input voltage has a small source resistance, then we can write the following:

$$sC_M(V_{out} - V_{in}) + g_mV_{in} + G_{out}V_{out} + sC_{out}V_{out} = 0$$

$$\therefore V_{out}(G_{out} + sC_M + sC_{out}) = -(g_m - sC_M)V_{in}$$



$$\frac{V_{out}}{V_{in}} = \frac{-(g_m - sC_M)}{G_{out} + sC_M + sC_{out}} = -g_m R_{out} \left[\frac{1 - \frac{sC_M}{g_m}}{1 + sR_{out}(C_M + C_{out})} \right] = \frac{-g_m R_{out} \left(1 - \frac{s}{z_1} \right)}{1 - \frac{s}{p_1}}$$

$$\text{where } g_m = g_{m1}, \quad p_1 = \frac{-1}{R_{out}(C_{out} + C_M)}, \quad \text{and } z_1 = \frac{g_{m1}}{C_M}$$

$$\text{and } R_{out} = [g_{ds1} + g_{ds2} + g_{m2}]^{-1} \cong \frac{1}{g_{m2}}, \quad C_M = C_{gd1}, \quad \text{and} \quad C_{out} = C_{bd1} + C_{bd2} + C_{gs2} + C_L$$

Complex Frequency (*s*) Analysis of Circuits – (Optional)

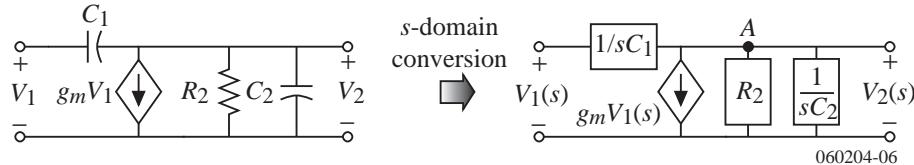
The frequency response of linear circuits can be analyzed using the complex frequency variable *s* which avoids having to solve the circuit in the time domain and then transform into the frequency domain.

Passive components in the *s* domain are:

$$Z_R(s) = R \quad Z_L(s) = sL \quad \text{and} \quad Z_C(s) = \frac{1}{sC}$$

s-domain analysis uses the complex impedance of elements as if they were “resistors”.

Example:



Sum currents flowing away from node A to get,

$$sC_1(V_2 - V_1) + g_m V_1 + G_2 V_2 + sC_2 V_2 = 0$$

Solving for the voltage gain transfer function gives,

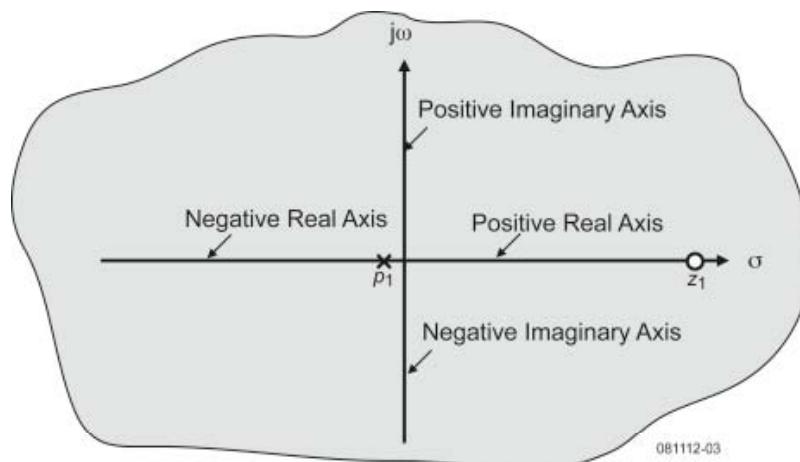
$$T(s) = \frac{V_2(s)}{V_1(s)} = \frac{-sC_1 + g_m}{s(C_1 + C_2) + G_2} = -g_m R_2 \left(\frac{sC_1/g_m - 1}{s(C_1 + C_2)R_2 + 1} \right)$$

Complex Frequency Plane – (Optional)

The complex frequency variable, *s*, is really a complex number and can be expressed as

$$s = \sigma + j\omega \quad \text{where } \sigma = \text{Re}[s] \text{ and } \omega = \text{Im}[s].$$

Complex frequency plane:



It is useful to plot the roots of the transfer function on the complex frequency plane.

For the previous $T(s)$, the roots are:

The numerator root (zero) is $s = z_1 = +(g_m/C_1)$

The denominator root (pole) is $s = p_1 = -[1/R_2(C_1 + C_2)]$

What is the Frequency Response of an Amplifier? – (Optional)

Frequency response results when we replace the complex frequency variable s with $j\omega$ in the transfer function of an amplifier. (This amounts to evaluating $T(s)$ on the imaginary axis of the complex frequency plane.)

The frequency response is characterized by the magnitude and phase of $T(j\omega)$.

Example:

$$\text{Assume } T(s) = \frac{a_0 + a_1 s}{b_0 + b_1 s} \quad s = j\omega \quad \rightarrow \quad T(j\omega) = \frac{a_0 + a_1 j\omega}{b_0 + b_1 j\omega} = \frac{a_0 + j\omega a_1}{b_0 + j\omega b_1}$$

Since $T(j\omega)$ is a complex number, we can express the magnitude and phase as,

$$|T(j\omega)| = \sqrt{\frac{a_0^2 + (\omega a_1)^2}{b_0^2 + (\omega b_1)^2}} \quad \text{Arg}[T(j\omega)] = +\tan^{-1}\left(\frac{\omega a_1}{a_0}\right) - \tan^{-1}\left(\frac{\omega b_1}{b_0}\right)$$

For the previous example, the magnitude and phase would be,

$$|T(j\omega)| = g_m R_2 \sqrt{\frac{1 + (\omega C_1/g_m)^2}{1 + [\omega R_2(C_1+C_2)]^2}} \quad \text{Arg}[T(j\omega)] = -\tan^{-1}(\omega C_1/g_m) - \tan^{-1}[\omega R_2(C_1+C_2)]$$

Note: Because the zero is on the positive real axis, the phase due to the zero is $-\tan^{-1}()$ rather than $+\tan^{-1}()$. More about that later.

Linear Graphical Illustration of Magnitude and Phase – (Optional)

The important concepts of frequency response are communicated through the graphical portrayal of the magnitude and phase.

Consider our example,

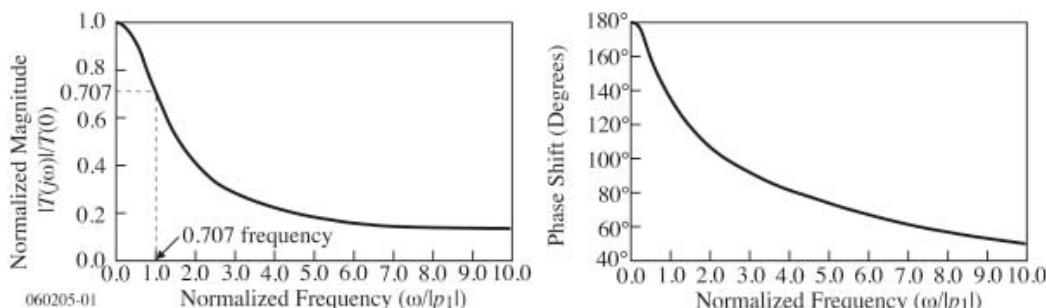
$$T(s) = \frac{V_2(s)}{V_1(s)} = -g_m R_2 \left(\frac{sC_1/g_m - 1}{s(C_1+C_2)R_2 + 1} \right) = -T(0) \left(\frac{s/z_1 - 1}{s/p_1 - 1} \right)$$

where $T(0) = g_m R_2$, $z_1 = +(g_m/C_1)$ and $p_1 = -[1/R_2(C_1+C_2)]$.

Replacing s with $j\omega$ gives [remember $\tan^{-1}(-x) = -\tan^{-1}(x)$],

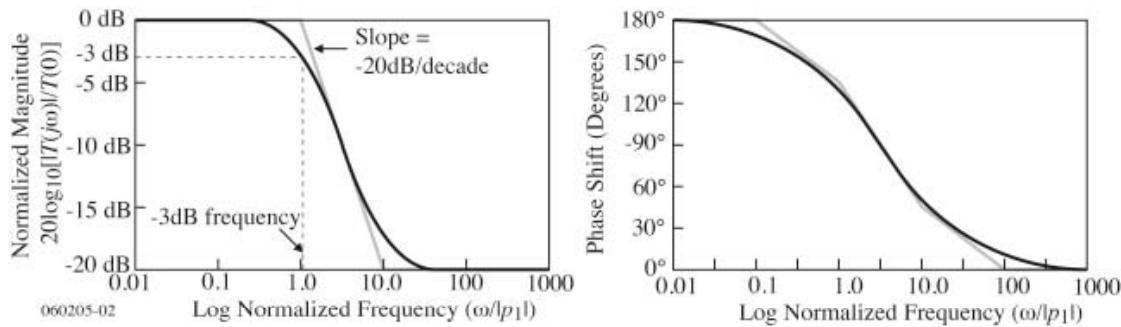
$$|T(j\omega)| = T(0) \sqrt{\frac{1 + (\omega/z_1)^2}{1 + (\omega/p_1)^2}} \quad \text{and} \quad \text{Arg}[T(j\omega)] = \pm 180^\circ - \tan^{-1}(\omega/z_1) - \tan^{-1}[\omega/p_1]$$

Graphically, we get the following if we assume $|p_1| = 0.1|z_1|$,



Logarithmic Graphical Illustration of Frequency Response – (Optional)

If the frequency range is large, it is more useful to use a logarithmic scale for the frequency. In addition, if one expresses the magnitude as $20 \log_{10}(|T(j\omega)|)$, the plots can be closely approximated with straight lines which enables quick analysis by hand. Such plots are called *Bode plots*.



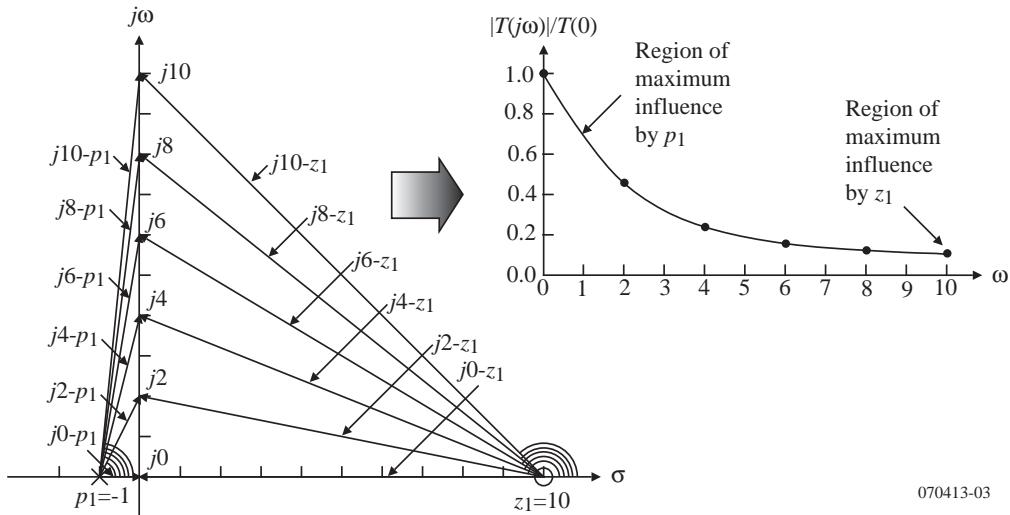
To construct a Bode asymptotic magnitude plot for a low pass transfer function in the form of products of roots:

- 1.) Start at a low frequency and plot $20 \log_{10}(|T(0)|)$ until you reach the smallest root.
- 2.) At the frequency equal to magnitude of the smallest root, change to a line with a slope of +20dB/decade if the root is a zero or -20dB/decade if the root is a pole.
- 3.) Continue increasing in frequency until you have plotted the influence of all roots.

The Influence of the Complex Frequency Plane on Frequency Response – (Optional)

The root locations in the complex frequency plane have a direct influence on the frequency response as illustrated below. Consider the transfer function:

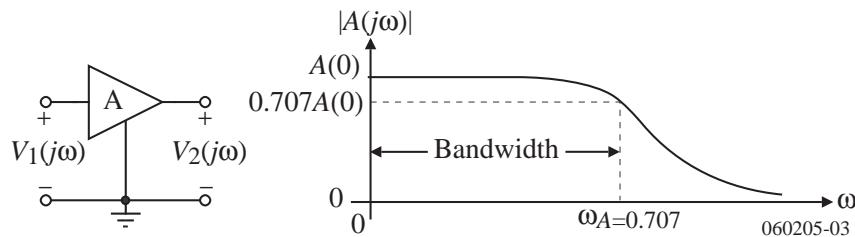
$$T(s) = -T(0) \left(\frac{s/z_1 - 1}{s/p_1 - 1} \right) = -\frac{|p_1|}{z_1} T(0) \left(\frac{s-z_1}{s-p_1} \right) = -0.1 T(0) \left(\frac{s-z_1}{s-p_1} \right) \quad \text{where } z_1 = 10|p_1|$$



Note: The roots maximally influence the magnitude when ω is such that the angle between the vector and the horizontal axis is 45° . This occurs at $j1$ for p_1 and $j10$ for z_1 .

Bandwidth of a Low-Pass Amplifier – (Optional)

One of the most important aspects of frequency analysis is to find the frequency at which the amplitude decreases by -3dB or $1/\sqrt{2}$. This can easily be found from the magnitude of the frequency response.



Amplifier with a Dominant Root:

Since the amplifier is low-pass, the poles will be smaller in magnitude than the zeros. If one of the poles is approximately 4-5 times smaller than the next smallest pole, the bandwidth of the amplifier is given as

$$\text{Bandwidth} \approx |\text{Smallest pole}|$$

Amplifier with no Dominant Root:

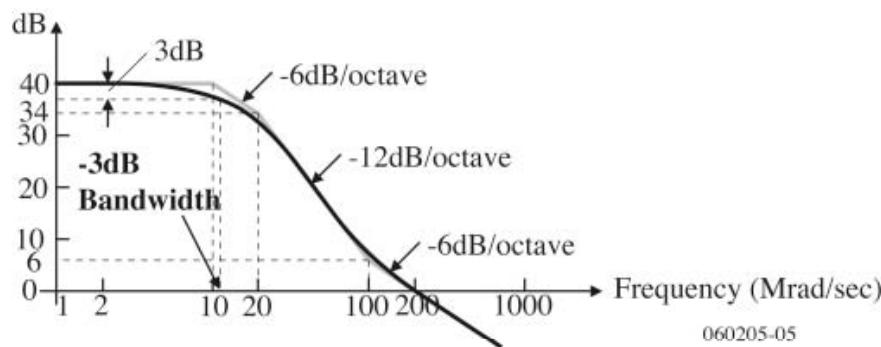
If there are several poles with roughly the same magnitude, then one should use the graphical method above to find the bandwidth.

Example of Finding the Bandwidth of an Amplifier– (Optional)

Suppose an amplifier has a pole at -10 rads/sec and another at -20 rads/sec. and a zero at +50 radians/sec. Find the bandwidth of this amplifier if the low frequency gain is 100.

Solution

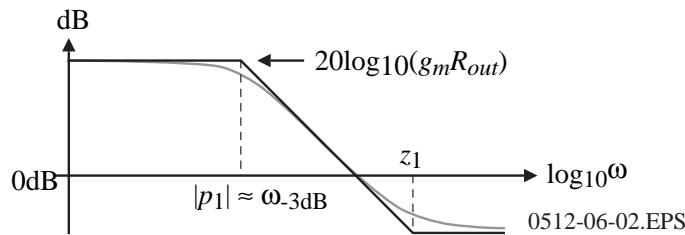
Since the poles are close together, construct a Bode plot and graphically find the bandwidth.



From the graph, we see that the -3dB bandwidth is close to 11-12 Mrad/sec or 1.75-1.91MHz.

Frequency Response of the Active Inverter - Continued

So, back to the frequency response of the active load inverter, we find that if $|p_1| < z_1$, then the -3dB frequency is approximately equal to the magnitude of the pole which is $[R_{out}(C_{out}+C_M)]^{-1}$.



Observation:

In general, the poles in a MOSFET circuit can be found by summing the capacitance connected to a node and multiplying this capacitance times the equivalent resistance from this node to ground and inverting the product.

Example 180 -1 - Performance of an Active Resistor-Load Inverter

Calculate the output-voltage swing limits for $V_{DD} = 5$ volts, the small-signal gain, the output resistance, and the -3 dB frequency of active load inverter if $(W_1/L_1) = 2 \mu\text{m}/1 \mu\text{m}$ and $W_2/L_2 = 1 \mu\text{m}/1 \mu\text{m}$, $C_{gd1} = 100\text{fF}$, $C_{bd1} = 200\text{fF}$, $C_{bd2} = 100\text{fF}$, $C_{gs2} = 200\text{fF}$, $C_L = 1 \text{ pF}$, and $I_{D1} = I_{D2} = 100\mu\text{A}$, using the parameters in Table 3.1-2.

Solution

From the above results we find that:

$$v_{OUT}(\max) = 4.3 \text{ volts}$$

$$v_{OUT}(\min) = 0.418 \text{ volts}$$

$$\text{Small-signal voltage gain} = -1.92\text{V/V}$$

$$R_{out} = 9.17 \text{ k}\Omega \text{ including } g_{ds1} \text{ and } g_{ds2} \text{ and } 10 \text{ k}\Omega \text{ ignoring } g_{ds1} \text{ and } g_{ds2}$$

$$z_1 = 2.10 \times 10^9 \text{ rads/sec}$$

$$p_1 = -64.1 \times 10^6 \text{ rads/sec.}$$

Thus, the -3 dB frequency is 10.2 MHz.

CURRENT SOURCE INVERTER

Voltage Transfer Characteristic of the Current Source Inverter

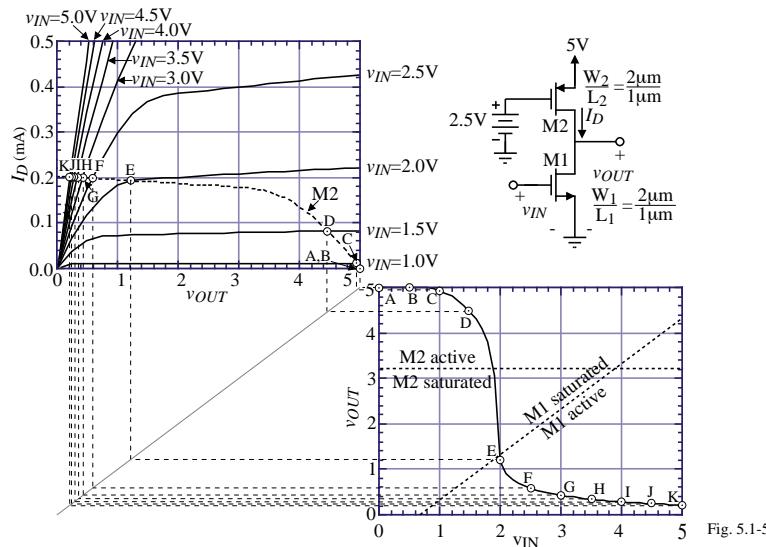


Fig. 5.1-5

Regions of operation for the transistors:

$$M1: v_{DS1} \geq v_{GS1} - V_{Th} \rightarrow v_{OUT} \geq v_{IN} - 0.7V$$

$$M2: v_{SD2} \geq v_{SG2} - |V_{Tp}| \rightarrow V_{DD} - v_{OUT} \geq V_{DD} - V_{GG2} - |V_{Tp}| \rightarrow v_{OUT} \leq 3.2V$$

Large-Signal Voltage Swing Limits of the Current Source Load Inverter

Maximum output voltage, $v_{OUT(max)}$:

$$v_{OUT(max)} \approx V_{DD}$$

Minimum output voltage, $v_{OUT(min)}$:

Assume that M1 is nonsaturated. The minimum output voltage is,

$$v_{OUT(min)} = \left[v_{OUT(min)} = (V_{DD} - V_{T1}) \sqrt{1 + \frac{(\beta_2)}{\beta_1} \left(\frac{V_{DD} - V_{GG} - |V_{T2}|}{V_{DD} - V_{T1}} \right)^2} \right]$$

This result assumes that v_{IN} is taken to V_{DD} .

Small-Signal Midband Performance of the Current Source Load Inverter

Small-Signal Model:

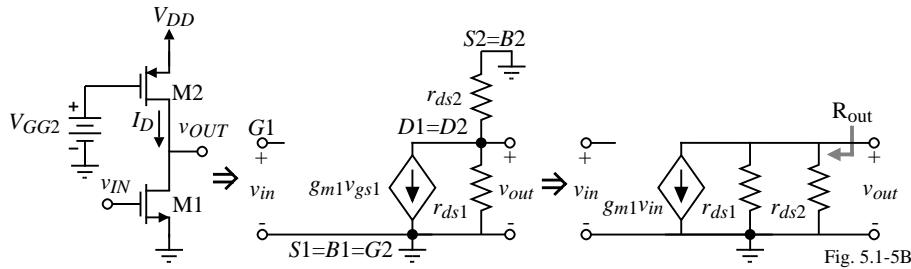
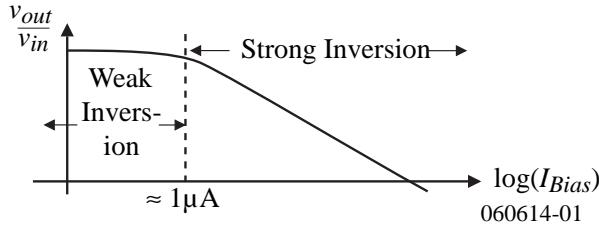


Fig. 5.1-5B

Midband Performance:

$$\frac{v_{out}}{v_{in}} = \frac{-g_m1}{g_{ds1} + g_{ds2}} = \left(\frac{2K'_N W_1}{L_1 I_D} \right)^{1/2} \left(\frac{-1}{\lambda_1 + \lambda_2} \right) \propto \frac{1}{\sqrt{I_D}} \quad !!! \quad \text{and } R_{out} = \frac{1}{g_{ds1} + g_{ds2}} \cong \frac{1}{I_D(\lambda_1 + \lambda_2)}$$



Frequency Response of the Current Source Load Inverter

Incorporation of the parasitic capacitors into the small-signal model (x is connected to V_{GG2}):

If we assume the input voltage has a small source resistance, then we can write the following:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-g_m R_{out} \left(1 - \frac{s}{z_1} \right)}{1 - \frac{s}{p_1}}$$

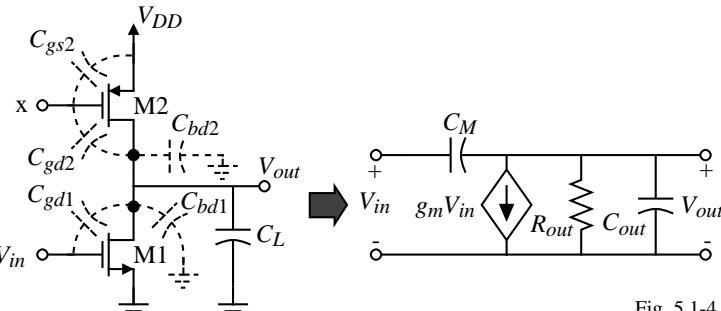


Fig. 5.1-4

where $g_m = g_{m1}$, $p_1 = \frac{-1}{R_{out}(C_{out} + C_M)}$, and $z_1 = \frac{g_m}{C_M}$

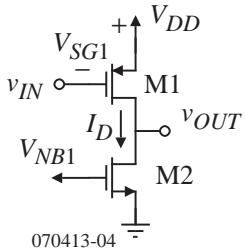
and $R_{out} = \frac{1}{g_{ds1} + g_{ds2}}$ and $C_{out} = C_{gd1} + C_{bd1} + C_{gd2} + C_{bd2} + C_L$ $C_M = C_{gd1}$

Therefore, if $|p_1| < |z_1|$, then the -3 dB frequency response can be expressed as

$$\omega_{-3dB} \approx \omega_1 = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}$$

Example 180-2 - Performance of a Current-Sink Inverter

A current-sink inverter is shown. Assume that $W_1 = 2 \mu\text{m}$, $L_1 = 1 \mu\text{m}$, $W_2 = 1 \mu\text{m}$, $L_2 = 1 \mu\text{m}$, $V_{DD} = 5$ volts, $V_{NB1} = 3$ volts, and the parameters of Table 3.1-2 describe M1 and M2. Use the capacitor values of Example 180-1 ($C_{gd1} = C_{gd2}$). Calculate the output-swing limits and the small-signal performance.



Solution

To attain the output signal-swing limitations, we treat current sink inverter as a current source CMOS inverter with PMOS parameters for the NMOS and NMOS parameters for the PMOS and use NMOS equations. Using a prime notation to designate the results of the current source CMOS inverter that exchanges the PMOS and NMOS model parameters,

$$v_{OUT}(\max)' = 5\text{V} \text{ and } v_{OUT}(\min)' = (5-0.7)\left[1 - \sqrt{1 - \left(\frac{110 \cdot 1}{50 \cdot 2}\right)\left(\frac{3-0.7}{5-0-0.7}\right)^2}\right] = 0.74\text{V}$$

In terms of the current sink CMOS inverter, these limits are subtracted from 5V to get $v_{OUT}(\max) = 4.26\text{V}$ and $v_{OUT}(\min) = 0\text{V}$.

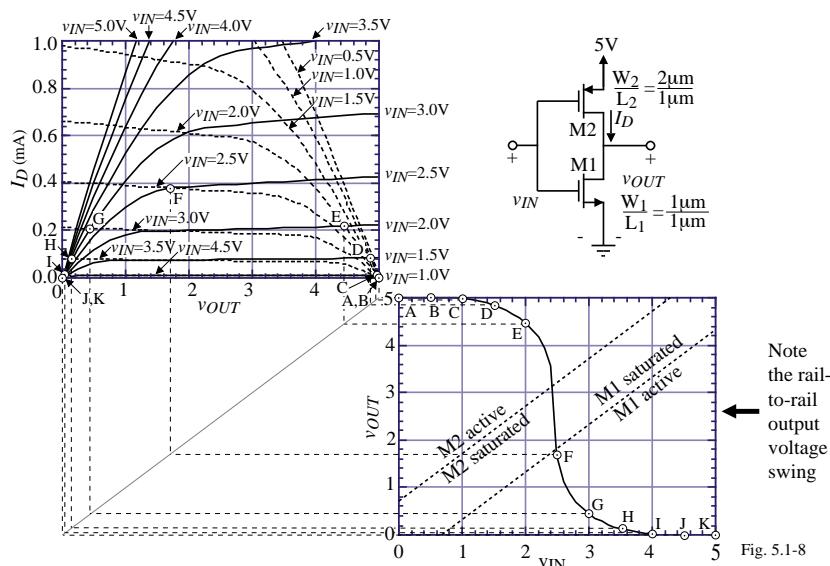
To find the small signal performance, first calculate the dc current. The dc current, I_D , is

$$I_D = \frac{K_N' W_1}{2L_1} (V_{GG1} - V_{TN})^2 = \frac{110 \cdot 1}{2 \cdot 1} (3-0.7)^2 = 291 \mu\text{A}$$

$$v_{out}/v_{in} = -9.2\text{V/V}, \quad R_{out} = 38.1 \text{ k}\Omega, \quad \text{and} \quad f_{-3\text{dB}} = 2.78 \text{ MHz.}$$

PUSH-PULL INVERTING AMPLIFIER

Voltage Transfer Characteristic of the Push-Pull Inverting Amplifier



Regions of operation for M1 and M2:

$$\text{M1: } v_{DS1} \geq v_{GS1} - V_{T1} \rightarrow v_{OUT} \geq v_{IN} - 0.7\text{V}$$

$$\text{M2: } v_{SD2} \geq v_{SG2} - |V_{T2}| \rightarrow V_{DD} - v_{OUT} \geq V_{DD} - v_{IN} - |V_{T2}| \rightarrow v_{OUT} \leq v_{IN} + 0.7\text{V}$$

Small-Signal Performance of the Push-Pull Amplifier

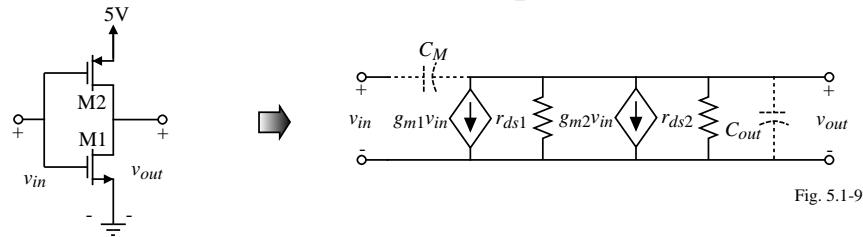


Fig. 5.1-9

Small-signal analysis gives the following results:

$$\frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} = -\sqrt{(2/I_D)} \left[\frac{\sqrt{K'_N(W_1/L_1)} + \sqrt{K'_P(W_2/L_2)}}{\lambda_1 + \lambda_2} \right]$$

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

$$z = \frac{g_{m1} + g_{m2}}{C_M} = \frac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}} \quad \text{and} \quad p_1 = \frac{-(g_{ds1} + g_{ds2})}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}$$

If $z_1 > |p_1|$, then

$$\omega_{-3dB} = \frac{g_{ds1} + g_{ds2}}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}$$

Example 180-3 - Performance of a Push-Pull Inverter

The performance of a push-pull CMOS inverter is to be examined. Assume that $W_1 = 1 \mu\text{m}$, $L_1 = 1 \mu\text{m}$, $W_2 = 2 \mu\text{m}$, $L_2 = 1 \mu\text{m}$, $V_{DD} = 5$ volts, and use the parameters of Table 3.1-2 to model M1 and M2. Use the capacitor values of Example 180-1 ($C_{gd1} = C_{gd2}$). Calculate the output-swing limits and the small-signal performance assuming that $I_{D1} = I_{D2} = 300 \mu\text{A}$.

Solution

The output swing is seen to be from 0V to 5V. In order to find the small signal performance, we will make the important assumption that both transistors are operating in the saturation region. Therefore:

$$\frac{v_{out}}{v_{in}} = \frac{-257 \mu\text{S} - 245 \mu\text{S}}{12 \mu\text{S} + 15 \mu\text{S}} = -18.6 \text{V/V}$$

$$R_{out} = 37 \text{ k}\Omega$$

$$f_{-3dB} = 2.86 \text{ MHz}$$

and

$$z_1 = 399 \text{ MHz}$$

NOISE ANALYSIS OF INVERTING AMPLIFIERS

Noise Analysis of Inverting Amplifiers

Noise model:

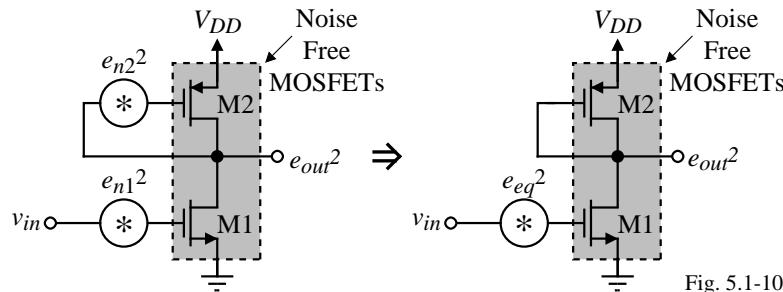


Fig. 5.1-10

Approach:

- 1.) Assume a mean-square input-voltage-noise spectral density e_n^2 in series with the gate of each MOSFET.
(This step assumes that the MOSFET is the common source configuration.)
- 2.) Calculate the output-voltage-noise spectral density, e_{out}^2 (Assume all sources are additive).
- 3.) Refer the output-voltage-noise spectral density back to the input to get equivalent input noise e_{eq}^2 .
- 4.) Substitute the type of noise source, 1/f or thermal.

Noise Analysis of the Active Load Inverter

- 1.) See model to the right.

$$2.) e_{out}^2 = e_{n1}^2 \left(\frac{g_{m1}}{g_{m2}} \right)^2 + e_{n2}^2$$

$$3.) e_{eq}^2 = e_{n1}^2 \left[1 + \left(\frac{g_{m2}}{g_{m1}} \right)^2 \left(\frac{e_{n2}}{e_{n1}} \right)^2 \right]$$

Up to now, the type of noise is not defined.

1/f Noise

Substituting $e_n^2 = \frac{K_F}{2fC_{ox}WLK} = \frac{B}{fWL}$, into the above gives,

$$e_{eq(1/f)}^2 = \left(\frac{B_1}{fW_1L_1} \right) \left[1 + \left(\frac{K'_2B_2}{K'_1B_1} \right) \left(\frac{L_1}{L_2} \right)^2 \right] \rightarrow e_{eq(1/f)} = \left(\frac{B_1}{fW_1L_1} \right)^{1/2} \left[1 + \left(\frac{K'_2B_2}{K'_1B_1} \right) \left(\frac{L_1}{L_2} \right)^2 \right]^{1/2}$$

To minimize 1/f noise, 1.) Make $L_2 \gg L_1$, 2.) increase the value of W_1 and 3.) choose M1 as a PMOS.

Thermal Noise

Substituting $e_n^2 = \frac{8kT}{3g_m}$ into the above gives,

$$e_{eq(th)} = \left\{ \left(\frac{8kT}{3[2K'_1(W/L)_1 I_1]^{1/2}} \right) \left[1 + \left(\frac{W_2 L_1 K'_2}{L_2 W_1 K'_1} \right)^2 \right]^{1/2} \right\}^{1/2}$$

To minimize thermal noise, maximize the gain of the inverter.

Noise Analysis of the Active Load Inverter - Continued

When calculating the contribution of e_{n2}^2 to e_{out}^2 , it was assumed that the gain was unity. To verify this assumption consider the following model:

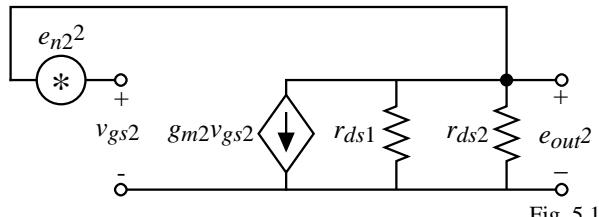


Fig. 5.1-11

We can show that,

$$\frac{e_{out}^2}{e_{n2}^2} = \left[\frac{g_m2(r_{ds1}\parallel r_{ds2})}{1 + g_m2(r_{ds1}\parallel r_{ds2})} \right]^2 \approx 1$$

Noise Analysis of the Current Source Load Inverting Amplifier

Model:

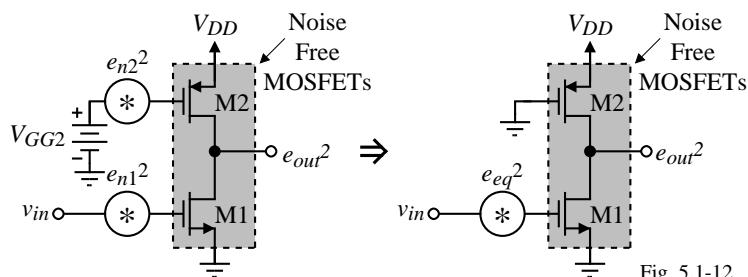


Fig. 5.1-12.

The output-voltage-noise spectral density of this inverter can be written as,

$$e_{out}^2 = (g_{m1}r_{out})^2e_{n1}^2 + (g_{m2}r_{out})^2e_{n2}^2$$

or

$$e_{eq}^2 = e_{n1}^2 + \frac{(g_{m2}r_{out})^2}{(g_{m1}r_{out})^2}e_{n2}^2 = e_{n1}^2 \left[1 + \left(\frac{g_{m2}}{g_{m1}} \right)^2 \frac{\overline{e_{n2}^2}}{e_{n1}^2} \right]$$

This result is identical with the active load inverter.

Thus the noise performance of the two circuits are equivalent although the small-signal voltage gain is significantly different.

Noise Analysis of the Push-Pull Amplifier

Model:

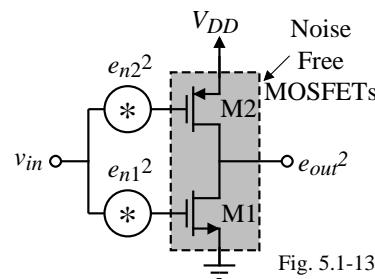


Fig. 5.1-13.

The equivalent input-voltage-noise spectral density of the push-pull inverter can be found as

$$e_{eq} = \sqrt{\left(\frac{g_{m1}e_{n1}}{g_{m1} + g_{m2}}\right)^2 + \left(\frac{g_{m2}e_{n2}}{g_{m1} + g_{m2}}\right)^2}$$

If the two transconductances are balanced ($g_{m1} = g_{m2}$), then the noise contribution of each device is divided by two.

The total noise contribution can only be reduced by reducing the noise contribution of each device.

(Basically, both M1 and M2 act like the “load” transistor and “input” transistor, so there is no defined input transistor that can cause the noise of the load transistor to be insignificant.)

SUMMARY

Table of Performance

Inverter	AC Voltage Gain	AC Output Resistance	Bandwidth (CGB=0)	Equivalent, input-referred, mean-square noise voltage
p-channel active load inverter	$\frac{-gm_1}{gm_2}$	$\frac{1}{gm_2}$	$\frac{gm_2}{CBD_1 + CGS_1 + CGS_2 + CBD_2}$	$e_{n1}^2 + e_{n2}^2 \left(\frac{gm_2}{gm_1} \right)^2$
Current source load inverter	$\frac{-gm_1}{gds_1 + gds_2}$	$\frac{1}{gds_1 + gds_2}$	$\frac{gds_1 + gds_2}{CBD_1 + CGD_1 + CDG_2 + CBD_2}$	$e_{n1}^2 + e_{n2}^2 \left(\frac{gm_2}{gm_1} \right)^2$
Push-Pull inverter	$\frac{-(gm_1 + gm_2)}{gds_1 + gds_2}$	$\frac{1}{gds_1 + gds_2}$	$\frac{gds_1 + gds_2}{CBD_1 + CGD_1 + CGS_2 + CBD_2}$	$\left(\frac{gm_1 e_{n1}}{gm_1 + gm_2} \right)^2 + \left(\frac{gm_2 e_{n2}}{gm_1 + gm_2} \right)^2$

LECTURE 190 – DIFFERENTIAL AMPLIFIER

LECTURE ORGANIZATION

Outline

- Characterization of a differential amplifier
- Differential amplifier with a current mirror load
- Differential amplifier with MOS diode loads
- An intuitive method of small signal analysis
- Large signal performance of differential amplifiers
- Differential amplifiers with current source loads
- Design of differential amplifiers
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 180-199

CHARACTERIZATION OF A DIFFERENTIAL AMPLIFIER

What is a Differential Amplifier?

A differential amplifier is an amplifier that amplifies the difference between two voltages and rejects the average or common mode value of the two voltages.

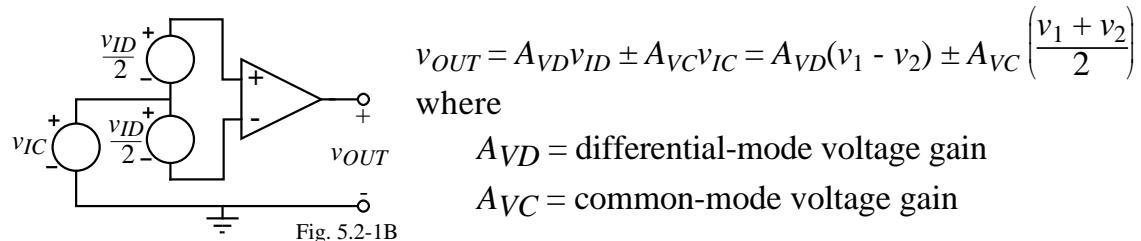
Differential and common mode voltages:

v_1 and v_2 are called *single-ended* voltages. They are voltages referenced to ac ground.

The *differential-mode* input voltage, v_{ID} , is the voltage difference between v_1 and v_2 .

The *common-mode* input voltage, v_{IC} , is the average value of v_1 and v_2 .

$$\therefore v_{ID} = v_1 - v_2 \quad \text{and} \quad v_{IC} = \frac{v_1 + v_2}{2} \Rightarrow v_1 = v_{IC} + 0.5v_{ID} \quad \text{and} \quad v_2 = v_{IC} - 0.5v_{ID}$$



Differential Amplifier Definitions

- Common mode rejection ratio (*CMRR*)

$$CMRR = \left| \frac{A_{VD}}{A_{VC}} \right|^3$$

CMRR is a measure of how well the differential amplifier rejects the common-mode input voltage in favor of the differential-input voltage.

- Input common-mode range (*ICMR*)

The input common-mode range is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

- Output offset voltage ($V_{OS(out)}$)

The output offset voltage is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

- Input offset voltage ($V_{OS}(\text{in}) = V_{OS}$)

The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

$$V_{OS} = \frac{V_{OS(\text{out})}}{A_{VD}}$$

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Transconductance Characteristic of the Differential Amplifier

Consider the following n-channel differential amplifier (called a source-coupled pair). Where should bulk be connected? Consider a p-well, CMOS technology:

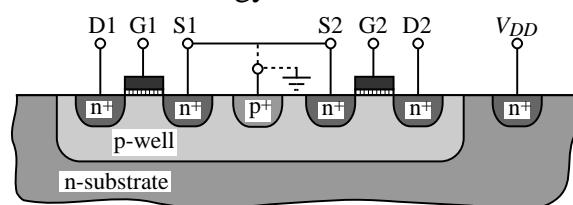


Fig. 5.2-3

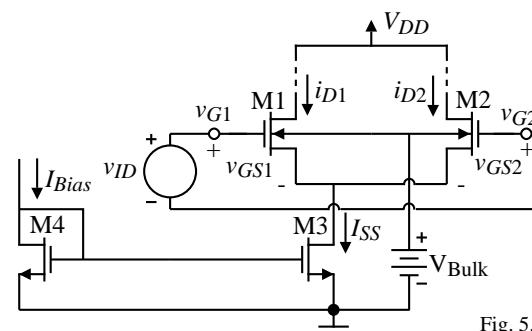
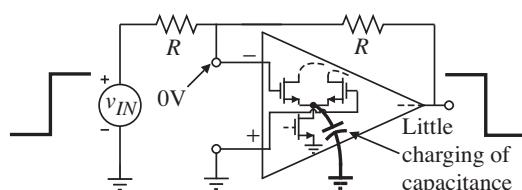


Fig. 5.2-2

- 1.) Bulks connected to the sources: No modulation of V_T but large common mode parasitic capacitance.
 - 2.) Bulks connected to ground: Smaller common mode parasitic capacitors, but modulation of V_T .

What are the implications of a large common mode capacitance?



The diagram shows a unity-gain feedback operational amplifier circuit. A square-wave input voltage V_{IN} is connected to the non-inverting terminal ($+$) through a resistor. The inverting terminal ($-$) is grounded. The output voltage is taken from the inverting terminal. Inside the op-amp symbol, a large transient current arrow points into the non-inverting terminal, indicating the flow of charge during the transition. A note to the right states "Large charging of capacitance".

Transconductance Characteristic of the Differential Amplifier - Continued

Defining equations:

$$v_{ID} = v_{GS1} - v_{GS2} = \left(\frac{2i_{D1}}{\beta}\right)^{1/2} - \left(\frac{2i_{D2}}{\beta}\right)^{1/2} \quad \text{and} \quad I_{SS} = i_{D1} + i_{D2}$$

Solution:

$$i_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2} \left(\frac{\beta v_{ID}}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2} \right)^{1/2} \quad \text{and} \quad i_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2} \left(\frac{\beta v_{ID}}{I_{SS}} - \frac{\beta^2 v_{ID}^4}{4I_{SS}^2} \right)^{1/2}$$

which are valid for $v_{ID} < 2(I_{SS}/\beta)^{1/2}$.

Illustration of the result:

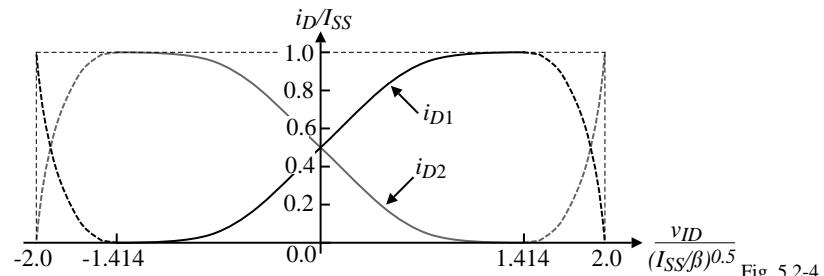


Fig. 5.2-4

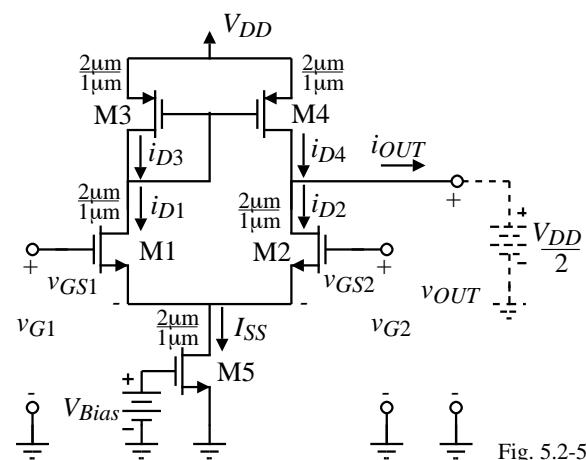
Differentiating i_{D1} (or i_{D2}) with respect to v_{ID} and setting $V_{ID} = 0V$ gives

$$g_m = \frac{di_{D1}}{dv_{ID}} (V_{ID} = 0) = \sqrt{\frac{bI_{SS}}{4}} = \sqrt{\frac{K'1 I_{SS} W_1}{4L_1}} \quad (\text{half the } g_m \text{ of an inverting amplifier})$$

DIFFERENTIAL AMPLIFIER WITH A CURRENT MIRROR LOAD

Voltage Transfer Characteristic of the Differential Amplifier

In order to obtain the voltage transfer characteristic, a load for the differential amplifier must be defined. We will select a current mirror load as illustrated below.



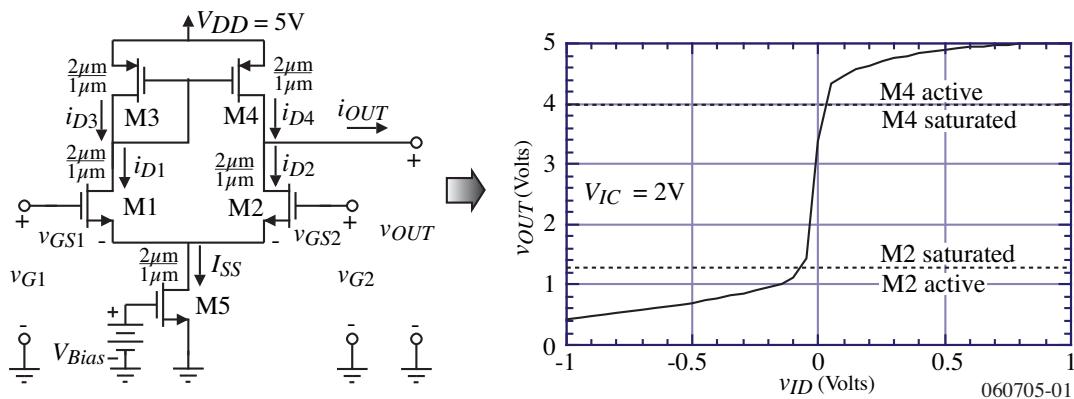
Note that output signal to ground is equivalent to the differential output signal due to the current mirror.

The short-circuit, transconductance is given as

$$g_m = \frac{di_{OUT}}{dv_{ID}} (V_{ID} = 0) = \sqrt{\beta I_{SS}} = \sqrt{\frac{K'1 I_{SS} W_1}{L_1}}$$

Fig. 5.2-5

Voltage Transfer Function of the Differential Amplifier with a Current Mirror Load



Regions of operation of the transistors:

M2 is saturated when,

$$v_{DS2} \geq v_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{S1} \geq V_{IC} - 0.5v_{ID} - V_{S1} - V_{TN} \rightarrow v_{OUT} \geq V_{IC} - V_{TN}$$

where we have assumed that the region of transition for M2 is close to $v_{ID} = 0V$.

M4 is saturated when,

$$v_{SD4} \geq v_{SG4} - |V_{TP}| \rightarrow V_{DD} - v_{OUT} \geq V_{SG4} - |V_{TP}| \rightarrow v_{OUT} \leq V_{DD} - V_{SG4} + |V_{TP}|$$

The regions of operations shown on the voltage transfer function assume $I_{SS} = 100\mu A$.

Note: $V_{SG4} = \sqrt{\frac{2.50}{50.2}} + |V_{TP}| = 1 + |V_{TP}| \Rightarrow v_{OUT} \leq 5 - 1 - 0.7 + 0.7 = 4V$

Differential Amplifier Using p-channel Input MOSFETs

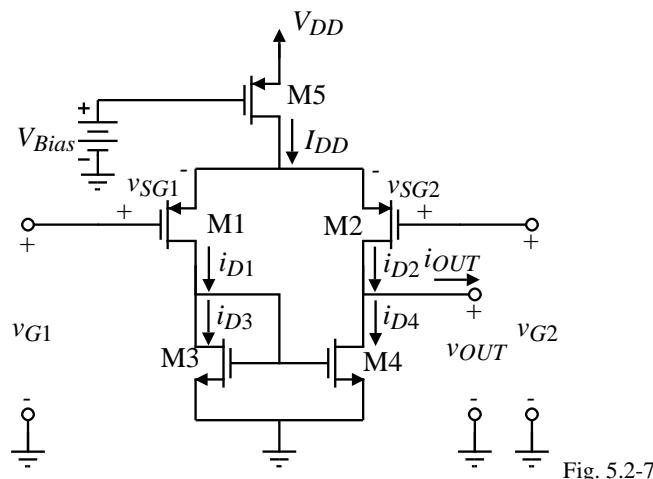


Fig. 5.2-7

Input Common Mode Range (ICMR)

ICMR is found by setting $v_{ID} = 0$ and varying v_{IC} until one of the transistors leaves the saturation.

Highest Common Mode Voltage

Path from G1 through M1 and M3 to V_{DD} :

$$V_{IC(\max)} = V_{G1}(\max) = V_{G2}(\max)$$

$$= V_{DD} - V_{SG3} - V_{DS1}(\text{sat}) + V_{GS1}$$

or

$$V_{IC(\max)} = V_{DD} - V_{SG3} + V_{TN1}$$

Path from G2 through M2 and M4 to V_{DD} :

$$V_{IC(\max)}' = V_{DD} - V_{SD4}(\text{sat}) - V_{DS2}(\text{sat}) + V_{GS2}$$

$$= V_{DD} - V_{SD4}(\text{sat}) + V_{TN2}$$

$$\therefore \boxed{V_{IC(\max)} = V_{DD} - V_{SG3} + V_{TN1}}$$

Lowest Common Mode Voltage (Assume a V_{SS} for generality)

$$\boxed{V_{IC(\min)} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}}$$

where we have assumed that $V_{GS1} = V_{GS2}$ during changes in the input common mode voltage.

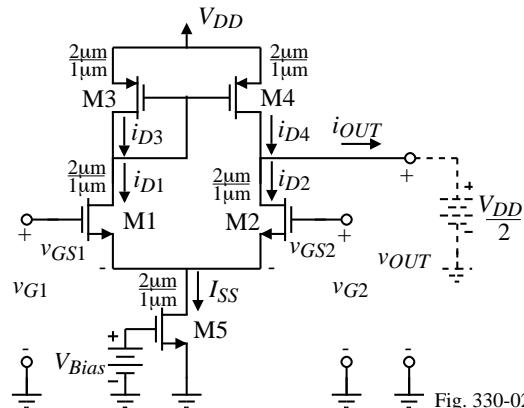


Fig. 330-02

Example 190-1 - Small-Signal Analysis of the Differential-Mode of the Diff. Amp

A requirement for differential-mode operation is that the differential amplifier is balanced[†]

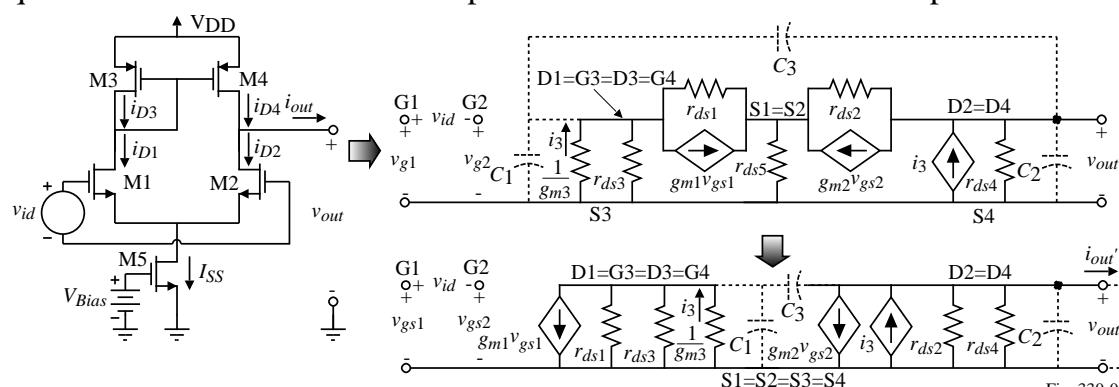


Fig. 330-03

Differential Transconductance:

Assume that the output of the differential amplifier is an ac short.

$$i_{\text{out}}' = \frac{g_{m1}g_{m3}r_{p1}}{1 + g_{m3}r_{p1}} v_{gs1} - g_{m2}v_{gs2} \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}v_{id}$$

where $g_{m1} = g_{m2} = g_{md}$, $r_{p1} = r_{ds1} \parallel r_{ds3}$ and i'_{out} designates the output current into a short circuit.

[†] It can be shown that the current mirror causes this requirement to be invalid because the drain loads are not matched. However, we will continue to use the assumption regardless.

Small-Signal Analysis of the Differential-Mode of the Diff. Amplifier - Continued

Output Resistance:

$$r_{\text{out}} = \frac{1}{g_{ds2} + g_{ds4}} = r_{ds2} \| r_{ds4}$$

Differential Voltage Gain:

$$A_v = \frac{v_{\text{out}}}{v_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}$$

If we assume that all transistors are in saturation and replace the small signal parameters of g_m and r_{ds} in terms of their large-signal model equivalents, we achieve

$$A_v = \frac{v_{\text{out}}}{v_{id}} = \frac{(K'_1 I_{SS} W_1 / L_1)^{1/2}}{(\lambda_2 + \lambda_4)(I_{SS}/2)} = \frac{2}{\lambda_2 + \lambda_4} \left(\frac{K'_1 W_1}{I_{SS} L_1} \right)^{1/2} \propto \frac{1}{\sqrt{I_{SS}}}$$

Note that the small-signal gain is inversely proportional to the square root of the bias current!

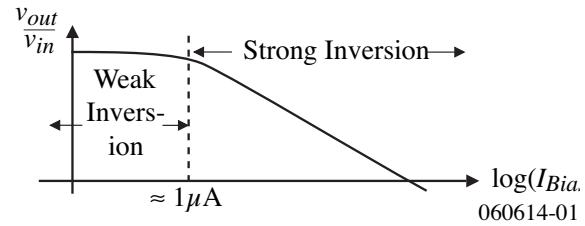
Example:

If $W_1/L_1 = 2\mu\text{m}/1\mu\text{m}$ and $I_{SS} = 50\mu\text{A}$ ($10\mu\text{A}$), then

$$A_v(\text{n-channel}) = 46.6\text{V/V} (104.23\text{V/V})$$

$$A_v(\text{p-channel}) = 31.4\text{V/V} (70.27\text{V/V})$$

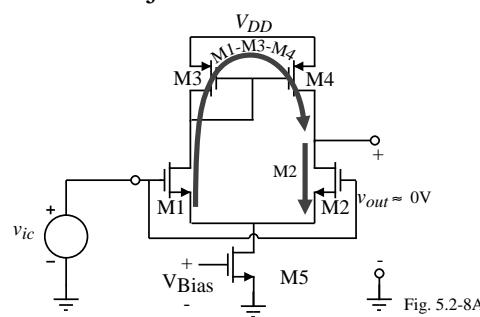
$$r_{\text{out}} = \frac{1}{g_{ds2} + g_{ds4}} = \frac{1}{25\mu\text{A} \cdot 0.09\text{V}^{-1}} = 0.444\text{M}\Omega (2.22\text{M}\Omega)$$



060614-01

Common Mode Analysis for the Current Mirror Load Differential Amplifier

The current mirror load differential amplifier is not a good example for common mode analysis because the current mirror rejects the common mode signal.



$$\begin{bmatrix} \text{Total common mode Output due to } v_{ic} \end{bmatrix} = \begin{bmatrix} \text{Common mode output due to M1-M3-M4 path} \end{bmatrix} - \begin{bmatrix} \text{Common mode output due to M2 path} \end{bmatrix}$$

Therefore:

- The common mode output voltage should ideally be zero.
- Any voltage that exists at the output is due to mismatches in the gain between the two different paths.

DIFFERENTIAL AMPLIFIER WITH MOS DIODE LOADS

Small-Signal Analysis of the Common-Mode of the Differential Amplifier

The common-mode gain of the differential amplifier with a current mirror load is ideally zero.

To illustrate the common-mode gain, we need a different type of load so we will consider the following:

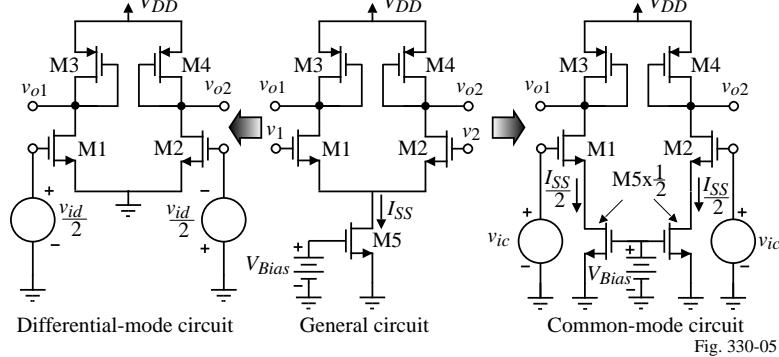


Fig. 330-05

Differential-Mode Analysis:

$$\frac{v_{o1}}{v_{id}} \approx -\frac{g_{m1}}{2g_{m3}} \quad \text{and} \quad \frac{v_{o2}}{v_{id}} \approx +\frac{g_{m2}}{2g_{m4}}$$

Note that these voltage gains are half of the active load inverter voltage gain.

Small-Signal Analysis of the Common-Mode of the Differential Amplifier – Cont'd

Common-Mode Analysis:

Assume that r_{ds1} is large and can be ignored (greatly simplifies the analysis).

$$\therefore v_{gs1} = v_{g1} - v_{s1} = v_{ic} - 2g_{m1}r_{ds5}v_{gs1}$$

Solving for v_{gs1} gives

$$v_{gs1} = \frac{v_{ic}}{1 + 2g_{m1}r_{ds5}}$$

The single-ended output voltage, v_{o1} , as a function of v_{ic} can be written as

$$\frac{v_{o1}}{v_{ic}} = -\frac{g_{m1}[r_{ds3}||(1/g_{m3})]}{1 + 2g_{m1}r_{ds5}} \approx -\frac{(g_{m1}/g_{m3})}{1 + 2g_{m1}r_{ds5}} \approx -\frac{g_{ds5}}{2g_{m3}}$$

Common-Mode Rejection Ratio (CMRR):

$$CMRR = \frac{|v_{o1}/v_{id}|}{|v_{o1}/v_{ic}|} = \frac{g_{m1}/2g_{m3}}{g_{ds5}/2g_{m3}} = g_{m1}r_{ds5}$$

How could you easily increase the CMRR of this differential amplifier?

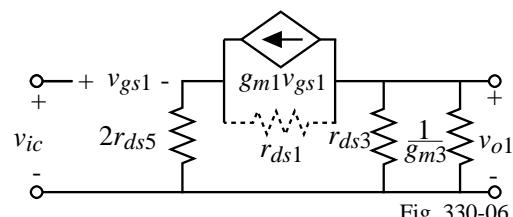
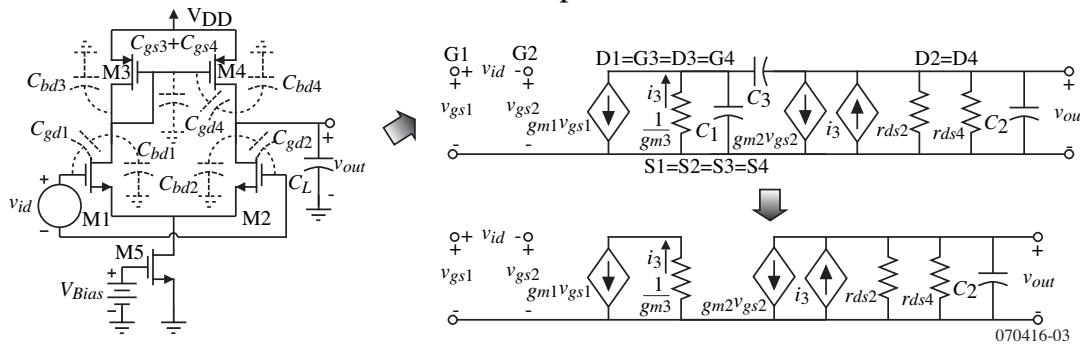


Fig. 330-06

Frequency Response of the Differential Amplifier

Back to the current mirror load differential amplifier:



Ignore the zeros that occur due to C_{gd1} , C_{gd2} and C_{gd4} .

$$C_1 = C_{gd1} + C_{bd1} + C_{bd3} + C_{gs3} + C_{gs4}, \quad C_2 = C_{bd2} + C_{bd4} + C_{gd2} + C_L \quad \text{and} \quad C_3 = C_{gd4}$$

If $gm_3/C_1 \gg (g_{ds2}+g_{ds4})/C_2$, then we can write

$$V_{out}(s) \approx \frac{gm_1}{g_{ds2} + g_{ds4}} \left(\frac{\omega_2}{s + \omega_2} \right) [V_{gs1}(s) - V_{gs2}(s)] \quad \text{where } \omega_2 \approx \frac{g_{ds2} + g_{ds4}}{C_2}$$

then the approximate frequency response of the differential amplifier reduces to

$$\frac{V_{out}(s)}{V_{id}(s)} \approx \left(\frac{gm_1}{g_{ds2} + g_{ds4}} \right) \left(\frac{\omega_2}{s + \omega_2} \right) \quad (\text{A more detailed analysis will be made in Lecture 220})$$

AN INTUITIVE METHOD OF SMALL SIGNAL ANALYSIS

Simplification of Small Signal Analysis

Small signal analysis is used so often in analog circuit design that it becomes desirable to find faster ways of performing this important analysis.

Intuitive Analysis (or Schematic Analysis)

Technique:

- 1.) Identify the transistor(s) that convert the input voltage to current (these transistors are called *transconductance transistors*).
- 2.) Trace the currents to where they flow into an equivalent resistance to ground.
- 3.) Multiply this resistance by the current to get the voltage at this node to ground.
- 4.) Repeat this process until the output is reached.

Simple Example:

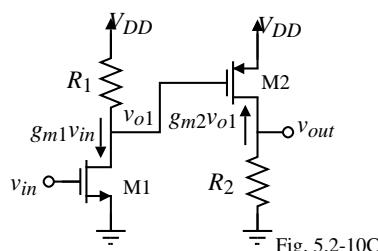


Fig. 5.2-10C

$$v_{o1} = -(gm_1 v_{in}) R_1 \rightarrow v_{out} = -(gm_2 v_{o1}) R_2 \rightarrow v_{out} = (gm_1 R_1 gm_2 R_2) v_{in}$$

Intuitive Analysis of the Current-Mirror Load Differential Amplifier

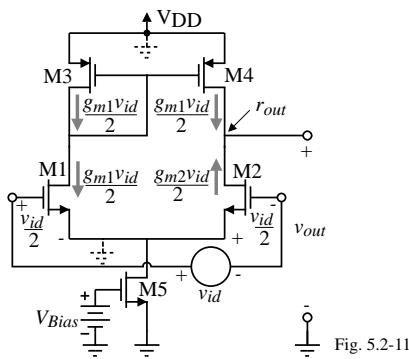


Fig. 5.2-11

- 1.) $i_1 = 0.5g_{m1}v_{id}$ and $i_2 = -0.5g_{m2}v_{id}$
- 2.) $i_3 = i_1 = 0.5g_{m1}v_{id}$
- 3.) $i_4 = i_3 = 0.5g_{m1}v_{id}$
- 4.) The resistance at the output node, r_{out} , is $r_{ds2}||r_{ds4}$ or $\frac{1}{g_{ds2} + g_{ds4}}$
- 5.) $\therefore v_{out} = (0.5g_{m1}v_{id} + 0.5g_{m2}v_{id})r_{out} = \frac{g_{m1}v_{in}}{g_{ds2} + g_{ds4}} = \frac{g_{m2}v_{in}}{g_{ds2} + g_{ds4}} \Rightarrow \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$

Some Concepts to Help Extend the Intuitive Method of Small-Signal Analysis

- 1.) Approximate the output resistance of any cascode circuit as $R_{out} \approx (g_{m2}r_{ds2})r_{ds1}$ where M1 is a transistor cascoded by M2.
- 2.) If there is a resistance, R , in series with the source of the transconductance transistor, let the effective transconductance be

$$g_{m(eff)} = \frac{g_m}{1+g_m R}$$

Proof:

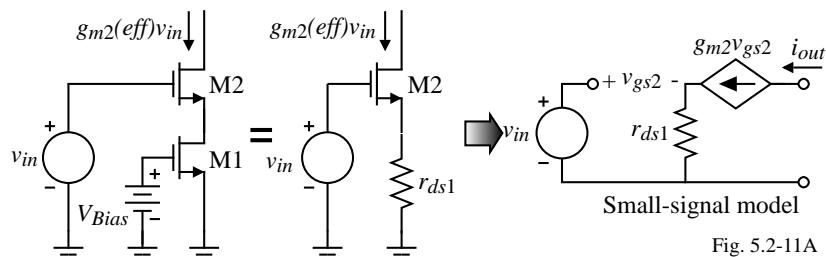


Fig. 5.2-11A

$$\therefore v_{gs2} = v_{g2} - v_{s2} = v_{in} - (g_{m2}r_{ds1})v_{gs2} \Rightarrow v_{gs2} = \frac{v_{in}}{1+g_{m2}r_{ds1}}$$

$$\text{Thus, } i_{out} = \frac{g_{m2}v_{in}}{1+g_{m2}r_{ds1}} = g_{m2}(eff) v_{in}$$

Noise Analysis of the Differential Amplifier

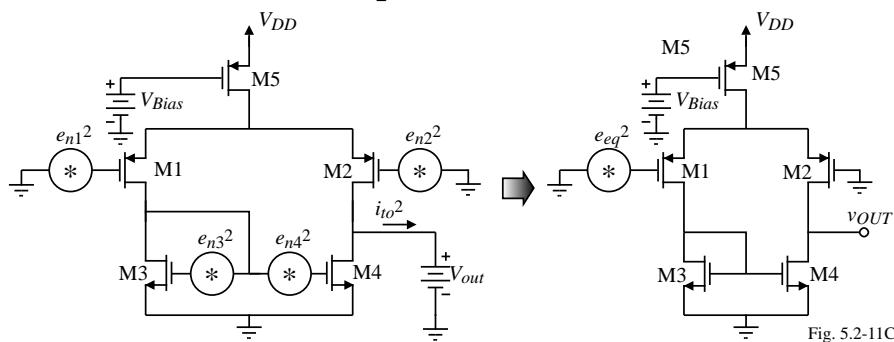


Fig. 5.2-11C

Solve for the total output-noise current to get,

$$i_{to}^2 = g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2$$

This output-noise current can be expressed in terms of an equivalent input noise voltage e_{eq}^2 , given as

$$i_{to}^2 = g_{m1}^2 e_{eq}^2$$

Equating the above two expressions for the total output-noise current gives,

$$e_{eq}^2 = e_{n1}^2 + e_{n2}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 [e_{n3}^2 + e_{n4}^2]$$

1/f Noise ($e_{n1}^2=e_{n2}^2$ and $e_{n3}^2=e_{n4}^2$):

$$e_{eq(1/f)} = \sqrt{\frac{2B_P}{fW_1L_1}} \sqrt{1 + \left(\frac{K'_N B_N}{K'_P B_P}\right) \left(\frac{L_1}{L_3}\right)^2}$$

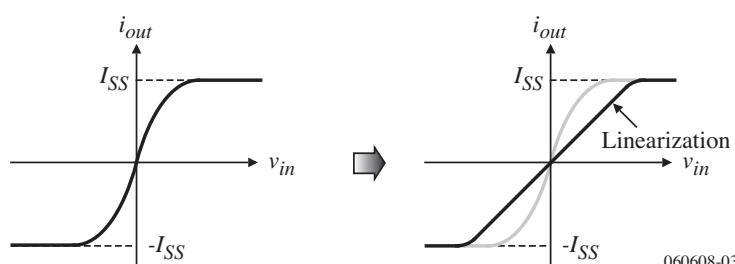
Thermal Noise ($e_{n1}^2=e_{n2}^2$ and $e_{n3}^2=e_{n4}^2$):

$$e_{eq(th)} = \sqrt{\frac{16kT}{3[2K'_1(W/L)_1 I_1]^{1/2}}} \left[1 + \left(\frac{W_3 L_1 K'_3}{L_3 W_1 K'_1}\right)^{1/2} \right]$$

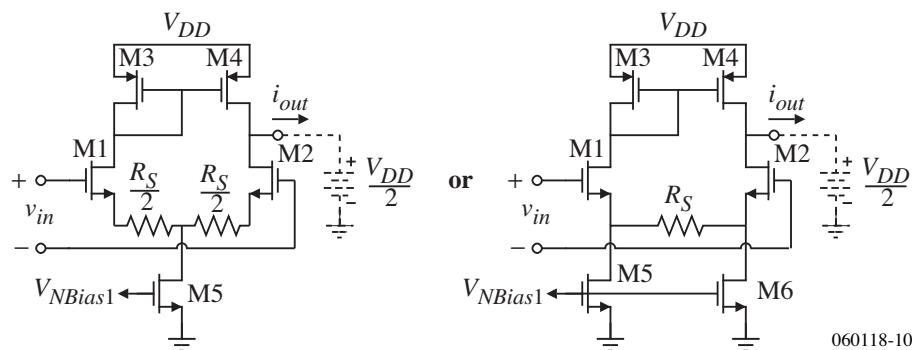
LARGE SIGNAL PERFORMANCE OF THE DIFFERENTIAL AMPLIFIER

Linearization of the Transconductance

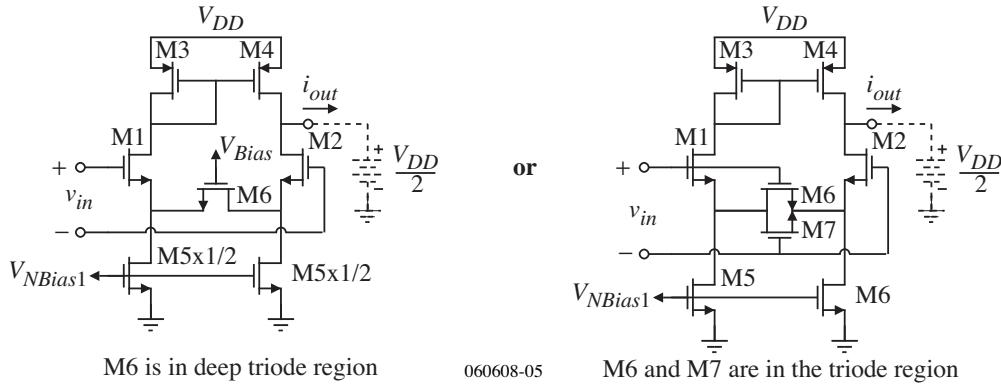
Goal:



Method (degeneration):



Linearization with Active Devices



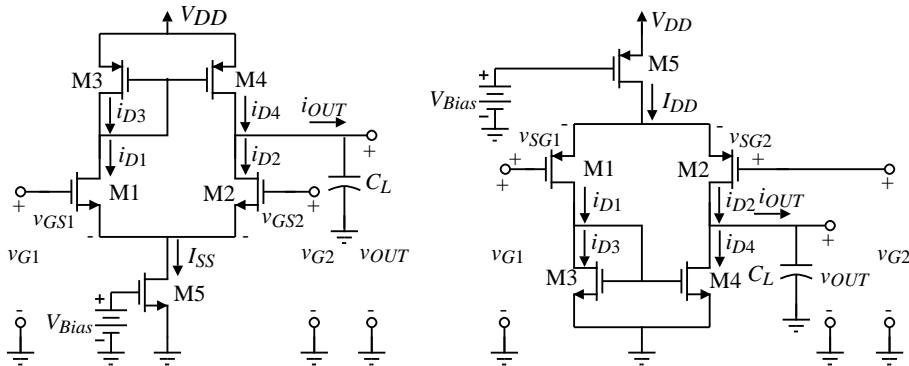
Note that these transconductors on this slide and the last can all have a varying transconductance by changing the value of I_{SS} .

Slew Rate of the Differential Amplifier

Slew Rate (SR) = Maximum output-voltage rate (either positive or negative)

It is caused by, $i_{OUT} = C_L \frac{dv_{OUT}}{dt}$. When i_{OUT} is a constant, the rate is a constant.

Consider the following current-mirror load, differential amplifiers:



Note that slew rate can only occur when the differential input signal is large enough to cause I_{SS} (I_{DD}) to flow through only one of the differential input transistors.

$$SR = \frac{I_{SS}}{C_L} = \frac{I_{DD}}{C_L} \Rightarrow \text{If } C_L = 5\text{pF} \text{ and } I_{SS} = 10\mu\text{A}, \text{ the slew rate is } SR = 2\text{V}/\mu\text{s.}$$

(For the BJT differential amplifier slewing occurs at $\pm 100\text{mV}$ whereas for the MOSFET differential amplifier it can be $\pm 2\text{V}$ or more.)

DIFFERENTIAL AMPLIFIERS WITH CURRENT SOURCE LOADS

Current-Source Load Differential Amplifier

Gives a truly balanced differential amplifier.

Also, the upper input common-mode range is extended.

However, a problem occurs if $I_1 \neq I_3$ or if $I_2 \neq I_4$.

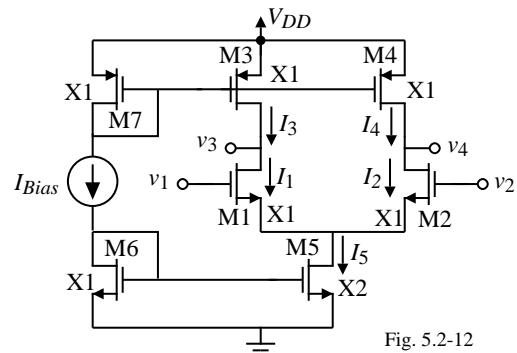


Fig. 5.2-12

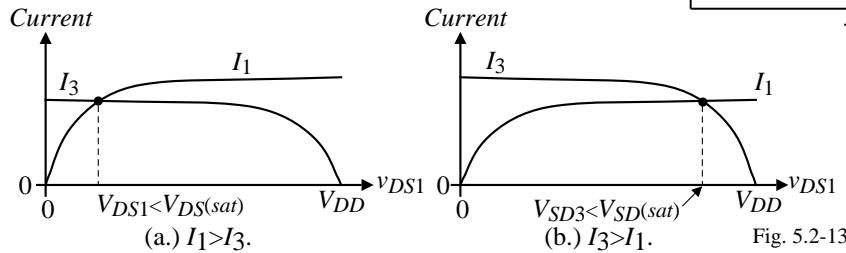


Fig. 5.2-13

A Differential-Output, Differential-Input Amplifier

Probably the best way to solve the current mismatch problem is through the use of common-mode feedback.

Consider the following solution to the previous problem.

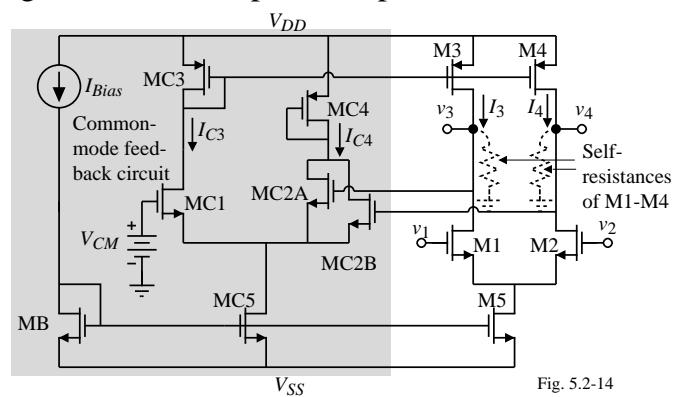


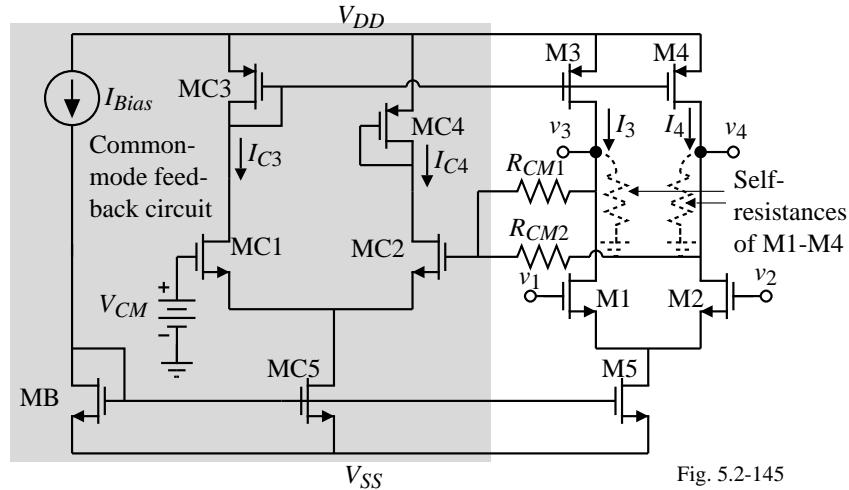
Fig. 5.2-14

Operation:

- Common mode output voltages are sensed at the gates of MC2A and MC2B and compared to V_{CM} .
- The current in MC3 provides the negative feedback to drive the common mode output voltage to the desired level.
- With large values of output voltage, this common mode feedback scheme has flaws.

Common-Mode Stabilization of the Diff.-Output, Diff.-Input Amplifier - Continued

The following circuit avoids the large differential output signal swing problems.



Note that R_{CM1} and R_{CM2} must not load the output of the differential amplifier.
(We will examine more CM feedback schemes in Lecture 280.)

DESIGN OF DIFFERENTIAL AMPLIFIERS

Design of a CMOS Differential Amplifier with a Current Mirror Load

Design Considerations:

<u>Constraints</u>	<u>Specifications</u>
Power supply	Small-signal gain
Technology	Frequency response (C_L)
Temperature	ICMR
	Slew rate (C_L)
	Power dissipation

Relationships

$$A_v = g_m R_{out}$$

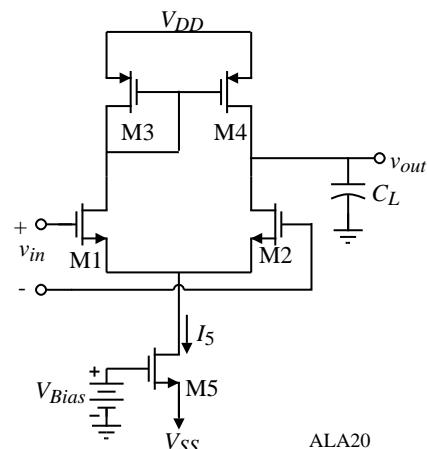
$$\omega_{-3dB} = 1/R_{out} C_L$$

$$V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1}$$

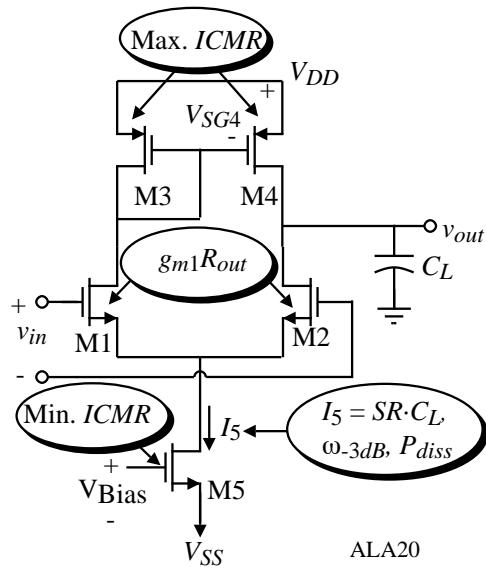
$$V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} = V_{SS} + V_{DS5}(\text{sat}) + V_{GS2}$$

$$SR = I_{SS}/C_L$$

$$P_{diss} = (V_{DD} + |V_{SS}|) \times (\text{All dc currents flowing from } V_{DD} \text{ or to } V_{SS})$$



Design of a CMOS Differential Amplifier with a Current Mirror Load - Continued



Schematic-wise, the design procedure is illustrated as shown:

Procedure:

- 1.) Pick I_{SS} to satisfy the slew rate knowing C_L or the power dissipation
- 2.) Check to see if R_{out} will satisfy the frequency response, if not change I_{SS} or modify circuit
- 3.) Design W_3/L_3 (W_4/L_4) to satisfy the upper ICMR
- 4.) Design W_1/L_1 (W_2/L_2) to satisfy the gain
- 5.) Design W_5/L_5 to satisfy the lower ICMR
- 6.) Iterate where necessary

Example 190-2 - Design of a MOS Differential Amp. with a Current Mirror Load

Design the currents and W/L values of the current mirror load MOS differential amplifier to satisfy the following specifications: $V_{DD} = -V_{SS} = 2.5V$, $SR \geq 10V/\mu s$ ($C_L=5pF$), $f_{-3dB} \geq 100kHz$ ($C_L=5pF$), a small signal gain of $100V/V$, $-1.5V \leq ICMR \leq 2V$ and $P_{diss} \leq 1mW$. Use the parameters of $K_N = 110\mu A/V^2$, $K_P = 50\mu A/V^2$, $V_{TN} = 0.7V$, $V_{TP} = -0.7V$, $\lambda_N = 0.04V^{-1}$ and $\lambda_P = 0.05V^{-1}$.

Solution

- 1.) To meet the slew rate, $I_{SS} \geq 50\mu A$. For maximum P_{diss} , $I_{SS} \leq 200\mu A$.
- 2.) f_{-3dB} of $100kHz$ implies that $R_{out} \leq 318k\Omega$. Therefore $R_{out} = \frac{2}{(\lambda_N + \lambda_P)I_{SS}} \leq 318k\Omega$
 $\therefore I_{SS} \geq 70\mu A$ Thus, pick $I_{SS} = 100\mu A$
- 3.) $V_{IC}(\max) = V_{DD} - V_{SG3} + V_{TN1} \rightarrow 2V = 2.5 - V_{SG3} + 0.7$
 $V_{SG3} = 1.2V = \sqrt{\frac{2 \cdot 50\mu A}{50\mu A/V^2(W_3/L_3)}} + 0.7$
 $\therefore \frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2}{(0.5)^2} = 8$
- 4.) $100 = g_{m1}R_{out} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{\sqrt{2 \cdot 110\mu A/V^2(W_1/L_1)}}{(0.04 + 0.05)\sqrt{50\mu A}} = 23.31 \sqrt{\frac{W_1}{L_1}} \rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = 18.4$

Example 190-2 - Continued

$$5.) V_{IC}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{GS1} \rightarrow -1.5 = -2.5 + V_{DS5}(\text{sat}) + \sqrt{\frac{2.50\mu\text{A}}{110\mu\text{A}/\text{V}^2(18.4)}} + 0.7$$

$$V_{DS5}(\text{sat}) = 0.3 - 0.222 = 0.0777 \Rightarrow \frac{W_5}{L_5} = \frac{2I_{SS}}{K_N' V_{DS5}(\text{sat})^2} = 150.6$$

We probably should increase W_1/L_1 to reduce V_{GS1} . If we choose $W_1/L_1 = 40$, then $V_{DS5}(\text{sat}) = 0.149\text{V}$ and $W_5/L_5 = 41$. (Larger than specified gain should be okay.)

SUMMARY

- Differential amplifiers are compatible with the matching properties of IC technology
- The differential amplifier has two modes of signal operation:
 - Differential mode
 - Common mode
- Differential amplifiers are excellent input stages for voltage amplifiers
- Differential amplifiers can have different loads including:
 - Current mirrors
 - MOS diodes
 - Current sources/sinks
 - Resistors
- The small signal performance of the differential amplifier is similar to the inverting amplifier in gain, output resistance and bandwidth
- The large signal performance includes slew rate and the linearization of the transconductance
- The design of CMOS analog circuits uses the relationships of the circuit to design the dc currents and the W/L ratios of each transistor

LECTURE 200 – LOW INPUT RESISTANCE AMPLIFIERS – THE COMMON GATE, CASCODE AND CURRENT AMPLIFIERS

LECTURE ORGANIZATION

Outline

- Voltage driven common gate amplifiers
- Voltage driven cascode amplifier
- Non-voltage driven cascode amplifier – the Miller effect
- Further considerations of cascode amplifiers
- Current amplifiers
- Summary

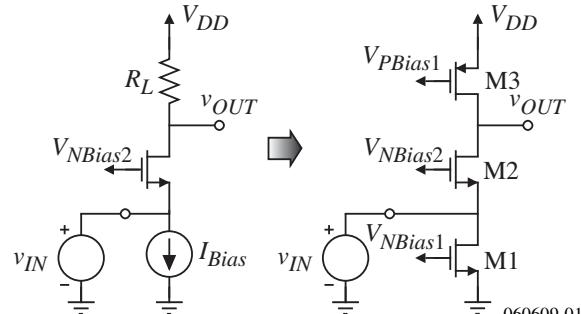
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 199-218

VOLTAGE-DRIVEN COMMON GATE AMPLIFIER

Common Gate Amplifier

Circuit:

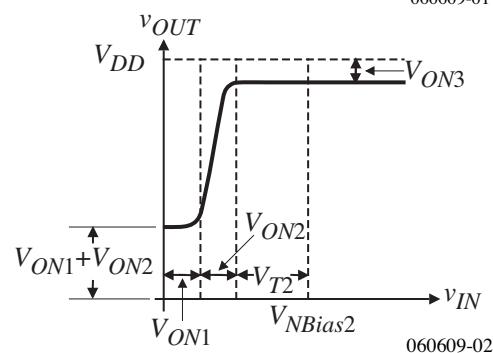


Large Signal Characteristics:

$$V_{OUT}(\max) \approx V_{DD} - V_{DS3}(\text{sat})$$

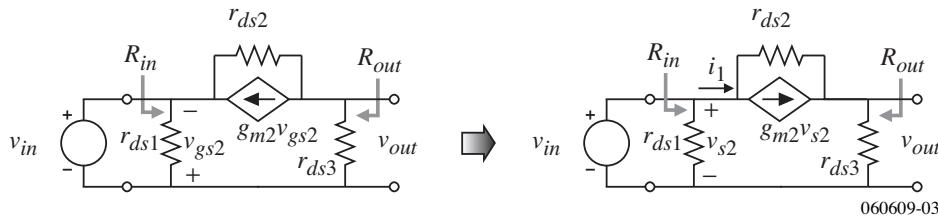
$$V_{OUT}(\min) \approx V_{DS1}(\text{sat}) + V_{DS2}(\text{sat})$$

Note $V_{DS1}(\text{sat}) = V_{ON1}$



Small Signal Performance of the Common Gate Amplifier

Small signal model:



$$v_{out} = g_{m2} v_{s2} \left(\frac{r_{ds2}}{r_{ds2} + r_{ds3}} \right) r_{ds3} = \left(\frac{g_{m2} r_{ds2} r_{ds3}}{r_{ds2} + r_{ds3}} \right) v_{in} \rightarrow A_v = \frac{v_{out}}{v_{in}} = + \frac{g_{m2} r_{ds2} r_{ds3}}{r_{ds2} + r_{ds3}}$$

$R_{in} = R_{in}' \| r_{ds1}$, R_{in}' is found as follows

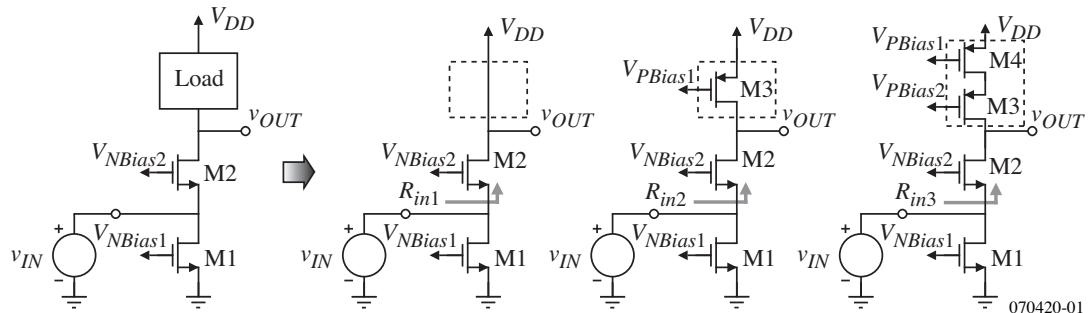
$$v_{s2} = (i_1 - g_{m2} v_{s2}) r_{ds2} + i_1 r_{ds3} = i_1 (r_{ds2} + r_{ds3}) - g_{m2} r_{ds2} v_{s2}$$

$$R_{in}' = \frac{v_{s2}}{i_1} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2} r_{ds2}} \rightarrow R_{in} = r_{ds1} \| \frac{r_{ds2} + r_{ds3}}{1 + g_{m2} r_{ds2}}$$

$$R_{out} \approx r_{ds2} \| r_{ds3}$$

Influence of the Load on the Input Resistance of a Common Gate Amplifier

Consider a common gate amplifier with a general load:



From the previous page, the input resistance to the common gate configuration is,

$$R_{in} = \frac{r_{ds2} + R_{Load}}{1 + g_{m2} r_{ds2}}$$

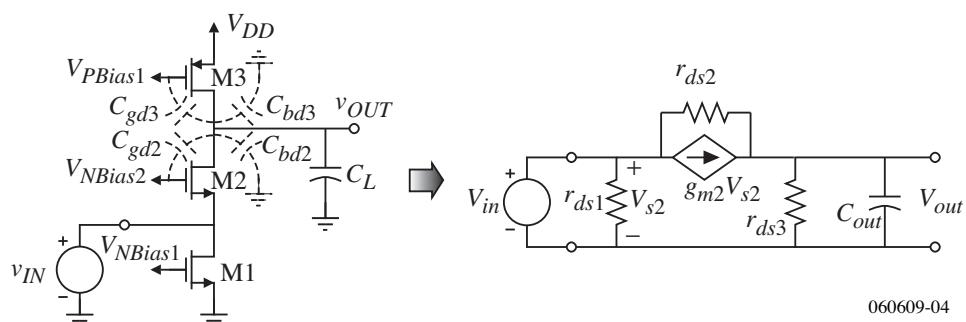
For the various loads shown, R_{in} becomes:

$$R_{in1} = \frac{r_{ds2}}{1 + g_{m2} r_{ds2}} \approx \frac{1}{g_{m2}} \quad R_{in2} = \frac{r_{ds2} + r_{ds3}}{1 + g_{m2} r_{ds2}} \approx \frac{2}{g_{m2}} \quad R_{in3} = \frac{r_{ds2} + r_{ds4} g_{m3} r_{ds3}}{1 + g_{m2} r_{ds2}} \approx r_{ds} !!!$$

.: The input resistance of the common gate configuration depends on the load at the drain

Frequency Response of the Common Gate Amplifier

Circuit:



The frequency response can be found by replacing r_{ds3} in the previous slide with,

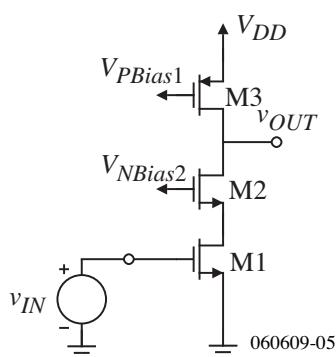
$$r_{ds3} \leftarrow \frac{r_{ds3}}{sr_{ds3}C_{out} + 1} \quad \text{where } C_{out} = C_{gd2} + C_{gd3} + C_{bd2} + C_{bd3} + C_L$$

$$A_v(s) = \frac{V_{out}}{V_{in}} = + \frac{g_m2r_{ds2}r_{ds3}}{r_{ds2}+r_{ds3}} \left(\frac{1}{s \frac{r_{ds2}r_{ds3}C_{out}}{r_{ds2}+r_{ds3}} + 1} \right) = + \frac{g_m2r_{ds2}r_{ds3}}{r_{ds2}+r_{ds3}} \left(\frac{1}{1 - \frac{s}{p_1}} \right)$$

where $p_1 = \frac{-1}{r_{ds2}r_{ds3}C_{out}}$ $\omega_{-3dB} = |p_1|$

VOLTAGE-DRIVEN CASCODE AMPLIFIER

Cascode[†] Amplifier



Advantages of the cascode amplifier:

- Increases the output resistance and gain (if M3 is cascaded also)
- Eliminates the Miller effect when the input source resistance is large

[†] "Cascode" = "Cascaded triode" see H. Wallman, A.B. Macnee, and C.P. Gadsden, "A Low-Noise Amplifier, Proc. IRE, vol. 36, pp. 700-708, June 1948.

Large-Signal Characteristics of the Cascode Amplifier

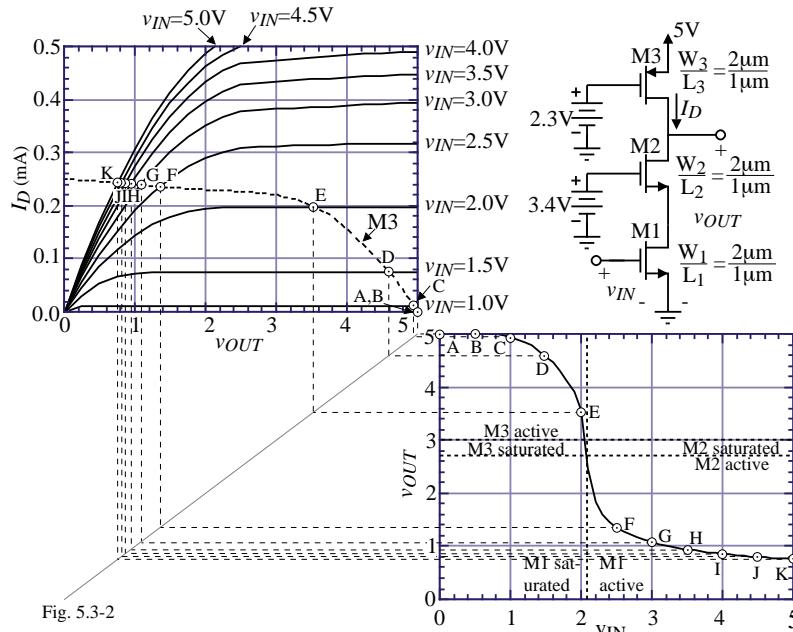


Fig. 5.3-2

M1 sat. when $V_{GG2} - V_{GS2} \geq V_{GS1} - V_T \rightarrow v_{IN} \leq 0.5(V_{GG2} + V_{TN})$ where $V_{GS1} = V_{GS2}$
 M2 sat. when $V_{DS1} \geq V_{GS2} - V_{TN} \rightarrow v_{OUT} - V_{DS1} \geq V_{GG2} - V_{DS1} - V_{TN} \rightarrow v_{OUT} \geq V_{GG2} - V_{TN}$
 M3 is saturated when $V_{DD} - v_{OUT} \geq V_{DD} - V_{GG3} - |V_{TP}| \rightarrow v_{OUT} \leq V_{GG3} + |V_{TP}|$

Large-Signal Voltage Swing Limits of the Cascode Amplifier

Maximum output voltage, $v_{OUT(max)}$:

$$v_{OUT(max)} = V_{DD}$$

Minimum output voltage, $v_{OUT(min)}$:

Referencing all potentials to the negative power supply (ground in this case), we may express the current through each of the devices, M1 through M3, as

$$\begin{aligned} i_{D1} &= \beta_1 \left((V_{DD} - V_{T1})v_{DS1} - \frac{v_{DS1}^2}{2} \right) \approx \beta_1(V_{DD} - V_{T1})v_{DS1} \\ i_{D2} &= \beta_2 \left((V_{GG2} - v_{DS1} - V_{T2})(v_{OUT} - v_{DS1}) - \frac{(v_{OUT} - v_{DS1})^2}{2} \right) \\ &\approx \beta_2(V_{GG2} - v_{DS1} - V_{T2})(v_{OUT} - v_{DS1}) \end{aligned}$$

and

$$i_{D3} = \frac{\beta_3}{2} (V_{DD} - V_{GG3} - |V_{T3}|)^2$$

where we have also assumed that both v_{DS1} and v_{OUT} are small, and $v_{IN} = V_{DD}$.

Solving for v_{OUT} by realizing that $i_{D1} = i_{D2} = i_{D3}$ and $\beta_1 = \beta_2$ we get,

$$v_{OUT(min)} = \frac{\beta_3}{2\beta_2} (V_{DD} - V_{GG3} - |V_{T3}|)^2 \left(\frac{1}{V_{GG2} - V_{T2}} + \frac{1}{V_{DD} - V_{T1}} \right)$$

Small-Signal Midband Performance of the Cascode Amplifier

Small-signal model:

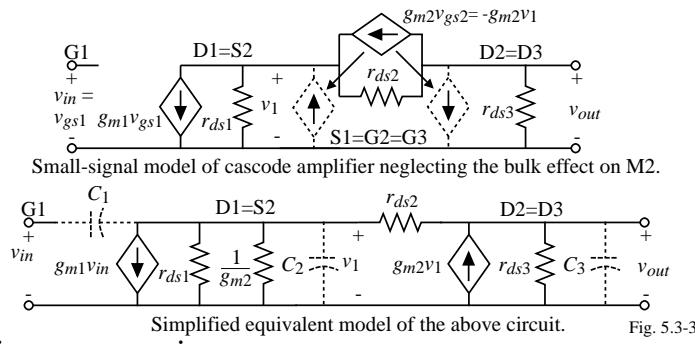


Fig. 5.3-3

Using nodal analysis, we can write,

$$\begin{aligned} [g_{ds1} + g_{ds2} + g_{m2}]v_1 - g_{ds2}v_{out} &= -g_{m1}v_{in} \\ -[g_{ds2} + g_{m2}]v_1 + (g_{ds2} + g_{ds3})v_{out} &= 0 \end{aligned}$$

Solving for v_{out}/v_{in} yields

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds3}g_{m2}} \cong \frac{-g_{m1}}{g_{ds3}} = -\sqrt{\frac{2K'_1W_1}{L_1I_D\lambda^2_3}}$$

(Intuitive analysis give the same result with much less effort.)

The small-signal output resistance is,

$$r_{out} = [r_{ds1} + r_{ds2} + g_{m2}r_{ds1}r_{ds2}] \parallel r_{ds3} \cong r_{ds3}$$

Frequency Response of the Cascode Amplifier

Small-signal model ($R_S = 0$):

where

$$C_1 = C_{gd1},$$

$$C_2 = C_{bd1} + C_{bs2} + C_{gs2}, \text{ and}$$

$$C_3 = C_{bd2} + C_{bd3} + C_{gd2} + C_{gd3} + C_L$$

The nodal equations now become:

$$(g_{m2} + g_{ds1} + g_{ds2} + sC_1 + sC_2)v_1 - g_{ds2}v_{out} = -(g_{m1} - sC_1)v_{in}$$

$$\text{and } -(g_{ds2} + g_{m2})v_1 + (g_{ds2} + g_{ds3} + sC_3)v_{out} = 0$$

Solving for $V_{out}(s)/V_{in}(s)$ gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{1}{1 + as + bs^2} \right) \left(\frac{-(g_{m1} - sC_1)(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})} \right)$$

where

$$a = \frac{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}$$

and

$$b = \frac{C_3(C_1 + C_2)}{g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})}$$

A Simplified Method of Finding an Algebraic Expression for the Two Poles

Assume that a general second-order polynomial can be written as:

$$P(s) = 1 + as + bs^2 = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2}$$

Now if $|p_2| \gg |p_1|$, then $P(s)$ can be simplified as

$$P(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}$$

Therefore we may write p_1 and p_2 in terms of a and b as

$$p_1 = \frac{-1}{a} \text{ and } p_2 = \frac{-a}{b}$$

Applying this to the previous problem gives,

$$p_1 = \frac{-[g_{ds1}g_{ds2} + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2})]}{C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})} \approx \frac{-g_{ds3}}{C_3}$$

The nondominant root p_2 is given as

$$p_2 = \frac{-[C_3(g_{ds1} + g_{ds2} + g_{m2}) + C_2(g_{ds2} + g_{ds3}) + C_1(g_{ds2} + g_{ds3})]}{C_3(C_1 + C_2)} \approx \frac{-g_{m2}}{C_1 + C_2}$$

Assuming C_1 , C_2 , and C_3 are the same order of magnitude, and g_{m2} is greater than g_{ds3} , then $|p_1|$ is smaller than $|p_2|$. Therefore the approximation of $|p_2| \gg |p_1|$ is valid.

Note that there is a right-half plane zero at $z_1 = g_{m1}/C_1$.

NON-VOLTAGE DRIVEN CASCODE AMPLIFIER – THE MILLER EFFECT Miller Effect

Consider the following inverting amplifier:

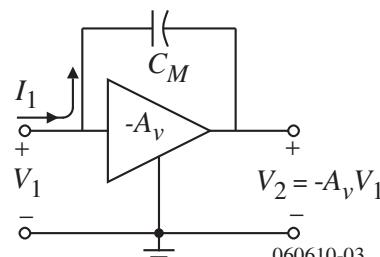
Solve for the input impedance:

$$Z_{in}(s) = \frac{V_1}{I_1}$$

$$I_1 = sC_M(V_1 - V_2) = sC_M(V_1 + A_v V_1) = sC_M(1 + A_v)V_1$$

Therefore,

$$Z_{in}(s) = \frac{V_1}{I_1} = \frac{V_1}{sC_M(1 + A_v)V_1} = \frac{1}{sC_M(1 + A_v)} = \frac{1}{sC_{eq}}$$



The Miller effect can take $C_{gd} = 5\text{fF}$ and make it look like a 0.5pF capacitor in parallel with the input of the inverting amplifier ($A_v \approx -100$).

If the source resistance is large, this creates a dominant pole at the input.

Simple Inverting Amplifier Driven with a High Source Resistance

Examine the frequency response of a current-source load inverter driven from a high resistance source:

Assuming the input is I_{in} , the nodal equations are,

$$[G_1 + s(C_1 + C_2)]V_1 - sC_2V_{out} = I_{in} \quad \text{and} \quad (g_{m1} - sC_2)V_1 + [G_3 + s(C_2 + C_3)]V_{out} = 0$$

where

$$G_1 = G_s (=1/R_s), \quad G_3 = g_{ds1} + g_{ds2}, \quad C_1 = C_{gs1}, \quad C_2 = C_{gd1} \quad \text{and} \quad C_3 = C_{bd1} + C_{bd2} + C_{gd2}.$$

Solving for $V_{out}(s)/V_{in}(s)$ gives

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(sC_2 - g_{m1})G_1}{G_1G_3 + s[G_3(C_1 + C_2) + G_1(C_2 + C_3) + g_{m1}C_2] + (C_1C_2 + C_1C_3 + C_2C_3)s^2} \quad \text{or,}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{-g_{m1}}{G_3} \right) \frac{[1 - s(C_2/g_{m1})]}{1 + [R_1(C_1 + C_2) + R_3(C_2 + C_3) + g_{m1}R_1R_3C_2]s + (C_1C_2 + C_1C_3 + C_2C_3)R_1R_3s^2}$$

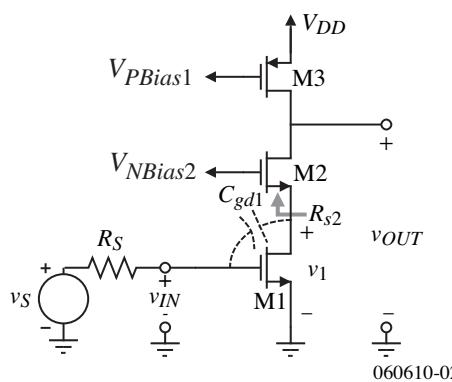
Assuming that the poles are split allows the use of the previous technique to get,

$$p_1 = \frac{-1}{R_1(C_1 + C_2) + R_3(C_2 + C_3) + g_{m1}R_1R_3C_2} \approx \frac{-1}{g_{m1}R_1R_3C_2} \quad \text{and} \quad p_2 \approx \frac{-g_{m1}C_2}{C_1C_2 + C_1C_3 + C_2C_3}$$

The Miller effect has caused the input pole, $1/R_1C_1$, to be decreased by a value of $g_{m1}R_3$.

How Does the Cascode Amplifier Solve the Miller Effect?

Cascode amplifier:



The Miller effect causes C_{gs1} to be increased by the value of $1 + (v_1/v_{in})$ and appear in parallel with the gate-source of M1 causing a dominant pole to occur.

The cascode amplifier eliminates this problem by keeping the value of v_1/v_{in} small by making the value of R_{s2} approximately $2/g_{m2}$.

Comparison of the Inverting and Cascode Non-Voltage Driven Amplifiers

The dominant pole of the inverting amplifier with a large source resistance was found to be

$$p_1(\text{inverter}) = \frac{-1}{R_1(C_1+C_2)+R_3(C_2+C_3)+g_{m1}R_1R_3C_2} \approx \frac{-1}{g_{m1}R_1R_3C_2}$$

Now if a cascode amplifier is used, R_3 , can be approximated as $2/g_m$ of the cascoding transistor (assuming the drain sees an r_{ds} to ac ground).

$$\therefore p_1(\text{cascode}) = \frac{-1}{R_1(C_1+C_2) + \left(\frac{2}{g_m}\right)(C_2+C_3) + g_{m1}R_1\left(\frac{2}{g_m}\right)C_2}$$

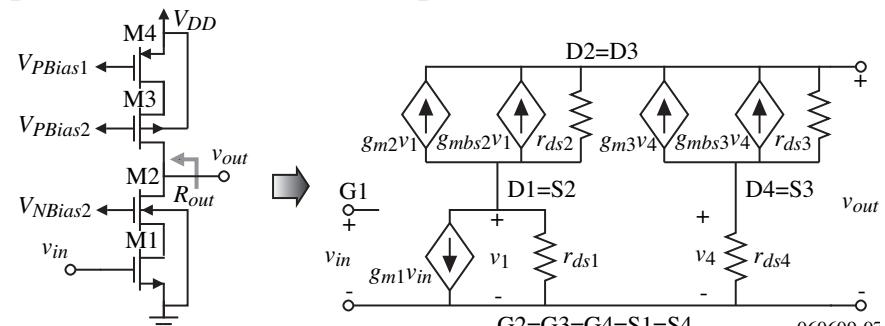
$$= \frac{-1}{R_1(C_1+C_2) + \left(\frac{2}{g_m}\right)(C_2+C_3) + 2R_1C_2} \approx \frac{-1}{R_1(C_1+3C_2)}$$

Thus we see that $p_1(\text{cascode}) \gg p_1(\text{inverter})$.

FURTHER CONSIDERATIONS OF CASCODE AMPLIFIERS

High Gain and High Output Resistance Cascode Amplifier

If the load of the cascode amplifier is a cascode current source, then both high output resistance and high voltage gain is achieved.



The output resistance is,

$$r_{out} \cong [g_{m2}r_{ds1}r_{ds2}] \parallel [g_{m3}r_{ds3}r_{ds4}] = \frac{I_D^{-1.5}}{\frac{\lambda_1\lambda_2}{\sqrt{2K_2(W/L)_2}} + \frac{\lambda_3\lambda_4}{\sqrt{2K_3(W/L)_3}}}$$

Knowing r_{out} , the gain is simply

$$A_v = -g_{m1}r_{out} \cong -g_{m1}\{[g_{m2}r_{ds1}r_{ds2}] \mid [g_{m3}r_{ds3}r_{ds4}]\} \cong \frac{\sqrt{2K_1(W/L)_1}I_D^{-1}}{\frac{\lambda_1\lambda_2}{\sqrt{2K_2(W/L)_2}} + \frac{\lambda_3\lambda_4}{\sqrt{2K_3(W/L)_3}}}$$

Example 200-1 - Comparison of the Cascode Amplifier Performance

Calculate the small-signal voltage gain, output resistance, the dominant pole, and the nondominant pole for the low-gain, cascode amplifier and the high-gain, cascode amplifier. Assume that $I_D = 200$ microamperes, that all W/L ratios are $2\mu\text{m}/1\mu\text{m}$, and that the parameters of Table 3.1-2 are valid. The capacitors are assumed to be: $C_{gd} = 3.5$ fF, $C_{gs} = 30$ fF, $C_{bsn} = C_{bdn} = 24$ fF, $C_{bsp} = C_{bdp} = 12$ fF, and $C_L = 1$ pF.

Solution

The low-gain, cascode amplifier has the following small-signal performance:

$$A_V = -37.1 \text{V/V}$$

$$R_{out} = 125 \text{k}\Omega$$

$$p_1 \approx -g_{ds3}/C_3 \rightarrow 1.22 \text{ MHz}$$

$$p_2 \approx g_{m2}/(C_1+C_2) \rightarrow 605 \text{ MHz.}$$

The high-gain, cascode amplifier has the following small-signal performance:

$$A_V = -414 \text{V/V}$$

$$R_{out} = 1.40 \text{ M}\Omega$$

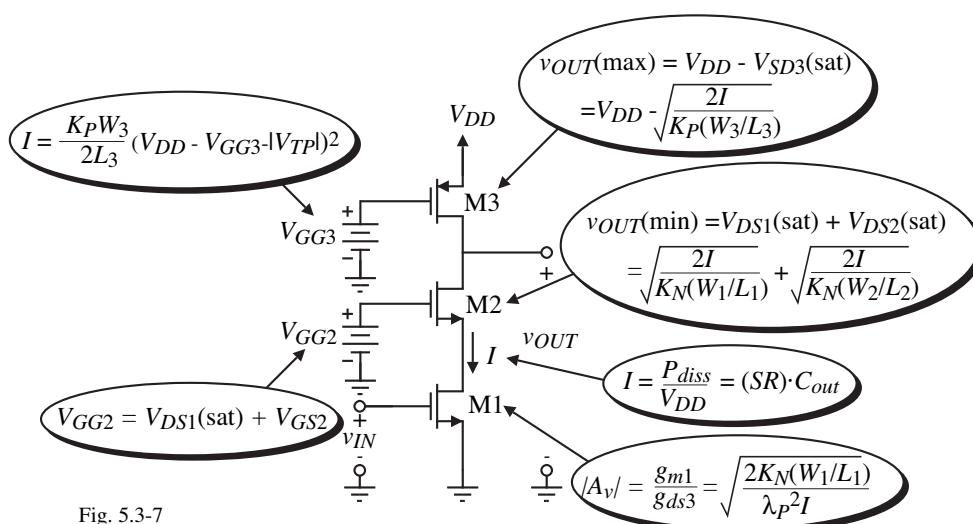
$$p_1 \approx 1/R_{out}C_3 \rightarrow 108 \text{ kHz}$$

$$p_2 \approx g_{m2}/(C_1+C_2) \rightarrow 579 \text{ MHz}$$

(Note at this frequency, the drain of M2 is shorted to ground by the load capacitance, C_L)

Designing Cascode Amplifiers

Pertinent design equations for the simple cascode amplifier.



Example 200-2 - Design of a Cascode Amplifier

The specs for a cascode amplifier are $A_v = -50V/V$, $v_{OUT}(\max) = 4V$, $v_{OUT}(\min) = 1.5V$, $V_{DD}=5V$, and $P_{diss}=1mW$. The slew rate with a $10pF$ load should be $10V/\mu s$ or greater.

Solution

The slew rate requires a current greater than $100\mu A$ while the power dissipation requires a current less than $200\mu A$. Compromise with $150\mu A$. Beginning with M3,

$$\frac{W_3}{L_3} = \frac{2I}{K_P[V_{DD}-v_{OUT}(\max)]^2} = \frac{2 \cdot 150}{50(1)^2} = 6$$

From this find V_{GG3} : $V_{GG3} = V_{DD} - |V_{TP}| - \sqrt{\frac{2I}{K_P(W_3/L_3)}} = 5 - 1 - \sqrt{\frac{2 \cdot 150}{50 \cdot 6}} = 3V$

Next, $\frac{W_1}{L_1} = \frac{(A_v\lambda)^2 I}{2K_N} = \frac{(50 \cdot 0.05)^2 (150)}{2 \cdot 110} = 2.73$

To design W_2/L_2 , we will first calculate $V_{DS1}(\text{sat})$ and use the $v_{OUT}(\min)$ specification to

define $V_{DS2}(\text{sat})$. $V_{DS1}(\text{sat}) = \sqrt{\frac{2I}{K_N(W_1/L_1)}} = \sqrt{\frac{2 \cdot 150}{110 \cdot 4.26}} = 0.8V$

Subtracting this value from $1.5V$ gives $V_{DS2}(\text{sat}) = 0.7V$.

$$\therefore \frac{W_2}{L_2} = \frac{2I}{K_N V_{DS2}(\text{sat})^2} = \frac{2 \cdot 150}{110 \cdot 0.72} = 5.57$$

Finally, $V_{GG2} = V_{DS1}(\text{sat}) + \sqrt{\frac{2I}{K_N(W_2/L_2)}} + V_{TN} = 0.8V + 0.7V + 0.7V = 2.2V$

CURRENT AMPLIFIERS

What is a Current Amplifier?

- An amplifier that has a defined output-input current relationship
- Low input resistance
- High output resistance

Application of current amplifiers:

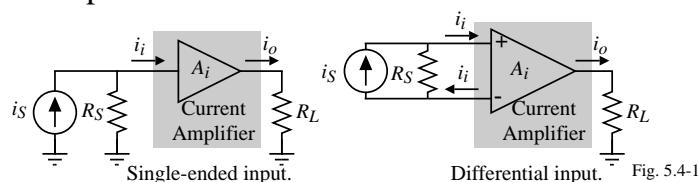


Fig. 5.4-1

$$R_S \gg R_{in} \quad \text{and} \quad R_{out} \gg R_L$$

Advantages of current amplifiers:

- Currents are not restricted by the power supply voltages so that wider dynamic ranges are possible with lower power supply voltages.
- -3dB bandwidth of a current amplifier using negative feedback is independent of the closed loop gain.

Frequency Response of a Current Amplifier with Current Feedback

Consider the following current amplifier with resistive negative feedback applied.

Assuming that the small-signal resistance looking into the current amplifier is much less than R_1 or R_2 ,

$$i_o = A_i(i_1 - i_2) = A_i \left(\frac{v_{in}}{R_1} - i_o \right)$$

Solving for i_o gives

$$i_o = \left(\frac{A_i}{1+A_i} \right) \frac{v_{in}}{R_1} \rightarrow v_{out} = R_2 i_o = \frac{R_2}{R_1} \left(\frac{A_i}{1+A_i} \right) v_{in}$$

If $A_i(s) = \frac{A_o}{\frac{s}{\omega_A} + 1}$, then

$$\frac{v_{out}}{v_{in}} = \frac{R_2}{R_1} \left(\frac{1}{1 + \frac{1}{1+A_o}} \right) = \frac{R_2}{R_1} \left(\frac{A_o}{\frac{s}{\omega_A} + (1+A_o)} \right) = \frac{R_2}{R_1} \left(\frac{A_o}{1+A_o} \right) \left(\frac{1}{\frac{s}{\omega_A(1+A_o)} + 1} \right)$$

$$\therefore \omega_{-3dB} = \omega_A(1+A_o)$$

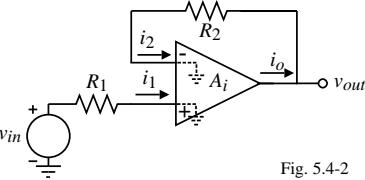


Fig. 5.4-2

Bandwidth Advantage of a Current Feedback Amplifier

The unity-gainbandwidth is,

$$GB = |A_v(0)| \omega_{-3dB} = \frac{R_2 A_o}{R_1 (1+A_o)} \cdot \omega_A (1+A_o) = \frac{R_2}{R_1} A_o \cdot \omega_A = \frac{R_2}{R_1} GB_i$$

where GB_i is the unity-gainbandwidth of the current amplifier.

Note that if GB_i is constant, then increasing R_2/R_1 (the voltage gain) increases GB .

Illustration:

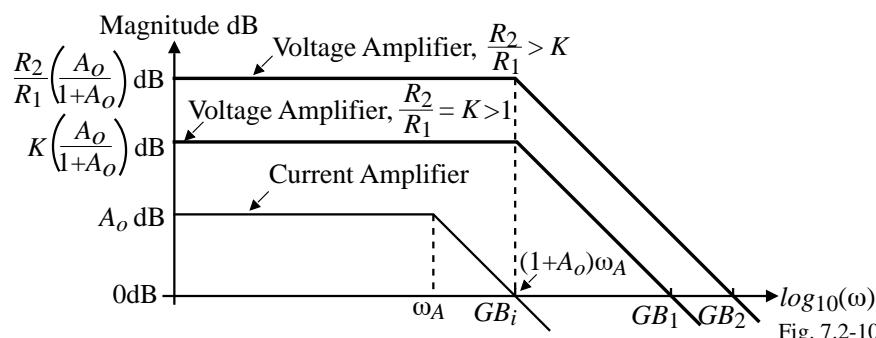
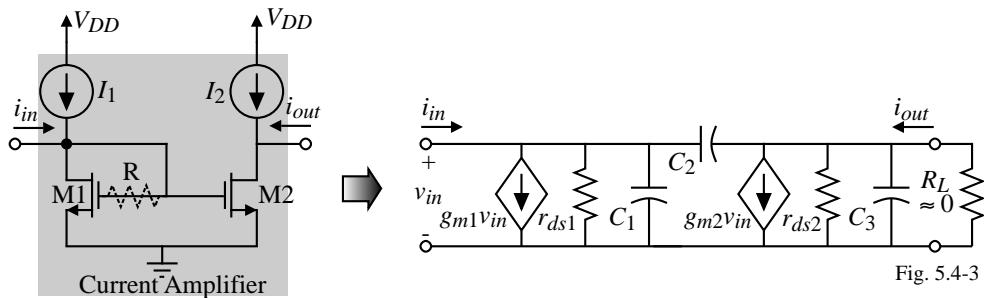


Fig. 7.2-10

Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the GB of the voltage amplifier realizing the voltage buffer is greater than the GB achieved from the above method.

Current Amplifier using the Simple Current Mirror



$$R_{in} = \frac{1}{g_{m1}} \quad R_{out} = \frac{1}{\lambda_1 I_o} \quad \text{and} \quad A_i = \frac{W_2/L_2}{W_1/L_1}.$$

Frequency response:

$$P_1 = \frac{-(g_{m1} + g_{ds1})}{C_1 + C_2} = \frac{-(g_{m1} + g_{ds1})}{C_{bd1} + C_{gs1} + C_{gs2} + C_{gd2}} \approx \frac{-g_{m1}}{C_{bd1} + C_{gs1} + C_{gs2} + C_{gd2}}$$

Note that the bandwidth can be almost doubled by including the resistor, R .

(R removes C_{gs1} from P_1)

Example 200-3 - Performance of a Simple Current Mirror as a Current Amplifier

Find the small-signal current gain, A_i , the input resistance, R_{in} , the output resistance R_{out} , and the -3dB frequency in Hertz for the current amplifier of previous slide if $10I_1 = I_2 = 100\mu\text{A}$ and $W_2/L_2 = 10W_1/L_1 = 10\mu\text{m}/1\mu\text{m}$. Assume that $C_{bd1} = 10\text{fF}$, $C_{gs1} = C_{gs2} = 100\text{fF}$, and $C_{gd2} = 50\text{fF}$.

Solution

Ignoring channel modulation and mismatch effects, the small-signal current gain,

$$A_i = \frac{W_2/L_2}{W_1/L_1} \approx 10\text{A/A.}$$

The small-signal input resistance, R_{in} , is approximately $1/g_{m1}$ and is

$$R_{in} \approx \frac{1}{\sqrt{2K_N(1/1)10\mu\text{A}}} = \frac{1}{46.9\mu\text{S}} = 21.3\text{k}\Omega$$

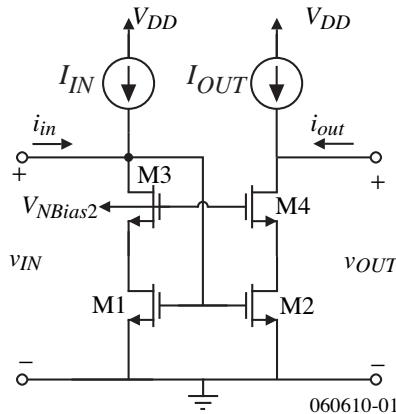
The small-signal output resistance is equal to

$$R_{out} = \frac{1}{\lambda_N I_2} = 250\text{k}\Omega.$$

The -3dB frequency is

$$\omega_{-3\text{dB}} = \frac{46.9\mu\text{S}}{260\text{fF}} = 180.4 \times 10^6 \text{ radians/sec.} \rightarrow f_{-3\text{dB}} = 28.7 \text{ MHz}$$

Wide-Swing, Cascode Current Mirror Implementation of a Current Amplifier



$$R_{in} \approx \frac{1}{g_m 1}, \quad R_{out} \approx r_{ds2} g_m 4 r_{ds4}, \quad \text{and} \quad A_i = \frac{W_2/L_2}{W_1/L_1}$$

Example 200-4 - Current Amplifier Implemented by the Wide-Swing, Cascode Current Mirror

Assume that I_{IN} and I_{OUT} of the wide-swing cascode current mirror are $100\mu\text{A}$. Find the value of R_{in} , R_{out} , and A_i if the W/L ratios of all transistors are $182\mu\text{m}/1\mu\text{m}$.

Solution

The input resistance requires $g_m 1$ which is $\sqrt{2 \cdot 110 \cdot 182 \cdot 100} = 2\text{mS}$

$$\therefore R_{in} \approx 500\Omega$$

From our knowledge of the cascode configuration, the small-signal output resistance should be

$$R_{out} \approx g_m 4 r_{ds4} r_{ds2} = (2001\mu\text{S})(250\text{k}\Omega)(250\text{k}\Omega) = 125\text{M}\Omega$$

Because $V_{DS1} = V_{DS2}$, the small-signal current gain is

$$A_i = \frac{W_2/L_2}{W_1/L_1} = 1$$

Simulation results using the level 1 model for this example give

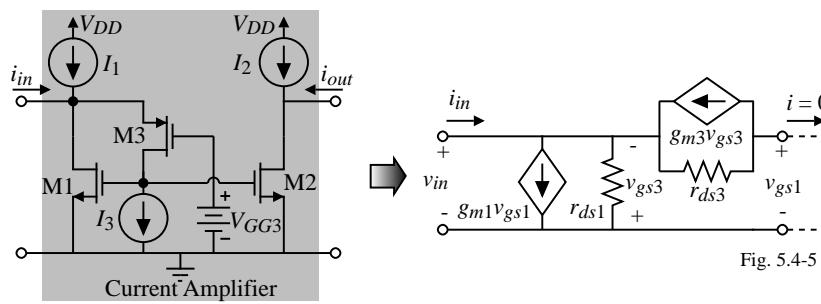
$$R_{in} = 497\Omega, \quad R_{out} = 164.7\text{M}\Omega \quad \text{and} \quad A_i = 1.000 \text{ A/A.}$$

The value of V_{ON} for all transistors is

$$V_{ON} = \sqrt{\frac{2 \cdot 100\mu\text{A}}{110\mu\text{A/V}^2 \cdot 182}} = 0.1\text{V}$$

Low-Input Resistance Current Amplifier

To decrease R_{in} below $1/g_m$ requires the use of negative shunt feedback. Consider the following example.



Feedback concept:

Input resistance without feedback $\approx r_{ds1}$.

$$\text{Loop gain} \approx \frac{(g_m 1)(g_m 3)}{(g_{ds1})(g_{ds3})} \quad \text{assuming that the resistances of } I_1 \text{ and } I_3 \text{ are very large.}$$

$$\therefore R_{in} = \frac{R_{in}(\text{no fb.})}{1 + \text{Loop gain}} \approx \frac{r_{ds1}}{g_m 1 r_{ds1} g_m 3 r_{ds3}} = \frac{1}{g_m 1 g_m 3 r_{ds3}}$$

Small signal analysis:

$$i_{in} = g_m 1 v_{gs1} - g_{ds1} v_{gs3}$$

$$\text{and } v_{gs3} = -v_{in} \quad v_{gs1} = v_{in} - (g_m 3 v_{gs3} r_{ds3}) = v_{in}(1 + g_m 3 r_{ds3})$$

$$\therefore i_{in} = g_m 1(1 + g_m 3 r_{ds3}) v_{in} + g_{ds1} v_{in} \approx g_m 1 g_m 3 r_{ds3} v_{in} \Rightarrow R_{in} \approx \frac{1}{g_m 1 g_m 3 r_{ds3}}$$

Use of Blackman's Formula to Find the Input Resistance of Previous Slide

Recall that the resistance seen looking into port X is given as,

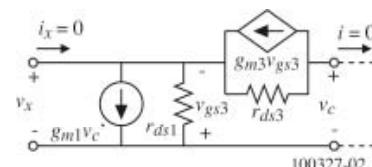
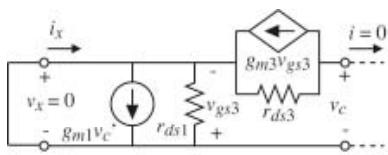
$$R_X = R_X(k=0) \left[\frac{1 + RR(\text{port shorted})}{1 + RR(\text{port opened})} \right]$$

The small signal circuit (from the previous slide) is,

Choosing $g_m 1$ as k , we see that,

$$R_X(k=0) = r_{ds1}$$

The circuits for calculating the shorted and open return-ratios are:



$$RR(v_x = 0): -\frac{v_c}{v_c} = 0 \quad RR(i_x = 0): v_c = -v_{gs3}(1 + g_m 3 r_{ds3}) = -g_m 1 r_{ds1} (1 + g_m 3 r_{ds3}) v_c$$

$$\therefore RR(i_x = 0) = -\frac{v_c}{v_c} = g_m 1 r_{ds1} (1 + g_m 3 r_{ds3})$$

Finally,

$$R_X = R_{in} = r_{ds1} \frac{1 + 0}{1 + g_m 1 r_{ds1} (1 + g_m 3 r_{ds3})} \approx \frac{1}{g_m 1 g_m 3 r_{ds3}}$$

Differential-Input, Current Amplifiers

Definitions for the differential-mode, i_{ID} , and common-mode, i_{IC} , input currents of the differential-input current amplifier.

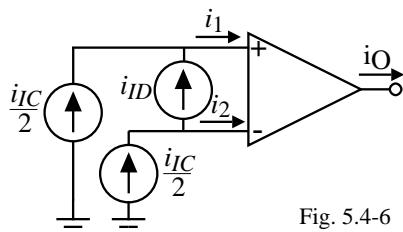


Fig. 5.4-6

$$i_o = A_{ID}i_{ID} \pm A_{IC}i_{IC} = A_{ID}(i_1 - i_2) \pm A_{IC}\left(\frac{i_1 + i_2}{2}\right)$$

Implementations:

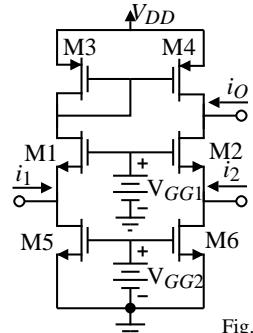
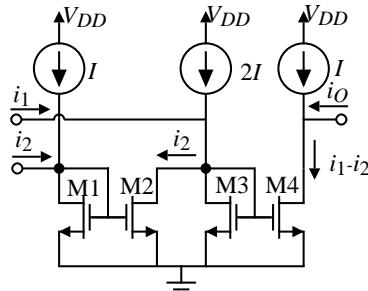


Fig. 5.4-7

SUMMARY

- Low input resistance amplifiers use the source as the input terminal with the gate generally on ground
 - The input resistance to the common gate amplifier depends on what is connected to the drain
 - The voltage driven common gate/common source amplifier has one dominant pole
 - The current driven common gate/common source amplifier has two dominant poles
 - The cascode amplifier eliminates the input dominant pole for the current driven common gate/common source amplifier
 - Current amplifiers have a low input resistance, high output resistance, and a defined output-input current relationship
 - Input resistances less than $1/g_m$ require feedback

However, all feedback loops have internal poles that cause the benefits of negative feedback to vanish at high frequencies.

In addition, feedback loops can have a slow time constant from a pole-zero pair.

- Voltage amplifiers using a current amplifier have high values of gain-bandwidth
 - Current amplifiers are useful at low power supplies and for switched current applications

LECTURE 210 – OUTPUT AMPLIFIERS

LECTURE ORGANIZATION

Outline

- Introduction
- Class A Amplifiers
- Push-Pull Amplifiers
- Bipolar Junction Transistor Output Amplifiers
- Using Negative Feedback to Reduce the Output Resistance
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 218-229

INTRODUCTION

General Considerations of Output Amplifiers

Requirements:

- 1.) Provide sufficient output power in the form of voltage or current.
- 2.) Avoid signal distortion.
- 3.) Be efficient
- 4.) Provide protection from abnormal conditions (short circuit, over temperature, etc.)

Types of Output Amplifiers:

- 1.) Class A amplifiers
- 2.) Source followers
- 3.) Push-pull amplifiers
- 4.) Substrate BJT amplifiers
- 5.) Amplifiers using negative shunt feedback

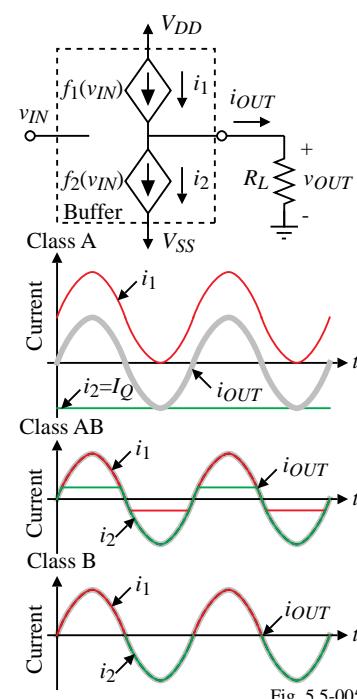
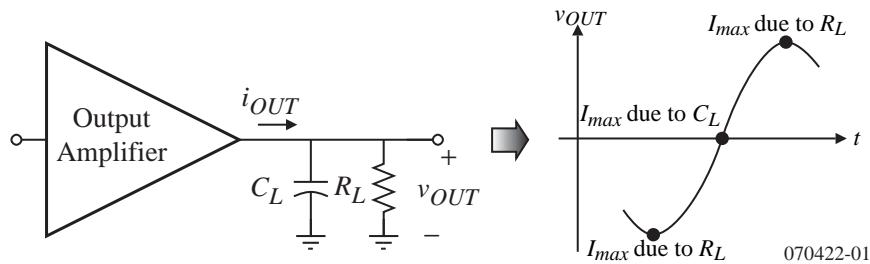


Fig. 5.5-005

Output Current Requirements for an Output Amplifier

Consider the current requirements placed by the load on the output amplifier:



Result:

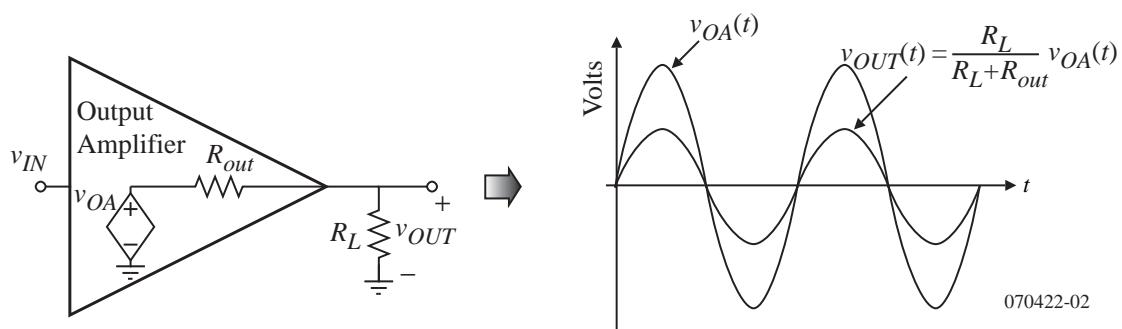
$$|i_{OUT}| > C_L \cdot SR$$

$$|i_{OUT}| > \frac{v_{OUT}(\text{peak})}{R_L}$$

Fortunately, the maximum current for the resistor and capacitor do not occur at the same time.

Output Resistance Requirements for an Output Amplifier

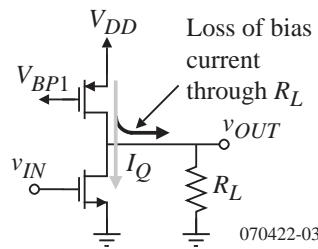
In order to avoid attenuation of the amplifier voltage signal, the output resistance of the amplifier must be less than the load resistance.



To avoid attenuation of the amplifier voltage signal, $R_{out} \ll R_L$.

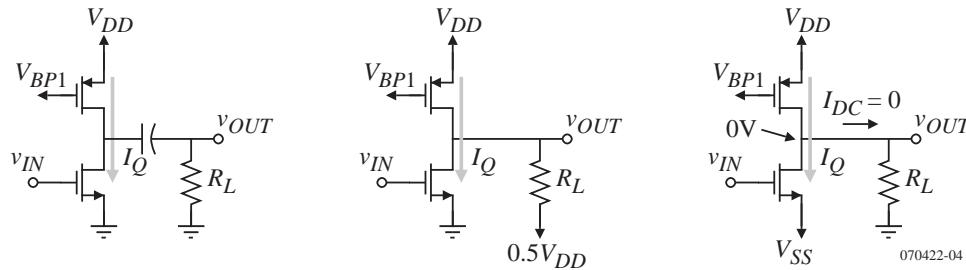
Separation of the Amplifier Bias from the Load Resistance

Unfortunately, when a low load resistance is connected to the output of an amplifier, the bias conditions can be changed.



Solution:

- 1.) Use a coupling capacitance for singled-ended power supplies.
- 2.) Redefine the output analog ground as ($V_{DD}/2$).
- 3.) Use dc coupling for split power supplies.



CLASS A AMPLIFIERS

Current source load inverter

A Class A circuit has current flow in the MOSFETs during the entire period of a sinusoidal signal.

Characteristics of Class A amplifiers:

- Unsymmetrical sinking and sourcing
- Linear
- Poor efficiency

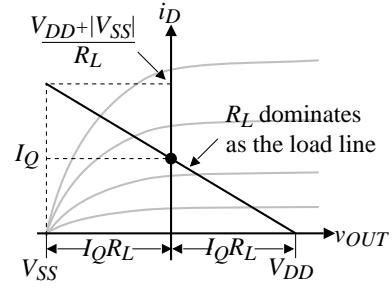
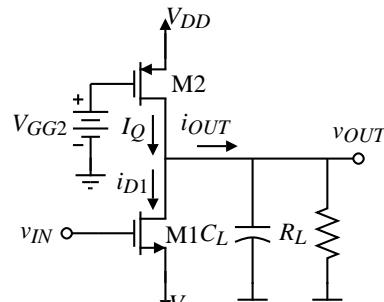


Fig. 5.5-1

$$\text{Efficiency} = \frac{P_{RL}}{P_{\text{Supply}}} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})I_Q} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD}-V_{SS})\left(\frac{(V_{DD}-V_{SS})}{2R_L}\right)} = \left(\frac{v_{OUT}(\text{peak})}{V_{DD}-V_{SS}}\right)^2$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD} = |V_{SS}|$ which gives 25%.

Optimum Value of Load Resistor

Depending on the value of R_L , the signal swing can be symmetrical or asymmetrical.
(This ignores the limitations of the transistor.)

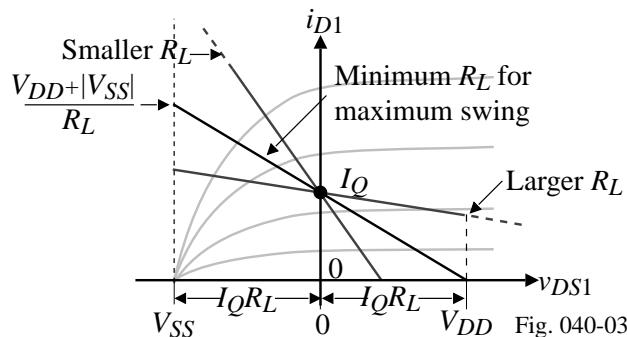


Fig. 040-03

Small-Signal Performance of the Class A Amplifier

Although we have considered the small-signal performance of the Class A amplifier as the current source load inverter, let us include the influence of the load.

The modified small-signal model:

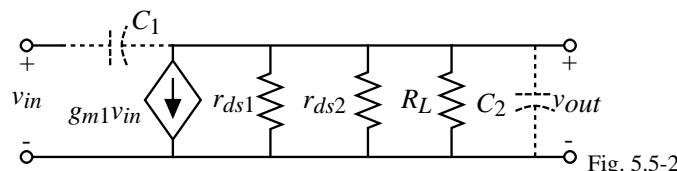


Fig. 5.5-2

The small-signal voltage gain is:

$$\frac{v_{out}}{v_{in}} = \frac{-g_m 1}{g_{ds1} + g_{ds2} + G_L}$$

The small-signal frequency response includes:

A zero at

$$z = \frac{g_m 1}{C_{gd1}}$$

and a pole at

$$p = \frac{-(g_{ds1} + g_{ds2} + G_L)}{C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L}$$

Example 210-1 - Design of a Simple Class-A Output Stage

Assume that $K_N' = 2K_P' = 100\mu A/V^2$, $V_{TN} = 0.5V$ and $V_{TP} = -0.5V$. Design the W/L ratios of M1 and M2 so that a voltage swing of $\pm 1V$ and a slew rate of $\approx 1 V/\mu s$ is achieved if $R_L = 1 k\Omega$ and $C_L = 1000 pF$. Assume $V_{DD} = |V_{SS}| = 2V$ and $V_{GG2} = 0V$. Let $L = 1 \mu m$ and assume that $C_{gd1} = 100fF$. Find the voltage gain and roots of this output amplifier.

Solution

Let us first consider the effects of R_L and C_L .

$$i_{OUT}(\text{peak}) = \pm 1V/1k\Omega = \pm 1000\mu A \quad \text{and} \quad C_L \cdot SR = 10^{-9} \cdot 10^6 = 1000\mu A$$

Since the current for C_L and R_L occur at different times, choose a bias current of 1mA.

$$\frac{W_1}{L_1} = \frac{2(I_{OUT} + I_Q)}{K_N'(V_{DD} + |V_{SS}| - V_{TN})^2} = \frac{4000}{100 \cdot (3.5)^2} \approx \frac{3\mu m}{1\mu m}$$

and

$$\frac{W_2}{L_2} = \frac{2I_{OUT}^+}{K_P'(V_{DD} - V_{GG2} - |V_{TP}|)^2} = \frac{2000}{50 \cdot (1.5)^2} \approx \frac{18\mu m}{1\mu m}$$

The small-signal performance is $A_v = -0.775 \text{ V/V}$.

The roots are, zero $= g_m L / C_{gd1} \Rightarrow 1.23\text{GHz}$ and pole $\approx 1/(R_L C_L) \Rightarrow -159.15 \text{ kHz}$

Broadband Harmonic Distortion

The linearity of an amplifier can be characterized by its influence on a pure sinusoidal input signal.

Assume the input is,

$$V_{in}(\omega) = V_p \sin(\omega t)$$

The output of an amplifier with distortion will be

$$V_{out}(\omega) = a_1 V_p \sin(\omega t) + a_2 V_p \sin(2\omega t) + \dots + a_n V_p \sin(n\omega t)$$

Harmonic distortion (HD) for the i th harmonic can be defined as the ratio of the magnitude of the i th harmonic to the magnitude of the fundamental.

For example, second-harmonic distortion would be given as

$$HD_2 = \frac{a_2}{a_1}$$

Total harmonic distortion (THD) is defined as the square root of the ratio of the sum of all of the second and higher harmonics to the magnitude of the first or fundamental

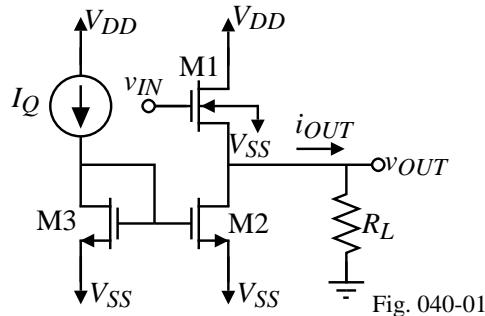
$$\text{Thus, } THD = \frac{\sqrt{a_2^2 + a_3^2 + \dots + a_n^2}}{a_1}^{1/2}$$

The distortion of the class A amplifier is good for small signals and becomes poor at maximum output swings because of the nonlinearity of the voltage transfer curve for large-signal swing

Class-A Source Follower

The class-A source follower has lower output resistance and less attenuation of the amplifier voltage signal.

N-Channel Source Follower with current sink bias:



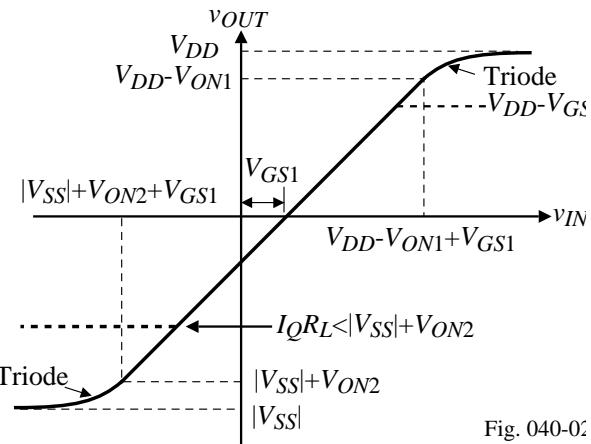
Maximum output voltage swings:

$$v_{OUT}(\min) \approx V_{SS} - V_{ON2} \text{ (if } R_L \text{ is large)}$$

or $v_{OUT}(\min) \approx -I_Q R_L \text{ (if } R_L \text{ is small)}$

$$v_{OUT}(\max) = V_{DD} - V_{ON1} \text{ (if } v_{IN} > V_{DD})$$

Voltage transfer curve:



$$\text{or } v_{OUT}(\max) \approx V_{DD} - V_{GS1}$$

Output Voltage Swing of the Follower

The previous results do not include the bulk effect on V_{T1} of V_{GS1} .

Therefore,

$$V_{T1} = V_{T01} + \gamma_1 \sqrt{2|\phi_F| - v_{BS}} - \sqrt{2|\phi_F|} \approx V_{T01} + \gamma_1 \sqrt{v_{SB}} = V_{T01} + \gamma_1 \sqrt{v_{OUT}(\max) - V_{SS}}$$

$$\therefore v_{OUT}(\max) - V_{SS} \approx V_{DD} - V_{SS} - V_{ON1} - V_{T1} = V_{DD} - V_{SS} - V_{ON1} - V_{T01} - \gamma_1 \sqrt{v_{OUT}(\max) - V_{SS}}$$

Define $v_{OUT}(\max) - V_{SS} = v_{OUT}'(\max)$

which gives the quadratic,

$$v_{OUT}'(\max) + \gamma_1 \sqrt{v_{OUT}'(\max)} - (V_{DD} - V_{SS} - V_{ON1} - V_{T01}) = 0$$

Solving the quadratic gives,

$$v_{OUT}'(\max) \approx \frac{\gamma_1^2}{4} - \frac{\gamma_1}{2} \sqrt{\gamma_1^2 + 4(V_{DD} - V_{SS} - V_{ON1} - V_{T01})} + \frac{\gamma_1^2 + 4(V_{DD} - V_{SS} - V_{ON1} - V_{T01})}{4}$$

If $V_{DD} = 2.5V$, $\gamma_1 = 0.4V^{1/2}$, $V_{T01} = 0.7V$, and $V_{ON1} = 0.2V$, then $v_{OUT}'(\max) = 3.661V$
and

$$v_{OUT}(\max) = 3.661 - 2.5 = 0.8661V$$

Maximum Sourcing and Sinking Currents for the Source Follower

Maximum Sourcing Current (into a short circuit):

We assume that the transistors are in saturation and $V_{DD} = -V_{SS} = 2.5V$, thus

$$I_{OUT}(\text{sourcing}) = \frac{K' W_1}{2L_1} [V_{DD} - v_{OUT} - V_{T1}]^2 - I_Q$$

where v_{IN} is assumed to be equal to V_{DD} .

If $W_1/L_1 = 10$ and if $v_{OUT} = 0V$, then

$$V_{T1} = 1.08V \Rightarrow I_{OUT} \text{ equal to } 1.11 \text{ mA.}$$

However, as v_{OUT} increases above 0V, the current rapidly decreases.

Maximum Sinking Current:

For the current sink load, the sinking current is limited by the bias current.

$$I_{OUT}(\text{sinking}) = I_Q$$

Efficiency of the Class A, source follower:

Same as the Class A, common source which is 25% maximum efficiency

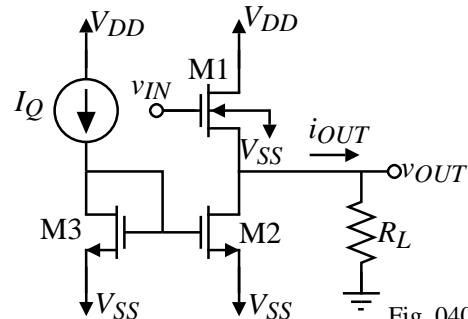


Fig. 040-01

Small Signal Performance of the Source Follower

Small-signal model:

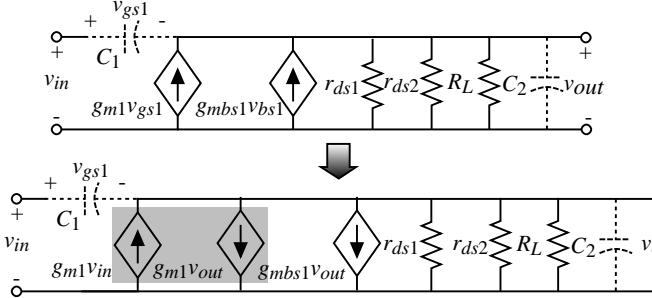


Fig. 040-04

$$\frac{V_{out}}{V_{in}} = \frac{g_m1}{g_{ds1} + g_{ds2} + g_m1 + g_{mbs1} + G_L} \cong \frac{g_m1}{g_m1 + g_{mbs1} + G_L} \cong \frac{g_m1 R_L}{1 + g_m1 R_L}$$

If $V_{DD} = -V_{SS} = 2.5V$, $V_{out} = 0V$, $W_1/L_1 = 10\mu\text{m}/1\mu\text{m}$, $W_2/L_2 = 1\mu\text{m}/1\mu\text{m}$, and $I_D = 500\mu\text{A}$, then:

For the current sink load follower ($R_L = \infty$):

$$\frac{V_{out}}{V_{in}} = 0.869 \text{V/V, if the bulk effect were ignored, then } \frac{V_{out}}{V_{in}} = 0.963 \text{V/V}$$

For a finite load, $R_L = 1000\Omega$:

$$\frac{V_{out}}{V_{in}} = 0.512 \text{V/V}$$

Small Signal Performance of the Source Follower - Continued

The output resistance is:

$$R_{out} = \frac{1}{g_{m1} + g_{mbs1} + g_{ds1} + g_{ds2}}$$

For the current sink load follower:

$$R_{out} = 830\Omega$$

The frequency response of the source follower:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{(g_{m1} + sC_1)}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + G_L + s(C_1 + C_2)}$$

where

$$C_1 = \text{capacitances connected between the input and output} \approx C_{GS1}$$

$$C_2 = C_{bs1} + C_{bd2} + C_{gd2} (\text{or } C_{gs2}) + C_L$$

$$z = -\frac{g_{m1}}{C_1} \quad \text{and} \quad p \approx -\frac{g_{m1} + G_L}{C_1 + C_2}$$

The presence of a LHP zero leads to the possibility that in most cases the pole and zero will provide some degree of cancellation leading to a broadband response.

PUSH-PULL AMPLIFIERS

Push-Pull Source Follower

Can both sink and source current and provide a slightly lower output resistance.

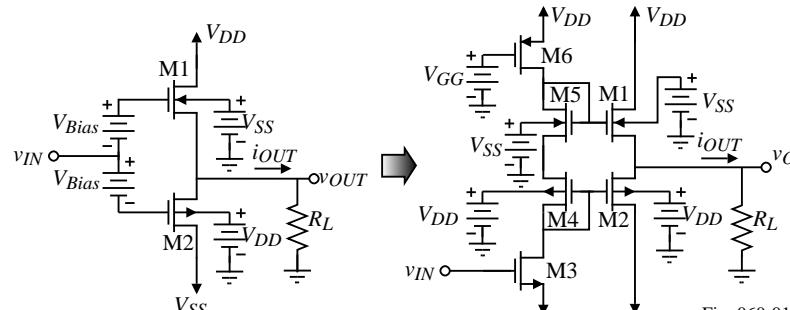


Fig. 060-01

Efficiency:

Depends on how the transistors are biased.

- Class B - one transistor has current flow for only 180° of the sinusoid (half period)

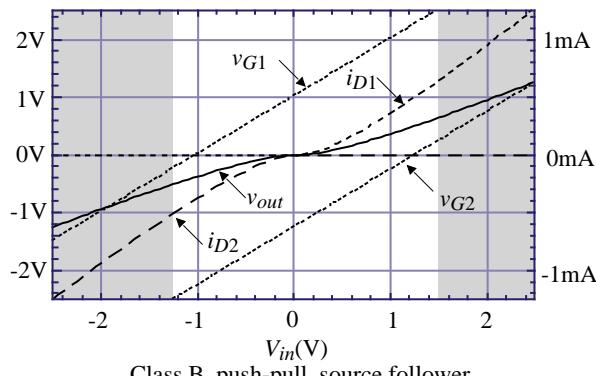
$$\therefore \text{Efficiency} = \frac{P_{RL}}{P_{VDD}} = \frac{\frac{v_{OUT}(\text{peak})^2}{2R_L}}{(V_{DD} - V_{SS}) \left(\frac{1}{2} \right) \left(\frac{2v_{OUT}(\text{peak})}{\pi R_L} \right)} = \frac{\pi}{2} \frac{v_{OUT}(\text{peak})^2}{V_{DD} - V_{SS}}$$

Maximum efficiency occurs when $v_{OUT}(\text{peak}) = V_{DD}$ and is 78.5%

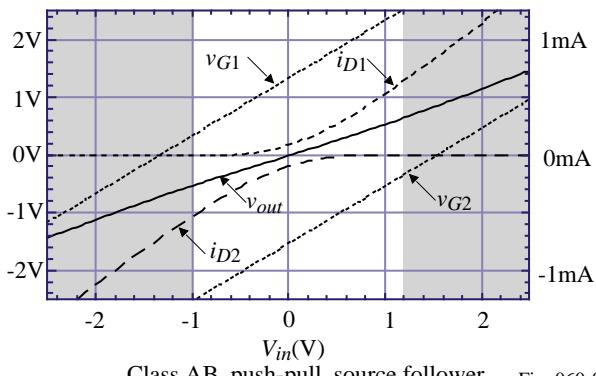
- Class AB - each transistor has current flow for more than 180° of the sinusoid. Maximum efficiency is between 25% and 78.5%

Illustration of Class B and Class AB Push-Pull, Source Follower

Output current and voltage characteristics of the push-pull, source follower ($R_L = 1\text{k}\Omega$):



Class B, push-pull, source follower



Class AB, push-pull, source follower

Fig. 060-02

Comments:

- Note that v_{OUT} cannot reach the extreme values of V_{DD} and V_{SS}
- $I_{OUT+}(\text{max})$ and $I_{OUT-}(\text{max})$ is always less than V_{DD}/R_L or V_{SS}/R_L
- For $v_{OUT}=0\text{V}$, there is quiescent current flowing in M1 and M2 for Class AB
- Note that there is significant distortion at $v_{IN}=0\text{V}$ for the Class B push-pull follower

Small-Signal Performance of the Push-Pull Follower

Model:

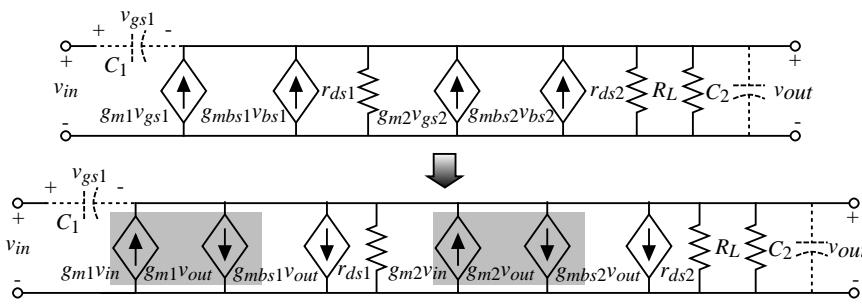


Fig. 060-03

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2} + G_L}$$

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2}} \quad (\text{does not include } R_L)$$

If $V_{DD} = -V_{SS} = 2.5\text{V}$, $V_{out} = 0\text{V}$, $I_{D1} = I_{D2} = 500\mu\text{A}$, and $\text{W/L} = 20\mu\text{m}/2\mu\text{m}$, $A_v = 0.787$ ($R_L = \infty$) and $R_{out} = 448\Omega$.

A zero and pole are located at

$$z = \frac{-(g_{m1} + g_{m2})}{C_1} \quad p = \frac{-(g_{ds1} + g_{ds2} + g_{m1} + g_{mbs1} + g_{m2} + g_{mbs2} + G_L)}{C_1 + C_2}.$$

These roots will be at high frequencies because the associated resistances are small.

Push-Pull, Common Source Amplifiers

Similar to the class A but can operate as class B providing higher efficiency.

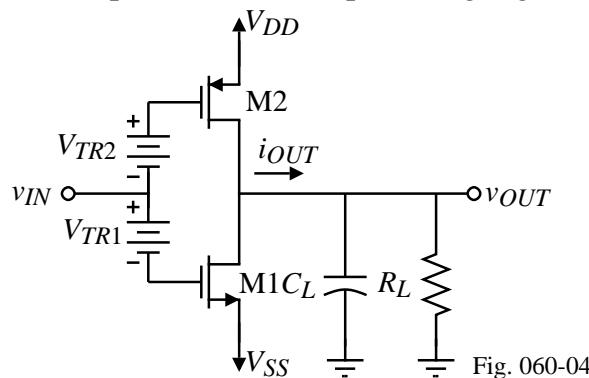


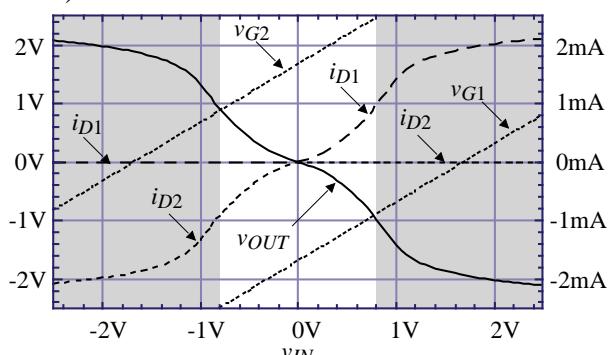
Fig. 060-04

Comments:

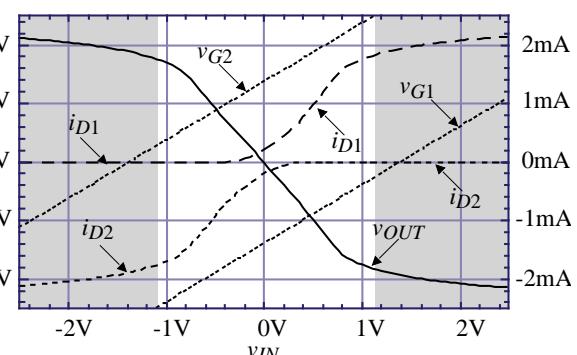
- The batteries V_{TR1} and V_{TR2} are necessary to control the bias current in M1 and M2.
- The efficiency is the same as the push-pull, source follower.

Illustration of Class B and Class AB Push-Pull, Inverting Amplifier

Output current and voltage characteristics of the push-pull, inverting amplifier ($R_L = 1\text{k}\Omega$):



Class B, push-pull, inverting amplifier.



Class AB, push-pull, inverting amplifier. Fig.060-06

Comments:

- Note that there is significant distortion at $v_{IN} = 0\text{V}$ for the Class B inverter
- Note that v_{OUT} cannot reach the extreme values of V_{DD} and V_{SS}
- $I_{OUT}^{+}(\text{max})$ and $I_{OUT}^{-}(\text{max})$ is always less than V_{DD}/R_L or V_{SS}/R_L
- For $v_{OUT} = 0\text{V}$, there is quiescent current flowing in M1 and M2 for Class AB

Practical Implementation of the Push-Pull, Common Source Amplifier – Method 1

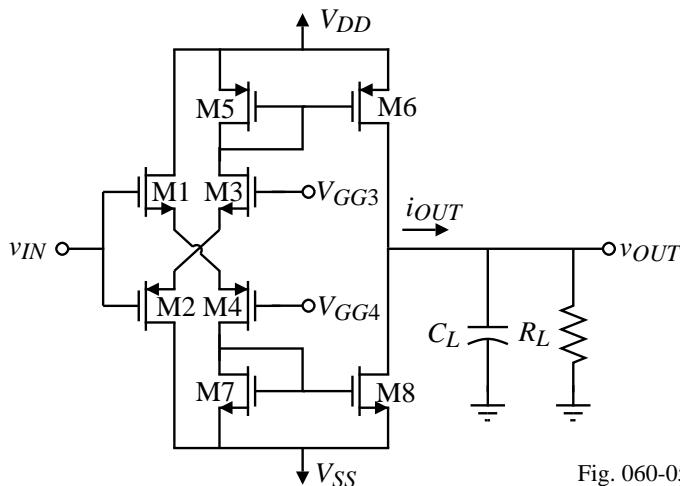


Fig. 060-05

V_{GG3} and V_{GG4} can be used to bias this amplifier in class AB or class B operation.

Note, that the bias current in M6 and M8 is not dependent upon V_{DD} or V_{SS} (assuming V_{GG3} and V_{GG4} are not dependent on V_{DD} and V_{SS}).

Practical Implementation of the Push-Pull, Common Source Amplifier – Method 2

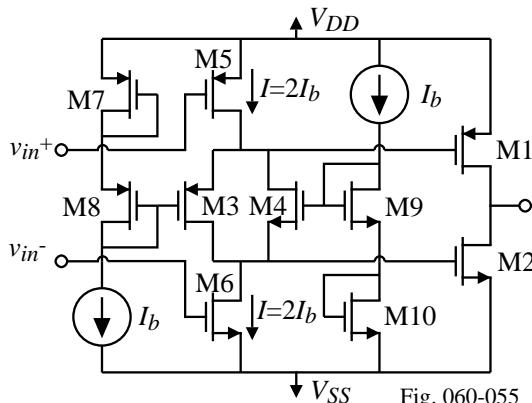


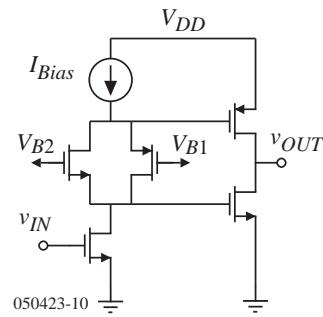
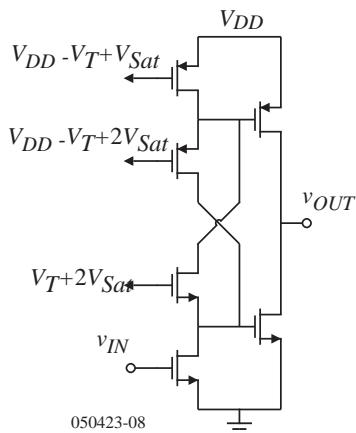
Fig. 060-055

In steady-state, the current through M5 and M6 is $2I_b$. If $W_4/L_4 = W_9/L_9$ and $W_3/L_3 = W_8/L_8$, then the currents in M1 and M2 can be determined by the following relationship:

$$I_1 = I_2 = I_b \left(\frac{W_1/L_1}{W_7/L_7} \right) = I_b \left(\frac{W_2/L_2}{W_{10}/L_{10}} \right)$$

If v_{in^+} goes low, M5 pulls the gates of M1 and M2 high. M4 shuts off causing all of the current flowing through M5 ($2I_b$) to flow through M3 shutting off M1. The gate of M2 is high allowing the buffer to strongly sink current. If v_{in^-} goes high, M6 pulls the gates of M1 and M2 low. As before, this shuts off M2 and turns on M1 allowing strong sourcing.

Additional Methods of Biasing the Push-Pull Common-Source Amplifier



BIPOLAR JUNCTION TRANSISTOR OUTPUT AMPLIFIERS

What about the use of BJTs?

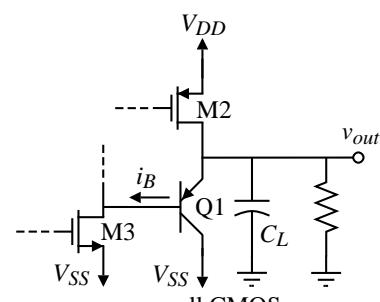
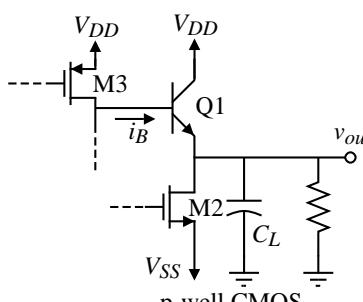


Fig. 5.5-8A

Comments:

- Can use either substrate or lateral BJTs.
- Small-signal output resistance is $1/g_m$ which can easily be less than 100Ω .
- Unfortunately, only PNP or NPN BJTs are available but not both on a standard CMOS technology.
- In order for the BJT to sink (or source) large currents, the base current, i_B , must be large. Providing large currents as the voltage gets to extreme values is difficult for MOSFET circuits to accomplish.
- If one considers the MOSFET driver, the emitter can only pull to within $v_{BE} + V_{ON}$ of the power supply rails. This value can be 1V or more.

Low Output Resistance using BJTs

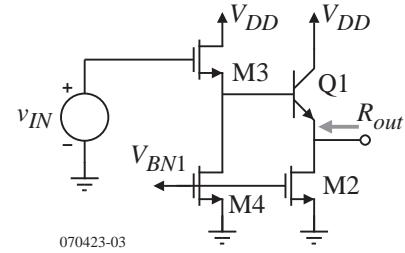
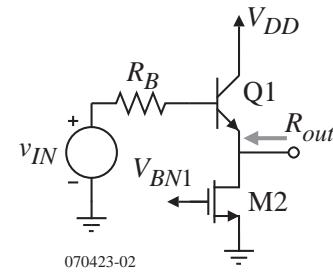
The output resistance of a class A BJT stage is:

$$R_{out} = \frac{r_{\pi 1} + R_B}{1+\beta_F} = \frac{1}{g_m 1} + \frac{R_B}{1+\beta_F}$$

Note that the second term must be less than $1/g_m 1$ in order to achieve the low output resistance possible.

Consequently, the driver for the BJT should be a MOS follower as shown:

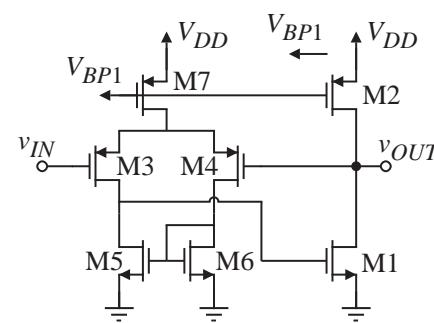
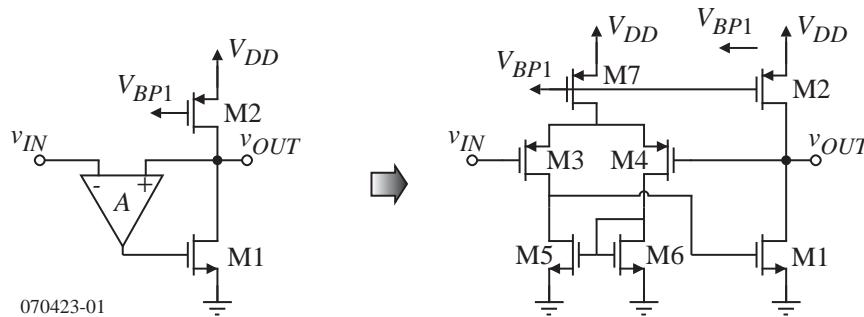
$$R_{out} = \frac{r_{\pi 1} + 1/g_m 3}{1+\beta_F} = \frac{1}{g_m 1} + \frac{1}{g_m 3(1+\beta_F)} \approx \frac{1}{g_m 1}$$



We will consider the BJT as an output stage in more detail later.

USING NEGATIVE FEEDBACK TO REDUCE THE OUTPUT RESISTANCE Concept

Use negative shunt feedback – Class A implementation:



$$R_{out} = \frac{r_{ds1} \| r_{ds2}}{1+\text{Loop Gain}} \approx \frac{1}{2g_m^2 r_{ds}} \approx 10\Omega \text{ if } g_m = 500\mu\text{S} \text{ and } g_m r_{ds} \approx 100.$$

The actual value of R_{out} will be influenced by the value of R_L , particularly if it is small.

Push-Pull Implementation

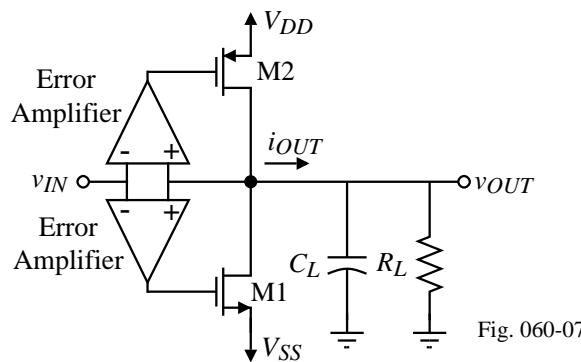


Fig. 060-07

$$R_{out} = \frac{r_{ds1} \| r_{ds2}}{1 + \text{Loop Gain}}$$

Comments:

- Can achieve output resistances as low as 10Ω .
- If the error amplifiers are not balanced, it is difficult to control the quiescent current in M1 and M2
- Great linearity because of the strong feedback
- Can be efficient if operated in class B or class AB
- We will consider this circuit in more detail in a later lecture.

Simple Implementation of Neg., Shunt Feedback to Reduce the Output Resistance

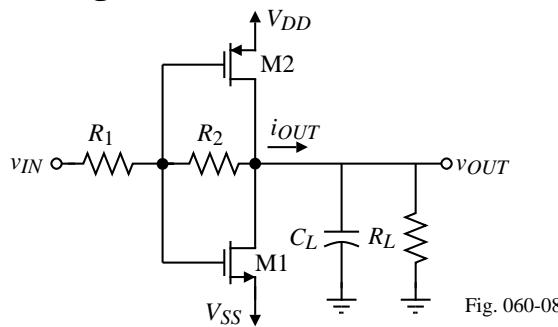


Fig. 060-08

$$\text{Loop gain} \approx \left(\frac{R_1}{R_1 + R_2} \right) \left(\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + G_L} \right)$$

$$\therefore R_{out} = \frac{r_{ds1} \| r_{ds2}}{1 + \left(\frac{R_1}{R_1 + R_2} \right) \left(\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2} + G_L} \right)}$$

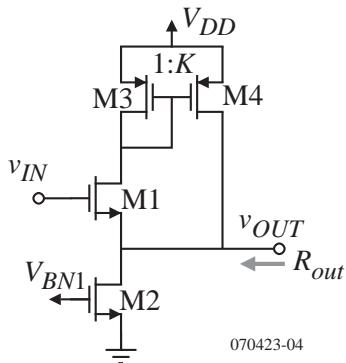
Let $R_1 = R_2$, $R_L = \infty$, $I_{Bias} = 500\mu\text{A}$, $W_1/L_1 = 100\mu\text{m}/1\mu\text{m}$ and $W_2/L_2 = 200\mu\text{m}/1\mu\text{m}$.

Thus, $g_{m1} = 3.316\text{mS}$, $g_{m2} = 3.162\text{mS}$, $r_{ds1} = 50\text{k}\Omega$ and $r_{ds2} = 40\text{k}\Omega$.

$$\therefore R_{out} = \frac{50\text{k}\Omega \| 40\text{k}\Omega}{1 + 0.5 \left(\frac{3316 + 3162}{25 + 20} \right)} = \frac{22.22\text{k}\Omega}{1 + 0.5(143.9)} = 304\Omega \quad (R_{out} = 5.42\text{k}\Omega \text{ if } R_L = 1\text{k}\Omega)$$

Boosting the Transconductance of the Source Follower

The following configuration allows the output resistance of the source follower to be decreased by a factor of K , where K is the current ratio between M4 and M3.



$$R_{out} = \frac{1}{g_m 1 K}$$

SUMMARY

- The objectives are to provide output power in form of voltage and/or current.
- In addition, the output amplifier should be linear and be efficient.
- Low output resistance is required to provide power efficiently to a small load resistance
- High source/sink currents are required to provide sufficient output voltage rate due to large load capacitances.
- Types of output amplifiers considered:

Class A amplifier
 Source follower
 Class B and AB amplifier
 Use of BJTs
 Negative shunt feedback

LECTURE 220 – INTRODUCTION TO OP AMPS

LECTURE OUTLINE

Outline

- Op Amps
- Categorization of Op Amps
- Compensation of Op Amps
- Miller Compensation
- Other Forms of Compensation
- Op Amp Slew Rate
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 243-269

OP AMPS

What is an Op Amp?

The op amp (operational amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function.

The basic requirements for an op amp:

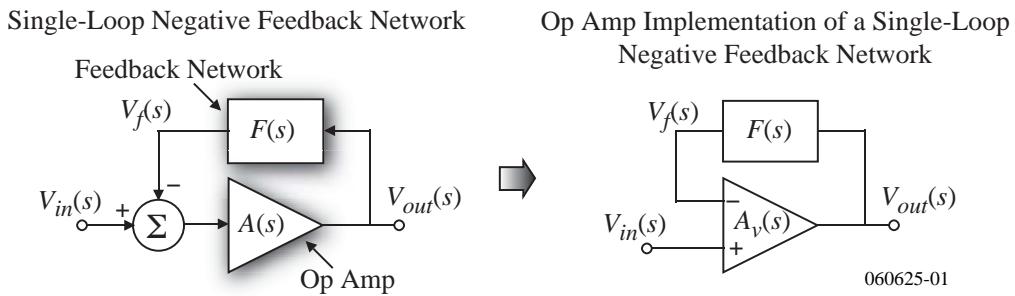
- Sufficiently large gain (the accuracy of the signal processing determines this)
- Differential inputs
- Frequency characteristics that permit stable operation when negative feedback is applied

Other requirements:

- High input impedance
- Low output impedance
- High speed/frequency

Why Op Amps?

The op amp is designed to be used with single-loop, negative feedback to accomplish precision signal processing as illustrated below.



The voltage gain, $\frac{V_{out}(s)}{V_{in}(s)}$, can be shown to be equal to,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_v(s)}{1+A_v(s)F(s)}$$

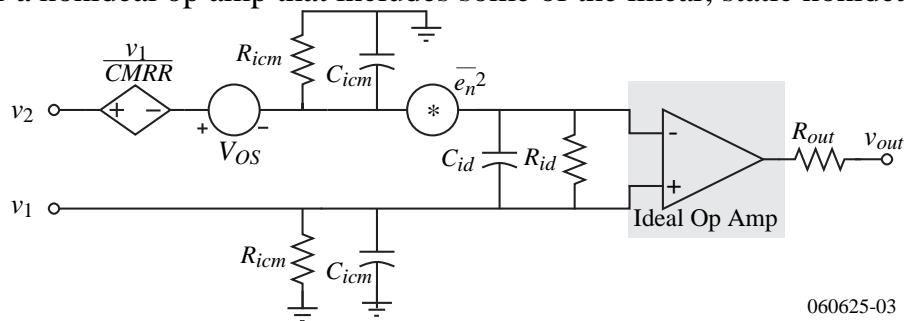
If the product of $A_v(s)F(s)$ is much greater than 1, then the voltage gain becomes,

$$\frac{V_{out}(s)}{V_{in}(s)} \approx \frac{1}{F(s)} \quad \Rightarrow \quad \text{The precision of the voltage gain is defined by } F(s).$$

OP AMP CHARACTERIZATION

Linear and Static Characterization of the CMOS Op Amp

A model for a nonideal op amp that includes some of the linear, static nonidealities:



where

R_{id} = differential input resistance

C_{id} = differential input capacitance

R_{icm} = common mode input resistance

C_{icm} = common mode input capacitance

V_{OS} = input-offset voltage

$CMRR$ = common-mode rejection ratio (when $v_1=v_2$ an output results)

e_n^2 = voltage-noise spectral density (mean-square volts/Hertz)

Linear and Dynamic Characteristics of the Op Amp

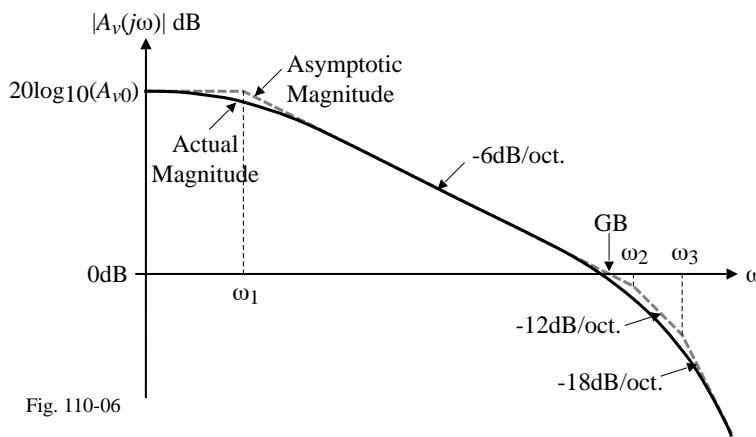
Differential and common-mode frequency response:

$$V_{out}(s) = A_v(s)[V_1(s) - V_2(s)] \pm A_c(s) \left(\frac{V_1(s) + V_2(s)}{2} \right)$$

Differential-frequency response:

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\dots} = \frac{A_{v0} p_1 p_2 p_3 \dots}{(s - p_1)(s - p_2)(s - p_3)\dots}$$

where p_1, p_2, p_3, \dots are the poles of the differential-frequency response (ignoring zeros).



Other Characteristics of the Op Amp

Power supply rejection ratio (*PSRR*):

$$PSRR = \frac{\Delta V_{DD}}{\Delta V_{OUT}} A_v(s) = \frac{V_o/V_{in} (V_{dd} = 0)}{V_o/V_{dd} (V_{in} = 0)}$$

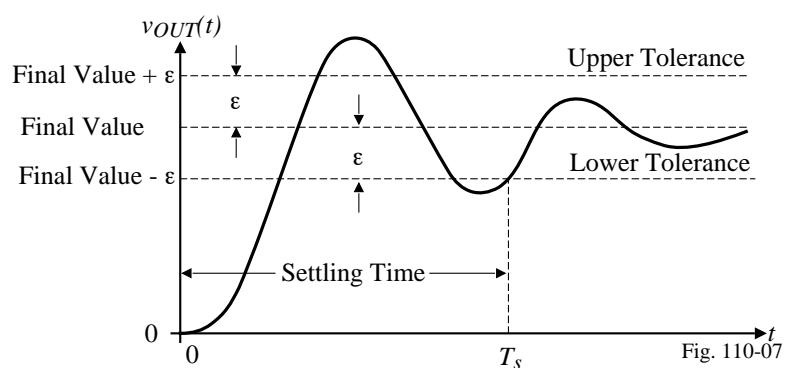
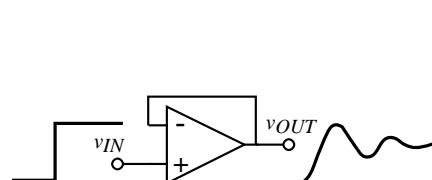
Input common mode range (*ICMR*):

ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

Slew rate (*SR*):

SR = output voltage rate limit of the op amp

Settling time (T_s):



OP AMP CATEGORIZATION

Classification of CMOS Op Amps

Conversion	Hierarchy		
Voltage to Current	Classic Differential Amplifier	Modified Differential Amplifier	First Voltage Stage
Current to Voltage	Differential-to-single ended Load (Current Mirror)	Source/Sink Current Loads	MOS Diode Load
Voltage to Current	Transconductance Grounded Gate	Transconductance Grounded Source	Current Stage
Current to Voltage	Class A (Source or Sink Load)	Class B (Push-Pull)	Second Voltage Stage

Table 110-01

Two-Stage CMOS Op Amp

Classical two-stage CMOS op amp broken into voltage-to-current and current-to-voltage stages:

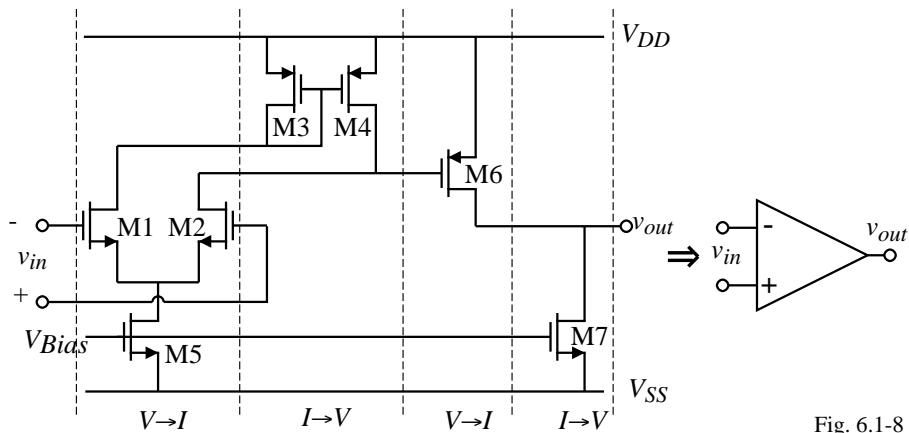
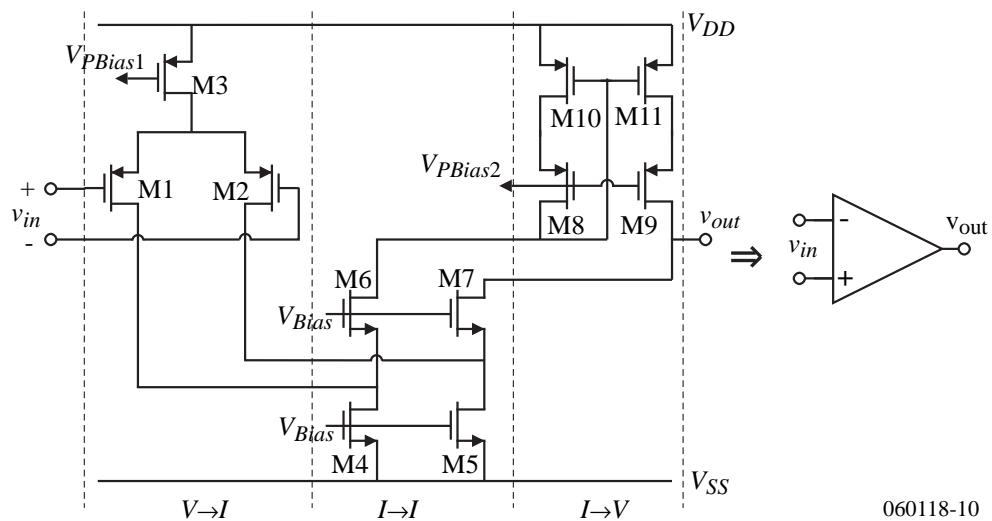


Fig. 6.1-8

Folded Cascode CMOS Op Amp

Folded cascode CMOS op amp broken into stages.



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COMPENSATION OF OP AMPS

Compensation

Objective

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
 - Miller capacitor only
 - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
 - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

Because compensation plays such a strong role in design, it is considered before design.

Single-Loop, Negative Feedback Systems

Block diagram:

$A(s)$ = differential-mode voltage gain of the op amp

$F(s)$ = feedback transfer function from the output of op amp back to the input.

Definitions:

- Open-loop gain = $L(s) = -A(s)F(s)$

$$\text{Closed-loop gain} = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1+A(s)F(s)}$$

Stability Requirements:

The requirements for stability for a single-loop, negative feedback system is,

$$|A(j\omega_{360^\circ})F(j\omega_{360^\circ})| = |L(j\omega_{360^\circ})| < 1 \quad -|A(j\omega_0^\circ)F(j\omega_0^\circ)| = |L(j\omega_0^\circ)| < 1$$

where $\omega_{360^\circ} = \omega_0^\circ$ is defined as

$$\text{Arg}[-A(j\omega_0^\circ)F(j\omega_0^\circ)] = \text{Arg}[L(j\omega_0^\circ)] = 0^\circ = 360^\circ$$

Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_0 \text{dB})F(j\omega_0 \text{dB})] = \text{Arg}[L(j\omega_0 \text{dB})] > 0^\circ$$

where $\omega_0 \text{dB}$ is defined as

$$|A(j\omega_0 \text{dB})F(j\omega_0 \text{dB})| = |L(j\omega_0 \text{dB})| = 1$$

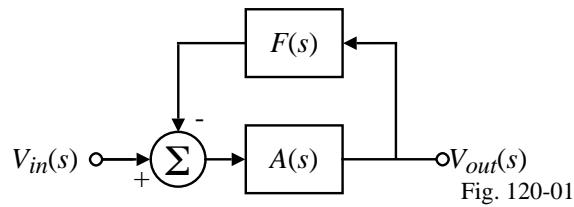
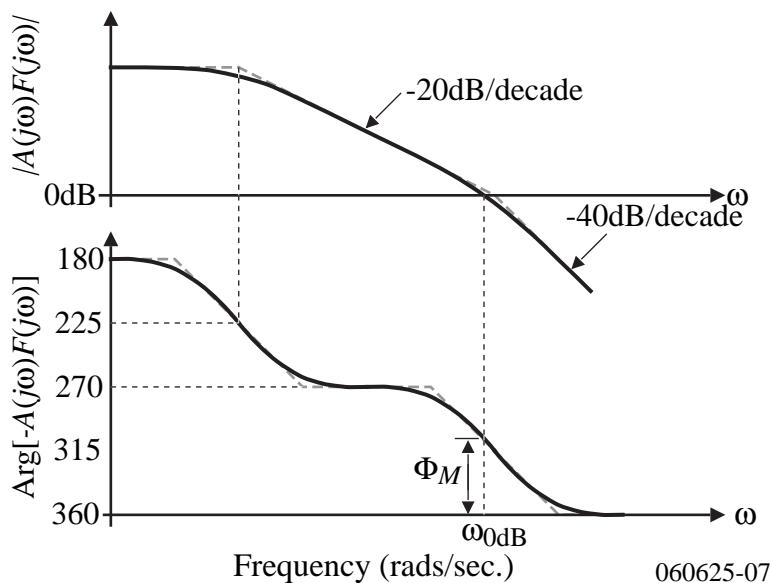


Fig. 120-01

Illustration of the Stability Requirement using Bode Plots



060625-07

A measure of stability is given by the phase when $|A(j\omega)F(j\omega)| = 1$. This phase is called *phase margin*.

$$\text{Phase margin} = \Phi_M = 360^\circ - \text{Arg}[-A(j\omega_0 \text{dB})F(j\omega_0 \text{dB})] = 360^\circ - \text{Arg}[L(j\omega_0 \text{dB})]$$

Why Do We Want Good Stability?

Consider the step response of second-order system which closely models the closed-loop gain of the op amp connected in unity gain.

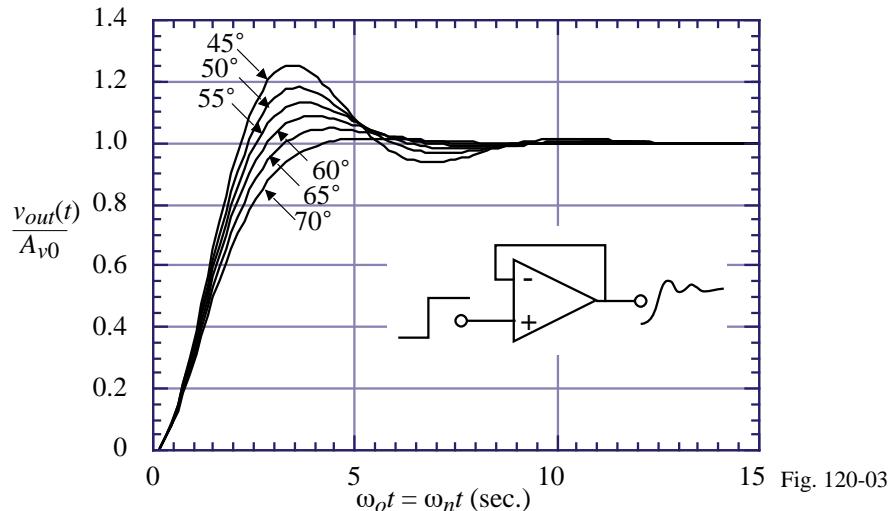


Fig. 120-03

A “good” step response is one that quickly reaches its final value.

Therefore, we see that phase margin should be at least 45° and preferably 60° or larger.

(A rule of thumb for satisfactory stability is that there should be less than three rings.)

Note that good stability is not necessarily the quickest rise time.

Uncompensated Frequency Response of Two-Stage Op Amps

Two-Stage Op Amps:

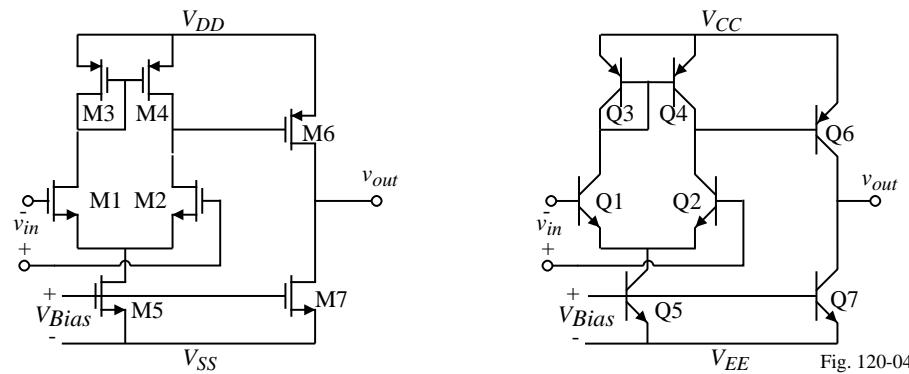


Fig. 120-04

Small-Signal Model:

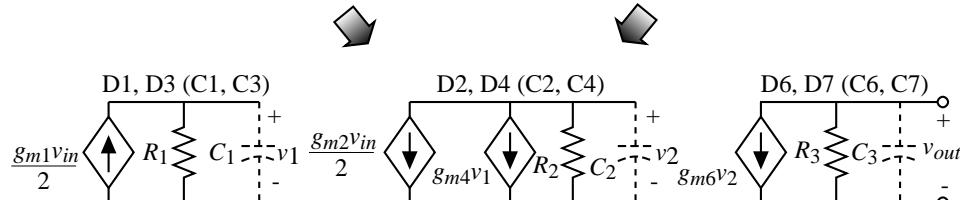


Fig. 120-05

Note that this model neglects the base-collector and gate-drain capacitances for purposes of simplification.

Uncompensated Frequency Response of Two-Stage Op Amps - Continued

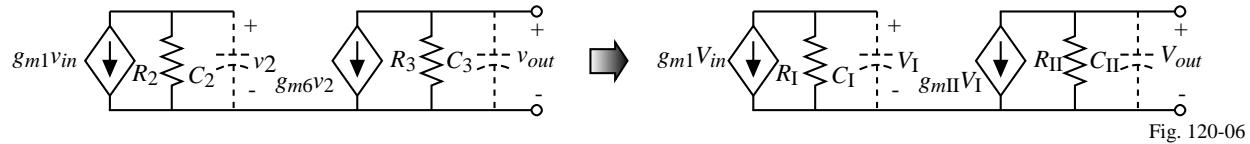
For the MOS two-stage op amp:

$$\begin{aligned} R_1 &\approx \frac{1}{g_{m3}} \| r_{ds3} \| r_{ds1} \approx \frac{1}{g_{m3}} & R_2 = r_{ds2} \| r_{ds4} & \text{and } R_3 = r_{ds6} \| r_{ds7} \\ C_1 = C_{gs3} + C_{gs4} + C_{bd1} + C_{bd3} & & C_2 = C_{gs6} + C_{bd2} + C_{bd4} & \text{and } C_3 = C_L + C_{bd6} + C_{bd7} \end{aligned}$$

For the BJT two-stage op amp:

$$\begin{aligned} R_1 &= \frac{1}{g_{m3}} \| r_{\pi3} \| r_{\pi4} \| r_{o1} \| r_{o3} \approx \frac{1}{g_{m3}} & R_2 = r_{\pi6} \| r_{o2} \| r_{o4} \approx r_{\pi6} & \text{and } R_3 = r_{o6} \| r_{o7} \\ C_1 = C_{\pi3} + C_{\pi4} + C_{cs1} + C_{cs3} & & C_2 = C_{\pi6} + C_{cs2} + C_{cs4} & \text{and } C_3 = C_L + C_{cs6} + C_{cs7} \end{aligned}$$

Assuming the pole due to C_1 is much greater than the poles due to C_2 and C_3 gives,

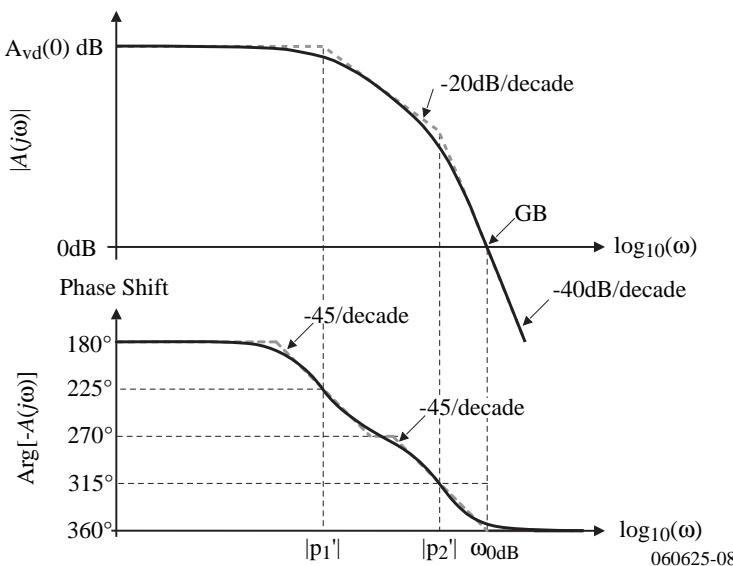


The locations for the two poles are given by the following equations

$$p'_1 = \frac{-1}{R_I C_I} \quad \text{and} \quad p'_2 = \frac{-1}{R_{II} C_{II}}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage.

Uncompensated Frequency Response of an Op Amp ($F(s) = 1$)



If we assume that $F(s) = 1$ (this is the worst case for stability considerations), then the above plot is the same as the loop gain.

Note that the phase margin is much less than 45° ($\approx 6^\circ$).

Therefore, the op amp must be compensated before using it in a closed-loop configuration.

MILLER COMPENSATION

Miller Compensation of the Two-Stage Op Amp

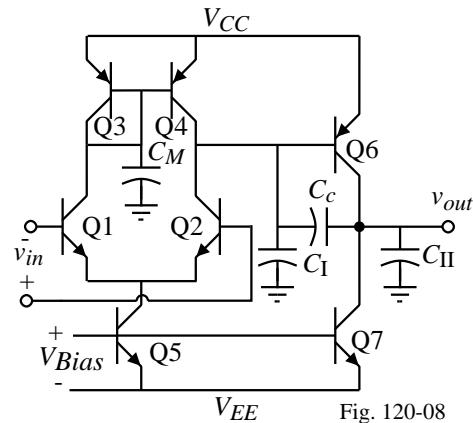
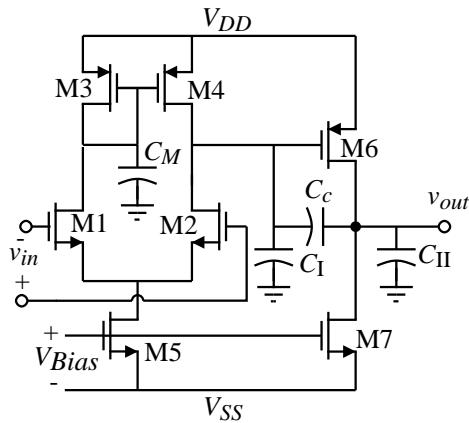


Fig. 120-08

The various capacitors are:

C_c = accomplishes the Miller compensation

C_M = capacitance associated with the first-stage mirror (mirror pole)

C_I = output capacitance to ground of the first-stage

C_{II} = output capacitance to ground of the second-stage

Compensated Two-Stage, Small-Signal Frequency Response Model Simplified

Use the CMOS op amp to illustrate:

1.) Assume that $g_{m3} \gg g_{ds3} + g_{ds1}$

2.) Assume that $\frac{g_{m3}}{C_M} \gg GB$

Therefore,

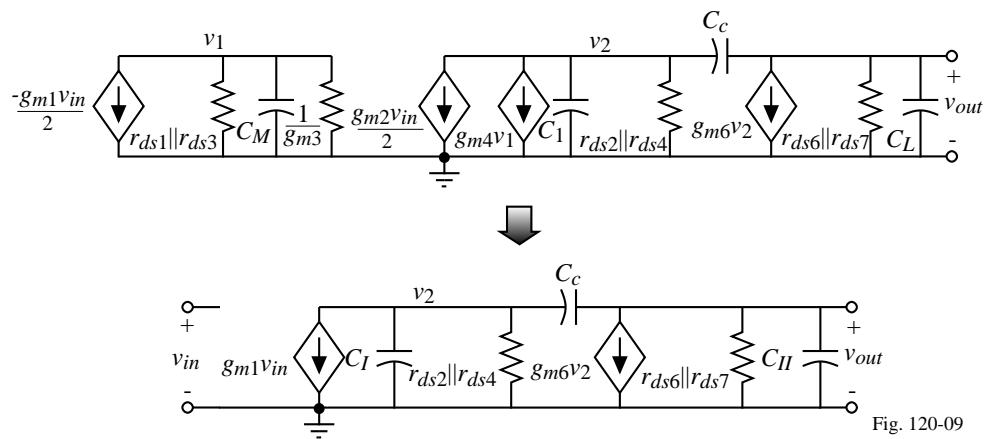
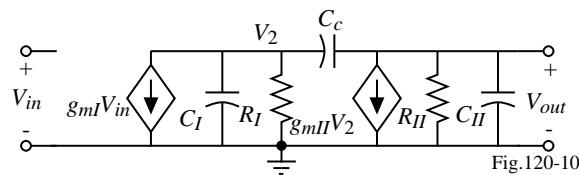


Fig. 120-09

Same circuit holds for the BJT op amp with different component relationships.

General Two-Stage Frequency Response Analysis



where

$$g_{mI} = g_{m1} = g_{m2}, R_I = r_{ds2} \| r_{ds4}, C_I = C_1$$

and

$$g_{mII} = g_{m6}, R_{II} = r_{ds6} \| r_{ds7}, C_{II} = C_2 = C_L$$

Nodal Equations:

$$-g_{mI}V_{in} = [G_I + s(C_I + C_c)]V_2 - [sC_c]V_{out} \quad \text{and} \quad 0 = [g_{mII} - sC_c]V_2 + [G_{II} + sC_{II} + sC_c]V_{out}$$

Solving using Cramer's rule gives,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mI}(g_{mII} - sC_c)}{G_I G_{II} + s[G_{II}(C_I + C_{II}) + G_I(C_{II} + C_c) + g_{mII}C_c] + s^2[C_I C_{II} + C_c C_I + C_c C_{II}]}$$

$$= \frac{A_o[1 - s(C_c/g_{mII})]}{1 + s[R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII}R_I R_{II} C_c] + s^2[R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II})]}$$

where, $A_o = g_{mI}g_{mII}R_I R_{II}$

In general, $D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \rightarrow D(s) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2}$, if $|p_2| \gg |p_1|$

$$\therefore p_1 = \frac{-1}{R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII}R_I R_{II} C_c} \approx \frac{-1}{g_{mII}R_I R_{II} C_c}, \quad z = \frac{g_{mII}}{C_c}$$

$$p_2 = \frac{-[R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII}R_I R_{II} C_c]}{R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II})} \approx \frac{-g_{mII}C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \approx \frac{-g_{mII}}{C_{II}}, \quad C_{II} > C_c > C_I$$

Summary of Results for Miller Compensation of the Two-Stage Op Amp

There are three roots of importance:

1.) Right-half plane zero:

$$z_1 = \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c}$$

This root is very undesirable- it boosts the magnitude while decreasing the phase.

2.) Dominant left-half plane pole (the Miller pole):

$$p_1 \approx \frac{-1}{g_{mII}R_I R_{II} C_c} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}C_c}$$

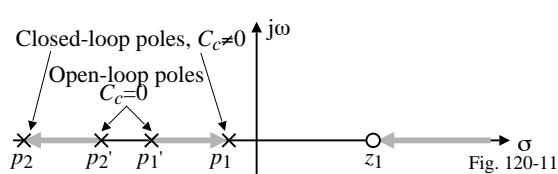
This root accomplishes the desired compensation.

3.) Left-half plane output pole:

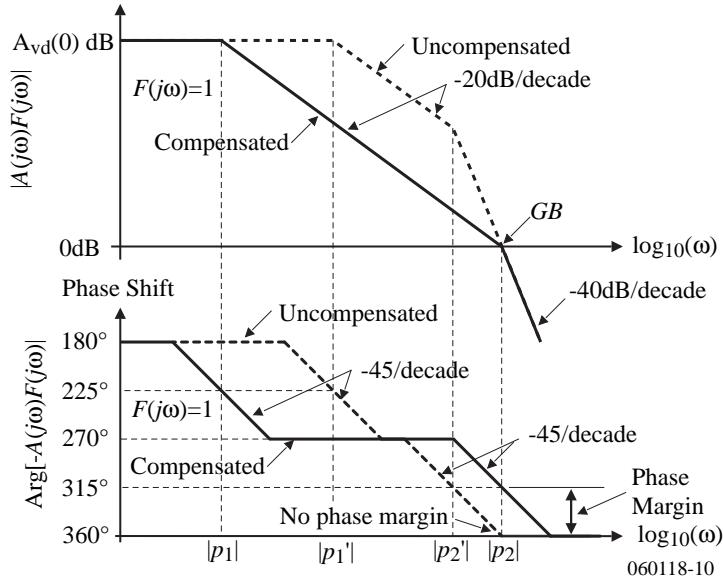
$$p_2 \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{m6}}{C_L}$$

p_2 must be \geq unity-gainbandwidth or satisfactory phase margin will not be achieved.

Root locus plot of the Miller compensation:



Compensated Open-Loop Frequency Response of the Two-Stage Op Amp



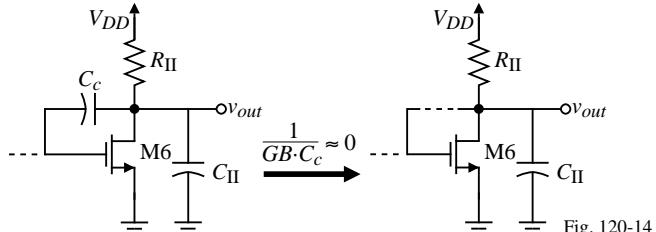
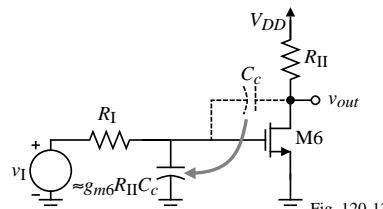
Note that the unity-gainbandwidth, GB , is

$$GB = A_{vd}(0) \cdot |p_1| = (g_m I g_m II R_I R_{II}) \frac{1}{g_m II R_I R_{II} C_c} = \frac{g_m I}{C_c} = \frac{g_m 1}{C_c} = \frac{g_m 2}{C_c}$$

Conceptually, where do these roots come from?

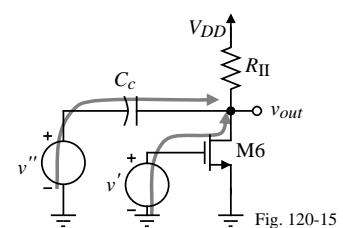
1.) The Miller pole:

$$|p_1| \approx \frac{1}{R_I(g_m 6 R_{II} C_c)}$$



2.) The left-half plane output pole:

$$|p_2| \approx \frac{g_m 6}{C_{II}}$$



3.) Right-half plane zero (*One source of zeros is from multiple paths from the input to output*):

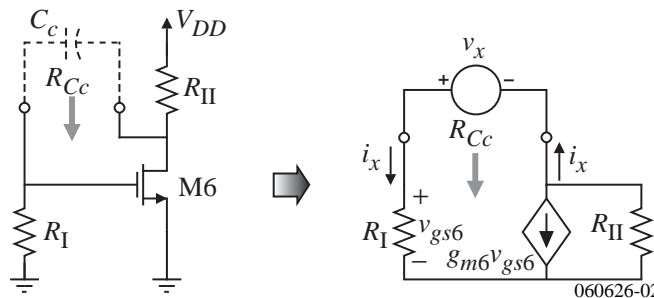
$$v_{out} = \left(\frac{-g_m 6 R_{II} (1/s C_c)}{R_{II} + 1/s C_c} \right) v' + \left(\frac{R_{II}}{R_{II} + 1/s C_c} \right) v'' = \frac{-R_{II} \left(\frac{g_m 6}{s C_c} - 1 \right)}{R_{II} + 1/s C_c} v$$

where $v = v' = v''$.

Further Comments on p_2

The previous observations on p_2 can be proved as follows:

Find the resistance R_{Cc} seen by the compensation capacitor, C_c .



$$v_x = i_x R_I + (i_x + g_{m6} v_{gs6}) R_{II} = i_x R_I + (i_x + g_{m6} i_x R_I) R_{II}$$

Therefore,

$$R_{Cc} = \frac{v_x}{i_x} = R_I + (1 + g_{m6} R_I) R_{II} \approx g_{m6} R_I R_{II}$$

The frequency at which C_c begins to become a short is,

$$\frac{1}{\omega C_c} < g_{m6} R_I R_{II} \quad \text{or} \quad \omega > \frac{1}{g_{m6} R_I R_{II} C_c} \approx |p_1|$$

Thus, at the frequency where C_{II} begins to short the output, C_c is acting as a short.

Influence of the Mirror Pole

Up to this point, we have neglected the influence of the pole, p_3 , associated with the current mirror of the input stage. A small-signal model for the input stage that includes C_3 is shown below:

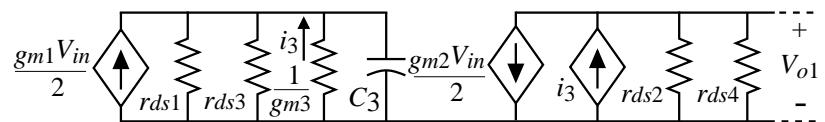


Fig. 120-16

The transfer function from the input to the output voltage of the first stage, $V_{o1}(s)$, can be written as

$$\frac{V_{o1}(s)}{V_{in}(s)} = \frac{-g_{m1}}{2(g_{ds2}+g_{ds4})} \left[\frac{g_{m3}+g_{ds1}+g_{ds3}}{g_{m3}+g_{ds1}+g_{ds3}+sC_3} + 1 \right] \approx \frac{-g_{m1}}{2(g_{ds2}+g_{ds4})} \left[\frac{sC_3 + 2g_{m3}}{sC_3 + g_{m3}} \right]$$

We see that there is a pole and a zero given as

$$p_3 = -\frac{g_{m3}}{C_3} \quad \text{and} \quad z_3 = -\frac{2g_{m3}}{C_3}$$

Summary of the Conditions for Stability of the Two-Stage Op Amp

- Unity-gainbandwidth is given as:

$$GB = A_v(0) \cdot |p_1| = (g_{mI} g_{mII} R_I R_{II}) \cdot \left(\frac{1}{g_{mII} R_I R_{II} C_c} \right) = \frac{g_{mI}}{C_c} = (g_{m1} g_{m2} R_1 R_2) \cdot \left(\frac{1}{g_{m2} R_1 R_2 C_c} \right) = \frac{g_{m1}}{C_c}$$

- The requirement for 45° phase margin is:

$$\pm 180^\circ - \text{Arg}[\text{Loop Gain}] = \pm 180^\circ - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45^\circ$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180^\circ - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45^\circ$$

$$135^\circ \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90^\circ + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7^\circ$$

$$39.3^\circ \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow |p_2| \geq 1.22GB$$

- The requirement for 60° phase margin:

$$|p_2| \geq 2.2GB \text{ if } z \geq 10GB$$

- If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{m6}}{C_c} > \frac{10g_{m1}}{C_c} \Rightarrow g_{m6} > 10g_{m1} \quad \text{and} \quad \frac{g_{m6}}{C_2} > \frac{2.2g_{m1}}{C_c} \Rightarrow C_c > 0.22C_2$$

OTHER FORMS OF COMPENSATION

Feedforward Compensation

Use two parallel paths to achieve a LHP zero for lead compensation purposes.

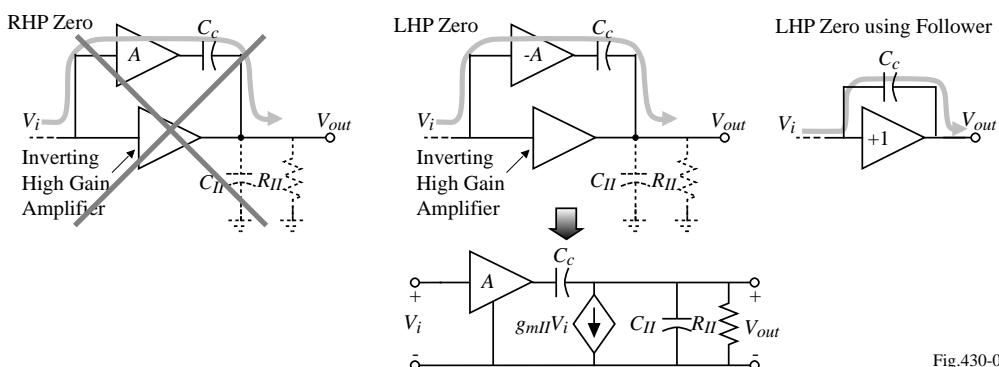


Fig.430-09

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{AC_c}{C_c + C_{II}} \left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]} \right)$$

To use the LHP zero for compensation, a compromise must be observed.

- Placing the zero below GB will lead to boosting of the loop gain that could deteriorate the phase margin.
- Placing the zero above GB will have less influence on the leading phase caused by the zero.

Note that a source follower is a good candidate for the use of feedforward compensation.

Self-Compensated Op Amps

Self compensation occurs when the load capacitor is the compensation capacitor (can never be unstable for resistive feedback)

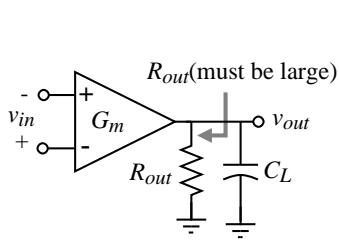
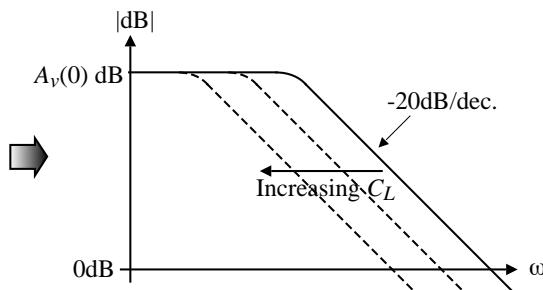


Fig. 430-10



Voltage gain:

$$\frac{v_{out}}{v_{in}} = A_v(0) = G_m R_{out}$$

Dominant pole:

$$p_1 = \frac{-1}{R_{out} C_L}$$

Unity-gainbandwidth:

$$GB = A_v(0) \cdot |p_1| = \frac{G_m}{C_L}$$

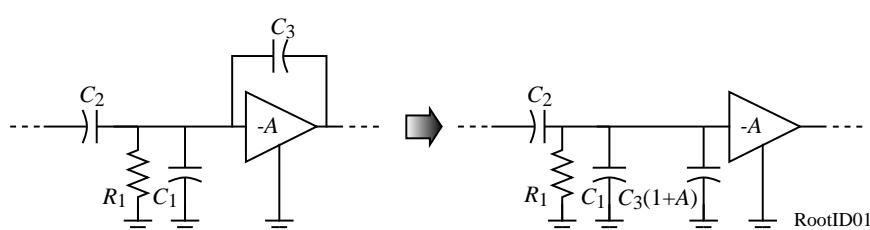
Stability:

Large load capacitors simply reduce GB but the phase is still 90° at GB .

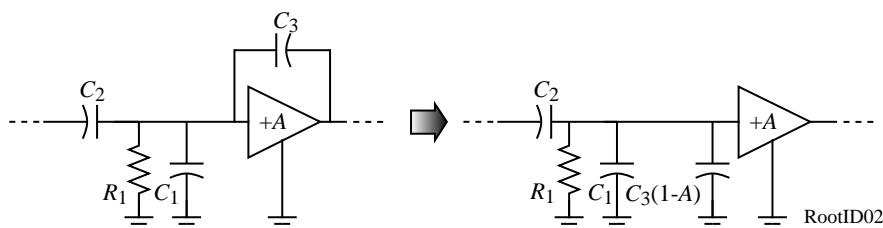
FINDING ROOTS BY INSPECTION

Identification of Poles from a Schematic

- 1.) Most poles are equal to the reciprocal product of the resistance from a node to ground and the capacitance connected to that node.
- 2.) Exceptions (generally due to feedback):
 - a.) Negative feedback:



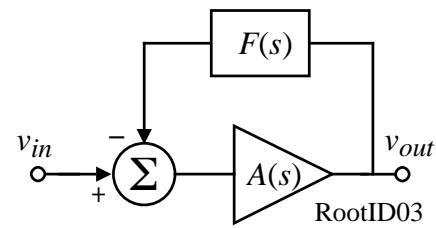
b.) Positive feedback ($A < 1$):



Identification of Zeros from a Schematic

1.) Zeros arise from poles in the feedback path.

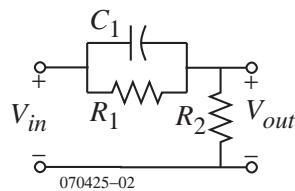
$$\text{If } F(s) = \frac{1}{\frac{s}{p_1} + 1},$$



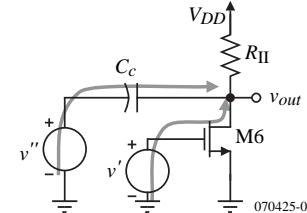
$$\text{then } \frac{V_{out}}{V_{in}} = \frac{A(s)}{1+A(s)F(s)} = \frac{A(s)}{1+A(s)\frac{1}{\frac{s}{p_1} + 1}} = \frac{A(s)\left(\frac{s}{p_1} + 1\right)}{\frac{s}{p_1} + 1 + A(s)}$$

2.) Zeros are also created by two paths from the input to the output and one of more of the paths is frequency dependent.

3.) Zeros also come from simple RC networks.



$$\frac{V_{out}}{V_{in}} = \frac{s + 1/(R_1 C_1)}{s + 1/(R_1 || R_2) C_1}$$



CMOS Analog Circuit Design

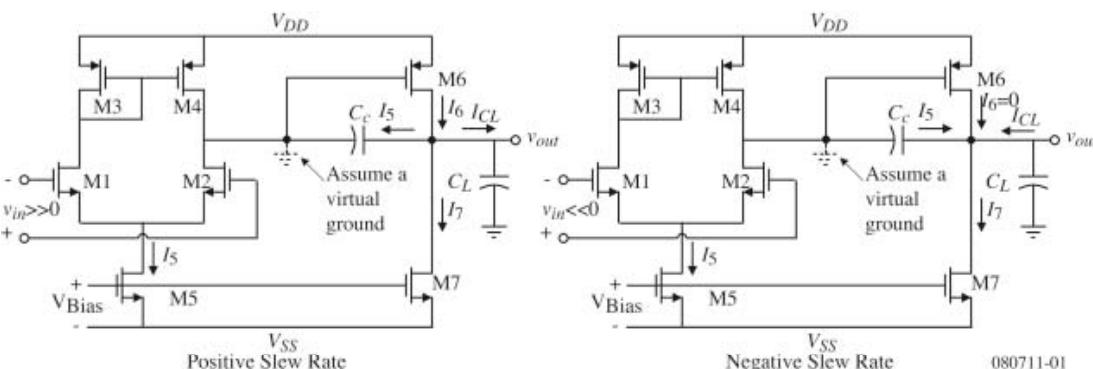
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CMOS OP AMP SLEW RATE

Slew Rate of a Two-Stage CMOS Op Amp

Remember that slew rate occurs when currents flowing in a capacitor become limited and is given as

$$I_{lim} = C \frac{dv_C}{dt} \text{ where } v_C \text{ is the voltage across the capacitor } C.$$



$$SR^+ = \min\left[\frac{I_5}{C_c}, \frac{I_6 - I_5 - I_7}{C_L}\right] = \frac{I_5}{C_c} \text{ because } I_6 \gg I_5 \quad SR^- = \min\left[\frac{I_5}{C_c}, \frac{I_7 - I_5}{C_L}\right] = \frac{I_5}{C_c} \text{ if } I_7 \gg I_5.$$

Therefore, if C_L is not too large and if I_7 is significantly greater than I_5 , then the slew rate of the two-stage op amp should be, I_5/C_c .

SUMMARY

- Op amps achieve accuracy by using negative feedback
- Compensation is required to insure that the feedback loop is stable
- The degree of stability is measured by phase margin and is necessary to achieve small settling times
- A compensated op amp will have one dominant pole and all other poles will be greater than GB
- A two-stage op amp requires some form of Miller compensation
- A high output resistance op amp is compensated by the load capacitor
- Poles of a CMOS circuit are generally equal to the negative reciprocal of the product of the resistance to ground from a node times the sum of the capacitances connected to that node.
- The slew rate of the two-stage op amp is equal to the input differential stage current sink/source divided by the Miller capacitor

LECTURE 230 – DESIGN OF TWO-STAGE OP AMPS

LECTURE OUTLINE

Outline

- Steps in Designing an Op Amp
- Design Procedure for a Two-Stage Op Amp
- Design Example of a Two-Stage Op Amp
- Right Half Plane Zero
- PSRR of the Two-Stage Op Amp
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 269-293

STEPS IN DESIGNING A CMOS OP AMP

Steps

- 1.) Choosing or creating the basic structure of the op amp.
This step results in a schematic showing the transistors and their interconnections.
This diagram does not change throughout the remainder of the design unless the specifications cannot be met, then a new or modified structure must be developed.
- 2.) Selection of the dc currents and transistor sizes.
Most of the effort of design is in this category.
Simulators are used to aid the designer in this phase.
- 3.) Physical implementation of the design.
Layout of the transistors
Floorplanning the connections, pin-outs, power supply buses and grounds
Extraction of the physical parasitics and re-simulation
Verification that the layout is a physical representation of the circuit.
- 4.) Fabrication
- 5.) Measurement
Verification of the specifications
Modification of the design as necessary

Design Inputs

Boundary conditions:

1. Process specification (V_T , K' , C_{ox} , etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

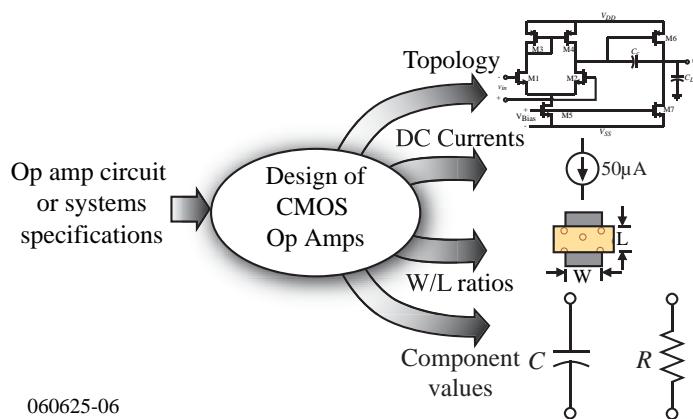
Requirements:

1. Gain
2. Gain bandwidth
3. Settling time
4. Slew rate
5. Common-mode input range, $ICMR$
6. Common-mode rejection ratio, $CMRR$
7. Power-supply rejection ratio, $PSRR$
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

Outputs of Op Amp Design

The basic outputs of design are:

- 1.) The topology
- 2.) The dc currents
- 3.) The W and L values of transistors
- 4.) The values of components



Some Practical Thoughts on Op Amp Design

- 1.) Decide upon a suitable topology.
 - Experience is a great help
 - The topology should be the one capable of meeting most of the specifications
 - Try to avoid “inventing” a new topology but start with an existing topology
- 2.) Determine the type of compensation needed to meet the specifications.
 - Consider the load and stability requirements
 - Use some form of Miller compensation or a self-compensated approach
- 3.) Design dc currents and device sizes for proper dc, ac, and transient performance.
 - This begins with hand calculations based upon approximate design equations.
 - Compensation components are also sized in this step of the procedure.
 - After each device is sized by hand, a circuit simulator is used to fine tune the design

Two basic steps of design:

- 1.) “First-cut” - this step is to use hand calculations to propose a design that has potential of satisfying the specifications. Design robustness is developed in this step.
- 2.) Optimization - this step uses the computer to refine and optimize the design.

A DESIGN PROCEDURE FOR THE TWO-STAGE CMOS OP AMP

Unbuffered, Two-Stage CMOS Op Amp

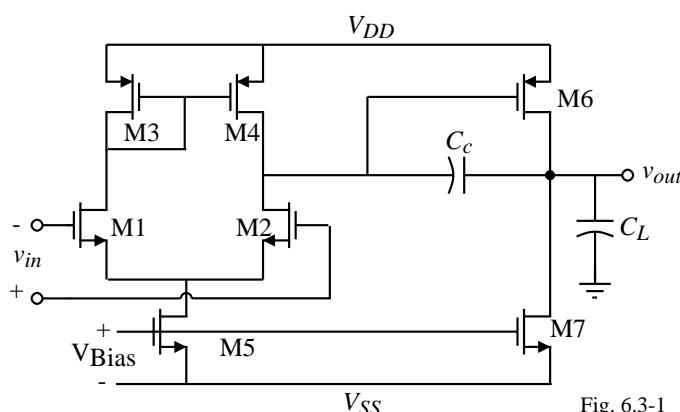


Fig. 6.3-1

Notation:

$$S_i = \frac{W_i}{L_i} = W/L \text{ of the } i\text{th transistor}$$

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

1.) First assume that $V_{SG4} = V_{SG6}$. This will cause “proper mirroring” in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is “guaranteed” to be in saturation.

$$2.) \text{ If } V_{SG4} = V_{SG6}, \text{ then } I_6 = \left(\frac{S_6}{S_4}\right) I_4$$

$$3.) \text{ However, } I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right) (2I_4)$$

$$4.) \text{ For balance, } I_6 \text{ must equal } I_7 \Rightarrow \boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}} \text{ called the “balance conditions”}$$

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

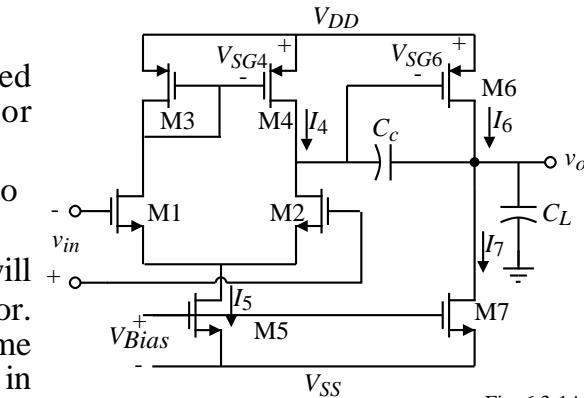


Fig. 6.3-1A

Summary of the Design Relationships for the Two-Stage Op Amp

$$\text{Slew rate } SR = \frac{I_5}{C_c} \text{ (Assuming } I_7 \gg I_5 \text{ and } C_L > C_c\text{)}$$

$$\text{First-stage gain } A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(l_2 + l_4)}$$

$$\text{Second-stage gain } A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(l_6 + l_7)}$$

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c}$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L}$$

$$\text{RHP zero } z_1 = \frac{g_{m6}}{C_c}$$

60° phase margin requires that $g_{m6} = 2.2g_{m2}(C_L/C_c)$ if all other roots are $\geq 10GB$.

$$\text{Positive ICMR } V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{b_3}} - |V_{T03}|_{(max)} + V_{T1(min)}$$

$$\text{Negative ICMR } V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{b_1}} + V_{T1(max)} + V_{DS5(sat)}$$

Op Amp Specifications

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, GB
3. Phase margin (or settling time)
4. Input common-mode range, ICMR
5. Load Capacitance, C_L
6. Slew-rate, SR
7. Output voltage swing
8. Power dissipation, P_{diss}

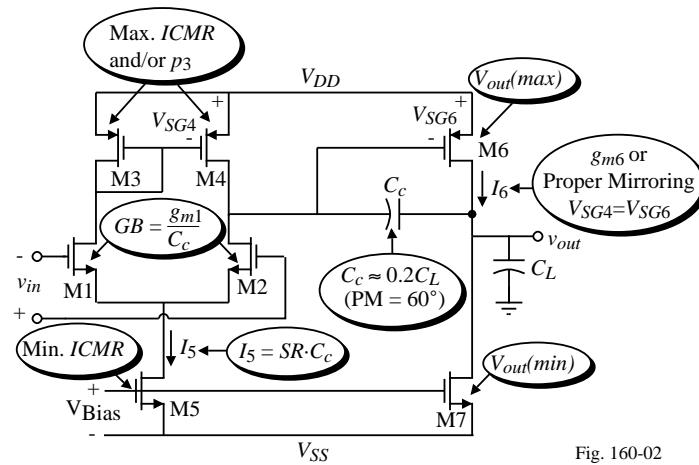


Fig. 160-02

Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range ($V_{in}(min)$ and $V_{in}(max)$), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing ($V_{out}(max)$ and $V_{out}(min)$), and power dissipation (P_{diss}) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, choose the minimum value for C_c , i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > 0.22C_L$$

2. Determine the minimum value for the “tail current” (I_5) from

$$I_5 = SR \cdot C_c$$

3. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(max) - |V_{T03}|(max) + V_{T1}(min)]^2}$$

4. Verify that the pole of M3 due to C_{gs3} and C_{gs4} ($= 0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than $10 GB$

$$\frac{gm_3}{2C_{gs3}} > 10GB.$$

Unbuffered Op Amp Design Procedure - Continued

5. Design for S_1 (S_2) to achieve the desired GB .

$$g_{m1} = GB \cdot C_c \rightarrow S_2 = \frac{g_{m1}^2}{K'_1 I_5}$$

6. Design for S_5 from the minimum input voltage. First calculate $V_{DS5}(\text{sat})$ then find S_5 .

$$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV} \rightarrow S_5 = \frac{2I_5}{K'_5 [V_{DS5}(\text{sat})]^2}$$

7. Find S_6 by letting the second pole (p_2) be equal to 2.2 times GB and assuming that $V_{SG4} = V_{SG6}$.

$$g_{m6} = 2.2g_{m2}(C_L/C_c) \quad \text{and} \quad \frac{g_{m6}}{g_{m4}} = \frac{\sqrt{2K_P S_6 I_6}}{\sqrt{2K_P S_4 I_4}} = \sqrt{\frac{S_6 I_6}{S_4 I_4}} = \frac{S_6}{S_4} \rightarrow S_6 = \frac{g_{m6}}{g_{m4}} S_4$$

8. Calculate I_6 from

$$I_6 = \frac{g_{m6}^2}{2K'_6 S_6}$$

Check to make sure that S_6 satisfies the $V_{out}(\text{max})$ requirement and adjust as necessary.

9. Design S_7 to achieve the desired current ratios between I_5 and I_6 .

$$S_7 = (I_6/I_5)S_5 \quad (\text{Check the minimum output voltage requirements})$$

Unbuffered Op Amp Design Procedure - Continued

10. Check gain and power dissipation specifications.

$$A_V = \frac{2g_{m2}g_{m6}}{I_5(l_2 + l_4)I_6(l_6 + l_7)} \quad P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

11. If the gain specification is not met, then the currents, I_5 and I_6 , can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they are satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6 . Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.

12. Simulate the circuit to check to see that all specifications are met.

DESIGN EXAMPLE OF A TWO-STAGE OP AMP

Example 230-1 - Design of a Two-Stage Op Amp

If $K_N' = 120 \mu\text{A/V}^2$, $K_P' = 25 \mu\text{A/V}^2$, $V_{TN} = |V_{TP}| = 0.5\text{V}$, $\lambda_N = 0.06\text{V}^{-1}$, and $\lambda_P = 0.08\text{V}^{-1}$, design a two-stage, CMOS op amp that meets the following specifications. Assume the channel length is to be $0.5\mu\text{m}$ and the load capacitor is $C_L = 10\text{pF}$.

$$A_V > 3000\text{V/V} \quad V_{DD} = 2.5\text{V} \quad GB = 5\text{MHz} \quad SR > 10\text{V}/\mu\text{s}$$

$$60^\circ \text{ phase margin} \quad 0.5\text{V} < V_{out} \text{ range} < 2\text{V} \quad ICMR = 1.25\text{V to } 2\text{V} \quad P_{diss} \leq 2\text{mW}$$

Solution

1.) The first step is to calculate the minimum value of the compensation capacitor C_c ,

$$C_c > (2.2/10)(10 \text{ pF}) = 2.2 \text{ pF}$$

2.) Choose C_c as 3pF . Using the slew-rate specification and C_c calculate I_5 .

$$I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30 \mu\text{A}$$

3.) Next calculate $(W/L)_3$ using ICMR requirements (use worst case thresholds $\pm 0.15\text{V}$).

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(25 \times 10^{-6})[2.5 - 2 - .65 + 0.35]^2} = 30 \quad \rightarrow \quad (W/L)_3 = (W/L)_4 = 30$$

Example 230-1 - Continued

4.) Now we can check the value of the mirror pole, p_3 , to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 6\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = -1.25 \times 10^9 (\text{rads/sec})$$

or 199 MHz . Thus, p_3 , is not of concern in this design because $p_3 \gg 10GB$.

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25 \mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K'_N I_1} = \frac{(94.25)^2}{2 \cdot 120 \cdot 15} = 2.47 \approx 3.0 \Rightarrow (W/L)_1 = (W/L)_2 = 3$$

6.) Next calculate V_{DS5} ,

$$V_{DS5} = 1.25 - \sqrt{\frac{30 \times 10^{-6}}{120 \times 10^{-6} \cdot 3}} - .65 = 0.31\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(120 \times 10^{-6})(0.31)^2} = 5.16 \approx 6 \quad \rightarrow \quad (W/L)_5 = 6$$

Example 230-1 - Continued

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$ and knowing that $g_{m4} = 150\mu\text{S}$, we calculate $(W/L)_6$ as

$$(W/L)_6 = 30 \frac{942.5 \times 10^{-6}}{(150 \times 10^{-6})} = 188.5 \approx 190 \quad (W/L)_6 = 190$$

8.) Calculate I_6 using the small-signal g_m expression:

$$I_6 = \frac{(942.5 \times 10^{-6})^2}{(2)(25 \times 10^{-6})(188.5)} = 94.2\mu\text{A} \approx 95\mu\text{A}$$

Calculating $(W/L)_6$ based on $V_{out}(\max)$, gives a value of 15. Since 190 exceeds the specification and gives better phase margin, we choose $(W/L)_6 = 190$ and $I_6 = 95\mu\text{A}$.

With $I_6 = 95\mu\text{A}$ the power dissipation is $P_{diss} = 2.5\text{V} \cdot (30\mu\text{A} + 95\mu\text{A}) = 0.3125\text{mW}$

9.) Finally, calculate $(W/L)_7$

$$(W/L)_7 = 6 \left(\frac{95 \times 10^{-6}}{30 \times 10^{-6}} \right) = 19 \approx 20 \rightarrow (W/L)_7 = 20$$

Let us check the $V_{out}(\min)$ specification although the W/L of M7 is so large that this is probably not necessary. The value of $V_{out}(\min)$ is

$$V_{out}(\min) = V_{DS7}(\text{sat}) = \sqrt{(2 \cdot 95)/(120 \cdot 20)} = 0.281\text{V}$$

which is less than required. At this point, the first-cut design is complete.

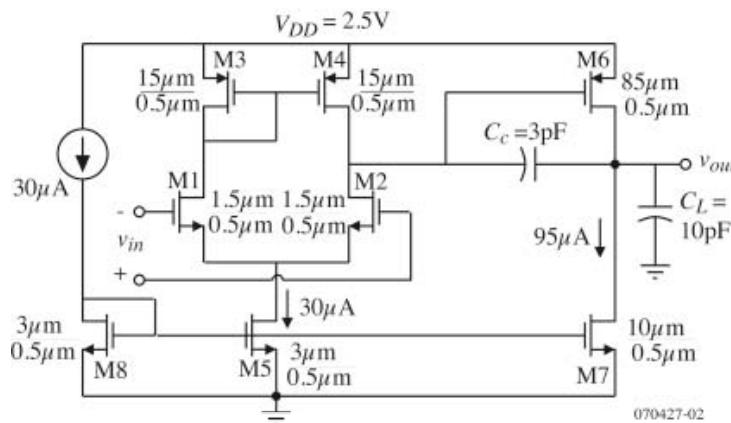
Example 230-1 - Continued

10.) Now check to see that the gain specification has been met

$$A_v = \frac{(94.25 \times 10^{-6})(942.5 \times 10^{-6})}{15 \times 10^{-6}(0.06 + 0.08)95 \times 10^{-6}(0.06 + 0.08)} = 3,180\text{V/V}$$

which barely exceeds the specifications. Since we are at $2xL_{min}$, it won't do any good to increase the channel lengths. Decreasing the currents or increasing W_6/L_6 will help.

The figure below shows the results of the first-cut design. The W/L ratios shown do not account for the lateral diffusion discussed above. The next phase requires simulation.

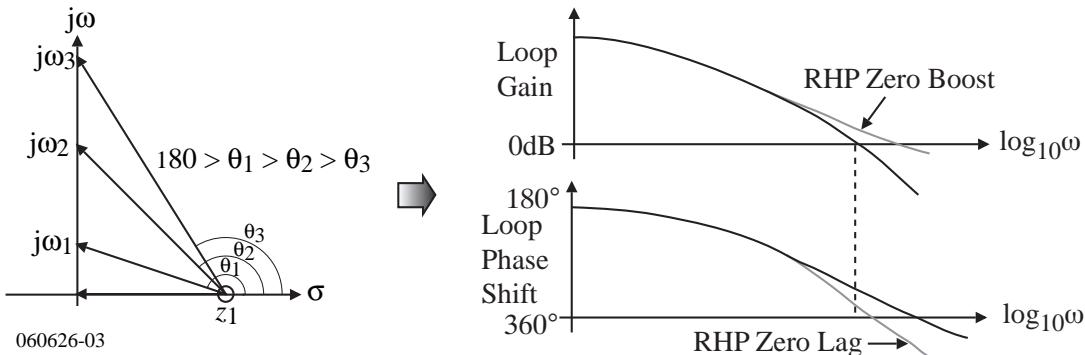


RIGHT-HALF PLANE ZERO

Controlling the Right-Half Plane Zero

Why is the RHP zero a problem?

Because it boosts the magnitude but lags the phase - the worst possible combination for stability.



Solution of the problem:

The compensation comes from the *feedback path* through C_C , but the RHP zero comes from the *feedforward path* through C_C so eliminate the feedforward path!

Use of Buffer to Eliminate the Feedforward Path through the Miller Capacitor

Model:

The transfer function is given by the following equation,

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_I C_I + R_{II} C_{II} + R_I C_c + g_{mII} R_I R_{II} C_c] + s^2 [R_I R_{II} C_{II} (C_I + C_c)]}$$

Using the technique as before to approximate p_1 and p_2 results in the following

$$p_1 \approx \frac{-1}{R_I C_I + R_{II} C_{II} + R_I C_c + g_{mII} R_I R_{II} C_c} \approx \frac{-1}{g_{mII} R_I R_{II} C_c}$$

and

$$p_2 \approx \frac{-g_{mII} C_c}{C_{II} (C_I + C_c)}$$

Comments:

Poles are approximately what they were before with the zero removed.

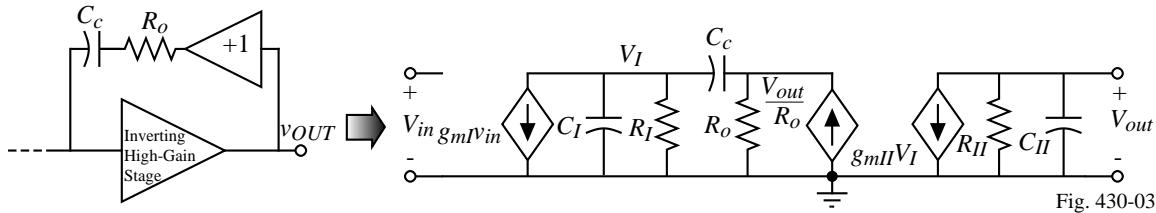
For 45° phase margin, $|p_2|$ must be greater than GB

For 60° phase margin, $|p_2|$ must be greater than $1.73GB$

Use of Buffer with Finite Output Resistance to Eliminate the RHP Zero

Assume that the unity-gain buffer has an output resistance of R_o .

Model:



It can be shown that if the output resistance of the buffer amplifier, R_o , is not neglected that another pole occurs at,

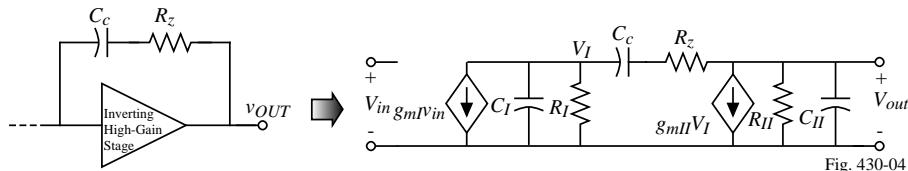
$$p_4 \approx \frac{-1}{R_o[C_I C_c / (C_I + C_c)]}$$

and a LHP zero at

$$z_2 \approx \frac{-1}{R_o C_c}$$

Closer examination shows that if a resistor, called a *nulling resistor*, is placed in series with C_c that the RHP zero can be eliminated or moved to the LHP.

Use of Nulling Resistor to Eliminate the RHP Zero (or turn it into a LHP zero)[†]



Nodal equations:

$$g_{mI}V_{in} + \frac{V_I}{R_I} + sC_I V_I + \left(\frac{sC_c}{1 + sC_c R_z} \right) (V_I - V_{out}) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{out} + \left(\frac{sC_c}{1 + sC_c R_z} \right) (V_{out} - V_I) = 0$$

Solution:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a \{ 1 - s[(C_c/g_{mII}) - R_z C_c] \}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_I R_{II}$$

$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_I R_{II}C_c + R_z C_c$$

$$c = [R_I R_{II} (C_I C_{II} + C_c C_I + C_c C_{II}) + R_z C_c (R_I C_I + R_{II} C_{II})]$$

$$d = R_I R_{II} R_z C_I C_{II} C_c$$

[†] W.J. Parrish, "An Ion Implanted CMOS Amplifier for High Performance Active Filters", Ph.D. Dissertation, 1976, Univ. of CA., Santa Barbara.

Use of Nulling Resistor to Eliminate the RHP - Continued

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots of the above transfer function can be approximated as

$$p_1 \approx \frac{-1}{(1 + g_{mII}R_{II})R_I C_c} \approx \frac{-1}{g_{mII}R_{II}R_I C_c}$$

$$p_2 \approx \frac{-g_{mII}C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \approx \frac{-g_{mII}}{C_{II}}$$

$$p_4 = \frac{-1}{R_z C_I}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

Note that the zero can be placed anywhere on the real axis.

A Design Procedure that Allows the RHP Zero to Cancel the Output Pole, p_2

We desire that $z_1 = p_2$ in terms of the previous notation.

Therefore,

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$

The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c} \right) (1/g_{mII})$$

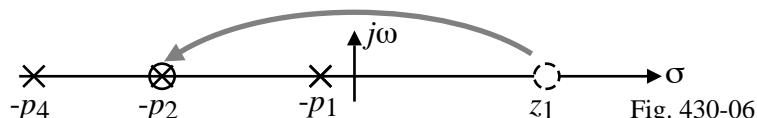


Fig. 430-06

With p_2 canceled, the remaining roots are p_1 and p_4 (the pole due to R_z). For unity-gain stability, all that is required is that

$$|p_4| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_I C_c} = \frac{g_{mI}}{C_c}$$

and $(1/R_z C_I) > (g_{mI}/C_c) = GB$

Substituting R_z into the above inequality and assuming $C_{II} \gg C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}}} C_I C_{II}$$

This procedure gives excellent stability for a fixed value of C_{II} ($\approx C_L$).

Unfortunately, as C_L changes, p_2 changes and the zero must be readjusted to cancel p_2 .

Incorporating the Nulling Resistor into the Miller Compensated Two-Stage Op Amp

Circuit:

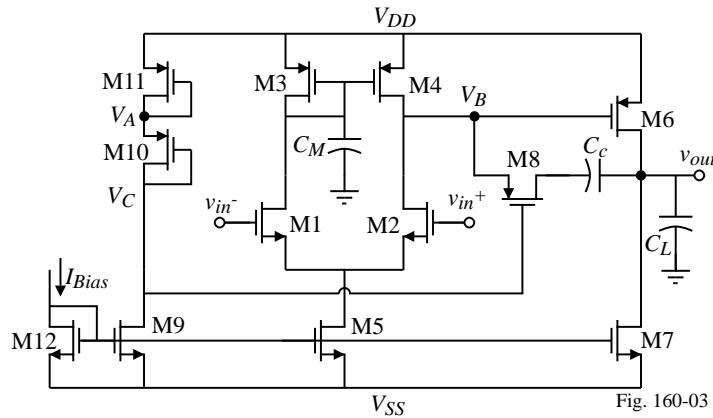


Fig. 160-03

We saw earlier that the roots were:

$$P_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \quad P_2 = -\frac{g_{m6}}{C_L}$$

$$P_4 = -\frac{1}{R_z C_I} \quad Z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}}$$

where $A_v = g_{m1}g_{m6}R_I R_{II}$.

(Note that P_4 is the pole resulting from the nulling resistor compensation technique.)

Design of the Nulling Resistor (M8)

For the zero to be on top of the second pole (P_2), the following relationship must hold

$$R_z = \frac{1}{g_{m6}} \left(\frac{C_L + C_c}{C_c} \right) = \left(\frac{C_c + C_L}{C_c} \right) \frac{1}{\sqrt{2K' P S_6 I_6}}$$

The resistor, R_z , is realized by the transistor M8 which is operating in the active region because the dc current through it is zero. Therefore, R_z , can be written as

$$R_z = \frac{\partial v_{DS8}}{\partial i_{D8}} \Big|_{V_{DS8}=0} = \frac{1}{K' P S_8 (V_{SG8} - |V_{TP}|)}$$

The bias circuit is designed so that voltage V_A is equal to V_B .

$$\therefore |V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \Rightarrow V_{SG11} = V_{SG6} \Rightarrow \left(\frac{W_{11}}{L_{11}} \right) = \left(\frac{I_{10}}{I_6} \right) \left(\frac{W_6}{L_6} \right)$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K' P (W_{10}/L_{10})}} = |V_{GS8}| - |V_T|$$

$$\therefore R_z = \frac{1}{K' P S_8} \sqrt{\frac{K' P S_{10}}{2I_{10}}} = \frac{1}{S_8} \sqrt{\frac{S_{10}}{2K' P I_{10}}}$$

Equating the two expressions for R_z gives $\left(\frac{W_8}{L_8} \right) = \left(\frac{C_c}{C_L + C_c} \right) \sqrt{\frac{S_{10} S_6 I_6}{I_{10}}}$

Example 230-2 - RHP Zero Compensation

Use results of Ex. 230-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2 . Use device data given in Ex. 230-1.

Solution

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10} . The first step in this design is to establish the bias components. In order to set V_A equal to V_B , then V_{SG11} must equal V_{SG6} . Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

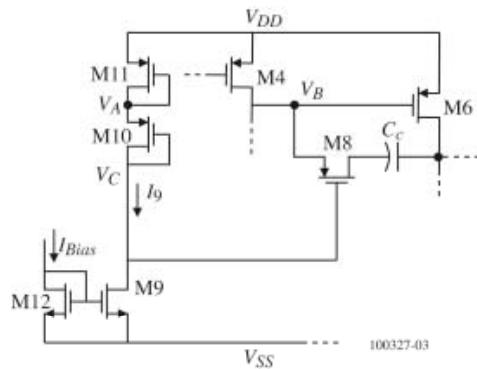
Choose $I_{11} = I_{10} = I_9 = 15\mu A$ which gives $S_{11} = (15\mu A/95\mu A)190 = 30$.

The aspect ratio of M10 is essentially a free parameter, and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11} , V_{SG10} , and V_{DS9} . The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(6) = 3$$

Now $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3\text{pF}}{3\text{pF} + 10\text{pF}} \right) \sqrt{\frac{1 \cdot 190 \cdot 95\mu A}{15\mu A}} = 8$$



Example 230-2 - Continued

It is worthwhile to check that the RHP zero has been moved on top of p_2 . To do this, first calculate the value of R_z . V_{SG8} must first be determined. It is equal to V_{SG10} , which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'P S_{10}}} + |V_{TP}| = \sqrt{\frac{2 \cdot 15}{25 \cdot 1}} + 0.5 = 1.595\text{V}$$

Next determine R_z .

$$R_z = \frac{1}{K'P S_8(V_{SG10}-|V_{TP}|)} = \frac{10^6}{25 \cdot 8(1.595 - 0.7)} = 4.564\text{k}\Omega$$

The location of z_1 is calculated as

$$z_1 = \frac{-1}{(4.564 \times 10^3)(3 \times 10^{-12}) - \frac{3 \times 10^{-12}}{950 \times 10^{-6}}} = -94.91 \times 10^6 \text{ rads/sec}$$

The output pole, p_2 , is

$$p_2 = -\frac{950 \times 10^{-6}}{10 \times 10^{-12}} = -95 \times 10^6 \text{ rads/sec}$$

Thus, we see that for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below where $L = 0.5\mu m$.

$$W_8 = 4\mu m \quad W_9/L_9 = 1.5\mu m \quad W_{10} = 0.5\mu m \quad \text{and} \quad W_{11} = 15\mu m$$

An Alternate Form of Nulling Resistor

To cancel p_2 ,

$$z_1 = p_2 \rightarrow R_z = \frac{C_c + C_L}{g_{m6A} C_C} = \frac{1}{g_{m6B}}$$

Which gives

$$g_{m6B} = g_{m6A} \left(\frac{C_c}{C_c + C_L} \right)$$

In the previous example,

$$g_{m6A} = 950 \mu\text{S}, C_c = 3 \text{pF}$$

and $C_L = 10 \text{pF}$.

Choose $I_{6B} = 10 \mu\text{A}$ to get

$$g_{m6B} = \frac{g_{m6A} C_c}{C_c + C_L} \rightarrow \sqrt{\frac{2K_p W_{6B} I_{6B}}{L_{6B}}} = \left(\frac{C_c}{C_c + C_L} \right) \sqrt{\frac{2K_p W_{6A} I_{6A}}{L_{6A}}}$$

or

$$\frac{W_{6B}}{L_{6B}} = \left(\frac{3}{13} \right)_2 \frac{I_{6A}}{I_{6B}} \frac{W_{6A}}{L_{6A}} = \left(\frac{3}{13} \right)_2 \left(\frac{95}{10} \right) (190) = 96.12 \rightarrow W_{6B} = 48 \mu\text{m}$$

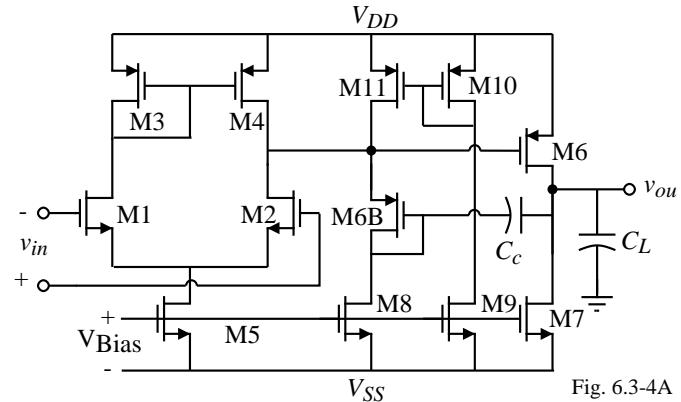
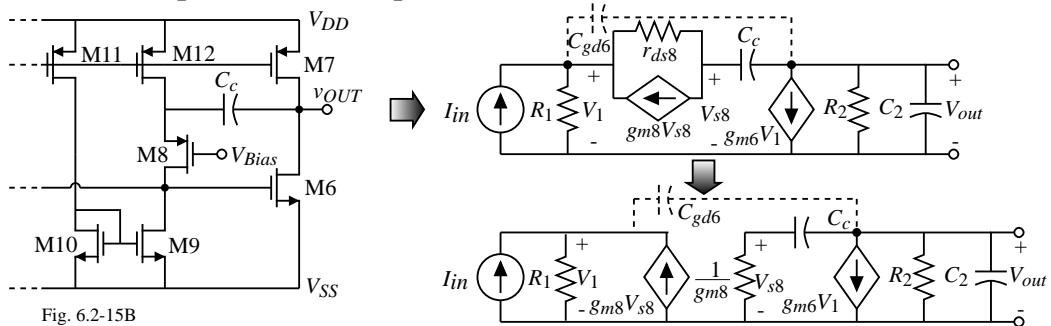


Fig. 6.3-4A

Increasing the Magnitude of the Output Pole[†]

The magnitude of the output pole, p_2 , can be increased by introducing gain in the Miller capacitor feedback path. For example,



The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \quad \text{and} \quad R_2 = \frac{1}{g_{ds6} + g_{ds7}}$$

where transistors M2 and M4 are the output transistors of the first stage.

Nodal equations:

$$I_{in} = G_1 V_1 - g_{m8} V_{s8} = G_1 V_1 - \left(\frac{g_{m8} s C_c}{g_{m8} + s C_c} \right) V_{out} \quad \text{and} \quad 0 = g_{m6} V_1 + \left[G_2 + s C_2 + \frac{g_{m8} s C_c}{g_{m8} + s C_c} \right] V_{out}$$

[†] B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE J. of Solid-State Circuits*, Vol. SC-18, No. 6 (Dec. 1983) pp. 629-633.

Increasing the Magnitude of the Output Pole - Continued

Solving for the transfer function V_{out}/I_{in} gives,

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_1 G_2} \right) \left[\frac{\left(1 + \frac{sC_c}{g_{m8}} \right)}{1 + s \left[\frac{C_c}{g_{m8}} + \frac{C_2}{G_2} + \frac{C_c}{G_2} + \frac{g_{m6} C_c}{G_1 G_2} \right] + s^2 \left(\frac{C_c C_2}{g_{m8} G_2} \right)} \right]$$

Using the approximate method of solving for the roots of the denominator gives

$$p_1 = \frac{-1}{\frac{C_c}{g_{m8}} + \frac{C_c}{G_2} + \frac{C_2}{G_2} + \frac{g_{m6} C_c}{G_1 G_2}} \approx \frac{-6}{g_{m6} r_{ds}^2 C_c}$$

$$\text{and } p_2 \approx \frac{-\frac{g_{m6} r_{ds}^2 C_c}{6}}{\frac{C_c C_2}{g_{m8} G_2}} = \frac{g_{m8} r_{ds}^2 G_2}{6} \left(\frac{g_{m6}}{C_2} \right) = \left(\frac{g_{m8} r_{ds}}{3} \right) |p_2|'$$

where all the various channel resistance have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation.

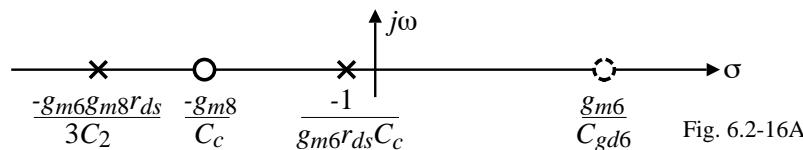
Result:

Dominant pole is approximately the same and the output pole is increased by $\approx g_m r_{ds}$.

Increasing the Magnitude of the Output Pole - Continued

In addition there is a LHP zero at $-g_{m8}/sC_c$ and a RHP zero due to C_{gd6} (shown dashed in the previous model) at g_{m6}/C_{gd6} .

Roots are:

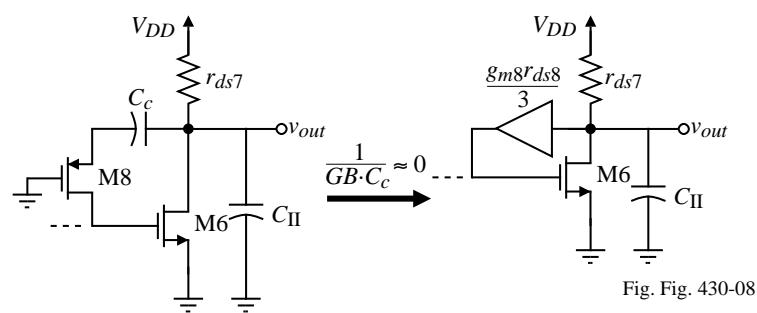


Concept:

$$R_{out} = r_{ds7} \parallel \left(\frac{3}{g_{m6} g_{m8} r_{ds8}} \right) \approx \frac{3}{g_{m6} g_{m8} r_{ds8}}$$

Therefore, the output pole is approximately,

$$|p_2| \approx \frac{g_{m6} g_{m8} r_{ds8}}{3C_{II}}$$



POWER SUPPLY REJECTION RATIO OF THE TWO-STAGE OP AMP

What is PSRR?

$$PSRR = \frac{A_v(V_{dd}=0)}{A_{dd}(V_{in}=0)}$$

How do you calculate PSRR?

You could calculate A_v and A_{dd} and divide, however

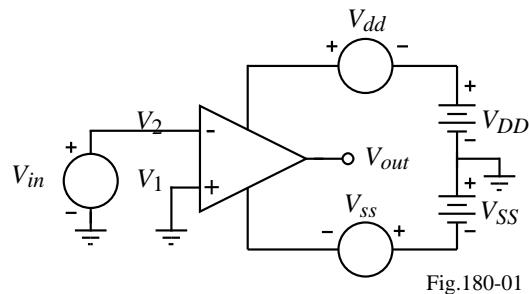


Fig. 180-01

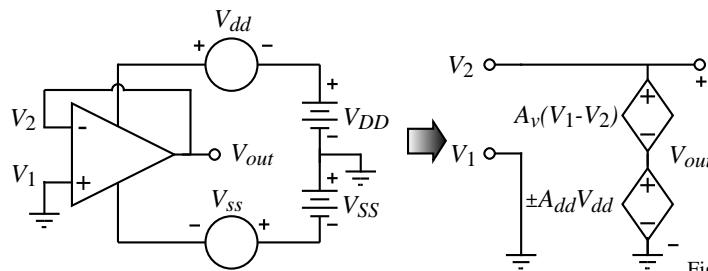


Fig. 180-02

$$V_{out} = A_{dd}V_{dd} + A_v(V_1 - V_2) = A_{dd}V_{dd} - A_vV_{out} \rightarrow V_{out}(1 + A_v) = A_{dd}V_{dd}$$

$$\therefore \frac{V_{out}}{V_{dd}} = \frac{A_{dd}}{1 + A_v} \approx \frac{A_{dd}}{A_v} = \frac{1}{PSRR^+} \quad (\text{Good for frequencies up to } GB)$$

Approximate Model for PSRR⁺

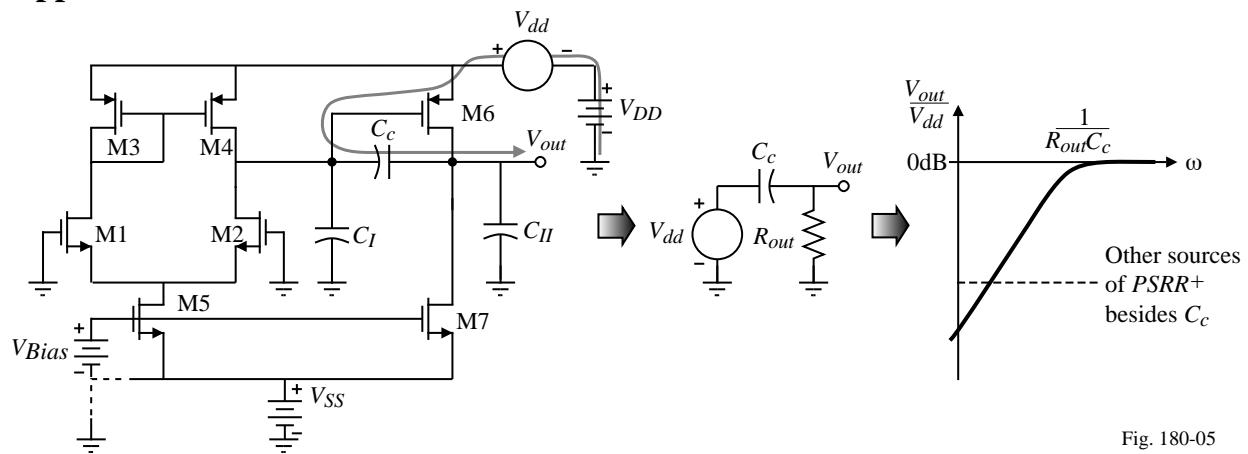
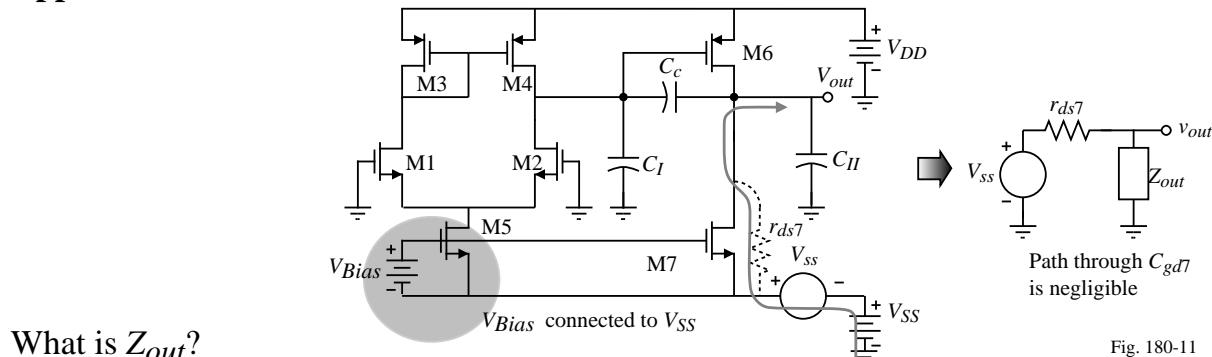


Fig. 180-05

- 1.) The M7 current sink causes V_{SG6} to act like a battery.
 - 2.) Therefore, V_{dd} couples from the source to gate of M6.
 - 3.) The path to the output is through any capacitance from gate to drain of M6.
- Conclusion:
- The Miller capacitor C_c couples the positive power supply ripple directly to the output.
Must reduce or eliminate C_c .

Approximate Model for PSRR-

$$Z_{out} = \frac{V_t}{I_t} \Rightarrow I_t = g_{mII} V_1 = g_{mII} \left(\frac{g_m I V_t}{G_I + s C_I + s C_c} \right)$$

$$\text{Thus, } Z_{out} = \frac{G_I + s(C_I + C_c)}{g_{mI} g_{mII}}$$

∴

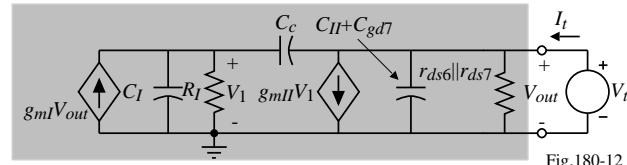


Fig. 180-11

$$\frac{V_{out}}{V_{ss}} = \frac{1 + \frac{r_{ds7}}{Z_{out}}}{1} = \frac{s(C_c + C_I) + G_I + g_{mI} g_{mII} r_{ds7}}{s(C_c + C_I) + G_I} \Rightarrow \text{Pole at } \frac{-G_I}{C_c + C_I}$$

The negative PSRR is much better than the positive PSRR.

CMOS Analog Circuit Design

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SUMMARY

- The output of the design of an op amp is
 - Schematic
 - DC currents
 - W/L ratios
 - Component values
- Design procedures provide an organized approach to creating the dc currents, W/L ratios, and the component values
- The right-half plane zero causes the Miller compensation to deteriorate
- Methods for eliminating the influence of the RHP zero are:
 - Nulling resistor
 - Increasing the magnitude of the output pole
- The PSRR of the two-stage op amp is poor because of the Miller capacitance, however, methods exist to eliminate this problem
- The two-stage op amp is a very general and flexible op amp

LECTURE 240 – CASCODE OP AMPS

LECTURE ORGANIZATION

Outline

- Lecture Organization
- Single Stage Cascode Op Amps
- Two Stage Cascode Op Amps
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 293-310

Cascode Op Amps

Why cascode op amps?

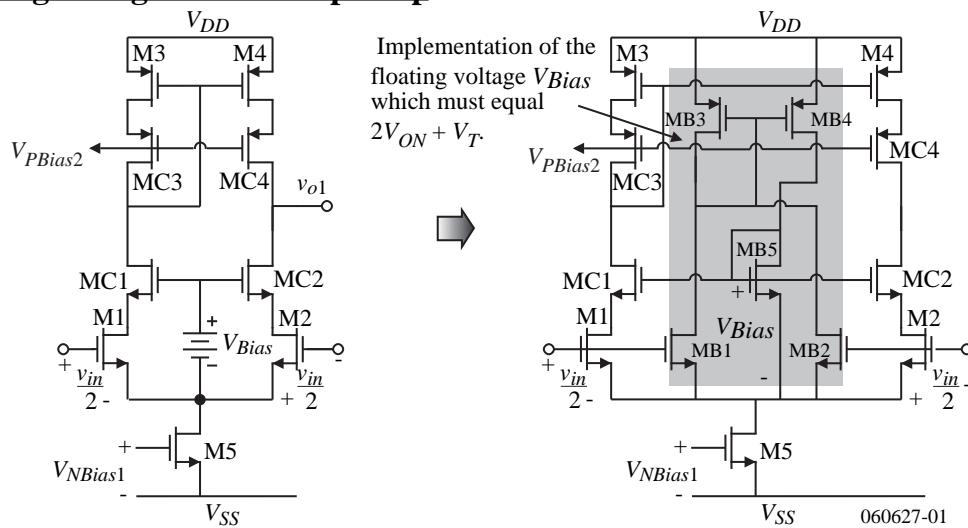
- Control of the frequency behavior
- Can get more gain by increasing the output resistance of a stage
- In the past section, *PSRR* of the two-stage op amp was insufficient for many applications
- A two-stage op amp can become unstable for large load capacitors (if nulling resistor is not used)
- The cascode op amp leads to wider *ICMR* and/or smaller power supply requirements

Where Should the Cascode Technique be Used?

- First stage -
 - Good noise performance
 - Requires level translation to second stage
 - Degrades the Miller compensation
- Second stage -
 - Self compensating
 - Increases the efficiency of the Miller compensation
 - Increases *PSRR*

SINGLE STAGE CASCODE OP AMPS

Simple Single Stage Cascode Op Amp



R_{out} of the first stage is $R_I \approx (g_m C_2 r_{ds2} C_2 r_{ds2}) \parallel (g_m C_4 r_{ds4} C_4 r_{ds4})$

Voltage gain $= \frac{v_{o1}}{v_{in}} = g_m R_I$ [The gain is increased by approximately 0.5($g_M C r_{ds} C$)]

As a single stage op amp, the compensation capacitor becomes the load capacitor.

Example 240-1 Single-Stage, Cascode Op Amp Performance

Assume that all W/L ratios are $10 \mu\text{m}/1 \mu\text{m}$, and that $I_{DS1} = I_{DS2} = 50 \mu\text{A}$ of single stage op amp. Find the voltage gain of this op amp and the value of C_L if $GB = 10 \text{ MHz}$. Use $K_N' = 120 \mu\text{A/V}^2$, $K_P' = 25 \mu\text{A/V}^2$, $V_{TN} = 0.5 \text{ V}$, $V_{TP} = -0.5 \text{ V}$, $\lambda_N = 0.06 \text{ V}^{-1}$ and $\lambda_P = 0.08 \text{ V}^{-1}$.

Solution

The device transconductances are

$$g_{m1} = g_{m2} = g_{mI} = 346.4 \mu\text{S}$$

$$g_{mC1} = g_{mC2} = 346.4 \mu\text{S}$$

$$g_{mC3} = g_{mC4} = 158.1 \mu\text{S}.$$

The output resistance of the NMOS and PMOS devices is $0.333 \text{ M}\Omega$ and $0.25 \text{ M}\Omega$, respectively.

$$\therefore R_I = 7.86 \text{ M}\Omega$$

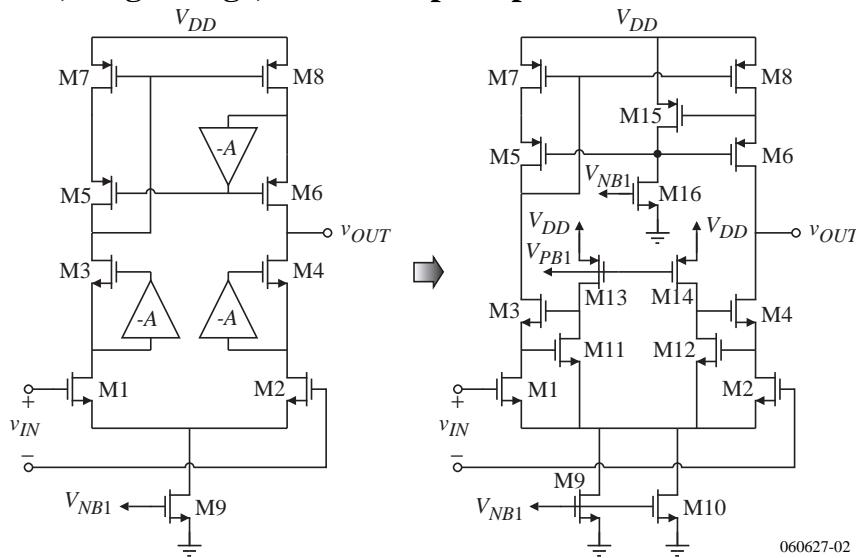
$$A_V(0) = 2,722 \text{ V/V.}$$

For a unity-gain bandwidth of 10 MHz , the value of C_L is 5.51 pF .

What happens if a 100 pF capacitor is attached to this op amp?

GB goes from 10 MHz to 0.551 MHz .

Enhanced Gain, Single Stage, Cascode Op Amp



From inspection, we can write the voltage gain as,

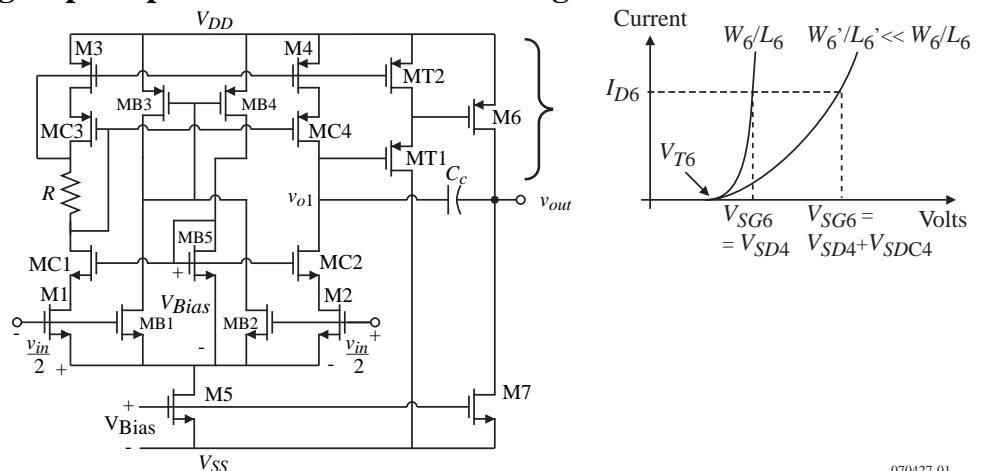
$$A_v = \frac{v_{OUT}}{v_{IN}} = g_m R_{out} \quad \text{where } R_{out} = (A r_{ds6} g_m r_{ds8}) \parallel (A r_{ds2} g_m r_{ds4})$$

Since $A \approx g_m r_{ds}/2$ the voltage gain would be equal to 100,000 to 500,000.

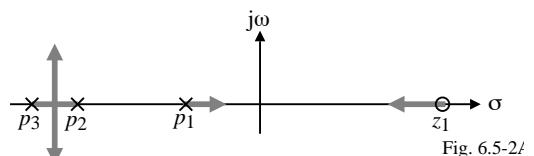
Output is not optimized for maximum signal swing.

TWO-STAGE, CASCODE OP AMPS

Two-Stage Op Amp with a Cascoded First-Stage



- MT1 and MT2 are required for level shifting from the first-stage to the second.
- The PSRR⁺ is improved by the presence of MT1
- Internal loop pole at the gate of M6 may cause the Miller compensation to fail.
- The voltage gain of this op amp could easily be 100,000V/V



Two-Stage Op Amp with a Cascode Second-Stage

$$A_v = g_{mI}g_{mII}R_I R_{II}$$

where $g_{mI} = g_{m1} = g_{m2}$, $g_{mII} = g_{m6}$,

$$R_I = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{D5}}$$

and

$$R_{II} = (g_{mC6}r_{dsC6}r_{ds6}) \parallel (g_{mC7}r_{dsC7}r_{ds7})$$

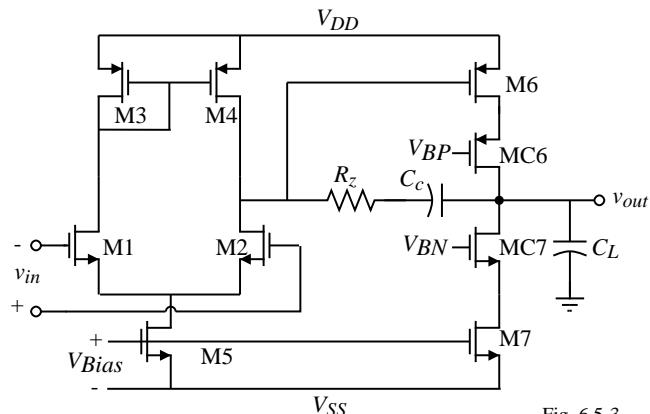
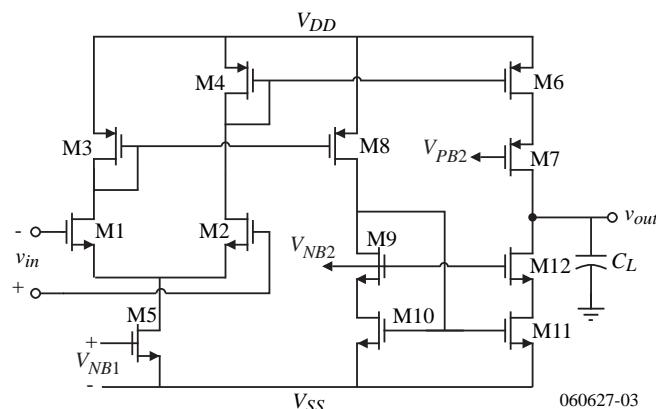


Fig. 6.5-3

Comments:

- The second-stage gain has greatly increased improving the Miller compensation
- The overall gain is approximately $(g_m r_{ds})^3$ or very large
- Output pole, p_2 , is approximately the same if C_c is constant
- The zero RHP is the same if C_c is constant
- PSRR is poor unless the Miller compensation is removed (then the op amp becomes self compensated)

A Balanced, Two-Stage Op Amp using a Cascode Output Stage



$$v_{out} = \left(\frac{g_{m1}g_{m8}}{g_{m3}} \frac{v_{in}}{2} + \frac{g_{m2}g_{m6}}{g_{m4}} \frac{v_{in}}{2} \right) R_{II}$$

$$= \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2} \right) k v_{in} R_{II} = g_{m1} \cdot k \cdot R_{II} v_{in}$$

where
 $R_{II} = (g_{m7}r_{ds7}r_{ds6}) \parallel (g_{m12}r_{ds12}r_{ds11})$
and

$$k = \frac{g_{m8}}{g_{m3}} = \frac{g_{m6}}{g_{m4}}$$

This op amp is balanced because the drain-to-ground loads for M1 and M2 are identical.

TABLE 1 - Design Relationships for Balanced, Cascode Output Stage Op Amp.

Slew rate = $\frac{I_{out}}{C_L}$	$GB = \frac{g_{m1}g_{m8}}{g_{m3}C_L}$	$A_v = \frac{1}{2} \left(\frac{g_{m1}g_{m8}}{g_{m3}} + \frac{g_{m2}g_{m6}}{g_{m4}} \right) R_{II}$
$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3} \right]^{1/2} - V_{TO3} (\max) + V_{TI}(\min)$		$V_{in}(\min) = V_{SS} + V_{DS5} + \left[\frac{I_5}{\beta_1} \right]^{1/2} + V_{TI}(\min)$

Example 240-2 Design of Balanced, Cascoded Output Stage Op Amp

Design a balanced, cascaded output stage op amp using the procedure outlined above. The specifications of the design are as follows:

$$V_{DD} = 2.5 \text{ V } (V_{SS} = 0) \quad \text{Slew rate} = 5 \text{ V}/\mu\text{s} \text{ with a } 50 \text{ pF load}$$

$$GB = 10 \text{ MHz with a } 25 \text{ pF load} \quad A_v \geq 5000$$

$$\text{Input CMR} = 1\text{V to } +2 \text{ V} \quad 0.5\text{V} < \text{Output swing} < 2 \text{ V}$$

Use $K_N' = 120 \mu\text{A/V}^2$, $K_P' = 25 \mu\text{A/V}^2$, $V_{TN} = |V_{TP}| = 0.5\text{V}$, $\lambda_N = 0.06\text{V}^{-1}$, and $\lambda_P = 0.08\text{V}^{-1}$ and let all device lengths be $0.5 \mu\text{m}$.

Solution

While numerous approaches can be taken, we shall follow one based on the above specifications. The steps will be numbered to help illustrate the procedure.

1.) The first step will be to find the maximum source/sink current. This is found from the slew rate.

$$I_{\text{source}}/I_{\text{sink}} = C_L \times \text{slew rate} = 50 \text{ pF}(5 \text{ V}/\mu\text{s}) = 250 \mu\text{A}$$

2.) Next some W/L constraints based on the maximum output source/sink current are developed. Under dynamic conditions, all of I_5 will flow in M4; thus we can write

$$\text{Max. } I_{\text{out}}(\text{source}) = (S_6/S_4)I_5 \quad \text{and} \quad \text{Max. } I_{\text{out}}(\text{sink}) = (S_8/S_3)I_5$$

The maximum output sinking current is equal to the maximum output sourcing current if

$$S_3 = S_4, \quad S_6 = S_8, \quad \text{and} \quad S_{10} = S_{11}$$

Example 240-2 - Continued

3.) Choose I_5 as $100 \mu\text{A}$. This current (which can be changed later) gives

$$S_6 = 2.5S_4 \quad \text{and} \quad S_8 = 2.5S_3$$

Note that S_8 could equal S_3 if $S_{11} = 2.5S_{10}$. This would minimize the power dissipation.

4.) Next design for $+0.5\text{V}$ output capability. We shall assume that the output must source or sink the $250 \mu\text{A}$ at the peak values of output. First consider the negative output peak. Since there is 0.5V difference between $V_{SS}(0\text{V})$ and the minimum output, let $V_{DS11(\text{sat})} = V_{DS12(\text{sat})} = 0.25 \text{ V}$ (we continue to ignore the bulk effects). Under the maximum negative peak assume that $I_{11} = I_{12} = 250 \mu\text{A}$. Therefore

$$0.25 = \sqrt{\frac{2I_{11}}{K'_N S_{11}}} = \sqrt{\frac{2I_{12}}{K'_N S_{12}}} = \sqrt{\frac{500 \mu\text{A}}{(120 \mu\text{A/V}^2)S_{11}}}$$

which gives $S_{11} = S_{12} = 67$ and $S_9 = S_{10} = 67$. For a maximum output voltage of 2V , we get

$$0.25 = \sqrt{\frac{2I_6}{K'_P S_6}} = \sqrt{\frac{2I_7}{K'_P S_7}} = \sqrt{\frac{500 \mu\text{A}}{(25 \mu\text{A/V}^2)S_6}}$$

which gives $S_6 = S_7 = S_8 = 320$ and $S_3 = S_4 = (320/2.5) = 128$.

Example 240-2 - Continued

5.) Now we must consider the possibility of conflict among the specifications.

First consider the input CMR. S_3 has already been designed as 67. Using ICMR relationship, we find that S_3 should be at least 8. A larger value of S_3 will give a higher value of $V_{in(max)}$ so that we continue to use $S_3 = 67$ which gives $V_{in(max)} = 2.32V$.

Next, check to see if the larger W/L causes a pole below the gainbandwidth. Assuming a C_{ox} of $6fF/\mu m^2$ gives the first-stage pole of

$$p_3 = \frac{-g_{m3}}{C_{gs3} + C_{gs8}} = \frac{-\sqrt{2K'P S_3 I_3}}{(0.667)(W_3 L_3 + W_8 L_8)C_{ox}} = 3.125 \times 10^9 \text{ rads/sec or } 497 \text{ MHz}$$

which is much greater than $10GB$.

6.) Next we find g_{m1} (g_{m2}). There are two ways of calculating g_{m1} .

(a.) The first is from the A_v specification. The gain is

$$A_v = (g_{m1}/2g_{m4})(g_{m6} + g_{m8}) R_{II}$$

Note, a current gain of k can be introduced by making S_6/S_4 ($S_8/S_3 = S_{11}/S_3$) equal to k .

$$\frac{g_{m6}}{g_{m4}} = \frac{g_{m11}}{g_{m3}} = \sqrt{\frac{2K'P \cdot S_6 \cdot I_6}{2K'P \cdot S_4 \cdot I_4}} = k$$

Calculating the various transconductances we get $g_{m4} = 566 \mu S$, $g_{m6} = g_{m7} = g_{m8} = 1414 \mu S$, $g_{m11} = g_{m12} = 1414 \mu S$, $r_{ds6} = r_{d7} = 100 k\Omega$, and $r_{ds11} = r_{ds12} = 133 k\Omega$. Assuming that the gain A_v must be greater than 5000 and $k = 2.5$ gives $g_{m1} > 221 \mu S$.

Example 240-2 - Continued

(b.) The second method of finding g_{m1} is from the GB specifications. Multiplying the gain by the dominant pole ($1/C_{II}R_{II}$) gives

$$GB = \frac{g_{m1}(g_{m6} + g_{m8})}{2g_{m4}C_L}$$

Assuming that $C_L = 25 \text{ pF}$ and using the specified GB gives $g_{m1} = 628 \mu S$.

Since this is greater than $221 \mu S$, we choose $g_{m1} = g_{m2} = 628 \mu S$. Knowing I_5 gives $S_1 = S_2 = 32.9 \approx 33$.

8.) The next step is to check that S_1 and S_2 are large enough to meet the $+1V$ input CMR specification. Use the saturation formula we find that V_{DS5} is 0.341 V . This gives $S_5 = 15$. The gain becomes $A_v = 14,182 \text{ V/V}$ and $GB = 10 \text{ MHz}$ for a 25 pF load. We shall assume that exceeding the specifications in this area is not detrimental to the performance of the op amp.

9.) Knowing the currents and W/L values, the bias voltages V_{NB1} , V_{NB2} and V_{PB2} can be designed.

The W/L values resulting from this design procedure are shown below. The power dissipation for this design is seen to be $350 \mu A \cdot 2.5V = 0.875 \text{ mW}$.

$$\begin{array}{lll} S_1 = S_2 = 33 & S_3 = S_4 = 128 & S_5 = 15 \\ S_6 = S_7 = S_8 = 320 & S_9 = S_{10} = S_{11} = S_{12} = 67 \end{array}$$

Technological Implications of the Cascode Configuration

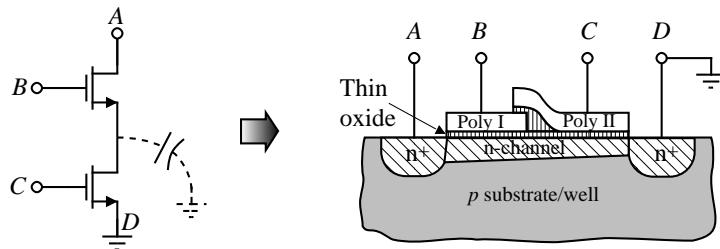


Fig. 6.5-5

If a double poly CMOS process is available, inter-node parasitics can be minimized. As an alternative, one should keep the drain/source between the transistors to a minimum area.

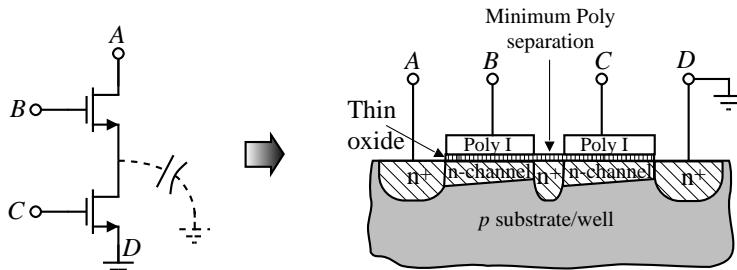
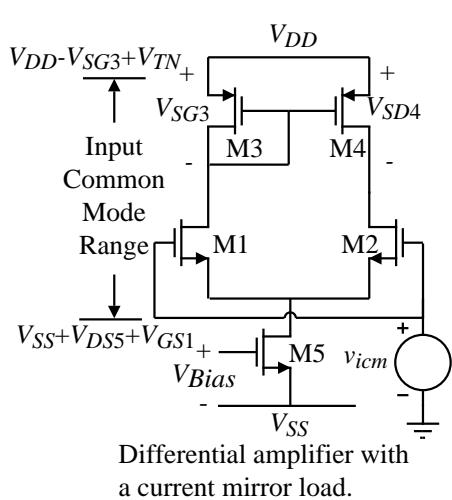
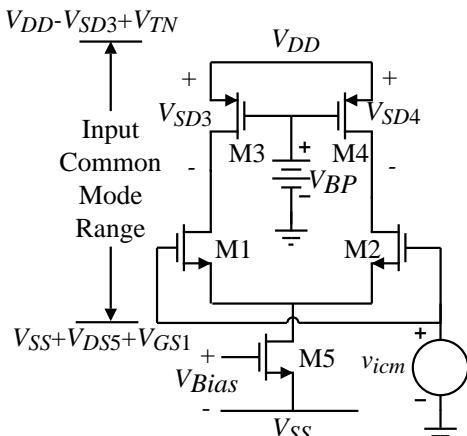


Fig. 6.5-5A

Input Common Mode Range for Two Types of Differential Amplifier Loads



Differential amplifier with a current mirror load.

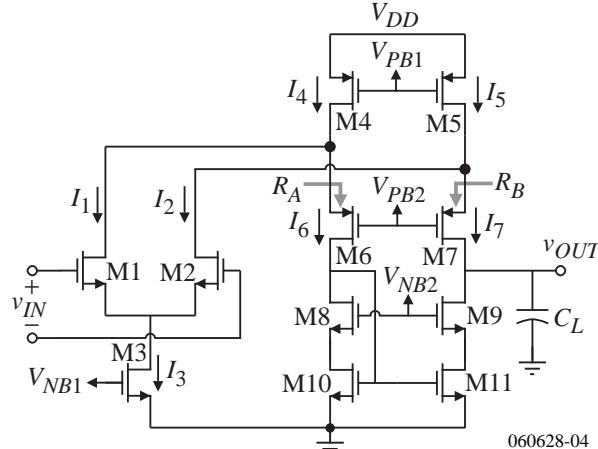


Differential amplifier with current source loads. Fig. 6.5-6

In order to improve the ICMR, it is desirable to use current source (sink) loads without losing half the gain.

The resulting solution is the *folded cascode op amp*.

The Folded Cascode Op Amp



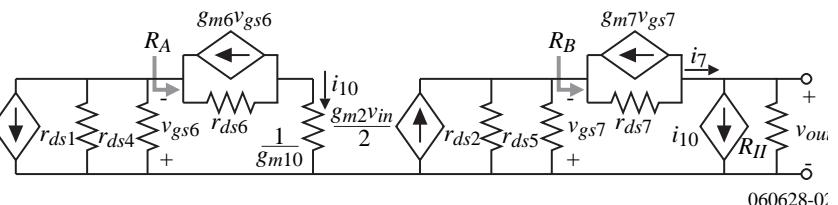
Comments:

- I_4 and I_5 , should be designed so that I_6 and I_7 never become zero (i.e. $I_4=I_5=1.5I_3$)
 - This amplifier is nearly balanced (would be exactly if R_A was equal to R_B)
 - Self compensating
 - Poor noise performance, the gain occurs at the output so all intermediate transistors contribute to the noise along with the input transistors. (Some first stage gain can be achieved if R_A and R_B are greater than gm_1 or gm_2 .)

Small-Signal Analysis of the Folded Cascode Op Amp

Model:

Recalling what we learned about the resistance looking into the source of the cascode transistor;



$$R_A = \frac{r_{ds6} + (1/g_{m10})}{1 + g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} \quad \text{and} \quad R_B = \frac{r_{ds7} + R_{II}}{1 + g_{m7}r_{ds7}} \approx \frac{R_{II}}{g_{m7}r_{ds7}} \quad \text{where} \quad R_{II} \approx g_{m9}r_{ds9}r_{ds11}$$

The voltage transfer function can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}(r_{ds1}||r_{ds4})v_{in}}{2[R_A + (r_{ds1}||r_{ds4})]} \approx \frac{-g_{m1}v_{in}}{2}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2}(r_{ds2}||r_{ds5})v_{in}}{2\left[\frac{R_{II}}{g_{m7}r_{ds7}} + (r_{ds2}||r_{ds5})\right]} = \frac{g_{m2}v_{in}}{2\left(1 + \frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}\right)} = \frac{g_{m2}v_{in}}{2(1+k)} \quad \text{where } k = \frac{R_{II}(g_{ds2}+g_{ds5})}{g_{m7}r_{ds7}}$$

The output voltage, v_{out} , is equal to the sum of i_7 and i_{10} flowing through R_{out} . Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)} \right) R_{out} = \left(\frac{2+k}{2+2k} \right) g_{mI} R_{out}$$

Intuitive Analysis of the Folded Cascode Op Amp

Assume that a voltage of ΔV is applied. We know that

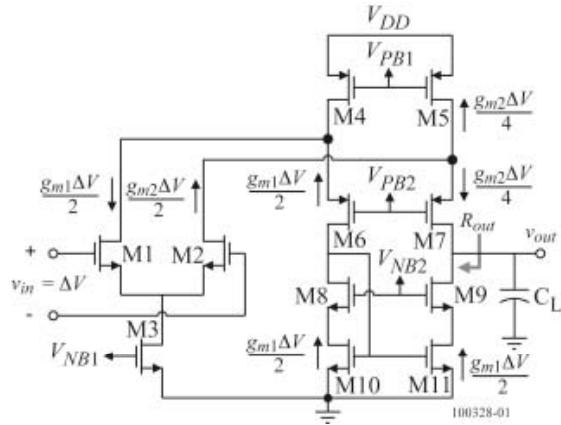
$$R_A(M6) \approx 1/g_{m6} \text{ and } R_B(M7) \approx r_{ds}$$

The currents flowing to the output are,

$$\frac{g_{m1}\Delta V}{2} + \frac{g_{m2}\Delta V}{4}$$

The output resistance is approximately,

$$R_{out} \approx (g_{m9}r_{ds9}r_{ds11})/[g_{m7}r_{ds7}(r_{ds2}||r_{ds5})] \\ \approx \left(\frac{g_m r_{ds}^2}{3}\right)$$



Therefore, the approximate voltage gain is,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{4}\right) R_{out} \approx \left(\frac{3g_m}{4}\right) R_{out} = \left(\frac{g_m^2 r_{ds}^2}{4}\right)$$

While the analysis is simpler than small signal analysis, the value of k defined in the previous slide is 1.

Frequency Response of the Folded Cascode Op Amp

The frequency response of the folded cascode op amp is determined primarily by the output pole which is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}} \quad \text{where } R_{out}' = \left(\frac{2+k}{2+2k}\right)R_{out}$$

where C_{out} is all the capacitance connected from the output of the op amp to ground.

All other poles must be greater than $GB = g_{m1}/C_{out}$. The approximate expressions for each pole is

- | | |
|---------------------------|---|
| 1.) Pole at node A: | $p_A \approx -g_{m6}/(C_{gs} + 2C_{db})$ |
| 2.) Pole at node B: | $p_B \approx -g_{m7}/(C_{gs} + 2C_{db})$ |
| 3.) Pole at drain of M6: | $p_6 \approx -g_{m10}/(2C_{gs} + 2C_{db})$ |
| 4.) Pole at source of M8: | $p_8 \approx -(g_{m8}r_{ds8}g_{m10})/(C_{gs} + C_{db})$ |
| 5.) Pole at source of M9: | $p_9 \approx -g_{m9}/(C_{gs} + C_{db})$ |

where the approximate expressions are found by the reciprocal product of the resistance and parasitic capacitance seen to ground from a given node. One might feel that because R_B is approximately r_{ds} that this pole also might be small. However, at frequencies where this pole has influence, C_{out} , causes R_{out} to be much smaller making p_B also non-dominant.

Example 240-3 - Folded Cascode, CMOS Op Amp

Assume that all $g_mN = g_mP = 100\mu\text{S}$, $r_{dsN} = 2\text{M}\Omega$, $r_{dsP} = 1\text{M}\Omega$, and $C_L = 10\text{pF}$. Find all of the small-signal performance values for the folded-cascode op amp.

$$R_{II} = 0.4\text{G}\Omega, R_A = 10\text{k}\Omega, \text{ and } R_B = 4\text{M}\Omega \quad \therefore k = \frac{0.4 \times 10^9 (0.3 \times 10^{-6})}{100} = 1.2$$

$$\frac{v_{out}}{v_{in}} = \frac{(2+1.2)}{(2+2.4)} (100)(57.143) = 4,156\text{V/V}$$

$$R_{out} = R_{II} \parallel [g_{m7}r_{ds7}(r_{ds5} \parallel r_{ds2})] = 400\text{M}\Omega \parallel [(100)(0.667\text{M}\Omega)] = 57.143\text{M}\Omega$$

$$|p_{out}| = \frac{1}{R_{out}C_{out}} = \frac{1}{57.143\text{M}\Omega \cdot 10\text{pF}} = 1,750 \text{ rads/sec.} \Rightarrow 278\text{Hz} \Rightarrow GB = 1.21\text{MHz}$$

PSRR of the Folded Cascode Op Amp

Consider the following circuit used to model the $PSRR^-$:

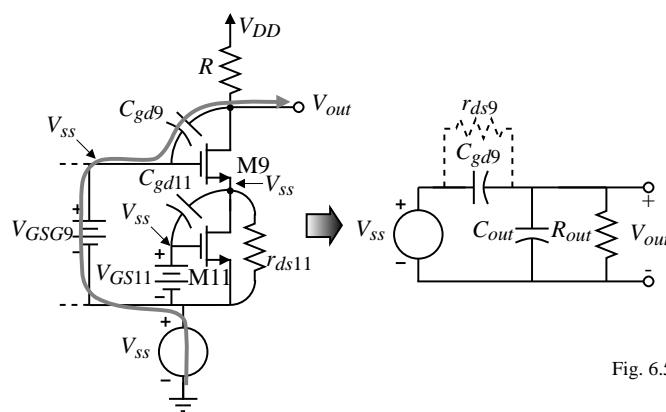


Fig. 6.5-9A

This model assumes that gate, source and drain of M11 and the gate and source of M9 all vary with V_{SS} .

We shall examine V_{out}/V_{ss} rather than $PSRR^-$. (Small V_{out}/V_{ss} will lead to large $PSRR^-$.)

The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd9}R_{out}}{sC_{out}R_{out} + 1} \quad \text{for } C_{gd9} < C_{out}$$

The approximate PSRR- is sketched on the next page.

Frequency Response of the PSRR⁻ of the Folded Cascode Op Amp

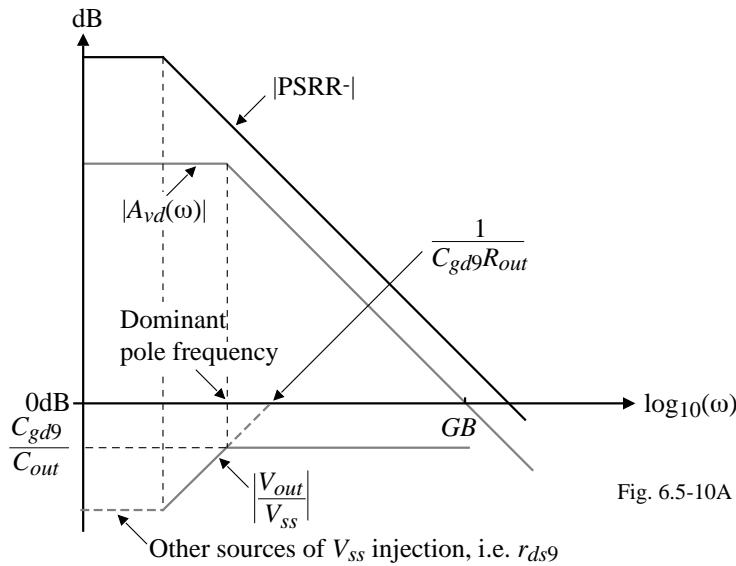


Fig. 6.5-10A

We see that the PSRR of the cascode op amp is much better than the two-stage op amp without any modifications to improve the PSRR.

Design Approach for the Folded-Cascode Op Amp

Step	Relationship	Design Equation/Constraint	Comments
1	Slew Rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, $v_{out}(\max)$	$S_5 = \frac{2I_5}{K_P V_{SD5}^2}, S_7 = \frac{2I_7}{K_P V_{SD7}^2}, (S_4=S_5 \text{ and } S_6=S_7)$	$V_{SD5}(\text{sat})=V_{SD7}(\text{sat}) = 0.5[V_{DD}-V_{out}(\max)]$
4	Minimum output voltage, $v_{out}(\min)$	$S_{11} = \frac{2I_{11}}{K_N V_{DS11}^2}, S_9 = \frac{2I_9}{K_N V_{DS9}^2}, (S_{10}=S_{11} \text{ and } S_8=S_9)$	$V_{DS9}(\text{sat})=V_{DS11}(\text{sat}) = 0.5[V_{out}(\min)-V_{SS}]$
5	$GB = \frac{g_m 1}{C_L}$	$S_1=S_2=\frac{g_m 1^2}{K_N I_3} = \frac{GB^2 C_L^2}{K_N I_3}$	
6	Minimum input CM	$S_3 = \frac{2I_3}{K_N (V_{in}(\min)-V_{SS}-\sqrt{(I_3/K_N S_1) \cdot V_{T1}})^2}$	
7	Maximum input CM	$S_4 = S_5 = \frac{2I_4}{K_P (V_{DD}-V_{in}(\max)+V_{T1})^2}$	S_4 and S_5 must meet or exceed value in step 3
8	Differential Voltage Gain	$\frac{v_{out}}{v_{in}} = \left(\frac{g_m 1}{2} + \frac{g_m 2}{2(1+k)} \right) R_{out} = \left(\frac{2+k}{2+2k} \right) g_m 1 R_{out}$	$k = \frac{R_I(g_{ds2}+g_{ds4})}{g_m 7 r_{ds7}}$
9	Power dissipation	$P_{diss} = (V_{DD}-V_{SS})(I_3+I_{10}+I_{11})$	

Example 240-4 Design of a Folded-Cascode Op Amp

Design a folded-cascode op amp if the slew rate is $10\text{V}/\mu\text{s}$, the load capacitor is 10pF , the maximum and minimum output voltages are 2V and 0.5V for a 2.5V power supply, the GB is 10MHz , the minimum input common mode voltage is $+1\text{V}$ and the maximum input common mode voltage is 2.5V . The differential voltage gain should be greater than $3,000\text{V/V}$ and the power dissipation should be less than 5mW . Use $K_N' = 120\mu\text{A/V}^2$, $K_P' = 25\mu\text{A/V}^2$, $V_{TN} = |V_{TP}| = 0.5\text{V}$, $\lambda_N = 0.06\text{V}^{-1}$, and $\lambda_P = 0.08\text{V}^{-1}$. Let $L = 0.5 \mu\text{m}$.

Solution

Following the approach outlined above we obtain the following results.

$$I_3 = SR \cdot C_L = 10 \times 10^6 \cdot 10^{-11} = 100\mu\text{A}$$

Select $I_4 = I_5 = 125\mu\text{A}$.

Next, we see that the value of $0.5(V_{DD} - V_{out}(\max))$ is $0.5\text{V}/2$ or 0.25V . Thus,

$$S_4 = S_5 = \frac{2 \cdot 125\mu\text{A}}{25\mu\text{A/V}^2 \cdot (0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{25} = 160$$

and assuming worst case currents in M6 and M7 gives,

$$S_6 = S_7 = \frac{2 \cdot 125\mu\text{A}}{25\mu\text{A/V}^2(0.25\text{V})^2} = \frac{2 \cdot 125 \cdot 16}{25} = 160$$

The value of $0.5(V_{out}(\min) - |V_{SS}|)$ is 0.25V which gives the value of S_8, S_9, S_{10} and S_{11} as

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' V_{DS8}^2} = \frac{2 \cdot 125}{120 \cdot (0.25)^2} = 20$$

Example 240-4 - Continued

In step 5, the value of GB gives S_1 and S_2 as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N' I_3} = \frac{(20\pi \times 10^6)^2 (10^{-11})^2}{120 \times 10^{-6} \cdot 100 \times 10^{-6}} = 32.9 \approx 33$$

The minimum input common mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{K_N' \left(V_{in}(\min) - V_{SS} - \sqrt{\frac{I_3}{K_N' S_1}} - V_{T1} \right)^2} = \frac{200 \times 10^{-6}}{120 \times 10^{-6} \left(1.0 + 0 - \sqrt{\frac{100}{120 \cdot 33}} - 0.5 \right)^2} = 14.3 \approx 15$$

We need to check that the values of S_4 and S_5 are large enough to satisfy the maximum input common mode voltage. The maximum input common mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P' [V_{DD} - V_{in}(\max) + V_{T1}]^2} = \frac{2 \cdot 125\mu\text{A}}{25 \times 10^{-6} \mu\text{A/V}^2 [0.5\text{V}]^2} = 40$$

which is less than 160 . In fact, with $S_4 = S_5 = 160$, the maximum input common mode voltage is 2.75V .

The power dissipation is found to be

$$P_{diss} = 2.5\text{V}(125\mu\text{A} + 125\mu\text{A}) = 0.625\text{mW}$$

Example 240-4 - Continued

The small-signal voltage gain requires the following values to evaluate:

$$S_4, S_5: \quad g_m = \sqrt{2 \cdot 125 \cdot 25 \cdot 160} = 1000\mu\text{S} \quad \text{and} \quad g_{ds} = 125 \times 10^{-6} \cdot 0.08 = 10\mu\text{S}$$

$$S_6, S_7: \quad g_m = \sqrt{2 \cdot 75 \cdot 25 \cdot 1600} = 774.6\mu\text{S} \quad \text{and} \quad g_{ds} = 75 \times 10^{-6} \cdot 0.08 = 6\mu\text{S}$$

$$S_8, S_9, S_{10}, S_{11}: \quad g_m = \sqrt{2 \cdot 75 \cdot 120 \cdot 20} = 600\mu\text{S} \quad \text{and} \quad g_{ds} = 75 \times 10^{-6} \cdot 0.06 = 4.5\mu\text{S}$$

$$S_1, S_2: \quad g_{mI} = \sqrt{2 \cdot 50 \cdot 120 \cdot 33} = 629\mu\text{S} \quad \text{and} \quad g_{ds} = 50 \times 10^{-6} \cdot (0.06) = 3\mu\text{S}$$

Thus,

$$R_{II} \approx g_{m9} r_{ds9} r_{ds11} = (600\mu\text{S}) \left(\frac{1}{4.5\mu\text{S}} \right) \left(\frac{1}{4.5\mu\text{S}} \right) = 29.63\text{M}\Omega$$

$$R_{out} \approx 29.63\text{M}\Omega \parallel (774.6\mu\text{S}) \left(\frac{1}{6\mu\text{S}} \right) \left(\frac{1}{10\mu\text{S} + 3\mu\text{S}} \right) = 7.44\text{M}\Omega$$

$$k = \frac{R_{II}(g_{ds2} + g_{ds4})}{g_{m7} r_{ds7}} = \frac{7.44\text{M}\Omega(3\mu\text{S} + 10\mu\text{S})(6\mu\text{S})}{774.6\mu\text{S}} = 0.75$$

The small-signal, differential-input, voltage gain is

$$A_{vd} = \left(\frac{2+k}{2+2k} \right) g_{mI} R_{out} = \left(\frac{2+0.75}{2+1.5} \right) 0.629 \times 10^{-3} \cdot 7.44 \times 10^6 = (0.786)(4680) = 3,678 \text{ V/V}$$

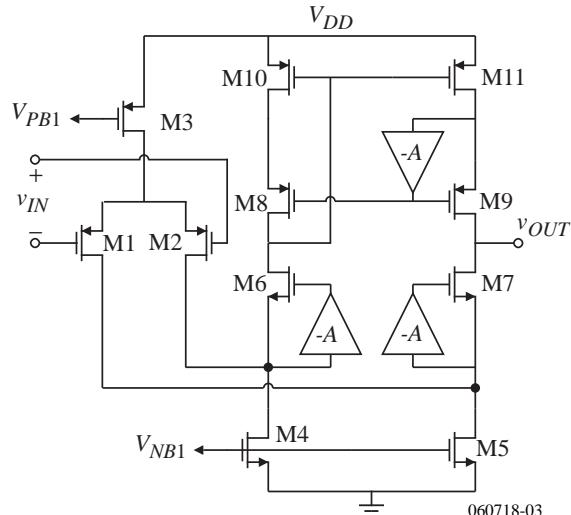
The gain is slightly larger than the specified 3,000 V/V.

Comments on Folded Cascode Op Amps

- Good PSRR
- Good ICMR
- Self compensated
- Can cascade an output stage to get extremely high gain with lower output resistance (use Miller compensation in this case)
- Need first stage gain for good noise performance
- Widely used in telecommunication circuits where large dynamic range is required

Enhanced-Gain, Folded Cascode Op Amps

If more gain is needed, the folded cascode op amp can be enhanced to boost the output impedance even higher as follows.



Voltage gain = $g_m R_{out}$,
where

$$R_{out} \approx [A r_{ds7} g_m 7 (r_{ds1} \| r_{ds5})] \| (A r_{ds9} g_m 9 r_{ds11})$$

Since $A \approx g_m r_{ds}$ the voltage gain would be in the range of 100,000 to 500,000.

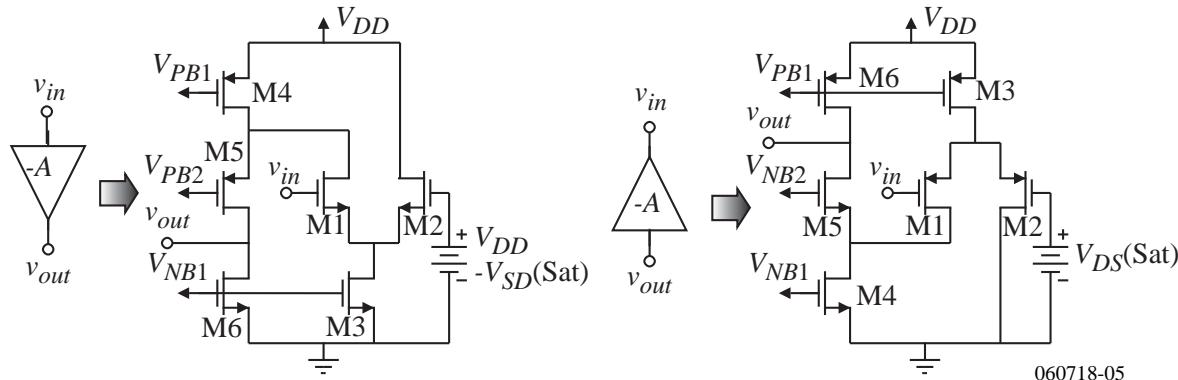
Note that to achieve maximum output swing, it will be necessary to make sure that M5 and M11 are biased with $V_{DS} = V_{DS}(\text{sat})$.

What are the Enhancement Amplifiers?

Requirements:

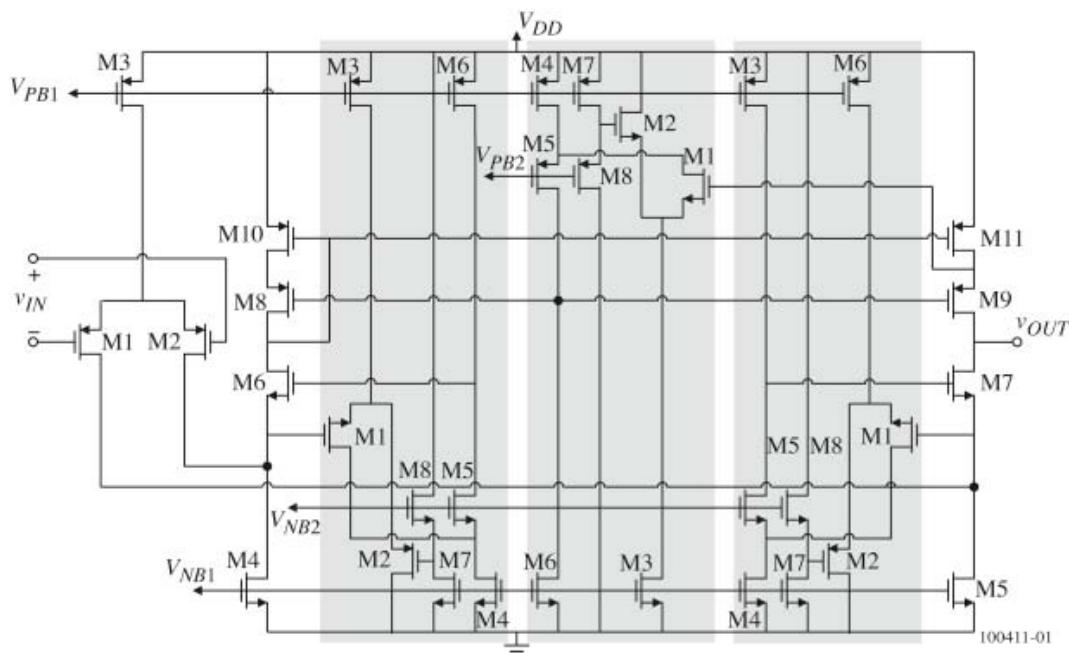
- 1.) Need a gain of $g_m r_{ds}$.
- 2.) Must be able to set the dc voltage at its input to get wide-output voltage swing.

Possible Enhancement Amplifiers:



Enhanced-Gain, Folded Cascode Op Amp

Detailed realization:

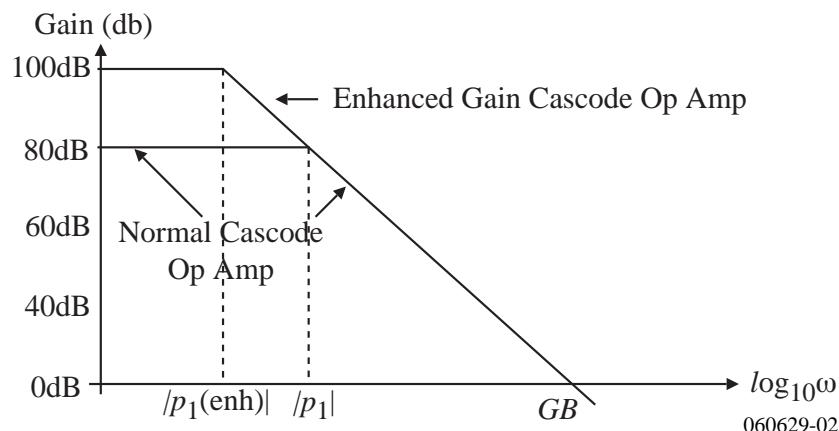


Frequency Response of the Enhanced Gain Cascode Op Amps

Normally, the frequency response of the cascode op amps would have one dominant pole at the output. The frequency response would be,

$$A_v(s) = g_m 1 \left(\frac{R_{out}(1/sC_{out})}{R_{out} + 1/sC_{out}} \right) = \frac{g_m R_{out}}{sR_{out}C_{out} + 1} = \frac{g_m R_{out}}{1 - \frac{s}{p_1}}$$

If the amplifier used to boost the output resistance had no frequency dependence then the frequency response would be as follows.



Frequency Response of the Enhanced Gain Cascode Op Amp – Continued

- Does the pole in the feedback amplifier A have an influence?

Although the output resistance can be modeled as,

$$R_{out}' \approx R_{out}A_o \left(\frac{1 - \frac{s}{p_2 A_o}}{1 - \frac{s}{p_2}} \right)$$

it has no influence on the frequency response because C_{out} has shorted out any influence a change in R_{out} might have.

- Higher order poles come from a diversion of the current flow in the op amp to ground rather than the intended destination of the current to the output. These poles that divert the current are:

- Pole at the source of M6 ($A g_{m6}/C_6$) - Pole at the source of M7 ($A g_{m7}/C_7$)
- Pole at the drain of M8 (g_{m10}/C_8) - Pole at the source of M9 ($A g_{m9}/C_6$)
- Pole at the drain of M10 ($g_{m8}r_{ds8}g_{m10}/C_{10}$)

Note that the enhancement amplifiers cause most of the higher-order poles to be moved out by $|A|$. However, each of the enhancement amplifiers introduce a pole at their output which is approximately $-1/[r_{ds}(C_{gs}+2C_{db}+2C_{gd})]$. These poles become the dominant poles that limit GB .

SUMMARY

- Cascode op amps give additional flexibility to the two-stage op amp
 - Increase the gain
 - Control the dominant and nondominant poles
- Enhanced gain, cascode amplifiers provide additional gain and are used when high gains are needed
- Folded cascode amplifier is an attractive alternate to the two-stage op amp
 - Wider ICMR
 - Self compensating
 - Good PSRR

LECTURE 250 – SIMULATION AND MEASUREMENT OF OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Open Loop Gain
- $CMRR$ and $PSRR$
- A general method of measuring A_{vd} , $CMRR$, and $PSRR$
- Other op amp measurements
- Simulation of a Two-Stage Op Amp
- Op amp macromodels
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 310-341

INTRODUCTION

Simulation and Measurement Considerations

Objectives:

- The objective of simulation is to verify and optimize the design.
- The objective of measurement is to experimentally confirm the specifications.

Similarity between Simulation and Measurement:

- Same goals
- Same approach or technique

Differences between Simulation and Measurement:

- Simulation can idealize a circuit
 - All transistor electrical parameters are ideally matched
 - Ideal stimuli
- Measurement must consider all nonidealities
 - Physical and electrical parameter mismatches
 - Nonideal stimuli
 - Parasitics

OPEN LOOP GAIN

Simulating or Measuring the Open-Loop Transfer Function of the Op Amp

Circuit (Darkened op amp identifies the op amp under test):

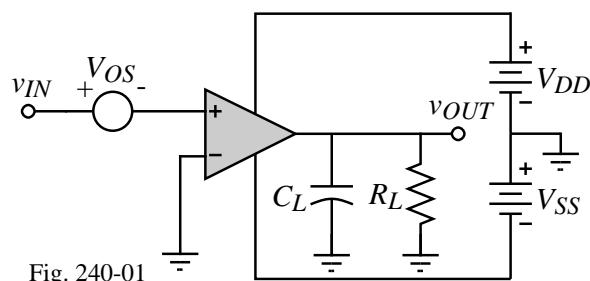
Simulation:

This circuit will give the voltage transfer function curve. This curve should identify:

- 1.) The linear range of operation
- 2.) The gain in the linear range
- 3.) The output limits
- 4.) The systematic input offset voltage
- 5.) DC operating conditions, power dissipation
- 6.) When biased in the linear range, the small-signal frequency response can be obtained
- 7.) From the open-loop frequency response, the phase margin can be obtained ($F = 1$)

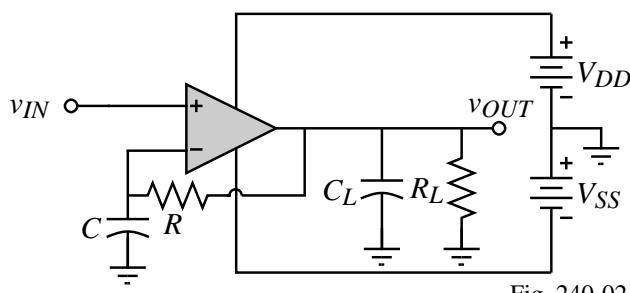
Measurement:

This circuit probably will not work unless the op amp gain is very low.

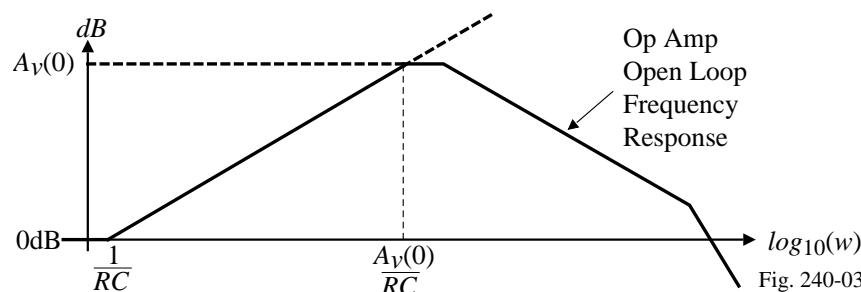


A More Robust Method of Measuring the Open-Loop Frequency Response

Circuit:



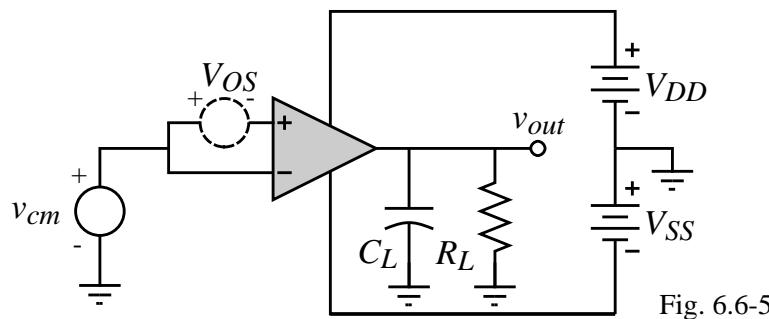
Resulting Closed-Loop Frequency Response:



Make the RC product as large as possible.

CMRR AND PSRR

Simulation of the Common-Mode Voltage Gain

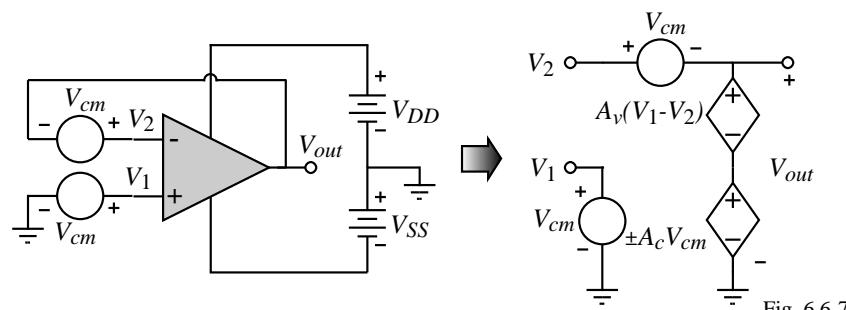


Make sure that the output voltage of the op amp is in the linear region.
Divide (subtract dB) the result into the open-loop gain to get *CMRR*.

Simulation of CMRR of an Op Amp

None of the above methods are really suitable for simulation of *CMRR*.

Consider the following:



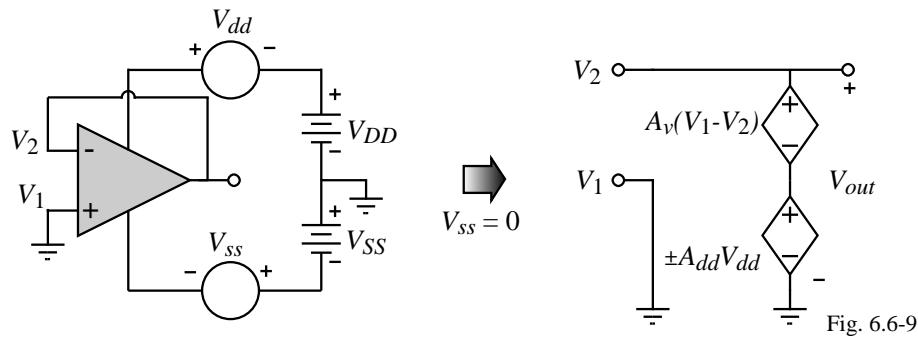
$$V_{out} = A_v(V_1 - V_2) \pm A_{cm} \left(\frac{V_1 + V_2}{2} \right) = -A_v V_{out} \pm A_{cm} V_{cm}$$

$$V_{out} = \frac{\pm A_{cm}}{1 + A_v} V_{cm} \approx \frac{\pm A_{cm}}{A_v} V_{cm}$$

$$\therefore |CMRR| = \frac{A_v}{A_{cm}} = \frac{V_{cm}}{V_{out}}$$

Direct Simulation of PSRR

Circuit:



$$V_{out} = A_v(V_1 - V_2) \pm A_{dd}V_{dd} = -A_v V_{out} \pm A_{dd}V_{dd}$$

$$V_{out} = \frac{\pm A_{dd}}{1 + A_v} V_{dd} \approx \frac{\pm A_{dd}}{A_v} V_{dd}$$

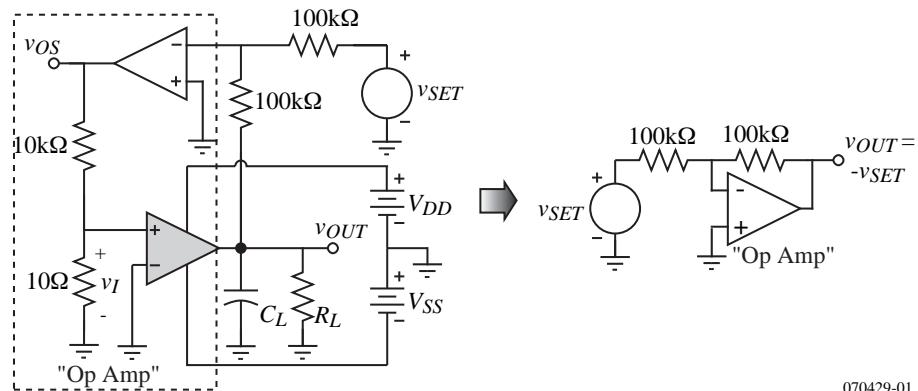
$$\therefore \boxed{PSRR^+ = \frac{A_v}{A_{dd}} = \frac{V_{dd}}{V_{out}}} \quad \text{and} \quad \boxed{PSRR^- = \frac{A_v}{A_{ss}} = \frac{V_{ss}}{V_{out}}}$$

Works well as long as CMRR is much greater than 1.

A GENERAL METHOD OF MEASURING A_{VD} , CMRR, AND PSRR

General Principle of the Measurement

Circuit:



The amplifier under test is shown as the darkened op amp.

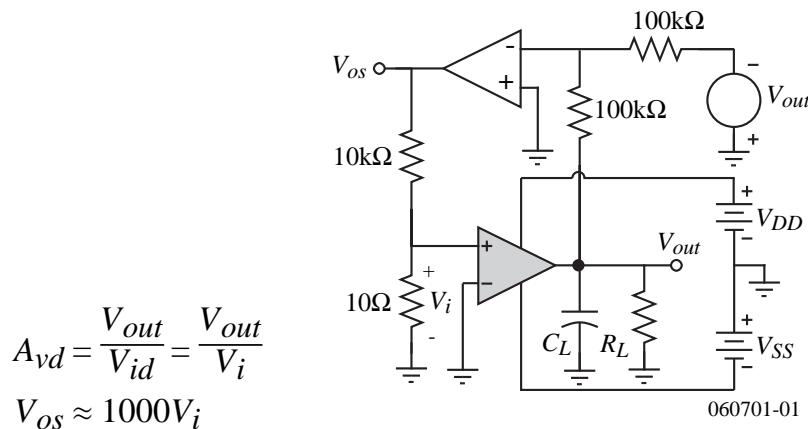
Principle:

Apply the stimulus to the output of the op amp under test and see how the input responds. Note that:

$$v_{OUT} = -v_{SET} \quad \text{and} \quad v_I \approx \frac{v_{OS}}{1000}$$

Measurement of Open-Loop Gain

Measurement configuration:



Therefore, $A_{vd} = \frac{1000V_{out}}{V_{os}}$

Sweep V_{out} as a function of frequency, invert the result and multiply by 1000 to get $A_{vd}(j\omega)$.

Measurement of CMRR

Measurement Configuration:

Note that the whole amplifier is stimulated by V_{icm} while the input responds to this change.

The definition of the common-mode rejection ratio is

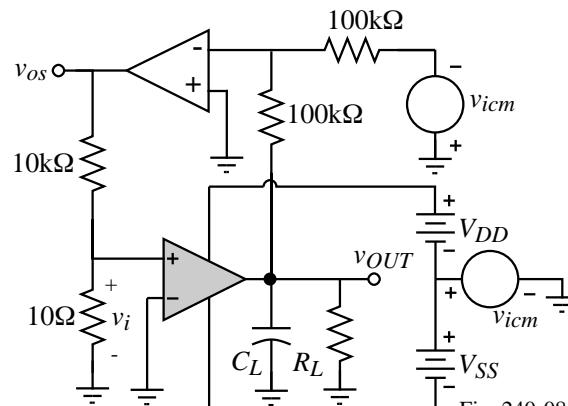
$$CMRR = \left| \frac{A_{vd}}{A_{cm}} \right| = \frac{(v_{out}/v_{id})}{(v_{out}/v_{icm})}$$

However, in the above circuit the value of v_{out} is the same so that we get

$$CMRR = \frac{v_{icm}}{v_{id}}$$

But $v_{id} = v_i$ and $v_{os} \approx 1000v_i = 1000v_{id} \Rightarrow v_{id} = \frac{v_{os}}{1000}$

Substituting in the previous expression gives, $CMRR = \frac{v_{icm}}{v_{os}} = \frac{1000 v_{icm}}{v_{os}}$



Make a frequency sweep of V_{icm} , invert the result and multiply by 1000 to get $CMRR$.

Measurement of PSRR

Measurement Configuration:

The definition of the positive power supply rejection ratio is

$$PSRR^+ = \left| \frac{A_{vd}}{A_{cm}} \right| = \frac{(V_{out}/V_{id})}{(V_{out}/V_{dd})}$$

However, in the above circuit the value of V_{out} is the same so that we get

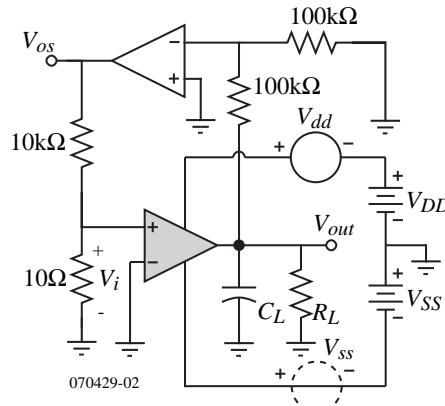
$$PSRR^+ = \frac{V_{dd}}{V_{id}}$$

But $V_{id} = V_i$ and $V_{os} \approx 1000V_i = 1000V_{id}$ $\Rightarrow V_{id} =$

$$\frac{V_{os}}{1000}$$

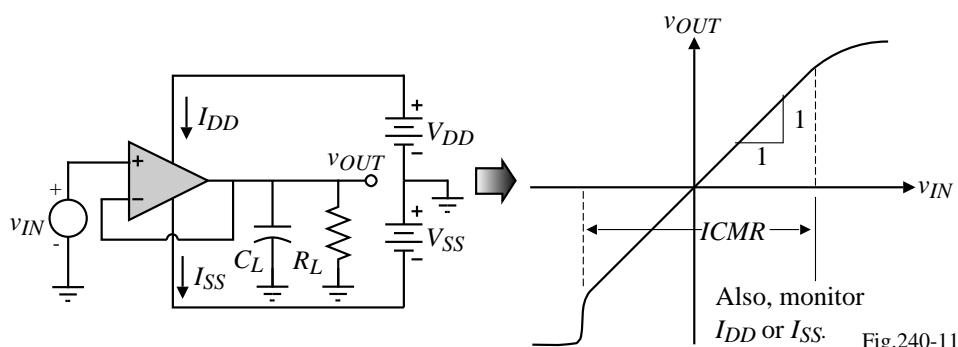
Substituting in the previous expression gives, $PSRR^+ = \frac{V_{dd}}{\frac{V_{os}}{1000}} = \frac{1000 V_{dd}}{V_{os}}$

Make a frequency sweep of V_{dd} , invert the result and multiply by 1000 to get $PSRR^+$.
(Same procedure holds for $PSRR^-$.)



OTHER OP AMP MEASUREMENTS

Simulation or Measurement of ICMR



Initial jump in sweep is due to the turn-on of M5.

Should also plot the current in the input stage (or the power supply current).

Measurement or Simulation of Slew Rate and Settling Time

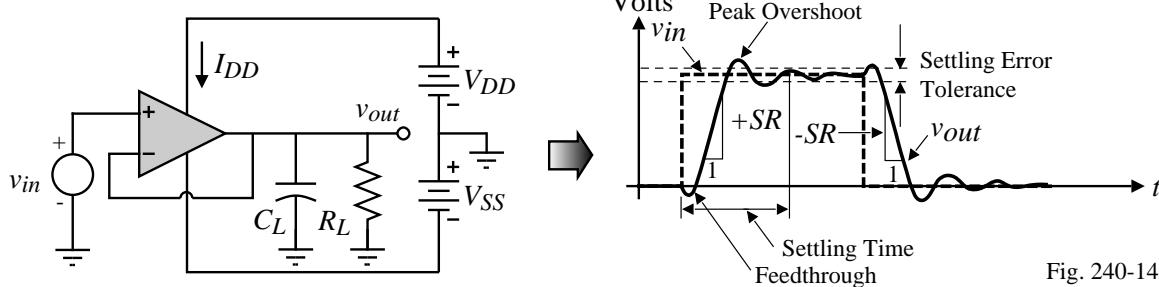


Fig. 240-14

If the slew rate influences the small signal response, then make the input step size small enough to avoid slew rate (i.e. less than 0.5V for MOS).

Phase Margin and Peak Overshoot Relationship

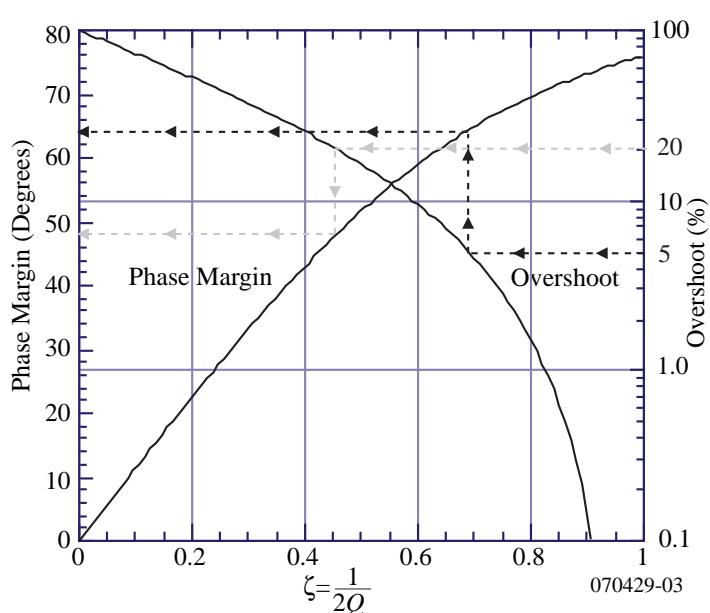
It can be shown (Appendix C of the text) that:

$$\text{Phase Margin (Degrees)} = 57.2958 \cos^{-1} [\sqrt{4\xi^4 + 1} - 2\xi^2]$$

Overshoot (%)

$$= 100 \exp\left(\frac{-\pi\xi}{\sqrt{1-\xi^2}}\right)$$

For example, a 5% overshoot corresponds to a phase margin of approximately 64° .



SIMULATION OF A TWO-STAGE CMOS OP AMP

Example 250-1 Simulation of a Two-Stage CMOS Op Amp

An op amp designed using the procedure described in Lecture 230 is to be simulated by SPICE. The device parameters to be used are those of Tables 3.1-2 and 3.2-1 of the textbook *CMOS Analog Circuit Design*.

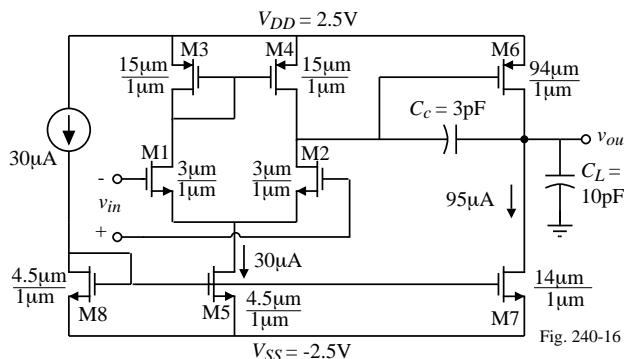


Fig. 240-16

The specifications of this op amp are as follows where the channel length is to be $1\mu\text{m}$ and the load capacitor is $C_L = 10\text{pF}$:

$$A_V > 3000\text{V/V}$$

$$V_{DD} = 2.5\text{V}$$

$$V_{SS} = -2.5\text{V}$$

$$GB = 5\text{MHz}$$

$$SR > 10\text{V}/\mu\text{s}$$

$$60^\circ \text{ phase margin}$$

$$V_{out} \text{ range} = \pm 2\text{V}$$

$$ICMR = -1 \text{ to } 2\text{V}$$

$$P_{diss} \leq 2\text{mW}$$

Example 250-1 – Continued

Bulk Capacitance Calculation:

If the values of the area and perimeter of the drain and source of each transistor are known, then the simulator will calculate the values of C_{BD} and C_{BS} . Since there is no layout yet, we estimate the values of the area and perimeter of the drain and source of each transistor as:

$$AS = AD \approx W[L1 + L2 + L3]$$

$$PS = PD \approx 2W + 2[L1 + L2 + L3]$$

where $L1$ is the minimum allowable distance between the polysilicon and a contact in the moat ($2\mu\text{m}$), $L2$ is the length of a minimum-size square contact to moat ($2\mu\text{m}$), and $L3$ is the minimum allowable distance between a contact to moat and the edge of the moat ($2\mu\text{m}$). (These values will be found from the physical design rules for the technology).

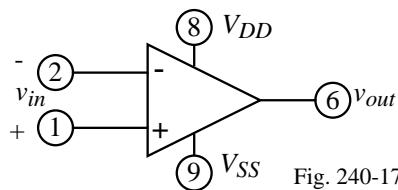
For example consider M1:

$$AS = AD = (3\mu\text{m}) \times (2\mu\text{m} + 2\mu\text{m} + 2\mu\text{m}) = 18\mu\text{m}^2$$

$$PS = PD = 2 \times 3\mu\text{m} + 2 \times 6\mu\text{m} = 19\mu\text{m}$$

Example 250-1 - Continued

Op Amp Subcircuit:



```

.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M2 5 1 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M3 4 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M4 5 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M5 3 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
M6 6 5 8 8 PMOS1 W=94U L=1U AD=564P AS=564P PD=200U PS=200U
M7 6 7 9 9 NMOS1 W=14U L=1U AD=84P AS=84P PD=40U PS=40U
M8 7 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO=0.70 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
+MJ=0.5 MJSW=0.38 CGBO=700P CGSO=220P CGDO=220P CJ=770U CJSW=380P
+LD=0.016U TOX=14N
.MODEL PMOS1 PMOS VTO=-0.7 KP=50U GAMMA=0.57 LAMBDA=0.05 PHI=0.8
+MJ=0.5 MJSW=.35 CGBO=700P CGSO=220P CGDO=220P CJ=560U CJSW=350P +LD=0.014U TOX=14N
IBIAS 8 7 30U
.ENDS

```

Example 250-1 - Continued

PSPICE Input File for the Open-Loop Configuration:

```

EXAMPLE 250-1 OPEN LOOP CONFIGURATION
.OPTION LIMPTS=1000
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 2.5
VSS 0 5 DC 2.5
VIN - 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
:
(Subcircuit of previous slide)
:
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
.PRINT DC V(3)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE (This entry is unique to PSPICE)
.END

```

Example 250-1 - Continued

Open-loop transfer characteristic:

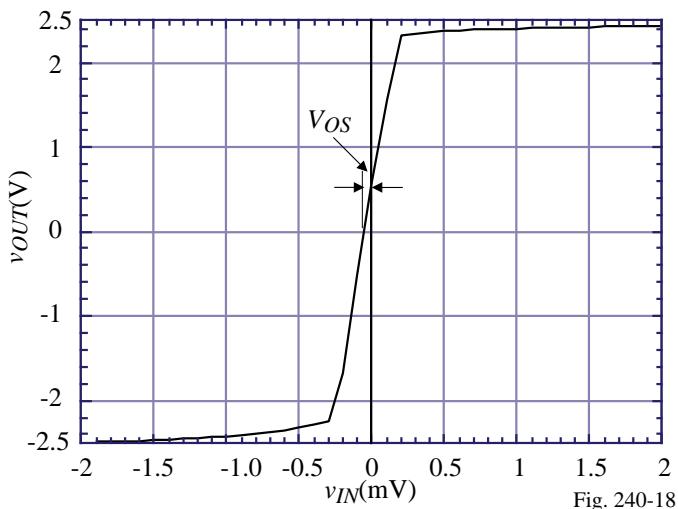


Fig. 240-18

Example 250-1 - Continued

Open-loop transfer frequency response:

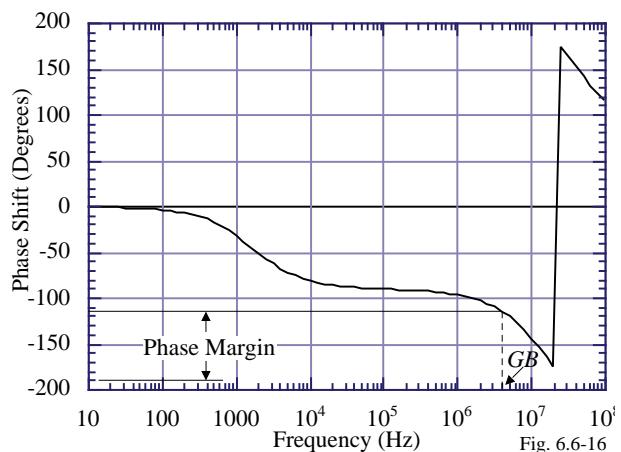
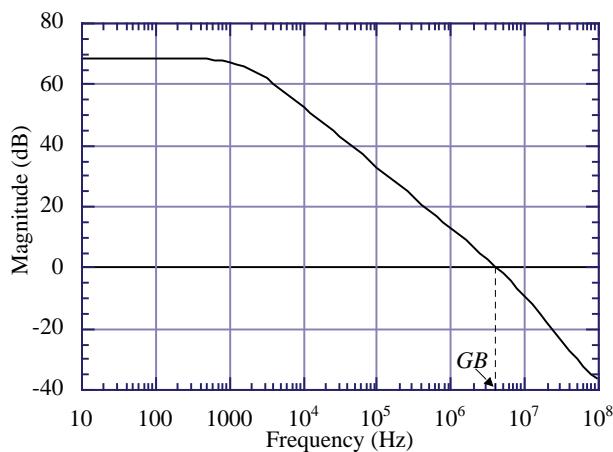


Fig. 6.6-16

Example 250-1 - Continued

Input common mode range:

EXAMPLE 250-1 UNITY GAIN CONFIGURATION.

.OPTION LIMPTS=501

VIN+ 1 0 PWL(0 -2 10N -2 20N 2 2U 2 2.01U -2 4U -2 4.01U
+ -.1 6U -.1 6.0 1U .1 8U .1 8.01U -.1 10U -.1)

VDD 4 0 DC 2.5 AC 1.0

VSS 0 5 DC 2.5

CL 3 0 20P

X1 1 3 3 4 5 OPAMP

⋮

(Subcircuit of Table 6.6-1)

⋮

.DC VIN+ -2.5 2.5 0.1

.PRINT DC V(3)

.TRAN 0.05U 10U 0 10N

.PRINT TRAN V(3) V(1)

.AC DEC 10 1 10MEG

.PRINT AC VDB(3) VP(3)

.PROBE (This entry is unique to PSPICE)

.END

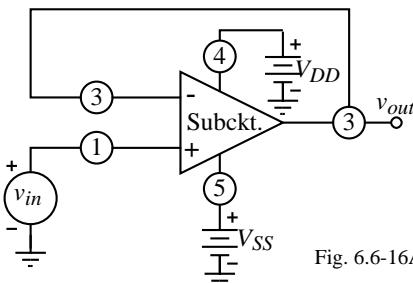


Fig. 6.6-16A

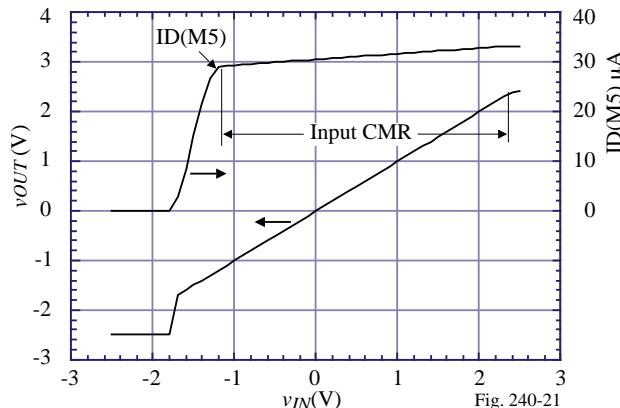


Fig. 240-21

Note the usefulness of monitoring the current in the input stage to determine the lower limit of the $ICMR$.

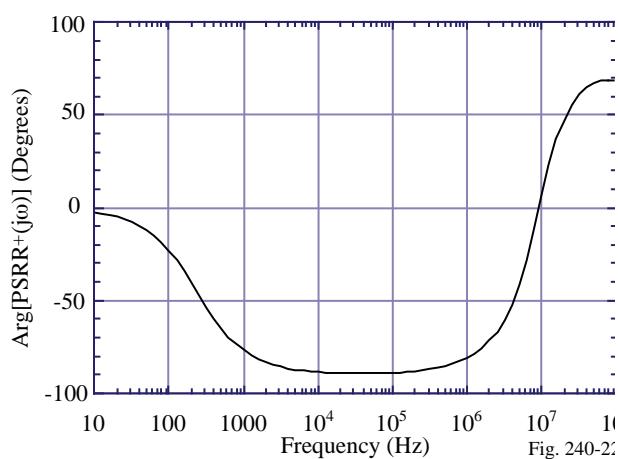
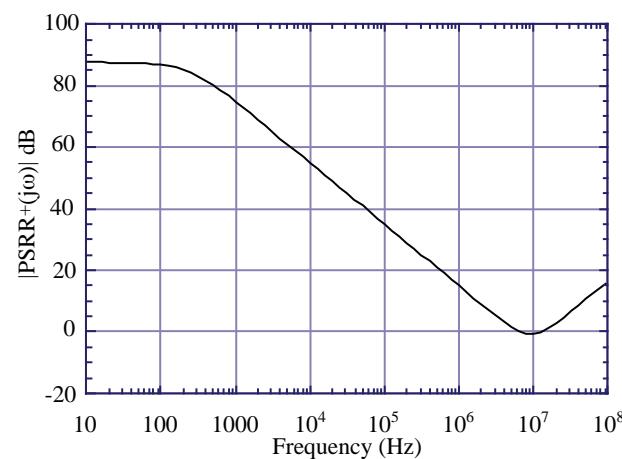
Example 250-1 - ContinuedPositive $PSRR$:

Fig. 240-22

This $PSRR^+$ is poor because of the Miller capacitor. The degree of $PSRR^+$ deterioration will be better shown when compared with the $PSRR^-$.

Example 250-1 - Continued

Negative PSRR:

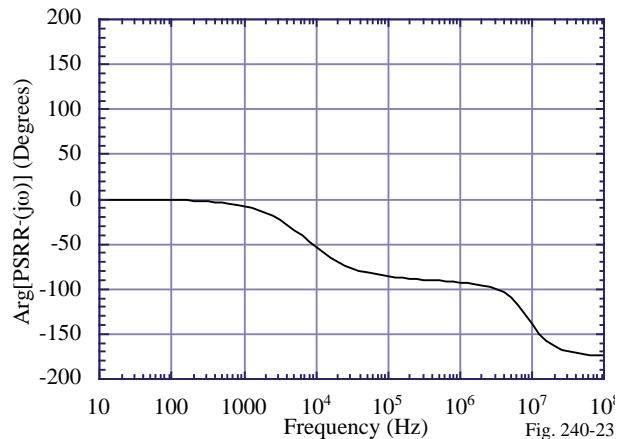
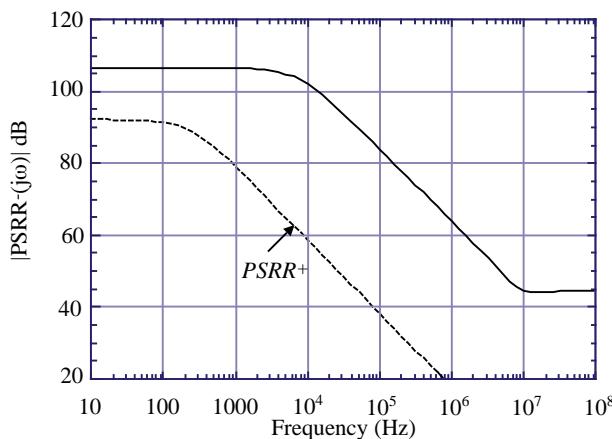


Fig. 240-23

Example 250-1 - Continued

Large-signal and small-signal transient response:

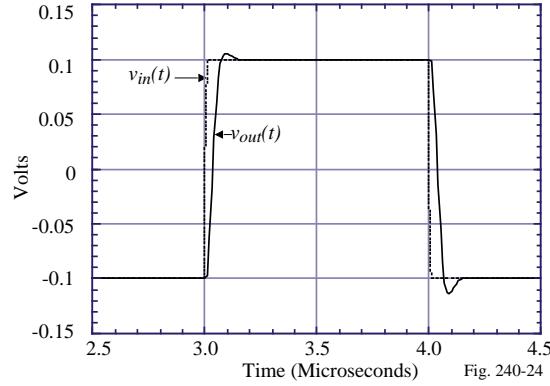
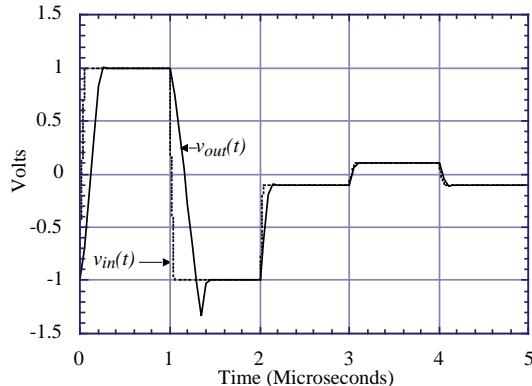


Fig. 240-24

Why the negative overshoot on the slew rate?

If M7 cannot sink sufficient current then the output stage slews and only responds to changes at the output via the feedback path which involves a delay.

Note that $-dv_{out}/dt \approx -2V/0.3\mu s = -6.67V/\mu s$. For a 10pF capacitor this requires $66.7\mu A$ and only $95\mu A - 66.7\mu A = 28\mu A$ is available for C_c . For the positive slew rate, M6 can provide whatever current is required by the capacitors and can immediately respond to changes at the output.

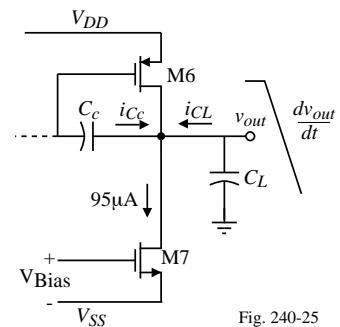


Fig. 240-25

Example 250-1 - Continued

Comparison of the Simulation Results with the Specifications of Example 250-1:

Specification (Power supply = $\pm 2.5V$)	Design	Simulation
Open Loop Gain	>5000	10,000
GB (MHz)	5 MHz	5 MHz
Input CMR (Volts)	-1V to 2V	-1.2 V to 2.4 V,
Slew Rate ($V/\mu\text{sec}$)	>10 ($V/\mu\text{sec}$)	+10, -7($V/\mu\text{sec}$)
Pdiss (mW)	< 2mW	0.625mW
Vout range (V)	$\pm 2V$	+2.3V, -2.2V
PSRR+ (0) (dB)	-	87
PSRR- (0) (dB)	-	106
Phase margin (degrees)	60°	65°
Output Resistance ($k\Omega$)	-	122.5kΩ

Relative Overshoots of Ex. 250-1

Why is the negative-going overshoot larger than the positive-going overshoot on the small-signal transient response of the last slide?

Consider the following circuit and waveform:

During the rise time,

$$i_{CL} = C_L(dv_{out}/dt) = 10\text{pF}(0.2\text{V}/0.1\mu\text{s}) = 20\mu\text{A} \text{ and } i_{Cc} = 3\text{pf}(2\text{V}/\mu\text{s}) = 6\mu\text{A}$$

$$\therefore i_6 = 95\mu\text{A} + 20\mu\text{A} + 6\mu\text{A} = 121\mu\text{A} \Rightarrow g_{m6} = 1066\mu\text{S} \text{ (nominal was } 942.5\mu\text{S)}$$

$$\text{During the fall time, } i_{CL} = C_L(-dv_{out}/dt) = 10\text{pF}(-0.2\text{V}/0.1\mu\text{s}) = -20\mu\text{A}$$

$$\text{and } i_{Cc} = -3\text{pf}(2\text{V}/\mu\text{s}) = -6\mu\text{A}$$

$$\therefore i_6 = 95\mu\text{A} - 20\mu\text{A} - 6\mu\text{A} = 69\mu\text{A} \Rightarrow g_{m6} = 805\mu\text{S}$$

The dominant pole is $p_1 \approx (R_{Ig_m6}R_{II}C_c)^{-1}$ but the GB is $g_{mI}/C_c = 94.25\mu\text{S}/3\text{pF} = 31.42 \times 10^6 \text{ rads/sec}$ and stays constant. Thus we must look elsewhere for the reason. Recall that $p_2 \approx g_{m6}/C_L$ which explains the difference.

$\therefore p_2(95\mu\text{A}) = 94.25 \times 10^6 \text{ rads/sec}$, $p_2(121\mu\text{A}) = 106.6 \times 10^6 \text{ rads/sec}$, and $p_2(69\mu\text{A}) = 80.05 \times 10^6 \text{ rads/sec}$. Thus, the phase margin is less during the fall time than the rise time.

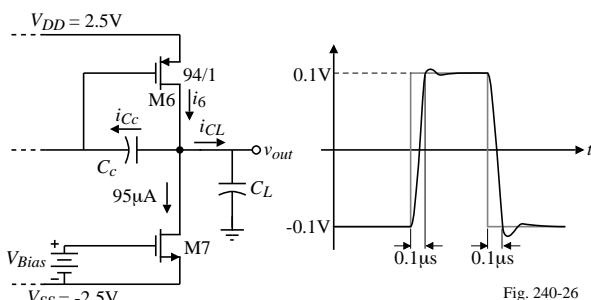


Fig. 240-26

OP AMP MACROMODELS

What is a Macromodel?

A *macromodel* uses resistors, capacitors, inductors, controlled sources, and some active devices (mostly diodes) to capture the essence of the performance of a complex circuit like an op amp without modeling every internal component of the op amp.

Small Signal, Frequency Independent Op Amp Macromodel

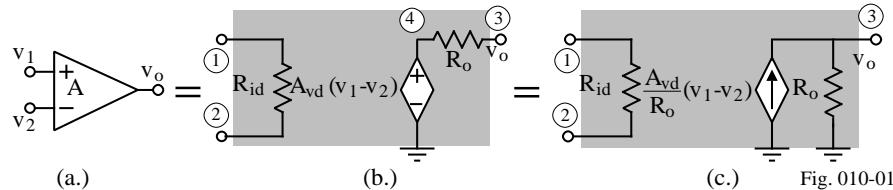


Figure 1 - (a.) Op amp symbol. (b.) Thevenin form. (c.) Norton form.

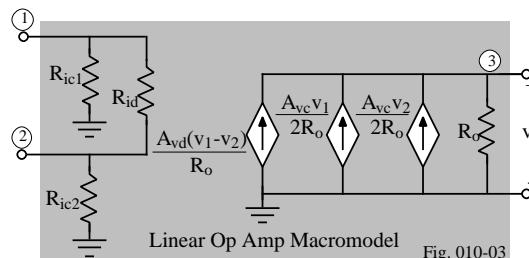


Figure 2 - Simple op amp model including differential and common mode behavior.

Small Signal, Frequency Dependent Op Amp Macromodel

$$A_{vd}(s) = \frac{A_{vd}(0)}{(s/\omega_1) + 1} \quad \text{where } \omega_1 = \frac{1}{R_1 C_1} \quad (\text{dominant pole})$$

Model Using Passive Components:

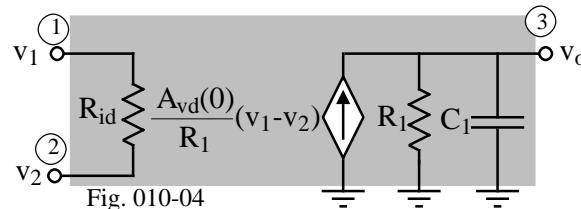


Figure 3 - Macromodel for the op amp including the frequency response of A_{vd} .

Model Using Passive Components with Constant Output Resistance:

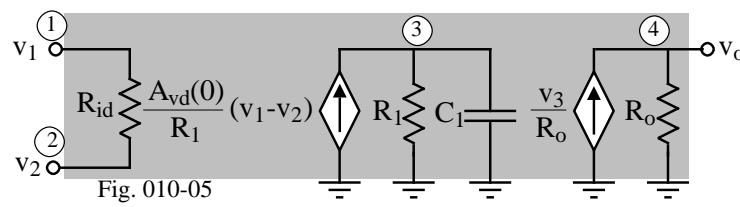


Figure 4 - Frequency dependent model with constant output resistance.

Large Signal, Frequency Independent Op Amp Macromodel

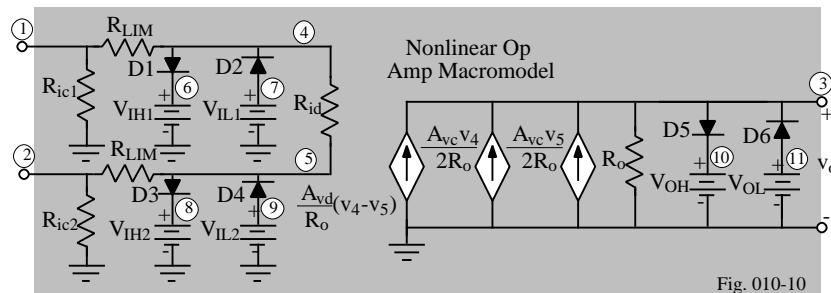


Figure 5 - Op amp macromodel that limits the input and output voltages.

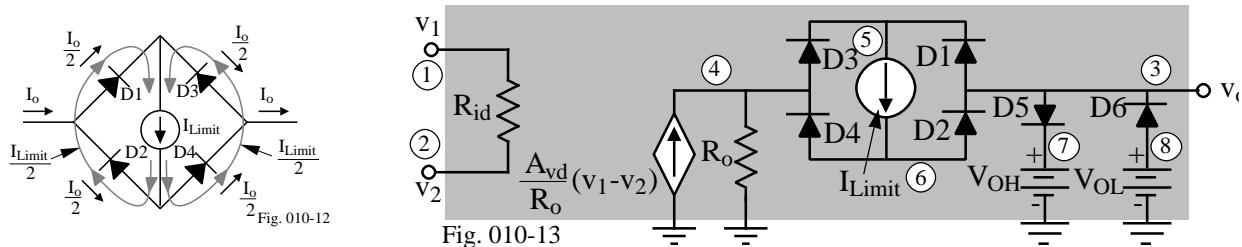


Figure 6 – Technique for current limiting and a macromodel for output voltage and current limiting.

Large Signal, Frequency Dependent Op Amp Macromodel

Slew Rate:

$$\frac{dv_o}{dt} = \frac{\pm I_{SR}}{C_1} = \text{Slew Rate}$$

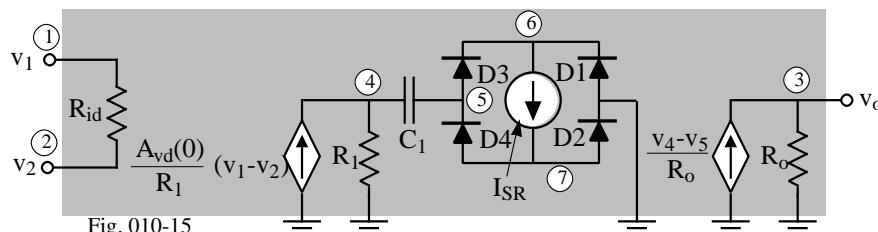
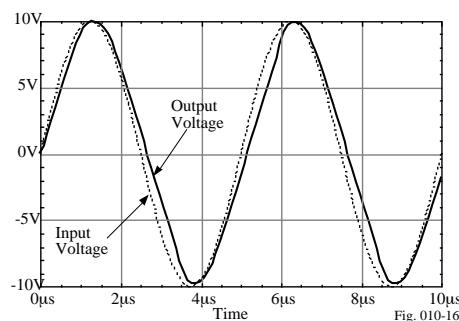


Figure 7 – Slew rate macromodel for an op amp.

Results for a unity gain op amp in slew:



SUMMARY

- Simulation and measurement of op amps has both similarities and differences
- Measurement of open loop gain is very challenging – the key is to keep the quiescent point output of the op amp well defined
- The method of stimulating the output of the op amp or power supplies and letting the input respond results in a robust method of measuring open loop gain, $CMRR$, and $PSRR$
- Carefully investigate any deviations or aberrations from expected behavior in the simulation and experimental results
- Macromodels are useful for modeling the op amp without including every individual transistor

LECTURE 260 – BUFFERED OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Open Loop Buffered Op Amps
- Closed Loop Buffered Op Amps
- Use of the BJT in Buffered Op Amps
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 352-368

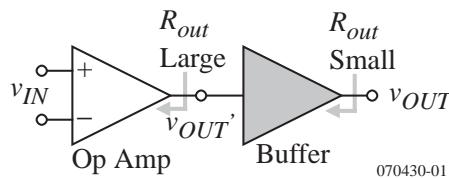
INTRODUCTION

Buffered Op Amps

What is a buffered op amp?

Buffered op amps are op amps with the ability to drive a low output resistance and/or a large output capacitance. This requires:

- An output resistance typically in the range of $10\Omega \leq R_o \leq 1000\Omega$
- Ability to sink and source sufficient current ($C_L \cdot SR$)



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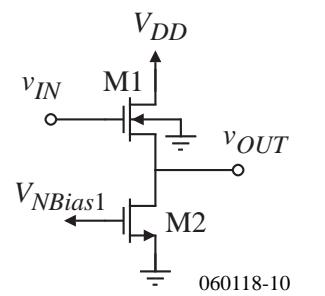
Types of buffered op amps:

- Open loop using output amplifiers
- Closed loop using negative shunt feedback to reduce the output resistance of the op amp

OPEN LOOP BUFFERED OP AMPS

The Class A Source Follower as a Buffer

- Simple
- Small signal gain $\approx \frac{g_m}{g_m + g_{mbs} + G_L} < 1$
- Low efficiency
- $R_{out} = \frac{1}{g_m + g_{mbs}} \approx 500$ to 1000Ω
- Level shift from input to output
- Maximum upper output voltage is limited
- Broadbanded as the pole and zero due to the source follower are close so compensation is typically not a problem



The Push-Pull Follower as a Buffer

- Voltage loss from 2 cascaded followers

$$A_v \approx \left(\frac{g_{m3}}{g_{m3} + g_{mbs3}} \right) \left(\frac{g_{m1}}{g_{m1} + g_{mbs1} + G_L} \right) < 1$$

- Higher efficiency

$$\bullet R_{out} \approx \frac{0.5}{g_m + g_{mbs}} \approx 250 \text{ to } 500\Omega$$

- Current in M1 and M2 determined by:

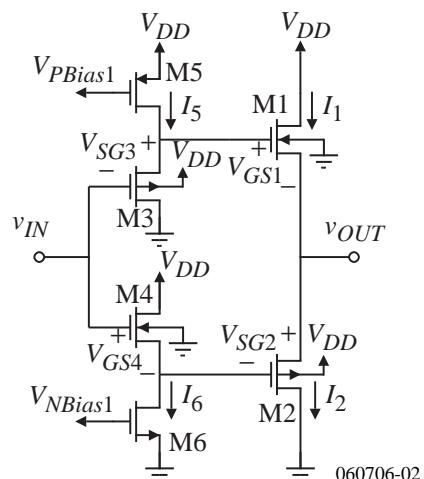
$$V_{GS4} + V_{SG3} = V_{GS1} + V_{SG2}$$

$$\sqrt{\frac{2I_6}{K_n'(W_4/L_4)}} + \sqrt{\frac{2I_5}{K_p'(W_3/L_3)}}$$

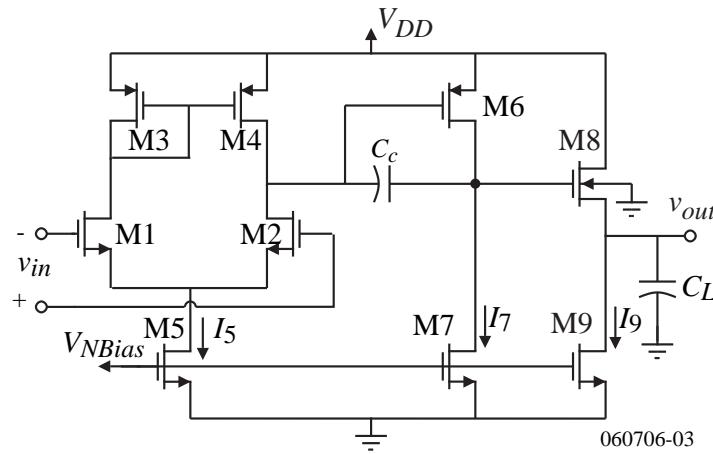
$$= \sqrt{\frac{2I_1}{K_n'(W_1/L_1)}} + \sqrt{\frac{2I_2}{K_p'(W_2/L_2)}}$$

Use the W/L ratios to define I_1 and I_2 from I_5 and I_6

- Maximum positive and negative output voltages are limited



Two-Stage Op Amp with Follower

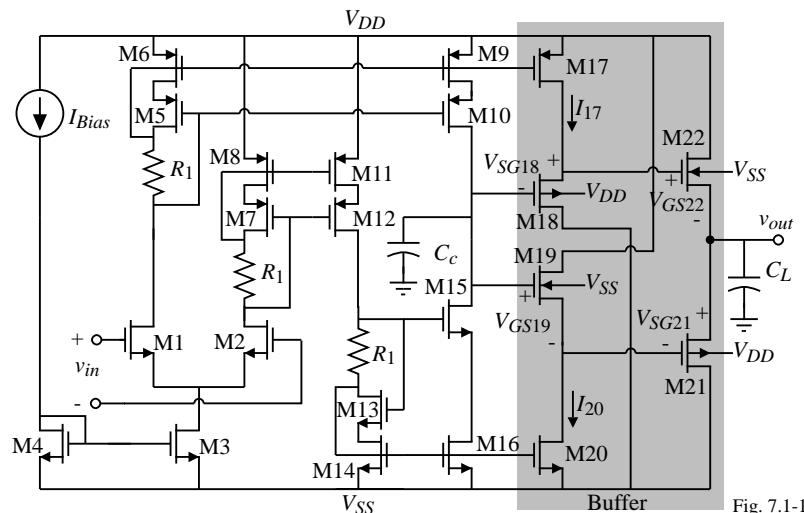


Power dissipation now becomes $(I_5 + I_7 + I_9)V_{DD}$

Gain becomes,

$$A_v = \left(\frac{g_m 1}{g_{ds2} + g_{ds4}} \right) \left(\frac{g_m 6}{g_{ds6} + g_{ds7}} \right) \left(\frac{g_m 8}{g_{m8} + g_{mbs8} + g_{ds8} + g_{ds9}} \right)$$

Source-Follower, Push-Pull Output Op Amp



$$R_{out} \approx \frac{1}{g_{m21} + g_{m22}} \leq 1000\Omega, A_v(0)=65\text{dB} (I_{Bias}=50\mu\text{A}), \text{ and } GB = 60\text{MHz} \text{ for } C_L = 1\text{pF}$$

Note the bias currents through M18 and M19 vary with the signal.

Compensation of Op Amps with Output Amplifiers

Compensation of a three-stage amplifier:

This op amp introduces a third pole, p'_3 (what about zeros?)

With no compensation,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-A_{vo}}{\left(\frac{s}{p'_1} - 1\right)\left(\frac{s}{p'_2} - 1\right)\left(\frac{s}{p'_3} - 1\right)}$$

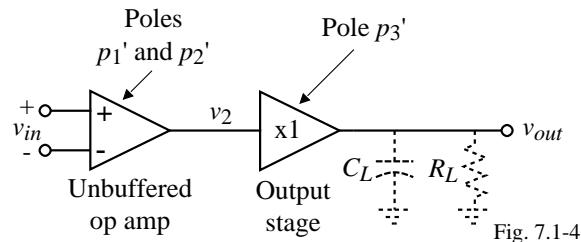
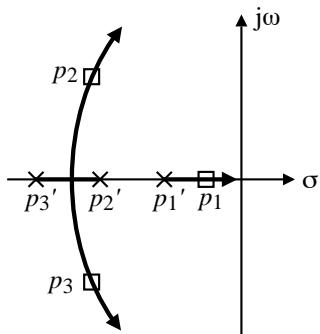
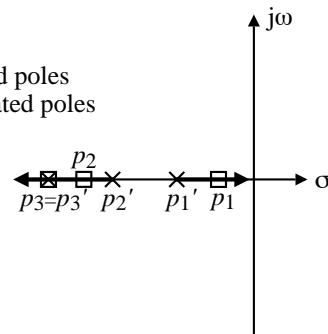


Fig. 7.1-4

Illustration of compensation choices:



Miller compensation applied around both the second and the third stage.

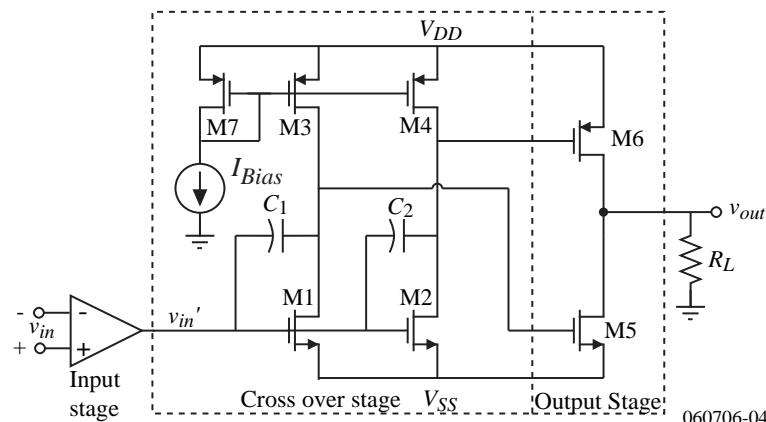


Miller compensation applied around the second stage only.

Fig. 7.1-5

Crossover-Inverter, Buffer Stage Op Amp

Principle: If the buffer has high output resistance and voltage gain (common source), this is okay if when loaded by a small R_L the gain of this stage is approximately unity.



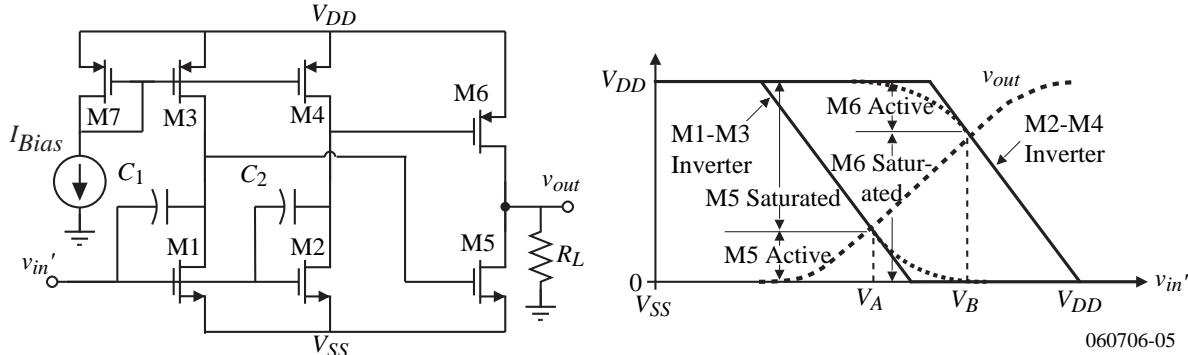
- This buffer trades gain for the ability to drive a low load resistance
- The load resistance should be fixed in order to avoid changes in the buffer gain
- The push-pull common source output will give good output voltage swing capability

Crossover-Inverter, Buffer Stage Op Amp - Continued

How does the output buffer work?

The two inverters, M1-M3 and M2-M4 are designed to work over different regions of the buffer input voltage, v_{in}' .

Consider the idealized voltage transfer characteristic of the crossover inverters:



$$\text{Crossover voltage} \equiv V_C = V_B - V_A \geq 0$$

V_C is designed to be small and positive for worst case variations in processing.

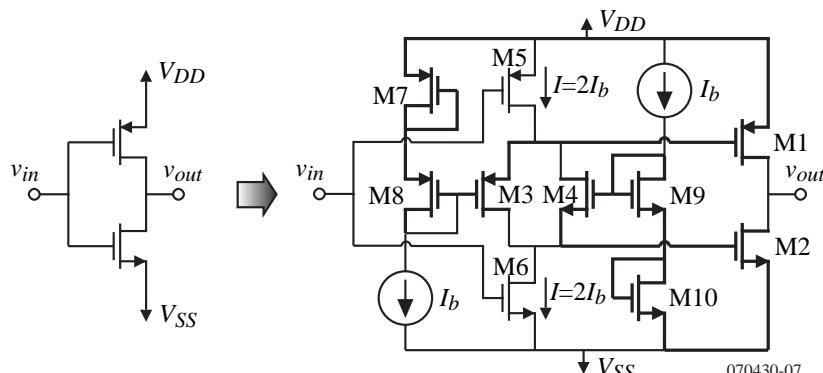
Large Output Current Buffer

In the case where the load consists of a large capacitor, the ability to sink and source a large current is much more important than reducing the output resistance. Consequently, the common-source, push-pull is ideal if the quiescent current can be controlled.

A possible implementation:

If $W_4/L_4 = W_9/L_9$ and $W_3/L_3 = W_8/L_8$, then the quiescent currents in M1 and M2 can be determined by the following relationship:

$$I_1 = I_2 = I_b \left(\frac{W_1/L_1}{W_7/L_7} \right) = I_b \left(\frac{W_2/L_2}{W_{10}/L_{10}} \right)$$

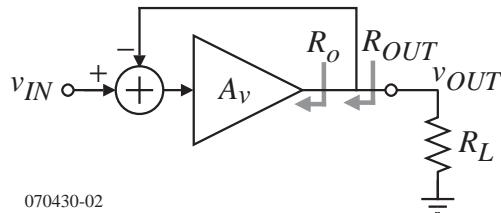


When v_{in} is increased, M6 turns off M2 and turns on M1 to source current. Similarly, when v_{in} is decreased, M5 turns off M1 and turns on M2 to sink current.

CLOSED LOOP BUFFERED OP AMPS

Principle

Use negative shunt feedback to reduce the output resistance of the buffer.

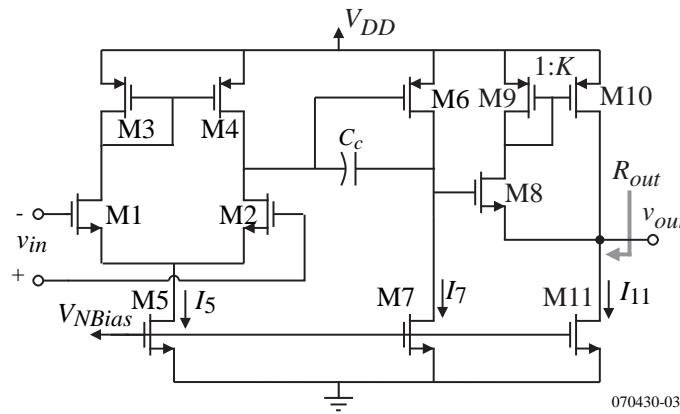


- Output resistance

$$R_{OUT} = \frac{R_o}{1 + A_v}$$

- Watch out for the case when R_L causes A_v to decrease.
- The bandwidth will be limited by the feedback (i.e. at high frequencies, the gain of A_v decreases causing the output resistance to increase).

Two Stage Op Amp with a Gain Boosted, Source Follower Buffer



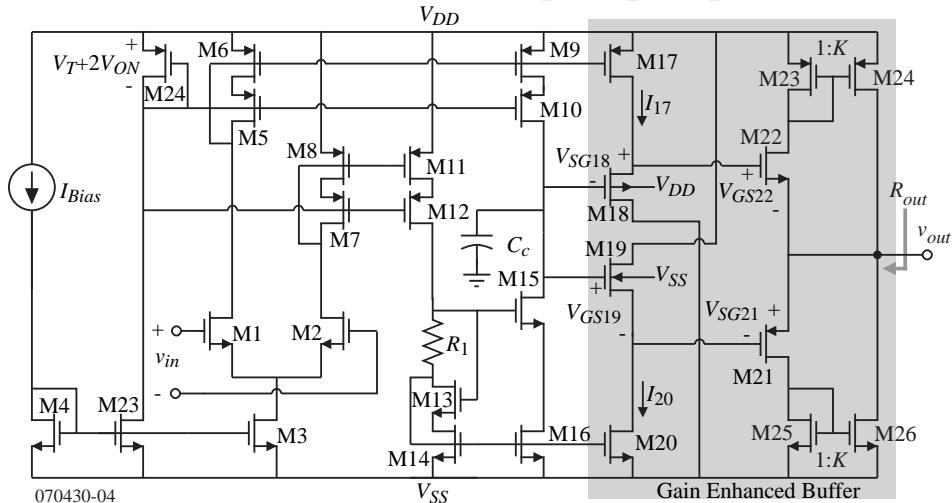
$$R_{out} \approx \frac{1}{g_m 8 K}$$

Power dissipation now becomes $(I_5 + I_7 + I_{11})V_{DD}$

Gain becomes,

$$A_v = \left(\frac{g_m 1}{g_{ds2} + g_{ds4}} \right) \left(\frac{g_m 6}{g_{ds6} + g_{ds7}} \right) \left(\frac{g_m 8 K}{g_m 8 K + g_{mbs8} K + G_L} \right)$$

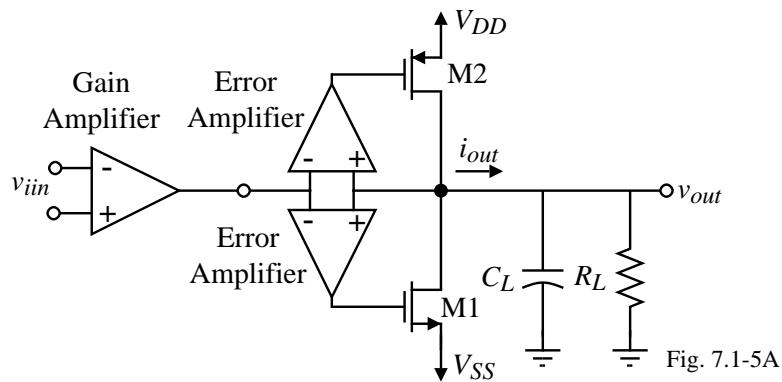
Gain Boosted, Source-Follower, Push-Pull Output Op Amp



Common Source, Push Pull Buffer with Shunt Feedback

To get low output resistance using MOSFETs, negative feedback must be used.

Ideal implementation:



Comments:

- The output resistance will be equal to $r_{ds1}\parallel r_{ds2}$ divided by the loop gain
- If the error amplifiers are not perfectly matched, the bias current in M1 and M2 is not defined

Low Output Resistance Op Amp - Continued

Offset correction circuitry:

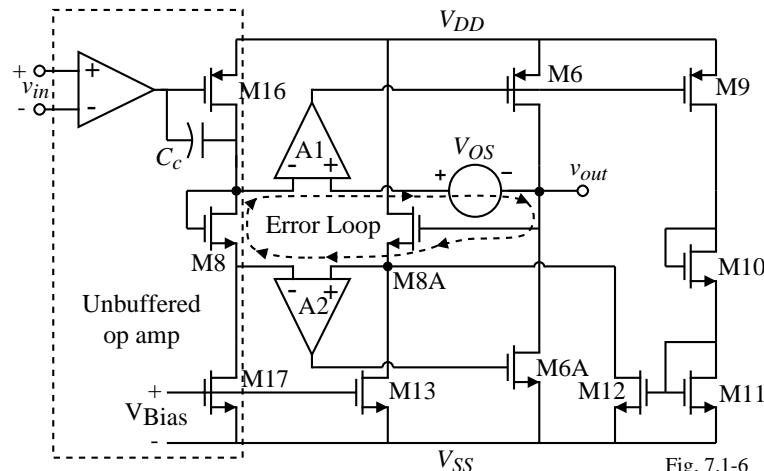


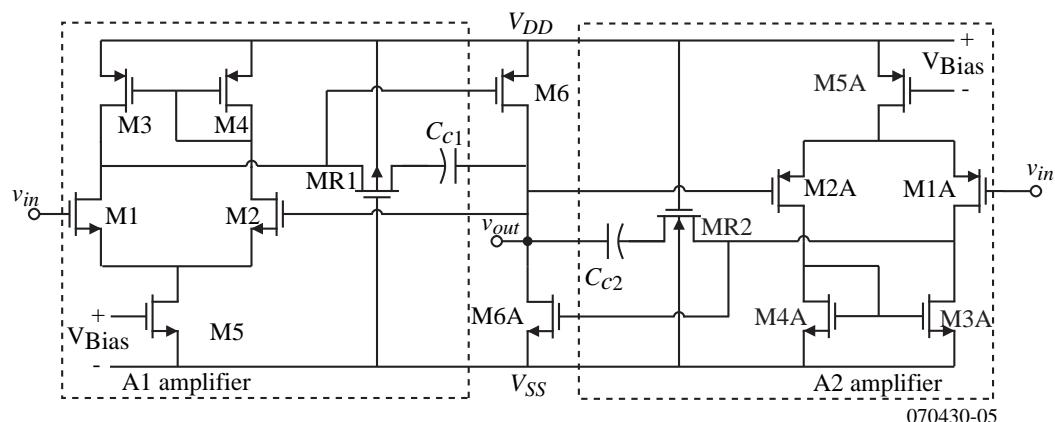
Fig. 7.1-6

The feedback circuitry of the two error amplifiers tries to insure that the voltages in the loop sum to zero. Without the M9-M12 feedback circuit, there is no way to adjust the output for any error in the loop. The circuit works as follows:

When V_{OS} is positive, M6 tries to turn off and so does M6A. I_{M9} reduces thus reducing I_{M12} . A reduction in I_{M12} reduces I_{M8A} thus decreasing V_{GS8A} . V_{GS8A} ideally decreases by an amount equal to V_{OS} . A similar result holds for negative offsets and offsets in EA2.

Low Output Resistance Op Amp - Continued

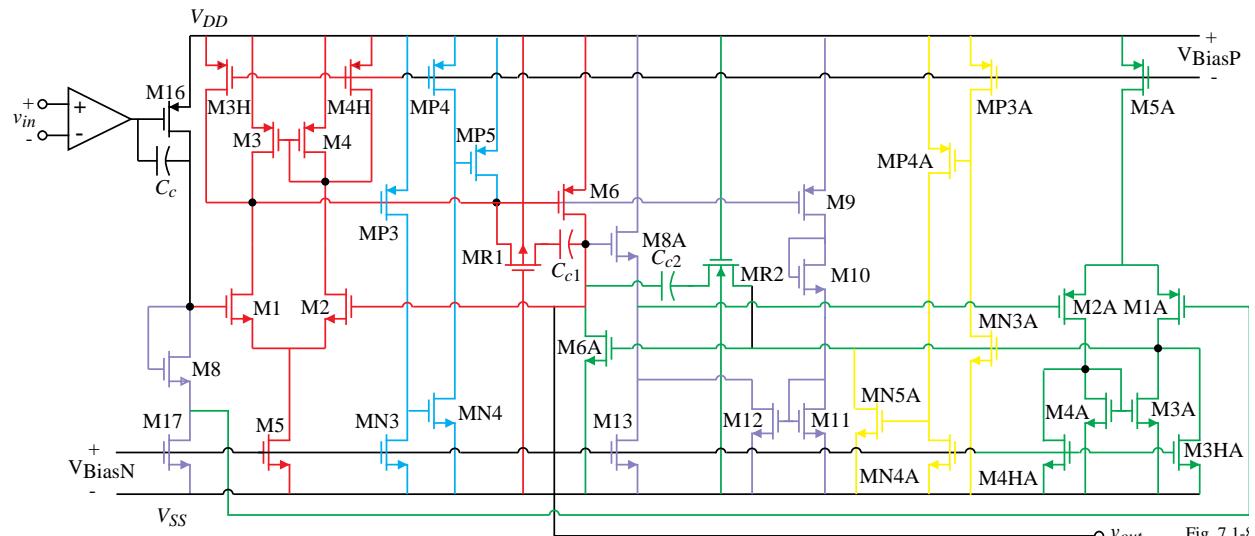
Error amplifiers:



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Basically a two-stage op amp with the output push-pull transistors as the second-stage of the op amp.

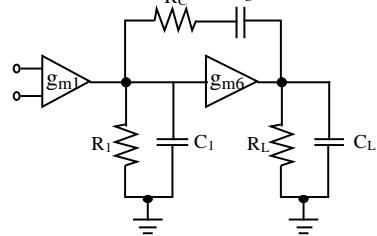
Low Output Resistance Op Amp - Complete Schematic



Short circuit protection(max. output $\pm 60\text{mA}$):

MP3-MN3-MN4-MP4-MP5
MN3A-MP3A-MP4A-MN4A-MN5A

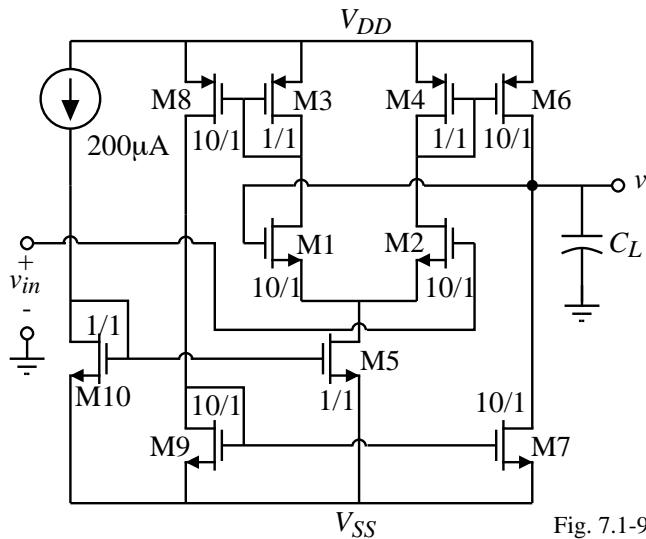
$$R_{out} \approx \frac{r_{ds6} \| r_{ds6A}}{\text{Loop Gain}} \approx \frac{50\text{k}\Omega}{5000} = 10\Omega$$



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Simpler Implementation of Negative Feedback to Achieve Low Output Resistance



Output Resistance:

$$R_{out} = \frac{R_o}{1+LG}$$

where

$$R_o = \frac{1}{g_{ds6} + g_{ds7}}$$

and

$$|LG| = \frac{g_{m2}}{2g_{m4}} (g_{m6} + g_{m7}) R_o$$

Therefore, the output resistance is:

$$R_{out} = \frac{1}{(g_{ds6} + g_{ds7}) \left[1 + \left(\frac{g_{m2}}{2g_{m4}} \right) (g_{m6} + g_{m7}) R_o \right]}$$

Example 260-1 - Low Output Resistance Using Shunt Negative Feedback Buffer

Find the output resistance of above op amp using the model parameters of $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, $\lambda_N = 0.06V^{-1}$ and $\lambda_P = 0.08V^{-1}$.

Solution

The current flowing in the output transistors, M6 and M7, is 1mA which gives R_o of

$$R_o = \frac{1}{(\lambda_N + \lambda_P)1\text{mA}} = \frac{1000}{0.14} = 7.143\text{k}\Omega$$

To calculate the loop gain, we find that

$$g_{m2} = \sqrt{2K_N' \cdot 10 \cdot 100\mu A} = 490\mu S$$

$$g_{m4} = \sqrt{2K_P' \cdot 1 \cdot 100\mu A} = 70.7\mu S$$

and

$$g_{m6} = \sqrt{2K_P' \cdot 10 \cdot 1000\mu A} = 707\mu S$$

Therefore, the loop gain is

$$|LG| = \frac{490}{2 \cdot 70.7} (0.707 + 0.071) 7.143 = 19.26$$

Solving for the output resistance, R_{out} , gives

$$R_{out} = \frac{7.143\text{k}\Omega}{1 + 19.26} = 353\Omega \quad (\text{Assumes that } R_L \text{ is large})$$

USE OF THE BJT IN BUFFERED OP AMPS

Substrate BJTs

Illustration of an NPN substrate BJT available in a p-well CMOS technology:

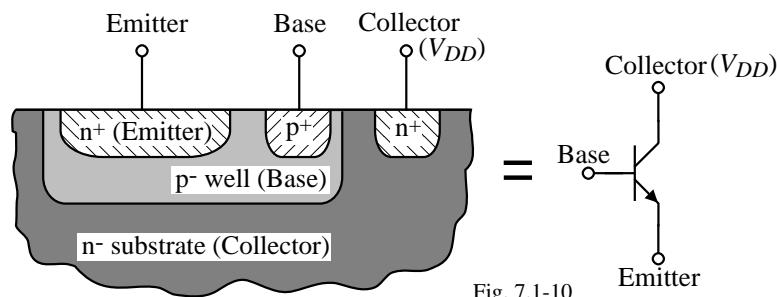


Fig. 7.1-10

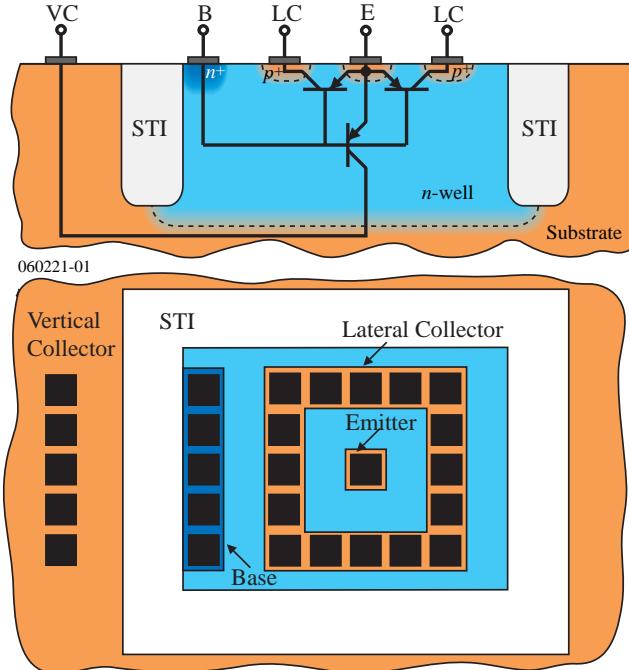
Comments:

- g_m of the BJT is larger than the FET so that the output resistance w/o feedback is lower
- Collector current will be flowing in the substrate
- Current is required to drive the BJT
- Only an NPN or a PNP bipolar transistor is available

A Lateral Bipolar Transistor

n-well CMOS technology:

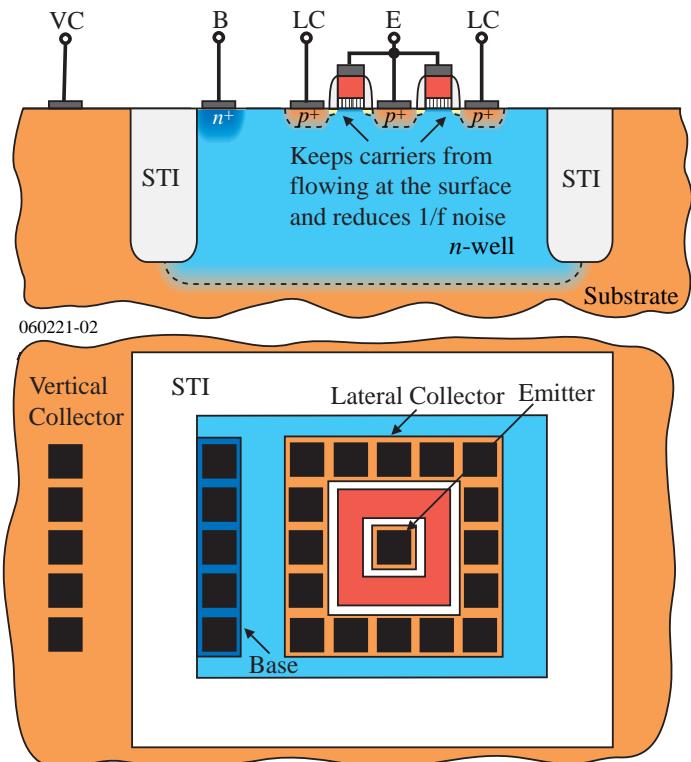
- It is desirable to have the lateral collector current much larger than the vertical collector current.
- Triple well technology allows the current of the vertical collector to avoid flowing in the substrate.
- Lateral BJT generally has good matching.



A Field-Aided Lateral BJT

Use minimum channel length to enhance beta:

$\beta_F \approx 50$ to 100 depending on the process



Two-Stage Op Amp with a Class-A BJT Output Buffer Stage

Purpose of the M8-M9 source follower:

- 1.) Reduce the output resistance (includes whatever is seen from the base to ground divided by $1+\beta_F$)
- 2.) Reduces the output load at the drains of M6 and M7

Small-signal output resistance :

$$R_{out} \approx \frac{r_{\pi 10} + (1/g_{m9})}{1+\beta_F} = \frac{1}{g_{m10}} + \frac{1}{g_{m9}(1+\beta_F)}$$

$= 51.6\Omega + 6.7\Omega = 58.3\Omega$ where $I_{10}=500\mu A$, $I_8=100\mu A$, $W_9/L_9=100$ and β_F is 100

$$v_{OUT}(\max) = V_{DD} - V_{SD8}(\text{sat}) - v_{BE10} = V_{DD} - \sqrt{\frac{2K_P'}{I_8(W_8/L_8)}} - V_t \ln\left(\frac{I_{c10}}{I_{s10}}\right)$$

Voltage gain:

$$\frac{v_{out}}{v_{in}} \approx \left(\frac{g_{m1}}{g_{ds2}+g_{ds4}} \right) \left(\frac{g_{m6}}{g_{ds6}+g_{ds7}} \right) \left(\frac{g_{m9}}{g_{m9}+g_{mbs9}+g_{ds8}+g_{\pi 10}} \right) \left(\frac{g_{m10}R_L}{1+g_{m10}R_L} \right)$$

Compensation will be more complex because of the additional stages.

Example 260-2 - Designing the Class-A, Buffered Op Amp

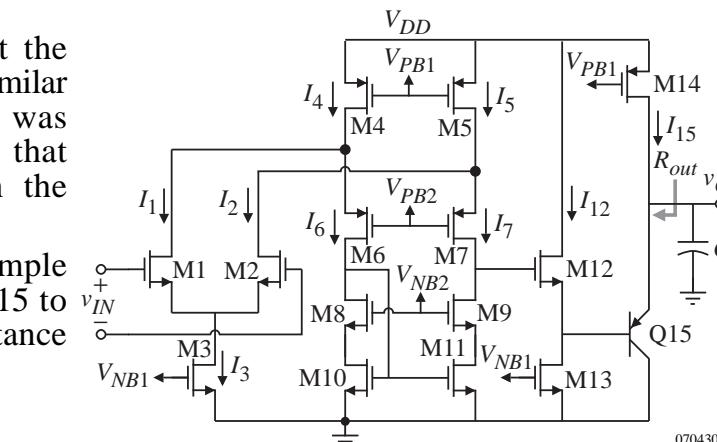
Use an *n*-well, $0.25\mu m$ CMOS technology to design an op amp using a class-A, BJT output stage to give the following specifications. Assume the channel length is to be $0.5\mu m$. The FETs have the model parameters of $K_N' = 120\mu A/V^2$, $K_P' = 25\mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5V$, $\lambda_N = 0.06V^{-1}$ and $\lambda_P = 0.08V^{-1}$ along with the BJT parameters of $I_s = 10^{-14}A$ and $\beta_F = 50$.

$$\begin{array}{llll} V_{DD} = 2.5V & V_{SS} = 0V & GB = 5MHz & A_{vd}(0) \geq 2500V/V \\ R_L = 500\Omega & R_{out} \leq 50\Omega & C_L = 100pF & \text{Slew rate} \geq 10V/\mu s \\ I_{CMR} = +1V \text{ to } 2V & & & \end{array}$$

Solution

A quick comparison shows that the specifications of this problem are similar to the folded cascode op amp that was designed in Ex. 240-3. Borrowing that design for this example results in the following op amp.

Therefore, the goal of this example will be the design of M12 through Q15 to satisfy the slew rate and output resistance requirements.



Example 260-2 – Continued

BJT follower (Q15):

$SR = 10V/\mu s$ and $100pF$ capacitor give $I_{15} = 1mA$.

\therefore Assuming the gate of M14 is connected to the gate of M5, the W/L ratio of M14 becomes

$$W_{14}/L_{14} = (1000\mu A/125\mu A)160 = 1280 \Rightarrow W_{14} = 640\mu m$$

$$I_{15} = 1mA \Rightarrow 1/g_{m15} = 0.0258V/1mA = 25.8\Omega$$

MOS follower:

To source $1mA$, the BJT requires $20\mu A$ ($\beta = 50$) from the MOS follower (M12-M13).

Therefore, select a bias current of $100\mu A$ for M13. If the gates of M3 and M13 are connected together, then

$$W_{13}/L_{13} = (100\mu A/100\mu A)15 = 15 \Rightarrow W_{13} = 7.5\mu m$$

To get $R_{out} = 50\Omega$, if $1/g_{m15}$ is 25.8Ω , then design g_{m12} as

$$\frac{1}{g_{m15}} = \frac{1}{g_{m12}(1+\beta_F)} = 24.2\Omega \rightarrow g_{m12} = \frac{1}{(24.2\Omega)(1+\beta_F)} = \frac{1}{24.2 \cdot 51} = 810\mu S$$

$$\therefore g_{m12} \text{ and } I_{12} \Rightarrow W/L = 27.3 \approx 30 \Rightarrow W_{12} = 15\mu m$$

Example 260-2 - Continued

To calculate the voltage gain of the MOS follower we need to find g_{mbs9} ($\gamma_N = 0.4\sqrt{V}$).

$$\therefore g_{mbs12} = \frac{g_{m12}\gamma_N}{2\sqrt{2\phi_F + V_{BS12}}} = \frac{810 \cdot 0.4}{2\sqrt{0.5+0.55}} = 158\mu S$$

where we have assumed that the value of V_{SB12} is approximately $1.25V - 0.7V = 0.55V$.

$$\therefore A_{MOS} = \frac{810\mu S}{810\mu S + 158\mu S + 6\mu S + 8\mu S} = 0.825$$

The voltage gain of the BJT follower is

$$A_{BJT} = \frac{500}{25.8+500} = 0.951 \text{ V/V}$$

Thus, the gain of the op amp is

$$A_{vd}(0) = (3,678)(0.825)(0.951) = 2,885 \text{ V/V}$$

The power dissipation of this amplifier is,

$$P_{diss.} = 2.5V(125\mu A + 125\mu A + 100\mu A + 1000\mu A) = 3.375\text{mW}$$

The signal swing across the 500Ω load resistor will be restricted to $\pm 0.5V$ due to the $1000\mu A$ output current limit.

SUMMARY

- A buffered op amp requires an output resistance between $10\Omega \leq R_o \leq 1000\Omega$
- Output resistance using MOSFETs only can be reduced by,
 - Source follower output ($1/g_m$)
 - Negative shunt feedback (frequency is a problem in this approach)
- Use of substrate (or lateral) BJT's can reduce the output resistance because g_m is larger than the g_m of a MOSFET
- Adding a buffer stage to lower the output resistance will most likely complicate the compensation of the op amp

LECTURE 270 – HIGH SPEED OP AMPS

LECTURE ORGANIZATION

Outline

- Extending the GB of conventional op amps
- Cascade Amplifiers
 - Voltage amplifiers
 - Voltage amplifiers using current feedback
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

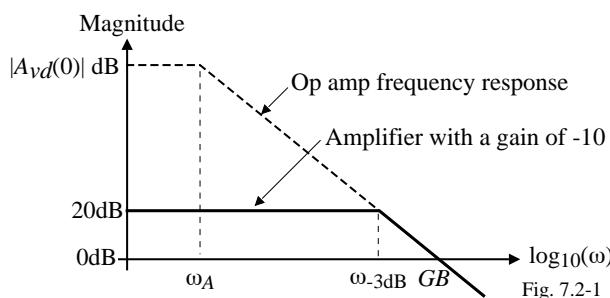
Pages 368-384

INCREASING THE GB OF OP AMPS

What is the Influence of GB on the Frequency Response?

The unity-gainbandwidth represents a limit in the trade-off between closed loop voltage gain and the closed-loop -3dB frequency.

Example of a gain of -10 voltage amplifier:



What defines the *GB*?

We know that

$$GB = \frac{g_m}{C}$$

where g_m is the transconductance that converts the input voltage to current and C is the capacitor that causes the dominant pole.

This relationship assumes that all higher-order poles are greater than *GB*.

What is the Limit of GB ?

The following illustrates what happens when the next higher pole is not greater than GB :

For a two-stage op amp, the poles and zeros are:

$$1.) \text{ Dominant pole } p_1 = \frac{-g_{m1}}{A_v(0)C_c}$$

$$2.) \text{ Output pole } p_2 = \frac{-g_{m6}}{C_L}$$

$$3.) \text{ Mirror pole } p_3 = \frac{-g_{m3}}{C_{gs3} + C_{gs4}} \text{ and } z_3 = 2p_3$$

$$4.) \text{ Nulling pole } p_4 = \frac{-1}{R_z C_I}$$

$$5.) \text{ Nulling zero } z_1 = \frac{-1}{R_z C_c - (C_c/g_{m6})}$$

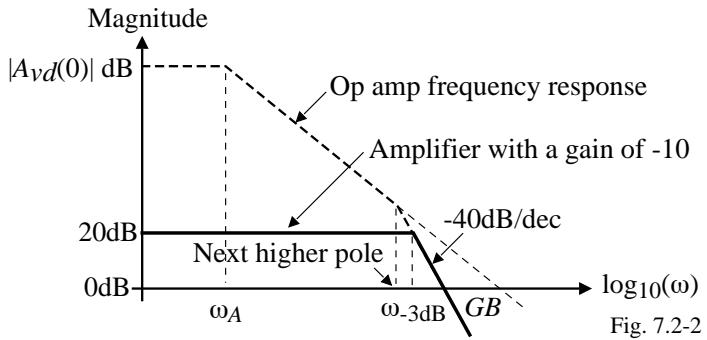
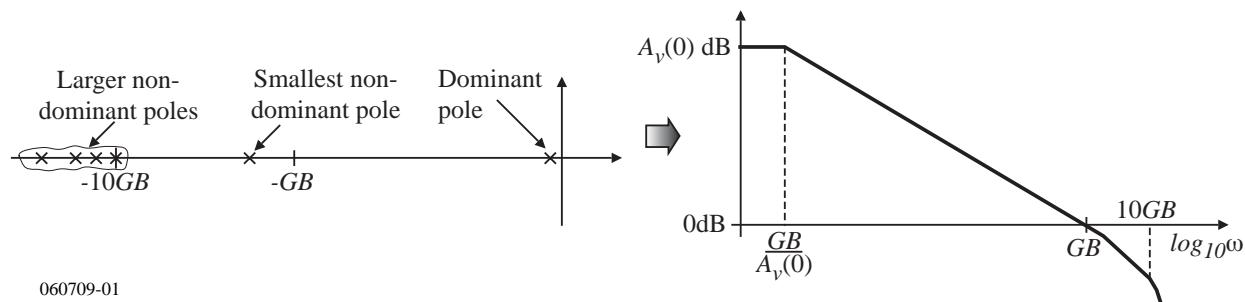


Fig. 7.2-2

Higher-Order Poles

For reasonable phase margin, the smallest higher-order pole should be 2-3 times larger than GB if all other higher-order poles are larger than $10GB$.

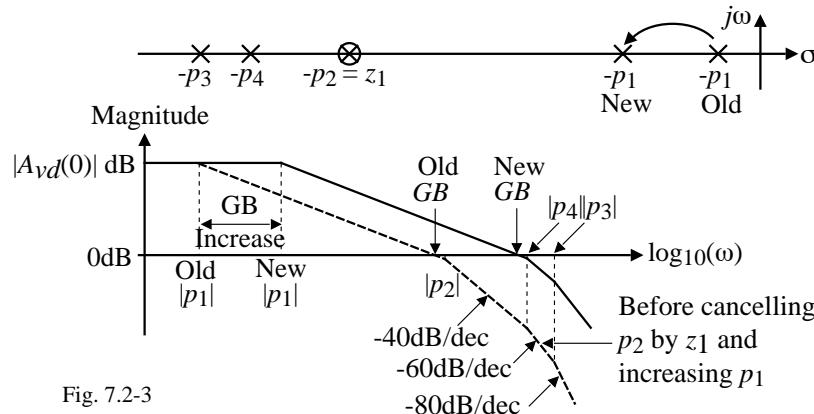


If the higher-order poles are not greater than $10GB$, then the distance from GB to the smallest non-dominant pole should be increased for reasonable phase margin.

Increasing the GB of a Two-Stage Op Amp

- 1.) Use the nulling zero to cancel the closest pole beyond the dominant pole.
- 2.) The maximum GB would be equal to the magnitude of the second closest pole beyond the dominant pole.
- 3.) Adjust the dominant pole so that $2.2GB \approx$ (second closest pole beyond the dominant pole)

Illustration which assumes that p_2 is the next closest pole beyond the dominant pole:



Example 270-1 - Increasing the GB of the Op Amp Designed in Ex. 230-1

Use the two-stage op amp designed in Example 230-1 and apply the above approach to increase the gainbandwidth as much as possible. Use the capacitor values in the table shown along with $C_{ox} = 6fF/\mu m^2$.

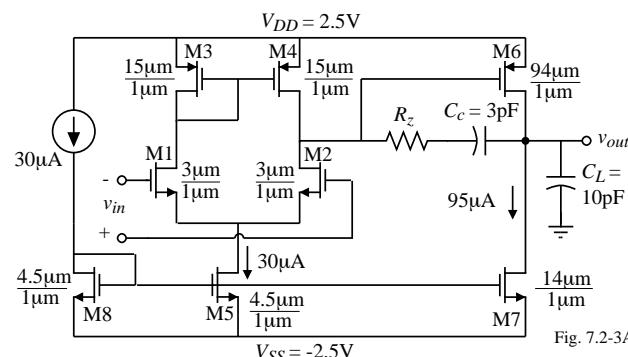
Solution

- 1.) First find the values of p_2 , p_3 , and p_4 .
 - a.) From Ex. 230-2, we see that

$$p_2 = -95 \times 10^6 \text{ rads/sec.}$$

b.) p_3 was found in Ex. 6.3-1 as

$$p_3 = -1.25 \times 10^9 \text{ rads/sec. (also there is a zero at } -2.5 \times 10^9 \text{ rads/sec.)}$$



Type	P-Channel	N-Channel	Units
CGSO	220×10^{-12}	220×10^{-12}	F/m
CGDO	220×10^{-12}	220×10^{-12}	F/m
CGBO	700×10^{-12}	700×10^{-12}	F/m
CJ	560×10^{-6}	770×10^{-6}	F/m ²
CJSW	350×10^{-12}	380×10^{-12}	F/m
MJ	0.5	0.5	
MJSW	0.35	0.38	

Example 270-1 - Continued

(c.) To find p_4 , we must find C_I which is the output capacitance of the first stage of the op amp. C_I consists of the following capacitors,

$$C_I = C_{bd2} + C_{bd4} + C_{gs6} + C_{gd2} + C_{gd4}$$

For C_{bd2} the width is $1.5\mu\text{m}$ $\Rightarrow L_1+L_2+L_3=3\mu\text{m}$ $\Rightarrow AS/AD=4.5\mu\text{m}^2$ and $PS/PD=9\mu\text{m}$.

For C_{bd4} the width is $15\mu\text{m}$ $\Rightarrow L_1+L_2+L_3=3\mu\text{m}$ $\Rightarrow AS/AD=45\mu\text{m}^2$ and $PS/PD=36\mu\text{m}$.

From Table 3.2-1:

$$C_{bd2} = (4.5\mu\text{m}^2)(770 \times 10^{-6}\text{F/m}^2) + (9\mu\text{m})(380 \times 10^{-12}\text{F/m}) = 3.47\text{fF} + 3.42\text{fF} \approx 6.89\text{fF}$$

$$C_{bd4} = (45\mu\text{m}^2)(560 \times 10^{-6}\text{F/m}^2) + (36\mu\text{m})(350 \times 10^{-12}\text{F/m}) = 25.2\text{fF} + 12.6\text{fF} \approx 37.8\text{fF}$$

C_{gs6} in saturation is,

$$\begin{aligned} C_{gs6} &= CGDO \cdot W_6 + 0.67(C_{ox}W_6L_6) = (220 \times 10^{-12})(85 \times 10^{-6}) + (0.67)(6 \times 10^{-15})(42.5) \\ &= 18.7\text{fF} + 255\text{fF} = 273.7\text{fF} \end{aligned}$$

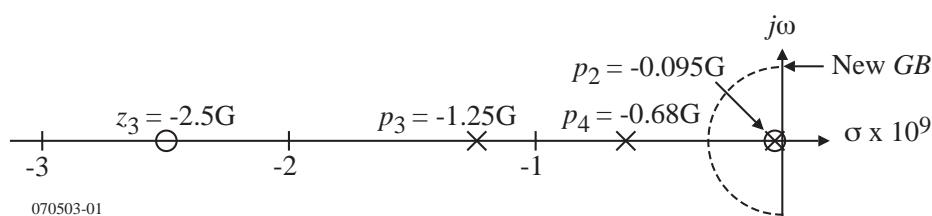
$$C_{gd2} = 220 \times 10^{-12} \times 1.5\mu\text{m} = 0.33\text{fF} \text{ and } C_{gd4} = 220 \times 10^{-12} \times 15\mu\text{m} = 3.3\text{fF}$$

Therefore, $C_I = 6.89\text{fF} + 37.8\text{fF} + 273.7\text{fF} + 0.33\text{fF} + 3.3\text{fF} = 322\text{fF}$. Although C_{bd2} and C_{bd4} will be reduced with a reverse bias, let us use these values to provide a margin. Thus let C_I be 322fF.

In Ex. 230-2, R_z was $4.564\text{k}\Omega$ which gives $p_4 = -0.680 \times 10^9$ rads/sec.

Example 270-1 - Continued

Therefore, the roots are:



When p_2 is cancelled, the next smaller pole is p_4 which will define the new GB . 2.)

Using the nulling zero, z_1 , to cancel p_2 , gives p_4 as the next smallest pole.

For 60° phase margin $GB = |p_4|/2.2$ if the next smallest pole is more than $10GB$.

$$\therefore GB = 0.680 \times 10^9 / 2.2 = 0.309 \times 10^9 \text{ rads/sec. or } 49.2\text{MHz.}$$

This value of GB is designed from the relationship that $GB = g_{m1}/C_c$. Assuming g_{m1} is constant, then $C_c = g_{m1}/GB = (94.25 \times 10^{-6})/(0.309 \times 10^9) = 307\text{fF}$. It might be useful to increase g_{m1} in order to keep C_c above the surrounding parasitic capacitors ($C_{gd6} = 18.7\text{fF}$). The success of this method assumes that there are no other roots with a magnitude smaller than $10GB$.

The result of this example is to increase the GB from 5MHz to 49MHz.

Example 270-2 - Increasing the GB of the Folded Cascode Op Amp of Ex. 240-4

Use the folded-cascode op amp designed in Example 240-4 and apply the above approach to increase the gainbandwidth as much as possible. Assume that the drain/source areas are equal to $2\mu\text{m}$ times the width of the transistor and that all voltage dependent capacitors are at zero voltage.

Solution

The poles of the folded cascode op amp are:

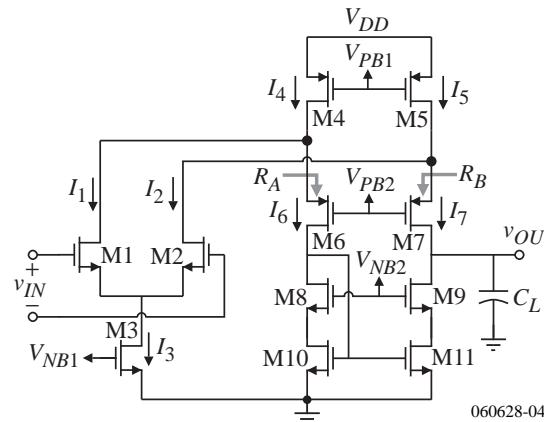
$$p_A \approx \frac{-1}{R_A C_A} \quad (\text{the pole at the source of M6})$$

$$p_B \approx \frac{-1}{R_B C_B} \quad (\text{the pole at the source of M7})$$

$$p_6 \approx \frac{-g_{m10}}{C_6} \quad (\text{the pole at the drain of M6})$$

$$p_8 \approx \frac{-g_{m8}r_{ds8}g_{m10}}{C_8} \quad (\text{the pole at the source of M8})$$

$$p_9 \approx \frac{-g_{m9}}{C_9} \quad (\text{the pole at the source of M9})$$



060628-04

Example 270-2 - Continued

Let us evaluate each of these poles.

1.) For p_A , the resistance R_A is approximately equal to g_{m6} and C_A is given as

$$C_A = C_{gs6} + C_{bd1} + C_{gd1} + C_{bd4} + C_{bs6} + C_{gd4}$$

From Ex. 240-4, $g_{m6} = 774.6\mu\text{S}$ and capacitors giving C_A are found as,

$$C_{gs6} = (220 \times 10^{-12} \cdot 80 \times 10^{-6}) + (0.67)(80\mu\text{m} \cdot 0.5\mu\text{m} \cdot 6\text{fF}/\mu\text{m}^2) = 177.6\text{fF}$$

$$C_{bd1} = (770 \times 10^{-6})(16.5 \times 10^{-6} \cdot 2 \times 10^{-6}) + (380 \times 10^{-12})(37 \times 10^{-6}) = 39.5\text{fF}$$

$$C_{gd1} = (220 \times 10^{-12} \cdot 16.5 \times 10^{-6}) = 3.6\text{fF}$$

$$C_{bd4} = C_{bs6} = (560 \times 10^{-6})(80 \times 10^{-6} \cdot 2 \times 10^{-6}) + (350 \times 10^{-12})(2 \cdot 82 \times 10^{-6}) = 147\text{fF}$$

and

$$C_{gd4} = (220 \times 10^{-12})(80 \times 10^{-6}) = 17.6\text{fF}$$

Therefore,

$$C_A = 177.6\text{fF} + 39.5\text{fF} + 3.6\text{fF} + 147\text{fF} + 17.6\text{fF} + 147\text{fF} = 0.532\text{pF}$$

Thus,

$$p_A = \frac{-774.6 \times 10^{-6}}{0.532 \times 10^{-12}} = -1.456 \times 10^9 \text{ rads/sec.}$$

2.) For the pole, p_B , the capacitance connected to this node is

$$C_B = C_{gd2} + C_{bd2} + C_{gs7} + C_{gd5} + C_{bd5} + C_{bs7}$$

Example 270-2 - Continued

The various capacitors above are found as

$$C_{gd2} = (220 \times 10^{-12} \cdot 16.5 \times 10^{-6}) = 3.6 \text{fF}$$

$$C_{bd2} = (770 \times 10^{-6}) \cdot (16.5 \times 10^{-6} \cdot 2 \times 10^{-6}) + (380 \times 10^{-12}) \cdot (37 \times 10^{-6}) = 39.5 \text{fF}$$

$$C_{gs7} = (220 \times 10^{-12} \cdot 80 \times 10^{-6}) + (0.67) \cdot (80 \mu\text{m} \cdot 0.5 \mu\text{m} \cdot 6 \text{fF}/\mu\text{m}^2) = 177.6 \text{fF}$$

$$C_{gd5} = (220 \times 10^{-12}) \cdot (80 \times 10^{-6}) = 17.6 \text{fF}$$

and

$$C_{bd5} = C_{bs7} = (560 \times 10^{-6}) \cdot (80 \times 10^{-6} \cdot 2 \times 10^{-6}) + (350 \times 10^{-12}) \cdot (2.82 \times 10^{-6}) = 147 \text{fF}$$

The value of C_B is the same as C_A and g_{m6} is assumed to be the same as g_{m7} giving $p_B = p_A = -1.456 \times 10^9$ rads/sec.

3.) For the pole, p_6 , the capacitance connected to this node is

$$C_6 = C_{bd6} + C_{gd6} + C_{gs10} + C_{gs11} + C_{bd8} + C_{gd8}$$

The various capacitors above are found as

$$C_{bd6} = (560 \times 10^{-6}) \cdot (80 \times 10^{-6} \cdot 2 \times 10^{-6}) + (350 \times 10^{-12}) \cdot (2.82 \times 10^{-6}) = 147 \text{fF}$$

$$C_{gs10} = C_{gs11} = (220 \times 10^{-12} \cdot 10 \times 10^{-6}) + (0.67) \cdot (10 \mu\text{m} \cdot 0.5 \mu\text{m} \cdot 6 \text{fF}/\mu\text{m}^2) = 22.2 \text{fF}$$

$$C_{bd8} = (770 \times 10^{-6}) \cdot (10 \times 10^{-6} \cdot 2 \times 10^{-6}) + (380 \times 10^{-12}) \cdot (2.12 \times 10^{-6}) = 24.5 \text{fF}$$

$$C_{gd8} = (220 \times 10^{-12}) \cdot (10 \times 10^{-6}) = 2.2 \text{fF} \quad \text{and} \quad C_{gd6} = C_{gd5} = 17.6 \text{fF}$$

Therefore,

$$C_6 = 147 \text{fF} + 17.6 \text{fF} + 22.2 \text{fF} + 22.2 \text{fF} + 2.2 \text{fF} + 17.6 \text{fF} = 0.229 \text{pF}$$

Example 270-2 - Continued

From Ex. 240-4, $g_{m6} = 774.6 \times 10^{-6}$. Therefore, p_6 , can be expressed as

$$-p_6 = \frac{774.6 \times 10^{-6}}{0.229 \times 10^{-12}} = 3.38 \times 10^9 \text{ rads/sec.}$$

4.) Next, we consider the pole, p_8 . The capacitance connected to this node is

$$C_8 = C_{bd10} + C_{gd10} + C_{gs8} + C_{bs8}$$

These capacitors are given as,

$$C_{bs8} = C_{bd10} = (770 \times 10^{-6}) \cdot (10 \times 10^{-6} \cdot 2 \times 10^{-6}) + (380 \times 10^{-12}) \cdot (2.12 \times 10^{-6}) = 24.5 \text{fF}$$

$$C_{gs8} = (220 \times 10^{-12} \cdot 10 \times 10^{-6}) + (0.67) \cdot (10 \mu\text{m} \cdot 0.5 \mu\text{m} \cdot 6 \text{fF}/\mu\text{m}^2) = 22.2 \text{fF}$$

and

$$C_{gd10} = (220 \times 10^{-12}) \cdot (10 \times 10^{-6}) = 2.2 \text{fF}$$

The capacitance C_8 is equal to

$$C_8 = 24.5 \text{fF} + 2.2 \text{fF} + 22.2 \text{fF} + 24.5 \text{fF} = 73.4 \text{fF}$$

Using the values of Ex. 240-4 of $600 \mu\text{S}$, the pole p_8 is found as,

$$-p_8 = g_{m8} r_{ds8} g_{m10} / C_8 = -600 \mu\text{S} \cdot 600 \mu\text{S} / 4.5 \mu\text{S} \cdot 73.4 \text{fF} = -1090 \times 10^9 \text{ rads/sec.}$$

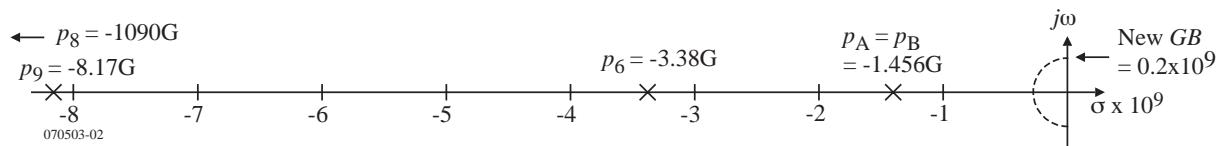
5.) The capacitance for the pole at p_9 is identical with C_8 . Therefore, since g_{m9} is $600 \mu\text{S}$, the pole p_9 is $-p_9 = 8.17 \times 10^9$ rads/sec.

Example 270-2 - Continued

The poles are summarized below:

$$p_A = -1.456 \times 10^9 \text{ rads/sec} \quad p_B = -1.456 \times 10^9 \text{ rads/sec} \quad p_6 = -3.38 \times 10^9 \text{ rads/sec}$$

$$p_8 = -1090 \times 10^9 \text{ rads/sec} \quad p_9 = -8.17 \times 10^9 \text{ rads/sec}$$



The smallest of these poles is p_A or p_B . Since p_6 is not much larger than p_A or p_B , we will find the new GB by dividing p_A or p_B by 4 (which is guess rather than 2.2) to get 364×10^6 rads/sec. Thus the new GB will be $364/2\pi$ or 58MHz.

Checking our guess gives a phase margin of,

$$\text{PM} = 90^\circ - 2\tan^{-1}(0.364/1.456) - \tan^{-1}(0.364/3.38) = 56^\circ \text{ which is okay}$$

The magnitude of the dominant pole is given as

$$p_{\text{dominant}} = GB/A_{vd}(0) = 364 \times 10^6 / 3,678 = 99,000 \text{ rads/sec.}$$

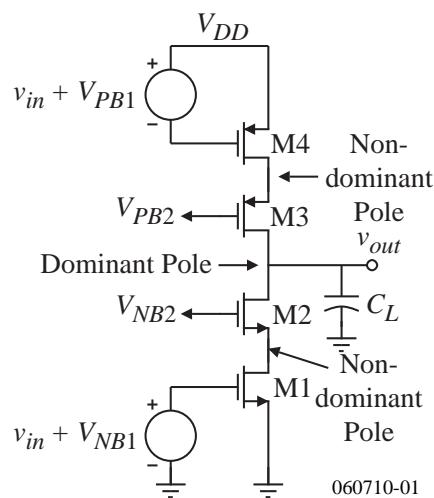
The value of load capacitor that will give this pole is

$$C_L = (p_{\text{dominant}} \cdot R_{out})^{-1} = (99 \times 10^3 \cdot 7.44 \text{ M}\Omega)^{-1} = 1.36 \text{ pF}$$

Therefore, the new $GB = 58\text{MHz}$ compared with the old $GB = 10\text{MHz}$.

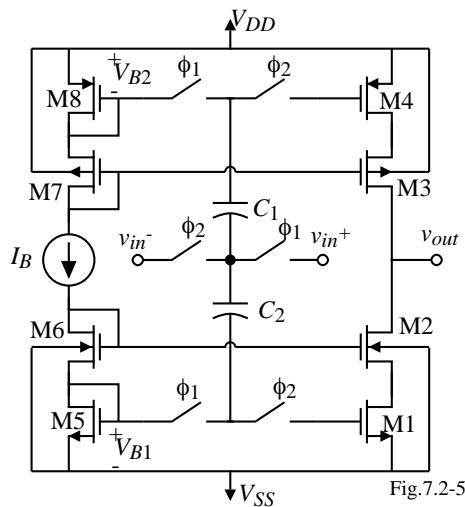
Elimination of Higher-Order Poles

The minimum circuitry for a cascode op amp is shown below:



If the source-drain area between M1 and M2 and M3 and M4 can be minimized, the non-dominant poles will be quite large.

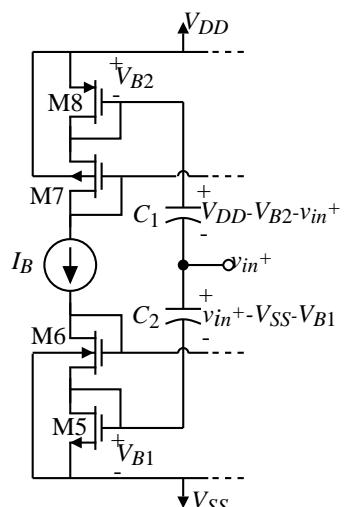
Dynamically Biased, Push-Pull, Cascode Op Amp



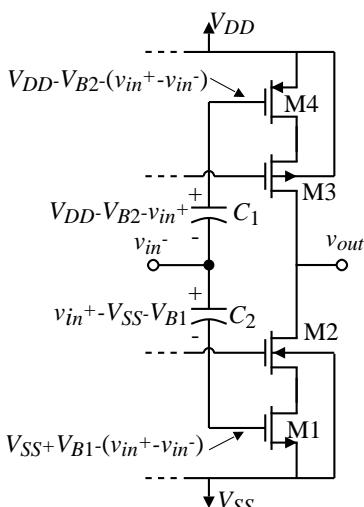
Push-pull, cascode amplifier: M1-M2 and M3-M4
Bias circuitry: M5-M6-C₂ and M7-M8-C₁

Dynamically Biased, Push-Pull, Cascode Op Amp - Continued

Operation:



Equivalent circuit during the ϕ_1 clock period

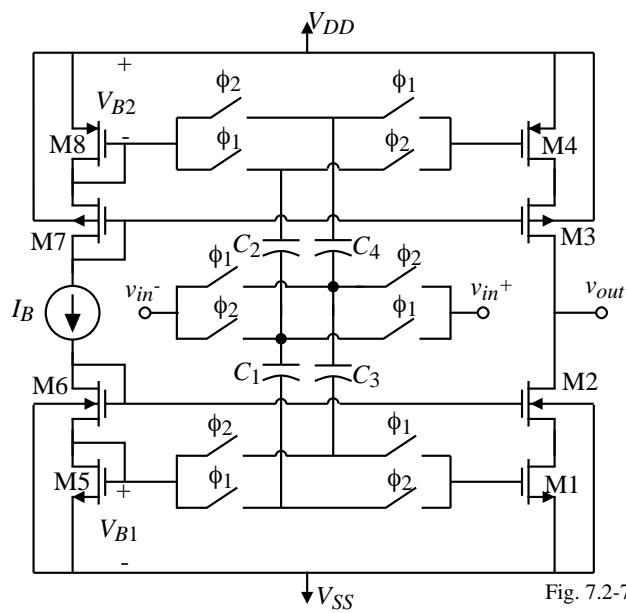


Equivalent circuit during the ϕ_2 clock period.

Fig. 7.2-6

Dynamically Biased, Push-Pull, Cascode Op Amp - Continued

This circuit will operate on both clock phases[†].



Performance (1.5μm CMOS):

- 1.6mW dissipation
- $GB \approx 130\text{MHz}$ ($C_L=2.2\text{pF}$)
- Settling time of 10ns ($C_L=10\text{pF}$)

This amplifier was used with a 28.6MHz clock to realize a 5th-order switched capacitor filter having a cutoff frequency of 3.5MHz.

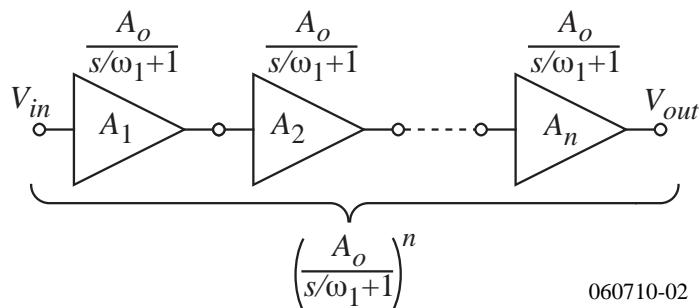
[†] S. Masuda, et. al., "CMOS Sampled Differential Push-Pull Cascode Op Amp," Proc. of 1984 International Symposium on Circuits and Systems, Montreal, Canada, May 1984, pp. 1211-12-14.

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CASCADED AMPLIFIERS USING VOLTAGE AMPLIFIERS

Bandwidth of Cascaded Amplifiers

Cascading of low-gain, wide-bandwidth amplifiers:



Overall gain is A_o^n

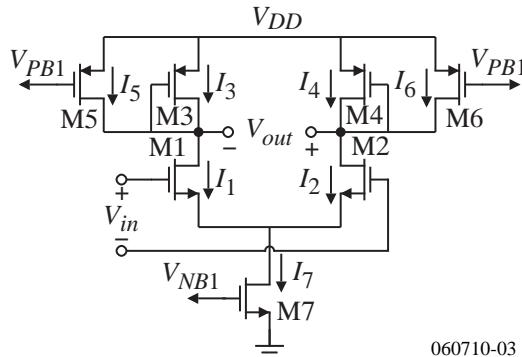
-3dB frequency is,

$$\omega_{-3\text{dB}} = \omega_1 \sqrt{2^{1/n}-1}$$

If $A_o = 10$, $\omega_1 = 300\pi \times 10^6$ rads/sec. and $n = 3$, then

$$\text{Overall gain is } 60\text{dB} \quad \text{and} \quad \omega_{-3\text{dB}} = 0.51\omega_1 = 480 \times 10^6 \text{ rads/sec.} \rightarrow 76.5 \text{ MHz}$$

Voltage Amplifier Suitable for Cascading



060710-03

Voltage Gain:

$$\frac{V_{out}}{V_{in}} = \frac{g_m 1}{g_m 3} = \sqrt{\frac{K_n' (W_1/L_1)(I_3+I_5)}{K_p' (W_3/L_3)I_3}}$$

$$\omega_{-3dB} \approx \frac{g_m 3}{C_{gs1}}$$

Ex. 270-3 - Design of a Voltage Amplifier for Cascading

Design the previous voltage amplifier for a gain of $A_o = 10$ and a power dissipation of no more than 1mW. The design should permit A_o to be well defined. What is the ω_{-3dB} for this amplifier and what would be the ω_{-3dB} for a cascade of three identical amplifiers?

Solution

To enhance the accuracy of the gain, we replace M3 and M4 with NMOS transistors to avoid the variation of the transconductance parameter. This assumes a *p*-well technology to avoid bulk effects.

The gain of 10 requires,

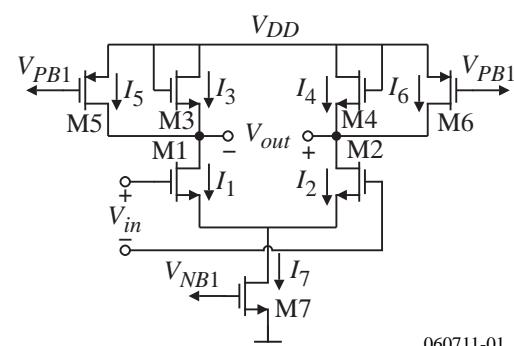
$$\frac{W_1}{L_1}(I_3+I_5) = 100 \frac{W_3}{L_3} I_3$$

If $V_{DD} = 2.5V$, then $2(I_3+I_5) \cdot 2.5V = 1000\mu W$.

Therefore, $I_3+I_5 = 200\mu A$. Let $I_3 = 20\mu A$ and $W_1/L_1 = 10W_3/L_3$.

Choose $W_1/L_1 = 5\mu m/0.5\mu m$ which gives $W_3/L_3 = 0.5\mu m/0.5\mu m$. M5 and M6 are designed to give $I_5 = 180\mu A$ and M7 is designed to give $I_7 = 400\mu A$.

The dominant pole is $g_m 3 / C_{out}$.



060711-01

Ex. 270-3 – Continued

$$C_{out} = C_{gs3} + C_{bs3} + C_{bd1} + C_{bd5} + C_{gd1} + C_{gd5} + C_{gs1}(\text{next stage}) \approx C_{gs3} + C_{gs1}$$

Using $C_{ox} = 60.6 \times 10^{-4} \text{ F/m}^2$, we get,

$$C_{out} \approx (2.5 + 0.25) \times 10^{-12} \text{ m}^2 \times 60.6 \times 10^{-4} \text{ F/m}^2 = 16.7 \text{ fF} \rightarrow C_{out} \approx 20 \text{ fF}$$

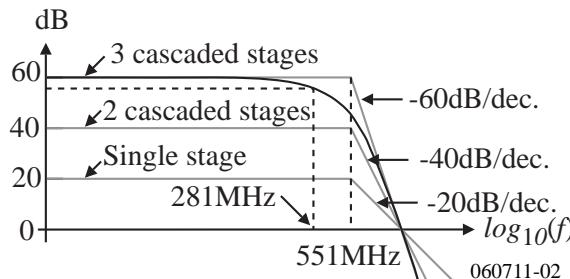
$$g_{m3} = \sqrt{2 \cdot 120 \cdot 1 \cdot 20} \mu\text{S} = 69.3 \mu\text{S}$$

\therefore Dominant pole $\approx 69.3 \mu\text{S}/20 \text{ fF} = 34.65 \times 10^8 \text{ rads/sec.} \rightarrow f_{-3\text{dB}} = 551 \text{ MHz}$

The bandwidth of three identical cascaded amplifiers giving a low-frequency gain of 60dB would have a $f_{-3\text{dB}}$ of

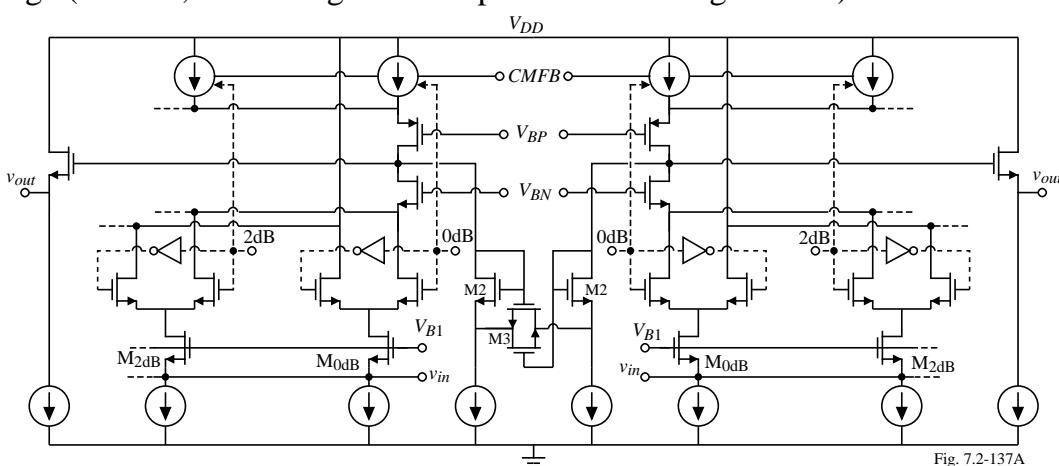
$$f_{-3\text{dB}(\text{Overall})} = f_{-3\text{dB}} \sqrt{2^{1/3} - 1} = 551 \text{ MHz} (0.5098) = 281 \text{ MHz}.$$

$$P_{diss} = 3 \text{ mW}$$

**A 71 MHz CMOS Programmable Gain Amplifier[†]**

Uses 3 ac-coupled stages.

First stage (0-20dB, common gate for impedance matching and NF):



$R_{in} = 330 \Omega$ to match source driving requirement

All current sinks are identical for the differential switches.

Dominant pole at 150MHz.

[†] P. Orsatti, F. Piazza, and Q. Huang, "A 71 MHz CMOS IF-Basband Strip for GSM, IEEE JSSC, vol. 35, No. 1, Jan. 2000, pp. 104-108.
CMOS Analog Circuit Design

A 71 MHz PGA – Continued

Second stage (-10dB to 20dB):

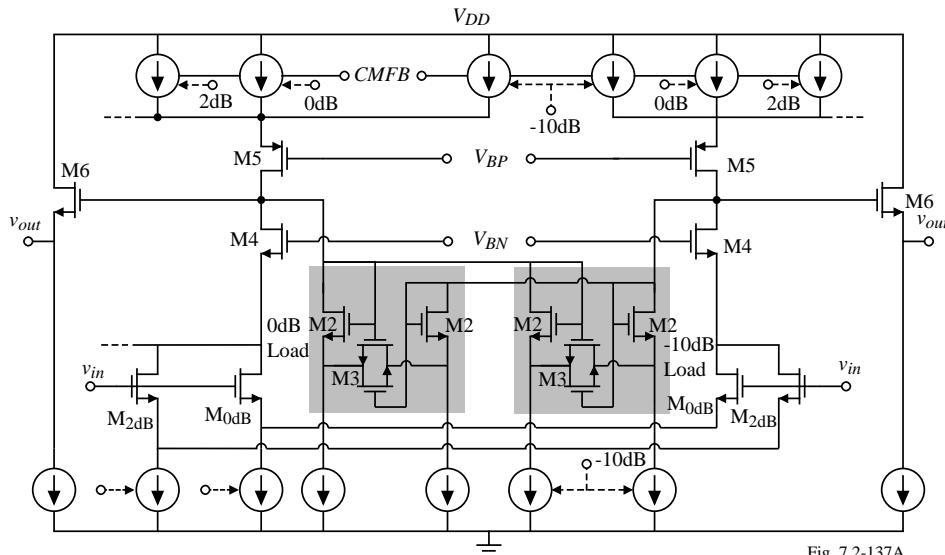


Fig. 7.2-137A

Dominant pole is also at 150MHz

For $V_{DD} = 2.5V$, at 60dB gain, the total current is 2.6mA

$IIP_3 \approx +1\text{dBm}$

CASCADED AMPLIFIERS USING CURRENT FEEDBACK AMPLIFIERS

Advantages of Using Current Feedback

Why current feedback?

- Higher GB
- Less voltage swing \Rightarrow more dynamic range

What is a current amplifier?

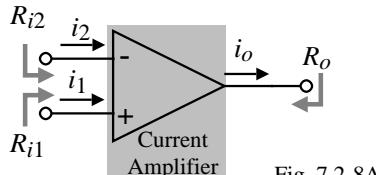


Fig. 7.2-8A

Requirements:

$$i_o = A_i(i_1 - i_2)$$

$$R_i1 = R_i2 = 0\Omega$$

$$R_o = \infty$$

Ideal source and load requirements:

$$R_{source} = \infty$$

$$R_{Load} = 0\Omega$$

Bandwidth Advantage of a Current Feedback Amplifier

Consider the inverting voltage amplifier shown using a current amplifier with negative current feedback:

The output current, i_o , of the current amplifier can be written as

$$i_o = A_i(s)(i_1 - i_2) = -A_i(s)(i_{in} + i_o)$$

The closed-loop current gain, i_o/i_{in} , can be found as

$$\frac{i_o}{i_{in}} = \frac{-A_i(s)}{1+A_i(s)}$$

However, $v_{out} = i_o R_2$ and $v_{in} = i_{in} R_1$. Solving for the voltage gain, v_{out}/v_{in} gives

$$\frac{v_{out}}{v_{in}} = \frac{i_o R_2}{i_{in} R_1} = \left(\frac{-R_2}{R_1} \right) \left(\frac{A_i(s)}{1+A_i(s)} \right)$$

If $A_i(s) = \frac{A_o}{(s/\omega_A) + 1}$, then

$$\frac{v_{out}}{v_{in}} = \left(\frac{-R_2}{R_1} \right) \left(\frac{A_o}{1+A_o} \right) \left(\frac{\omega_A(1+A_o)}{s + \omega_A(1+A_o)} \right) \Rightarrow A_v(0) = \frac{-R_2 A_o}{R_1(1+A_o)} \text{ and } \boxed{\omega_{-3dB} = \omega_A(1+A_o)}$$

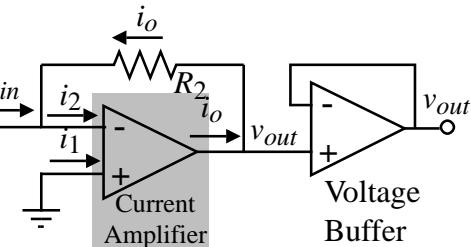


Fig. 7.2-9

Bandwidth Advantage of a Current Feedback Amplifier - Continued

The unity-gainbandwidth is,

$$GB = |A_v(0)| \omega_{-3dB} = \frac{R_2 A_o}{R_1(1+A_o)} \cdot \omega_A(1+A_o) = \frac{R_2}{R_1} A_o \cdot \omega_A = \frac{R_2}{R_1} GB_i$$

where GB_i is the unity-gainbandwidth of the current amplifier.

Note that if GB_i is constant, then increasing R_2/R_1 (the voltage gain) increases GB .

Illustration:

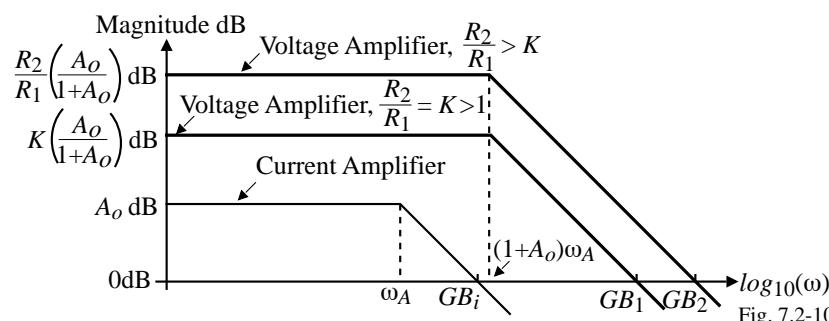


Fig. 7.2-10

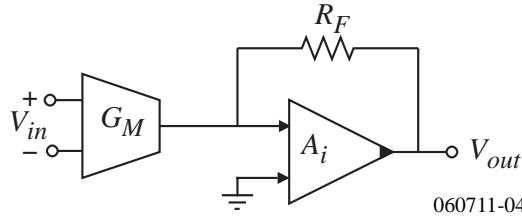
Note that $GB_2 > GB_1 > GB_i$

The above illustration assumes that the GB of the voltage amplifier realizing the voltage buffer is greater than the GB achieved from the above method.

Current Feedback Amplifier

In a current mirror implementation of the current amplifier, it is difficult to make the input resistance sufficiently small compared to R_1 .

This problem can be solved using a transconductance input stage shown in the following block diagram:

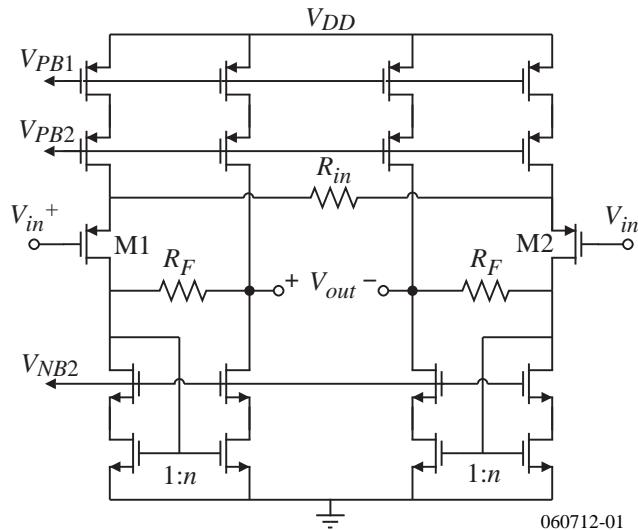


$$\frac{V_{out}}{V_{in}} = \frac{-G_M R_F A_i}{1 + A_i}$$

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Differential Implementation of the Current Feedback Amplifier



$$I_{in} = \frac{g_{m1}}{1 + 0.5g_{m1}R_{in}} \left(\frac{{V_{in}}^+ - {V_{in}}^-}{2} \right) \quad \text{and} \quad V_{out} = \frac{n(2R_F)}{1+n} I_{in}$$

$$\frac{V_{out}}{V_{in}} \approx \frac{2nR_F}{R_{in}}$$

A 20dB Voltage Amplifier using a Current Amplifier

The following circuit is a programmable voltage amplifier with up to 20dB gain:

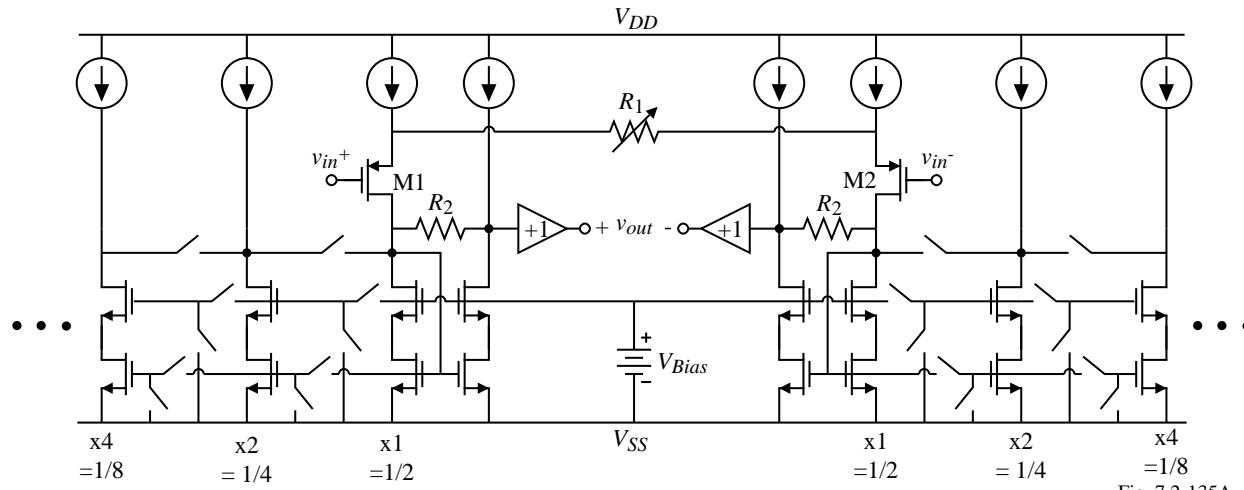
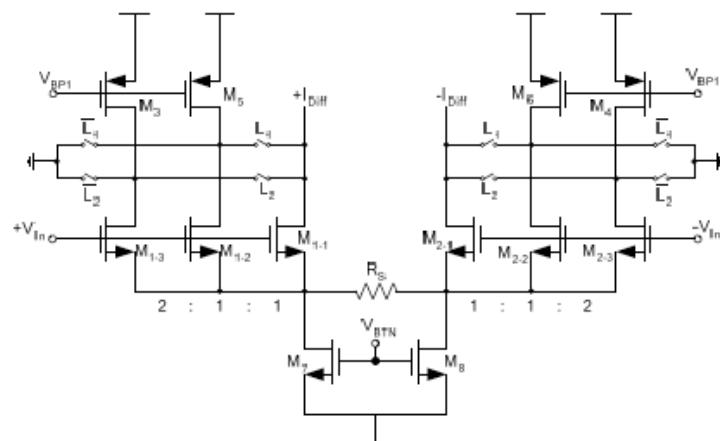


Fig. 7.2-135A

R_1 and the current mirrors are used for gain variation while R_2 is fixed.

Programmability of the Previous Stage

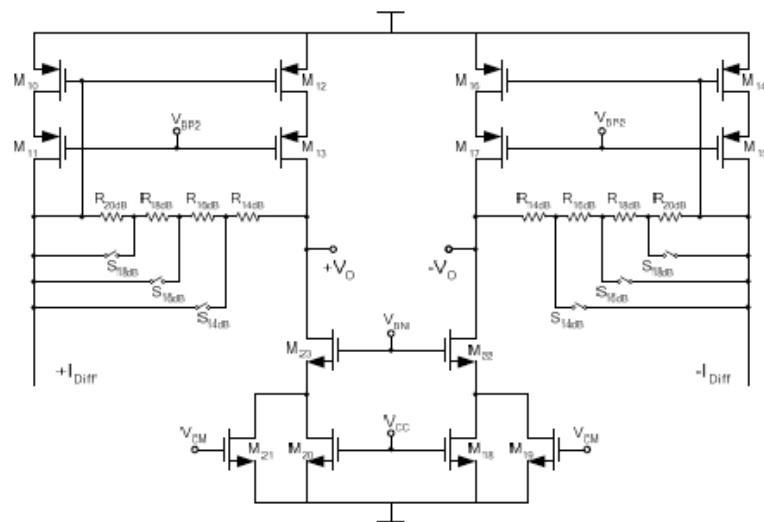
Input OTA:



Changes G_M in 6dB steps.

Programmability of the Voltage Stage – Cont'd

Current Amplifier:



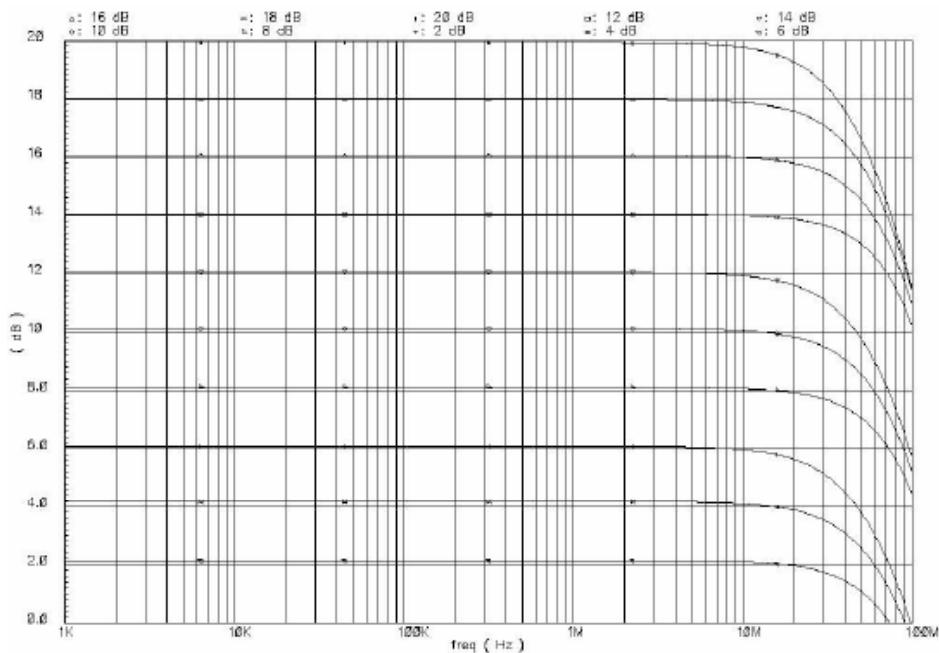
Changes R_F in 2dB steps

($R_{F20dB} = 2.1k\Omega$, $R_{F18dB} = 1.6k\Omega$, $R_{F16dB} = 1.3k\Omega$, and $R_{F14dB} = 5k\Omega$.)

$R_{FTotal} = 10k\Omega$.

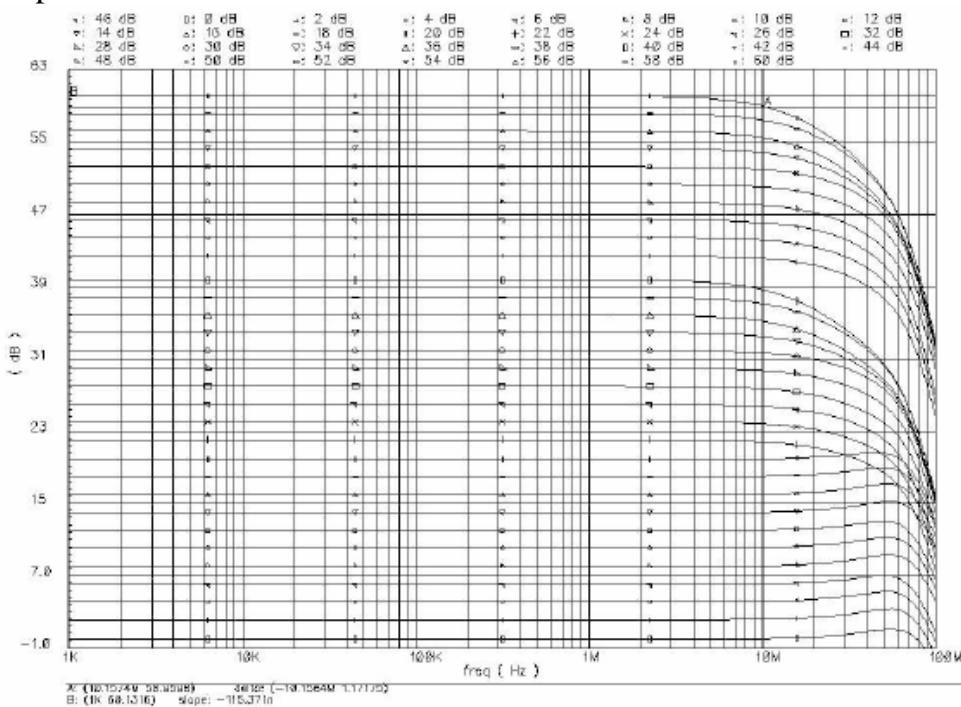
Frequency Response of the Current Feedback PGA Stage

0.5pF load:



Frequency Response of the Entire 60dB PGA

Includes output buffer:



SUMMARY

- Increasing the GB of an op amp requires that the magnitude of all non-dominant poles are much greater than GB from the origin of the complex frequency plane
- The practical limit of GB for an op amp is approximately 5-10 times less than the magnitude of the smallest non-dominant pole ($\approx 100\text{MHz}$)
- To achieve high values of GB it is necessary to eliminate the non-dominant poles (which come from parasitics) or increase the magnitude of the non-dominant poles
- The best way to achieve high-bandwidth amplifiers is to cascade high-bandwidth voltage amplifiers
- If the gain of the high-bandwidth voltage amplifiers is well defined, then it is not necessary to use negative feedback around the amplifier
- Amplifiers with well defined gains are obtainable with a -3dB bandwidth of 100MHz

LECTURE 280 – DIFFERENTIAL-IN, DIFFERENTIAL-OUT OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Examples of differential output op amps
- Common mode output voltage stabilization
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 384-393

INTRODUCTION

Why Differential Output Op Amps?

- Cancellation of common mode signals including clock feedthrough
- Increased signal swing

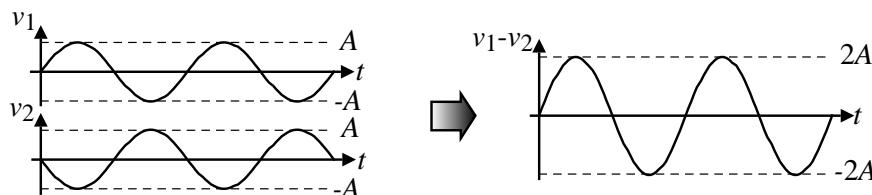


Fig. 7.3-1

- Cancellation of even-order harmonics

Symbol:

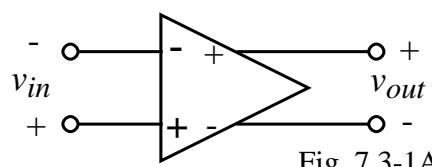
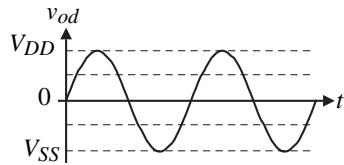


Fig. 7.3-1A

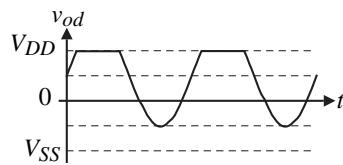
Common Mode Output Voltage Stabilization

If the common mode gain not small, it may cause the common mode output voltage to be poorly defined.

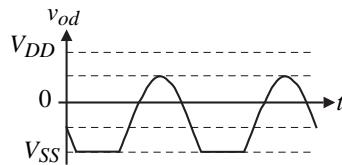
Illustration:



CM output voltage properly defined,
 $V_{cm} = 0$



CM output voltage too large,
 $V_{cm} = 0.5V_{DD}$



CM output voltage too small,
 $V_{cm} = 0.5V_{SS}$

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Remember that:

$$v_{OUT} = A_{vd}(v_{ID}) \pm A_{cm}(v_{CM})$$

EXAMPLES OF DIFFERENTIAL OUTPUT OP AMPS (OTA'S) Two-Stage, Miller, Differential-In, Differential-Out Op Amp

Note that the upper ICMR is

$$V_{DD} - V_{SGP} + V_{TN}$$

$$(OCMR) = V_{DD} + |V_{SS}| - V_{SDP(\text{sat})} - V_{DSN(\text{sat})}$$

The maximum peak-to-peak output voltage
 $\leq 2 \cdot OCMR$

Conversion between differential outputs and single-ended outputs:

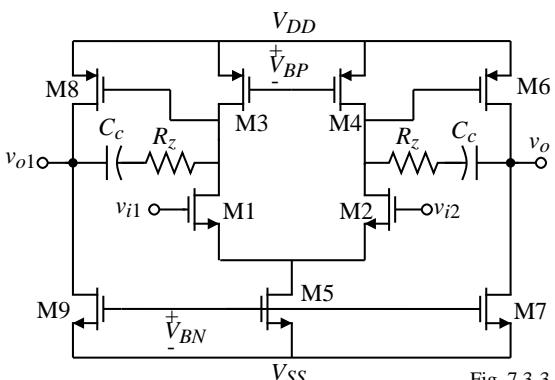
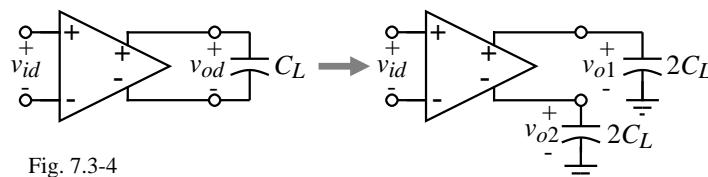
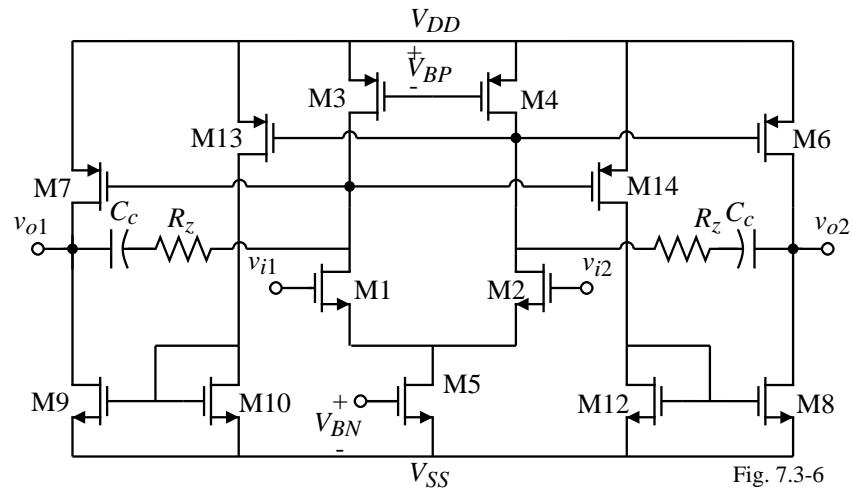


Fig. 7.3-3

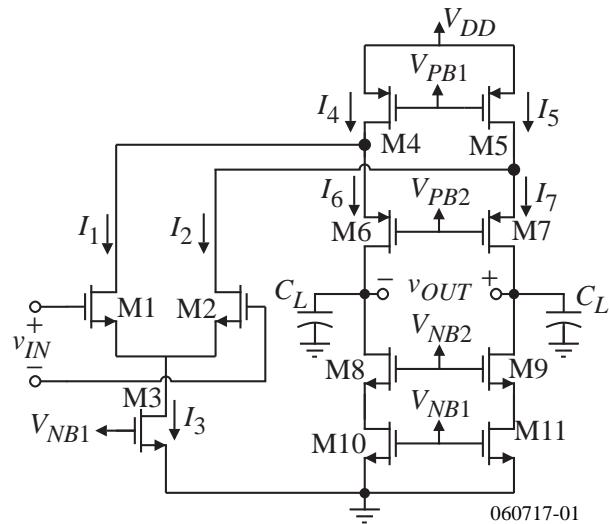
Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Push-Pull Output



Comments:

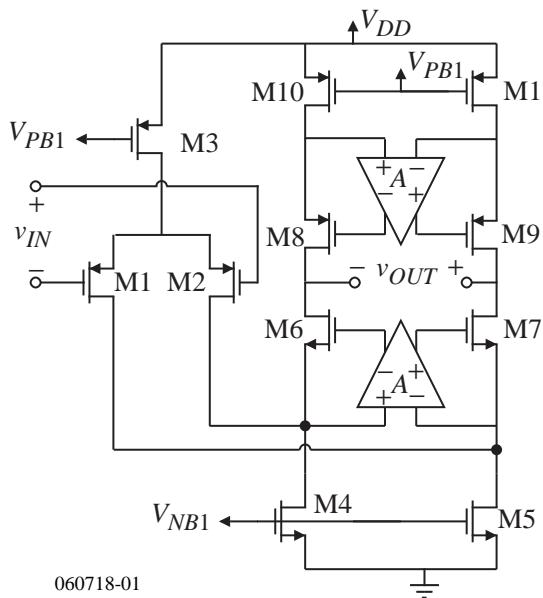
- Able to actively source and sink output current
- Output quiescent current poorly defined

Folded-Cascode, Differential Output Op Amp

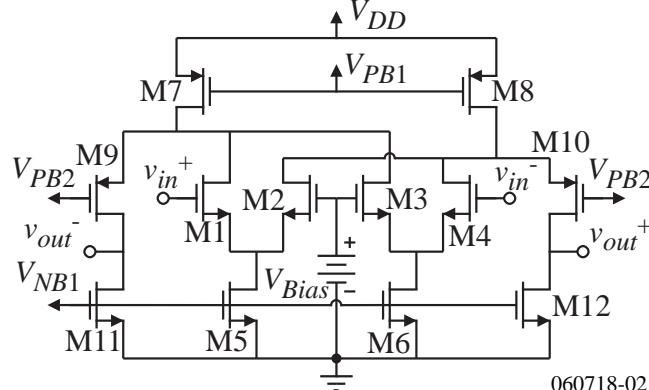


- No longer has the low-frequency asymmetry in signal path gains.
- Class A

Enhanced-Gain, Folded-Cascode, Differential Output Op Amp



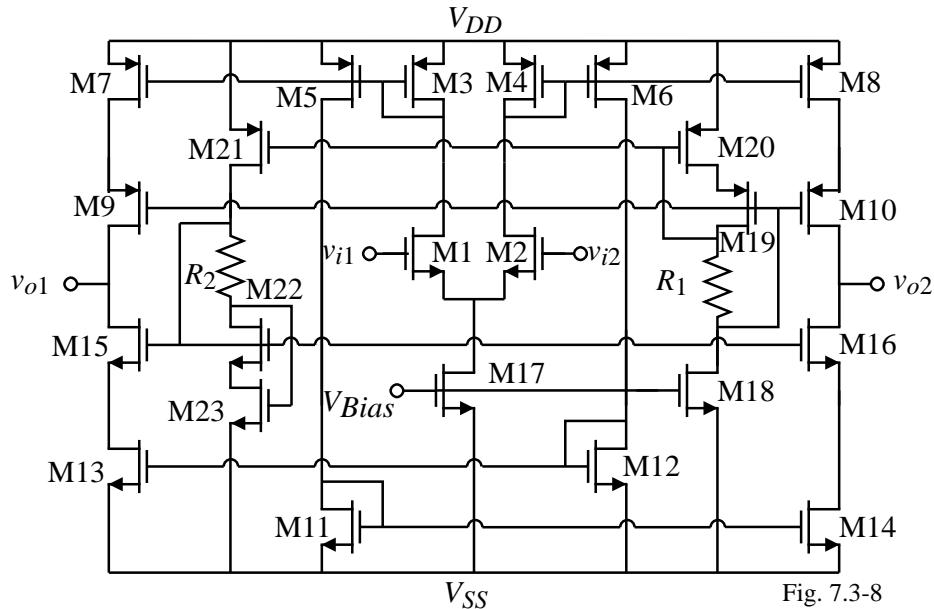
What about the A amplifier?
Below is the upper A amplifier:



Note that V_{Bias} controls the dc voltage at the input of the A amplifier through the negative feedback loop.

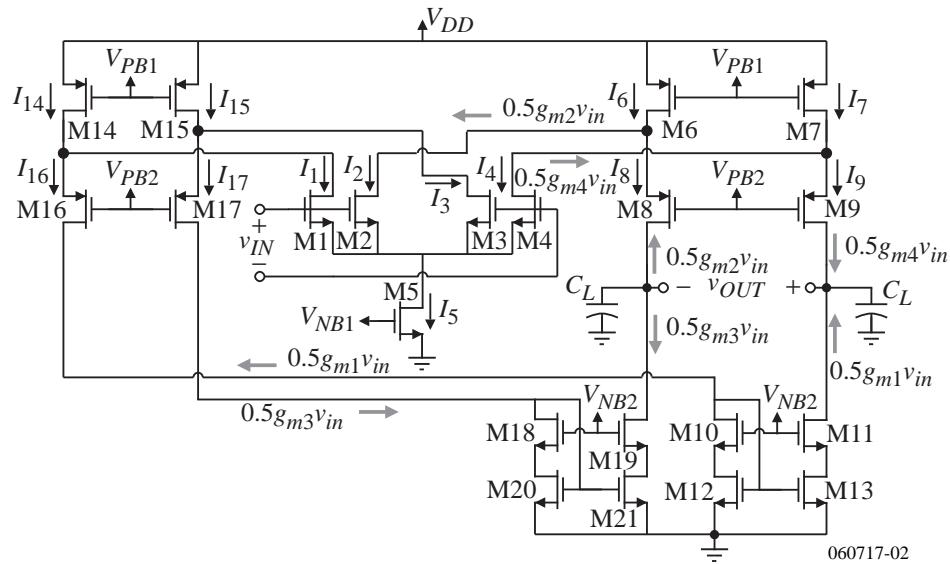
- Balanced inputs
- Class A

Push-Pull Cascode Op Amp with Differential-Outputs



- Output quiescent currents are well defined
- Self-biased circuits can be replaced with V_{NB2} and V_{PB2}

Folded-Cascode, Push-Pull, Differential Output Op Amp

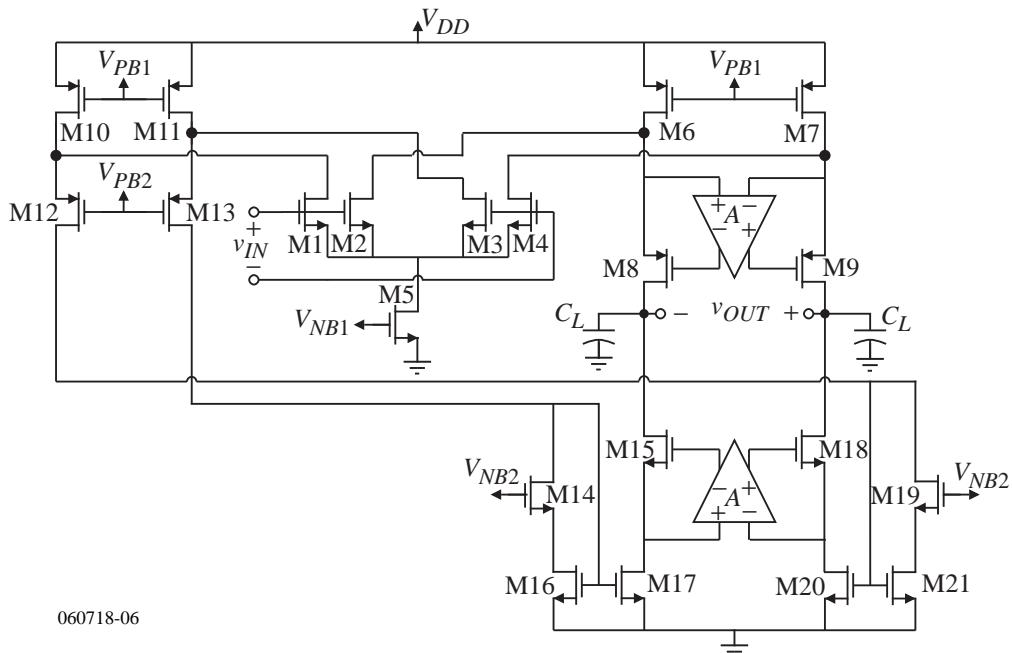


$$I_6 = I_7 = I_{14} = I_{15} > 0.5I_5$$

$$I_5 = I_1 + I_2 + I_3 + I_4$$

$$A_v = g_m R_{out}(\text{diff})$$

Enhanced-Gain, Folded-Cascode with Push-Pull Outputs



- Gain approaches $g_m^3 r_{ds}^3$

Cross-Coupled Differential Amplifier Stage

The cross-coupled input stage allows the push-pull output quiescent current to be well defined.

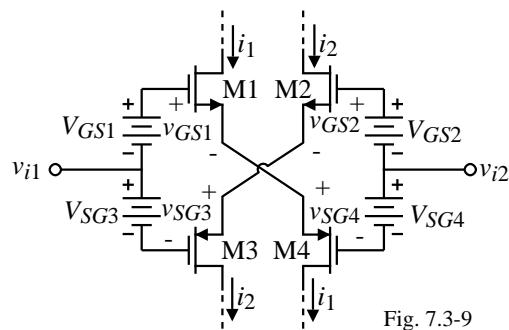


Fig. 7.3-9

Operation:

$$\text{Voltage loop } v_{i1} - v_{i2} = -V_{GS1} + v_{GS1} + v_{SG4} - V_{SG4} = V_{SG3} - v_{SG3} - v_{GS2} + V_{GS2}$$

Using the notation for ac, dc, and total variables gives,

$$v_{i2} - v_{i1} = v_{id} = (v_{sg1} + v_{gs4}) = -(v_{sg3} + v_{gs2})$$

If $gm_1 = gm_2 = gm_3 = gm_4$, then half of the differential input is applied across each transistor with the correct polarity.

$$\therefore i_1 = \frac{gm_1 v_{id}}{2} = \frac{gm_4 v_{id}}{2} \quad \text{and} \quad i_2 = -\frac{gm_2 v_{id}}{2} = -\frac{gm_3 v_{id}}{2}$$

Class AB, Differential Output Op Amp using a Cross-Coupled Differential Input Stage

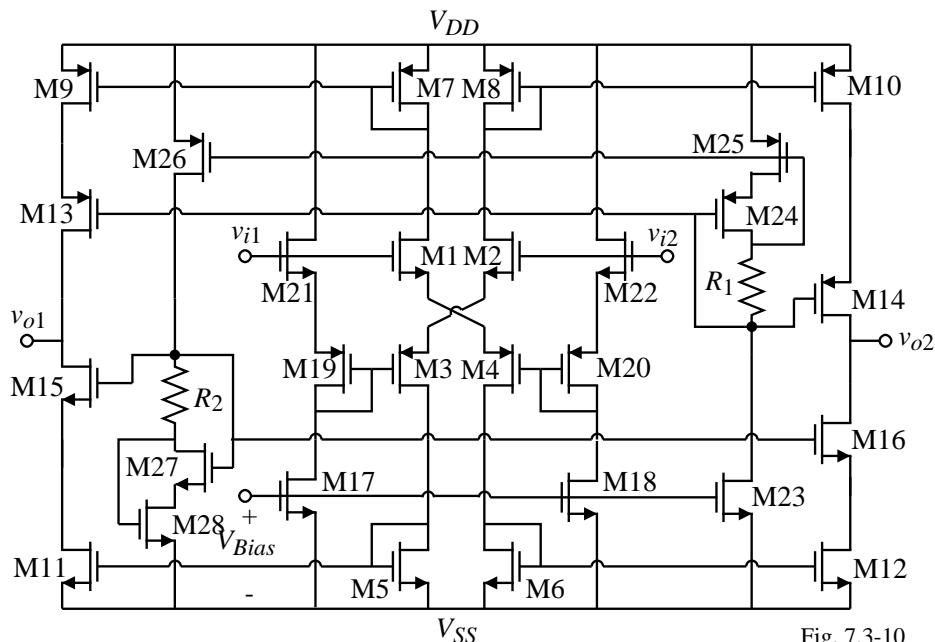


Fig. 7.3-10

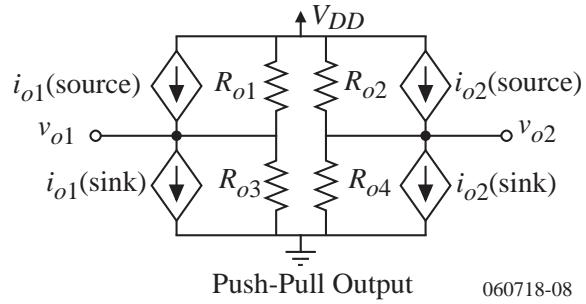
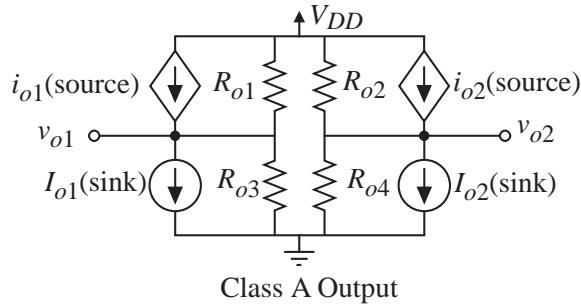
Quiescent output currents are defined by the current in the input cross-coupled differential amplifier.

COMMON MODE OUTPUT VOLTAGE STABILIZATION

Common Mode Feedback Circuits

Because the common mode gain is undefined, any common mode signal at the input can cause the output common mode voltage to be improperly defined. The common mode output voltage is stabilized by sensing the common mode output voltage and using negative feedback to adjust the common mode voltage to the desired value.

Model for the Output of Differential Output Op Amps:

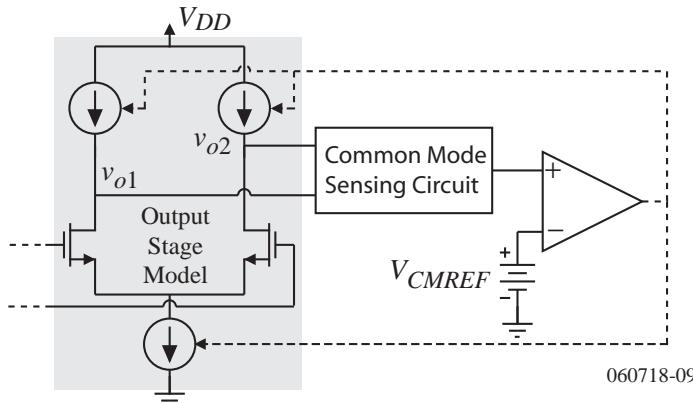


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R_{oi} represents the self-resistance of the output sink/sources.

- 1.) If the common mode output voltage increases the sourcing current is too large.
- 2.) If the common mode output voltage decreases the sinking current is too large.

Conceptual View of Common-Mode Feedback



Function of the common-mode feedback circuit:

- 1.) If the common-mode output voltage increases, decrease the upper currents sources or increase the lower current sink until the common-mode voltage is equal to V_{CMREF} .
- 2.) If the common-mode output voltage decreases, increase the upper currents sources or decrease the lower current sink until the common-mode voltage is equal to V_{CMREF} .

Two-Stage, Miller, Differential-In, Differential-Out Op Amp with Common-Mode Feedback

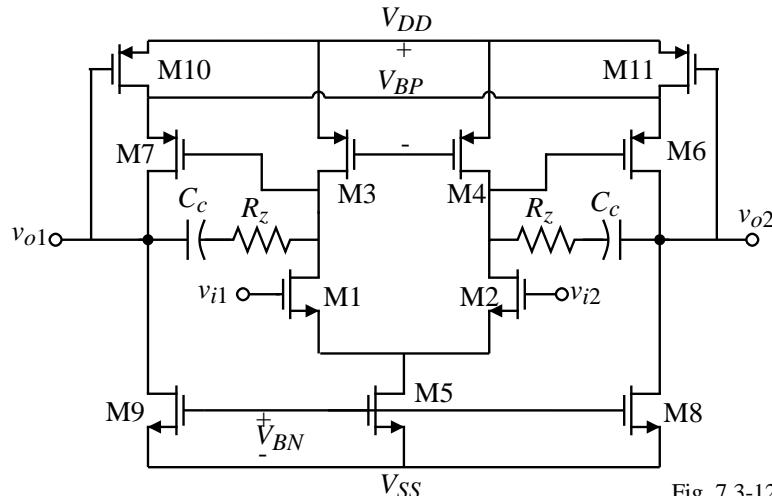


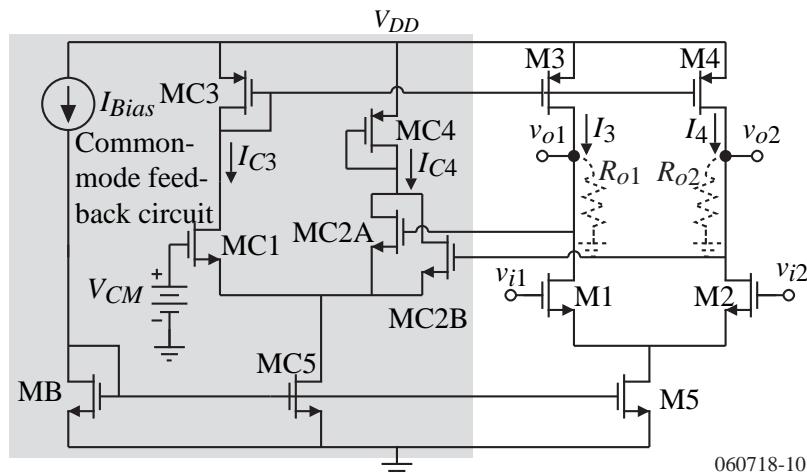
Fig. 7.3-12

Comments:

- Simple
- Unreferenced – value of common mode output voltage determined by the circuit characteristics

Common Mode Feedback Circuits

Implementation of common mode feedback circuit:



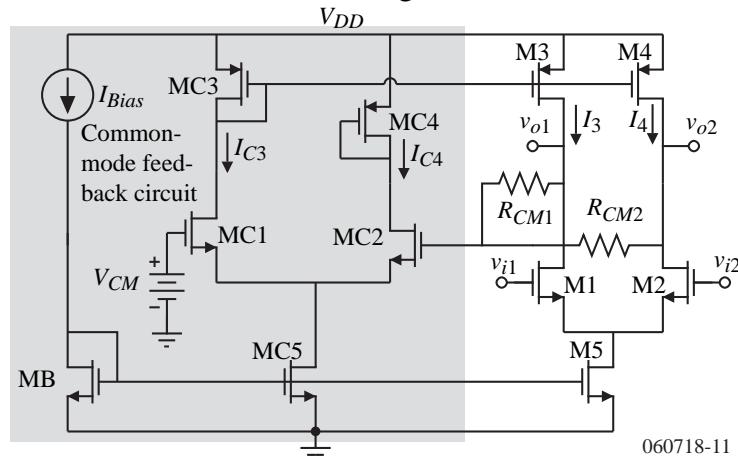
This scheme can be applied to any differential output amplifier.

CM Loop Gain = $-g_m C_1 R_{o1}$ which can be large if the output of the differential output amplifier is cascaded or a gain-enhanced cascode.

The common-mode loop gain may need to be compensated for proper dynamic performance.

Common Mode Feedback Circuits – Continued

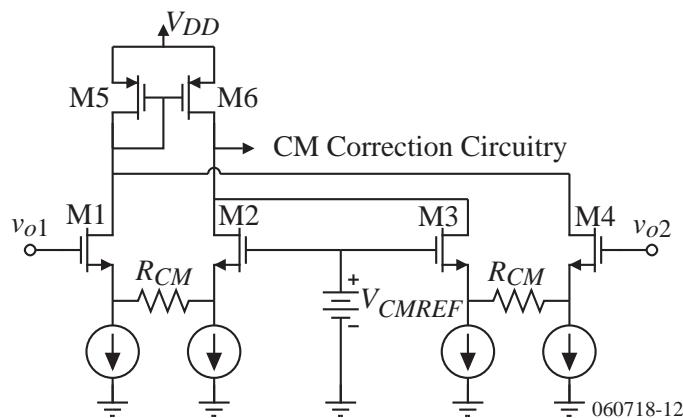
The previous circuit suffers when the input common mode voltage is low because the transistors MC2A and MC2B have a poor negative input common mode voltage. The following circuit alleviates this disadvantage:



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An Improved Common-Mode Feedback Circuit

The resistance loading of the previous circuit can be avoided in the following CM feedback implementation:

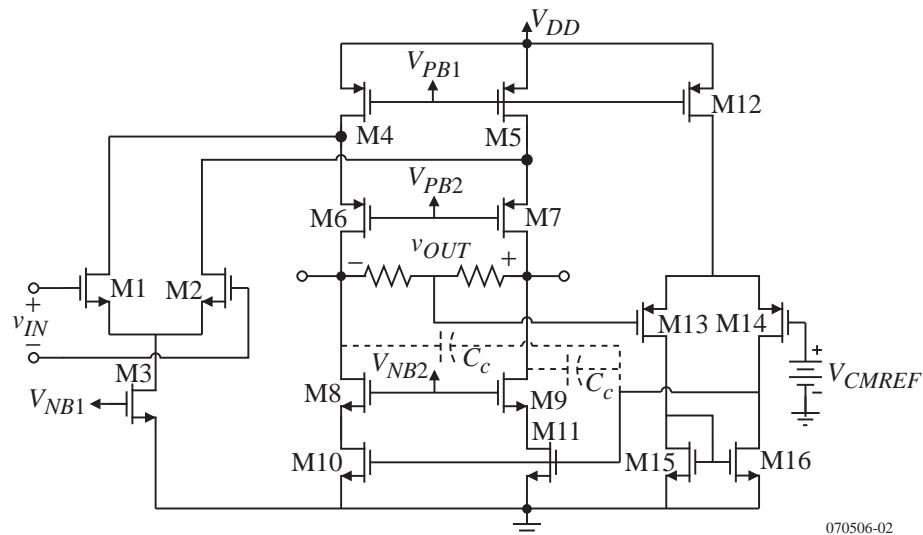


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This circuit is capable of sustaining a large differential voltage without loading the output of the differential output op amp.

Frequency Response of the CM Feedback Circuit

Consider the following CM feedback circuit implementation:

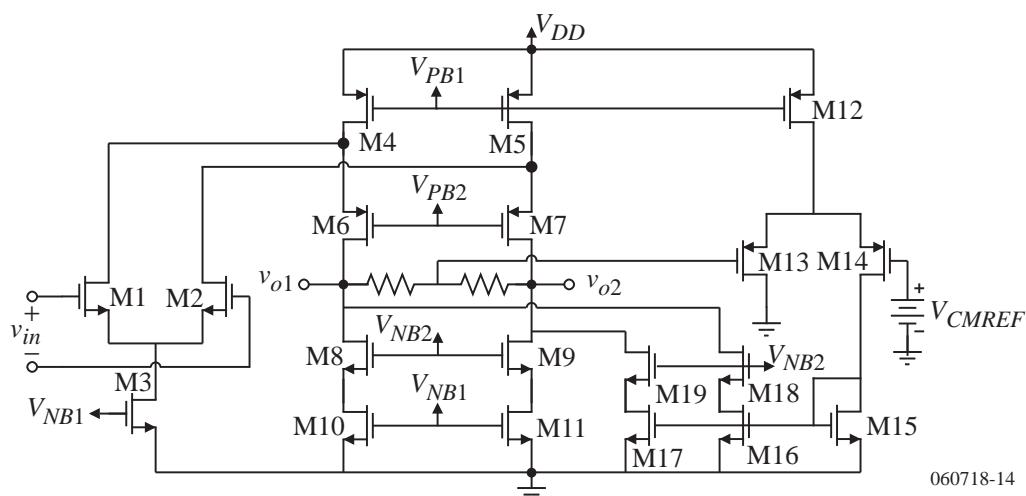


The CM feedback path has two poles – one at the gates of M10 and M11 and the dominant output pole of the differential output op amp.

Can compensate with Miller capacitors as shown.

Improved CM Feedback Frequency Response

The circuit on the previous page can be modified to eliminate the pole at the gates of M10 and M11 as follows:



- The need for compensation of the common mode loop no longer exists since there is only one dominant pole
- The dominant pole of the differential amplifier becomes the dominant pole of the common mode feedback

A Common Mode Feedback Correction Scheme for Discrete Time Applications

Correction Scheme:

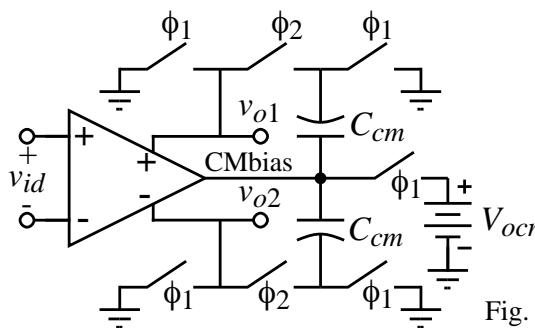


Fig. 7.3-14

Operation:

- 1.) During the ϕ_1 phase, both C_{cm} are charged to the desired value of V_{ocm} and $CMbias = V_{ocm}$.
- 2.) During the ϕ_2 phase, the C_{cm} capacitors are connected between the differential outputs and the CMbias node. The average value applied to the CMbias node will be V_{ocm} .

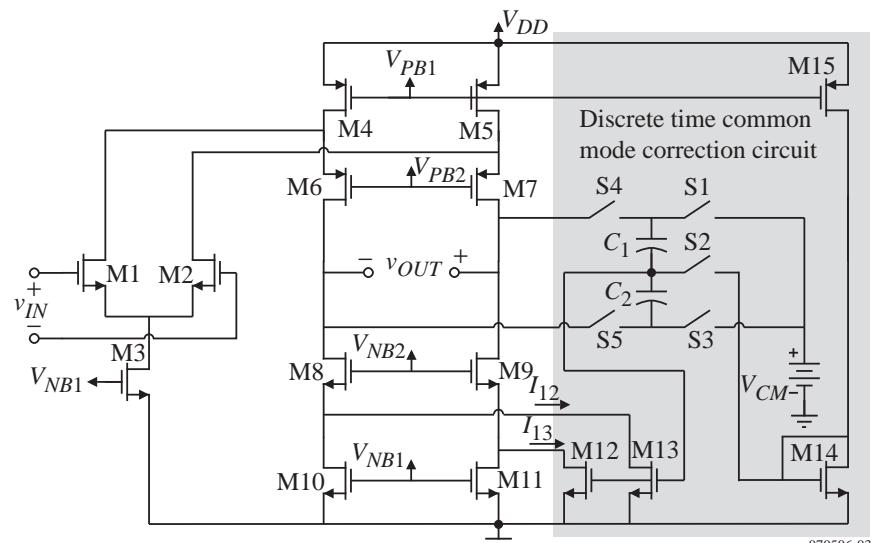
Example of a Common-Mode Output Voltage Stabilization Scheme for Discrete-Time Applications

Common mode adjustment phase:

Switches S1, S2 and S3 are closed. C_1 and C_2 are charged to the value necessary for I_{12} and I_{13} to keep the common mode output voltage at V_{CM} .

Amplification phase:

Switches S4 and S5 are closed. If the common mode output voltage is not at V_{CM} , the currents I_{12} and I_{13} will change



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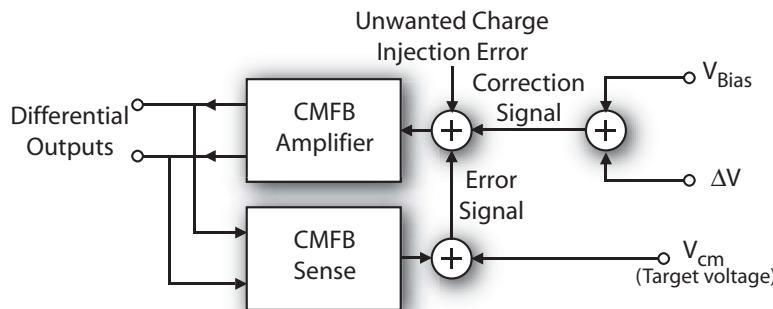
to force the value of the common mode output voltage back to V_{CM} .

Correction of Channel Charge and Clock Feedthrough

In the discrete-time common mode correction schemes, the switches can introduce error due to channel charge and clock feedthrough.

Through simulation, these errors can be predicted and corrected by applying a correction signal superimposed upon the error signal to achieve the desired (target) common mode voltage.

General principle:



SUMMARY

- Advantages of differential output op amps:
 - 6 dB increase in signal amplitude
 - Cancellation of even harmonics
 - Cancellation of common mode signals including clock feedthrough
- Disadvantages of differential output op amps:
 - Need for common mode output voltage stabilization
 - Compensation of common mode feedback loop
 - Difficult to interface with single-ended circuits
- Most differential output op amps are truly balanced
- For push-pull outputs, the quiescent current should be well defined
- Common mode feedback schemes include,
 - Continuous time
 - Discrete time

LECTURE 290 – LOW POWER AND LOW NOISE OP AMPS

LECTURE ORGANIZATION

Outline

- Review of subthreshold operation
- Low power op amps
- Review of MOSFET noise modeling and analysis
- Low noise op amps
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 393-414

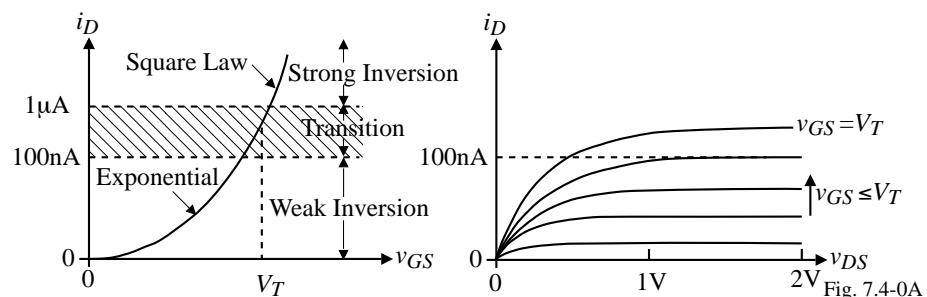
REVIEW OF SUBTHRESHOLD OPERATION

Subthreshold Operation

Most micropower op amps use transistors in the subthreshold region.

Subthreshold characteristics:

The model that has been developed for the large signal sub-threshold operation is:



$$i_D = I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \left(1 + \frac{v_{DS}}{V_A}\right) \quad \text{where } v_{DS} > 0 \quad \text{and } V_{DS(\text{sat})} = V_{ON} = V_{GS} - V_T = 2nV_t$$

Small-signal model:

$$g_m = \frac{di_D}{dv_{GS}} \Big|_Q = I_t \frac{W}{L} \frac{I_t}{nV_t} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \left(1 + \frac{v_{DS}}{V_A}\right) = \frac{I_D}{nV_t} = \frac{qI_D}{nkT} = \frac{I_D}{V_t} \frac{C_{ox}}{C_{ox} + C_{js}}$$

$$g_{ds} = \frac{di_D}{dv_{DS}} \Big|_Q \approx \frac{I_D}{V_A}$$

Boundary Between Subthreshold and Strong Inversion

It is useful to develop a means of estimating when a MOSFET is making the transition between subthreshold and strong inversion to know when to use the proper model.

The relationship developed is based on the following concept:

We will solve for the value of v_{GS} (actually $v_{GS} - V_T$) and find the drain current where these two values are equal [$v_{GS}(\text{tran.}) - V_T$].

The large signal expressions for each region are:

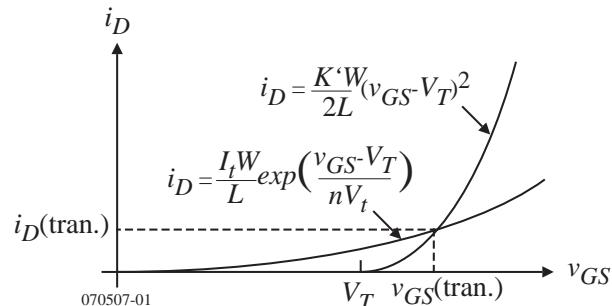
Subthreshold-

$$i_D \approx I_t \frac{W}{L} \exp\left(\frac{v_{GS}-V_T}{nV_t}\right) \Rightarrow v_{GS}-V_T = nV_t \ln\left(\frac{i_D}{I_t(W/L)}\right) \approx nV_t \left(1 - \frac{I_t(W/L)}{i_D}\right)$$

if $0.5 < i_D/(I_t W/L)$.

Strong inversion-

$$i_D = \frac{K'W}{2L} (v_{GS}-V_T)^2 \Rightarrow v_{GS}-V_T = \sqrt{\frac{2i_D}{K'(W/L)}}$$



Boundary Between Subthreshold and Strong Inversion - Continued

Equating the two large signal expressions gives,

$$nV_t \left(1 - \frac{I_t(W/L)}{i_D}\right) = \sqrt{\frac{2i_D}{K'(W/L)}} \Rightarrow n^2V_t^2 \left(1 - \frac{I_t(W/L)}{i_D}\right)^2 = \frac{2i_D}{K'(W/L)}$$

Expanding gives,

$$n^2V_t^2 \left(\frac{I_t^2(W/L)^2}{i_D^2} - \frac{2I_t(W/L)}{i_D} + 1 \right) \approx n^2V_t^2 = \frac{2i_D}{K'(W/L)} \quad \text{if } (I_t W/L)/i_D < 0.5$$

Therefore we get,

$$i_D(\text{tran.}) = \frac{K'W}{2L} n^2V_t^2$$

For example, if $K' = 120\mu\text{A/V}^2$, $W/L = 100$, and $n = 2$, then at room temperature the value of drain current at the transition between subthreshold and strong inversion is

$$i_D(\text{tran.}) = \frac{120\mu\text{A/V}^2 \cdot 100}{2} \cdot 4 \cdot (0.026)^2 = 16.22\mu\text{A}$$

One will find for UDSM technology, that weak inversion or subthreshold operation can occur at large currents for large values of W/L .

LOW POWER OP AMPS

Two-Stage, Miller Op Amp Operating in Weak Inversion

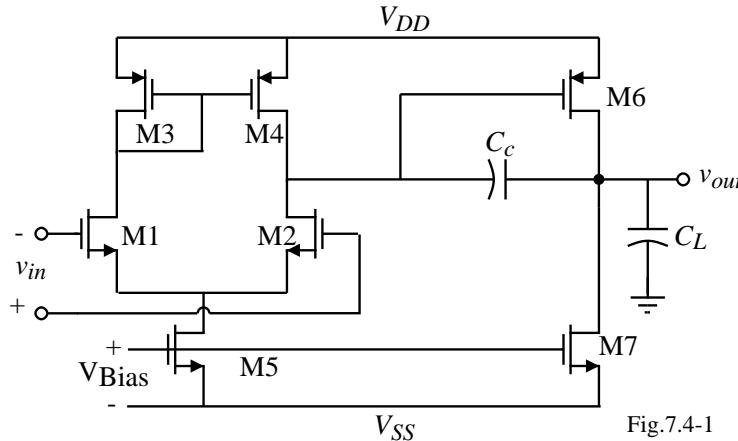


Fig.7.4-1

Low frequency response:

$$A_{vo} = g_{m2}g_{m6} \left(\frac{r_{o2}r_{o4}}{r_{o2} + r_{o4}} \right) \left(\frac{r_{o6}r_{o7}}{r_{o6} + r_{o7}} \right) = \frac{1}{n_2 n_6 (kT/q)^2 (\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)} \quad (\text{No longer } \propto \frac{1}{\sqrt{I_D}})$$

GB and SR:

$$GB = \frac{ID_1}{(n_1 kT/q)C} \quad \text{and} \quad SR = \frac{ID_5}{C} = 2 \frac{ID_1}{C} = 2GB \left(n_1 \frac{kT}{q} \right) = 2GBn_1V_t$$

Example 290-1 Gain and GB Calculations for Subthreshold Op Amp.

Calculate the gain, *GB*, and *SR* of the op amp shown above. The currents are $ID_5 = 200$ nA and $ID_7 = 500$ nA. The device lengths are 1 μ m. Values for *n* are 1.5 and 2.5 for p-channel and n-channel transistors respectively. The compensation capacitor is 5 pF. The channel length modulation parameters are $\lambda_N = 0.06V^{-1}$ and $\lambda_P = 0.08V^{-1}$. Assume that the temperature is 27 °C. If $V_{DD} = 1.5V$ and $V_{SS} = -1.5V$, what is the power dissipation of this op amp?

Solution

The low-frequency small-signal gain is,

$$A_v = \frac{1}{(1.5)(2.5)(0.026)^2(0.06 + 0.08)(0.06 + 0.08)} = 20,126 \text{ V/V}$$

The gain bandwidth is

$$GB = \frac{100 \times 10^{-9}}{2.5(0.026)(5 \times 10^{-12})} = 307,690 \text{ rps} \approx 49.0 \text{ kHz}$$

The slew rate is

$$SR = (2)(307690)(2.5)(0.026) = 0.04 \text{ V}/\mu\text{s}$$

The power dissipation is,

$$P_{diss} = 3(0.7\mu\text{A}) = 2.1\mu\text{W}$$

Push-Pull Output Op Amp in Weak Inversion

First stage gain is,

$$A_{vo} = \frac{g_{m2}}{g_{m4}} = \frac{I_{D2}n_4V_t}{I_{D4}n_2V_t} = \frac{I_{D2}n_4}{I_{D4}n_2} \cong 1$$

Total gain is,

$$A_{vo} = \frac{g_{m1}(S_6/S_4)}{(g_{ds6} + g_{ds7})} = \frac{(S_6/S_4)}{(\lambda_6 + \lambda_7)n_1V_t}$$

At room temperature ($V_t = 0.0259V$) and for typical device lengths, gains of 60dB can be obtained.

The GB is,

$$GB = \frac{g_{m1}}{C} \left(\frac{S_6}{S_4} \right) = \frac{g_{m1}b}{C}$$

where b is the current ratio between M4:M6 and M3:M8.

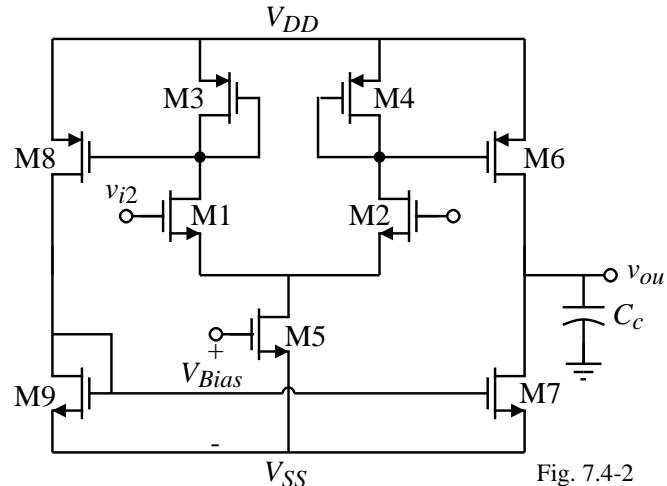


Fig. 7.4-2

Increasing the Gain of the Previous Op Amp

1.) Can reduce the currents in M3 and M4 and introduce gain in the current mirrors.

2.) Use a cascode output stage (can't use self-biased cascode, currents are too low).

$$\begin{aligned} A_v &= \left(\frac{g_{m1} + g_{m2}}{2} \right) R_{out} \\ &= \frac{g_{m1}}{\frac{g_{ds6}g_{ds10}}{g_{m10}} + \frac{g_{ds7}g_{ds11}}{g_{m11}}} \\ &= \frac{\frac{I_5}{2n_nV_t}}{\frac{I_7^2\lambda_n^2}{I_nV_t} + \frac{I_7^2\lambda_p^2}{I_pV_t}} = \left(\frac{I_5}{2I_7} \right) \left(\frac{1}{n_nV_t^2(n_n\lambda_n^2 + n_p\lambda_p^2)} \right) \end{aligned}$$

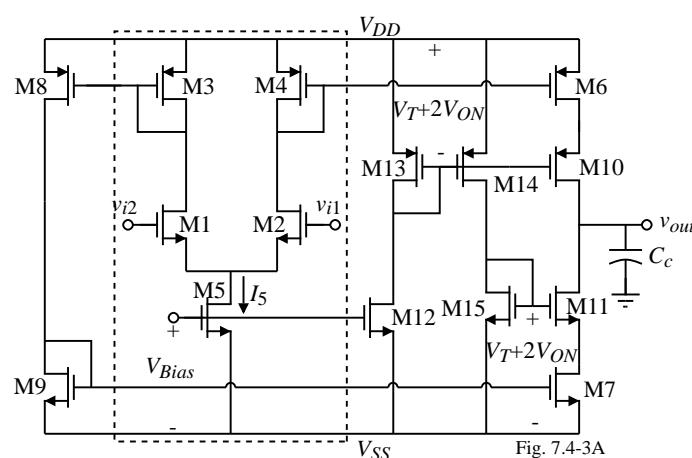


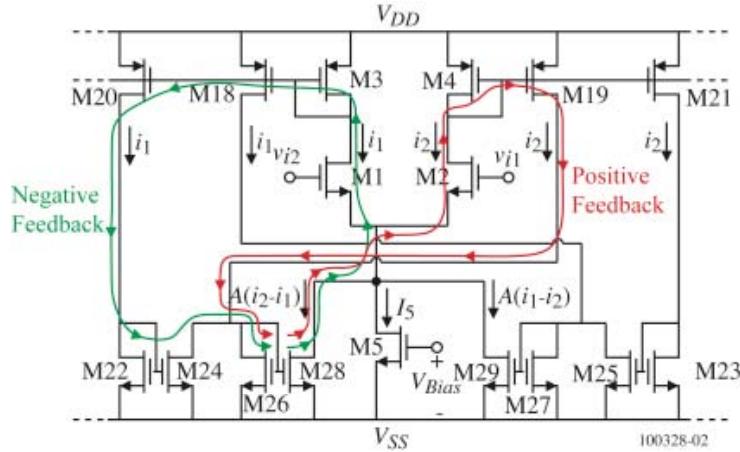
Fig. 7.4-3A

Can easily achieve gains greater than 80dB with power dissipation of less than $1\mu\text{W}$.

Increasing the Output Current for Weak Inversion Operation

A significant disadvantage of the weak inversion is that very small currents are available to drive output capacitance so the slew rate becomes very small.

Dynamically biased differential amplifier input stage:



Note that the sinking current for M1 and M2 is

$I_{sink} = I_5 + A(i_2 - i_1) + A(i_1 - i_2)$ where $(i_2 - i_1)$ and $(i_1 - i_2)$ are only positive or zero.

If $v_{i1} > v_{i2}$, then $i_2 > i_1$ and the sinking current is increased by $A(i_2 - i_1)$.

If $v_{i2} > v_{i1}$, then $i_1 > i_2$ and the sinking current is increased by $A(i_1 - i_2)$.

Dynamically Biased Differential Amplifier - Continued

How much output current is available from this circuit if there is no current gain from the input to output stage?

Assume transistors M18 through M21 are equal to M3 and M4 and that transistors M22 through M27 are all equal.

$$\text{Let } \frac{W_{28}}{L_{28}} = A \left(\frac{W_{26}}{L_{26}} \right) \text{ and } \frac{W_{29}}{L_{29}} = A \left(\frac{W_{27}}{L_{27}} \right)$$

The output current available can be found by assuming that $v_{in} = v_{j1} - v_{j2} > 0$.

$$\therefore i_1 + i_2 \equiv I_5 + A(i_2 - i_1)$$

The ratio of i_2 to i_1 can be expressed as

$$\frac{i_2}{i_1} = \exp\left(\frac{v_{in}}{nV_t}\right)$$

If the output current is $i_{OJT} = b(i_2 - i_1)$ then combining the above two equations gives,

$$i_{OUT} = \frac{bI_5 \left[\exp\left(\frac{v_{in}}{nV_t}\right) - 1 \right]}{(1+A) - (A-1)\exp\left(\frac{v_{in}}{nV_t}\right)} \quad \Rightarrow \quad i_{OUT} = \infty \text{ when } A = 2.16 \text{ and } \frac{v_{in}}{nV_t} = 1$$

where b corresponds to any current gain through current mirrors (M6-M4 and M8-M3).

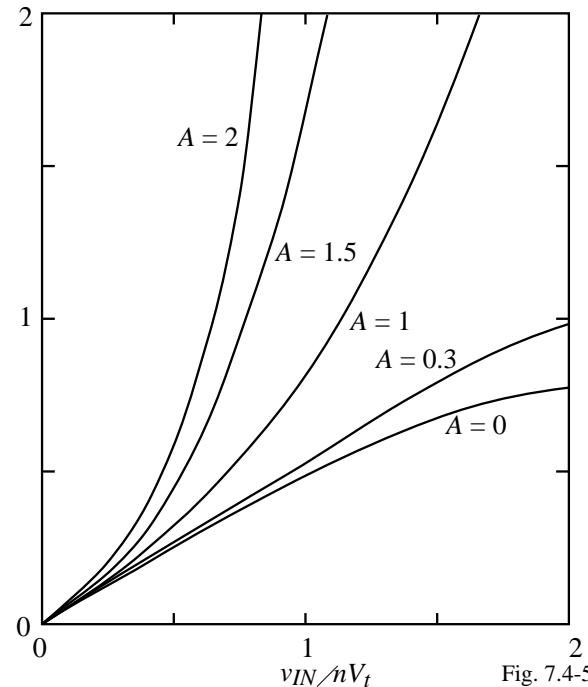
Overdrive of the Dynamically Biased Differential Amplifier

The enhanced output current is accomplished by the use of positive feedback (M28-M2-M19-M28).

The loop gain is,

$$LG = \left(\frac{g_m 28}{g_m 4} \right) \left(\frac{g_m 19}{g_m 26} \right) = A \frac{g_m 19}{g_m 4} = A$$

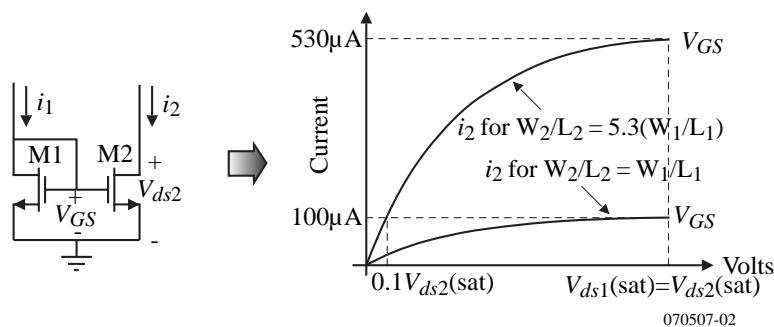
Note that as the output current increases, the transistors leave the weak inversion region and the above analysis is no longer valid.



Increasing the Output Current for Strong Inversion Operation

An interesting technique is to bias the output transistor of a current mirror in the active region and then during large overdrive cause the output transistor to become saturated causing a significant current gain.

Illustration:



Example 290-2 Current Mirror with M2 operating in the Active Region

Assume that M2 has a voltage across the drain-source of $0.1V_{ds}(\text{sat})$. Design the W_2/L_2 ratio so that $I_1 = I_2 = 100\mu\text{A}$ if $W_1/L_1 = 10$. Find the value of I_2 if M2 is saturated.

Solution

Using the value of $K_N' = 120\mu\text{A/V}^2$, we find that the saturation voltage of M2 is

$$V_{ds1}(\text{sat}) = \sqrt{\frac{2I_1}{K_N' (W_2/L_2)}} = \sqrt{\frac{200}{120 \cdot 10}} = 0.408\text{V}$$

Now using the active equation of M2, we set $I_2 = 100\mu\text{A}$ and solve for W_2/L_2 .

$$\begin{aligned} 100\mu\text{A} &= K_N' (W_2/L_2) [V_{ds1}(\text{sat}) \cdot V_{ds2} - 0.5V_{ds2}^2] \\ &= 120\mu\text{A/V}^2 (W_2/L_2) [0.408 \cdot 0.0408 - 0.5 \cdot 0.0408^2]\text{V}^2 = 1.898 \times 10^6 (W_2/L_2) \end{aligned}$$

Thus,

$$100 = 1.898(W_2/L_2) \rightarrow \frac{W_2}{L_2} = 52.7 \approx 53$$

Now if M2 should become saturated, the value of the output current of the mirror with $100\mu\text{A}$ input would be $530\mu\text{A}$ or a boosting of 5.3 times I_1 .

Implementation of the Current Mirror Boosting Concept

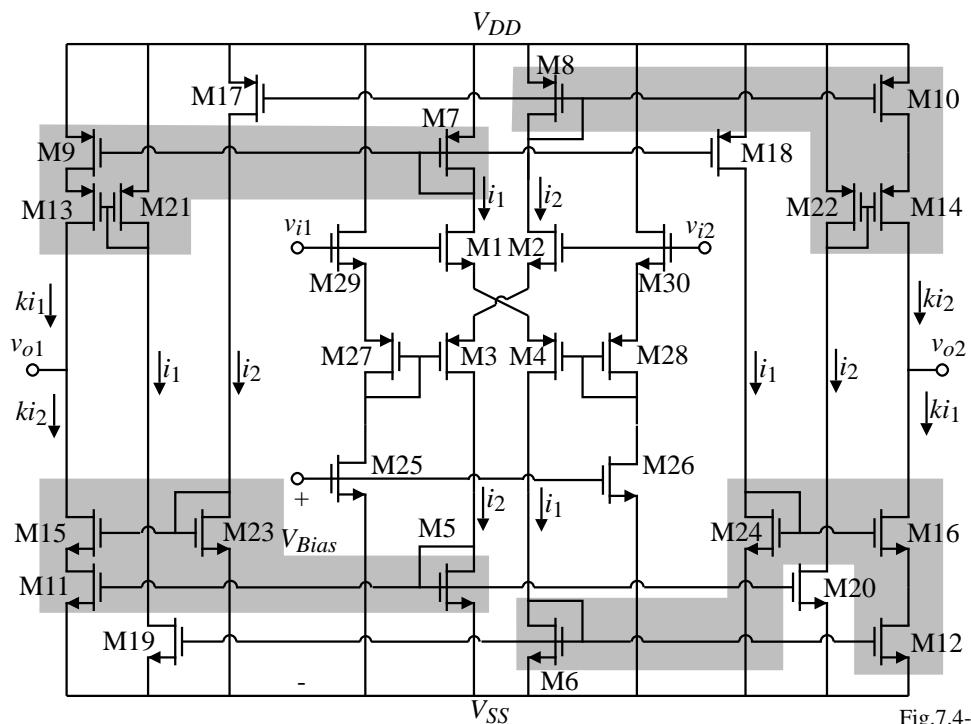


Fig.7.4-7

k = overdrive factor of the current mirror

A Better Way to Achieve the Current Mirror Boosting

It was found that when the current mirror boosting idea illustrated on the previous slide was used that when the current increased through the cascode device (M16) that V_{GS16} increased limiting the increase of V_{DS12} . This can be overcome by the following circuit.

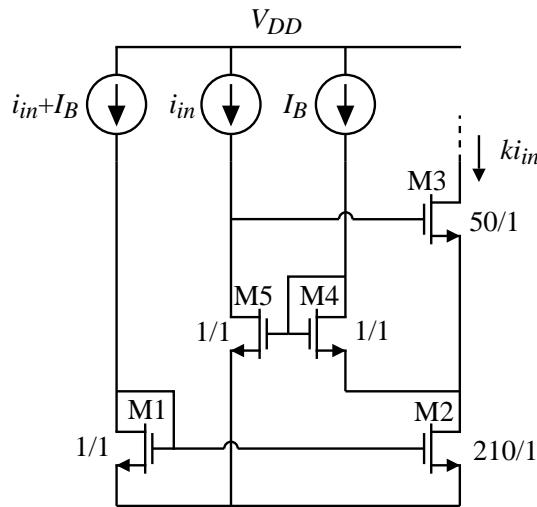
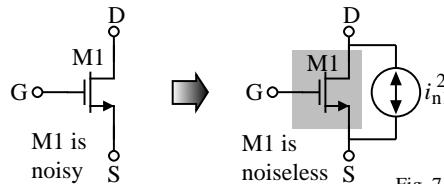


Fig. 7.4-7A

REVIEW OF MOSFET NOISE MODELING AND ANALYSIS

Transistor Noise Sources (Low-Frequency)

Drain current model:



$$i_n^2 = \left[\frac{8kTg_m}{3} + \frac{(KF)I_D}{fC_{ox}L^2} \right]$$

or $i_n^2 = \left[\frac{8kTg_m(1+\eta)}{3} + \frac{(KF)I_D}{fC_{ox}L^2} \right]$ if $v_{BS} \neq 0$

Recall that $\eta = \frac{g_{mbs}}{g_m}$

Gate voltage model assuming common source operation:

$$e_n^2 = \frac{i_N^2}{g_m^2} = \left[\frac{8kT}{3g_m} + \frac{KF}{2fC_{ox}WLK'} \right]$$

or $e_n^2 = \left[\frac{8kT}{3g_m(1+\eta)} + \frac{KF}{2fC_{ox}WLK'} \right]$ if $v_{BS} \neq 0$

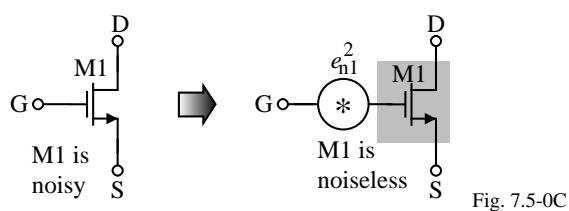


Fig. 7.5-0C

Minimization of Noise in Op Amps

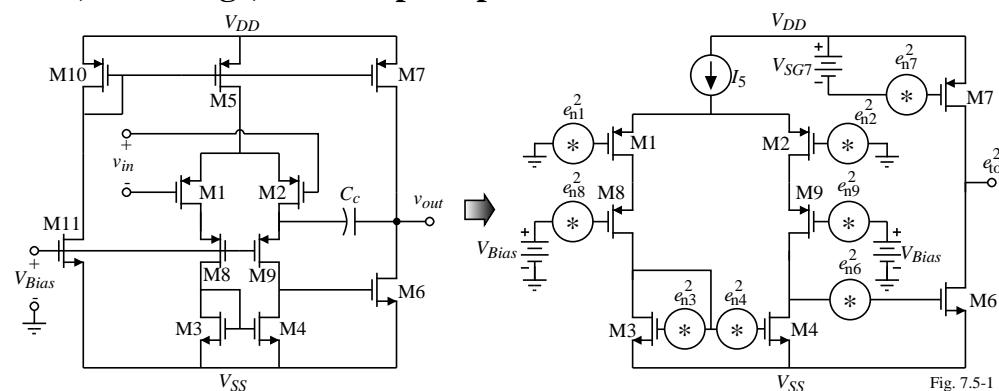
- 1.) Maximize the signal gain as close to the input as possible. (As a consequence, only the input stage will contribute to the noise of the op amp.)
- 2.) To minimize the 1/f noise:
 - a.) Use PMOS input transistors with appropriately selected dc currents and W and L values.
 - b.) Use lateral BJTs to eliminate the 1/f noise.
 - c.) Use chopper stabilization to reduce the low-frequency noise.

Noise Analysis

- 1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)
- 2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.
- 3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.

LOW NOISE OP AMPS

A Low-Noise, Two-Stage, Miller Op Amp



The total output-noise voltage spectral density, e_{to}^2 , is as follows where $g_{m8}(\text{eff}) \approx 1/r_{ds1}$,

$$e_{to}^2 = g_{m6}^2 R_{II}^2 [e_{n6}^2 + e_{n7}^2 + R_I^2 (g_{m1}^2 e_{n1}^2 + g_{m2}^2 e_{n2}^2 + g_{m3}^2 e_{n3}^2 + g_{m4}^2 e_{n4}^2 + (e_{n8}^2 / r_{ds1}^2) + (e_{n9}^2 / r_{ds2}^2))]$$

Divide by $(g_{m1} R_I g_{m6} R_{II})^2$ to get the eq. input-noise voltage spectral density, e_{eq}^2 , as

$$e_{eq}^2 = \frac{e_{to}^2}{(g_{m1} g_{m6} R_I R_{II})^2} = \frac{2 e_{n6}^2}{g_{m1}^2 R_I^2} + 2 e_{n1}^2 \left[1 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \left(\frac{e_{n3}^2}{e_{n1}^2} \right) + \frac{e_{n8}^2}{g_{m1}^2 r_{ds1}^2 e_{n1}^2} \right] \approx 2 e_{n1}^2 \left[1 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \left(\frac{e_{n3}^2}{e_{n1}^2} \right) \right]$$

where $e_{n6}^2 = e_{n7}^2$, $e_{n3}^2 = e_{n4}^2$, $e_{n1}^2 = e_{n2}^2$ and $e_{n8}^2 = e_{n9}^2$ and $g_{m1} R_I$ is large.

1/f Noise of a Two-Stage, Miller Op Amp

Consider the 1/f noise:

Therefore the noise generators are replaced by,

$$e_{ni}^2 = \frac{B}{fW_iL_i} \quad (\text{V}^2/\text{Hz}) \quad \text{and} \quad i_{ni}^2 = \frac{2BK'I_i}{fL_i^2} \quad (\text{A}^2/\text{Hz})$$

Therefore, the approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2e_{n1}^2 \left[1 + \left(\frac{K_N' B_N}{K_P' B_P} \right) \left(\frac{L_1}{L_3} \right)^2 \right] \quad (\text{V}^2/\text{Hz})$$

Comments;

- Because we have selected PMOS input transistors, e_{n1}^2 has been minimized if we choose W_1L_1 (W_2L_2) large.
- Make $L_1 \ll L_3$ to remove the influence of the second term in the brackets.

Thermal Noise of a Two-Stage, Miller Op Amp

Let us focus next on the thermal noise:

The noise generators are replaced by,

$$e_{ni}^2 \approx \frac{8kT}{3g_m} \quad (\text{V}^2/\text{Hz}) \quad \text{and} \quad i_{ni}^2 \approx \frac{8kTg_m}{3} \quad (\text{A}^2/\text{Hz})$$

where the influence of the bulk has been ignored.

The approximate equivalent input-noise voltage spectral density is,

$$e_{eq}^2 = 2e_{n1}^2 \left[1 + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \left(\frac{e_{n3}^2}{2} \right) \right] = 2e_{n1}^2 \left[1 + \sqrt{\frac{K_N W_3 L_1}{K_P W_1 L_3}} \right] \quad (\text{V}^2/\text{Hz})$$

Comments:

- The choices that reduce the 1/f noise also reduce the thermal noise.

Noise Corner:

Equating the equivalent input-noise voltage spectral density for the 1/f noise and the thermal noise gives the noise corner, f_c , as

$$f_c = \frac{3g_m B}{8kT W L}$$

Example 290-3 Design of A Two-Stage, Miller Op Amp for Low 1/f Noise

Use the model parameters of $K_N' = 120\mu\text{A}/\text{V}^2$, $K_P' = 25\mu\text{A}/\text{V}^2$, and $C_{ox} = 6\text{fF}/\mu\text{m}^2$ along with the value of $KF = 4 \times 10^{-28} \text{ F}\cdot\text{A}$ for NMOS and $0.5 \times 10^{-28} \text{ F}\cdot\text{A}$ for PMOS and design the previous op amp with $I_{D5} = 100\mu\text{A}$ to minimize the 1/f noise. Calculate the corresponding thermal noise and solve for the noise corner frequency. From this information, estimate the rms noise in a frequency range of 1Hz to 100kHz. What is the dynamic range of this op amp if the maximum signal is a 1V peak-to-peak sinusoid?

Solution

- 1.) The 1/f noise constants, B_N and B_P are calculated as follows.

$$B_N = \frac{KF}{2C_{ox}K_N'} = \frac{4 \times 10^{-28} \text{ F}\cdot\text{A}}{2 \cdot 60 \times 10^{-4} \text{ F/m}^2 \cdot 120 \times 10^{-6} \text{ A/V}^2} = 1.33 \times 10^{-22} (\text{V}\cdot\text{m})^2$$

and

$$B_P = \frac{KF}{2C_{ox}K_P'} = \frac{0.5 \times 10^{-28} \text{ F}\cdot\text{A}}{2 \cdot 60 \times 10^{-4} \text{ F/m}^2 \cdot 25 \times 10^{-6} \text{ A/V}^2} = 1.67 \times 10^{-22} (\text{V}\cdot\text{m})^2$$

- 2.) Now select the geometry of the various transistors that influence the noise performance.

To keep e_{n1}^2 small, let $W_1 = 100\mu\text{m}$ and $L_1 = 1\mu\text{m}$. Select $W_3 = 10\mu\text{m}$ and $L_3 = 20\mu\text{m}$ and let W_8 and L_8 be the same as W_1 and L_1 since they little influence on the noise.

Example 290-3 - Continued

Of course, M1 is matched with M2, M3 with M4, and M8 with M9.

$$\therefore e_{n1}^2 = \frac{B_P}{fW_1L_1} = \frac{1.67 \times 10^{-22}}{f \cdot 100 \mu\text{m} \cdot 1 \mu\text{m}} = \frac{1.67 \times 10^{-12}}{f} (\text{V}^2/\text{Hz})$$

$$e_{eq}^2 = 2 \times \frac{1.67 \times 10^{-12}}{f} \left[1 + \left(\frac{120 \cdot 1.33}{25 \cdot 1.67} \right) \left(\frac{1}{20} \right)^2 \right] = \frac{3.33 \times 10^{-12}}{f} \cdot 1.0365 = \frac{3.452 \times 10^{-12}}{f} (\text{V}^2/\text{Hz})$$

Note at 100Hz, the voltage noise in a 1Hz band is $\approx 3.45 \times 10^{-14} \text{ V}^2$ (rms) or $0.186\mu\text{V}$ (rms).

- 3.) The thermal noise at room temperature is

$$e_{n1}^2 = \frac{8kT}{3g_m} = \frac{8 \cdot 1.38 \times 10^{-23} \cdot 300}{3.500 \times 10^{-6}} = 2.208 \times 10^{-17} (\text{V}^2/\text{Hz})$$

which gives

$$e_{eq}^2 = 2 \cdot 2.208 \times 10^{-17} \left[1 + \sqrt{\frac{120 \cdot 10 \cdot 1}{25 \cdot 100 \cdot 20}} \right] = 4.416 \times 10^{-17} \cdot 1.155 = 5.093 \times 10^{-17} (\text{V}^2/\text{Hz})$$

- 4.) The noise corner frequency is found by equating the two expressions for e_{eq}^2 to get

$$f_c = \frac{3.452 \times 10^{-12}}{5.093 \times 10^{-17}} = 67.8 \text{ kHz}$$

This noise corner is indicative of the fact that the thermal noise is much less than the 1/f noise.

Example 290-1 - Continued

5.) To estimate the rms noise in the bandwidth from 1Hz to 100,000Hz, we will ignore the thermal noise and consider only the 1/f noise. Performing the integration gives

$$V_{eq(\text{rms})}^2 = \int \frac{3.452 \times 10^{-12}}{f} df = 3.452 \times 10^{-12} [\ln(100,000) - \ln(1)] = \\ 0.408 \times 10^{-10} \text{ Vrms}^2 = 6.39 \mu\text{Vrms}$$

The maximum signal in rms is 0.353V. Dividing this by $6.39 \mu\text{V}$ gives 55,279 or 94.85dB which is equivalent to more than 15 bits of resolution.

6.) Note that the design of the remainder of the op amp will have little influence on the noise and is not included in this example.

Low-Noise Op Amp using Lateral BJT's at the Input

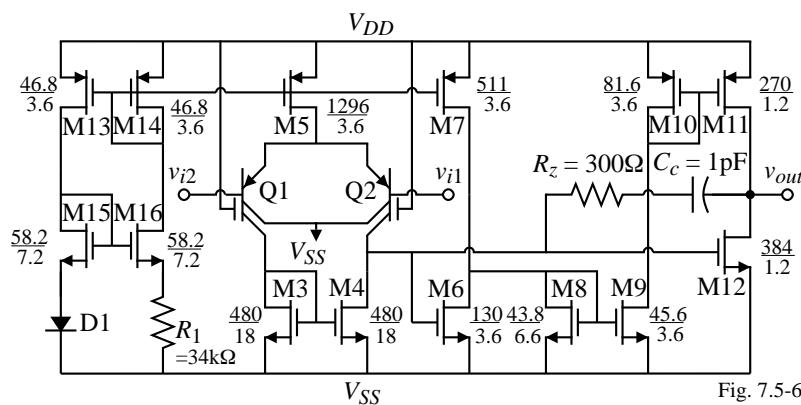


Fig. 7.5-6

Experimental noise performance:

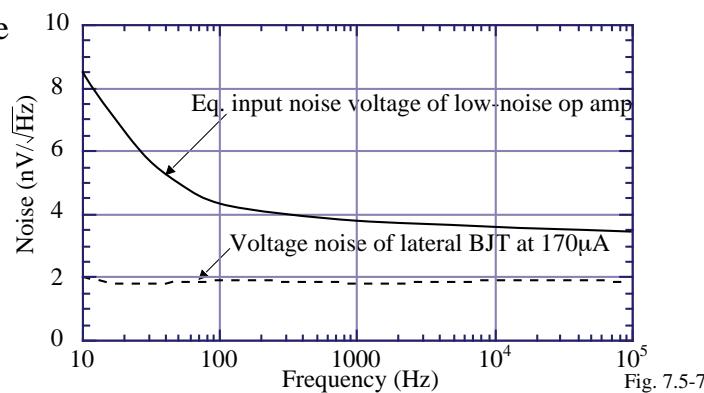


Fig. 7.5-7

Summary of Experimental Performance for the Low-Noise Op Amp

Experimental Performance	Value
Circuit area ($1.2\mu\text{m}$)	0.211 mm^2
Supply Voltages	$\pm 2.5 \text{ V}$
Quiescent Current	2.1 mA
-3dB frequency (at a gain of 20.8 dB)	11.1 MHz
e_n at 1Hz	$23.8 \text{ nV}/\sqrt{\text{Hz}}$
e_n (midband)	$3.2 \text{ nV}/\sqrt{\text{Hz}}$
$f_c(e_n)$	55 Hz
i_n at 1Hz	$5.2 \text{ pA}/\sqrt{\text{Hz}}$
i_n (midband)	$0.73 \text{ pA}/\sqrt{\text{Hz}}$
$f_c(i_n)$	50 Hz
Input bias current	$1.68 \mu\text{A}$
Input offset current	14.0 nA
Input offset voltage	1.0 mV
CMRR(DC)	99.6 dB
PSRR+(DC)	67.6 dB
PSRR-(DC)	73.9 dB
Positive slew rate (60 pF, 10 kΩ load)	$39.0 \text{ V}/\mu\text{s}$
Negative slew rate (60 pF, 10 kΩ load)	$42.5 \text{ V}/\mu\text{s}$

Chopper-Stabilized Op Amps - Doubly Correlated Sampling (DCS)

Illustration of the use of chopper stabilization to remove the undesired signal, v_u , from the desired signal, v_{in} .

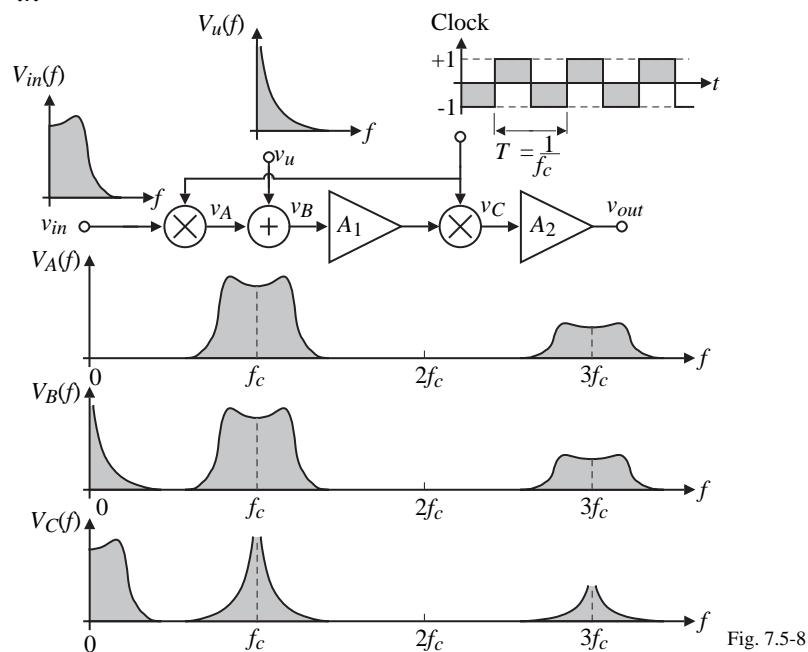


Fig. 7.5-8

Chopper-Stabilized Amplifier

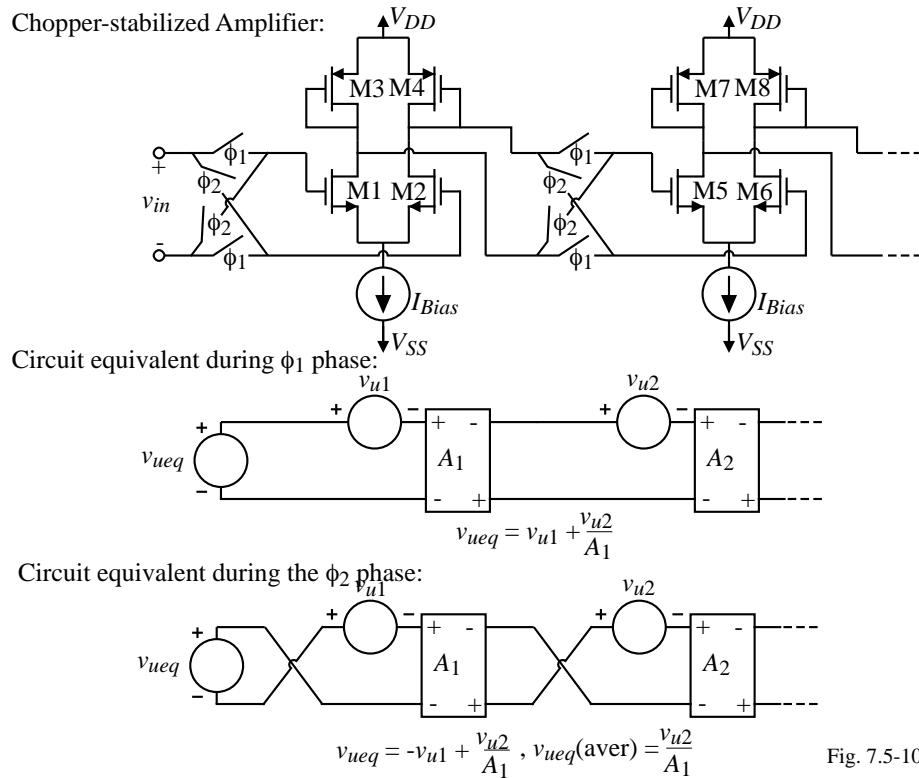
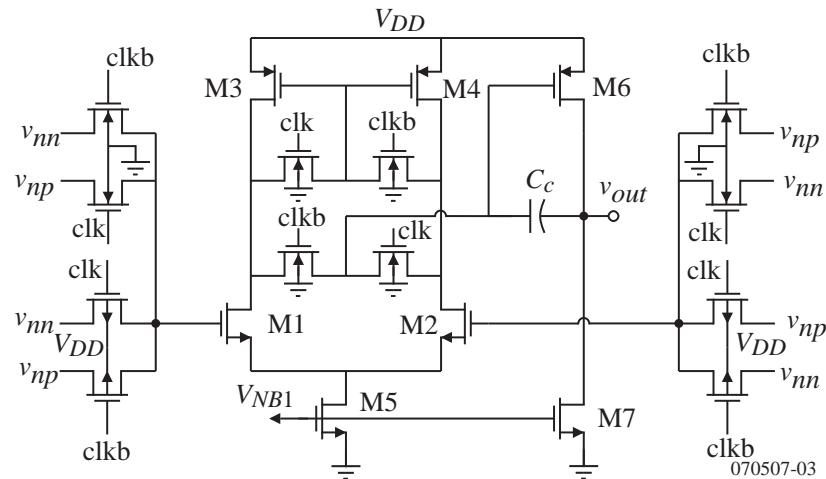


Fig. 7.5-10

Example of a Two-Stage, Chopper-Stabilized Op Amp



Experimental Noise Response of the Chopper-Stabilized Amplifier

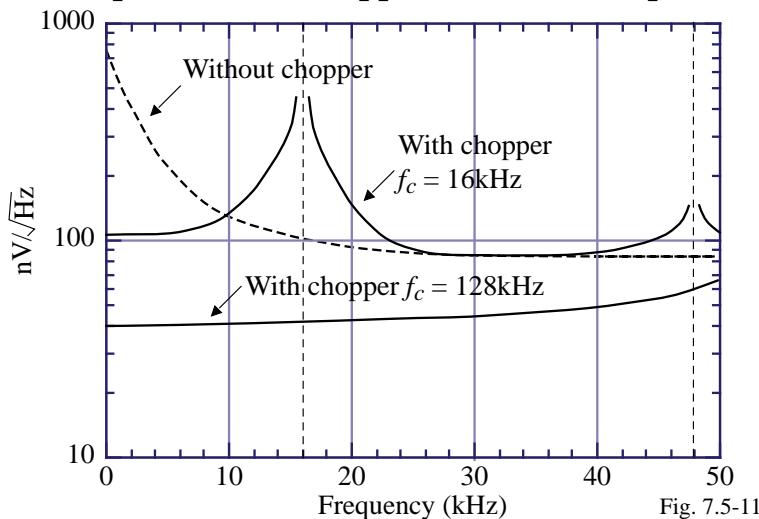


Fig. 7.5-11

Comments:

- The switches in the chopper-stabilized op amp introduce a thermal noise equal to kT/C where k is Boltzmann's constant, T is absolute temperature and C are capacitors charged by the switches (parasitics in the case of the chopper-stabilized amplifier).
- Requires two-phase, non-overlapping clocks.
- Trade-off between the lowering of $1/f$ noise and the introduction of the kT/C noise.

Improved Chopper Operation

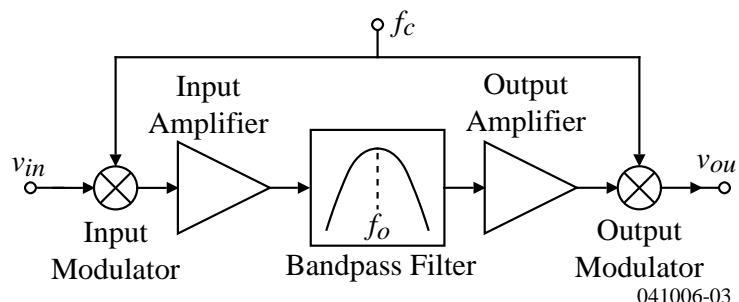
In some cases, there are spurious signals in the neighborhood of the chopping frequencies and its harmonics. These spurious signals such as common-mode interference can mix to the baseband since the chopper amplifier is a time variant system and therefore inherently nonlinear.

A bandpass filter centered at the clock frequency can be used to eliminate the aliasing of the spurious signals and achieve a reduction in effective offset.

Let $\varepsilon = \frac{f_c - f_o}{f_o}$ and σ_ε be a given bound of ε . It can be shown[†] that the achievable effective offset reduction, EOR , and the optimum Q for the bandpass filter, Q_{opt} , is

$$EOR = \frac{8Q}{\pi(1 + 8Q_2\varepsilon)}, \quad \varepsilon \ll 1 \quad \text{and} \quad Q_{opt} = 1/\sqrt{8\sigma_\varepsilon}$$

Improvements of 14dB reduction in effective offset are possible for $\varepsilon = 0.8\%$.



041006-03

[†] C. Menolfi and Q. Huang, "A Fully Integrated, Untrimmed CMOS Instrumentation Amplifier with Submicrovolt Offset," *IEEE J. of Solid-State Circuits*, vol. 34, no.8, March 1999, pp. 415-420.

SUMMARY

- Operation of transistors for low power op amps is generally in weak inversion
- Boosting techniques are needed to get output sourcing and sinking currents that are larger than that available during quiescent operation
- Be careful about using circuits at weak inversion, i.e. the self-biased cascode will cause the resistor to be too large
- Primary sources of noise for CMOS circuits is thermal and 1/f
- Noise analysis:
 - 1.) Insert a noise generator for each transistor that contributes to the noise. (Generally ignore the current source transistor of source-coupled pairs.)
 - 2.) Find the output noise voltage across an open-circuit or output noise current into a short circuit.
 - 3.) Reflect the total output noise back to the input resulting in the equivalent input noise voltage.
- Noise is reduced in op amps by making the input stage gain as large as possible and reducing the noise of this stage as much as possible.
- The input stage noise can be reduced by using lateral BJTs (particularly the 1/f noise)
- Doubly correlated sampling can transfer the noise at low frequencies to the clock frequency (this technique is used to achieve low input offset voltage op amps).

LECTURE 300 – LOW VOLTAGE OP AMPS

LECTURE ORGANIZATION

Outline

- Introduction
- Low voltage input stages
- Low voltage gain stages
- Low voltage bias circuits
- Low voltage op amps
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 415-432

INTRODUCTION

Implications of Low-Voltage, Strong-Inversion Operation

- Reduced power supply means decreased dynamic range
- Nonlinearity will increase because the transistor is working close to $V_{DS}(\text{sat})$
- Large values of λ because the transistor is working close to $V_{DS}(\text{sat})$
- Increased drain-bulk and source-bulk capacitances because they are less reverse biased.
- Large values of currents and W/L ratios to get high transconductance
- Small values of currents and large values of W/L will give small $V_{DS}(\text{sat})$
- Severely reduced input common mode range
- Switches will require charge pumps

What are the Limits of Power Supply?

The limit comes when there is no signal range left when the dc drops are subtracted from V_{DD} .

Minimum power supply (no signal swing range):

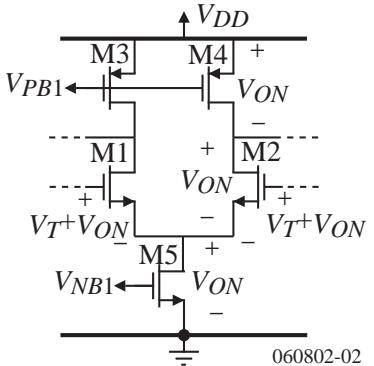
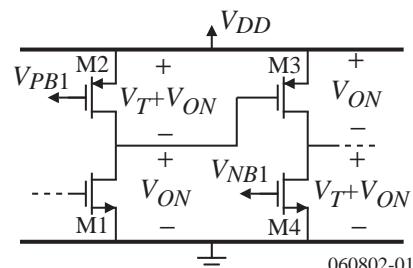
$$V_{DD}(\text{min.}) = V_T + 2V_{ON}$$

For differential amplifiers, the minimum power supply is:

$$V_{DD}(\text{min.}) = 3V_{ON}$$

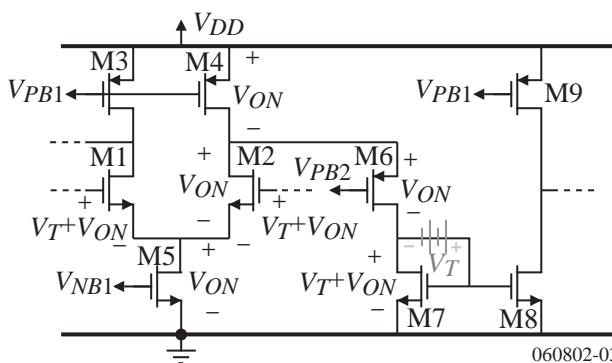
However, to have any input common mode range, the effective minimum power supply is,

$$V_{DD}(\text{min.}) = V_T + 2V_{ON}$$



Minimum Power Supply Limit – Continued

The previous consideration of the differential amplifier did not consider getting the signal out of the amplifier. This will add another V_{ON} .



Therefore,

$$V_{DD}(\text{min.}) = V_T + 3V_{ON}$$

This could be reduced to $3V_{ON}$ with the floating battery but its implementation probably requires more than $3V_{ON}$ of power supply.

Note the output signal swing is $V_T + V_{ON}$ while the input common range is V_{ON} .

LOW VOLTAGE INPUT STAGES

Input Common Mode Voltage Range

Minimum power supply ($ICMR = 0$):

$$\begin{aligned} V_{DD}(\min) &= V_{SD3}(\text{sat}) - V_{T1} + V_{GS1} + V_{DS5}(\text{sat}) \\ &= V_{SD3}(\text{sat}) + V_{DS1}(\text{sat}) + V_{DS5}(\text{sat}) \end{aligned}$$

Input common-mode range:

$$\begin{aligned} V_{icm}(\text{upper}) &= V_{DD} - V_{SD3}(\text{sat}) + V_{T1} \\ V_{icm}(\text{lower}) &= V_{DS5}(\text{sat}) + V_{GS1} \end{aligned}$$

If the threshold magnitudes are 0.7V, $V_{DD} = 1.5\text{V}$ and the saturation voltages are 0.3V, then

$$V_{icm}(\text{upper}) = 1.5 - 0.3 + 0.7 = 1.9\text{V}$$

and

$$V_{icm}(\text{lower}) = 0.3 + 1.0 = 1.3\text{V}$$

giving an $ICMR$ of 0.6V.

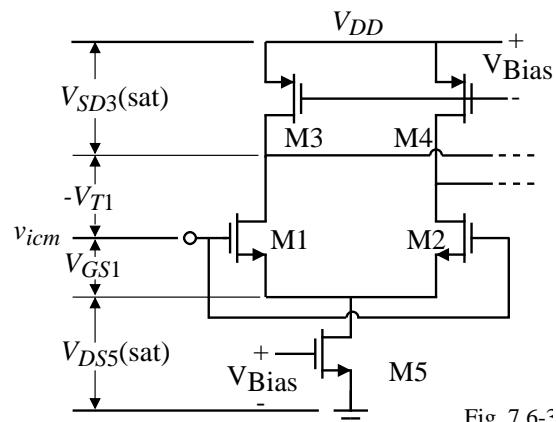


Fig. 7.6-3

Increasing $ICMR$ using Parallel Input Stages

Turn-on voltage for the n-channel input:

$$V_{onN} = V_{DSN5}(\text{sat}) + V_{GSN1}$$

Turn-on voltage for the p-channel input:

$$V_{onP} = V_{DD} - V_{SDP5}(\text{sat}) - V_{SGP1}$$

The sum of V_{onN} and V_{onP} equals the minimum power supply.

Regions of operation:

$$V_{DD} > V_{icm} > V_{onP}: \text{(n-channel on and p-channel off)}$$

$$V_{onP} \geq V_{icm} \geq V_{onN}: \text{(n-channel on and p-channel on)}$$

$$V_{onN} > V_{icm} > 0: \text{(n-channel off and p-channel on)}$$

$$g_m(\text{eq}) = g_{mN}$$

$$g_m(\text{eq}) = g_{mN} + g_{mP}$$

$$g_m(\text{eq}) = g_{mP}$$

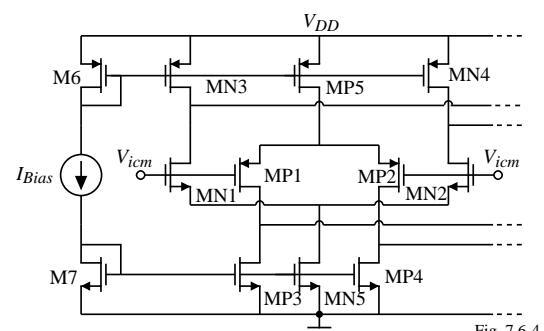


Fig. 7.6-4

where $g_m(\text{eq})$ is the equivalent input transconductance of the above input stage, g_{mN} is the input transconductance for the n-channel input and g_{mP} is the input transconductance for the p-channel input.

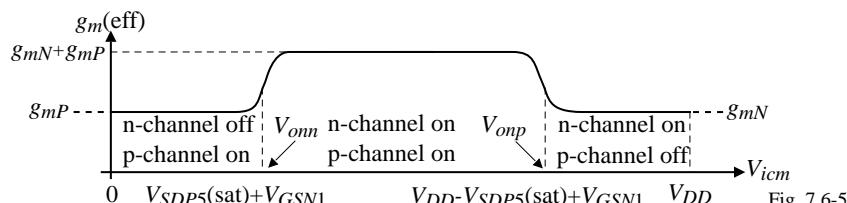


Fig. 7.6-5

Removing the Nonlinearity in Transconductances as a Function of $ICMR$

Increase the bias current in the differential amplifier that is on when the other differential amplifier is off.

Three regions of operation depending on the value of V_{icm} :

- 1.) $V_{icm} < V_{onN}$: n-channel diff. amp. off
and p-channel on with $I_p = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_P' W_P}{L_P}} 2\sqrt{I_b}$$

- 2.) $V_{onn} < V_{icm} < V_{onp}$: both on with

$$I_n = I_p = I_b:$$

$$g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}} \sqrt{I_b} + \sqrt{\frac{K_P' W_P}{L_P}} \sqrt{I_b}$$

- 3.) $V_{icm} > V_{onp}$: p-channel diff. amp. off and n-channel on with $I_n = 4I_b$:

$$g_m(\text{eff}) = \sqrt{\frac{K_N' W_N}{L_N}} 2\sqrt{I_b}$$

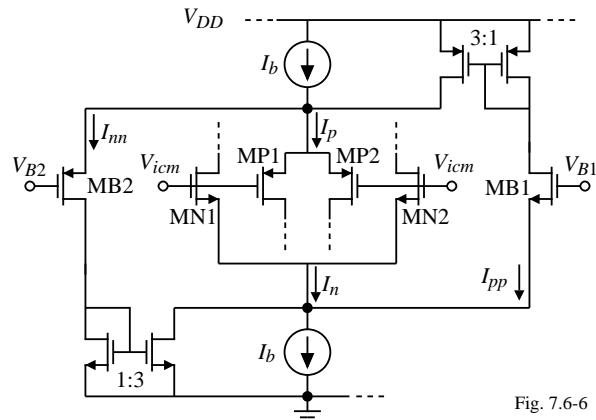


Fig. 7.6-6

CMOS Analog Circuit Design

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How Does the Current Compensation Work?

Set $V_{B1} = V_{opp}$ and $V_{B2} = V_{opp}$:

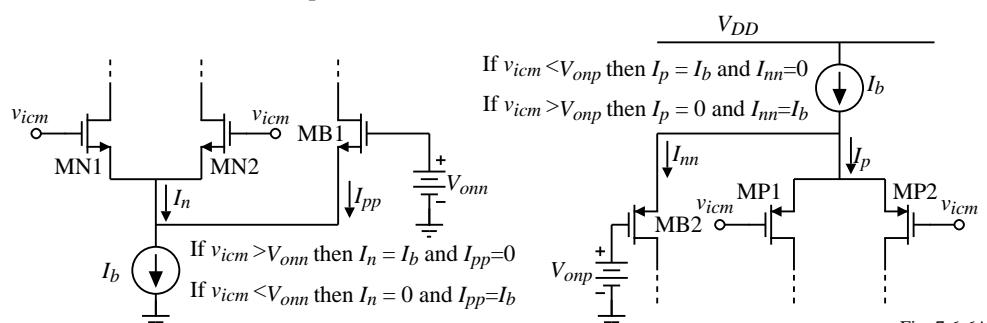
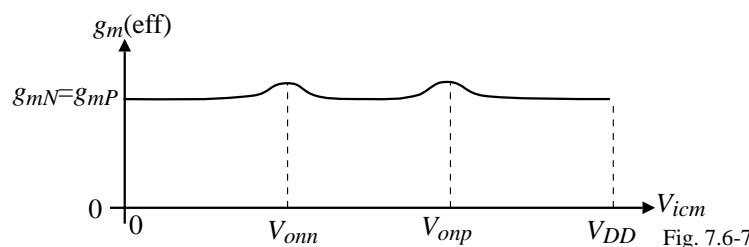


Fig. 7.6-6A

Result:



The above techniques and many similar ones are good for power supply values down to about 1.5V. Below that, different techniques must be used or the technology must be modified (natural devices).

Natural Transistors

Natural or native NMOS transistors normally have a threshold voltage around 0.1V before the threshold is increased by increasing the *p* concentration in the channel.

If these transistors are characterized, then they provide a means of achieving low voltage operation.

Minimum power supply ($ICMR = 0$):

$$V_{DD}(\min) = 3V_{ON}$$

Input common mode range:

$$V_{icm}(\text{upper}) = V_{DD} - V_{ON} + V_T(\text{natural})$$

$$V_{icm}(\text{lower}) = 2V_{ON} + V_T(\text{natural})$$

If $V_T(\text{natural}) \approx V_{ON} = 0.1\text{V}$, then

$$V_{icm}(\text{upper}) = V_{DD}$$

$$V_{icm}(\text{lower}) = 3V_{ON} = 0.3\text{V}$$

Therefore,

$$ICMR = V_{DD} - 3V_{ON} = V_{DD} - 0.3\text{V} \Rightarrow V_{DD}(\min) \approx 1\text{V}$$

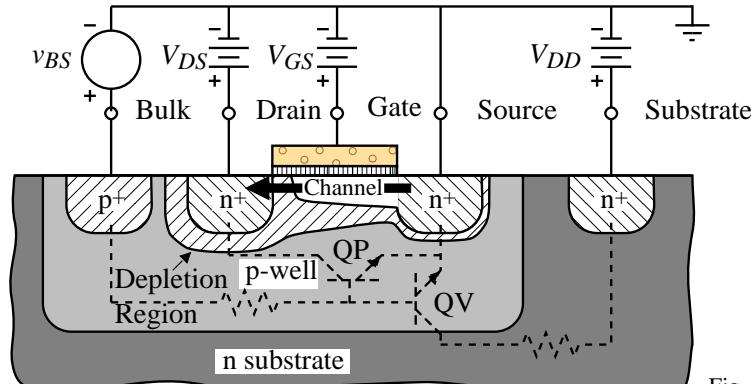
Matching tends to be better (less doping and magnitude is smaller).

Bulk-Driven MOSFET

A depletion device would permit large $ICMR$ even with very small power supply voltages because V_{GS} is zero or negative.

When a MOSFET is driven from the bulk with the gate held constant, it acts like a depletion transistor.

Cross-section of an n-channel bulk-driven MOSFET:



Large signal equation:

$$i_D = \frac{K_N' W}{2L} [V_{GS} - V_{TO} - \gamma\sqrt{2|\phi_F| - v_{BS}} + \gamma\sqrt{2|\phi_F|}]^2$$

Small-signal transconductance:

$$g_{mbs} = \frac{\gamma\sqrt{(2K_N' W/L)I_D}}{2\sqrt{2|\phi_F| - V_{BS}}}$$

Fig. 7.6-8

Bulk-Driven MOSFET - Continued

Transconductance characteristics:

Saturation: $V_{DS} > V_{BS} - V_P$ gives,

$$V_{BS} = V_P + V_{ON}$$

$$i_D = I_{DSS} \left(1 - \frac{V_{BS}}{V_P}\right)^2$$

Comments:

- g_m (bulk) $> g_m$ (gate) if $V_{BS} > 0$ (forward biased)
- Noise of both configurations are the same (any differences comes from the gate versus bulk noise)
- Bulk-driven MOSFET tends to be more linear at lower currents than the gate-driven MOSFET
- Very useful for generation of I_{DSS} floating current sources.

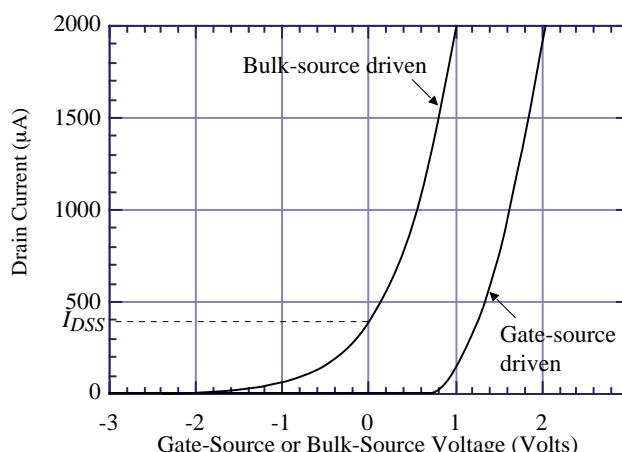


Fig. 7.6-9

Bulk-Driven, n-channel Differential Amplifier

What is the $ICMR$?

$$V_{icm}(\min) = V_{SS} + V_{DS5}(\text{sat}) + V_{BS1} = V_{SS} + V_{DS5}(\text{sat}) - |V_{P1}| + V_{DS1}(\text{sat})$$

Note that V_{icm} can be less than V_{SS} if $|V_{P1}| > V_{DS5}(\text{sat}) + V_{DS1}(\text{sat})$

$$V_{icm}(\max) = ?$$

As V_{icm} increases, the current through M1 and M2 is constant so the source increases. However, the gate voltage stays constant so that V_{GS1} decreases. Since the current must remain constant through M1 and M2 because of M5, the bulk-source voltage becomes less negative causing V_{TN1} to decrease and maintain the currents through M1 and M2 constant. If V_{icm} is increased sufficiently, the bulk-source voltage will become positive. However, current does not start to flow until V_{BS} is greater than 0.3 volts so the effective $V_{icm}(\max)$ is

$$V_{icm}(\max) \approx V_{DD} - V_{SD3}(\text{sat}) - V_{DS1}(\text{sat}) + V_{BS1}.$$

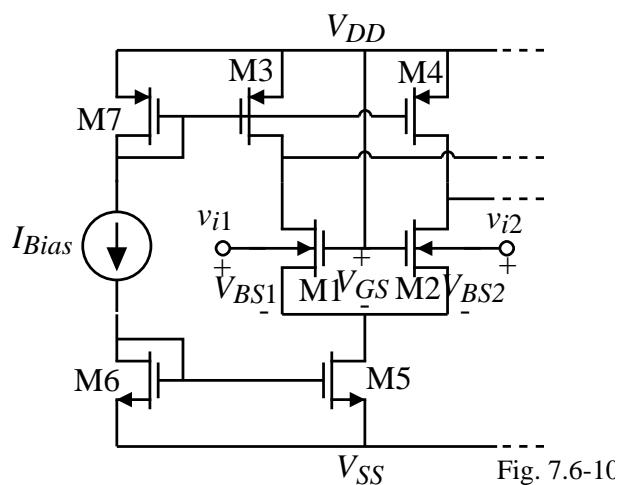
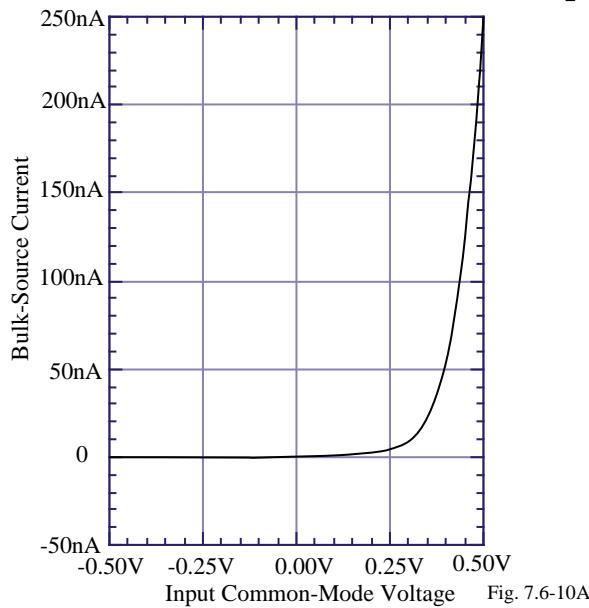


Fig. 7.6-10

Illustration of the *ICMR* of the Bulk-Driven, Differential Amplifier



Comments:

- Effective *ICMR* is from V_{SS} to $V_{DD} - 0.3V$
- The transconductance of the input stage can vary as much as 100% over the *ICMR* which makes it very difficult to compensate

Reduction of V_T through Forward Biasing the Bulk-Source

The bulk can be used to reduce the threshold sufficiently to permit low voltage applications. The key is to control the amount of forward bias of the bulk-source.

Current-Driven Bulk Technique[†]:

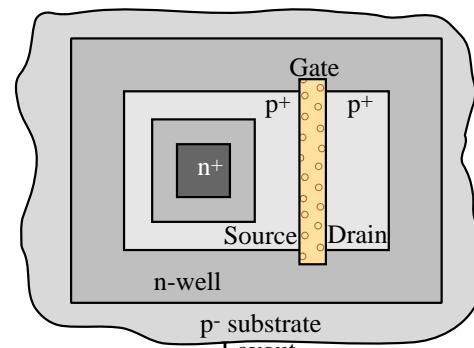
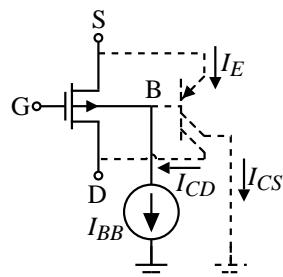
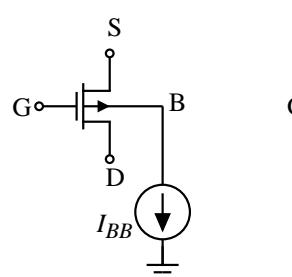


Fig. 7.6-19

Problem:

Want to limit the BJT current to some value called, I_{max} .

Therefore,

$$I_{BB} = \frac{I_{max}}{\beta_{CS} + \beta_{CD} + 1}$$

[†] T. Lehmann and M. Cassia, "1V Power Supply CMOS Cascode Amplifier," *IEEE J. of Solid-State Circuits*, Vol. 36, No. 7, 2001.
CMOS Analog Circuit Design

Current-Driven Bulk Technique

Bias circuit for keeping the I_{max} defined independent of BJT betas.

Note:

$$\begin{aligned} I_{D,C} &= I_{CD} + I_D \\ I_{S,E} &= I_D + I_E + I_R \end{aligned}$$

The circuit feedback causes a bulk bias current I_{BB} and hence a bias voltage V_{BIAS} such that

$$I_{S,E} = I_D + I_{BB}(1 + \beta_{CS} + \beta_{CD}) + I_R$$

Use V_{Bias1} and V_{Bias2} to set $I_{D,C} \approx 1.1I_D$,

$I_{S,E} \approx 1.3I_D$ and $I_R \approx 0.1I_D$ which sets I_{BB} at $0.1I_D$ assuming we can neglect I_{CS} with respect to I_{CD} .

For this circuit to work, the following conditions must be satisfied:

$$V_{BE} < V_{TN} + I_{RR} \quad \text{and} \quad |V_{TP}| + V_{DS(\text{sat})} < V_{TN} + I_{RR}$$

If $|V_{TP}| > V_{TN}$, then the level shifter I_{RR} can be eliminated.

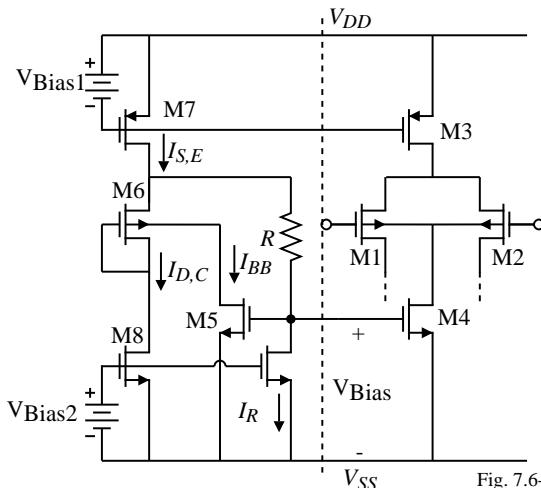
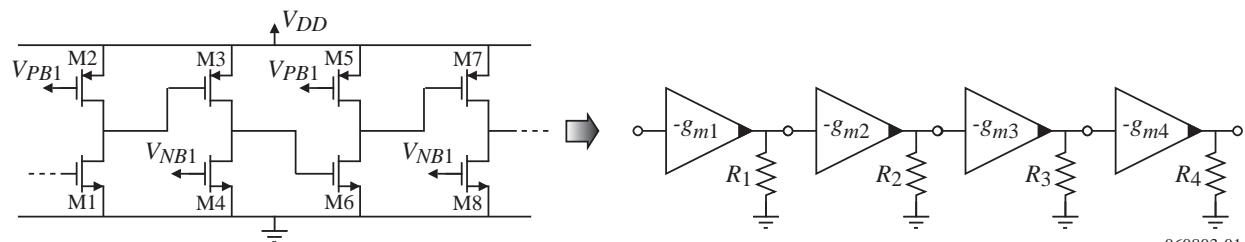


Fig. 7.6-20

LOW VOLTAGE GAIN STAGES

Cascade Stages

Simple cascade of inverters:



The problem with this approach is the number of poles that occur (one per stage) if the amplifier is to be used in a closed loop application.

Nested Miller Compensation

Principle: Use Miller compensation to split the poles within a feedback loop.

Compensating Results:

- 1) C_{m1} pushes p_4 to higher frequencies and p_3 down to lower frequencies
- 2) C_{m2} pushes p_2 to higher frequencies and p_1 down to lower frequencies
- 3) C_{m3} pushes p_3 to higher frequencies (feedback path) & pulls p_1 further to lower frequencies

Equations:

$$GB \approx g_m 1 / C_{m3} \quad p_2 \approx g_m 2 / C_{m3} \quad p_3 \approx g_m 3 C_{m3} / (C_{m1} C_{m2}) \quad p_4 \approx g_m 4 / C_L$$

The objective is to get all poles larger than GB :

$$GB < p_2, p_3, p_4$$

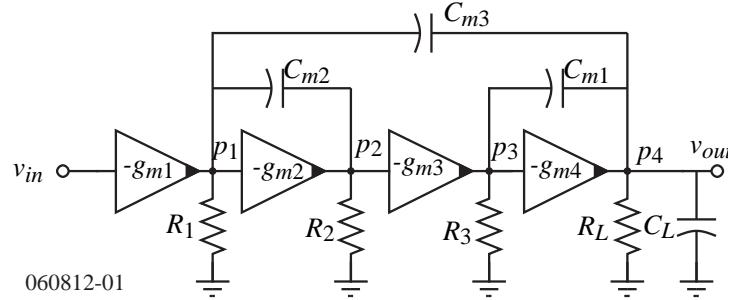
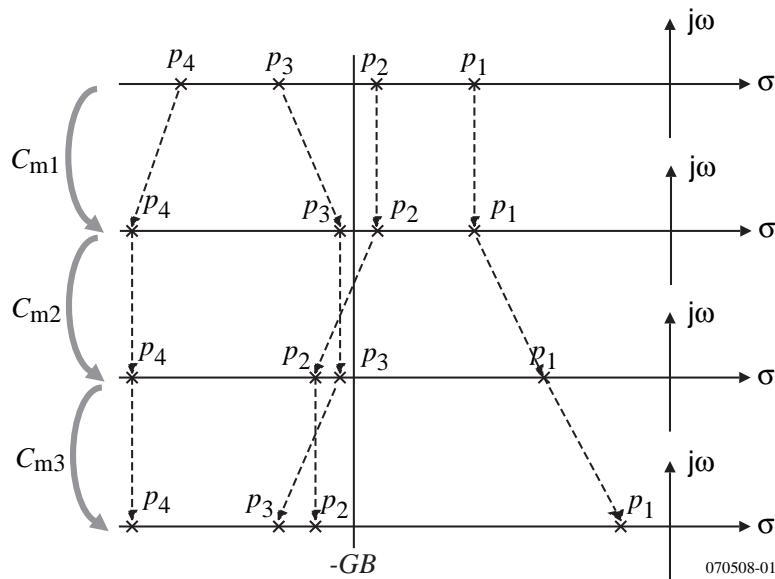


Illustration of the Nested Miller Compensation Technique

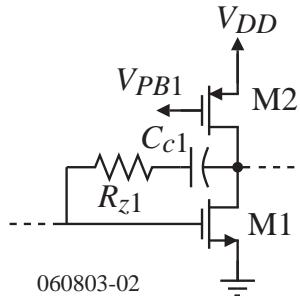


This approach is complicated by the feedforward paths which create RHP zeros.

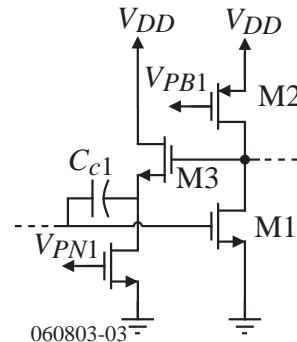
Elimination of the RHP Zeros

The following are least three ways in which the RHP zeros can be eliminated.

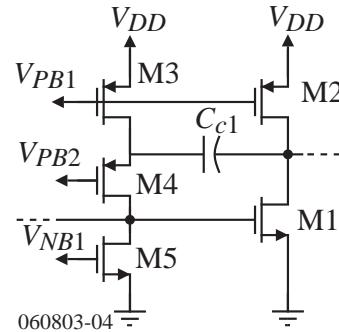
- 1.) Nulling resistor.
- 2.) Feedback only – buffer.
- 3.) Feedback only – gain.



$$z_1 = \frac{1}{C_{c1}(1/g_{m1} - R_{z1})}$$



Increases the minimum power supply by V_{ON} .

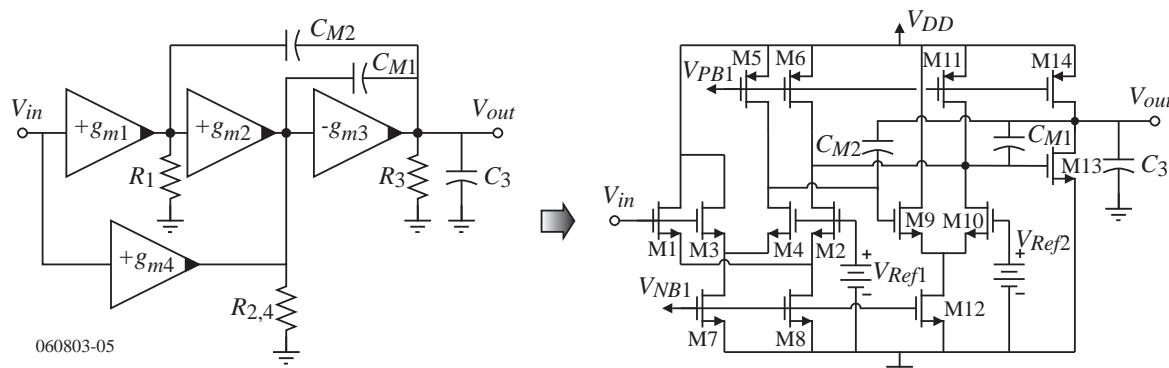


Increases the pole and increases the minimum power supply by V_{ON} .

Use of LHP Zeros to Compensate Cascaded Amplifiers

Principle: Feedforward around a noninverting stage creates a LHP zero or inverting feedforward around an inverting stage also creates a LHP zero.

Example of Multipath, Nested Miller Compensation[†]:

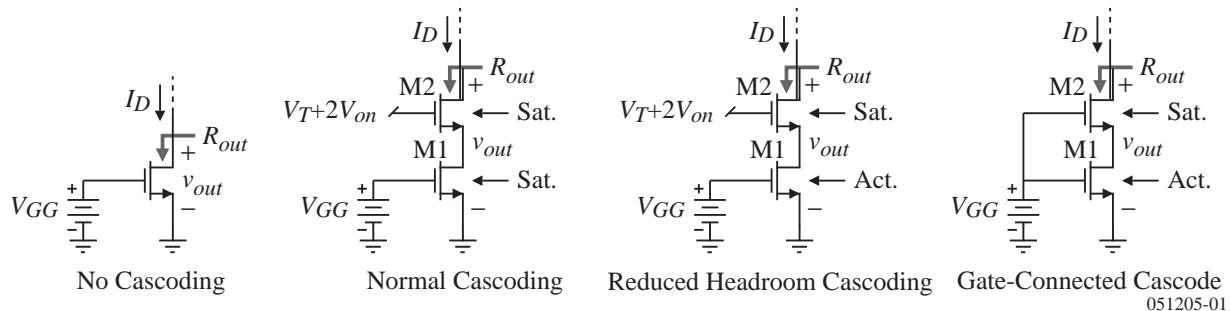


Unfortunately, the analysis becomes quite complex - for the details refer to the reference below.

[†] R. Hogervorst and J. H. Huijsing, *Design of Low-Voltage, Low-Power Operational Amplifier Cells*, Kluwer Academic Publishers, 1996, pp. 127-131.
CMOS Analog Circuit Design

Cascoding

Possibilities that trade off output resistance and headroom:



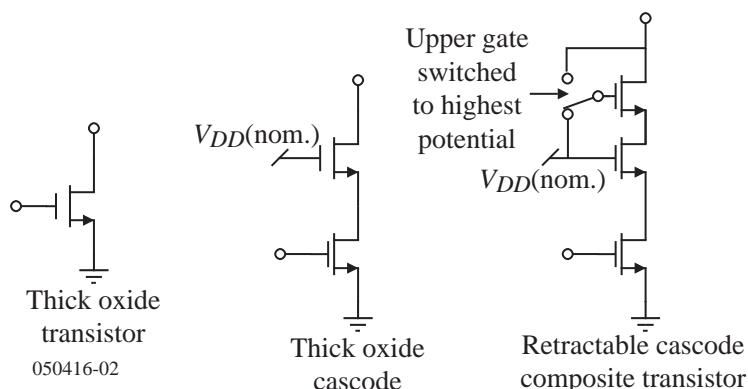
	No Cascode	Normal Cascode	Reduced Headroom Cascode	Gate-Connected Cascode
$\frac{v_{out}}{V_{on1}}$	1	$1 + \sqrt{\frac{\beta_1}{\beta_2}}$	$1 + \sqrt{\frac{\beta_1}{\beta_2}}(2x-x^2)$	$2x + \sqrt{\frac{\beta_1}{\beta_2}}(2x-x^2)$
$\frac{R_{out}}{r_{ds}}$	1	$\sqrt{\frac{2\beta_2}{\lambda^2 ID}}$	$\frac{\sqrt{2\beta_2(x-0.5x^2)}}{\sqrt{\beta_1(1-x)} + \lambda\sqrt{ID}\sqrt{x-0.5x^2}}$	$\frac{\sqrt{2\beta_2(x-0.5x^2)}}{\sqrt{\beta_1(1-x)} + \lambda\sqrt{ID}\sqrt{x-0.5x^2}}$

Note: $v_{DS}(\text{active}) = x \cdot V_{on1} = x \cdot (V_{GG} - V_T)$

$x = 0.1$ and $\beta_2 = 9\beta_1 \rightarrow v_{out} = 1.145V_{on1}$ and $R_{out} = 1.45r_{ds}$ for reduced headroom cascode

Solutions to the Low Headroom Problem – High Voltage Tolerant Circuits

High voltage tolerant transistors in standard CMOS[†]:



(Transistor symbols with additional separation between the gate line and the channel line represent thick oxide transistors.)

[†] Anne-Johan Annema, et. Al., “5.5-V I/O in a 2.5-V 0.25 μ m CMOS Technology,” *IEEE J. of Solid-State Circuits*, Vol. 36, No. 3, March 2001, pp. 528-538.

LOW VOLTAGE BIAS CIRCUITS

A Low-Voltage Current Mirror with Wide Input and Output Swings

The current mirror below requires a power supply of $V_T + 3V_{ON}$ and has a $V_{in}(\min) = V_{ON}$ and a $V_{out}(\min) = 2V_{ON}$ (less for the regulated cascode output mirror).

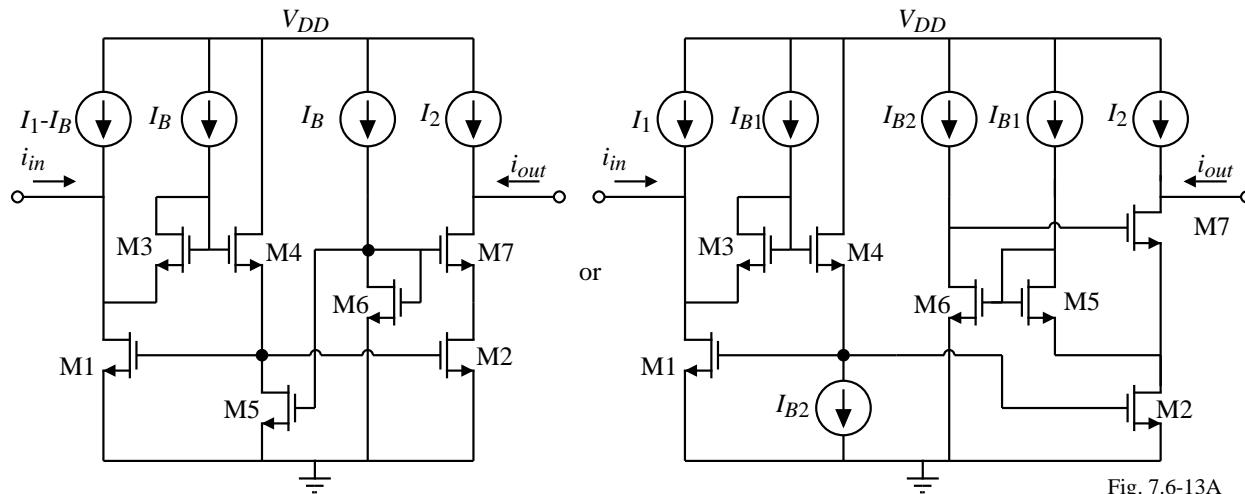
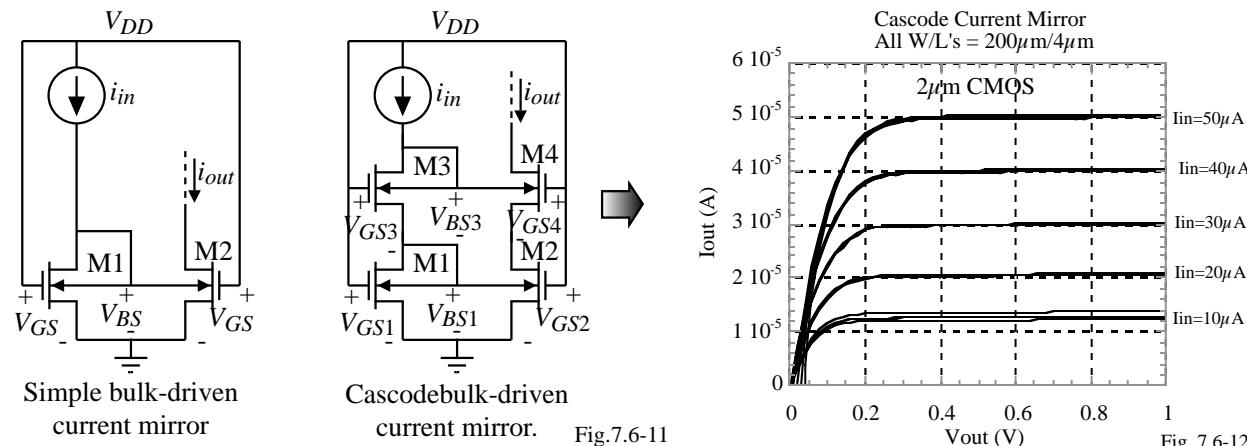


Fig. 7.6-13A

Low-Voltage Current Mirrors using the Bulk-Driven MOSFET

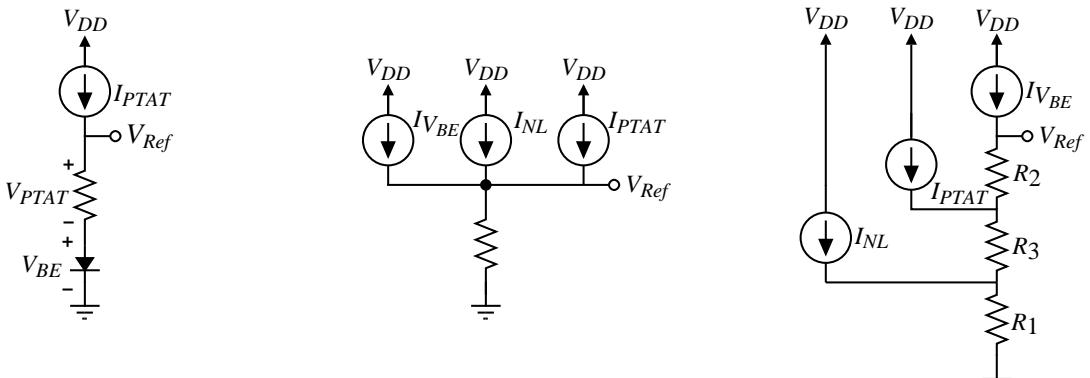
The biggest problem with current mirrors is the large minimum input voltage required for previously examined current mirrors.

If the bulk-driven MOSFET is biased with a current that exceeds I_{DSS} then it is enhancement and can be used as a current mirror.



The cascode current mirror gives a minimum input voltage of less than 0.5V for currents less than $100\mu\text{A}$

Bandgap Topologies Compatible with Low Voltage Power Supply



Voltage-mode bandgap topology.

Current-mode bandgap topology.

Voltage-current mode bandgap topology

Fig. 7.6-1.

Technique for Canceling the Bandgap Curvature

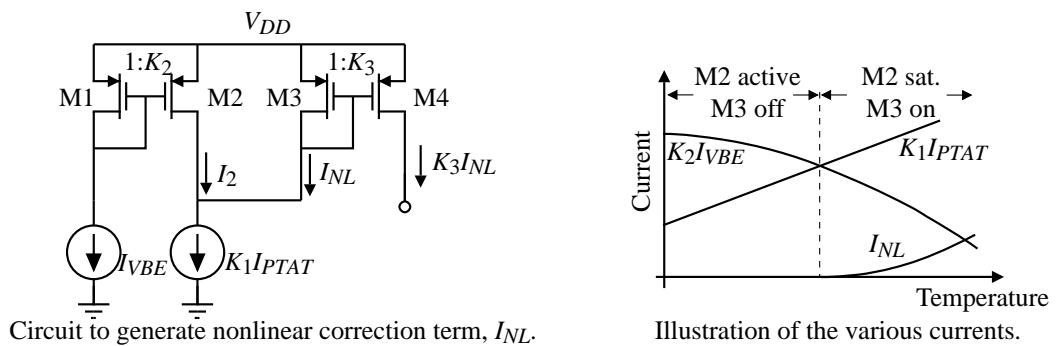
Circuit to generate nonlinear correction term, I_{NL} .

Illustration of the various currents.

Fig. 7.6-16

$$I_{NL} = \begin{cases} 0 & , \quad K_2 I_{VBE} > K_1 I_{PTAT} \\ K_1 I_{PTAT} - K_2 I_{VBE} & , \quad K_2 I_{VBE} < K_1 I_{PTAT} \end{cases}$$

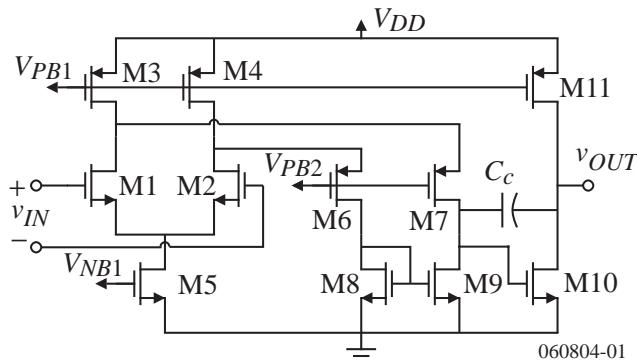
The combination of the above concept with the previous slide yielded a curvature-corrected bandgap reference of 0.596V with a TC of 20ppm/C° from -15C° to 90C° using a 1.1V power supply.[†] In addition, the line regulation was 408 ppm/V for $1.2 \leq V_{DD} \leq 10$ V and 2000 ppm/V for $1.1 \leq V_{DD} \leq 10$ V. The quiescent current was 14μA.

[†] G.A. Rincon-Mora and P.E. Allen, "A 1.1-V Current-Mode and Piecewise-Linear Curvature-Corrected Bandgap Reference," *J. of Solid-State Circuits*, vol. 33, no. 10, October 1998, pp. 1551-1554.

LOW VOLTAGE OP AMPS

A Low Voltage Op Amp using Normal Technology

$V_{DD(\min)} = 3V_{ON} + V_T$ ($ICMR = V_{ON}$):



060804-01

Performance:

$$\text{Gain} \approx g_m^2 r_{ds}^2$$

Miller compensated

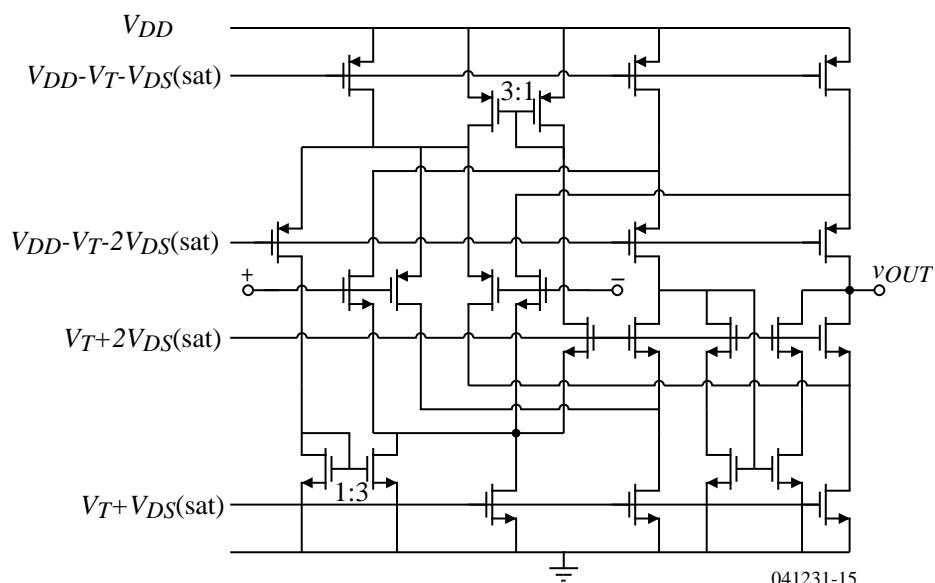
Output swing is $V_{DD} - 2V_{ON}$

Max. CM input = V_{DD}

Min. CM input = $2V_{ON} + V_T$

A Low-Voltage, Wide ICMR Op Amp

$V_{DD(\min)} = 4V_{ON} + 2V_T$ ($ICMR = V_{DD}$):



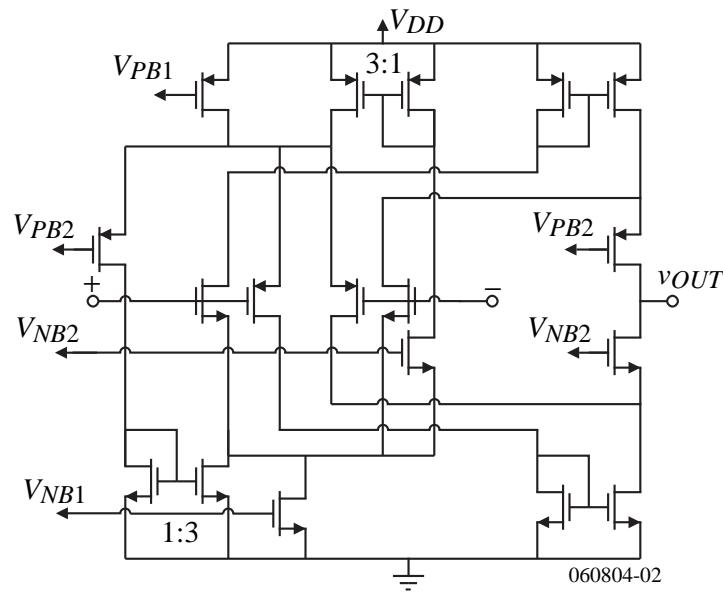
041231-15

Performance:

$$\text{Gain} \approx g_m^2 r_{ds}^2, \text{ self compensated, and output swing is } V_{DD} - 4V_{ON}$$

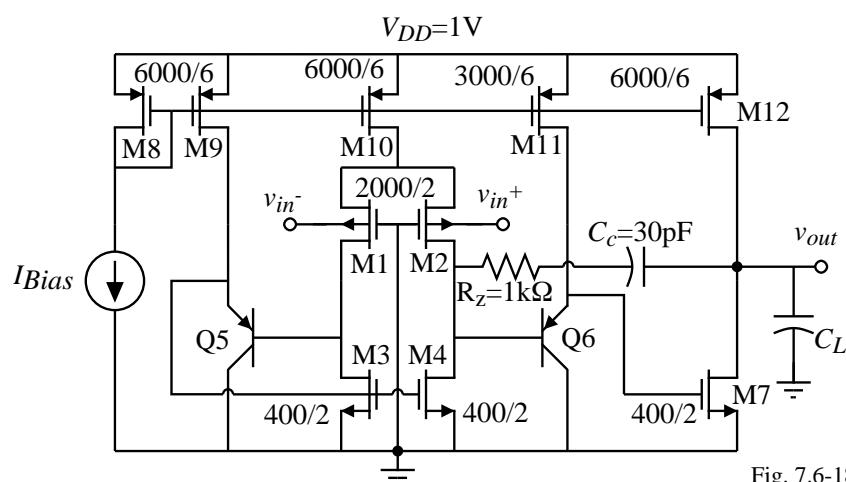
An Alternate Low-Voltage, Wide ICMR Op Amp

$V_{DD(\min)} = 4V_{ON} + 2V_T$ ($ICMR = V_{DD}$):



A 1-Volt, Two-Stage Op Amp

Uses a bulk-driven differential input amplifier.



Performance of the 1-Volt, Two-Stage Op Amp

Specification ($V_{DD}=0.5V$, $V_{SS}=-0.5V$)	Measured Performance ($C_L = 22pF$)
DC open-loop gain	49dB (V_{icm} mid range)
Power supply current	$300\mu A$
Unity-gainbandwidth (GB)	1.3MHz (V_{icm} mid range)
Phase margin	57° (V_{icm} mid range)
Input offset voltage	$\pm 3mV$
Input common mode voltage range	-0.475V to 0.450V
Output swing	-0.475V to 0.491V
Positive slew rate	+0.7V/ μsec
Negative slew rate	-1.6V/ μsec
THD, closed loop gain of -1V/V	-60dB (0.75Vp-p, 1kHz sinewave) -59dB (0.75Vp-p, 10kHz sinewave)
THD, closed loop gain of +1V/V	-59dB (0.75Vp-p, 1kHz sinewave) -57dB (0.75Vp-p, 10kHz sinewave)
Spectral noise voltage density	$367nV/\sqrt{Hz}$ @ 1kHz $181nV/\sqrt{Hz}$ @ 10kHz, $81nV/\sqrt{Hz}$ @ 100kHz $444nV/\sqrt{Hz}$ @ 1MHz
Positive Power Supply Rejection	61dB at 10kHz, 55dB at 100kHz, 22dB at 1MHz
Negative Power Supply Rejection	45dB at 10kHz, 27dB at 100kHz, 5dB at 1MHz

CMOS Analog Circuit Design

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A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique

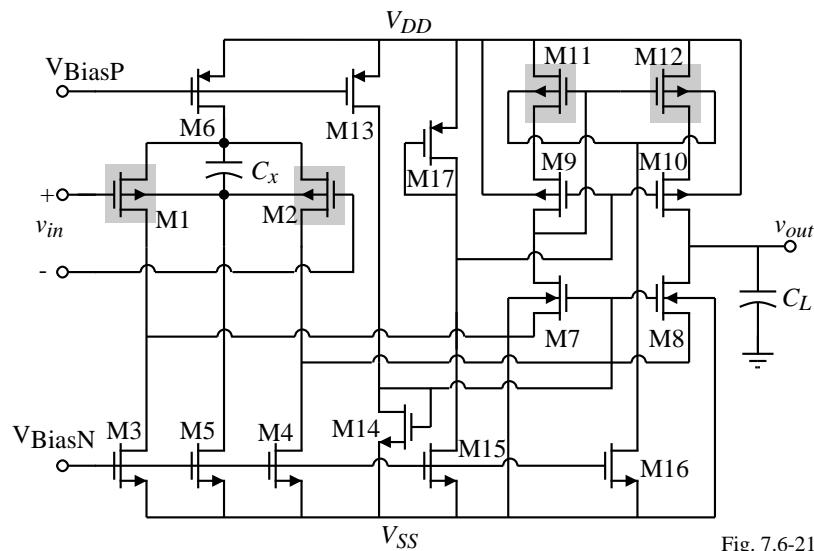


Fig. 7.6-21

Transistors with forward-biased bulks are in a shaded box.

For large common mode input changes, C_x , is necessary to avoid slewing in the input stage.

To get more voltage headroom at the output, the transistors of the cascode mirror have their bulks current driven.

A 1-Volt, Folded-Cascode OTA using the Current-Driven Bulk Technique - Continued

Experimental results:

0.5μm CMOS, 40μA total bias current ($C_x = 10\text{pF}$)

Supply Voltage	1.0V	0.8V	0.7V
Common-mode input range	0.0V-0.65V	0.0V-0.4V	0.0V-0.3V
High gain output range	0.35V-0.75V	0.25V-0.5V	0.2V-0.4V
Output saturation limits	0.1V-0.9V	0.15V-0.65V	0.1V-0.6V
DC gain	62dB-69dB	46dB-53dB	33dB-36dB
Gain-Bandwidth	2.0MHz	0.8MHz	1.3MHz
Slew-Rate ($C_L=20\text{pF}$)	0.5V/ μs	0.4V/ μs	0.1V/ μs
Phase margin ($C_L=20\text{pF}$)	57°	54°	48°

The nominal value of bulk current is 10nA gives a 10% increase in differential pair quiescent current assuming a BJT β of 100.

SUMMARY

- Integrated circuit power supplies are rapidly decreasing (today 2-3Volts)
- Classical analog circuit design techniques begin to deteriorate at 1.5-2 Volts
- Approaches for lower voltage circuits:
 - Use natural NMOS transistors ($V_T \approx 0.1\text{V}$)
 - Drive the bulk terminal
 - Forward bias the bulk
 - Use depletion devices
- The dynamic range will be compressed if the noise is not also reduced
- Fortunately, the threshold reduction continues to allow the techniques of this section to be used in today's technology

LECTURE 310 – OPEN-LOOP COMPARATORS

LECTURE ORGANIZATION

Outline

- Characterization of comparators
- Dominant pole, open-loop comparators
- Two-pole, open-loop comparators
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

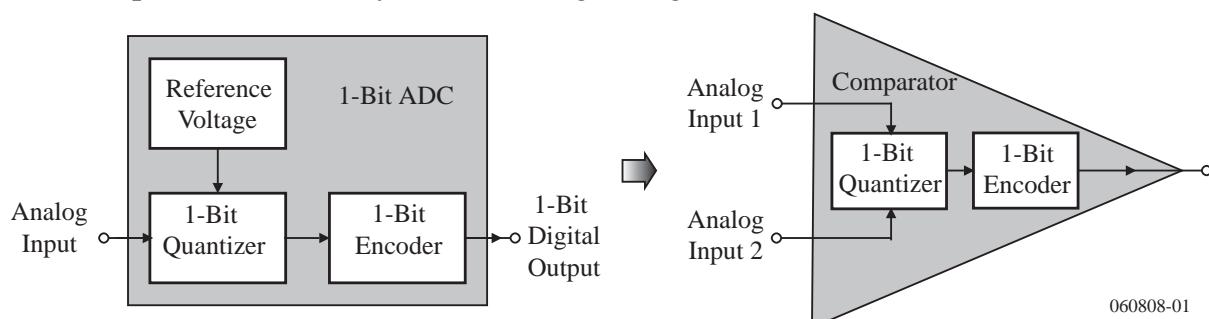
Pages 439-461

CHARACTERIZATION OF COMPARATORS

What is a Comparator?

The comparator is a circuit that compares one analog signal with another analog signal or a reference voltage and outputs a binary signal based on the comparison.

The comparator is basically a 1-bit analog-to-digital converter:



Comparator symbol:

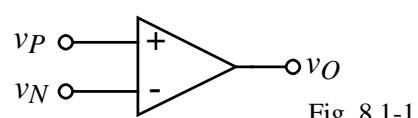


Fig. 8.1-1

Noninverting and Inverting Comparators

The comparator output is binary with the two-level outputs defined as,

V_{OH} = the high output of the comparator

V_{OL} = the low level output of the comparator

Voltage transfer function of a Noninverting and Inverting Comparator:

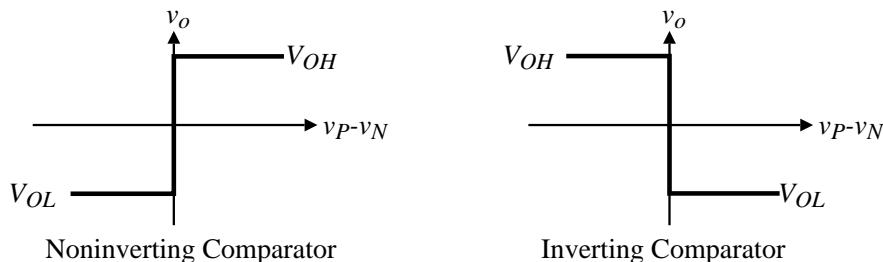


Fig. 8.1-2A

Infinite Gain Comparator

Voltage transfer function curve:

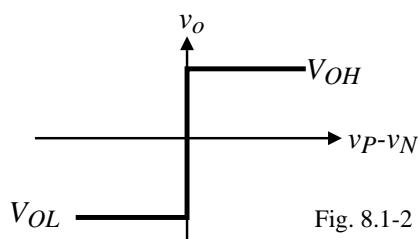
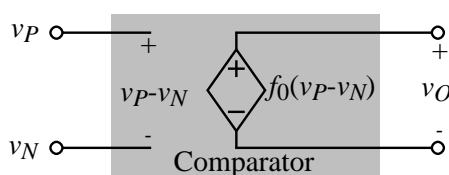


Fig. 8.1-2

Model:



$$f_0(v_p - v_n) = \begin{cases} V_{OH} & \text{for } (v_p - v_n) > 0 \\ V_{OL} & \text{for } (v_p - v_n) \leq 0 \end{cases}$$

Fig. 8.1-3

$$\text{Gain} = A_v = \lim_{\Delta V \rightarrow 0} \frac{V_{OH} - V_{OL}}{\Delta V} \quad \text{where } \Delta V \text{ is the input voltage change}$$

Finite Gain Comparator

Voltage transfer curve:

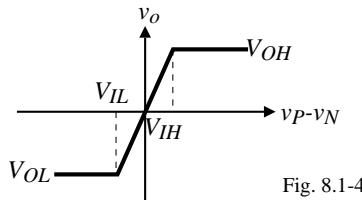


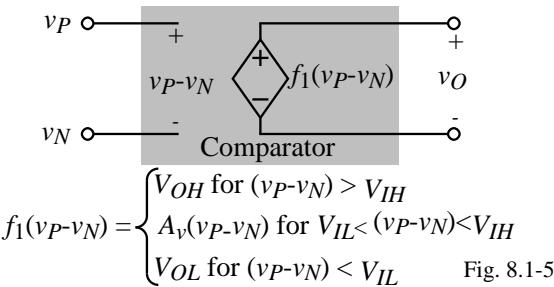
Fig. 8.1-4

where for a noninverting comparator,

$$V_{IH} = \text{smallest input voltage at which the output voltage is } V_{OH}$$

$$V_{IL} = \text{largest input voltage at which the output voltage is } V_{OL}$$

Model:



$$\text{The voltage gain is } A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}$$

Fig. 8.1-5

Input Offset Voltage of a Comparator

Voltage transfer curve:

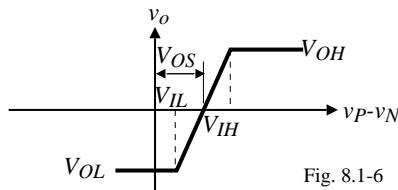


Fig. 8.1-6

V_{OS} = the input voltage necessary to make the output equal $\frac{V_{OH} + V_{OL}}{2}$ when $v_P = v_N$.

Model:

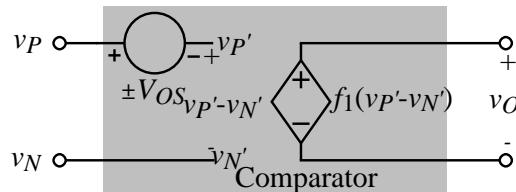


Fig. 8.1-7

Other aspects of the model:

$ICMR$ = input common mode voltage range (all transistors remain in saturation)

R_{in} = input differential resistance

R_{icm} = common mode input resistance

Comparator Noise

Noise of a comparator is modeled as if the comparator were biased in the transition region.

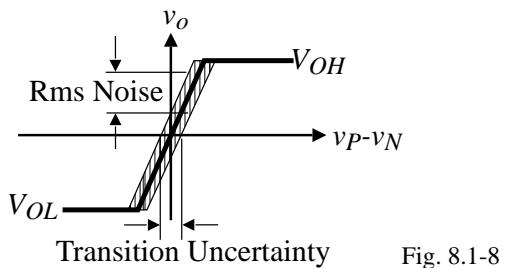


Fig. 8.1-8

Noise leads to an uncertainty in the transition region causing jitter or phase noise.

Input Common Mode Range

Because the input is analog and normally differential, the input common mode range of the comparator is also important.

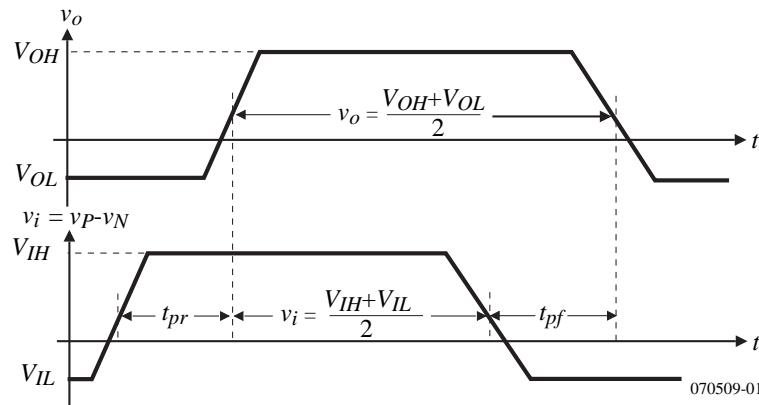
Input common mode range (*ICMR*):

ICMR = the voltage range over which the input common-mode signal can vary without influence the differential performance

As we have seen before, the *ICMR* is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region.

Propagation Delay Time

Rising propagation delay time:



$$\text{Propagation delay time} = \frac{\text{Rising propagation delay time} + \text{Falling propagation delay time}}{2}$$

$$= \frac{t_{pr} + t_{pf}}{2}$$

Linear Frequency Response – Dominant Single-Pole

Model:

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

where

$A_v(0)$ = dc voltage gain of the comparator

$\omega_c = \frac{1}{\tau_c}$ = -3dB frequency of the comparator or the magnitude of the pole

Step Response:

$$v_o(t) = A_v(0) [1 - e^{-t/\tau_c}] V_{in}$$

where

V_{in} = the magnitude of the step input.

Maximum slope of the step response:

$$\frac{dv_o(t)}{dt} = \frac{A_v(0)}{\tau_c} e^{-t/\tau_c} V_{in}$$

The maximum slope occurs at $t = 0$ giving,

$$\left. \frac{dv_o(t)}{dt} \right|_{t=0} = \frac{A_v(0)}{\tau_c} V_{in}$$

Propagation Time Delay

The rising propagation time delay for a single-pole comparator is:

$$\frac{V_{OH} - V_{OL}}{2} = A_v(0) [1 - e^{-t_p/\tau_c}] V_{in} \rightarrow t_p = \tau_c \ln \left[\frac{1}{1 - \frac{V_{OH} - V_{OL}}{2A_v(0)V_{in}}} \right]$$

Define the minimum input voltage to the comparator as,

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v(0)} \rightarrow t_p = \tau_c \ln \left[\frac{1}{1 - \frac{V_{in}(\min)}{2V_{in}}} \right]$$

Define k as the ratio, V_{in} , to the minimum input voltage, $V_{in}(\min)$,

$$k = \frac{V_{in}}{V_{in}(\min)} \rightarrow t_p = \tau_c \ln \left[\frac{2k}{2k-1} \right]$$

Thus, if $k = 1$, $t_p = 0.693\tau_c$.

Illustration:

Obviously, the more overdrive applied to the input, the smaller the propagation delay time.

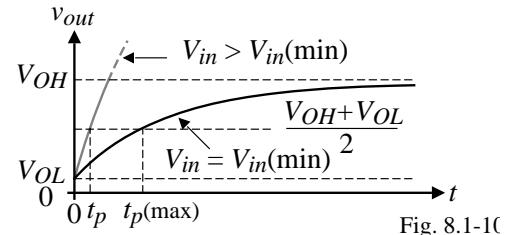
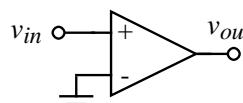


Fig. 8.1-1c

Dynamic Characteristics - Slew Rate of a Comparator

If the rate of rise or fall of a comparator becomes large, the dynamics may be limited by the slew rate.

Slew rate comes from the relationship,

$$i = C \frac{dv}{dt}$$

where i is the current through a capacitor and v is the voltage across it.

If the current becomes limited, then the voltage rate becomes limited.

Therefore for a comparator that is slew rate limited we have,

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR}$$

where

SR = slew rate of the comparator.

If $SR < |\text{maximum slope}|$, then the comparator is slewing.

Example 310-1 - Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4 , a slew rate of $1V/\mu s$, and a binary output voltage swing of 1V. Assume the applied input voltage is 10mV.

Solution

The input resolution for this comparator is $1V/10^4$ or 0.1mV. Therefore, the 10mV input is 100 times larger than $v_{in}(\text{min})$ giving a k of 100. Therefore, we get

$$t_p = \frac{1}{10^3} \ln\left(\frac{2 \cdot 100}{2 \cdot 100 - 1}\right) = 10^{-3} \ln\left(\frac{200}{199}\right) = 5.01\mu s$$

For slew rate considerations, we get

$$\text{Maximum slope} = \frac{10^4}{10^{-3}} \cdot 10\text{mV} = 10^5 \text{ V/sec.} = 0.1\text{V}/\mu s.$$

Therefore, the propagation delay time for this case is limited by the linear response and is $5.01\mu s$.

DOMINANT POLE, OPEN-LOOP COMPARATORS

Dominant Pole Comparators

Any of the self-compensated op amps provide a straight-forward implementation of an open loop comparator without any modification.

The previous characterization gives the relationships for:

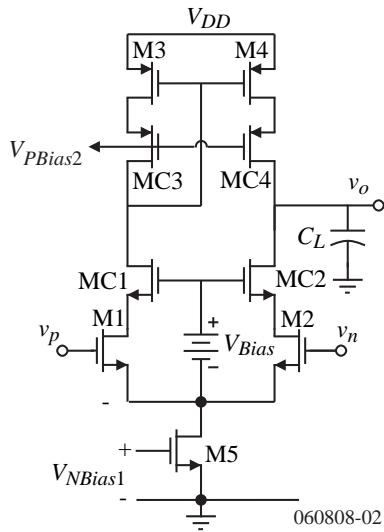
1.) The static characteristics

- Gain
- Input offset
- Noise

2.) The dynamic characteristics

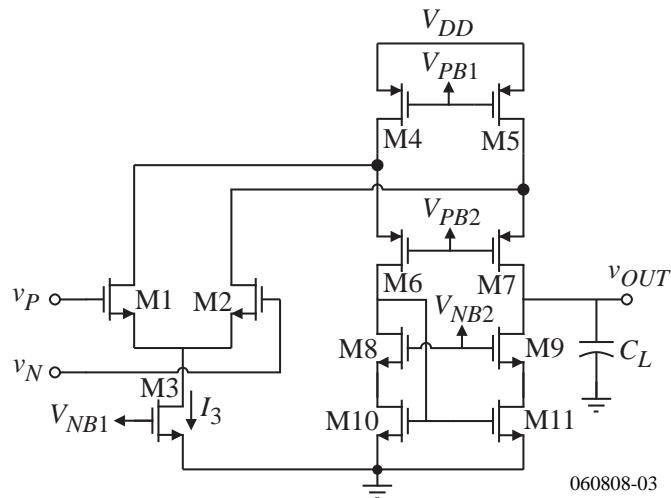
- Linear frequency response
- Slew rate response

Single-Stage Dominant Pole Comparator



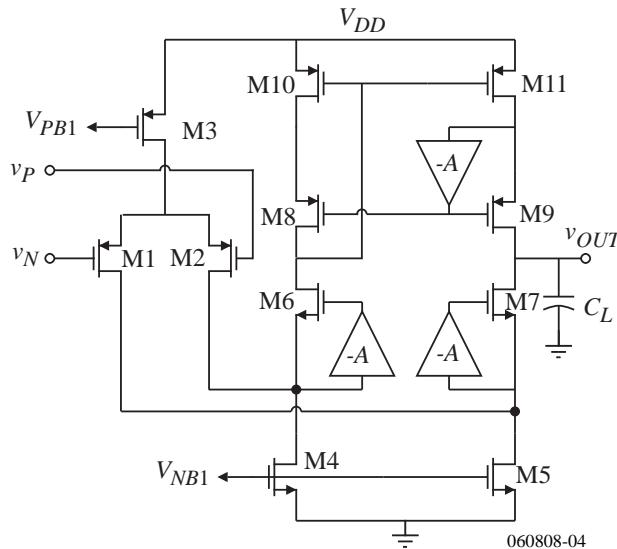
- Gain $\approx g_m^2 r_{ds}^2$
- Slew rate = I_5/C_L
- Dominant pole = $-1/(R_{out}C_L) = -1/(g_m r_{ds}^2 C_L)$

Folded-Cascode Comparator



- Gain $\approx g_m^2 r_{ds}^2$
- Slew rate = I_3/C_L
- Dominant pole = $-1/(R_{out}C_L) \approx -1/(g_m r_{ds}^2 C_L)$
- Slightly improved ICMR

Enhanced-Gain, Folded-Cascode Comparator

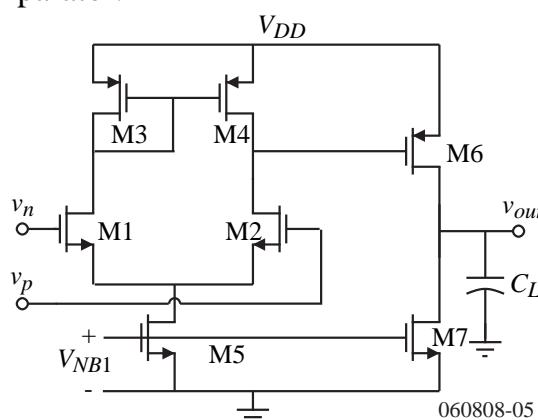


- Gain $\approx g_m 1 R_{out}$
- $R_{out} \approx [A r_{ds7} g_m 7 (r_{ds1} || r_{ds5})] || (A r_{ds9} g_m 9 r_{ds11})$
- Slew rate = I_3/C_L
- Dominant pole = $-1/(R_{out} C_L)$

TWO-POLE, OPEN-LOOP COMPARATORS

Two-Stage Comparator

The two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.



- Much faster linear response – the two poles of the comparator are typically much larger than the dominant pole of the self-compensated type of comparator.
- Be careful not to close the loop because the amplifier is uncompensated.
- Slew rate: $SR^- = \frac{I_7}{C_{II}}$ and $SR^+ = \frac{I_6 - I_7}{C_{II}}$

Linear Step Response of the Two-Stage Comparator

The step response of a circuit with two real poles ($p_1 \neq p_2$) is,

$$v_{out}(t) = A_v(0)V_{in} \left[1 + \frac{p_2 e^{tp_1}}{p_1 - p_2} - \frac{p_1 e^{tp_2}}{p_1 - p_2} \right]$$

Normalizing gives,

$$v_{out}'(t_n) = \frac{v_{out}(t)}{A_v(0)V_{in}} = 1 - \frac{m}{m-1}e^{-t_n} + \frac{1}{m-1}e^{-mt_n} \text{ where } m = \frac{p_2}{p_1} \neq 1 \text{ and } t_n = -tp_1$$

If $p_1 = p_2$ ($m = 1$), then $v_{out}'(t_n) = 1 - e^{tp_1} + tp_1 e^{tp_1} = 1 - e^{-t_n} - t_n e^{-t_n}$

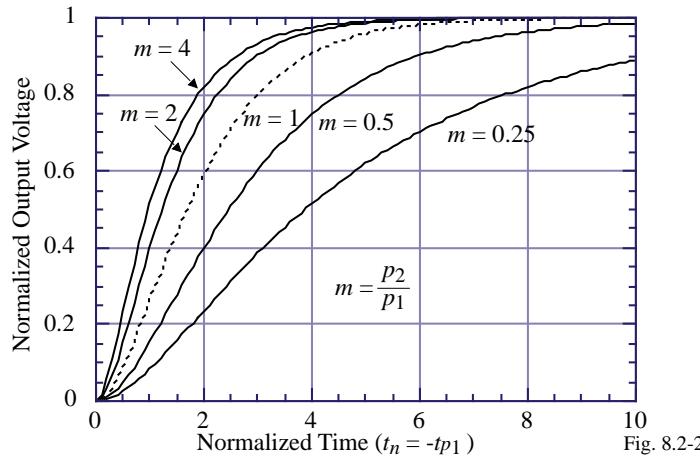


Fig. 8.2-2

Linear Step Response of the Two-Stage Comparator - Continued

The above results are valid as long as the slope of the linear response does not exceed the slew rate.

- Slope at $t = 0$ is zero
- Maximum slope occurs at ($m \neq 1$)

$$t_n(\max) = \frac{\ln(m)}{m-1}$$

and is

$$\frac{dv_{out}'(t_n(\max))}{dt_n} = \frac{m}{m-1} \left[\exp\left(\frac{-\ln(m)}{m-1}\right) - \exp\left(-m \frac{\ln(m)}{m-1}\right) \right]$$

- For the two-stage comparator using NMOS input transistors, the slew rate is

$$SR^- = \frac{I_7}{C_{II}}$$

$$SR^+ = \frac{I_6 - I_7}{C_{II}} = \frac{0.5\beta_6(V_{DD} - V_{G6(\min)} - |V_{TP}|)^2 - I_7}{C_{II}}$$

Example 310-2 - Step Response of Ex. 310-1

Find the maximum slope of Ex. 310-1 and the time it occurs if the magnitude of the input step is $v_{in}(\text{min})$. If the dc bias current in M7 is $100\mu\text{A}$, at what value of load capacitance, C_L would the transient response become slew limited? If the magnitude of the input step is $100v_{in}(\text{min})$, what is the new value of C_L at which slewing would occur?

Solution

The poles of the comparator were given in Ex. 310-1 as $p_1 = -6.75 \times 10^6$ rads/sec. and $p_2 = -1.71 \times 10^6$ rads/sec. This gives a value of $m = 0.253$. From the previous expressions, the maximum slope occurs at $t_n(\text{max}) = 1.84$ secs. Dividing by $|p_1|$ gives $t(\text{max}) = 0.272\mu\text{s}$. The slope of the transient response at this time is found as

$$\frac{dv_{out}'(t_n(\text{max}))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253 \cdot 1.84)] = 0.159 \text{ V/sec}$$

Multiplying the above by $|p_1|$ gives $dv_{out}'(t(\text{max}))/dt = 1.072\text{V}/\mu\text{s}$. If the slew rate is less than $1.072\text{V}/\mu\text{s}$, the transient response will experience slewing. Therefore, if $C_L \geq 100\mu\text{A}/1.072\text{V}/\mu\text{s}$ or 93.3pF , the comparator will slew.

If the input is $100v_{in}(\text{min})$, then we must unnormalize the output slope as follows.

$$\frac{dv_{out}'(t(\text{max}))}{dt} = \frac{v_{in}}{v_{in}(\text{min})} \frac{dv_{out}'(t(\text{max}))}{dt} = 100 \cdot 1.072\text{V}/\mu\text{s} = 107.2\text{V}/\mu\text{s}$$

Therefore, the comparator will slew with a load capacitance greater than 0.933pF .

Propagation Delay Time (Non-Slew)

To find t_p , we want to set $0.5(V_{OH}-V_{OL})$ equal to $v_{out}(t_n)$. However, $v_{out}(t_n)$ given as

$$v_{out}(t_n) = A_v(0)V_{in} \left[1 - \frac{m}{m-1} e^{-t_n} + \frac{1}{m-1} e^{-mt_n} \right]$$

can't be easily solved so approximate the step response as a power series to get

$$v_{out}(t_n) \approx A_v(0)V_{in} \left[1 - \frac{m}{m-1} \left(1 - t_n + \frac{t_n^2}{2} + \dots \right) + \frac{1}{m-1} \left(1 - mt_n + \frac{m^2 t_n^2}{2} + \dots \right) \right] \approx \frac{mt_n^2 A_v(0) V_{in}}{2}$$

Therefore, set $v_{out}(t_n) = 0.5(V_{OH}-V_{OL})$

$$\frac{V_{OH}-V_{OL}}{2} \approx \frac{mt_{pn}^2 A_v(0) V_{in}}{2}$$

or

$$t_{pn} \approx \sqrt{\frac{V_{OH}-V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\text{min})}{mV_{in}}} = \frac{1}{\sqrt{mk}}$$

This approximation is particularly good for large values of k .

Example 310-3 - Propagation Delay Time of a Two-Pole Comparator (Non-Slew)

Find the propagation time delay of Ex. 310-1 if $V_{in} = 10\text{mV}$, 100mV and 1V .

Solution

From Ex. 310-1 we know that $V_{in}(\min) = 0.611\text{mV}$ and $m = 0.253$. For $V_{in} = 10\text{mV}$, $k = 16.366$ which gives $t_{pn} \approx 0.491$. The propagation time delay is equal to $0.491/6.75 \times 10^6$ or 72.9nS . This corresponds well with the figure shown where the normalized propagation time delay is the time at which the amplitude is $1/2k$ or 0.031 which corresponds to t_{pn} of approximately 0.5. Similarly, for $V_{in} = 100\text{mV}$ and 1V we get a propagation time delay of 23ns and 7.3ns , respectively.

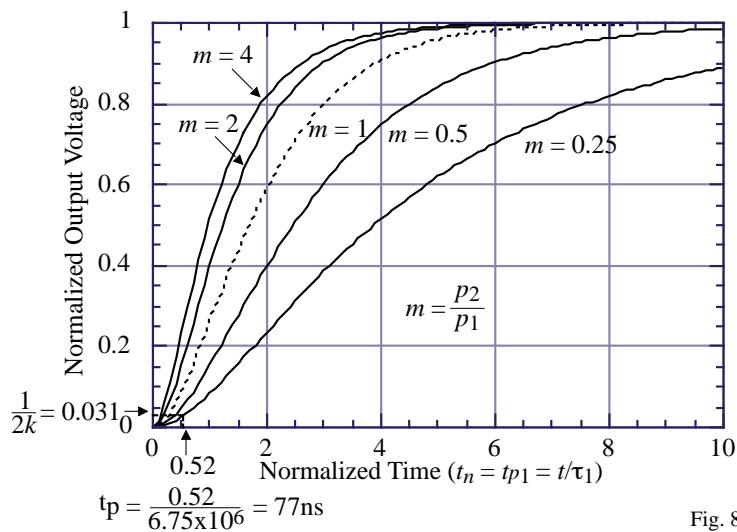


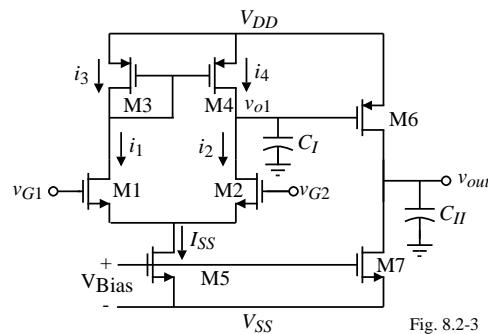
Fig. 8.2-2A

Initial Operating States for the Two-Stage, Open-Loop Comparator

What are the initial operating states for the two-stage, open-loop comparator? The following table summarizes the results for the two-stage, open-loop comparator shown.

Conditions	Initial State of v_{o1}	Initial State of v_{out}
$v_{G1} > V_{G2}, i_1 < I_{SS}$ and $i_2 > 0$	$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G1} \gg V_{G2}, i_1 = I_{SS}$ and $i_2 = 0$	V_{DD}	V_{SS}
$v_{G1} < V_{G2}, i_1 > 0$ and $i_2 < I_{SS}$	$v_{o1} = V_{G2} - V_{GS2,\text{act}}(I_{SS}/2), \approx V_{SS}$ if M5 act.	V_{OH} see equation below tabl
$v_{G1} \ll V_{G2}, i_1 > 0$ and $i_2 < I_{SS}$	V_{SS}	V_{OH} see equation below tabl
$v_{G2} > V_{G1}, i_1 > 0$ and $i_2 < I_{SS}$	$V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(\text{sat})$	V_{OH} see equation below tabl
$v_{G2} \gg V_{G1}, i_1 > 0$ and $i_2 < I_{SS}$	$V_{G1} - V_{GS1}(I_{SS}/2), \approx V_{SS}$ if M5 active	V_{OH} see equation below tabl
$v_{G2} < V_{G1}, i_1 < I_{SS}$ and $i_2 > 0$	$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$v_{G2} \ll V_{G1}, i_1 = I_{SS}$ and $i_2 = 0$	V_{DD}	V_{SS}

$$V_{OH} = V_{DD} - (V_{DD} - V_{G6}(\min) - |V_{TP}|) \\ \times \left[1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD} - V_{G6}(\min) - |V_{TP}|)^2}} \right]$$

Fig. 8.2-3
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Trip Point of an Inverter

In order to determine the propagation delay time, it is necessary to know when the second stage of the two-stage comparator begins to “turn on”.

Second stage:

Trip point:

Assume that M6 and M7 are saturated. (We know that the steepest slope occurs for this condition.)

Equate i_6 to i_7 and solve for v_{in} which becomes the trip point.

$$\therefore v_{in} = V_{TRP} = V_{DD} - |V_{TP}| - \sqrt{\frac{K_N(W_7/L_7)}{K_P(W_6/L_6)}} (V_{Bias} - V_{SS} - V_{TN})$$

Example:

If $W_7/L_7 = W_6/L_6$, $V_{DD} = 2.5V$, $V_{SS} = -2.5V$, and $V_{Bias} = 0V$ the trip point for the circuit above is

$$V_{TRP} = 2.5 - 0.7 - \sqrt{110/50} (0 + 2.5 - 0.7) = -0.870V$$

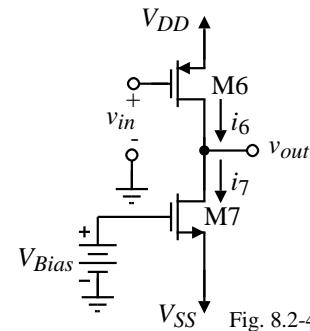


Fig. 8.2-4

Propagation Delay Time of a Slew, Two-Stage, Open-Loop Comparator

Previously we calculated the propagation delay time for a nonslewing comparator.

If the comparator slews, then the propagation delay time is found from

$$i_i = C_i \frac{dv_i}{dt_i} = C_i \frac{\Delta v_i}{\Delta t_i}$$

where

C_i is the capacitance to ground at the output of the i -th stage

The propagation delay time of the i -th stage is,

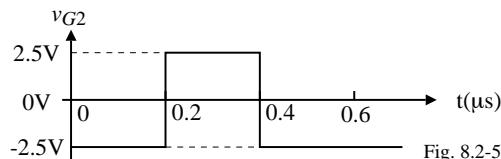
$$t_i = \Delta t_i = C_i \frac{\Delta V_i}{I_i}$$

The propagation delay time is found by summing the delays of each stage.

$$t_p = t_1 + t_2 + t_3 + \dots$$

Example 310-4 - Propagation Time Delay of a Two-Stage, Open-Loop Comparator

For the two-stage comparator shown assume that $C_I = 0.2\text{pF}$ and $C_{II} = 5\text{pF}$. Also, assume that $v_{G1} = 0\text{V}$ and that v_{G2} has the waveform shown. If the input voltage is large enough to cause slew to dominate, find the propagation time delay of the rising and falling output of the comparator and give the propagation time delay of the comparator.



- Fig. 8.2-5

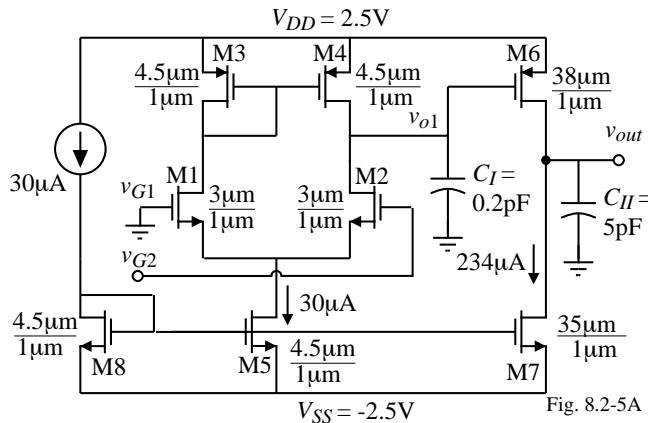


Fig. 8.2-5A

Solution

- 1.) Total delay = sum of the first and second stage delays, t_1 and t_2
 - 2.) First, consider the change of v_{G2} from -2.5V to 2.5V at $0.2\mu s$.

The last row of table on Slide 310-28 gives $v_{o1} = +2.5V$ and $v_{out} = -2.5V$

- 3.) t_{f1} , requires C_I , ΔV_{o1} , and I_5 . $C_I = 0.2\text{pF}$, $I_5 = 30\mu\text{A}$ and ΔV_1 can be calculated by finding the trip point of the output stage.

Example 310-4 - Continued

- 4.) The trip point of the output stage by setting the current of M6 when saturated equal to $234\mu\text{A}$.

$$\frac{\beta_6}{2} (V_{SG6} - |V_{TP}|)^2 = 234 \mu\text{A} \rightarrow V_{SG6} = 0.7 + \sqrt{\frac{234 \cdot 2}{50 \cdot 38}} = 1.196 \text{V}$$

Therefore, the trip point of the second stage is $V_{TRP2} = 2.5 - 1.196 = 1.304V$

Therefore, $\Delta V_1 = 2.5V - 1.304V = V_{SG6} = 1.196V$. Thus the falling propagation time delay of the first stage is

$$t_{fo1} = 0.2 \text{ pF} \left(\frac{1.196 \text{ V}}{30 \mu \text{A}} \right) = 8 \text{ ns}$$

- 5.) The rising propagation time delay of the second stage requires C_{II} , ΔV_{out} , and I_6 . C_{II} is given as 5pF, $\Delta V_{out} = 2.5V$ (assuming the trip point of the circuit connected to the output of the comparator is 0V), and I_6 can be found as follows:

$$V_{G6}(\text{guess}) \approx 0.5[V_{G6}(I_6=234\mu\text{A}) + V_{G6}(\text{min})]$$

$$V_{G6(\min)} = V_{G1} - V_{GS1}(I_{SS}/2) + V_{DS2} \approx -V_{GS1}(I_{SS}/2) = -0.7 - \sqrt{\frac{2 \cdot 15}{110 \cdot 3}} = -1.00 \text{V}$$

$$V_{G6}(\text{guess}) \approx 0.5(1.304\text{V}-1.00\text{V}) = 0.152\text{V}$$

$$\text{Therefore } V_{SG6} = 2.348V \quad \text{and} \quad I_6 = \frac{\beta_6}{2} (V_{SG6} - |V_{TP}|)^2 = \frac{38.50}{2} (2.348 - 0.7)^2 = 2,580\mu\text{A}$$

Example 310-4 - Continued

6.) The rising propagation time delay for the output can expressed as

$$t_{rout} = 5\text{pF} \left(\frac{2.5\text{V}}{2580\mu\text{A}-234\mu\text{A}} \right) = 5.3 \text{ ns}$$

Thus the total propagation time delay of the rising output of the comparator is approximately 13.3 ns and most of this delay is attributable to the first stage.

7.) Next consider the change of v_{G2} from 2.5V to -2.5V at 0.4μs. We shall assume that v_{G2} has been at 2.5V long enough for the conditions of the table on Slide 310-28 to be valid. Therefore, $v_{o1} \approx V_{SS} = -2.5\text{V}$ and $v_{out} \approx V_{DD}$. The propagation time delays for the first and second stages are calculated as

$$t_{ro1} = 0.2\text{pF} \left(\frac{1.304\text{V}-(-1.00\text{V})}{30\mu\text{A}} \right) = 15.4 \text{ ns}$$

$$t_{fout} = 5\text{pF} \left(\frac{2.5\text{V}}{234\mu\text{A}} \right) = 53.42\text{ns}$$

8.) The total propagation time delay of the falling output is 68.82 ns. Taking the average of the rising and falling propagation time delays gives a propagation time delay for this two-stage, open-loop comparator of about 41.06ns.

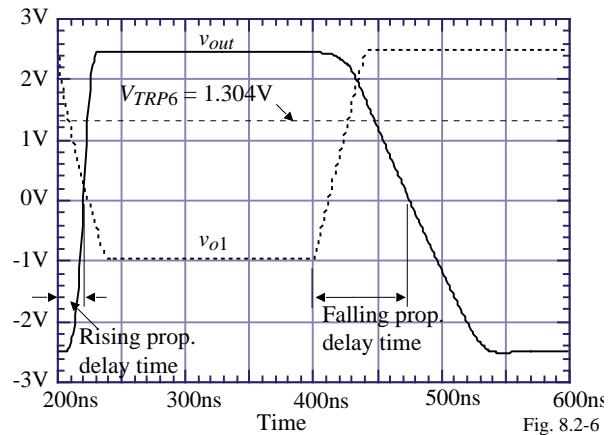


Fig. 8.2-6

SUMMARY

- The two-stage, open-loop comparator has two poles which should as large as possible
- The transient response of a two-stage, open-loop comparator will be limited by either the bandwidth or the slew rate
- It is important to know the initial states of a two-stage, open-loop comparator when finding the propagation delay time
- If the comparator is gainbandwidth limited then the poles should be as large as possible for minimum propagation delay time
- If the comparator is slew rate limited, then the current sinking and sourcing ability should be as large as possible

LECTURE 320 – IMPROVED OPEN-LOOP COMPARATORS AND LATCHES

LECTURE ORGANIZATION

Outline

- Autozeroing
- Hysteresis
- Simple Latches
- Summary

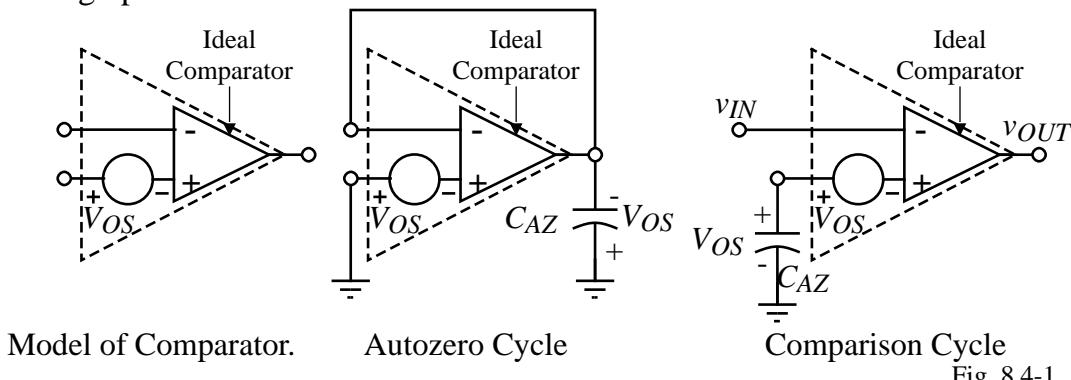
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 464-483

AUTOZEROING

Principle of Autozeroing

Use the comparator as an op amp to sample the dc input offset voltage and cancel the offset during operation.



Comments:

- The comparator must be stable in the unity-gain mode (self-compensating comparators are ideal, the two-stage comparator would require compensation to be switched in during the autozero cycle.)
- Complete offset cancellation is limited by charge injection

Differential Implementation of Autozeroed Comparators

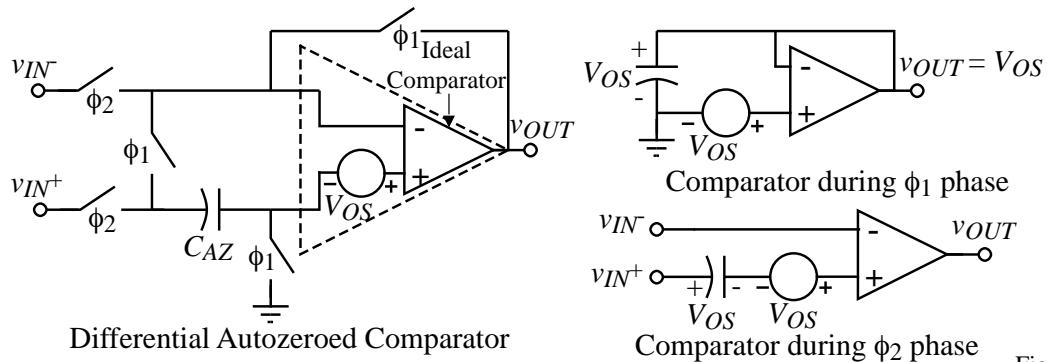


Fig. 8.4-2

Single-Ended Autozeroed Comparators

Noninverting:

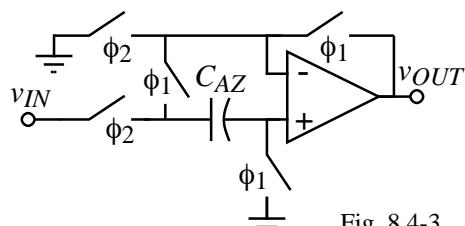


Fig. 8.4-3

Inverting:

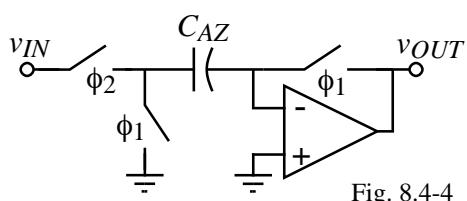


Fig. 8.4-4

Comment on autozeroing:

Need to be careful about noise that gets sampled onto the autozeroing capacitor and is present on the comparison phase of the process.

HYSTERESIS

Influence of Input Noise on the Comparator

Comparator without hysteresis:

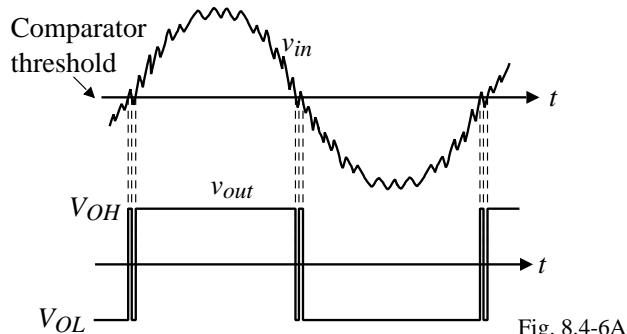


Fig. 8.4-6A

Comparator with hysteresis:

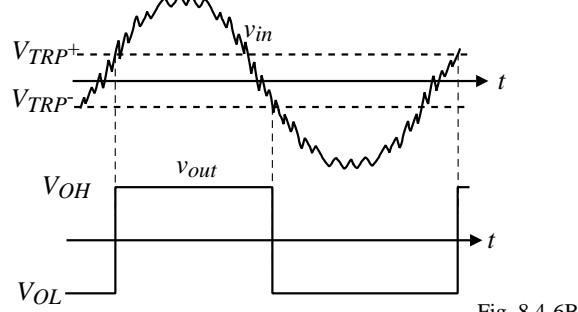


Fig. 8.4-6B

Use of Hysteresis for Comparators in a Noisy Environment

Transfer curve of a comparator with hysteresis:

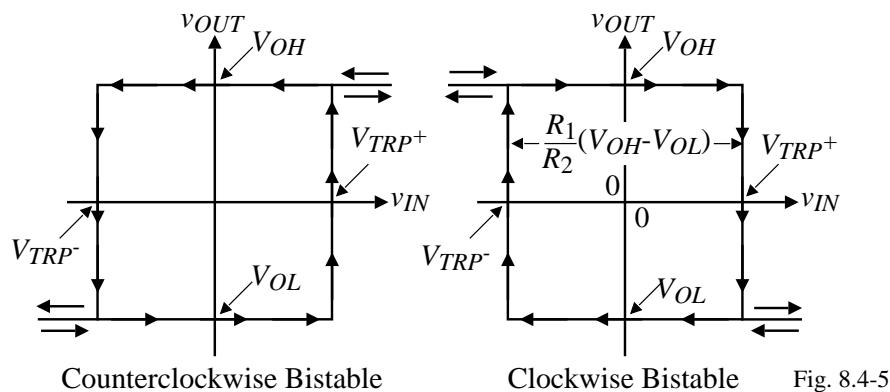


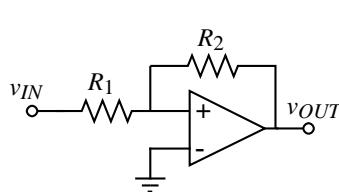
Fig. 8.4-5

Hysteresis is achieved by the use of positive feedback

- Externally
- Internally

Noninverting Comparator using External Positive Feedback

Circuit:



Upper Trip Point:

Fig. 8.4-7

Assume that $v_{OUT} = V_{OL}$, the upper trip point occurs when,

$$0 = \left(\frac{R_1}{R_1+R_2} \right) V_{OL} + \left(\frac{R_2}{R_1+R_2} \right) V_{TRP^+} \rightarrow V_{TRP^+} = -\frac{R_1}{R_2} V_{OL}$$

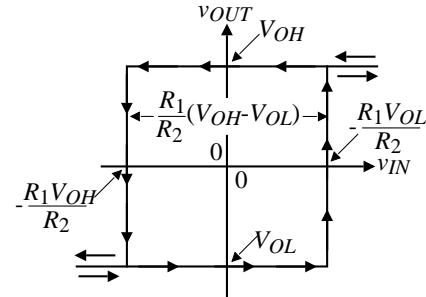
Lower Trip Point:

Assume that $v_{OUT} = V_{OH}$, the lower trip point occurs when,

$$0 = \left(\frac{R_1}{R_1+R_2} \right) V_{OH} + \left(\frac{R_2}{R_1+R_2} \right) V_{TRP^-} \rightarrow V_{TRP^-} = -\frac{R_1}{R_2} V_{OH}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP^+} - V_{TRP^-} = \left(\frac{R_1}{R_2} \right) (V_{OH} - V_{OL})$$



Inverting Comparator using External Positive Feedback

Circuit:

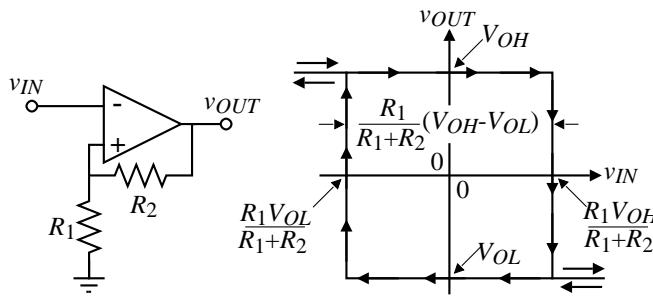


Fig. 8.4-8

Upper Trip Point:

$$v_{IN} = V_{TRP^+} = \left(\frac{R_1}{R_1+R_2} \right) V_{OH}$$

Lower Trip Point:

$$v_{IN} = V_{TRP^-} = \left(\frac{R_1}{R_1+R_2} \right) V_{OL}$$

Width of the bistable characteristic:

$$\Delta V_{in} = V_{TRP^+} - V_{TRP^-} = \left(\frac{R_1}{R_1+R_2} \right) (V_{OH} - V_{OL})$$

Horizontal Shifting of the CCW Bistable Characteristic

Circuit:

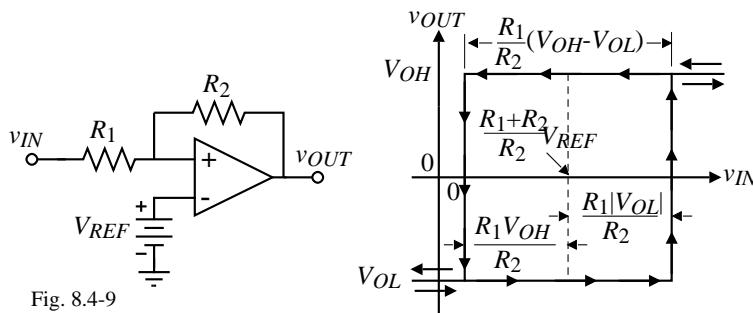


Fig. 8.4-9

Upper Trip Point:

$$V_{REF} = \left(\frac{R_1}{R_1+R_2} \right) V_{OL} + \left(\frac{R_2}{R_1+R_2} \right) V_{TRP^+} \rightarrow V_{TRP^+} = \left(\frac{R_1+R_2}{R_2} \right) V_{REF} - \frac{R_1}{R_2} V_{OL}$$

Lower Trip Point:

$$V_{REF} = \left(\frac{R_1}{R_1+R_2} \right) V_{OH} + \left(\frac{R_2}{R_1+R_2} \right) V_{TRP^-} \rightarrow V_{TRP^-} = \left(\frac{R_1+R_2}{R_2} \right) V_{REF} - \frac{R_1}{R_2} V_{OH}$$

Shifting Factor:

$$\pm \frac{R_2}{R_1+R_2} V_{REF}$$

Horizontal Shifting of the CW Bistable Characteristic

Circuit:

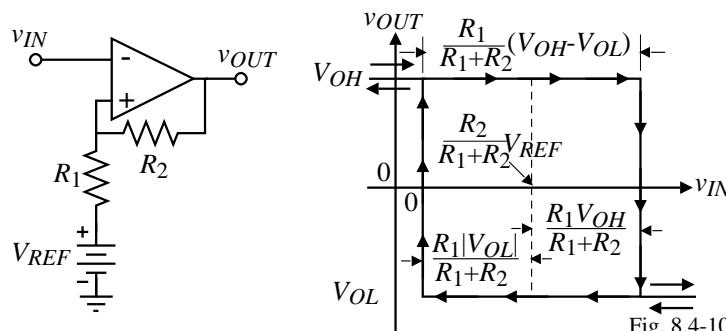


Fig. 8.4-10

Upper Trip Point:

$$v_{IN} = V_{TRP^+} = \left(\frac{R_1}{R_1+R_2} \right) V_{OH} + \left(\frac{R_2}{R_1+R_2} \right) V_{REF}$$

Lower Trip Point:

$$v_{IN} = V_{TRP^-} = \left(\frac{R_1}{R_1+R_2} \right) V_{OL} + \left(\frac{R_2}{R_1+R_2} \right) V_{REF}$$

Shifting Factor:

$$\pm \frac{R_2}{R_1+R_2} V_{REF}$$

Example 320-1 Design of an Inverting Comparator with Hysteresis

Use the inverting bistable to design a high-gain, open-loop comparator having an upper trip point of 1V and a lower trip point of 0V if $V_{OH} = 2V$ and $V_{OL} = -2V$.

Solution

Putting the values of this example into the above relationships gives

$$1 = \left(\frac{R_1}{R_1+R_2} \right) 2 + \left(\frac{R_2}{R_1+R_2} \right) V_{REF}$$

and

$$0 = \left(\frac{R_1}{R_1+R_2} \right) (-2) + \left(\frac{R_2}{R_1+R_2} \right) V_{REF}$$

Solving these two equations gives $3R_1 = R_2$ and $V_{REF} = (2/3)V$.

Hysteresis using Internal Positive Feedback

Simple comparator with internal positive feedback:

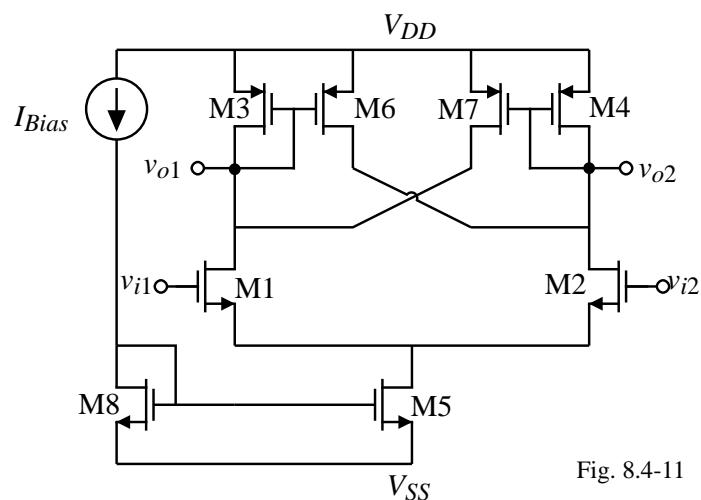


Fig. 8.4-11

Internal Positive Feedback - Upper Trip Point

Assume that the gate of M1 is on ground and the input to M2 is much smaller than zero. The resulting circuit is:

M1 on, M2 off \rightarrow M3 on, M6 on (active), M4 and M7 off.

$\therefore v_{o2}$ is high.

M6 wants to source the current $i_6 = \frac{W_6/L_6}{W_3/L_3} i_1$

As v_{in} begins to increase towards the trip point, the current flow through M2 increases. When $i_2 = i_6$, the upper trip point will occur.

$$\therefore i_5 = i_1 + i_2 = i_3 + i_6 = i_3 + \left[\frac{W_6/L_6}{W_3/L_3} \right] i_3 = i_3 \left[1 + \frac{W_6/L_6}{W_3/L_3} \right] \rightarrow i_1 = i_3 = \frac{i_5}{1 + [(W_6/L_6)/(W_3/L_3)]}$$

Also, $i_2 = i_5 - i_1 = i_5 - i_3$

Knowing i_1 and i_2 allows the calculation of v_{GS1} and v_{GS2} which gives

$$V_{TRP^+} = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} - V_{T1}$$

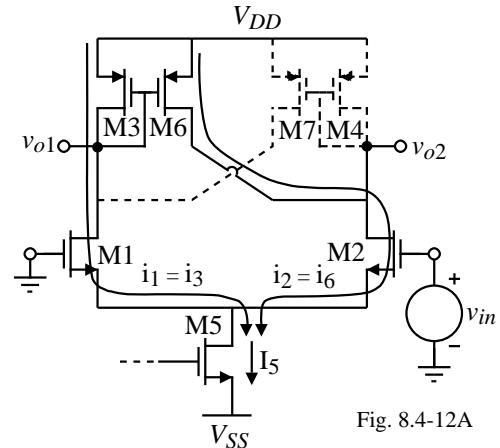


Fig. 8.4-12A

Internal Positive Feedback - Lower Trip Point

Assume that the gate of M1 is on ground and the input to M2 is much greater than zero. The resulting circuit is:

M2 on, M1 off \rightarrow M4 and M7 on, M3 and M6 off.

$\therefore v_{o1}$ is high.

M7 wants to source the current $i_7 = \frac{W_7/L_7}{W_4/L_4} i_2$

As v_{in} begins to decrease towards the trip point, the current flow through M1 increases. When $i_1 = i_7$, the lower trip point will occur.

$$\therefore i_5 = i_1 + i_2 = i_7 + i_4 = \left[\frac{W_7/L_7}{W_4/L_4} \right] i_4 + i_4 = i_4 \left[1 + \frac{W_7/L_7}{W_4/L_4} \right] \rightarrow i_2 = i_4 = \frac{i_5}{1 + [(W_7/L_7)/(W_4/L_4)]}$$

Also, $i_1 = i_5 - i_2 = i_5 - i_4$

Knowing i_1 and i_2 allows the calculation of v_{GS1} and v_{GS2} which gives

$$V_{TRP^-} = v_{GS2} - v_{GS1} = \sqrt{\frac{2i_2}{\beta_2}} + V_{T2} - \sqrt{\frac{2i_1}{\beta_1}} - V_{T1}$$

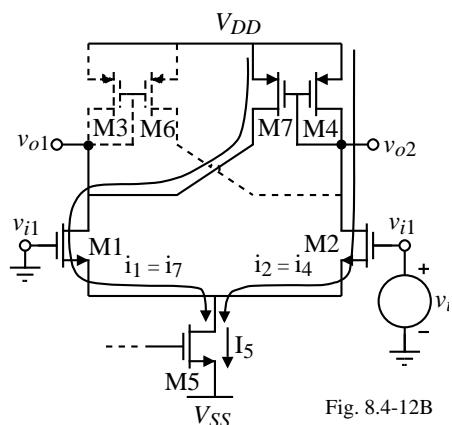


Fig. 8.4-12B

Example 320-2 - Calculation of Trip Voltages for a Comparator with Hysteresis

Consider the circuit shown. If $K_N' = 110\mu A/V^2$, $K_P' = 50\mu A/V^2$, and $V_{TN} = |V_{TP}| = 0.7V$, calculate the positive and negative threshold points if the device lengths are all $1 \mu m$ and the widths are given as: $W_1 = W_2 = W_6 = W_7 = 10 \mu m$ and $W_3 = W_4 = 2 \mu m$. The gate of M1 is tied to ground and the input is the gate of M2. The current, $i_5 = 20 \mu A$

Solution

To calculate the positive trip point, assume that the input has been negative and is heading positive.

$$i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 = (5/1)(i_3) \rightarrow i_3 = \frac{i_5}{1 + [(W/L)_6/(W/L)_3]} = i_1 = \frac{20 \mu A}{1 + 5} = 3.33 \mu A$$

$$i_2 = i_5 - i_1 = 20 - 3.33 = 16.67 \mu A \rightarrow v_{GS1} = \left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1} = \left(\frac{2 \cdot 3.33}{(5)110}\right)^{1/2} + 0.7 = 0.81V$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} = \left(\frac{2 \cdot 16.67}{(5)110}\right)^{1/2} + 0.7 = 0.946V$$

$$\therefore V_{TRP+} \cong v_{GS2} - v_{GS1} = 0.946 - 0.810 = 0.136V$$

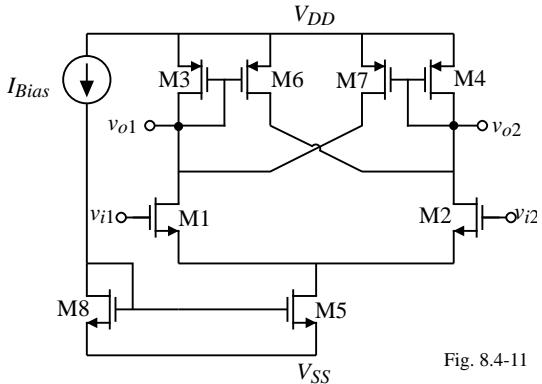


Fig. 8.4-11

Example 320-2 - Continued

Determining the negative trip point, similar analysis yields

$$i_4 = 3.33 \mu A$$

$$i_1 = 16.67 \mu A$$

$$v_{GS2} = 0.81V$$

$$v_{GS1} = 0.946V$$

$$V_{TRP-} \cong v_{GS2} - v_{GS1} = 0.81 - 0.946 = -0.136V$$

PSPICE simulation results of this circuit are shown below.

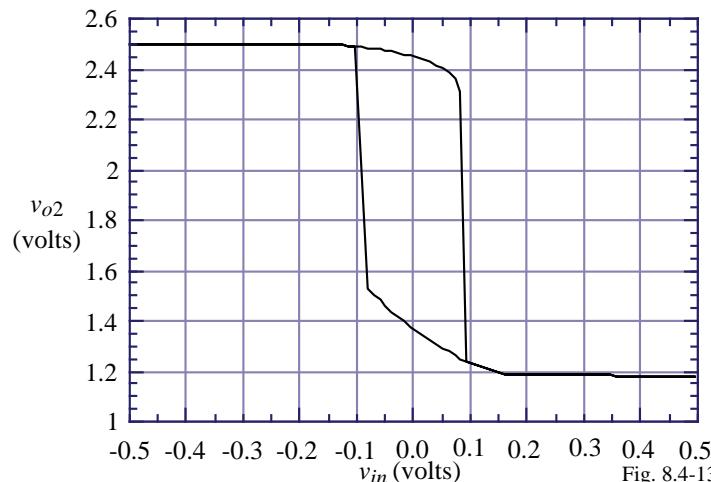


Fig. 8.4-13

Complete Comparator with Internal Hysteresis

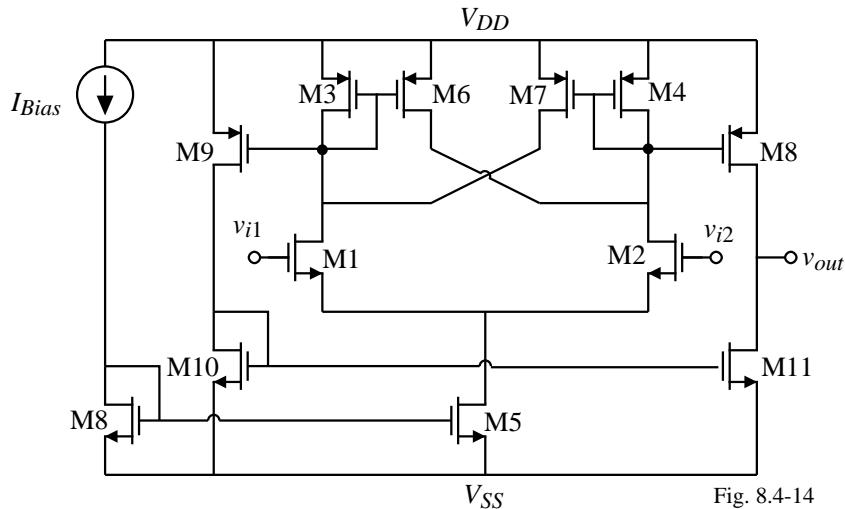
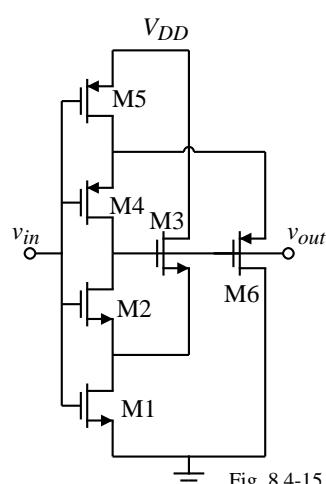


Fig. 8.4-14

Schmitt Trigger

The Schmitt trigger is a circuit that has better defined switching points.

Consider the following circuit:



How does this circuit work?

Assume the input voltage, v_{in} , is low and the output voltage, v_{out} , is high. M3, M4 and M5 are on and M1, M2 and M6 are off.

When v_{in} is increased from zero, M2 starts to turn on causing M3 to start turning off. Positive feedback causes M2 to turn on further and eventually both M1 and M2 are on and the output is at zero.

The upper switching point, V_{TRP^+} is found as follows:

When v_{in} is low, the voltage at the source of M2 (M3) is

$$v_{S2} = V_{DD} - V_{TN3}$$

$$V_{TRP^+} = v_{in} \text{ when M2 turns on given as } V_{TRP^+} = V_{TN2} + v_{S2}$$

V_{TRP^+} occurs when the input voltage causes the currents in M3 and M1 to be equal.

Schmitt Trigger – Continued

Thus, $i_{D1} = \beta_1(V_{TRP^+} - V_{TN1})^2 = \beta_3(V_{DD} - v_{S2} - V_{TN3})^2 = i_{D3}$
which can be written as, assuming that $V_{TN2} = V_{TN3}$,

$$\beta_1(V_{TRP^+} - V_{TN1})^2 = \beta_3(V_{DD} - V_{TRP^+})^2 \Rightarrow V_{TRP^+} = \frac{V_{TN1} + \sqrt{\beta_3/\beta_1} V_{DD}}{1 + \sqrt{\beta_3/\beta_1}}$$

The switching point, V_{TRP^-} is found in a similar manner and is:

$$\beta_5(V_{DD} - V_{TRP^-} - V_{TP5})^2 = \beta_6(V_{TRP^-})^2 \Rightarrow V_{TRP^-} = \frac{\sqrt{\beta_5/\beta_6} (V_{DD} - V_{TP5})}{1 + \sqrt{\beta_5/\beta_6}}$$

The bistable characteristic is,

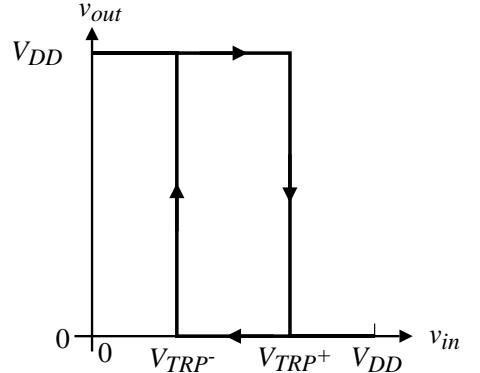


Fig. 8.4-16

SIMPLE LATCHES

Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. Latches can have a faster switching speed than the previous comparators.

NMOS and PMOS latch:

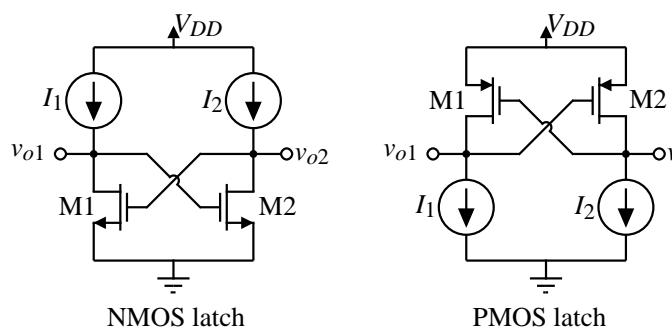


Fig. 8.5-3

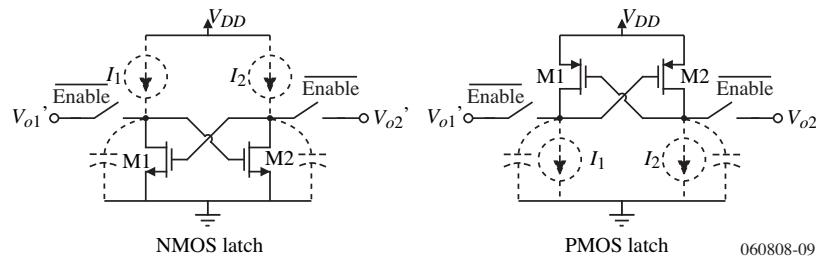
Operating Modes of the Latch

The latch has two modes of operation – enable or latch and $\overline{\text{Enable}}$ (enable_bar) or $\overline{\text{Latch}}$ (latch_bar).

1.) During the Enable_bar, the latch is turned off (currents are removed) and the unknown inputs are applied to it. The parasitic capacitance at the latch nodes hold the unknown voltage.

2.) During Enable, the latch is turned on, and the positive feedback acts on the applied inputs and causes one side of the latch to go high and the other side to go low.

Enable_bar:



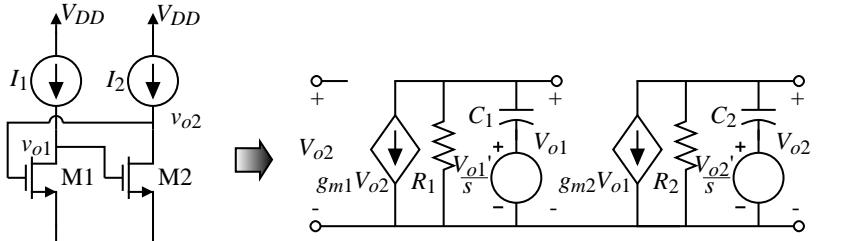
The inputs are initially applied to the outputs of the latch.

V_{o1}' = initial input applied to v_{o1}

Step Response of a Latch (Enable)

Circuit:

R_i and C_i are the resistance and capacitance seen to ground from the i -th transistor.



Nodal equations:

$$g_{m1}V_{o2} + G_1V_{o1} + sC_1\left(V_{o1} - \frac{V_{o1}'}{s}\right) = g_{m1}V_{o2} + G_1V_{o1} + sC_1V_{o1} - C_1V_{o1}' = 0$$

$$g_{m2}V_{o1} + G_2V_{o2} + sC_2\left(V_{o2} - \frac{V_{o2}'}{s}\right) = g_{m2}V_{o1} + G_2V_{o2} + sC_2V_{o2} - C_2V_{o2}' = 0$$

Solving for V_{o1} and V_{o2} gives,

$$V_{o1} = \frac{R_1C_1}{sR_1C_1+1} V_{o1}' - \frac{g_{m1}R_1}{sR_1C_1+1} V_{o2} = \frac{\tau_1}{s\tau_1+1} V_{o1}' - \frac{g_{m1}R_1}{s\tau_1+1} V_{o2}$$

$$V_{o2} = \frac{R_2C_2}{sR_2C_2+1} V_{o2}' - \frac{g_{m2}R_2}{sR_2C_2+1} V_{o1} = \frac{\tau_2}{s\tau_2+1} V_{o2}' - \frac{g_{m2}R_2}{s\tau_2+1} V_{o1}$$

Defining the output, ΔV_O , and input, ΔV_i , as

$$\Delta V_O = V_{o2} - V_{o1} \quad \text{and} \quad \Delta V_i = V_{o2}' - V_{o1}'$$

Step Response of the Latch - Continued

Solving for ΔV_o gives,

$$\Delta V_o = V_{o2} - V_{o1} = \frac{\tau}{s\tau+1} \Delta V_i + \frac{g_m R}{s\tau+1} \Delta V_o$$

or

$$\Delta V_o = \frac{\tau \Delta V_i}{s\tau+(1-g_m R)} = \frac{\frac{\tau \Delta V_i}{1-g_m R}}{\frac{s\tau}{1-g_m R} + 1} = \frac{\tau' \Delta V_i}{s\tau'+1}$$

where

$$\tau' = \frac{\tau}{1-g_m R}$$

Taking the inverse Laplace transform gives

$$\Delta V_o(t) = \Delta V_i e^{-t/\tau'} = \Delta V_i e^{-t(1-g_m R)/\tau} \approx e^{g_m R t / \tau} \Delta V_i, \quad \text{if } g_m R \gg 1.$$

Define the latch time constant as

$$\tau_L = |\tau'| \approx \frac{\tau}{g_m R} = \frac{C}{g_m} = \frac{0.67 WLC_{ox}}{\sqrt{2K'(W/L)I}} = 0.67 C_{ox} \sqrt{\frac{WL^3}{2K'I}}$$

if $C \approx C_{gs}$.

$$\therefore \Delta V_{out}(t) = e^{t/\tau_L} \Delta V_i$$

Step Response of a Latch - Continued

Normalize the output voltage by $(V_{OH} - V_{OL})$ to get

$$\frac{\Delta V_{out}(t)}{V_{OH} - V_{OL}} = e^{t/\tau_L} \frac{\Delta V_i}{V_{OH} - V_{OL}}$$

which is plotted as,

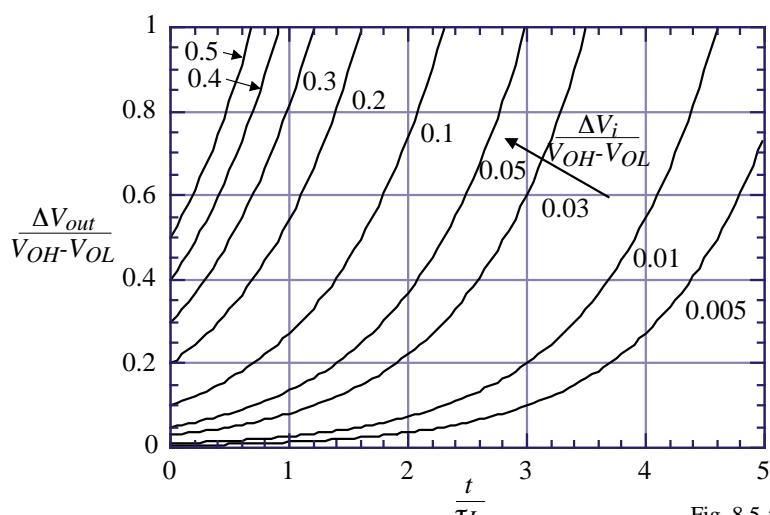


Fig. 8.5-5

The propagation delay time is

$$t_p = \tau_L \ln \left(\frac{V_{OH} - V_{OL}}{2\Delta V_i} \right)$$

Note that the larger the ΔV_i , the faster the response.

Example 320-3 - Time Domain Characteristics of a Latch.

Find the propagation time delay for the NMOS if the W/L of the latch transistors is $5\mu\text{m}/0.5\mu\text{m}$ and the latch dc current is $10\mu\text{A}$ when $\Delta V_i = 0.1(V_{OH} - V_{OL})$ and $\Delta V_i = 0.01(V_{OH} - V_{OL})$.

Solution

The transconductance of the latch transistors is

$$g_m = \sqrt{2 \cdot 120 \cdot 10 \cdot 10} = 155\mu\text{S}$$

The output conductance is $0.6\mu\text{S}$ which gives g_mR of 93V/V . Since g_mR is greater than 1, we can use the above results. Therefore the latch time constant is found as

$$\tau_L = 0.67 C_{ox} \sqrt{\frac{WL^3}{2KI}} = 0.67(60.6 \times 10^{-4}) \sqrt{\frac{(5 \cdot 0.5) \times 10^{-24}}{2 \cdot 120 \times 10^{-6} \cdot 10 \times 10^{-6}}} = 0.131\text{ns}$$

Since the propagation time delay is the time when the output is $0.5(V_{OH} - V_{OL})$, then using the above results or Fig. 8.5-5 we find for $\Delta V_i = 0.01(V_{OH} - V_{OL})$ that $t_p = 3.91\tau_L = 0.512\text{ns}$ and for $\Delta V_i = 0.1(V_{OH} - V_{OL})$ that $t_p = 1.61\tau_L = 0.211\text{ns}$.

Comparator using a Latch with a Built-In Reference[†]

How does it operate?

- 1.) Devices in shaded region operate in the triode region.
- 2.) When the latch/reset goes high, the upper cross-coupled inverter-latch regenerates. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances.

$$\frac{1}{R_1} = K_N \left[\frac{W_1}{L} (v_{in}^+ - V_T) + \frac{W_2}{L} (V_{REF}^- - V_T) \right]$$

and

$$\frac{1}{R_2} = K_N \left[\frac{W_1}{L} (v_{in}^- - V_T) + \frac{W_2}{L} (V_{REF}^+ - V_T) \right]$$

- 3.) The input voltage which causes $R_1 = R_2$ is $v_{in}(\text{threshold}) = (W_2/W_1)V_{REF}$
- $W_2/W_1 = 1/4$ generates a threshold of $\pm 0.25V_{REF}$.

Performance → 20Ms/s & $200\mu\text{W}$

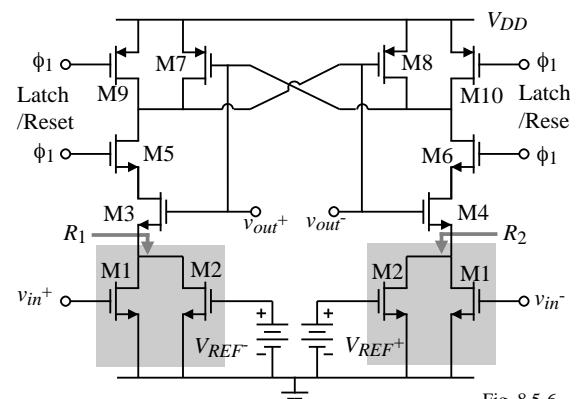


Fig. 8.5-6

[†] T.B. Cho and P.R. Gray, "A 10b, 20Msamples/s, 35mW pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

Simple, Low Power Latched Comparator[†]

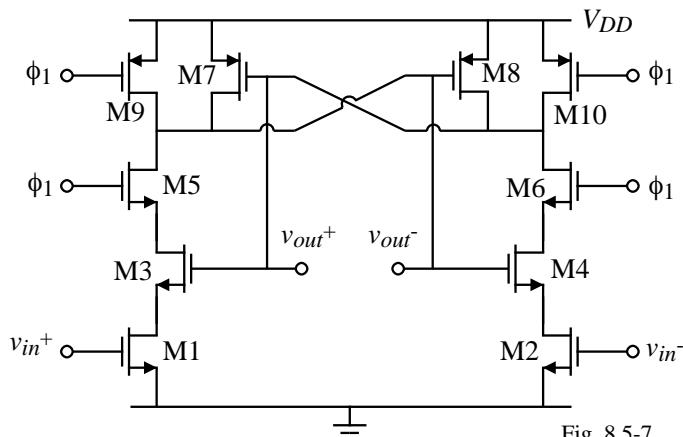


Fig. 8.5-7

Dissipated $50\mu\text{W}$ when clocked at 2MHz.

Self-referenced

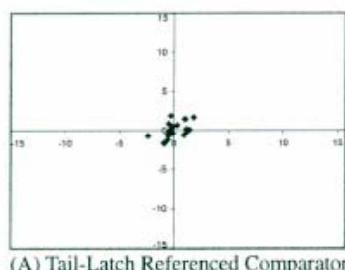
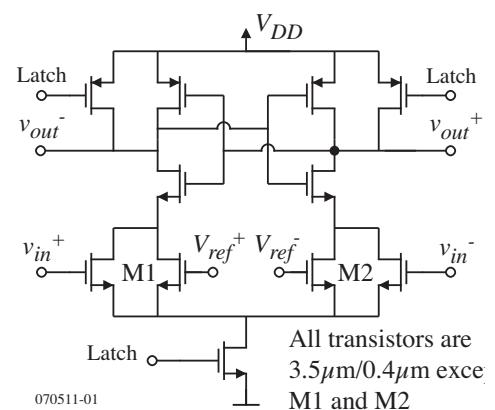
[†] A. Coban, “1.5V, 1mW, 98-dB Delta-Sigma ADC”, Ph.D. dissertation, School of ECE, Georgia Tech, Atlanta, GA 30332-0250.
CMOS Analog Circuit Design

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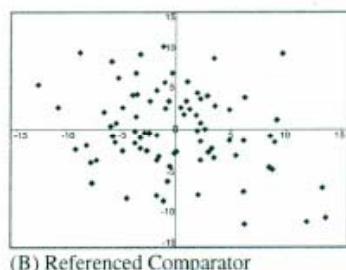
Tail-Referenced Latch

The previous two latches experience poor input offset voltage characteristics because the input devices are working in the linear region during the latch phase. The latch below keeps the input devices in the saturation region. The resulting larger gain of the input devices reduces the input offset voltage as shown.

The input offset voltage of the tail referenced latch is compared between two latches with the referenced latch for 100 samples. The x-axis is the deviation from the mean of the first latch and the y-axis is the deviation of the mean of the second latch.



(A) Tail-Latch Referenced Comparator



(B) Referenced Comparator

CMOS Latch

Circuit:

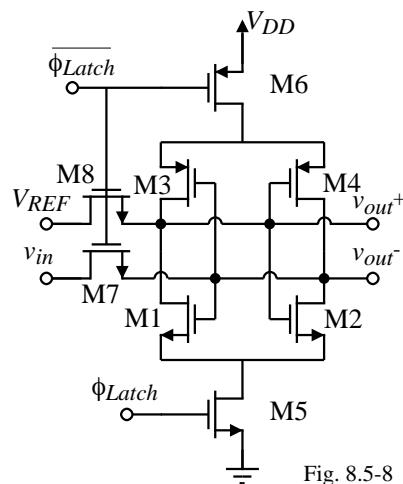


Fig. 8.5-8

Input offset voltage distribution:

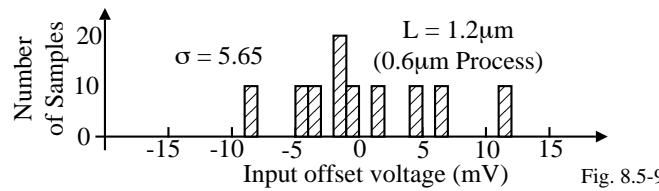
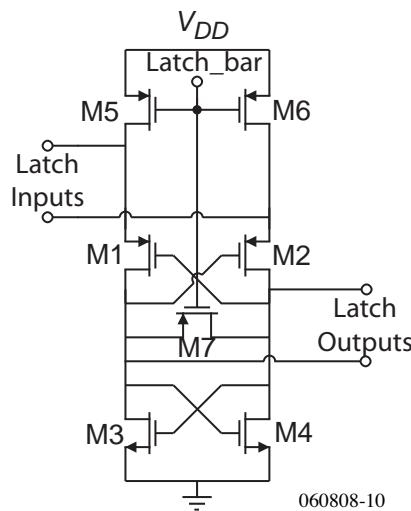


Fig. 8.5-9

CMOS Latch with Different Inputs and Outputs



When Latch_bar is high, M5, M6 and M7 are off and the latch is disabled and the outputs are shorted together.

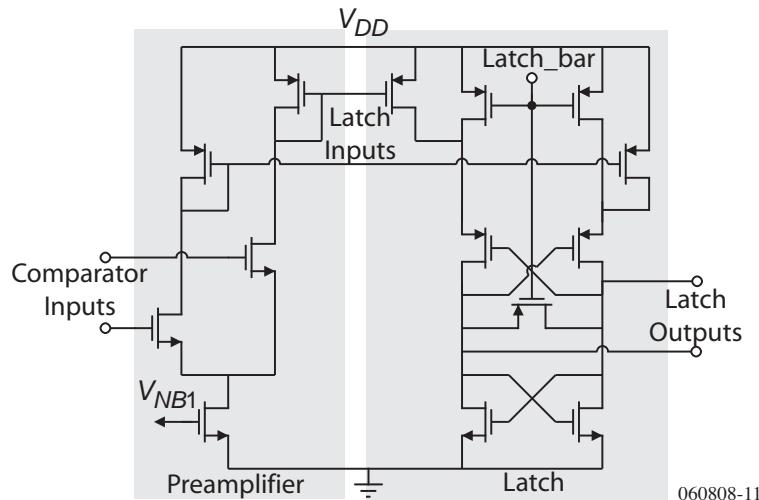
When Latch_bar is low, the input voltages stored at the sources of M1 and M2 will cause one of the latch outputs to be high and the other to be low.

The source of M1 and M2 that is higher will have a larger source-gate voltage resulting in a larger transconductance and more gain than the other transistor.

Metastability

Metastability is the condition where the latch cannot make a decision in the time allocated. Normally due to the fact that the input is small (within the input resolution range).

Metastability can be improved (reduced) by increasing the gain of the comparator by preceding it with an amplifier to keep the signal input to the latch as large as possible under all conditions. The preamplifier also reduced the input offset voltage.



060808-11

SUMMARY

- Discrete-time comparators must work with clocks
- Switched capacitor comparators use op amps to transfer charge and autozero
- Regenerative comparators (latches) use positive feedback
- The propagation delay of the regenerative comparator is slow at the beginning and speeds up rapidly as time increases
- The highest speed comparators will use a combination of open-loop comparators and latches

LECTURE 330 – HIGH SPEED COMPARATORS

LECTURE ORGANIZATION

Outline

- Speed limitations of comparators
- High speed comparators
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

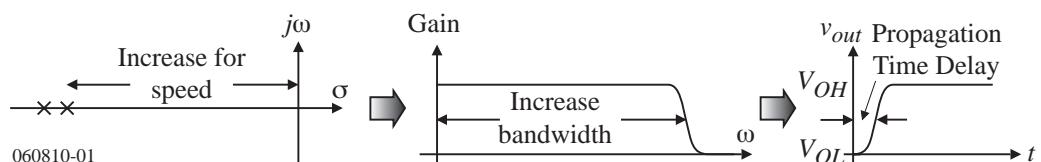
Pages 461-464 and 483-487

SPEED LIMITATIONS OF COMPARATORS

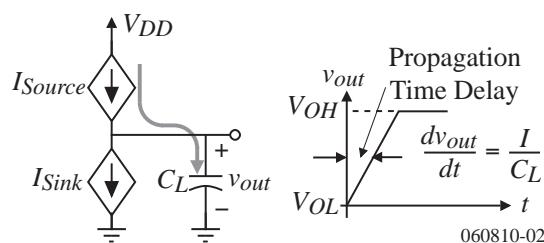
Speed Limitations of Comparators

The speed of a comparator is limited by either:

- Linear response – response time is inversely proportional to the magnitude of poles

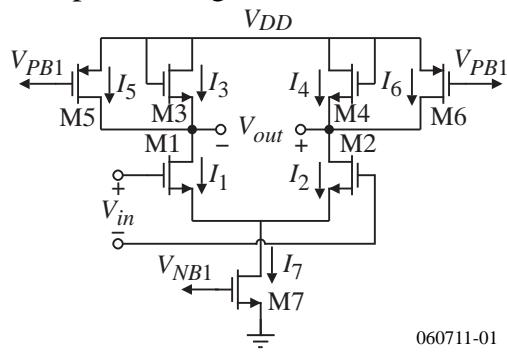


- Slew rate – delay is proportional to capacitance and inversely proportional to current sinking or sourcing capability



Maximizing the Linear Response

Consider the amplifier of Example 270-3 given below:



One stage of this amplifier had a gain of 10 and a dominant pole at 551MHz. The response of this amplifier to a step input is

$$V_{out}(t) = 10V_{in} (1 - e^{-p_1 t})$$

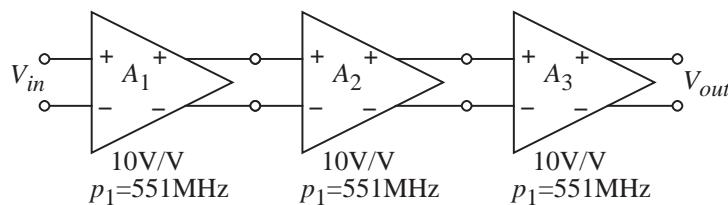
If the output signal swing is 1V and the step is 0.1V, the propagation time delay is,

$$V_{in}(\text{min}) = 1/10 = 0.1\text{V} \Rightarrow k = 1$$

$$\therefore t_p = \frac{1}{p_1} \ln \left[\frac{2k}{2k-1} \right] = \frac{1}{2\pi \cdot 551 \times 10^6} \ln \left[\frac{2}{2-1} \right] = 0.20 \text{ ns}$$

Trading Speed for Sensitivity (Gain)

In the previous example, the gain was too small for good sensitivity. To enhance the sensitivity, cascade three of the gain of 10 stages. The result is,



The frequency response of this amplifier is,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1000}{(1 + s/p_1)^3}$$

The step response of this amplifier is

$$v_{out}(t) = \frac{A_o}{2} V_{in} p_1^3 t^2 e^{-p_1 t} \approx \frac{A_o}{2} V_{in} p_1^3 t^2 [1 - p_1 t + p_1^2 t^2 - \dots] \approx \frac{A_o}{2} V_{in} p_1^3 t^2 \quad \text{if } p_1 t < 1$$

The propagation delay time is

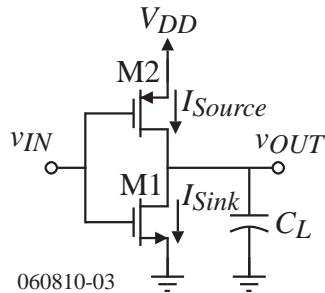
$$t_p^2 = \frac{V_{OH} - V_{OL}}{A_o} \frac{1}{V_{in} p_1^3} = \frac{1}{k p_1^3} \quad \rightarrow \quad t_p = 0.0049 \text{ ps if } k = 1$$

The speed of the amplifier will be limited by the slew capability!

Maximizing Speed for Slew Rate Limitation

The key is to make the sourcing/sinking current large and the capacitance small.

Best possible sinking/sourcing circuit in CMOS is:



Assuming a W/L ratio of 42 for M1 and 200 for M2, if the input can swing to V_{DD} ($=2.5V$) and ground, the sourcing and sinking currents are:

$$I_{Sourcing} = \frac{K_p' W}{2L} (V_{DD} - |V_{TP}|)^2 = \frac{25 \cdot 200}{2} (2.5V - 0.5)^2 \mu\text{A} = 10.0 \text{ mA}$$

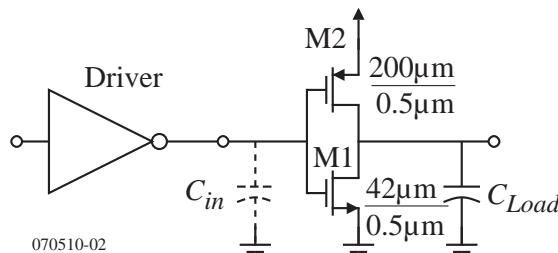
$$I_{Sinking} = \frac{K_n' W}{2L} (V_{DD} - V_{TN})^2 = \frac{120 \cdot 42}{2} (2.5V - 0.5)^2 \mu\text{A} = 10.1 \text{ mA}$$

If larger currents are required, cascaded stages can be used to optimize the delay versus the current output.

Driver Delay of a Push-Pull Inverter

If too much current is required, the device sizes become large and the driver delay increases. For the previous example, the input capacitance for the driver assuming $C_{ox} \approx 6\text{fF}/\mu\text{m}^2$ and the channel lengths are $0.5\mu\text{m}$, is,

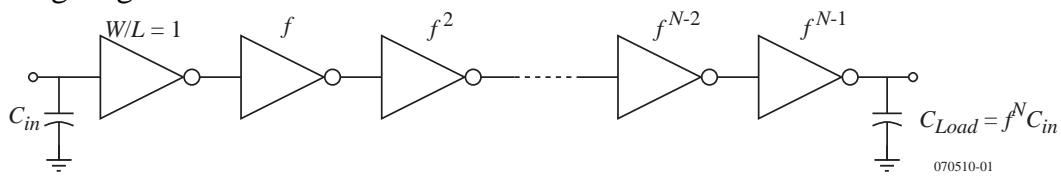
$$\begin{aligned} C_{in} &= C_{gs1} + C_{gs2} = 2 \cdot (2/3) C_{ox} (W_1 L_1 + W_2 L_2) \\ &= 1.33 \cdot 6\text{fF}/\mu\text{m}^2 (121\mu\text{m}^2) = 0.968 \text{ pF} \end{aligned}$$



If the effective resistance of the driver is $30\text{k}\Omega$, then the delay is 29 ns which is much too large.

Optimizing the Delay of a Chain of Push-Pull Inverters

For a series of N inverters as shown below, the W/L is increased by a factor of f for each succeeding stage.



From the above figure we see that $C_{Load} = f^N C_{in}$ – $N = \frac{\ln(C_{Load}/C_{in})}{\ln f}$

The delay of a single, push-pull inverter can be expressed as,

$$t_{inv} = \tau_{inv} \left(\frac{C_j}{C_{j-1}} + \gamma_{inv} \right)$$

where

$$\tau_{inv} = R_{eff} C_{in} \quad (R_{eff} \text{ is the effective output resistance of the inverter})$$

$$\gamma_{inv} = \frac{C_{self}}{C_{in}} = \frac{C_{junction}}{C_{in}} \quad (C_{junction} \text{ is the bulk-drain capacitances})$$

Optimizing the Delay of a Chain of Push-Pull Inverters – Continued

The total delay of the chain of inverters is

$$t_{total} = N \tau_{inv} \left(\frac{C_j}{C_{j-1}} + \gamma_{inv} \right)$$

Setting $f = \frac{C_j}{C_{j-1}}$ gives

$$t_{total} = \frac{\ln(C_{Load}/C_{in})}{\ln f} \tau_{inv} (f + \gamma_{inv})$$

Plotting the total delay versus f for various values of γ_{inv} shows that the optimum value of f lies in the range of 2.5 to 4[†].

[†] D.A. Hodges, H.G. Jackson, and R.A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd ed., McGraw-Hill Book Co., 2004, Chapter 6.

Example 330-1 – Finding the Optimum Delay for a Chain of Inverters

Assume that C_{Load} is 5pf, $C_{in} = 50fF$, $\tau_{inv} = 10ps$, and $\gamma_{inv} = 0.5$. If $f = 3.6$, find the optimal number of stages and the total delay of this chain of inverters.

Solution

From above we get the optimal number of stages as,

$$N = \frac{\ln(C_{Load}/C_{in})}{\ln f} = \frac{\ln(100)}{\ln 3.6} = 3.59$$

If we choose $N = 4$, then f can be recomputed as

$$\ln f = \frac{1}{4} \ln(100) \Rightarrow f = 3.16$$

The total delay is,

$$t_{total} = N \tau_{inv} \left(\frac{C_j}{C_{j-1}} + \gamma_{inv} \right) = 4 \cdot 10ps(3.16 + 0.5) = 146ps$$

Self-Biased Differential Amplifier[†]

Not as good as the push-pull inverter but interesting.

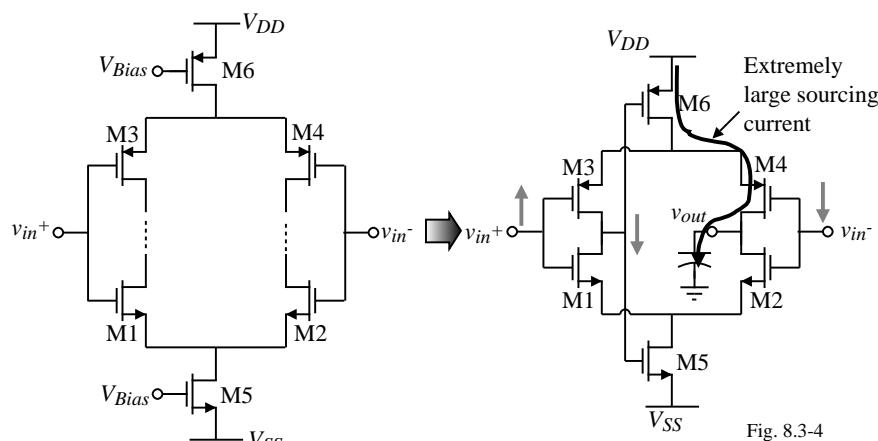


Fig. 8.3-4

Advantage:

Large sink or source current with out a large quiescent current.

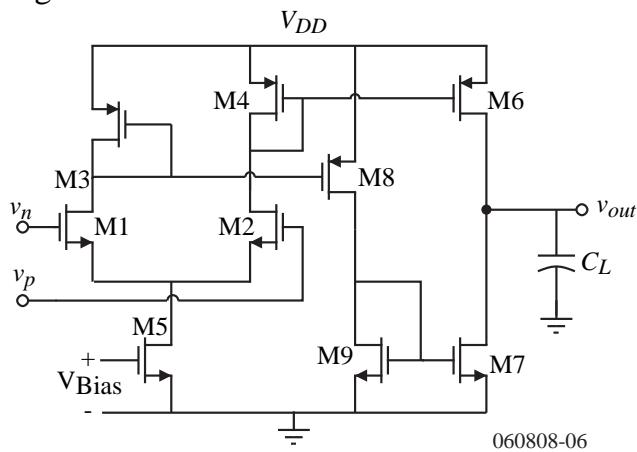
Disadvantage:

Poor common mode range (v_{in^+} slower than v_{in^-})

[†] M. Bazes, "Two Novel Full Complementary Self-Biased CMOS Differential Amplifiers," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 2, Feb. 1991, pp. 165-168.

Two-Stage Comparator with Increased Speed

Clamp the input stage with $1/g_m$ loads to decrease the signal swing and avoid slew rate limitation in the first stage.

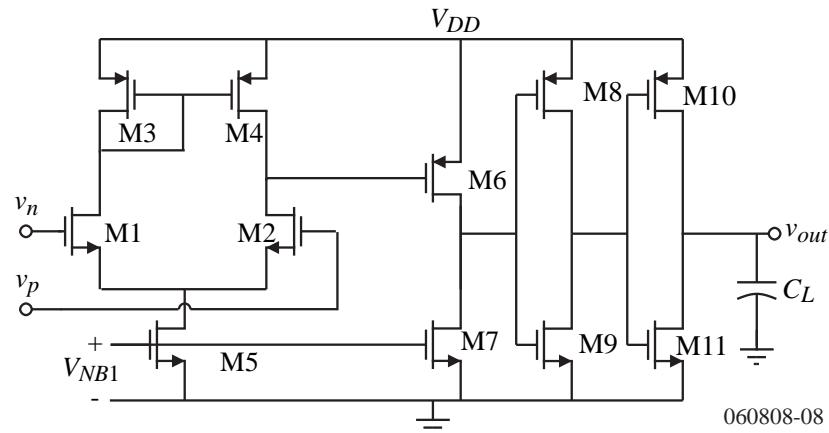


060808-06

Comments:

- Gain reduced \rightarrow Larger input resolution
- Push-pull output \rightarrow Higher slew rates
- Can increase the current drive by cascading the output stage

Comparators that Can Drive Large Capacitive Loads



060808-08

Comments:

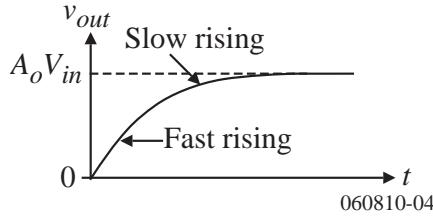
- Slew rate = $3V/\mu s$ into $50pF$
- Linear rise/fall time = $100ns$ into $50pF$
- Propagation delay time $\approx 1\mu s$
- Loop gain $\approx 32,000$ V/V
- The quiescent dc currents in the output stages are not well defined
- Use the principle of optimizing the delay in cascaded inverters

HIGH SPEED COMPARATORS

A Study in Exponentials

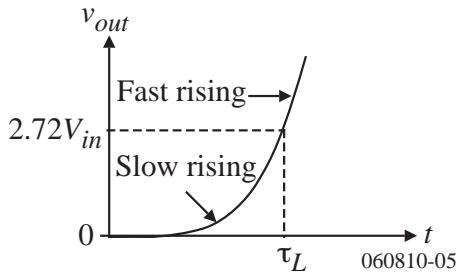
The step response of an amplifier with a gain of A_o and a dominant pole at ω_A is,

$$v_{out}(t) = A_o[1 - \exp(-\omega_A t)] V_{in}$$



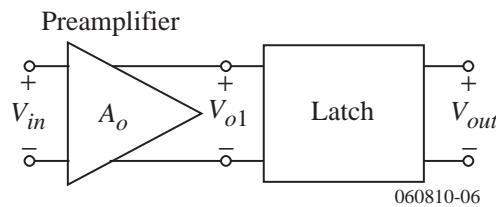
The latch response to a step input of V_{in} is,

$$v_{out}(t) = V_{in} \exp\left(\frac{t}{\tau_L}\right)$$

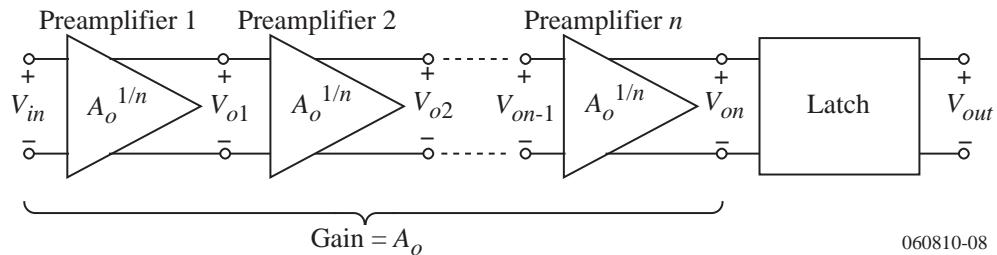


A High-Speed Comparator Architecture

Cascade an amplifier with a latch to take advantage of the exponential characteristics of the previous slide.



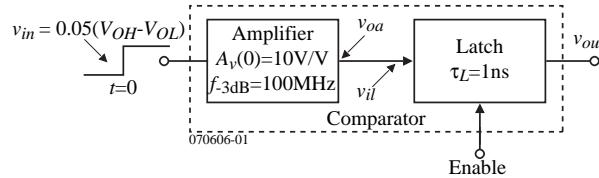
In order to keep the bandwidth of the amplifier large, the gain will be small. To achieve



Therefore, the question is how many stages of the amplifier and what is the gain of each stage for optimum results?

Ex. 330-2 – Optimizing the Propagation Time Delay

A comparator consists of an amplifier cascaded with a latch as shown below. The amplifier has a voltage gain of 10V/V and $f_{-3dB} = 100MHz$ and the latch has a time constant of 1ns. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL} . When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH}-V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay?



Solution

The solution is based on the figure shown.

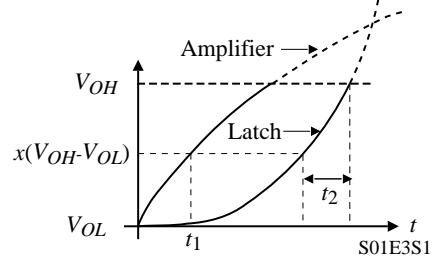
We note that,

$$v_{\alpha}(t) = 10[1-e^{-\omega_{-3dB}t}]0.05(V_{OH}-V_{OL}).$$

If we define the input voltage to the latch as,

$$v_{il} = x(V_{OH}-V_{OL})$$

then we can solve for t_1 and t_2 as follows:



Example 330-2 - Continued

$$x \cdot (V_{OH}-V_{OL}) = 10[1-e^{-\omega_{-3dB}t_1}]0.05(V_{OH}-V_{OL}) \rightarrow x = 0.5[1-e^{-\omega_{-3dB}t_1}]$$

This gives,

$$t_1 = \frac{1}{\omega_{-3dB}} \ln \left(\frac{1}{1-2x} \right)$$

From the propagation time delay of the latch we get,

$$t_2 = \tau_L \ln \left(\frac{V_{OH}-V_{OL}}{2v_{il}} \right) = \tau_L \ln \left(\frac{1}{2x} \right)$$

$$\therefore t_p = t_1 + t_2 = \frac{1}{\omega_{-3dB}} \ln \left(\frac{1}{1-2x} \right) + \tau_L \ln \left(\frac{1}{2x} \right) \rightarrow \frac{dt_p}{dx} = 0 \text{ gives}$$

$$2x = \frac{2\tau_L \omega_{-3dB}}{2+2\tau_L \omega_{-3dB}} = \frac{0.4\pi}{2+0.4\pi} = 0.3859 \quad (x = 0.1930)$$

$$t_1 = \frac{10\text{ns}}{2\pi} \ln \left(\frac{1}{1-0.3859} \right) = 1.592\text{ns} \cdot 0.4875 = 0.7762 \text{ ns}$$

$$\text{and } t_2 = 1\text{ns} \ln \left(\frac{1}{0.3859} \right) = 0.9522\text{ns}$$

$$\therefore t_p = t_1 + t_2 = 0.776 \text{ ns} + 0.952 \text{ ns} = \underline{1.728 \text{ ns}}$$

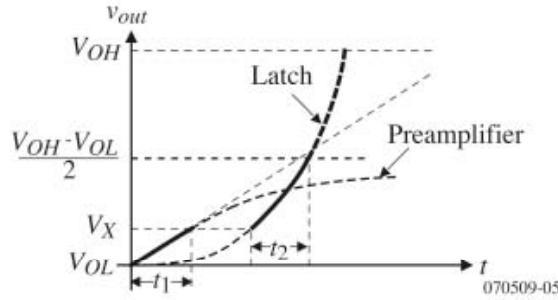
Minimizing the Propagation Delay Time in Comparators

Facts:

- The input signal is equal to $V_{in}(\min)$ for worst case
- Amplifiers have a step response with a negative argument in the exponential
- Latches have a step response with a positive argument in the exponential
- If the amplifiers rise too quickly, they will be slew limited

Approach:

- Use a cascade of low-gain, wide-bandwidth amplifiers to take a small input signal and amplify it without suffering slew limit
- Use a latch to take the amplified input and quickly reach $0.5(V_{OH}-V_{OL})$

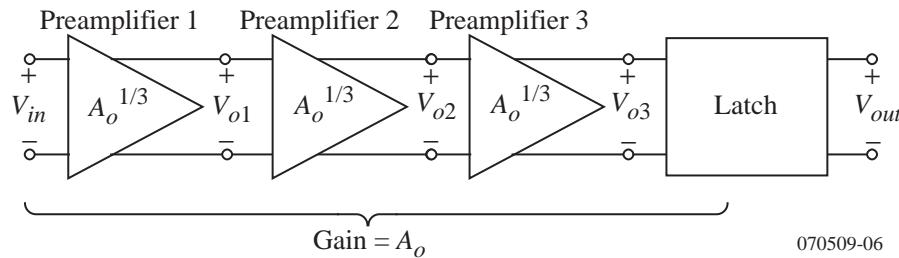


Minimization of the Propagation Delay Time

Minimization of t_p :

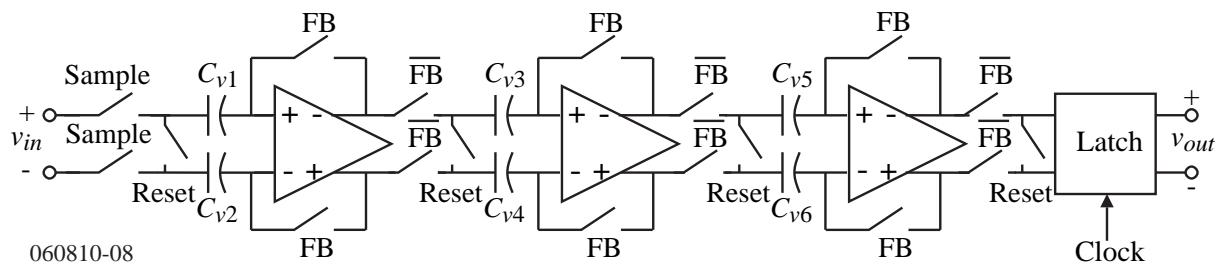
Q. If the preamplifier consists of n stages of gain A having a single-pole response, what is the value of n and A that gives minimum propagation delay time?

A. $n = 6$ and $A = 2.62$ but this is a very broad minimum and n is usually 3 and $A \approx 6-7$ to save area.



Fully Differential, Three-Stage Amplifier and Latch Comparator

Circuit:



Comments:

- Autozero and reset phase followed by comparison phase
- In the autozero phase, switches labeled “Reset” and “FB” are closed.
- In the sample phase, switches labeled “Sample” and “ \overline{FB} ” are closed.
- Can run as high as 200Msps

Preamplifier and Latch Circuits

Gain:

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\frac{g_{m2}}{g_{m4}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_p'(W_3/L_3)}}$$

Dominant Pole:

$$|p_{dominant}| = \frac{g_{m3}}{C} = \frac{g_{m4}}{C}$$

where C is the capacitance seen from the output nodes to ground.

If $(W_1/L_1)/(W_3/L_3) = 100$ and the bias current is $100\mu A$, then $A = -3.85$ and the bandwidth is 15.9MHz if $C = 0.5pF$.

Comments:

- If a buffer is used to reduce the output capacitance, one must take into account the loss of the buffer.
- The use of a preamplifier before the latch reduces the latch offset by the gain of the preamplifier so that the offset is due to the preamplifier only.

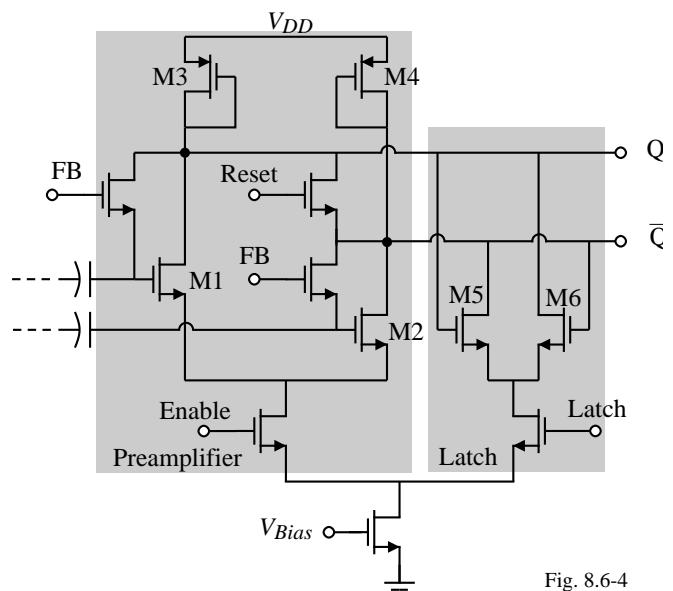


Fig. 8.6-4

An Improved Preamplifier

Circuit:

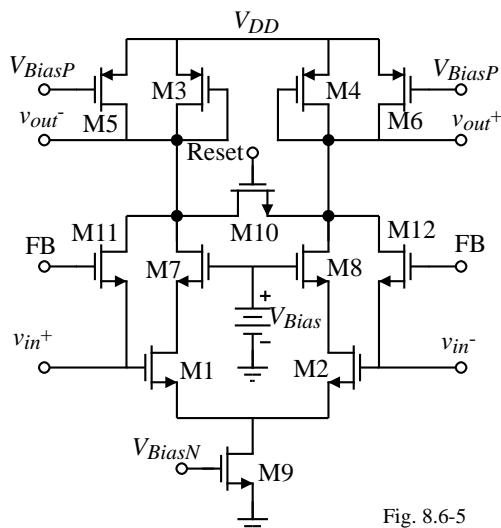


Fig. 8.6-5

Gain:

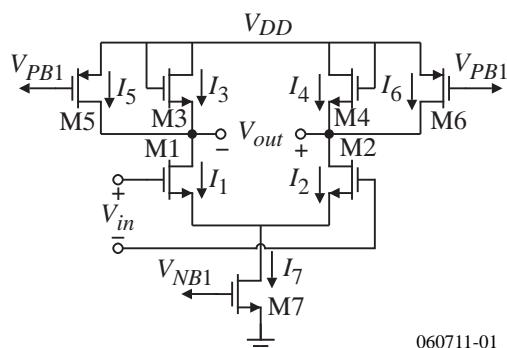
$$A_v = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K_N'(W_1/L_1)I_1}{K_P'(W_3/L_3)I_3}} = -\sqrt{\frac{K_N'(W_1/L_1)}{K_P'(W_3/L_3)}} \sqrt{1+I_5/I_3}$$

If $I_5 = 24I_3$, the gain is increased by a factor of 5

Improved Frequency Response of the Amplifier

If the ratio of transconductance W/L is much larger than the load W/L , the frequency response will suffer. Using the technique of the previous slide, we can keep the ratio of the W/L s to a more reasonable value. The result is higher frequency response.

Amplifier of Example 270-3:



060711-01

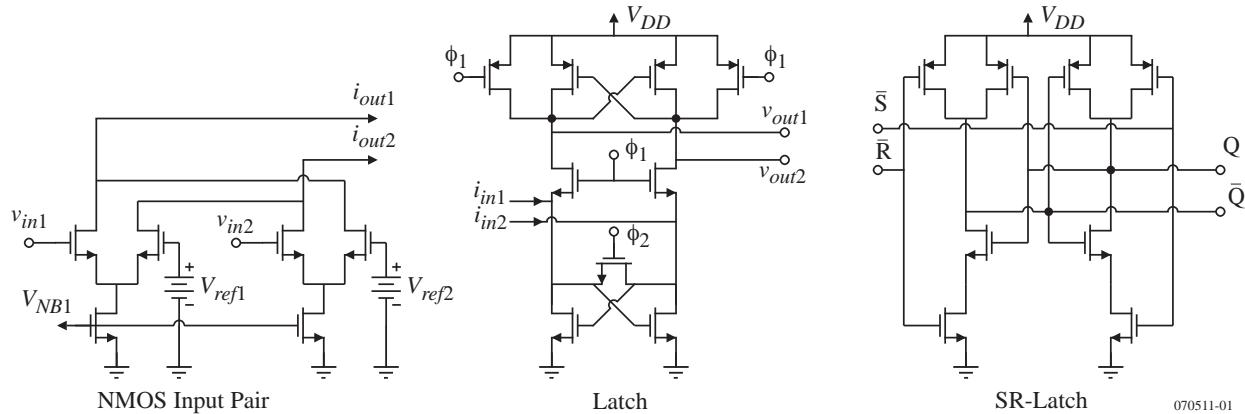
Gain = 20dB

$f_{-3dB} = 551\text{MHz}$

High-Speed CMOS Comparator

The comparator used in a 12-bit, 200 Msps ADC is shown below[†]. The comparator is used in each of the 4-bit pipeline stages which requires 15 comparators.

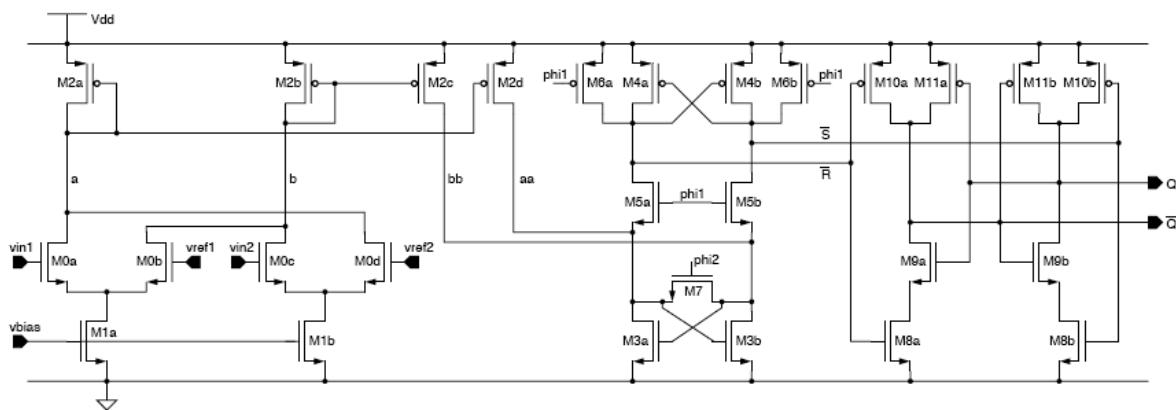
The comparators consist of three stages including (a.) differential input pairs, (b.) a cross-coupled latch, and (c.) an SR latch to hold the comparator output until the next clock cycle.



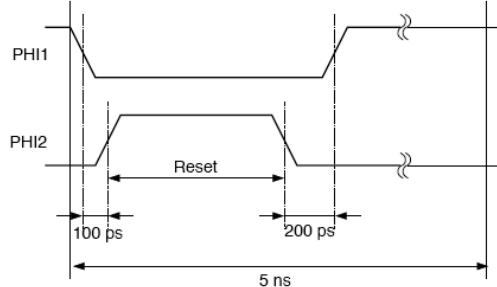
[†] T. Liechti, "Design of a High-Seed 12-bit Differential Pipelined A/D Converter," Diploma Project, Feb. 2004, Microelectronic Systems Laboratory, Swiss Federal Institute of Technology, Lausanne.

High Speed CMOS Comparator – Continued

Schematic of the fully differential comparator:



Clock waveforms:



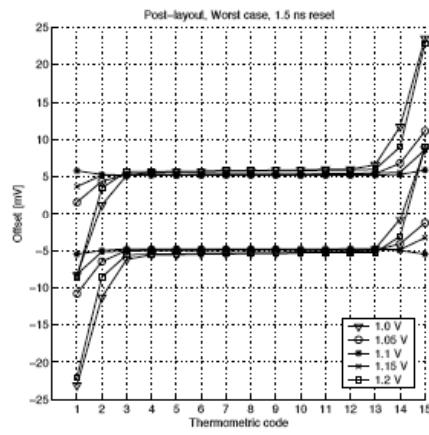
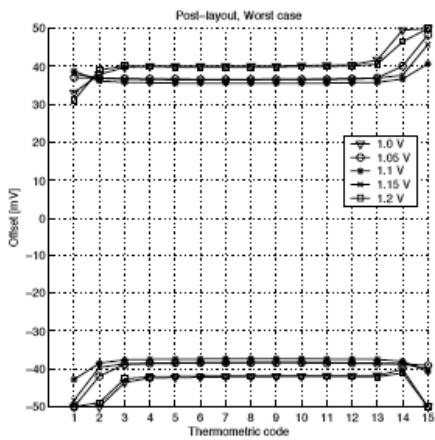
Mean comparator power dissipation is $140\mu\text{W}$ under typical conditions

High Speed CMOS Comparator – Continued

Transistor sizes:

Transistor	M0a, M0b, M0c, M0d	M1a, M1b	M2a, M2b, M2c, M2d	M3a, M3b	M4a, M4b	M5a, M5b	M6a, M6b	M7	M8a, M8b	M9a, M9b	M10a, M10b	M11a M11b
W(μm)	1.5	6	3.6	3	1	1	0.24	0.5	2	2.5	3	0.24
L(μm)	1	2.5	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18

Comparator offsets (worst case):



SUMMARY

- Comparators are limited in speed either by bandwidth or slew rate
- Increasing the magnitude of the poles improves the bandwidth limitations
- Increasing the current sinking/sourcing ability improves the slew rate limitation
- Most high speed comparators use a combination of preamplifier followed by a latch
 - The preamplifier uses bandwidth to quickly build up the input
 - The latch uses positive feedback to take the signal to its final state

LECTURE 340 – CHARACTERIZATION OF DACS AND CURRENT SCALING DACS

LECTURE ORGANIZATION

Outline

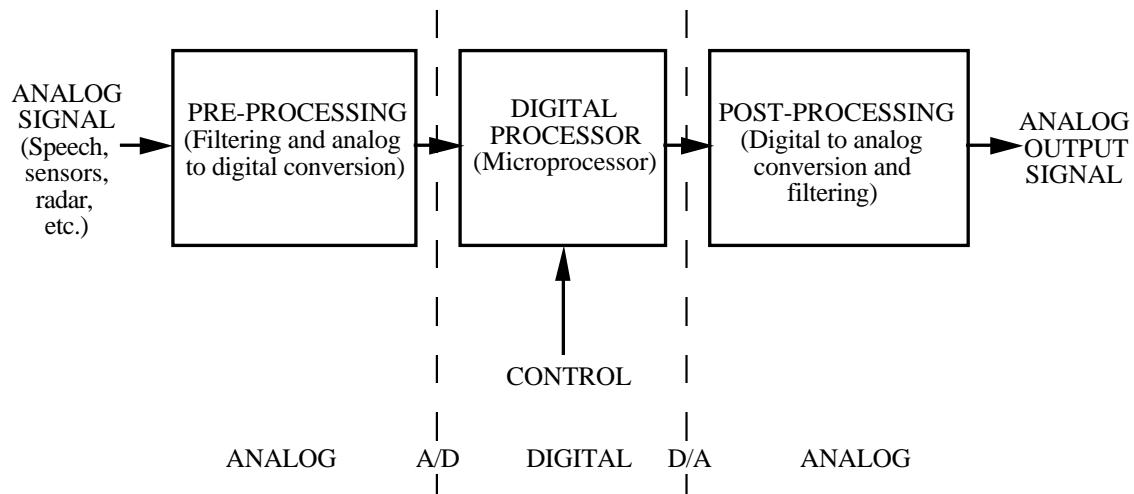
- Introduction
- Static characterization of DACs
- Dynamic characterization of DACs
- Testing of DACs
- Current scaling DACs
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 613-626

INTRODUCTION

Importance of Data Converters in Signal Processing



Digital-Analog Converters

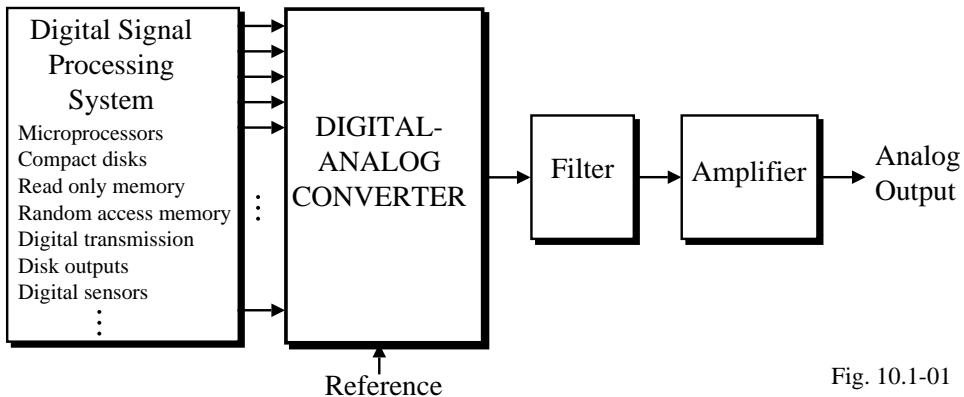
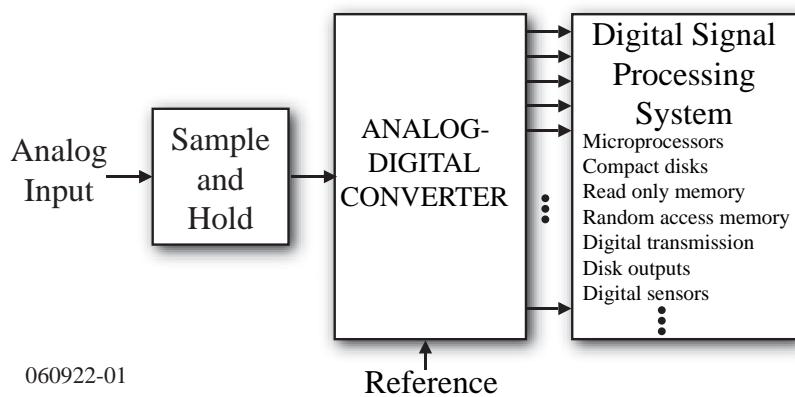


Fig. 10.1-01

Characteristics:

- Can be asynchronous or synchronous
- Primary active element is the op amp
- Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} \cdot T$)

Analog-Digital Converters



060922-01

Characteristics:

- Can only be synchronous (the analog signal must be sampled and held during conversion)
- Primary active element is the comparator
- Conversion time can vary from fast (one clock period, T) to slow ($2^{\text{No. of bits}} \cdot T$)

STATIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

Block Diagram of a Digital-Analog Converter

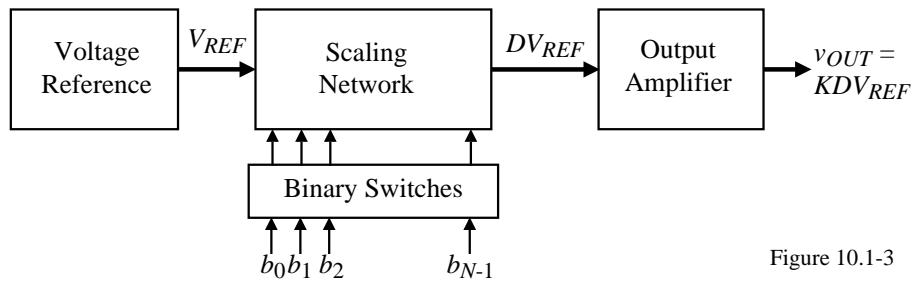


Figure 10.1-3

b_0 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

b_{N-1} is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

Input-Output Characteristics

Ideal input-output characteristics of a 3-bit DAC

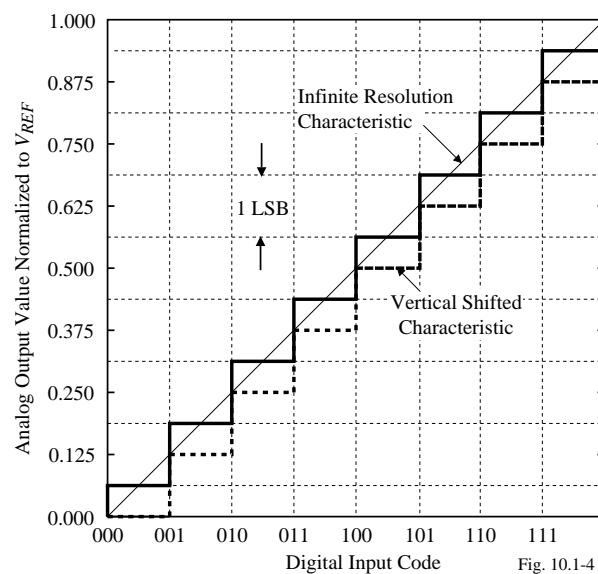


Fig. 10.1-4

Definitions

- *Resolution* of the DAC is equal to the number of bits in the applied digital input word.

- *The full scale (FS)*:

FS = Analog output when all bits are 1 - Analog output all bits are 0

$$FS = (V_{REF} - \frac{V_{REF}}{2^N}) - 0 = V_{REF}\left(1 - \frac{1}{2^N}\right)$$

- *Full scale range (FSR)* is defined as

$$FSR = \lim_{N \rightarrow \infty} (FS) = V_{REF}$$

- *Quantization Noise* is the inherent uncertainty in digitizing an analog value with a finite resolution converter.

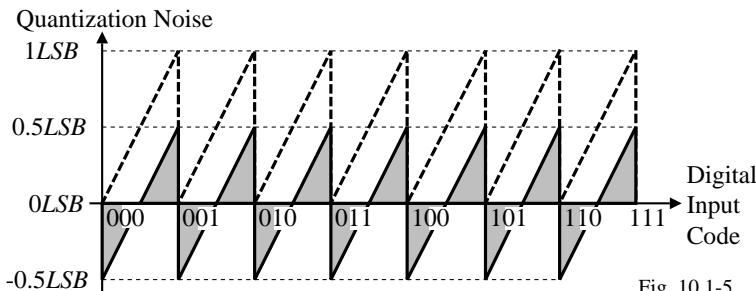


Fig. 10.1-5

More Definitions

- *Dynamic Range (DR)* of a DAC is the ratio of the FSR to the smallest difference that can be resolved (i.e. an *LSB*)

$$DR = \frac{FSR}{LSB \text{ change}} = \frac{FSR}{(FSR/2^N)} = 2^N$$

or in terms of decibels

$$DR(\text{dB}) = 6.02N \text{ (dB)}$$

- *Signal-to-noise ratio (SNR)* for the DAC is the ratio of the full scale value to the *rms* value of the quantization noise.

$$\text{rms(quantization noise)} = \sqrt{\frac{1}{T} \int_0^T LS B^2 \left(\frac{t}{T} - 0.5\right)^2 dt} = \frac{LSB}{\sqrt{12}} = \frac{FSR}{2^N \sqrt{12}}$$

$$\therefore SNR = \frac{v_{OUT}(\text{rms})}{(FSR/\sqrt{12}) 2^N}$$

- *Maximum SNR (SNR_{max})* for a sinusoid is defined as

$$SNR_{max} = \frac{v_{OUTmax}(\text{rms})}{(FSR/\sqrt{12}) 2^N} = \frac{FSR/(2\sqrt{2})}{FSR/(\sqrt{12}) 2^N} = \frac{\sqrt{6} 2^N}{2}$$

or in terms of decibels

$$SNR_{max}(\text{dB}) = 20 \log_{10} \left(\frac{\sqrt{6} 2^N}{2} \right) = 10 \log_{10}(6) + 20 \log_{10}(2^N) - 20 \log_{10}(2) = 1.76 + 6.02N \text{ dB}$$

Even More Definitions

- *Effective number of bits (ENOB)* can be defined from the above as

$$ENOB = \frac{SNR_{Actual} - 1.76}{6.02}$$

where SNR_{Actual} is the actual SNR of the converter.

Comment:

The DR is the amplitude range necessary to resolve N bits regardless of the amplitude of the output voltage.

However, when referenced to a given output analog signal amplitude, the DR required must include 1.76 dB more to account for the presence of quantization noise.

Thus, for a 10-bit DAC, the DR is 60.2 dB and for a full-scale, *rms* output voltage, the signal must be approximately 62 dB above whatever noise floor is present in the output of the DAC.

Accuracy Requirements of the i -th Bit

- The output of the i -th bit of the converter is expressed as:

$$\text{The output of the } i\text{-th bit} = \frac{V_{REF}}{2^{i+1}} \left(\frac{2^n}{2^n} \right) = 2^{n-i-1} \text{ LSBs}$$

- The uncertainty of each bit must be less than $\pm 0.5 \text{ LSB}$ (assuming all other bits are ideal. Must use $\pm 0.25 \text{ LSB}$ if each bit has a worst case error.)

- The accuracy of the i -th bit is equal to the uncertainty divided by the output giving:

$$\text{Accuracy of the } i\text{-th bit} = \frac{\pm 0.5 \text{ LSB}}{2^{n-i-1} \text{ LSB}} = \frac{1}{2^{n-i}} = \frac{100}{2^{n-i}} \%$$

Result: The highest accuracy requirement is always the MSB ($i = 0$).

The LSB bit only needs $\pm 50\%$ accuracy.

Example:

What is the accuracy requirement for each of the bits of a 10 bit converter?
Assuming all other bits are ideal, the accuracy requirement per bit is given below.

Bit Number	0	1	2	3	4	5	6	7	8	9
Accuracy %	0.098	0.195	0.391	0.781	1.563	3.125	6.25	12.5	25	50

(If all other bits are worst case, the numbers above must be divided by 2.)

Offset and Gain Errors

An *offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump.

A *gain error* is the difference between the slope of the actual finite resolution and the ideal finite resolution characteristic measured at the right-most vertical jump.

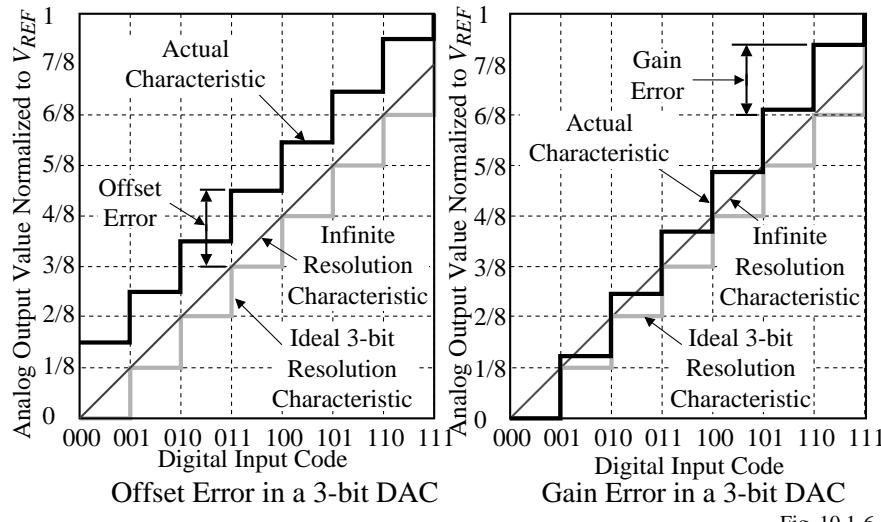


Fig. 10.1-6

Integral and Differential Nonlinearity

- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*).
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical jump (% or *LSB*).

$$DNL = V_{cx} - V_s = \left(\frac{V_{cx} - V_s}{V_s} \right) V_s = \left(\frac{V_{cx}}{V_s} - 1 \right) LSBs$$

where V_{cx} is the actual voltage change on a bit-to-bit basis and V_s is the ideal *LSB* change of ($V_{FSR}/2^N$)

Example of a 3-bit DAC:

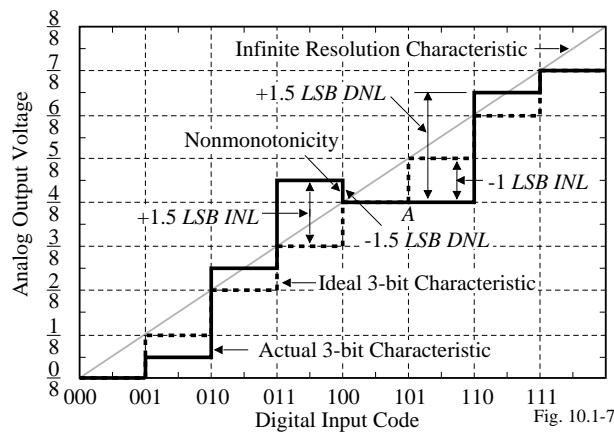


Fig. 10.1-7

Example of INL and DNL of a Nonideal 4-Bit Dac

Find the \pm INL and \pm DNL for the 4-bit DAC shown.

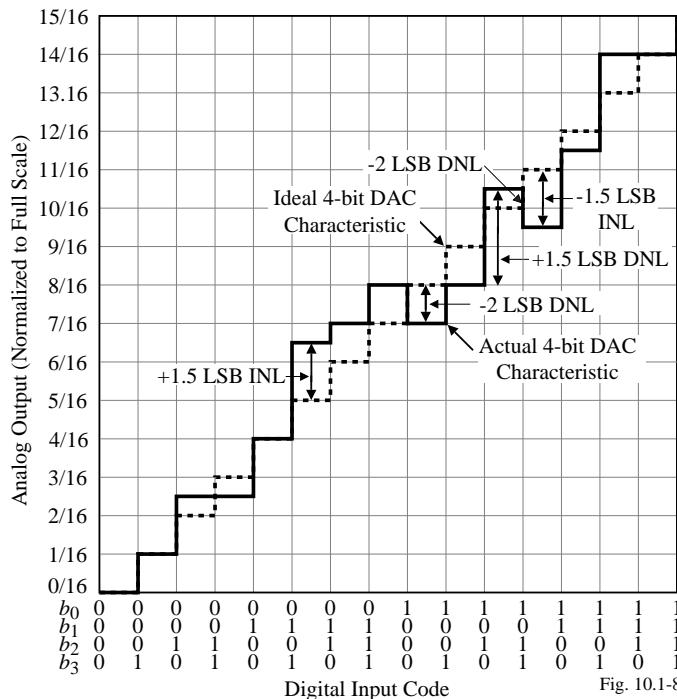


Fig. 10.1-8

DYNAMIC CHARACTERISTICS OF DIGITAL-ANALOG CONVERTERS

Dynamic characteristics include the influence of time.

Definitions

- *Conversion speed* is the time it takes for the DAC to provide an analog output when the digital input word is changed.

Factor that influence the conversion speed:

Parasitic capacitors (would like all nodes to be low impedance)

Op amp gainbandwidth

Op amp slew rate

- *Gain error* of an op amp is the difference between the desired and actual output voltage of the op amp (can have both a static and dynamic influence)

$$\text{Actual Gain} = \text{Ideal Gain} \times \left(\frac{\text{Loop Gain}}{1 + \text{Loop Gain}} \right)$$

$$\text{Gain error} = \frac{\text{Ideal Gain}-\text{Actual Gain}}{\text{Ideal Gain}} = \frac{1}{1+\text{Loop Gain}}$$

Example of Influence of Op Amp Gain Error on DAC Performance

Assume that a DAC using an op amp in the inverting configuration with $C_1 = C_2$ and $A_{vd}(0) = 1000$. Find the largest resolution of the DAC if V_{REF} is 1V and assuming worst case conditions.

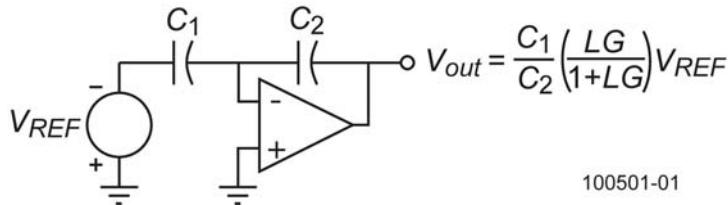
Solution

The loop gain of the inverting configuration is $LG = \frac{C_2}{C_1+C_2} A_{vd}(0) = 0.5 \cdot 1000 = 500$.

The gain error is therefore $1/501 \approx 0.002$. The gain error should be less than the quantization noise of $\pm 0.5LSB$ which is expressed as

$$\text{Gain error} = \frac{1}{501} \approx 0.002 \leq \frac{V_{REF}}{2^{N+1}}$$

Therefore the largest value of N that satisfies this equation is $N = 7$.



Influence of the Op Amp Gainbandwidth

Single-pole response:

$$v_{out}(t) = A_{CL}[1 - e^{-\omega_H t}]v_{in}(t)$$

where

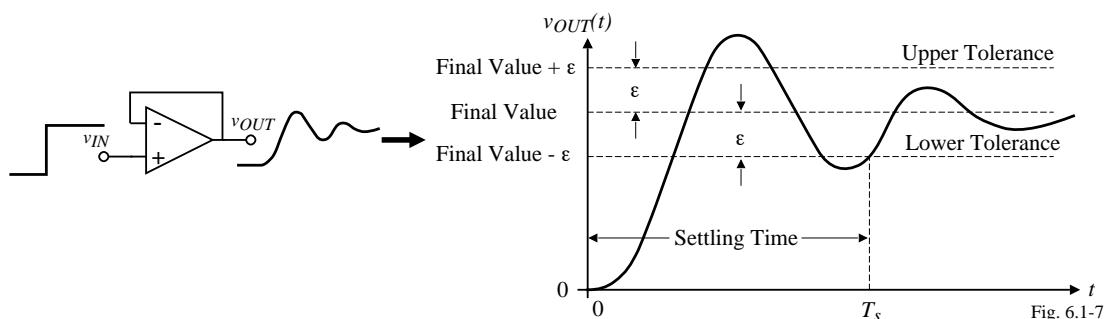
A_{CL} = closed-loop gain

$$\omega_H = GB \left(\frac{R_1}{R_1 + R_2} \right) \text{ or } GB \left(\frac{C_2}{C_1 + C_2} \right)$$

To avoid errors in DACs (and ADCs), $v_{out}(t)$ must be within $\pm 0.5LSB$ of the final value by the end of the conversion time.

Multiple-pole response:

Typically the response is underdamped like the following (see Appendix C of text).



Example of the Influence of GB and Settling Time on DAC Performance

Assume that a DAC uses a switched capacitor noninverting amplifier with $C_1 = C_2$ using an op amp with a dominant pole and $GB = 1\text{MHz}$. Find the conversion time of an 8-bit DAC if V_{REF} is 1V.

Solution

From the results in Sections 9.2 and 9.3 of the text, we know that

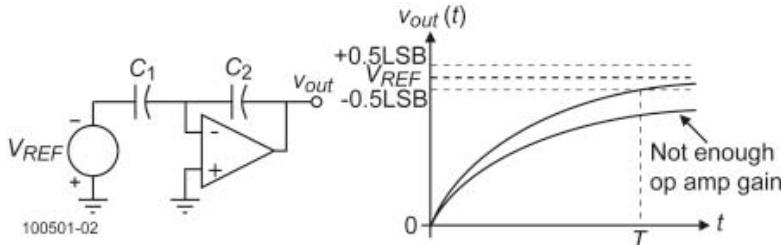
$$\omega_H = \left(\frac{C_2}{C_1+C_2} \right) GB = (2\pi)(0.5)(10^6) = 3.141 \times 10^6$$

and $A_{CL} = 1$. Assume that the ideal output is equal to V_{REF} . Therefore the value of the output voltage which is 0.5LSB of V_{REF} is

$$1 - \frac{1}{2^{N+1}} = 1 - e^{-\omega_H T}$$

or

$$2^{N+1} = e^{\omega_H T}$$



Solving for T gives

$$T = \left(\frac{N+1}{\omega_H} \right) \ln(2) = 0.693 \left(\frac{N+1}{\omega_H} \right) = \left(\frac{9}{3.141} \right) 0.693 = 1.986 \mu\text{s}$$

TESTING OF DACS

Input-Output Test

Test setup:

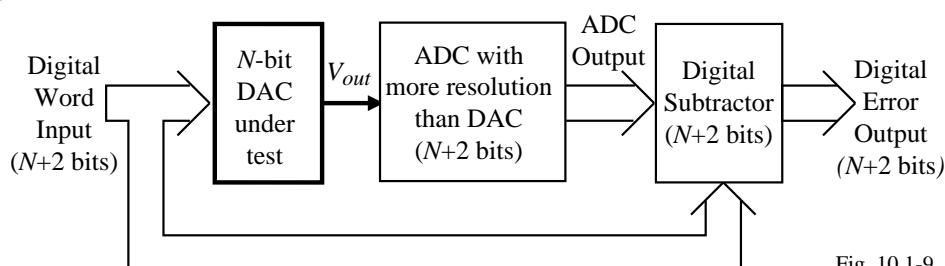


Fig. 10.1-9

Comments:

Sweep the digital input word from 000...0 to 111...1.

The ADC should have more resolution by at least 2 bits and be more accurate than the errors of the DAC

INL will show up in the output as the presence of 1's in any bit.

If there is a 1 in the N th bit, the *INL* is greater than $\pm 0.5\text{LSB}$

DNL will show up as a change between each successive digital error output.

The bits which are greater than N in the digital error output can be used to resolve the errors to less than $\pm 0.5\text{LSB}$

Spectral Test

Test setup:

Comments:

Digital input pattern is selected to have a fundamental frequency which has a magnitude of at least $6N$ dB above its harmonics.

Length of the digital sequence determines the spectral purity of the fundamental frequency.

All nonlinearities of the DAC (i.e. *INL* and *DNL*) will cause harmonics of the fundamental frequency

The THD can be used to determine the SNR dB range between the magnitude of the fundamental and the THD. This SNR should be at least $6N$ dB to have an *INL* of less than $\pm 0.5LSB$ for an ENOB of N -bits.

Note that the noise contribution of V_{REF} must be less than the noise floor due to nonlinearities.

If the period of the digital pattern is increased, the frequency dependence of *INL* can be measured.

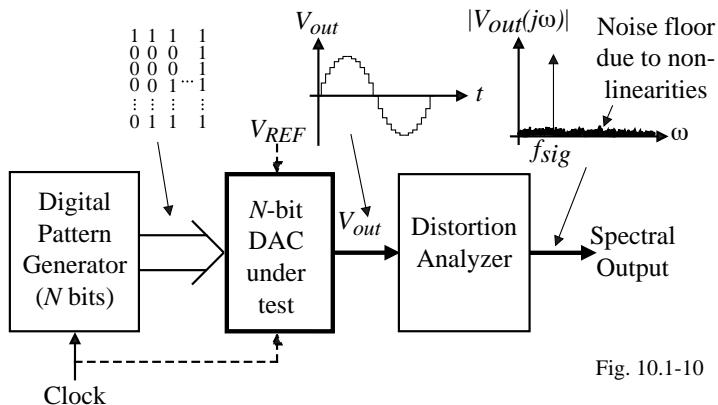


Fig. 10.1-10

CMOS Analog Circuit Design

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CURRENT SCALING DIGITAL-ANALOG CONVERTERS

Classification of Digital-Analog Converters

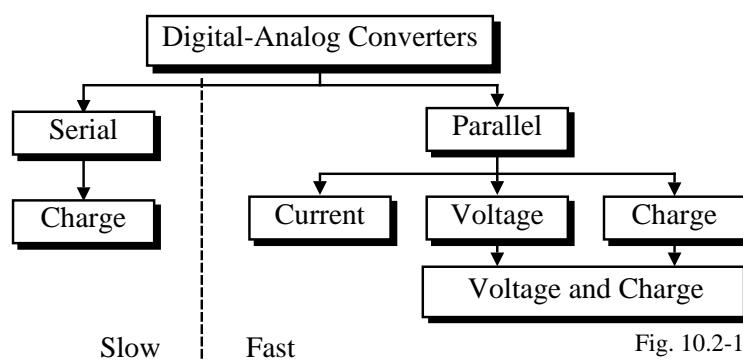


Fig. 10.2-1

General Current Scaling DACs

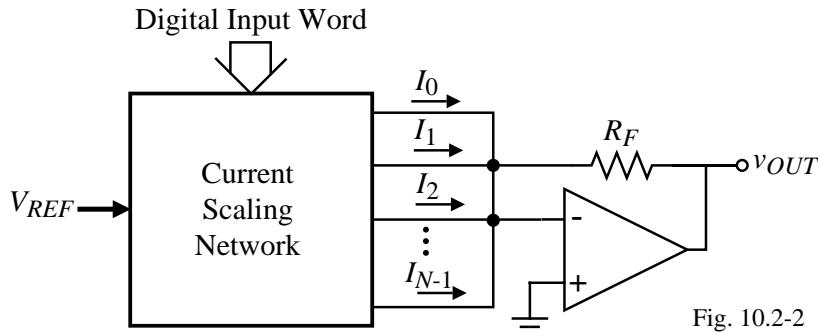


Fig. 10.2-2

The output voltage can be expressed as

$$V_{OUT} = -R_F(I_0 + I_1 + I_2 + \dots + I_{N-1})$$

where the currents I_0, I_1, I_2, \dots are binary weighted currents.

Binary-Weighted Resistor DAC

Circuit:

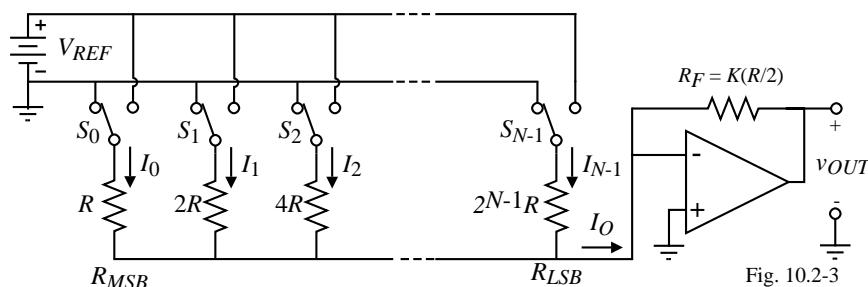


Fig. 10.2-3

Comments:

- 1.) R_F can be used to scale the gain of the DAC. If $R_F = KR/2$, then

$$v_{OUT} = -R_F I_O = \frac{-KR}{2} \left(\frac{b_0}{R} + \frac{b_1}{2R} + \frac{b_2}{4R} + \dots + \frac{b_{N-1}}{2^{N-1}R} \right) V_{REF} \Rightarrow v_{OUT} = -K \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \dots + \frac{b_{N-1}}{2^N} \right) V_{REF}$$

where b_i is 1 if switch S_i is connected to V_{REF} or 0 if switch S_i is connected to ground.

- 2.) Component spread value = $\frac{R_{MSB}}{R_{LSB}} = \frac{R}{2^{N-1}R} = \frac{1}{2^{N-1}}$

- 3.) Attributes:

Insensitive to parasitics \Rightarrow fast
Trimming required for large values of N

Large component spread value
Nonmonotonic

R-2R Ladder Implementation of the Binary Weighted Resistor DAC

Use of the R-2R concept to avoid large element spreads:

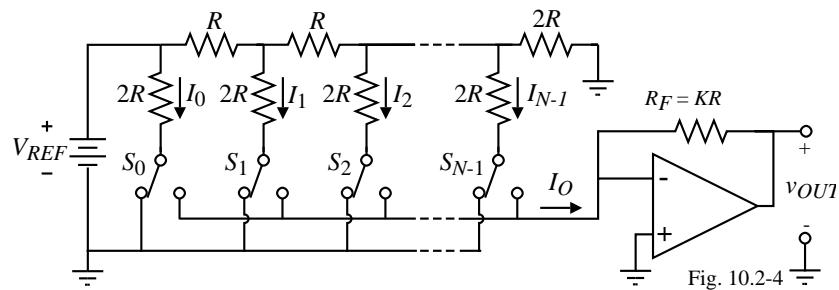


Fig. 10.2-4

How does the R-2R ladder work?

“The resistance seen to the right of any of the vertical $2R$ resistors is $2R$. ”

Attributes:

- Not sensitive to parasitics (currents through the resistors never change as S_i is varied)
- Small element spread. Resistors made from same unit ($2R$ consist of two in series or R consists of two in parallel)
- Not monotonic

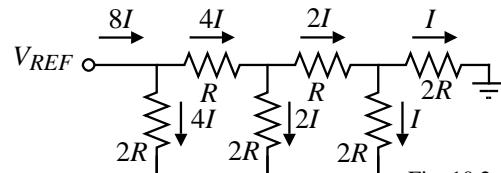


Fig. 10.2-4(2R-R)

Current Scaling Using Binary Weighted MOSFET Current Sinks

Circuit:

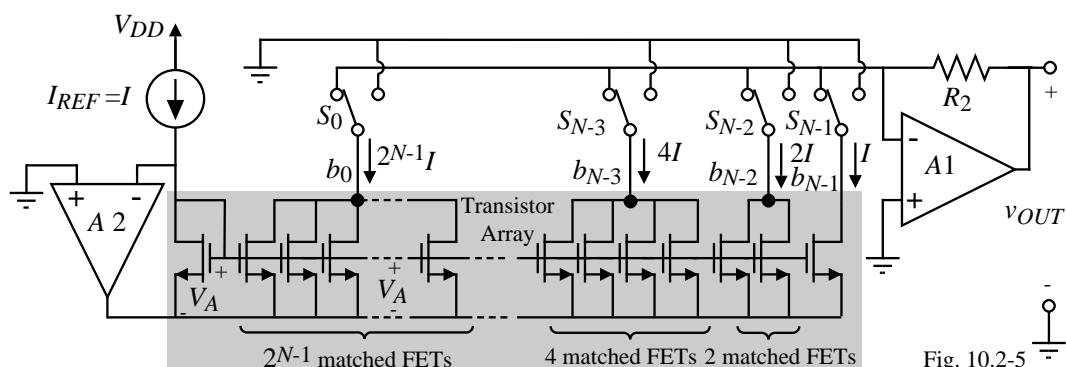


Fig. 10.2-5

Operation:

$$v_{OUT} = R_2(b_{N-1} \cdot I + b_{N-2} \cdot 2I + b_{N-3} \cdot 4I + \dots + b_0 \cdot 2^{N-1} \cdot I)$$

$$\text{If } I = I_{REF} = \frac{V_{REF}}{2N R_2}, \text{ then } v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \dots + \frac{b_{N-3}}{2^{N-2}} + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N} \right) V_{REF}$$

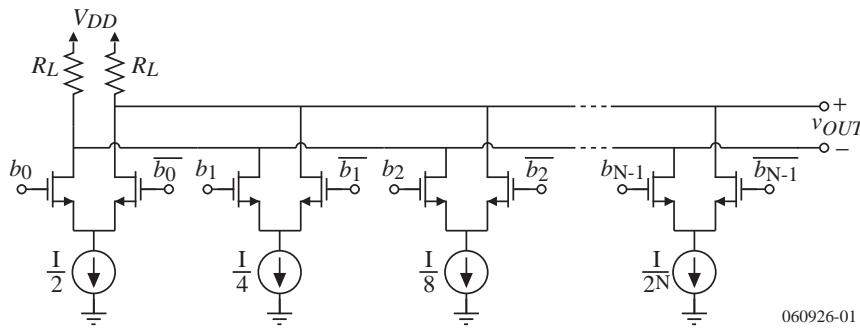
Attributes:

Fast (no floating nodes) and not monotonic

Accuracy of MSB greater than LSBs

High-Speed Current DACs

Current scaling DAC using current switches:



060926-01

$$v_{OUT} = IR_L \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \dots + \frac{b_{N-1}}{2^N} \right]$$

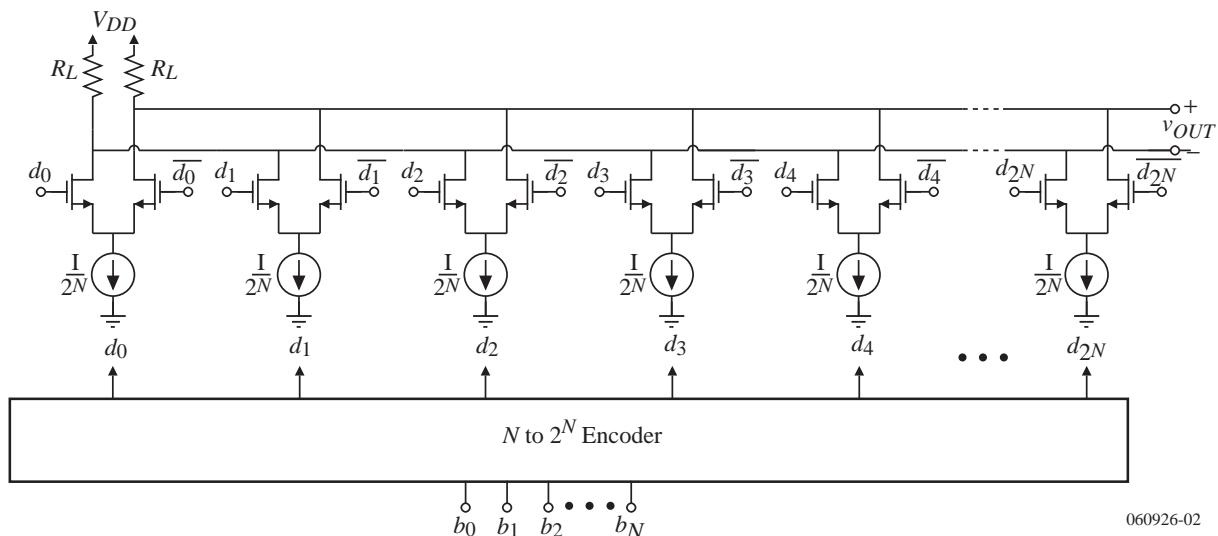
where

$$b_i = \begin{cases} +1 & \text{if the bit is 1} \\ -1 & \text{if the bit is 0} \end{cases}$$

A single-ended DAC can be obtained by replacing the left R_L by a short.

High-Speed, High-Accuracy Current Scaling DACs

The accuracy is increased by using the same value of current for each switch as shown.



060926-02

For a 4 bit DAC, there would be 16 current switches.

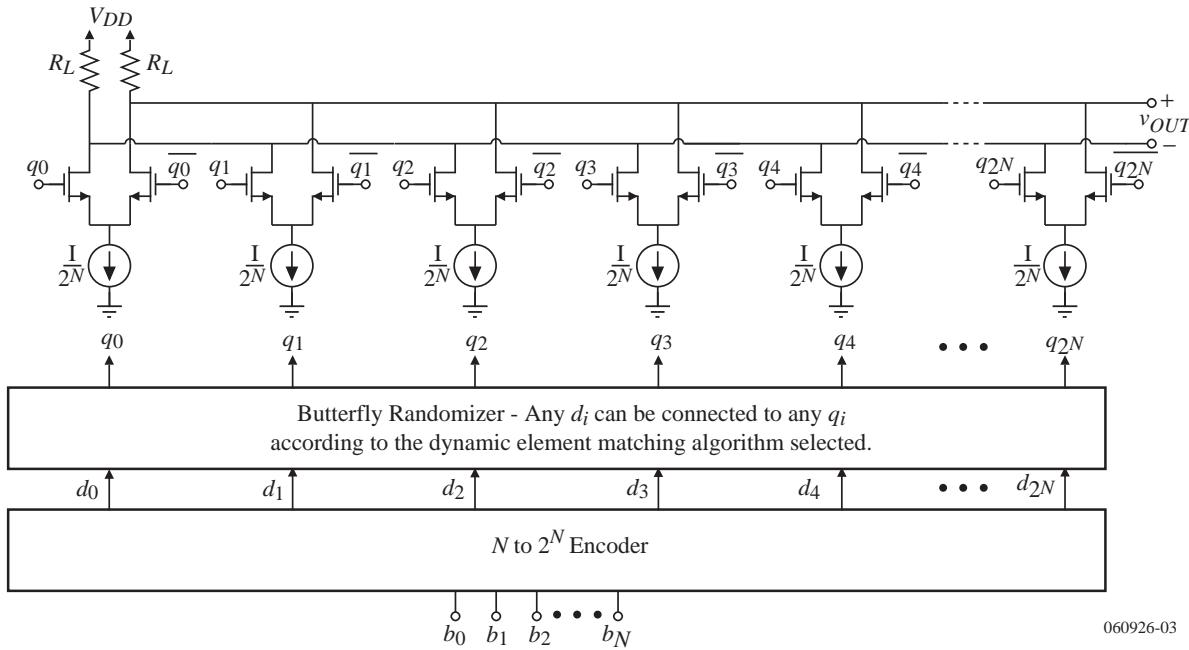
The MSB bit would switch 8 of the current switches to one side.

The next-MSB bit would switch 4 of the current switches to one side.

Etc.

Increasing the Accuracy of the Current Switching DAC

The accuracy of the previous DAC can be increased by using dynamic element matching techniques. This is illustrated below where a butterfly switching element allows the switch control bits, d_i , to be “randomly” connected to any of the current switches.



SUMMARY

- DACs scale a voltage reference as an analog output according to a digital word input
- Quantization noise is an inherent $\pm 0.5 \text{ LSB}$ uncertainty in digitizing an analog value with a finite resolution converter
- The most significant bit requires the greatest accuracy with the least significant bit requiring the least accuracy
- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or LSB)
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical jump (% or LSB)
- The limits to DAC speed include:
 - Parasitic capacitors
 - The op amp gainbandwidth
 - The op amp slew rate
- Current scaling DACs scale the reference voltage into binary-weighted currents that are summed into a resistor to obtain the analog output voltage.
- Current scaling DACs are generally fast but have large element spreads and are not monotonic

LECTURE 350 – PARALLEL DACS, IMPROVED DAC RESOLUTION AND SERIAL DACS

LECTURE ORGANIZATION

Outline

- Voltage scaling DACs
- Charge scaling DACs
- Extending the resolution of parallel DACs
- Serial DACs
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 626-652

VOLTAGE SCALING DIGITAL-ANALOG CONVERTERS

General Voltage Scaling Digital Analog Converter

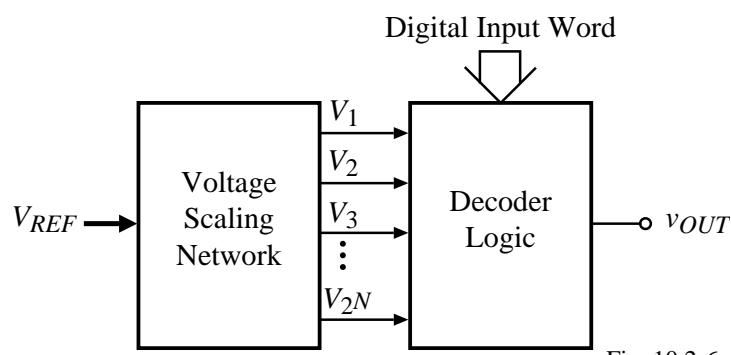


Fig. 10.2-6

Operation:

Creates all possible values of the analog output then uses a decoding network to determine which voltage to select based on the digital input word.

3-Bit Voltage Scaling Digital-Analog Converter

The voltage at any tap can be expressed as: $v_{OUT} = \frac{V_{REF}}{8}(n - 0.5) = \frac{V_{REF}}{16}(2n - 1)$

Attributes:

- Guaranteed monotonic
- Compatible with CMOS technology
- Large area if N is large
- Sensitive to parasitics
- Requires a buffer
- Large current can flow through the resistor string.

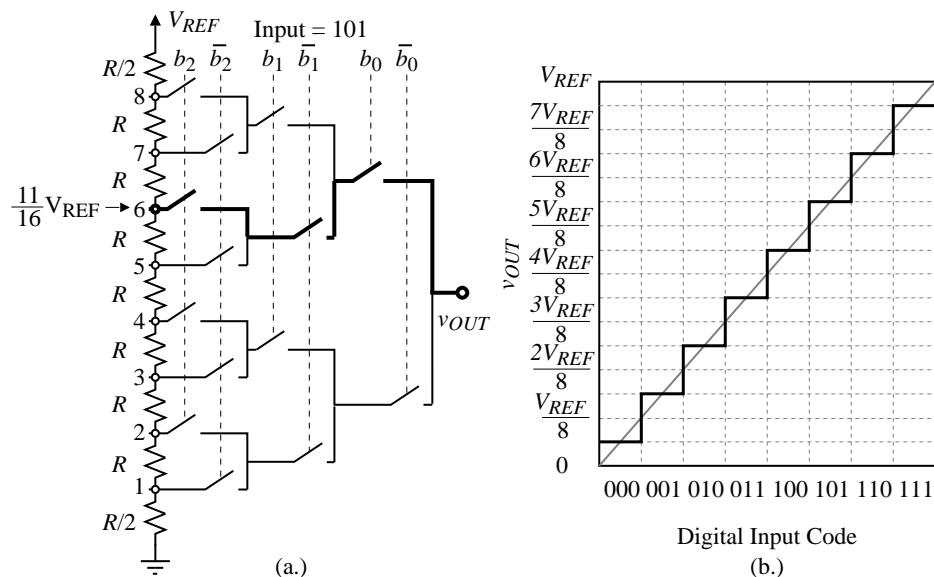


Figure 10.2-7 - (a.) Implementation of a 3-bit voltage scaling DAC. (b.) Input-output characteristics of Fig. 10.2-7(a.)

Alternate Realization of the 3-Bit Voltage Scaling DAC

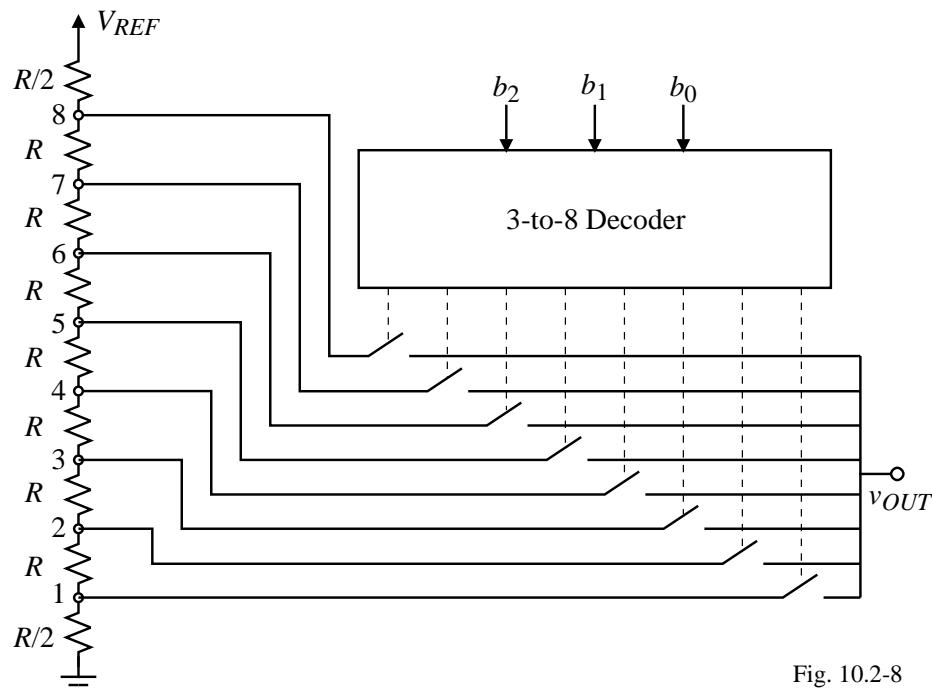


Fig. 10.2-8

INL and DNL of the Voltage Scaling DAC

Find an expression for the INL and DNL of the voltage scaling DAC using a worst-case approach. For an n -bit DAC, assume there are 2^n resistors between V_{REF} and ground and that the resistors are numbered from 1 to 2^n beginning with the resistor connected to V_{REF} and ending with the resistor connected to ground.

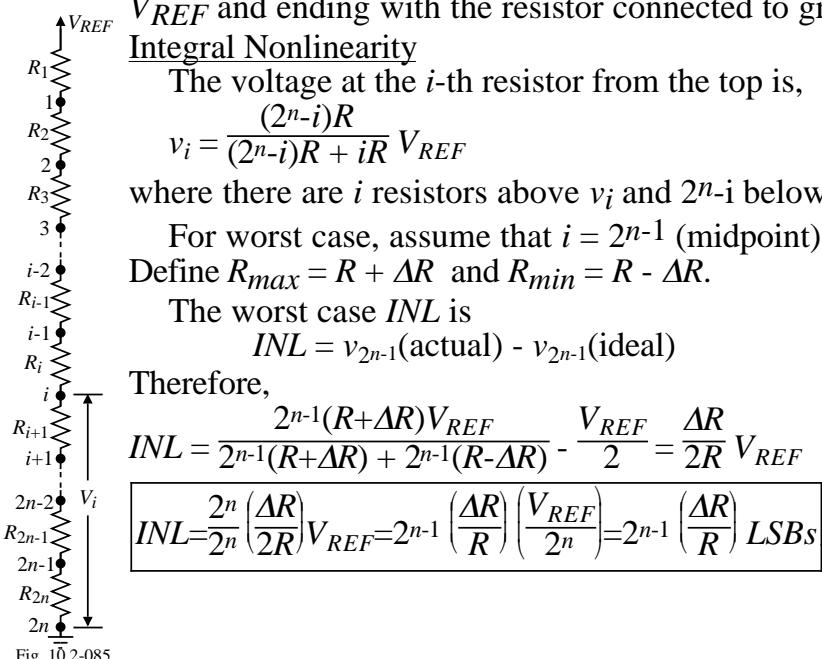


Fig. 10.2-085

Differential Nonlinearity

The worst case DNL is
 $DNL = v_{step}(\text{act}) - v_{step}(\text{ideal})$
 Substituting the actual and ideal steps gives,

$$\begin{aligned} &= \frac{(R \pm \Delta R)V_{REF}}{2^n R} - \frac{R V_{REF}}{2^n R} \\ &= \left(\frac{R \pm \Delta R}{R} - \frac{R}{R} \right) \frac{V_{REF}}{2^n} \\ &= \frac{\pm \Delta R}{R} \frac{V_{REF}}{2^n} \end{aligned}$$

Therefore,

$$DNL = \frac{\pm \Delta R}{R} LSBs$$

Example 350-1 - Accuracy Requirements of a Voltage-Scaling Digital-Analog Converter

If the resistor string of a voltage scaling digital-analog converter is a $5 \mu\text{m}$ wide polysilicon strip having a relative accuracy of $\pm 1\%$, what is the largest number of bits that can be resolved and keep the worst case INL within ± 0.5 LSB? For this number of bits what is the worst case DNL?

Solution

From the previous page, we can write that

$$2^{n-1} \left(\frac{\Delta R}{R} \right) = 2^{n-1} \left(\frac{1}{100} \right) \leq \frac{1}{2}$$

This inequality can be simplified

$$2^n \leq 100$$

which has a solution of $n = 6$.

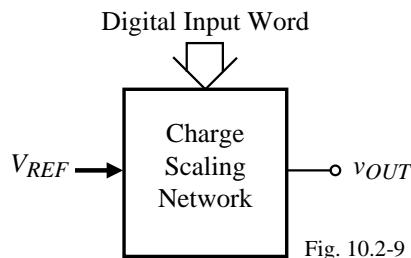
The value of the DNL for $n = 6$ is found from the previous page as

$$DNL = \frac{\pm 1}{100} LSBs = \pm 0.01 LSBs$$

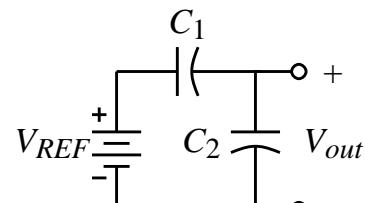
(This is the reason the resistor string is monotonic.)

CHARGE SCALING DIGITAL-ANALOG CONVERTERS

General Charge Scaling Digital-Analog Converter



General principle is to capacitively attenuate the reference voltage. Capacitive attenuation is simply:



Calculate as if the capacitors were resistors. For example,

$$V_{out} = \frac{\frac{1}{C_2}}{\frac{1}{C_1} + \frac{1}{C_2}} V_{REF} = \frac{C_1}{C_1 + C_2} V_{REF}$$

Fig. 10.2-9b

Binary-Weighted, Charge Scaling DAC

Circuit:

Operation:

1.) All switches connected to ground during ϕ_1 .

2.) Switch S_i closes to V_{REF} if $b_i = 1$ or to ground if $b_i = 0$.

Equating the charge in the capacitors gives,

$$V_{REF} C_{eq} = V_{REF} \left(b_0 C + \frac{b_1 C}{2} + \frac{b_2 C}{2^2} + \dots + \frac{b_{N-1} C}{2^{N-1}} \right) = C_{tot} v_{OUT} = 2C v_{OUT}$$

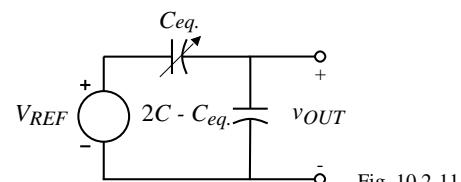
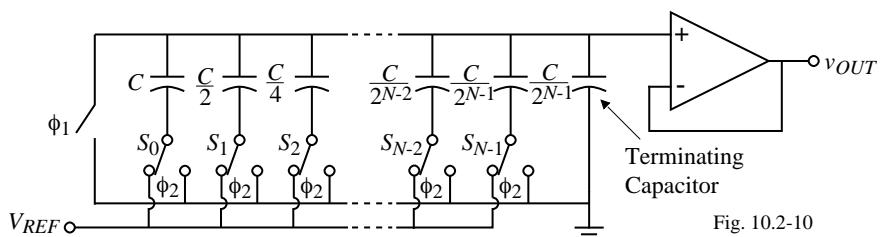
which gives

$$v_{OUT} = [b_0 2^{-1} + b_1 2^{-2} + b_2 2^{-3} + \dots + b_{N-1} 2^{-N}] V_{REF}$$

Equivalent circuit of the binary-weighted, charge scaling DAC is:

Attributes:

- Accurate
- Sensitive to parasitics
- Not monotonic
- Charge feedthrough occurs at turn on of switches



Integral Nonlinearity of the Charge Scaling DAC

Again, we use a worst case approach. Assume an n -bit charge scaling DAC with the *MSB* capacitor of C and the *LSB* capacitor of $C/2^{n-1}$ and the capacitors have a tolerance of $\Delta C/C$.

The ideal output when the i -th capacitor only is connected to V_{REF} is

$$v_{OUT}(\text{ideal}) = \frac{C/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \left(\frac{2^n}{2^n} \right) = \frac{2^n}{2^i} \text{ LSBs}$$

The maximum and minimum capacitance is $C_{max} = C + \Delta C$ and $C_{min} = C - \Delta C$. Therefore, the actual worst case output for the i -th capacitor is

$$v_{OUT}(\text{actual}) = \frac{(C \pm \Delta C)/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \pm \frac{\Delta C \cdot V_{REF}}{2^i C} = \frac{2^n}{2^i} \pm \frac{2^n \Delta C}{2^i C} \text{ LSBs}$$

Now, the *INL* for the i -th bit is given as

$$INL(i) = v_{OUT}(\text{actual}) - v_{OUT}(\text{ideal}) = \frac{\pm 2^n \Delta C}{2^i C} = \frac{2^{n-i} \Delta C}{C} \text{ LSBs}$$

Typically, the worst case value of i occurs for $i = 1$. Therefore, the worst case *INL* is

$INL = \pm 2^{n-1} \frac{\Delta C}{C} \text{ LSBs}$

Differential Nonlinearity of the Charge Scaling DAC

The worst case *DNL* for the binary weighted capacitor array is found when the *MSB* changes. The output voltage of the binary weighted capacitor array can be written as

$$v_{OUT} = \frac{C_{eq.}}{(2C - C_{eq.}) + C_{eq.}} V_{REF}$$

where C_{eq} are capacitors whose bits are 1 and $(2C - C_{eq})$ are capacitors whose bits are 0.

The worst case *DNL* can be expressed as

$$DNL = \frac{v_{step}(\text{worst case})}{v_{step}(\text{ideal})} - 1 = \frac{v_{OUT}(1000...) - v_{OUT}(0111...)}{LSB} - 1 \text{ LSBs}$$

The worst case choice for the capacitors is to choose C_1 larger by ΔC and the remaining capacitors smaller by ΔC giving,

$$C_1 = C + \Delta C, C_2 = \frac{1}{2}(C - \Delta C), \dots, C_{n-1} = \frac{1}{2^{n-2}}(C - \Delta C), C_n = \frac{1}{2^{n-1}}(C - \Delta C), \text{ and } C_{term} = \frac{1}{2^{n-1}}(C - \Delta C)$$

Note that $\sum_{i=2}^n C_i + C_{term} = C_2 + C_3 + \dots + C_{n-1} + C_n + C_{term} = C - \Delta C$

Differential Nonlinearity of the Charge Scaling DAC - Continued

$$\therefore v_{OUT}(1000...) = \left(\frac{C+\Delta C}{(C+\Delta C)+(C-\Delta C)} \right) V_{REF} = \left(\frac{C+\Delta C}{2C} V_{REF} \right)$$

$$= \left(\frac{C+\Delta C}{2C} V_{REF} \right) \frac{2^n}{2^n} = 2^n \left(\frac{C+\Delta C}{2C} \right) LSBs$$

and

$$v_{OUT}(0111...) = \left(\frac{(C-\Delta C) - C_{term}}{(C+\Delta C)+(C-\Delta C)} \right) V_{REF} = \frac{(C-\Delta C) - \frac{1}{2^{n-1}}(C-\Delta C)}{(C+\Delta C)+(C-\Delta C)} V_{REF}$$

$$= \left(\frac{C-\Delta C}{2C} \right) \left(1 - \frac{2}{2^n} \right) V_{REF} = \frac{2^n(C-\Delta C)}{2C} \left(1 - \frac{2}{2^n} \right) V_{REF} = 2^n \left(\frac{C-\Delta C}{2C} \right) \left(1 - \frac{2}{2^n} \right) LSBs$$

$$\therefore \frac{v_{OUT}(1000...) - v_{OUT}(0111...)}{LSB} - 1 LSBs = 2^n \left(\frac{C+\Delta C}{2C} \right) - 2^n \left(\frac{C-\Delta C}{2C} \right) \left(1 - \frac{2}{2^n} \right) - 1 = (2^n - 1) \frac{\Delta C}{C} LSBs$$

Therefore,

$$DNL = (2^n - 1) \frac{\Delta C}{C} LSBs$$

Example 350-2 - DNL and INL of a Binary Weighted Capacitor Array DAC

If the tolerance of the capacitors in an 8-bit, binary weighted, charge scaling DAC are $\pm 0.5\%$, find the worst case *INL* and *DNL*.

Solution

For the worst case *INL*, we get from above that

$$INL = (2^7)(\pm 0.005) = \pm 0.64 LSBs$$

For the worst case *DNL*, we can write that

$$DNL = (2^8 - 1)(\pm 0.005) = \pm 1.275 LSBs$$

Example 350-3 - Influence of Capacitor Ratio Accuracy on Number of Bits

Use the data shown to estimate the number of bits possible for a charge scaling DAC assuming a worst case approach for *INL* and that the worst conditions occur at the midscale (1 MSB).

Solution

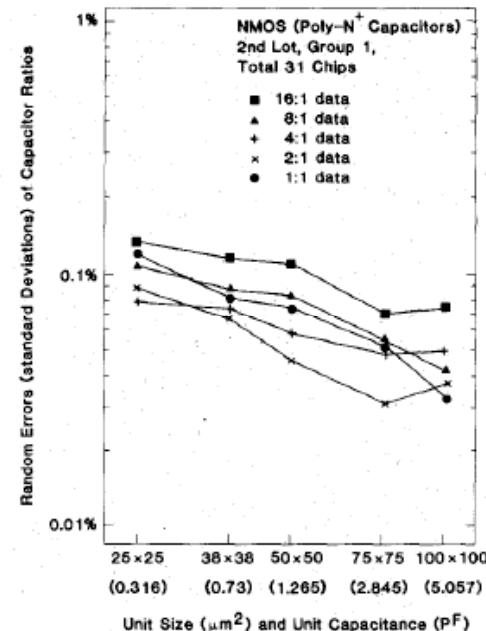
Assuming an *INL* of $\pm 0.5 \text{ LSB}$, we can write that

$$\text{INL} = \pm 2^{N-1} \frac{\Delta C}{C} \leq \pm \frac{1}{2} \rightarrow \left[\frac{\Delta C}{C} \right] = \frac{1}{2^N}$$

Let us assume a unit capacitor of $50 \mu\text{m} \times 50 \mu\text{m}$ by $50 \mu\text{m}$ and a relative accuracy of approximately $\pm 0.1\%$. Solving for N in the above equation gives approximately 10 bits. However, the $\pm 0.1\%$ figure corresponds to ratios of 16:1 or 4 bits. In order to get a solution, we estimate the relative accuracy of capacitor ratios as

$$\frac{\Delta C}{C} \approx 0.001 + 0.0001N$$

Using this approximate relationship, a 9-bit digital-analog converter should be realizable.



Binary Weighted, Charge Amplifier DAC

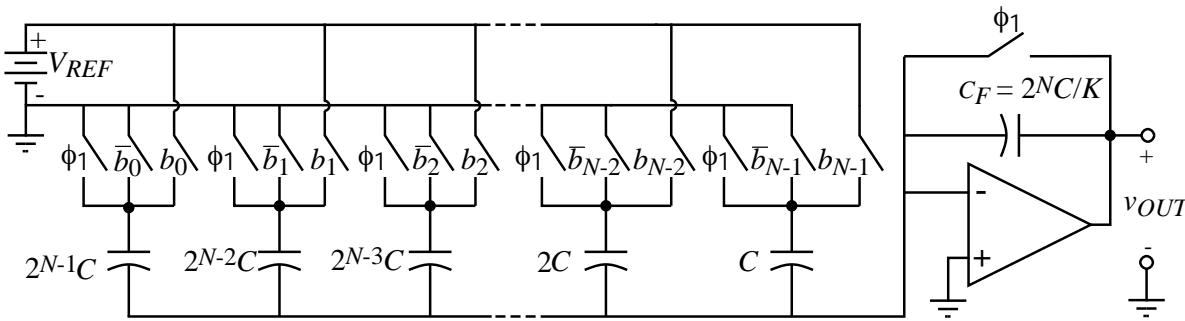


Fig. 10.2-12

Attributes:

- No floating nodes which implies insensitive to parasitics and fast
- No terminating capacitor required
- With the above configuration, charge feedthrough will be $\Delta V_{error} \approx -(COL/2CN)\Delta V$
- Can totally eliminate parasitics with parasitic-insensitive switched capacitor circuitry but not the charge feedthrough

EXTENDING THE RESOLUTION OF PARALLEL DIGITAL-ANALOG CONVERTERS

Background

Technique:

Divide the total resolution N into k smaller sub-DACs each with a resolution of $\frac{N}{k}$.

Result:

Smaller total area.

More resolution because of reduced largest to smallest component spread.

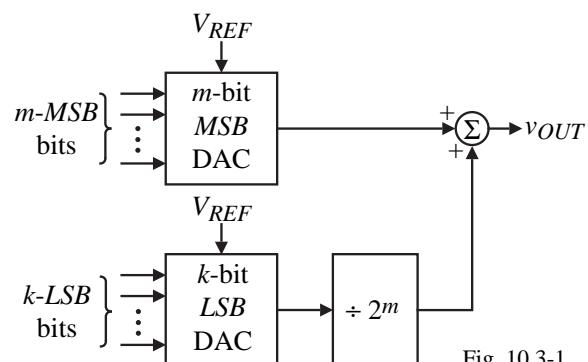
Approaches:

- Combination of similarly scaled subDACs
 - Divider approach (scale the analog output of the subDACs)
 - Subranging approach (scale the reference voltage of the subDACs)
- Combination of differently scaled subDACs

COMBINATION OF SIMILARLY SCALED SUBDACs

Analog Scaling - Divider Approach

Example of combining a m -bit and k -bit subDAC to form a $m+k$ -bit DAC.



$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \dots + \frac{b_{m-1}}{2^m} \right) V_{REF} + \left(\frac{1}{2^m} \left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \dots + \frac{b_{m+k-1}}{2^k} \right) V_{REF} \right)$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \dots + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k-1}}{2^{m+k}} \right) V_{REF}$$

Example 350-4 - Illustration of the Influence of the Scaling Factor

Assume that $m = 2$ and $k = 2$ in Fig. 10.3-1 and find the transfer characteristic of this DAC if the scaling factor for the *LSB* DAC is $3/8$ instead of $1/4$. Assume that $V_{REF} = 1V$. What is the $\pm INL$ and $\pm DNL$ for this DAC? Is this DAC monotonic or not?

Solution

The ideal DAC output is given as

$$v_{OUT} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{1}{4} \left(\frac{b_2}{2} + \frac{b_3}{4} \right) = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}.$$

The actual DAC output can be written as

$$v_{OUT}(\text{act.}) = \frac{b_0}{2} + \frac{b_1}{4} + \frac{3b_2}{16} + \frac{3b_3}{32} = \frac{16b_0}{32} + \frac{8b_1}{32} + \frac{6b_2}{32} + \frac{3b_3}{32}$$

The results are tabulated in the following table for this example.

Example 350-4 - Continued

Ideal and Actual Analog Output for the DAC in Ex. 350-4,

Input Digital Word	$v_{OUT}(\text{act.})$	v_{OUT}	$v_{OUT}(\text{act.}) - v_{OUT}$	Change in $v_{OUT}(\text{act.}) - 2/32$
0000	0/32	0/32	0/32	-
0001	3/32	2/32	1/32	1/32
0010	6/32	4/32	2/32	1/32
0011	9/32	6/32	3/32	1/32
0100	8/32	8/32	0/32	-3/32
0101	11/32	10/32	1/32	1/32
0110	14/32	12/32	2/32	1/32
0111	17/32	14/32	3/32	1/32
1000	16/32	16/32	0/32	-3/32
1001	19/32	18/32	1/32	1/32
1010	22/32	20/32	2/32	1/32
1011	25/32	22/32	3/32	1/32
1100	24/32	24/32	0/32	-3/32
1101	27/32	26/32	1/32	1/32
1110	30/32	28/32	2/32	1/32
1111	33/32	30/32	3/32	1/32

The table contains all the information we are seeking. An LSB for this example is $1/16$ or $2/32$. The fourth column gives the $+INL$ as $1.5LSB$ and the $-INL$ as $0LSB$. The fifth column gives the $+DNL$ as $-0.5LSB$ and the $-DNL$ as $-1.5LSB$. Because the $-DNL$ is greater than $-1LSB$, this DAC is non-monotonic.

Reference Scaling - Subranging Approach

Example of combining a m -bit and k -bit subDAC to form a $m+k$ -bit DAC.

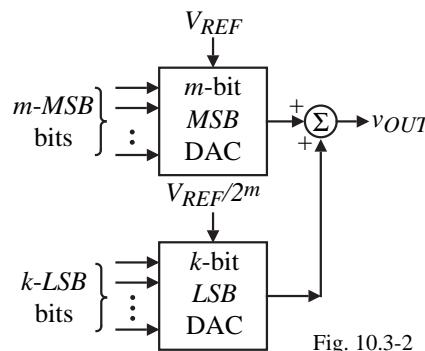


Fig. 10.3-2

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \dots + \frac{b_{m-1}}{2^m} \right) V_{REF} + \left(\frac{b_m}{2} + \frac{b_{m+1}}{4} + \dots + \frac{b_{m+k-1}}{2^k} \right) \left(\frac{V_{REF}}{2^m} \right)$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \dots + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k-1}}{2^{m+k}} \right) V_{REF}$$

Accuracy considerations of this method are similar to the analog scaling approach.

Advantage: There are no dynamic limitations associated with the scaling factor of $1/2^m$.

Current Scaling Dac Using Two SubDACs

Implementation:

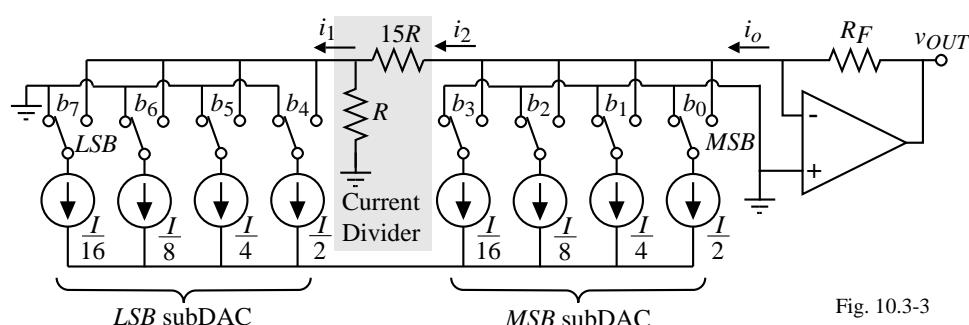
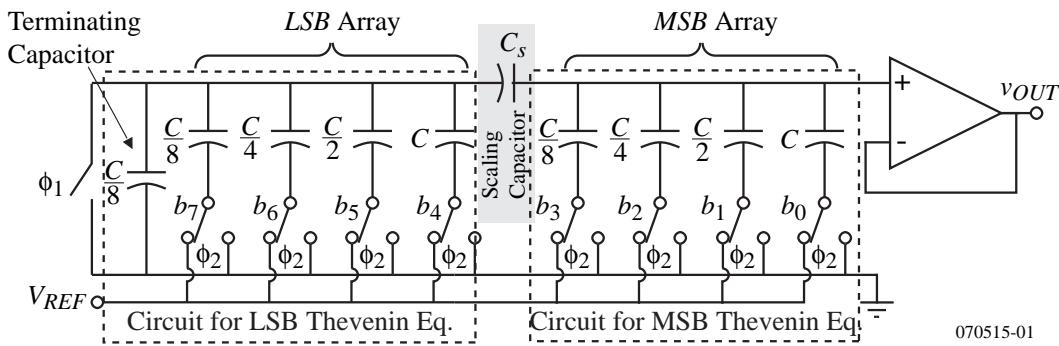


Fig. 10.3-3

$$v_{OUT} = R_F I \left[\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} \right) + \frac{1}{16} \left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16} \right) \right]$$

Charge Scaling DAC Using Two SubDACs

Implementation:



070515-01

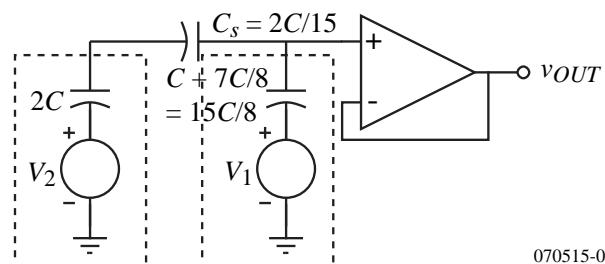
Design of the scaling capacitor, C_s :

The series combination of C_s and the *LSB* array must terminate the *MSB* array or equal $C/8$. Therefore, we can write

$$\frac{C}{8} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \quad \text{or} \quad \frac{1}{C_s} = \frac{8}{C} - \frac{1}{2C} = \frac{16}{2C} - \frac{1}{2C} = \frac{15}{2C}$$

Equivalent Circuit of the Charge Scaling Dac Using Two SubDACs

Simplified equivalent circuit:



070515-02

where the Thevenin equivalent voltage of the *MSB* array is

$$V_1 = \left[\left(\frac{1}{15/8} \right) b_0 + \left(\frac{1/2}{15/8} \right) b_1 + \left(\frac{1/4}{15/8} \right) b_2 + \left(\frac{1/8}{15/8} \right) b_3 \right] V_{REF} = \frac{16}{15} \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} \right) V_{REF}$$

and the Thevenin equivalent voltage of the *LSB* array is

$$V_2 = \left[\left(\frac{1/1}{2} \right) b_4 + \left(\frac{1/2}{2} \right) b_5 + \left(\frac{1/4}{2} \right) b_6 + \left(\frac{1/8}{2} \right) b_7 \right] V_{REF} = \left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16} \right) V_{REF}$$

Combining the elements of the simplified equivalent circuit above gives

$$v_{OUT} = \left(\frac{\frac{1}{2} + \frac{15}{2}}{\frac{1}{2} + \frac{15}{2} + 15} \right) V_1 + \left(\frac{\frac{8}{15}}{\frac{1}{2} + \frac{15}{2} + 15} \right) V_2 = \left(\frac{15+15 \cdot 15}{15+15 \cdot 15+16} \right) V_1 + \left(\frac{16}{15+15 \cdot 15+16} \right) V_2 = \frac{15}{16} V_1 + \frac{1}{16} V_2$$

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} + \frac{b_4}{32} + \frac{b_5}{64} + \frac{b_6}{128} + \frac{b_7}{256} \right) V_{REF} = \sum_{i=0}^7 \frac{b_i V_{REF}}{2^{i+1}}$$

Charge Amplifier DAC Using Two Binary Weighted Charge Amplifier SubDACs

Implementation:

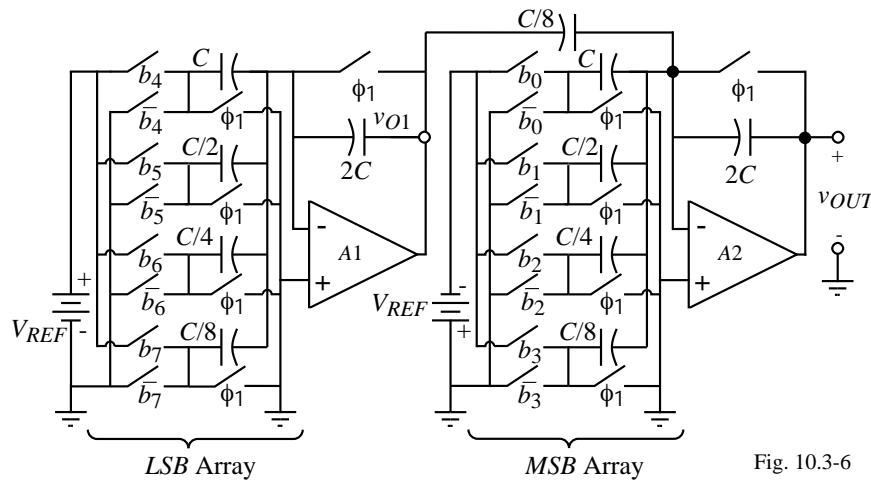


Fig. 10.3-6

Attributes:

- MSB subDAC is not dependent upon the accuracy of the scaling factor for the LSB subDAC.
- Insensitive to parasitics, fast
- Limited to op amp dynamics (GB)
- No ICMR problems with the op amp

COMBINATION OF DIFFERENTLY SCALED SUBDACs

Voltage Scaling MSB SubDAC And Charge Scaling LSB SubDAC

Implementation:

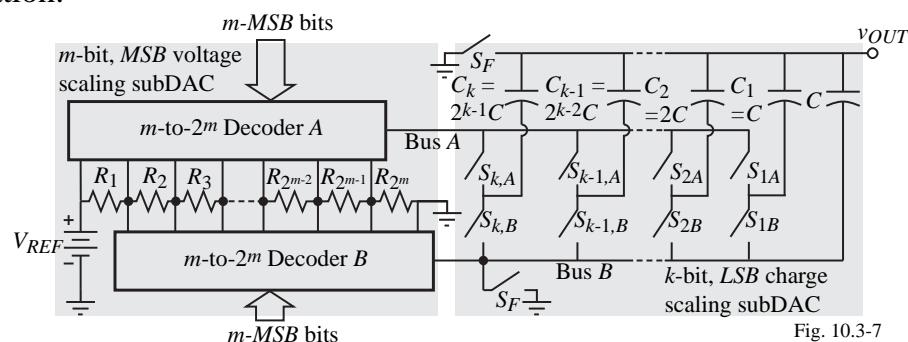


Fig. 10.3-7

Operation:

- 1.) Switches S_F and S_{1B} through $S_{k,B}$ discharge all capacitors.
- 2.) Decoders A and B connect Bus A and Bus B to the top and bottom, respectively, of the appropriate resistor as determined by the m -bits.
- 3.) The charge scaling subDAC divides the voltage across this resistor by capacitive division determined by the k -bits.

Attributes:

- MSB's are monotonic but the accuracy is poor
- Accuracy of LSBS is good

Voltage Scaling MSB SubDAC And Charge Scaling LSB SubDAC - Continued

Equivalent circuit of the voltage scaling (MSB) and charge scaling (LSB) DAC:

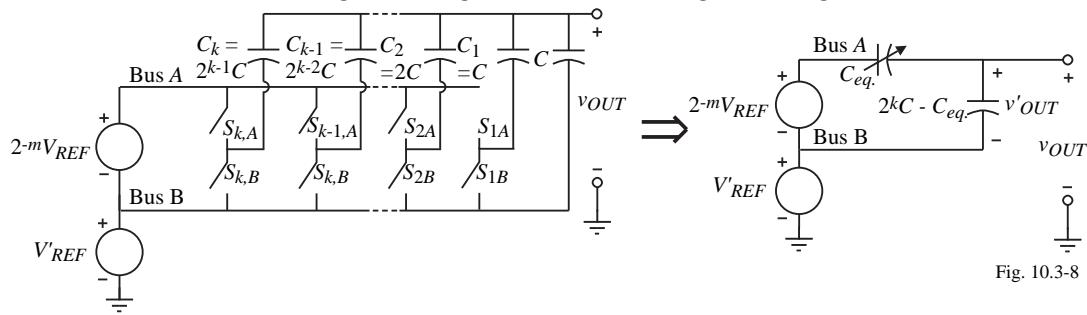


Fig. 10.3-8

where,

$$V'_{REF} = V_{REF} \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} \right)$$

and

$$v'_{OUT} = \frac{V_{REF}}{2^m} \left(\frac{b_m}{2} + \frac{b_{m+1}}{2^2} + \dots + \frac{b_{m+k}}{2^{k-1}} + \frac{b_{m+k-1}}{2^k} \right) = V_{REF} \left(\frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}} \right)$$

Adding V'_{REF} and v'_{OUT} gives the DAC output voltage as

$$v_{OUT} = V'_{REF} + v'_{OUT} = V_{REF} \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}} \right)$$

which is equivalent to an $m+k$ bit DAC.

Charge Scaling MSB SubDAC and Voltage Scaling LSB SubDAC

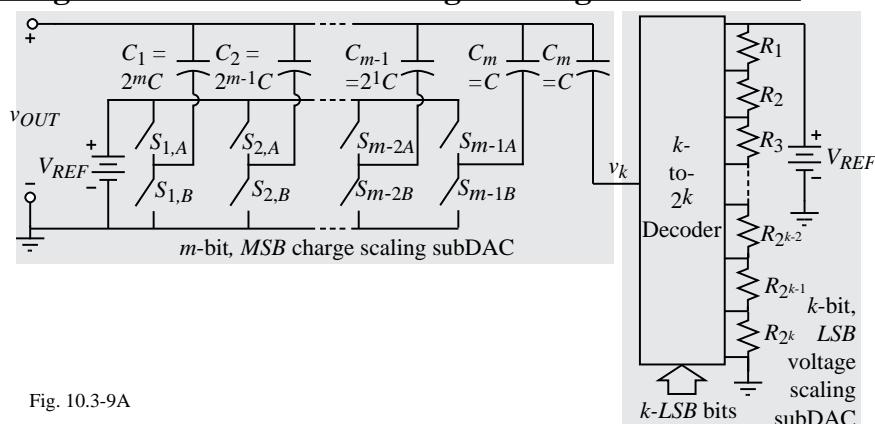


Fig. 10.3-9A

$$v_{OUT} = \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} \right) V_{REF} + \frac{v_k}{2^m} \quad \text{where} \quad v_k = \left(\frac{b_m}{2^1} + \frac{b_{m+1}}{2^2} + \dots + \frac{b_{m+k}}{2^{k-1}} + \frac{b_{m+k-1}}{2^k} \right) V_{REF}$$

$$\therefore v_{OUT} = \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \dots + \frac{b_{m-2}}{2^{m-1}} + \frac{b_{m-1}}{2^m} + \frac{b_m}{2^{m+1}} + \frac{b_{m+1}}{2^{m+2}} + \dots + \frac{b_{m+k}}{2^{m+k-1}} + \frac{b_{m+k-1}}{2^{m+k}} \right) V_{REF}$$

Attributes:

- *MSBs* have good accuracy
- *LSBs* are monotonic, have poor accuracy - require trimming for good accuracy

Tradeoffs in SubDAC Selection to Enhance Linearity Performance

Assume a m -bit MSB subDAC and a k -bit LSB subDAC.

MSB Voltage Scaling SubDAC and LSB Charge Scaling SubDAC ($n = m+k$)

INL and DNL of the m -bit MSB voltage-scaling subDAC:

$$INL(R) = 2^{m-1} \left(\frac{2^n}{2^m} \right) \frac{\Delta R}{R} = 2^{n-1} \frac{\Delta R}{R} LSBs \quad \text{and} \quad DNL(R) = \frac{\pm \Delta R}{R} \left(\frac{2^n}{2^m} \right) = 2^k \frac{\pm \Delta R}{R} LSBs$$

INL and DNL of the k -bit LSB charge-scaling subDAC:

$$INL(C) = 2^{k-1} \frac{\Delta C}{C} LSBs \quad \text{and} \quad DNL(C) = (2^{k-1}) \frac{\Delta C}{C} LSBs$$

Combining these relationships:

$$INL = INL(R) + INL(C) = \left(2^{n-1} \frac{\Delta R}{R} + 2^{k-1} \frac{\Delta C}{C} \right) LSBs$$

and $DNL = DNL(R) + DNL(C) = \left(2^k \frac{\Delta R}{R} + (2^{k-1}) \frac{\Delta C}{C} \right) LSBs$

MSB Charge Scaling SubDAC and LSB Voltage Scaling SubDAC

$$INL = INL(R) + INL(C) = \left(2^{k-1} \frac{\Delta R}{R} + 2^{n-1} \frac{\Delta C}{C} \right) LSBs$$

and $DNL = DNL(R) + DNL(C) = \left(\frac{\Delta R}{R} + (2^{n-1}) \frac{\Delta C}{C} \right) LSBs$

Example 350-5 - Design of a DAC using Voltage Scaling for MSBs and Charge Scaling for LSBs

Consider a 12-bit DAC that uses voltage scaling for the MSBs charge scaling for the LSBs. To minimize the capacitor element spread and the number of resistors, choose $m = 5$ and $k = 7$. Find the tolerances necessary for the resistors and capacitors to give an INL and DNL equal to or less than 2 LSB and 1 LSB, respectively.

Solution

Substituting $n = 12$ and $k = 7$ into the previous equations gives

$$2 = 2^{11} \frac{\Delta R}{R} + 2^6 \frac{\Delta C}{C} \quad \text{and} \quad 1 = 2^7 \frac{\Delta R}{R} + (2^7-1) \frac{\Delta C}{C}$$

Solving these two equations simultaneously gives

$$\frac{\Delta C}{C} = \frac{2^{11} - 2^6 - 2^7}{2^{11} - 2^6 - 2^7} = 0.0071 \rightarrow \frac{\Delta C}{C} = 0.71\%$$

$$\frac{\Delta R}{R} = \frac{2^7 - 2^6 - 2}{2^{11} - 2^6 - 2^7} = 0.0008 \rightarrow \frac{\Delta R}{R} = 0.075\%$$

We see that the capacitor tolerance will be easy to meet but that the resistor tolerance will require resistor trimming to meet the 0.075% requirement. Because of the 2^{n-1} multiplying $\Delta R/R$ in the relationship, we are stuck with approximately 0.075%. Therefore, choose $m = 2$ (which makes the 0.075% easier to achieve) and let $k = 10$ which gives $\Delta R/R = 0.083\%$ and $\Delta C/C = 0.12\%$.

Example 350-6 - Design of a DAC using Charge Scaling for MSBs and Voltage Scaling for LSBs

Consider a 12-bit DAC that uses charge scaling for the *MSBs* voltage scaling for the *LSBs*. To minimize the capacitor element spread and the number of resistors, choose $m = 7$ and $k = 5$. Find the tolerances necessary for the resistors and capacitors to give an *INL* and *DNL* equal to or less than 2 *LSB* and 1 *LSB*, respectively.

Solution

Substituting the values of this example into the relationships developed on a previous slide, we get

$$2 = 2^4 \frac{\Delta R}{R} + 2^{11} \frac{\Delta C}{C} \quad \text{and} \quad 1 = \frac{\Delta R}{R} + (2^{12}-1) \frac{\Delta C}{C}$$

Solving these two equations simultaneously gives

$$\frac{\Delta C}{C} = \frac{2^{4-2}}{2^{16}-2^{11}-2^4} = 0.000221 \rightarrow \frac{\Delta C}{C} = 0.0221\% \quad \text{and} \quad \frac{\Delta R}{R} \approx \frac{3}{2^{5-1}} = 0.0968 \rightarrow \frac{\Delta R}{R} = 9.68\%$$

For this example, the resistor tolerance is easy to meet but the capacitor tolerance will be difficult. To achieve accurate capacitor tolerances, we should decrease the value of m and increase the value of k to achieve a smaller capacitor value spread and thereby enhance the tolerance of the capacitors. If we choose $m = 4$ and $k = 8$, the capacitor tolerance is 0.049% and the resistor tolerance becomes 0.79% which is still reasonable. The largest to smallest capacitor ratio is 8 rather than 64 which helps to meet the capacitor tolerance requirements.

SERIAL DIGITAL-ANALOG CONVERTERS

Serial DACs

- Typically require one clock pulse to convert one bit
- Types considered here are:
Charge-redistribution
Algorithmic

Charge Redistribution DAC

Implementation:

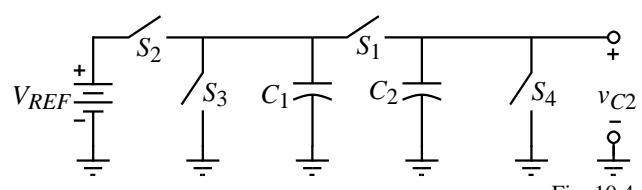


Fig. 10.4-1

Operation:

Switch S_1 is the redistribution switch that parallels C_1 and C_2 sharing their charge

Switch S_2 precharges C_1 to V_{REF} if the i th bit, b_i , is a 1

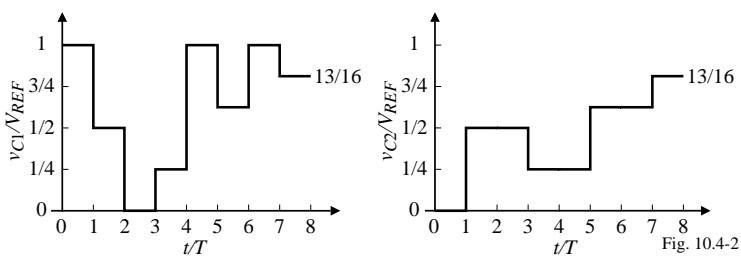
Switch S_3 discharges C_1 to zero if the i th bit, b_i , is a 0

Switch S_4 is used at the beginning of the conversion process to initially discharge C_2

Conversion always begins with the *LSB* bit and goes to the *MSB* bit.

Example 350-7 - Operation of the Serial, Charge Redistribution DAC

Assume that $C_1 = C_2$ and that the digital word to be converted is given as $b_0 = 1, b_1 = 1, b_2 = 0$, and $b_3 = 1$. Follow through the sequence of events that result in the conversion of this digital input word.



Solution

- 1.) S_4 closes setting $v_{C2} = 0$.
- 2.) $b_3 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
- 3.) Switch S_1 is closed causing $v_{C1} = v_{C2} = 0.5V_{REF}$.
- 4.) $b_2 = 0$, closes switch S_3 , causing $v_{C1} = 0V$.
- 5.) S_1 closes, the voltage across both C_1 and C_2 is $0.25V_{REF}$.
- 6.) $b_1 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
- 7.) S_1 closes, the voltage across both C_1 and C_2 is $(1+0.25)/2V_{REF} = 0.625V_{REF}$.
- 8.) $b_0 = 1$, closes switch S_2 causing $v_{C1} = V_{REF}$.
- 9.) S_1 closes, the voltage across both C_1 and C_2 is $(0.625 + 1)/2V_{REF} = 0.8125V_{REF} = (13/16)V_{REF}$.

Pipeline DAC

The pipeline DAC is simply an extension of the sub-DACs concept to the limit where the bits converted by each sub-DAC is 1.

Implementation:

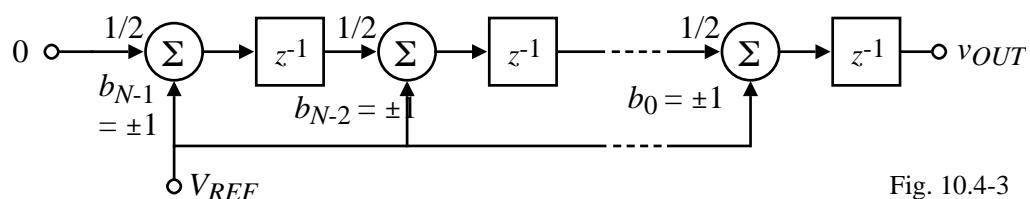


Fig. 10.4-3

$$V_{out}(z) = [b_0 z^{-1} + 2^{-1} b_1 z^{-2} + \dots + 2^{-(N-2)} b_{N-2} z^{-(N-1)} + b_{N-1} z^{-N}] V_{REF}$$

where b_i is either ± 1 if the i th bit is high or low. The z^{-1} blocks represent a delay of one clock period between the 1-bit sub-DACs.

Attributes:

- Takes $N+1$ clock cycles to convert the digital input to an analog output
- However, a new analog output is converted every clock after the initial $N+1$ clocks

Algorithmic (Iterative) DAC

Implementation:

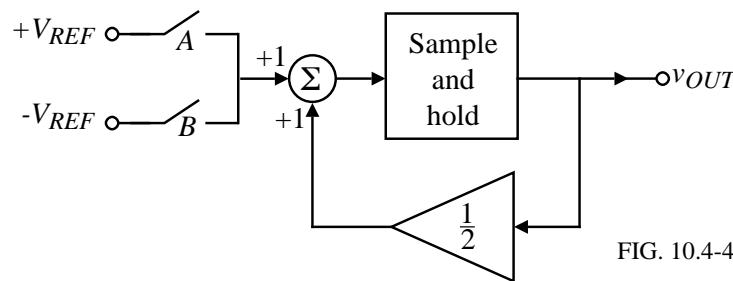


FIG. 10.4-4

Closed form of the previous series expression is,

$$V_{out}(z) = \frac{b_i z^{-1} V_{REF}}{1 - 0.5 z^{-1}}$$

Operation:

Switch *A* is closed when the *i*th bit is 1 and switch *B* is closed when the *i*th bit is 0.
Start with the *LSB* and work to the *MSB*.

Example 350-8 - Digital-Analog Conversion Using the Algorithmic Method

Assume that the digital word to be converted is 11001 in the order of *LSB* to *MSB*. Find the converted output voltage and sketch a plot of v_{OUT}/V_{REF} as a function of t/T where T is the period for one conversion.

Solution

- 1.) The conversion starts by zeroing the output (not shown on Fig. 10.4-4).
- 2.) The *LSB* = 1, switch *A* is closed and V_{REF} is summed with zero to give an output of $+V_{REF}$.
- 3.) The next *LSB* = 0, switch *B* is closed and $v_{OUT} = -V_{REF} + 0.5V_{REF} = -0.5V_{REF}$.
- 4.) The next *LSB* = 0, switch *B* is closed and $v_{OUT} = -V_{REF} + 0.5(-0.5V_{REF}) = -1.25V_{REF}$.
- 5.) The next *LSB* = 1, switch *A* is closed and $v_{OUT} = V_{REF} + 0.5(-1.25V_{REF}) = 0.375V_{REF}$.
- 6.) The *MSB* = 1, switch *A* is closed and $v_{OUT} = V_{REF} + 0.5(0.375V_{REF}) = 1.1875V_{REF} = (19/16)V_{REF}$. (Note that because the actual V_{REF} of this example is $\pm V_{REF}$ or $2V_{REF}$, the analog value of the digital word 11001 is 19/32 times $2V_{REF}$ or $(19/16)V_{REF}$.)

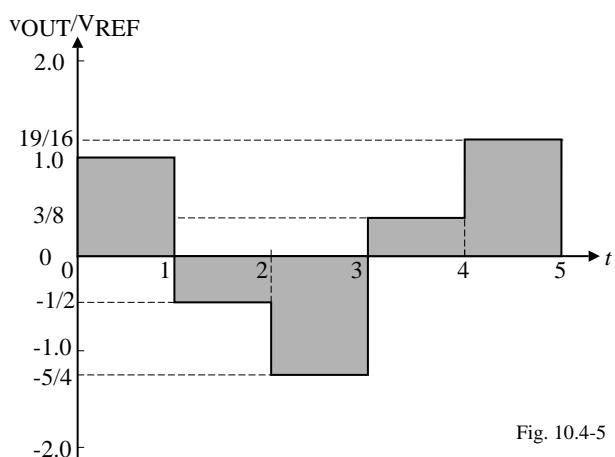


Fig. 10.4-5

SUMMARY

- Voltage scaling DACs are monotonic, use equal resistors but are sensitive to capacitive parasitics
- Charge scaling DACs are fast with good accuracy but have large element spread and are nonmonotonic
- DAC resolution can be increased by combining several subDACs with smaller resolution
- Methods of combining include scaling the output or the reference of the non-*MSB* subDACs
- SubDACs can use similar or different scaling methods
- Tradeoffs in the number of bits per subDAC and the type of subDAC allow minimization of the *INL* and *DNL*
- Serial, charge redistribution DAC is simple and requires minimum area but is slow and requires complex external circuitry
- Serial, algorithmic DAC is simple and requires minimum area but is slow and requires complex external circuitry

LECTURE 360 – CHARACTERIZATION OF ADCS AND SAMPLE AND HOLD CIRCUITS

LECTURE ORGANIZATION

Outline

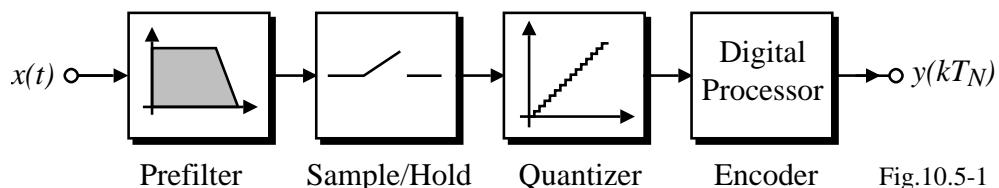
- Introduction to ADCs
- Static characterization of ADCs
- Dynamic characteristics of ADCs
- Sample and hold circuits
- Design of a sample and hold
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 652-665

INTRODUCTION

General Block Diagram of an Analog-Digital Converter



- Prefilter - Avoids the aliasing of high frequency signals back into the baseband of the ADC
- Sample-and-hold - Maintains the input analog signal constant during conversion
- Quantizer - Finds the subrange that corresponds to the sampled analog input
- Encoder - Encoding of the digital bits corresponding to the subrange

Nyquist Frequency Analog-Digital Converters

The sampled nature of the ADC places a practical limit on the bandwidth of the input signal. If the sampling frequency is f_S , and f_B is the bandwidth of the input signal, then

$$f_B < 0.5f_S$$

which is simply the *Nyquist* relationship which states that to avoid aliasing, the sampling frequency must be greater than twice the highest signal frequency.

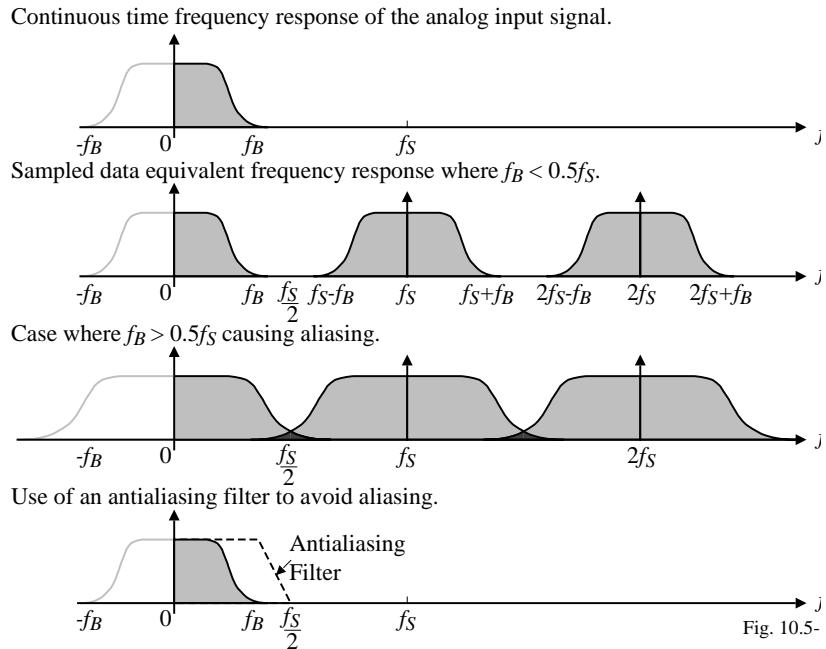


Fig. 10.5-

Classification of Analog-Digital Converters

Analog-digital converters can be classified by the relationship of f_B and $0.5f_S$ and by their conversion rate.

- *Nyquist ADCs* - ADCs that have f_B as close to $0.5f_S$ as possible.
- *Oversampling ADCs* - ADCs that have f_B much less than $0.5f_S$.

Classification of Analog-to-Digital Converter Architectures

Conversion Rate	Nyquist ADCs	Oversampled ADCs
Slow	Integrating (Serial)	Very high resolution <14-16 bits
Medium	Successive Approximation 1-bit Pipeline Algorithmic	Moderate resolution <10-12 bits
Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution < 6-8 bits

STATIC CHARACTERIZATION OF ANALOG-TO-DIGITAL CONVERTERS

Digital Output Codes

Digital Output Codes used for ADCs

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Input-Output Characteristics

Ideal input-output characteristics of a 3-bit ADC

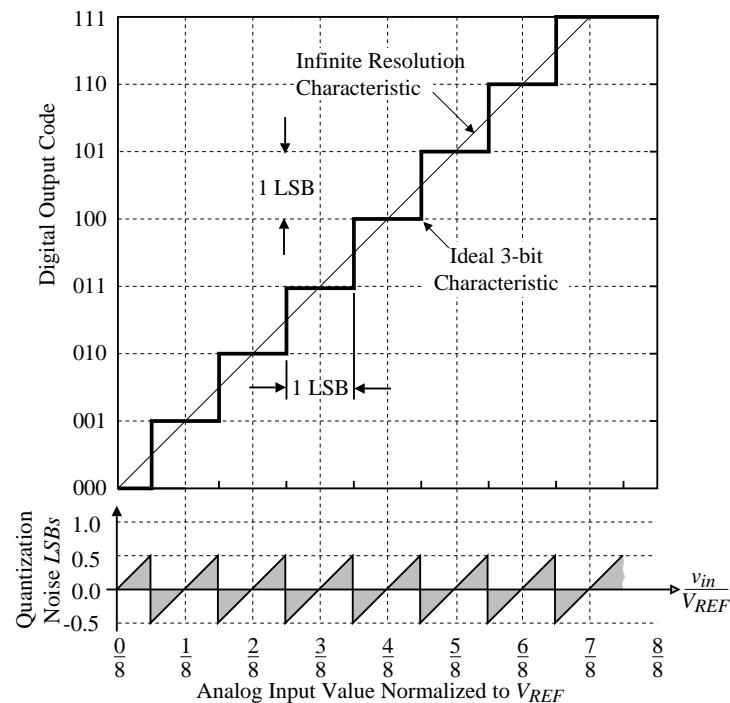


Figure 10.5-3 Ideal input-output characteristics of a 3-bit ADC.

Definitions

- The *dynamic range, signal-to-noise ratio (SNR)*, and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC
- Resolution* of the ADC is the smallest analog change that distinguishable by an ADC.
- Quantization Noise* is the $\pm 0.5LSB$ uncertainty between the infinite resolution characteristic and the actual characteristic.
- Offset Error* is the difference between the ideal finite resolution characteristic and actual finite resolution characteristic
- Gain Error* is the difference between the ideal finite resolution characteristic and actual finite resolution measured at full-scale input. This difference is *proportional* to the analog input voltage.

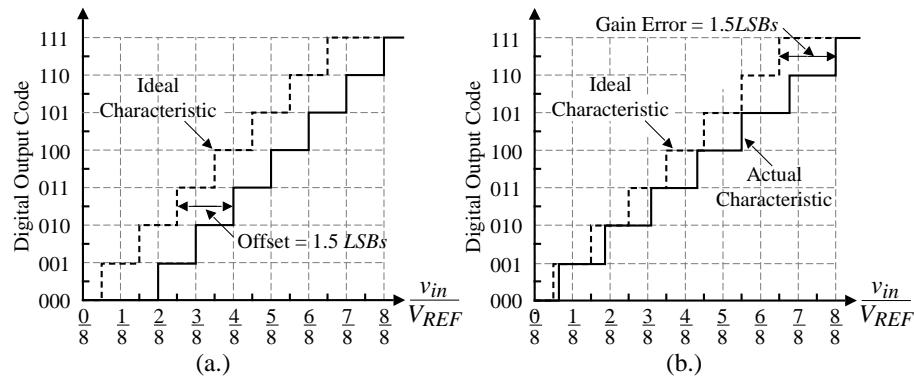


Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

Integral and Differential Nonlinearity

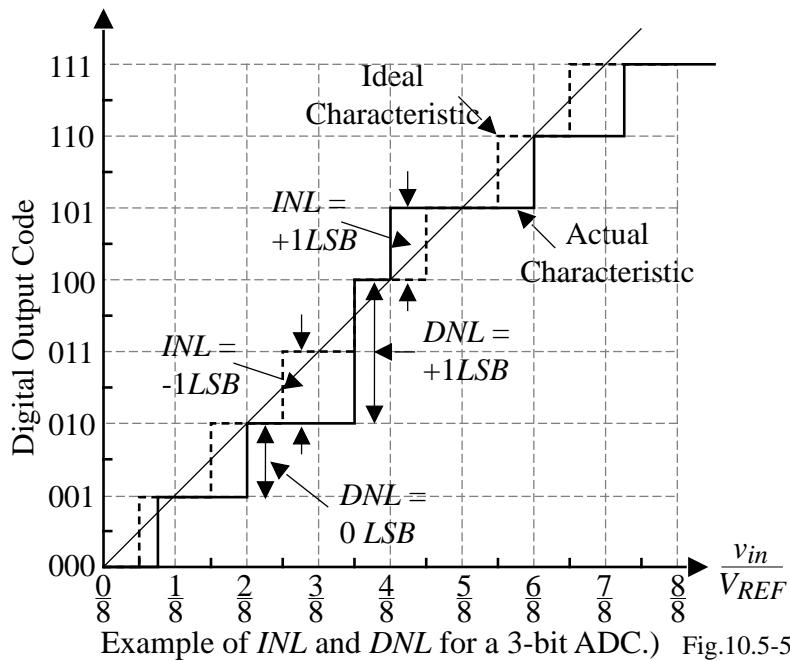
- The integral and differential nonlinearity of the ADC are referenced to the vertical (digital) axis of the transfer characteristic.
- Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)
 - Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical step (% or *LSB*).

$$DNL = (D_{cx} - 1) \text{ LSBs}$$

where D_{cx} is the size of the actual vertical step in *LSBs*.

Note that *INL* and *DNL* of an analog-digital converter will be in terms of integers in contrast to the *INL* and *DNL* of the digital-analog converter. As the resolution of the ADC increases, this restriction becomes insignificant.

Example of INL and DNL



Example of INL and DNL for a 3-bit ADC.) Fig.10.5-5

Note that the DNL and INL errors can be specified over some range of the analog input.

Monotonicity

A *monotonic* ADC has all vertical jumps positive. Note that monotonicity can only be detected by *DNL*.

Example of a nonmonotonic ADC:

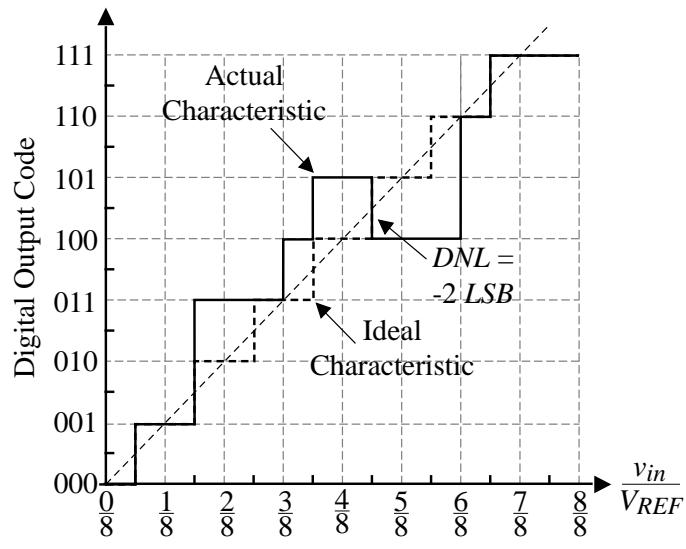


Fig. 10.5-6L

If a vertical jump is 2LSB or greater, missing output codes may result.

If a vertical jump is -1LSB or less, the ADC is not monotonic.

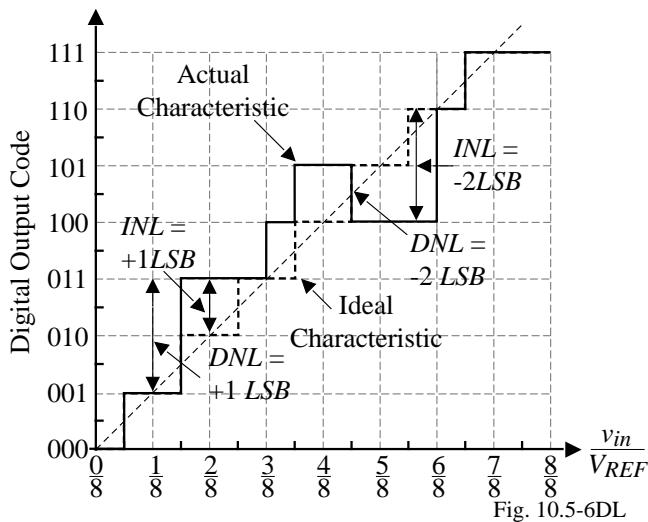
Example 360-1 - INL and DNL of a 3-bit ADC

Find the *INL* and *DNL* for the 3-bit ADC shown on the previous slide.

Solution

With respect to the digital axis:

- 1.) The largest value of *INL* for this 3-bit ADC occurs between $3/16$ to $5/16$ or $7/16$ to $9/16$ and is $1LSB$.
- 2.) The smallest value of *INL* occurs between $11/16$ to $12/16$ and is $-2LSB$.
- 3.) The largest value of *DNL* occurs at $3/16$ or $6/8$ and is $+1LSB$.
- 4.) The smallest value of *DNL* occurs at $9/16$ and is $-2LSB$ which is where the converter becomes nonmonotonic.



DYNAMIC CHARACTERISTICS OF ADCs

What are the Important Dynamic Characteristics for ADCs?

The dynamic characteristics of ADCs are influenced by:

- Comparators
 - Linear response
 - Slew response
- Sample-hold circuits
- Circuit parasitics
- Logic propagation delay

Comparator

The comparator is the quantizing unit of ADCs.

Open-loop model:

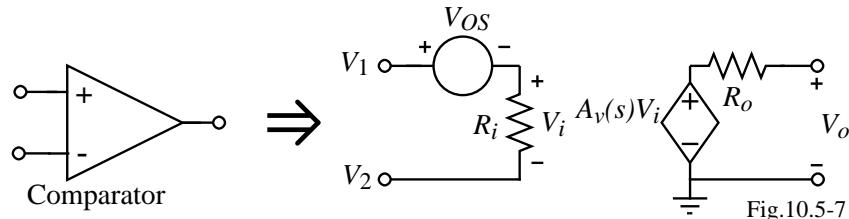


Fig.10.5-7

Nonideal aspects:

- Input offset voltage, V_{OS} (a static characteristic)
- Propagation time delay

- Bandwidth (linear)

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1}$$

- Slew rate (nonlinear)

$$\Delta T = \frac{C \cdot \Delta V}{I} \quad (I \text{ constant}) = \frac{\Delta V}{\text{Slew Rate}}$$

SAMPLE AND HOLD CIRCUITS

Requirements of a Sample and Hold Circuit

The objective of the sample and hold circuit is to sample the unknown analog signal and hold that sample while the ADC decodes the digital equivalent output.

The sample and hold circuit must:

- 1.) Have the accuracy required for the ADC resolution, i.e. accuracy = $\frac{100\%}{2^N}$
- 2.) The sample and hold circuit must be fast enough to work in a two-phase clock. For an ADC with a 100 Megasample/second sample rate, this means that the sample and hold must perform its function within 5 nanoseconds.
- 3.) Precisely sample the analog signal at the same time for each clock. An advantage of the sample and hold circuit is that it removes the precise timing requirements from the ADC itself.
- 4.) The power dissipation of the sample and hold circuit must be small. Unfortunately, the above requirements for accuracy and speed will mean that the power must be increased as the bits are increased and/or the clock period reduced.

Sample-and-Hold Circuit

Waveforms of a sample-and-hold circuit:

Definitions:

- *Acquisition time (t_a)* = time required to acquire the analog voltage
- *Settling time (t_s)* = time required to settle to the final held voltage to within an accuracy tolerance

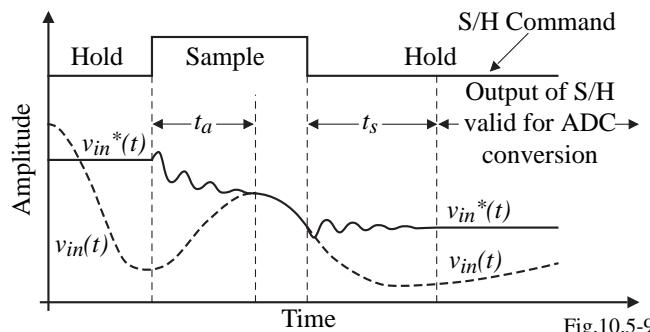


Fig.10.5-9

$$\therefore T_{sample} = t_a + t_s \quad \rightarrow \quad \text{Maximum sample rate} = f_{sample}(\max) = \frac{1}{T_{sample}}$$

Other considerations:

- *Aperture time* = the time required for the sampling switch to open after the S/H command is initiated
- *Aperture jitter* = variation in the aperture time due to clock variations and noise

Types of S/H circuits:

- No feedback - faster, less accurate
- Feedback - slower, more accurate

Open-Loop, Buffered S/H Circuit

Circuit:

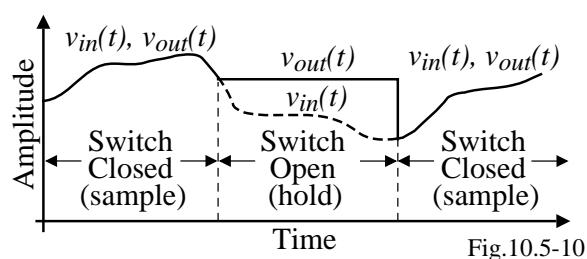
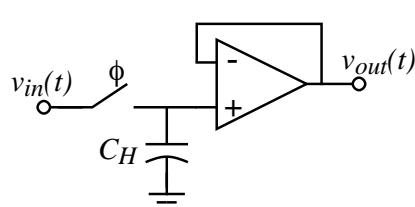


Fig.10.5-10

Attributes:

- Fast, open-loop
- Requires current from the input to charge C_H
- DC voltage offset of the op amp and the charge feedthrough of the switch will create dc errors

Settling Time

Assume the op amp has a dominant pole at $-\omega_a$ and a second pole at $-GB$.

The unity-gain response can be approximated as, $A(s) \approx \frac{GB^2}{s^2 + GB \cdot s + GB^2}$

The resulting step response is, $v_{out}(t) = 1 - \left(\sqrt{\frac{4}{3}} e^{-0.5GB \cdot t} \right) \sin\left(\sqrt{\frac{3}{4}} GB \cdot t + \phi\right)$

Defining the error as the difference between the final normalized value and $v_{out}(t)$, gives,

$$\text{Error}(t) = \epsilon = 1 - v_{out}(t) = \sqrt{\frac{4}{3}} e^{-0.5GB \cdot t}$$

In most ADCs, the error is equal to $\pm 0.5LSB$. Since the voltage is normalized,

$$\frac{1}{2^{N+1}} = \sqrt{\frac{4}{3}} e^{-0.5GB \cdot t_s} \rightarrow e^{-0.5GB \cdot t_s} = \frac{4}{\sqrt{3}} 2^N$$

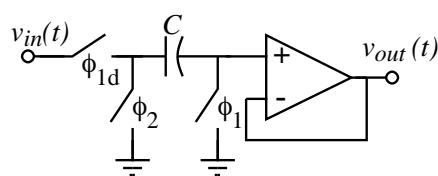
Solving for the time, t_s , required to settle with $\pm 0.5LSB$ from the above equation gives

$$t_s = \frac{2}{GB} \ln\left(\frac{4}{\sqrt{3}} 2^N\right) = \frac{1}{GB} [1.3863N + 1.6740]$$

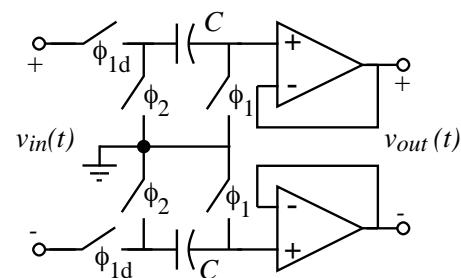
Thus as the resolution of the ADC increases, the settling time for any unity-gain buffer amplifiers will increase. For example, if we are using the open-loop, buffered S/H circuit in a 10 bit ADC, the amount of time required for the unity-gain buffer with a GB of 1MHz to settle to within 10 bit accuracy is $2.473\mu\text{s}$.

Open-Loop, Switched-Capacitor S/H Circuit

Circuit:



Switched capacitor S/H circuit.



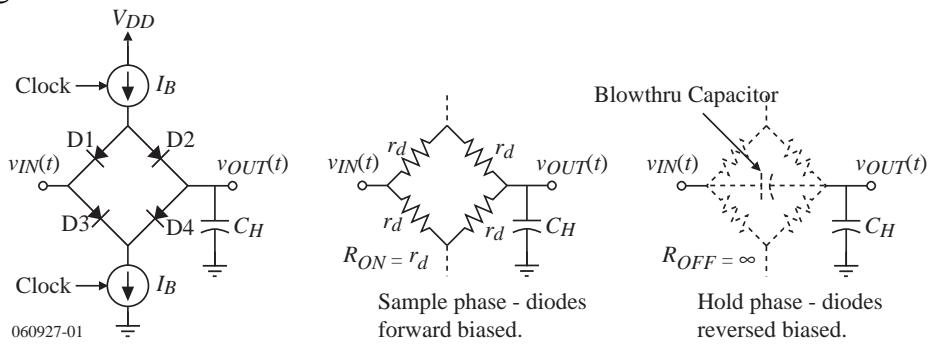
Differential switched-capacitor S/H

Fig.10.5-11

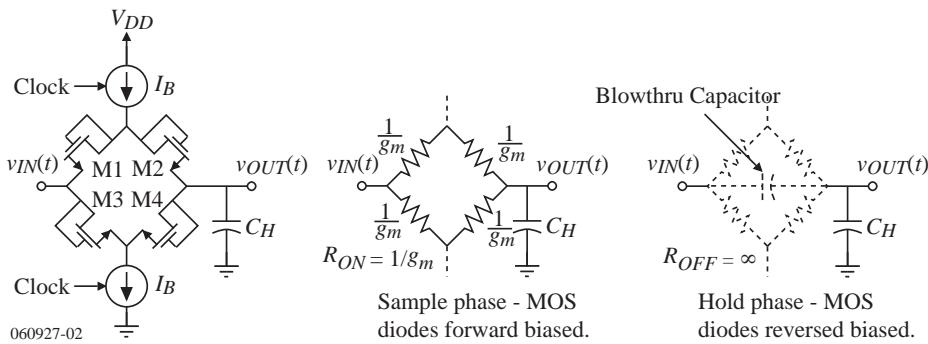
- Delayed clock used to remove input dependent feedthrough.
- Differential version has lower $PSRR$, cancellation of even harmonics, and reduction of charge injection and clock feedthrough

Open-Loop, Diode Bridge S/H Circuit

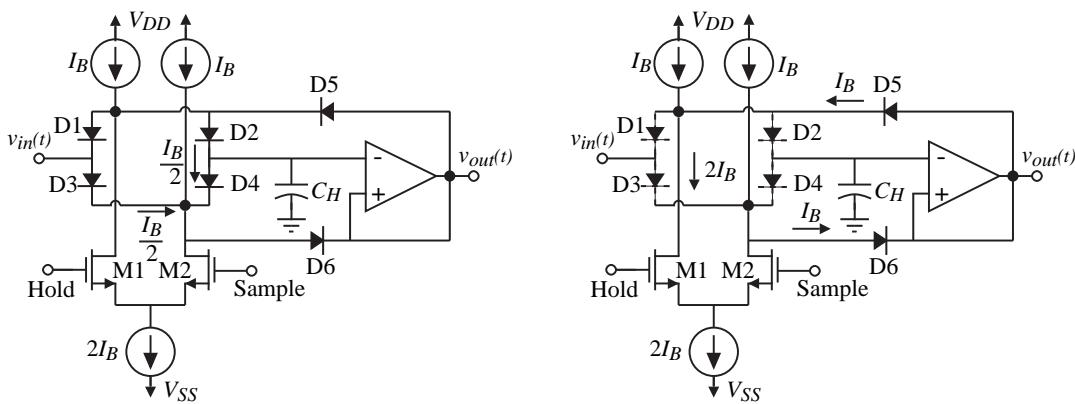
Diode bridge S/H circuit:



MOS diode bridge S/H circuit:



Practical Implementation of the Diode Bridge S/H Circuit



Practical implementation of the diode bridge sample and hold (sample mode).

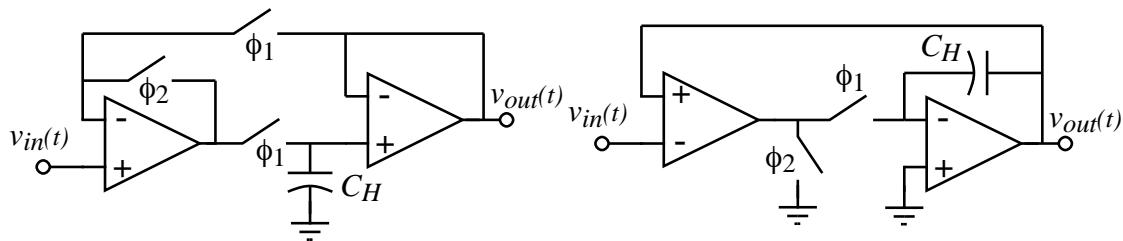
Hold mode.

060927-03

During the hold mode, the diodes D5 and D6 become forward biased and clamp the upper and lower nodes of the sampling bridge to the sampled voltage.

Closed-Loop S/H Circuit

Circuit:



Closed-loop S/H circuit. ϕ_1 is the sample phase and ϕ_2 is the hold phase.

An improved version.

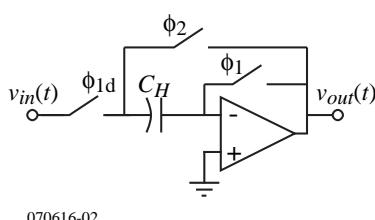
Fig.10.5-13

Attributes:

- Accurate
- First circuit has signal-dependent feedthrough
- Slower because of the op amp feedback loop

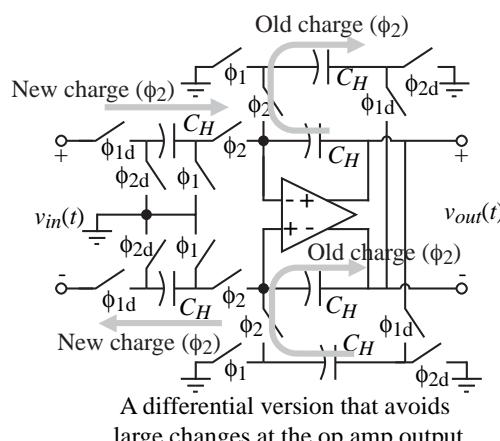
Closed-Loop, Switched Capacitor S/H Circuits

Circuit:



070616-02

Switched capacitor S/H circuit which autozeroses the op amp input offset voltage.



A differential version that avoids large changes at the op amp output

Attributes:

- Accurate
- Signal-dependent feedthrough eliminated by a delayed clock
- Differential circuit keeps the output of the op amps constant during the ϕ_1 phase avoiding slew rate limits

Current-Mode S/H Circuit

Circuit:

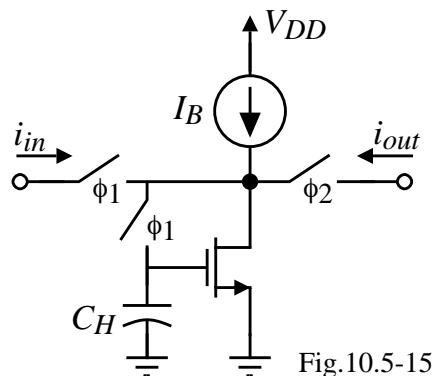


Fig.10.5-15

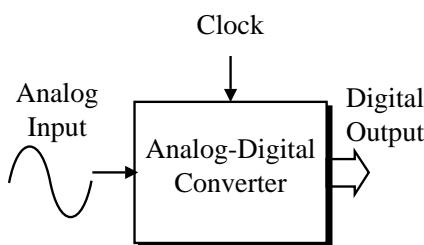
Attributes:

- Fast
- Requires current in and out
- Good for low voltage implementations

Aperature Jitter in S/H Circuits

Illustration:

If we assume that $v_{in}(t) = V_p \sin \omega t$, then the maximum slope is equal to ωV_p .



Therefore, the value of ΔV is given as

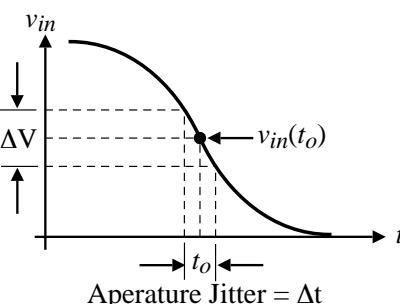


Figure 10.5-14 - Illustration of aperature jitter in an ADC.

$$\Delta V = \left| \frac{dv_{in}}{dt} \right| \Delta t = \omega V_p \Delta t .$$

The rms value of this noise is given as

$$\Delta V(\text{rms}) = \left| \frac{dv_{in}}{dt} \right| \Delta t = \frac{\omega V_p \Delta t}{\sqrt{2}} .$$

The aperature jitter can lead to a limitation in the desired dynamic range of an ADC. For example, if the aperature jitter of the clock is 100ps, and the input signal is a full scale peak-to-peak sinusoid at 1MHz, the rms value of noise due to this aperature jitter is $111\mu\text{V}(\text{rms})$ if the value of $V_{REF} = 1\text{V}$.

DESIGN OF A SAMPLE AND HOLD AMPLIFIER

Specifications

Accuracy = 10 bits

Clock frequency is 10 MHz

Power dissipation $\leq 1\text{mW}$

Signal level is from 0 to 1V

Slew rate $\geq 100\text{V}/\mu\text{s}$ with $C_L = 1\text{pF}$

Use $0.25\mu\text{m}$ CMOS

Technology Parameters ($C_{ox} = 60.6 \times 10^{-4} \text{ F/m}^2$):

Parameter Symbol	Parameter Description	Typical Parameter Value		Units
		N-Channel	P-Channel	
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.5 ± 0.15	-0.5 ± 0.15	V
K'	Transconductance Parameter (in saturation)	$120.0 \pm 10\%$	$25.0 \pm 10\%$	$\mu\text{A}/\text{V}^2$
γ	Bulk threshold parameter	0.4	0.6	$(\text{V})^{1/2}$
λ	Channel length modulation parameter	$0.32 (L=L_{min})$ $0.06 (L \geq 2L_{min})$	$0.56 (L=L_{min})$ $0.08 (L \geq 2L_{min})$	$(\text{V})^{-1}$
$2 \phi_F $	Surface potential at strong inversion	0.7	0.8	V

Op Amp Design

Gain:

$$\text{Gain error} = \frac{1}{1 + \text{Loop Gain}} \leq 0.5 \text{ LSB} = \frac{1}{2^{11}}$$

Therefore, the op amp gain $\geq 2^{11} = 2048 \text{ V/V}$

Choose the op amp gain as $\geq 5000 \text{ V/V}$

Gainbandwidth:

For a dominant pole op amp with unity-gain feedback, the relationship between the gain-bandwidth (GB), accuracy (N) and speed (t_s) is

$$t_s = \left(\frac{N+1}{GB} \right) \ln(2) = 0.693 \left(\frac{N+1}{GB} \right)$$

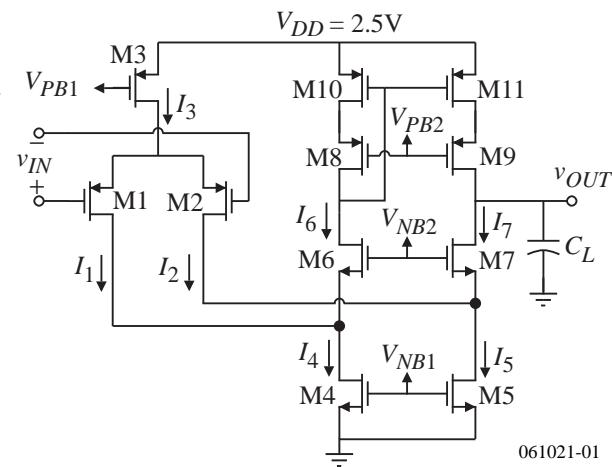
Therefore, if $t_s \leq 0.5 T_{clock} = 50 \text{ ns}$ (choose $t_s = 10 \text{ ns}$). For $N = 10$, the gain-bandwidth is

$$GB = 0.762 \times 10^9 = 120 \text{ MHz}$$

Dominant pole is 24 kHz and with an output capacitance of 1pF this means the output resistance of the op amp must be $\geq 6.6 \text{ M}\Omega$.

Op Amp Design – Continued

The previous specifications suggest a self-compensated op amp. The gain and output resistance should be easy to achieve with a cascaded output. A folded-cascode op amp is proposed for the design. In order to have the 0-1V signal range, a *p*-channel, differential input is selected. This will give the input 0-1V range. The output will effectively be 0-1V with the unity gain feedback around the op amp.



Bias Currents:

The $100\text{V}/\mu\text{s}$ slew rate requires $I_3 = 100\mu\text{A}$. Setting $I_4 = I_5 = 125\mu\text{A}$ gives a power dissipation of 0.875mW with $V_{DD} = 2.5\text{V}$.

Op Amp Design – Continued

Transistor sizes:

Design M4-M7 to give a saturation voltage of 0.1V with $125\mu\text{A}$.

$$\therefore \frac{W_4}{L_4} = \frac{W_5}{L_5} = \frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{2I_D}{K_n \cdot V_{DS(\text{sat})}^2} = \frac{2 \cdot 125}{120 \cdot 0.01} \approx \underline{\underline{200}}$$

Since the upper swing is not as important, choose a saturation voltage of 0.25V for M8 – M11.

$$\therefore \frac{W_8}{L_8} = \frac{W_9}{L_9} = \frac{W_{10}}{L_{10}} = \frac{W_{11}}{L_{11}} = \frac{2I_D}{K_p \cdot V_{DS(\text{sat})}^2} = \frac{2 \cdot 125}{25 \cdot 0.0625} = \underline{\underline{160}}$$

To get the GB of 120 MHz , this implies the g_m of M1 and M2 is

$$g_m = GB \cdot C_L = (120 \times 10^6 \cdot 2\pi)(10^{-12}) = 762 \mu\text{S}$$

$$\therefore \frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_m^2}{2I_D K_p} = \frac{762 \cdot 762}{2 \cdot 25 \cdot 50} = \underline{\underline{232}}$$

Let the upper input common mode voltage be 1.5V which gives the W/L of M3 as,

$$1\text{V} = V_{SG1} + V_{SD3} = 0.631 + V_{SD3} \Rightarrow V_{SD3} = 0.369\text{V} \Rightarrow \frac{W_3}{L_3} \approx \underline{\underline{60}}$$

Op Amp Design – Continued

We now need to check the output resistance and the gain to make sure the specifications are satisfied. Let us choose twice minimum channel length to keep the capacitive parasitics minimized and not have the output resistance too small. Therefore at quiescent conditions,

$$r_{ds5} = 133\text{k}\Omega, r_{ds7} = 222\text{k}\Omega, g_{m7} = 1.935\text{mS} \text{ and } r_{ds2} = 250\text{k}\Omega$$

$$\therefore R_{outdown} \approx (r_{ds5}||r_{ds2})g_{m7}r_{ds7} = 37.29\text{M}\Omega$$

$$r_{ds9} = r_{ds11} = 167\text{k}\Omega, \text{ and } g_{m11} = 1.697\text{mS}$$

$$\therefore R_{outup} \approx r_{ds11}g_{m9}r_{ds9} = 47.33\text{M}\Omega$$

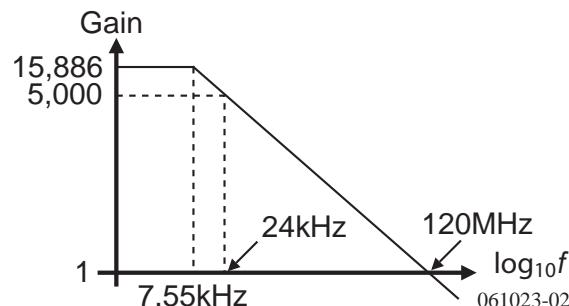
$$\therefore R_{out} \approx 20.86\text{M}\Omega$$

The low frequency gain is,

$$A_v \approx g_{m1}R_{out}$$

$$= 762\mu\text{S} \cdot 20.86\text{M}\Omega = 15,886 \text{ V/V}$$

The frequency response will be as shown:



Op Amp Bias Voltages

We also need to design the bias voltages V_{NB1} , V_{NB2} , V_{PB1} and V_{PB2} . This can be done using the following circuit:

Note, the W/L of M3, M4 and M7 will be 6 so that a current of $10\mu\text{A}$ gives $100\mu\text{A}$ in M3 of the op amp. Also, W/L of M1 and M5 will be 16 so a current of $10\mu\text{A}$ gives $125\mu\text{A}$ in M4 and M5 of the op amp.

If M2 is 4 times larger than M1, which gives a W/L of 64 for M2. Under these conditions,

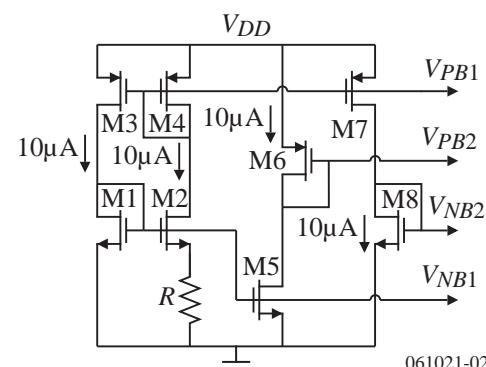
$$I_2 = I_1 = \frac{1}{2\beta_1 R^2} \Rightarrow R = \frac{10^6}{\sqrt{2 \cdot 120 \cdot 16 \cdot 10}} = 5.1\text{k}\Omega$$

The extra $40\mu\text{A}$ brings the power dissipation to 0.975mW which is still in specification.

The W/L of M6 and M8 are designed as follows:

$$V_{GS8} = V_T + 2V_{ON} \Rightarrow V_{GS8} - V_T = 0.2\text{V} = \sqrt{\frac{2 \cdot 10}{120 \cdot (W_8/L_8)}} \Rightarrow \frac{W_8}{L_8} = 4.167$$

$$V_{SG6} = |V_T| + 2V_{ON} \Rightarrow V_{SG6} - |V_T| = 0.5\text{V} = \sqrt{\frac{2 \cdot 10}{25 \cdot (W_6/L_6)}} \Rightarrow \frac{W_6}{L_6} = 3.20$$



Switch and Hold Capacitor Design

Switch:

Since the signal amplitude is from 0 to 1V, a single NMOS switch should be satisfactory. The resistance of a minimum size NMOS switch is,

$$R_{ON}(\text{worst case}) \approx \frac{1}{K_n'(W/L)(V_{GS}-V_T)} = \frac{10^6}{120(1)(1.5-0.5)} = 8.33\text{k}\Omega$$

For a $C_H = 1\text{pf}$, the time constant is 8 ns. This is too close to the 50 ns so let us increase the switch size to $0.5\mu\text{m}/0.25\mu\text{m}$ which gives a time constant of 4ns.

Therefore, the W/L ratio of the NMOS switch is $0.5\mu\text{m}/0.25\mu\text{m}$ and the hold capacitor is 1pf .

Check the error due to channel injection and clock feedthrough-

If we assume the clock that rises and falls in 1ns, then a $0.5\mu\text{m}/0.25\mu\text{m}$ switch works in the fast transition region. The channel/clock error can be calculated as:

$$V_{error} = -\left(\frac{W \cdot CGDO + \frac{C_{channel}}{2}}{C_L}\right) \left(V_{HT} - \frac{\beta V_{HT}^3}{6U \cdot C_L}\right) - \frac{W \cdot CGDO}{C_L} (V_S + 2V_T - V_L)$$

Switch and Hold Capacitor Design – Continued

Assuming $CGDO$ is 200×10^{-12} F/m we can calculate V_{HT} as 0.8131V. Thus,

$V_{error} =$

$$-\left(\frac{100 \times 10^{-18} + 0.5(7.57 \times 10^{-16})}{1 \times 10^{-12}}\right) \left(0.8131 - \frac{0.105 \times 10^{-3}}{15 \times 10^{-3}}\right) - \frac{100 \times 10^{-18}}{1 \times 10^{-12}} (1+1-0) = -0.586\text{mV}$$

For a 1volt signal with 10 bit accuracy, the error must be less than 1LSB which is 0.967mV. The channel/clock error is close to this value and one may have to consider using a CMOS switch or a dummy switch to reduce the error.

Design Summary

At this point, the analog designer understands the weaknesses and strengths of the design. The next steps will not be done but are listed below:

- 1.) Simulation to confirm and explore the hand-calculated performance
- 2.) Layout of the op amp, hold capacitor and switch.
- 3.) Verification of the layout
- 4.) Extraction of the parasitics from the layout
- 5.) Resimulation of the design.
- 6.) Check for sensitivity to ESD and latchup.
- 7.) Select package and include package parasitics in simulation.

SUMMARY

- An ADC is by nature a sampled data circuit (cannot continuously convert analog into digital)
- Two basic types of ADCs are:
 - Nyquist – analog bandwidth is as close to the Nyquist frequency as possible
 - Oversampled – analog bandwidth is much smaller than the Nyquist frequency
- The active components in an ADC are the comparator and the sample and hold circuit
- A sample and hold circuit must have at least the accuracy of $100\% / 2^N$
- Sample and hold circuits are divided into two types:
 - Open loop which are fast but not as accurate
 - Close loop which are slower but more accurate
- An example of designing a sample and hold amplifier was given to illustrate the electrical design process for CMOS analog circuits

LECTURE 370 – TESTING OF ADCS AND MODERATE SPEED NYQUIST ADCS

LECTURE ORGANIZATION

Outline

- Introduction
- Testing of ADCs
- Serial ADCs
- Successive approximation ADCs
- Single-bit/stage pipeline ADCs
- Iterative ADCs
- Self calibration techniques
- Summary

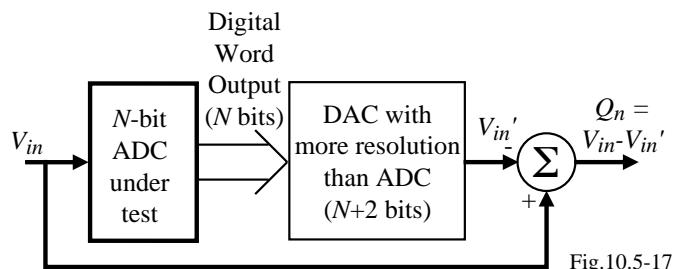
CMOS Analog Circuit Design, 2nd Edition Reference

Pages 665-681

TESTING OF ADCS

Input-Output Test for an ADC

Test Setup:

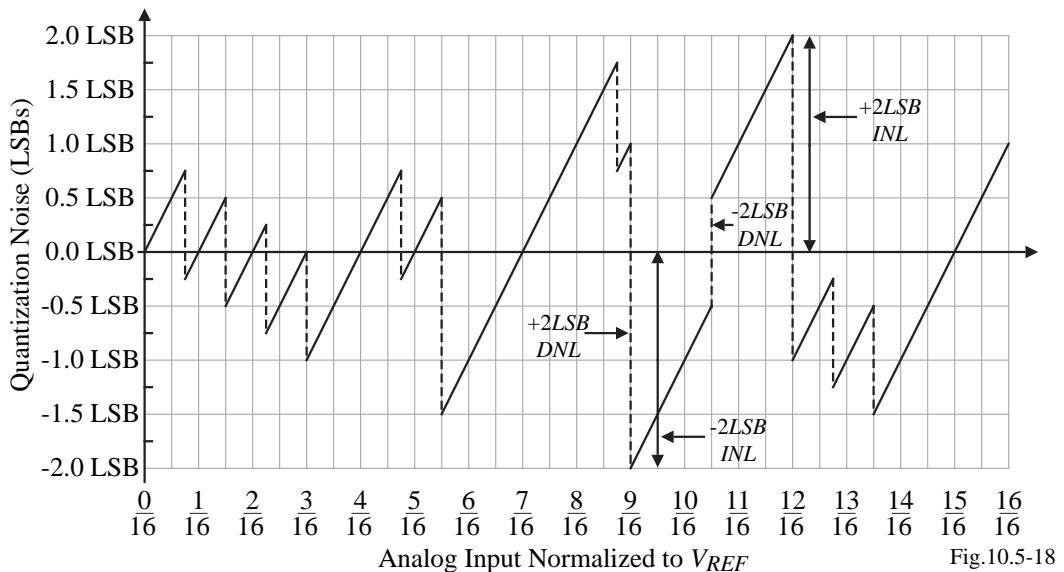


The ideal value of Q_n should be within $\pm 0.5LSB$

Can measure:

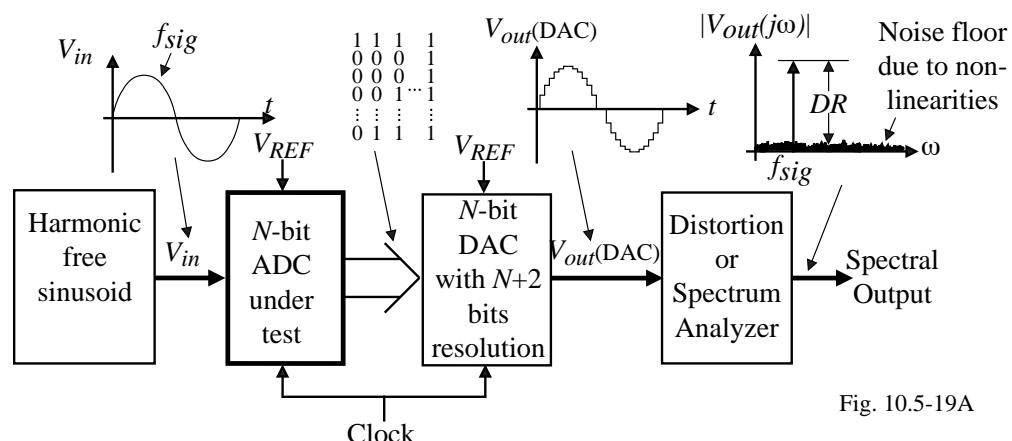
- Offset error = constant shift above or below the 0 LSB line
- Gain error = constant increase or decrease of the sawtooth plot as V_{in} is increased
- INL and DNL (see following page)

Illustration of the Input-Output Test for a 4-Bit ADC



Measurement of Nonlinearity Using a Pure Sinusoid

This test applies a pure sinusoid to the input of the ADC. Any nonlinearity will appear as harmonics of the sinusoid. Nonlinear errors will occur when the dynamic range (DR) is less than $6N$ dB where N = number of bits.



Comments:

- Input sinusoid must have less distortion than the required dynamic range
- DAC must have more accuracy than the ADC

FFT Test for an ADC

Test setup:

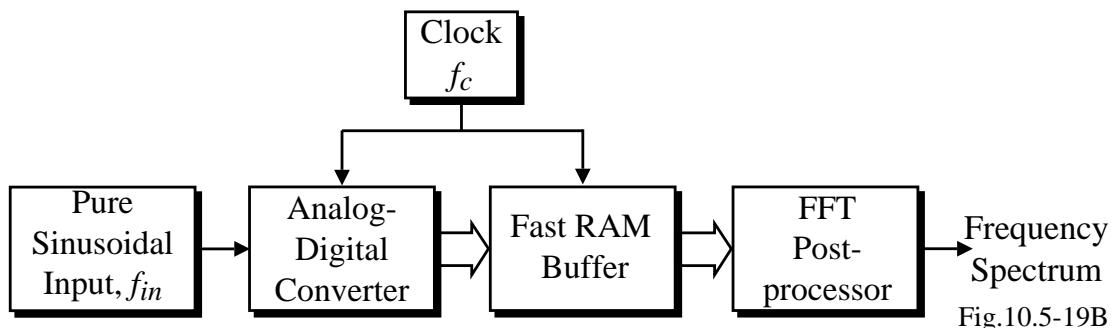


Fig.10.5-19B

Comments:

- Stores the digital output codes of the ADC in a RAM buffer
- After the measurement, a postprocessor uses the FFT to analyze the quantization noise and distortion components
- Need to use a window to eliminate measurement errors (Raised Cosine or 4-term Blackmann-Harris are often used)
- Requires a spectrally pure sinusoid

Histogram Test for an ADC

The number of occurrences of each digital output code is plotted as a function of the digital output code.

Illustration:

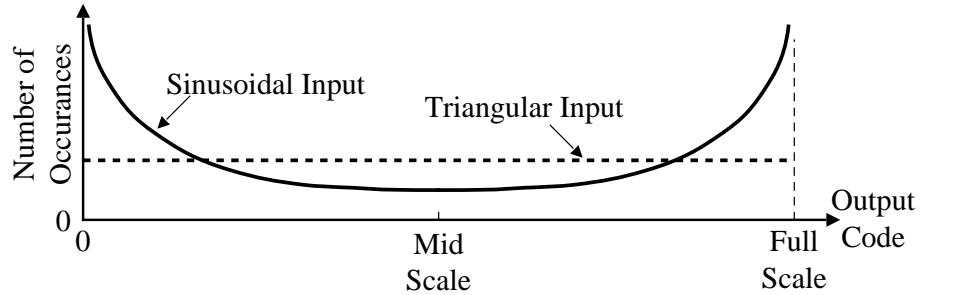


Fig.10.5-20

Comments:

- Emphasizes the time spent at a given level and can show *DNL* and missing codes
- *DNL*

$$DNL(i) = \frac{\text{Width of the bin as a fraction of full scale}}{\text{Ratio of the bin width to the ideal bin width}} - 1 = \frac{H(i)/N_t}{P(i)} - 1$$

where

$H(i)$ = number of counts in the i th bin

N_t = total number of samples

$P(i)$ = ratio of the bin width to the ideal bin width

- *INL* is found from the cumulative bin widths

Comparison of the Tests for Analog-Digital Converters

Other Tests

- Sinewave curve fitting (good for *ENOB*)
- Beat frequency test (good for a qualitative measure of dynamic performance)

Comparison

Test → Error ↓	Histogram or Code Test	FFT Test	Sinewave Curve Fit Test	Beat Frequency Test
DNL	Yes (spikes)	Yes (Elevated noise floor)	Yes	Yes
Missing Codes	Yes (Bin counts with zero counts)	Yes (Elevated noise floor)	Yes	Yes
INL	Yes (Triangle input gives INL directly)	Yes (Harmonics in the baseband)	Yes	Yes
Aperature Uncertainty	No	Yes (Elevated noise floor)	Yes	No
Noise	No	Yes (Elevated noise floor)	Yes	No
Bandwidth Errors	No	No	No	Yes (Measures analog bandwidth)
Gain Errors	Yes (Peaks in distribution)	No	No	No
Offset Errors	Yes (Offset of distribution average)	No	No	No

Bibliography on ADC Testing

- 1.) D. H. Sheingold, *Analog-Digital Conversion Handbook*, Analog Devices, Inc., Norwood, MA 02062, 1972.
- 2.) S.A. Tretter, *Introduction to Discrete-Time Signal Processing*, John Wiley & Sons New York, 1976.
- 3.) J. Doernberg, H.S. Lee, and D.A. Hodges, “Full-Speed Testing of A/D Converters,” *IEEE J. of Solid-State Circuits*, Vol. SC-19, No. 6, December 1984, pp. 820-827.
- 4.) “Dynamic performance testing of A to D converters,” *Hewlett Packard Product Note 5180A-2*.

INTRODUCTION TO MODERATE SPEED ADCS

Moderate Speed ADC Topics

- Serial ADCs - require $2^N T$ for conversion where T = period of the clock

Types:

- Single-slope
- Dual-slope

- Successive approximation ADCs – require NT for conversion where T = the clock period
- 1-bit per stage, pipeline ADCs – require T for conversion after a delay of NT
- Iterative ADCs – require NT for conversion
- Self-calibration techniques

SERIAL ANALOG-DIGITAL CONVERTERS

Single-Slope ADC

Block diagram:

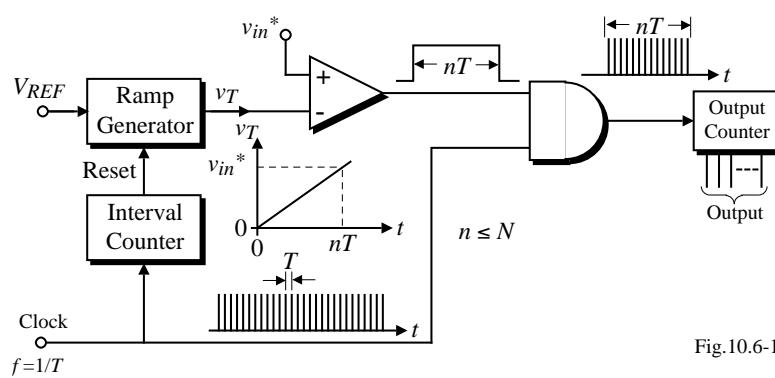


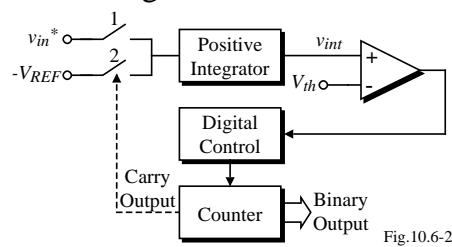
Fig.10.6-1

Attributes:

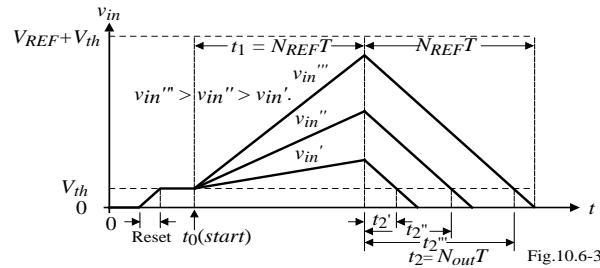
- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion time $\leq 2^N T$

Dual-Slope ADC

Block diagram:



Waveforms:



Operation:

- 1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($v_{IN}^* > 0$).
- 2.) Reset the positive integrator by integrating a positive voltage until $v_{int}(0) = V_{th}$.
- 3.) Integrate v_{in}^* for N_{REF} clock cycles to get,

$$v_{int}(t_1) = K \int_0^{N_{REF}T} v_{in}^* dt + v_{int}(0) = KN_{REF}Tv_{in}^* + V_{th}$$

- 4.) After N_{REF} counts, the carry output of the counter closes switch 2 and $-V_{REF}$ is applied to the positive integrator. The output of the integrator at $t = t_1 + t_2$ is,

$$v_{int}(t_1 + t_2) = v_{int}(t_1) + K \int_{t_1}^{N_{out}T} (-V_{REF}) dt = V_{th} \rightarrow KN_{REF}Tv_{in}^* + V_{th} - KN_{out}TV_{REF} = V_{th}$$

- 5.) Solving for N_{out} gives, $N_{out} = N_{REF} (v_{in}^* / V_{REF})$

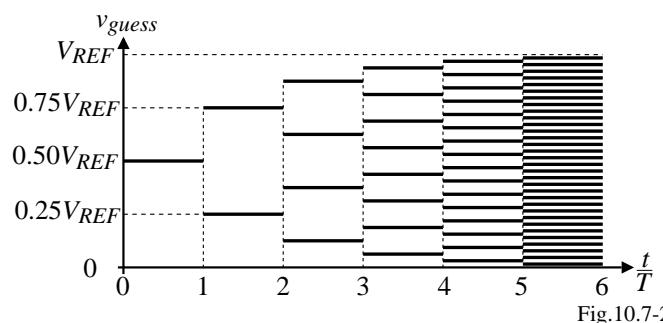
Comments: Conversion time $\leq 2(2^N)T$ and the operation is independent of V_{th} and K .

SUCCESSIVE APPROXIMATION ANALOG-DIGITAL CONVERTERS

Introduction

Successive Approximation Algorithm:

- 1.) Start with the *MSB* bit and work toward the *LSB* bit.
- 2.) Guess the *MSB* bit as 1.
- 3.) Apply the digital word 10000.... to a DAC.
- 4.) Compare the DAC output with the sampled analog input voltage.
- 5.) If the DAC output is greater, keep the guess of 1. If the DAC output is less, change the guess to 0.
- 6.) Repeat for the next *MSB*.



Block Diagram of a Successive Approximation ADC[†]

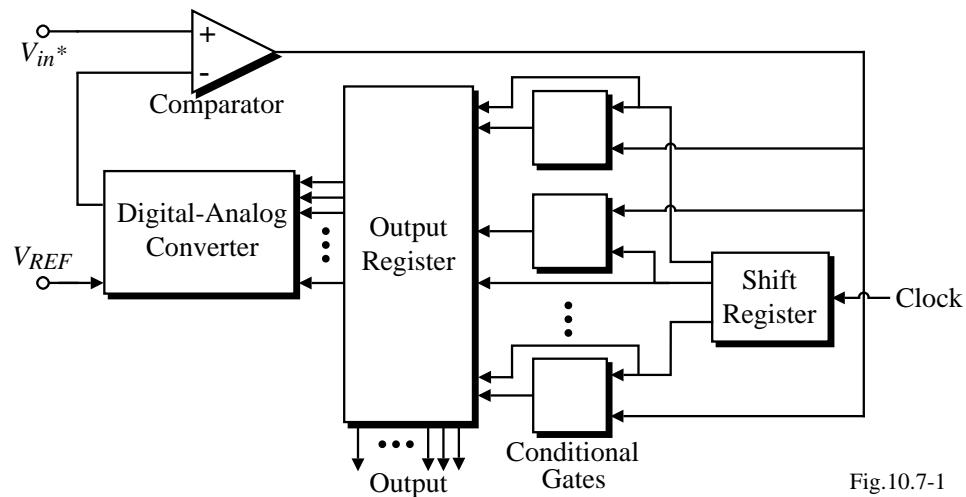


Fig.10.7-1

[†] R. Hnatek, *A User's Handbook of D/A and A/D Converters*, John Wiley and Sons, Inc., New York, NY, 1976.
CMOS Analog Circuit Design

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5-Bit Successive Approximation ADC

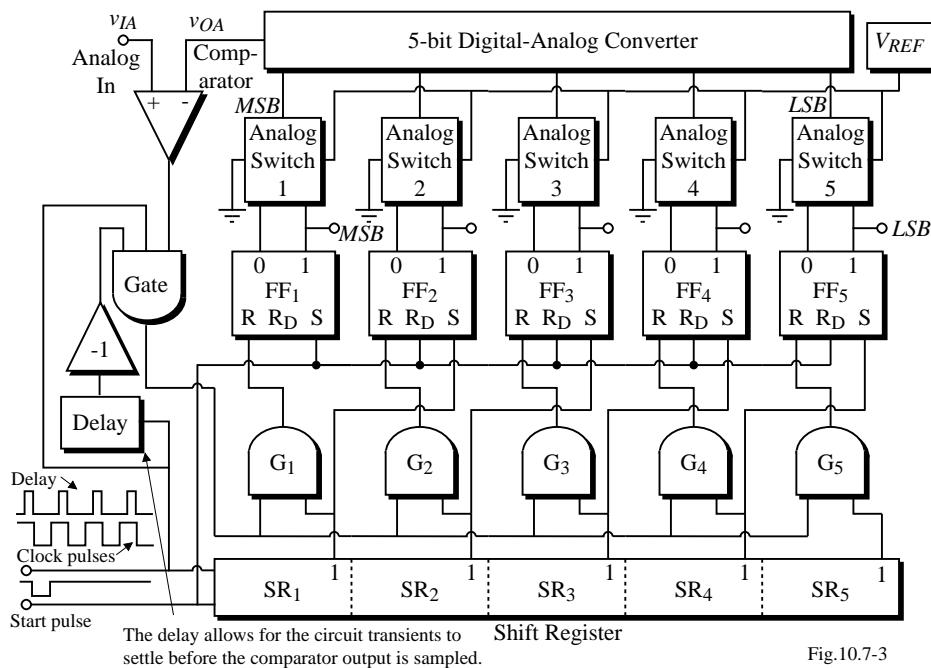


Fig.10.7-3

m-Bit Voltage-Scaling, k-Bit Charge-Scaling Successive Approximation ADC

Operation:

- 1.) With the two S_F switches closed, all capacitors are paralleled and connected to V_{in}^* which autozeros the comparator offset voltage.

- 2.) With all capacitors still in parallel, a successive approximation search is performed to find the resistor segment in which the analog signal lies.

- 3.) Finally, a successive approximation search is performed on charge scaling subDAC to establish the analog output voltage.

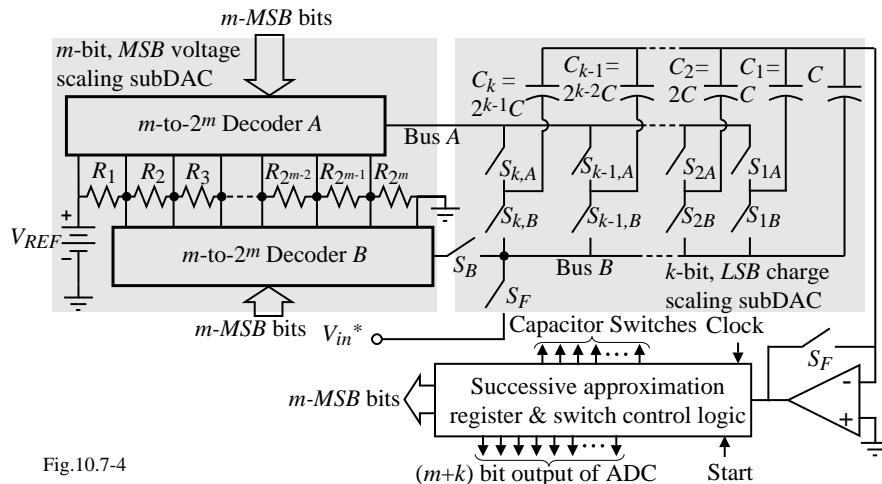


Fig.10.7-4

Voltage-Scaling, Charge-Scaling Successive Approximation ADC - Continued

Autozero Step

Removes the influence of the offset voltage of the comparator.

The voltage across the capacitor is given as,

$$v_C = V_{in}^* - V_{OS}$$

Successive Approximation Search on the Resistor String

The voltage at the comparator input is

$$v_{comp} = V_{Ri} - V_{in}^*$$

If $v_{comp} > 0$, then $V_{Ri} > V_{in}^*$, if $v_{comp} < 0$, then $V_{Ri} < V_{in}^*$

Successive Approximation Search on the Capacitor SubDAC

The input to the comparator is written as,

$$v_{comp} = (V_{Ri+1} - V_{in}^*) \frac{C_{eq}}{2kC} + (V_{Ri} - V_{in}^*) \frac{2kC - C_{eq}}{2kC}$$

However, $V_{Ri+1} = V_{Ri} + 2^{-m}V_{REF}$

Combining gives,

$$\begin{aligned} v_{comp} &= (V_{Ri} + 2^{-m}V_{REF} - V_{in}^*) \frac{C_{eq}}{2kC} + (V_{Ri} - V_{in}^*) \frac{2kC - C_{eq}}{2kC} \\ &= V_{Ri} - V_{in}^* + 2^{-m}V_{REF} \frac{C_{eq}}{2kC} \end{aligned}$$

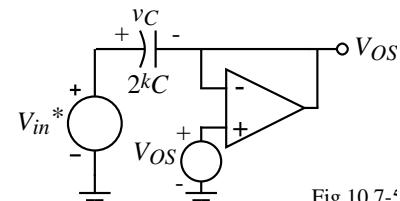


Fig.10.7-4

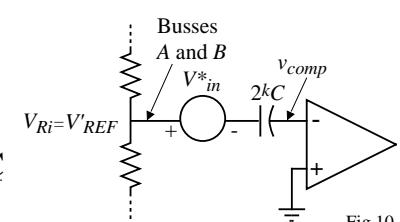


Fig.10.

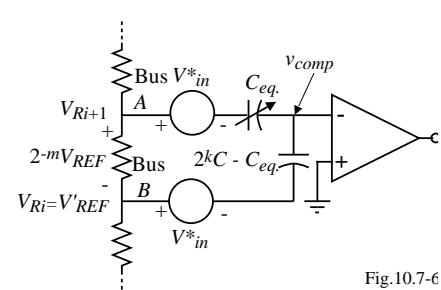
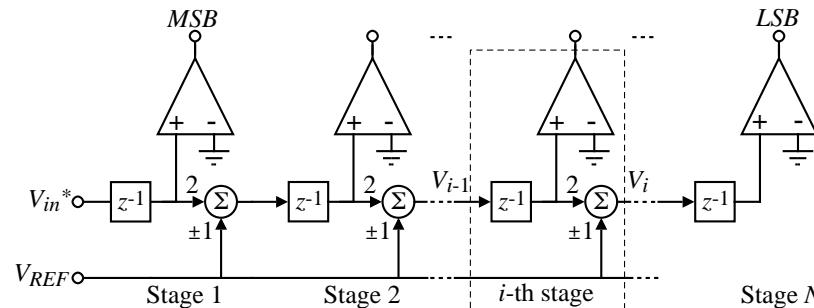


Fig.10.7-6

SINGLE-BIT/STAGE, PIPELINE ANALOG-DIGITAL CONVERTERS

Single-Bit/Stage Pipeline ADC Architecture

Implementation:



Operation:

- Each stage multiplies its input by 2 and adds or subtracts V_{REF} depending upon the sign of the input.
- i -th stage,

$$V_i = 2V_{i-1} - b_i V_{REF}$$

where b_i is given as

$$b_i = \begin{cases} +1 & \text{if } V_{i-1} > 0 \\ -1 & \text{if } V_{i-1} < 0 \end{cases}$$

Fig.10.7-9
multiplies

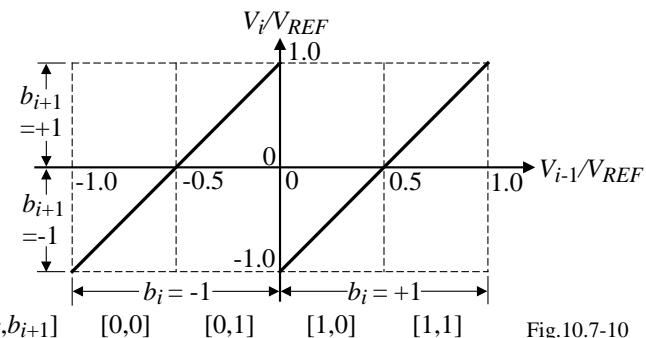


Fig.10.7-10

Example 370-1 - Illustration of the Operation of the Pipeline ADC

Assume that the sampled analog input to a 4-bit pipeline analog-digital converter is 2.00 V. If V_{REF} is equal to 5 V, find the digital output word and the analog equivalent voltage.

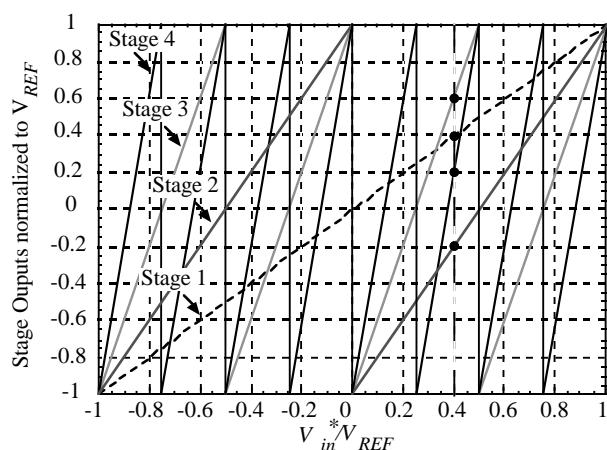
Solution

Stage No.	Input to the i th stage, V_{i-1}	$V_{i-1} > 0$?	Bit i
1	2V	Yes	1
2	$(2V \cdot 2) - 5 = -1V$	No	0
3	$(-1V \cdot 2) + 5 = 3V$	Yes	1
4	$(3V \cdot 2) - 5 = 1V$	Yes	1

Illustration:

$$\begin{aligned} V_{\text{analog}} &= 5 \left(\frac{1}{2} - \frac{1}{4} + \frac{1}{8} + \frac{1}{16} \right) \\ &= 5(0.4375) = 2.1875 \end{aligned}$$

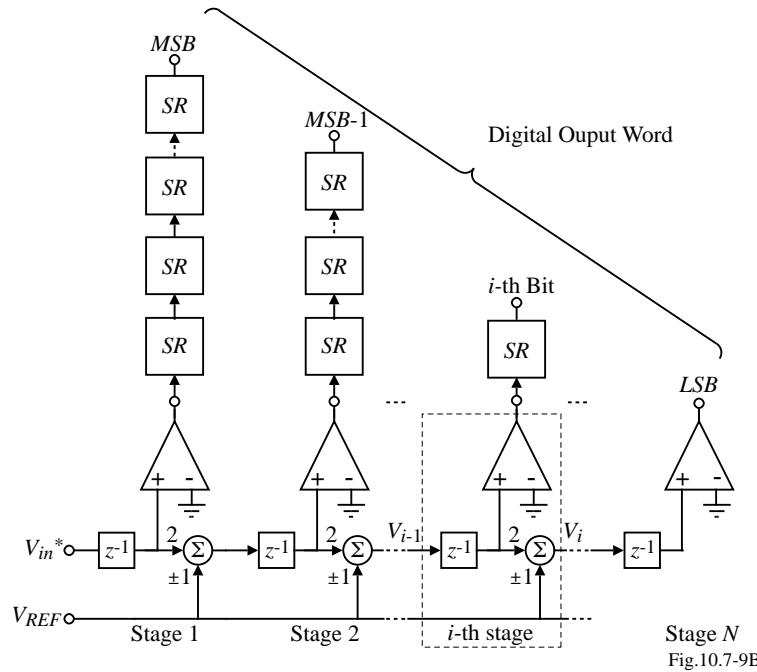
where $b_i = +1$ if the i th-bit is 1 and $b_i = -1$ if the i th bit is 0



Achieving the High Speed Potential of the Pipeline ADC

If shift registers are used to store the output bits and align them in time, the pipeline ADC can output a digital word at every clock cycle with a latency of NT .

Illustration:



CMOS Analog Circuit Design

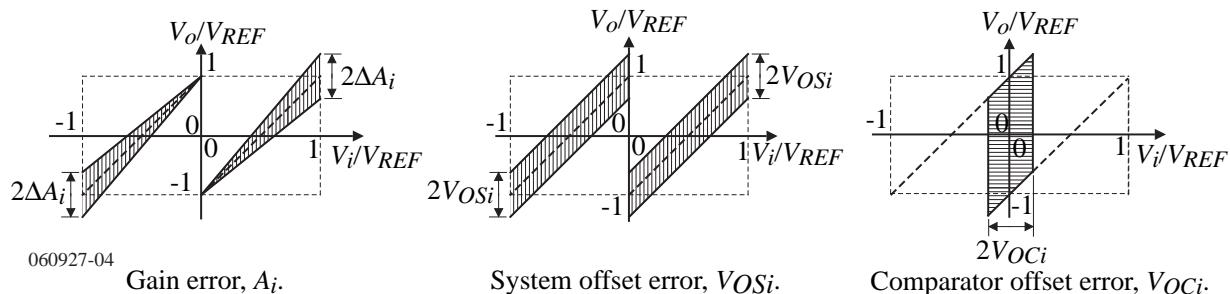
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Errors in the Pipeline ADC

Types of errors:

- Gain errors – $\times 2$ amplifier or summing junctions
- Offset errors – comparators or summing junctions

Illustration of errors:

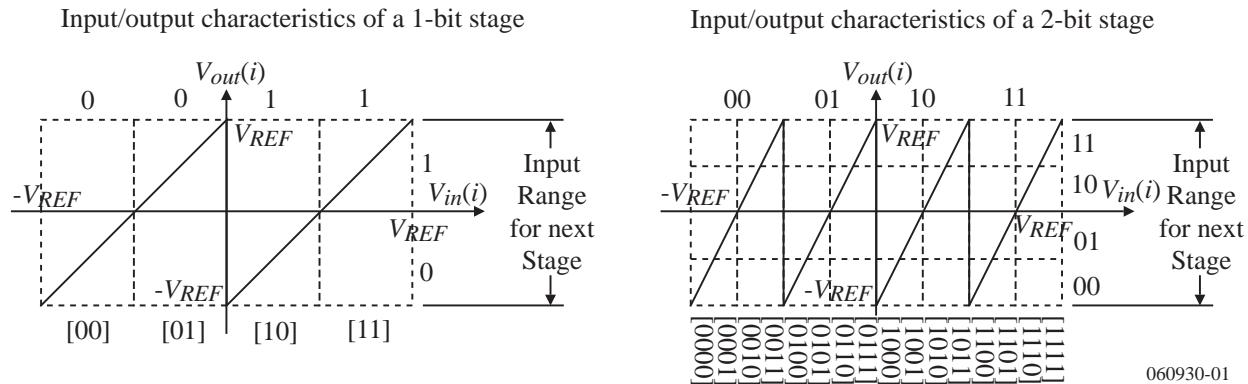


An error will occur if the output voltage of one stage exceeds $\pm V_{REF}$ (saturates).

Digital Error Correction

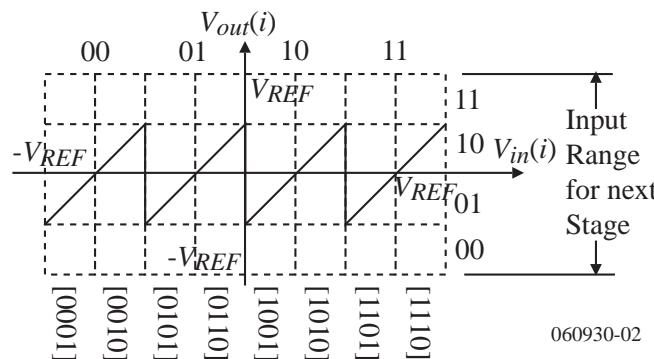
In the previous slide, we noted that if the analog output to the next stage exceeds $\pm V_{REF}$ that an error occurs. This error can be detected by adding one more bit to the following stage for the purposes of detecting the error.

Illustration (2nd bit not used for error correction):



Digital Error Correction – Continued

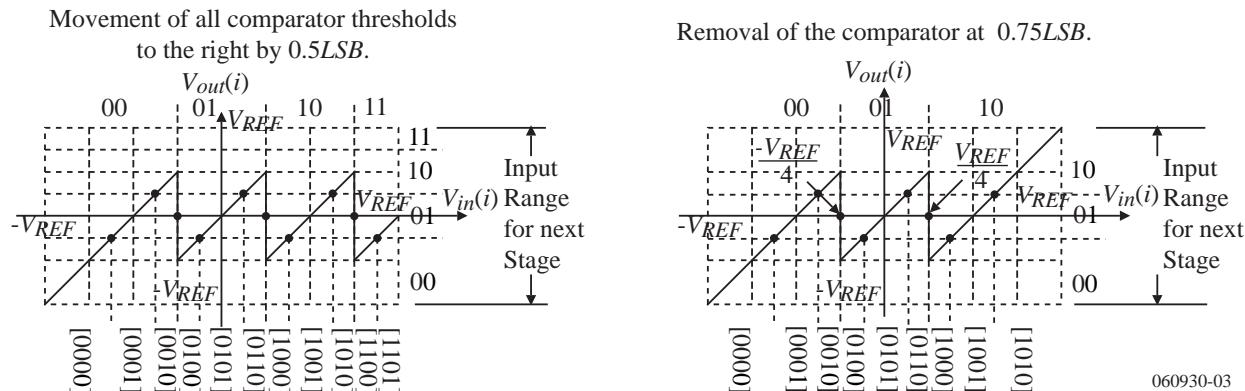
If the gain of 4 amplifier is reduced back to 2, the input/output characteristics of the 2-bit stage become:



The output bits can be used to determine the error. If these bits are 00, then 0.5LSB must be added to get the correct digital output. If the bits are 11, then 0.5LSB must be subtracted to get the correct digital output.

Modified Digital Error Correction (1.5 bits per stage)

In the previous slide, it was necessary sometimes to perform digital subtraction which is not easy to implement. To avoid this problem, a $0.5LSB$ shift has been added to the input/output characteristic resulting in the following.

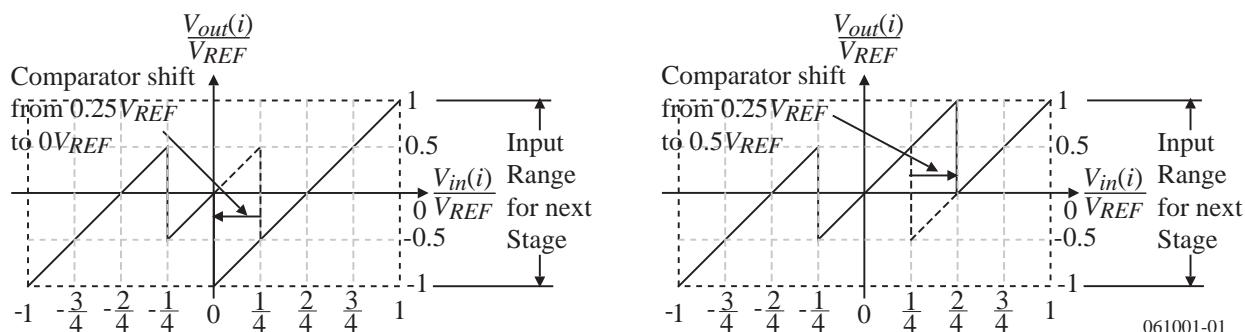


To obtain code 11 out of the stage after correction, the correction logic must increment the output of the stage.

To obtain code 00 from this stage after correction, the correction logic need do nothing. Therefore, only two comparators are needed to produce outputs of (00, 01, 10) as shown on the right-hand characteristic.

How Does the 1.5 Bit Stage Correct Offset Errors?

Consider a $\pm 0.25V_{REF}$ comparator offset shift in the input-output characteristics of the 1.5 bit stage.

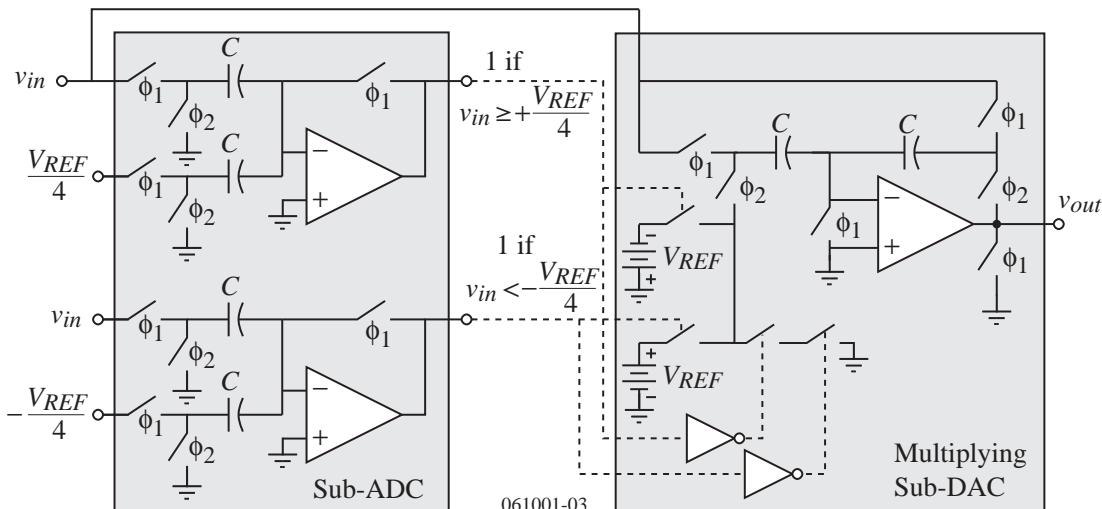


When the shift is to the left, the comparator will not be in error until the shift is greater than $0.25 V_{REF}$. This is because the comparator thresholds were shifted to the right by $0.5 V_{REF}$.

When the shift is to the right, the input to the next stage will be greater than $0.50V_{REF}$. This will cause the output code 10 which indicates that the digital word should be incremented by 1 bit.

The range of correction $\pm V_{REF} / 2^{B+1}$ where B is the number of bits per stage.

Implementation of the 1.5 Bit Stage



The multiplying Sub-DAC must implement the following equation:

$$V_{out} = \begin{cases} 2 \cdot v_{in} - V_{REF} & \text{if } v_{in} > V_{REF}/4 \\ 2 \cdot v_{in} & \text{if } -V_{REF}/4 \leq v_{in} \leq V_{REF}/4 \\ 2 \cdot v_{in} + V_{REF} & \text{if } v_{in} < -V_{REF}/4 \end{cases}$$

Example 370-2 - Accuracy requirements for a 5-bit pipeline ADC

Show that if $V_{in} = V_{REF}$, that the pipeline ADC will have an error in the 5th bit if the gain of the first stage is $2 \cdot (1/8) = 1.875$ which corresponds to when an error will occur. Show the influence of V_{in} on this result for V_{in} of $0.65V_{REF}$ and $0.22V_{REF}$.

Solution

For $V_{in} = V_{REF}$, we get the results shown below. The input to the fifth stage is 0V which means that the bit is uncertain. If A_1 was slightly less than 1.875, the fifth bit would be 0 which is in error. This result assumes that all stages but the first are ideal.

i	$V_i(\text{ideal})$	Bit i (ideal)	$V_i(A_1=1.875)$	Bit i ($A_1=1.875$)
1	1	1	1.000	1
2	1	1	0.875	1
3	1	1	0.750	1
4	1	1	0.500	1
5	1	1	0.000	?

Now let us repeat the above results for $V_{in} = 0.65V_{REF}$. The results are shown below.

i	$V_i(\text{ideal})$	Bit i (ideal)	$V_i(A_1=1.875)$	Bit i ($A_1=1.875$)
1	+0.65	1	0.6500	1
2	+0.30	1	0.2188	1
3	-0.40	0	-0.5625	0
4	+0.20	1	-0.1250	0
5	-0.60	0	0.7500	1

Example 370-2 - Continued

Next, we repeat for the results for $V_{in} = 0.22V_{REF}$. The results are shown below. We see that no errors occur.

i	$V_i(\text{ideal})$	Bit i (ideal)	$V_i(A_1=1.875)$	Bit i ($A_1=1.875$)
1	+0.22	1	0.2200	1
2	-0.56	0	-0.5875	0
3	-0.12	0	-0.1750	0
4	+0.76	1	0.6500	1
5	+0.52	1	0.3000	1

Note the influence of V_{in} in the fact that an error occurs for $A_1= 1.875$ for $V_{in} = 0.65V_{REF}$ but not for $V_{in} = 0.22V_{REF}$. Why? Note on the plot for the output of each stage, that for $V_{in} = 0.65V_{REF}$, the output of the fourth stage is close to 0V so any small error will cause problems. However, for $V_{in} = 0.22V_{REF}$, the output of the fourth stage is at $0.65V_{REF}$ which is further away from 0V and is less sensitive to errors.

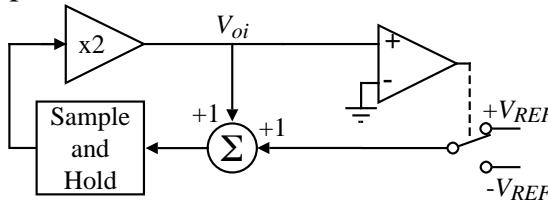
$\therefore \text{The most robust values of } V_{in} \text{ will be near } -V_{REF}, 0 \text{ and } +V_{REF}. \text{ or}$
when each stage output is furthest from the comparator threshold, 0V.

ITERATIVE ANALOG-DIGITAL CONVERTERS

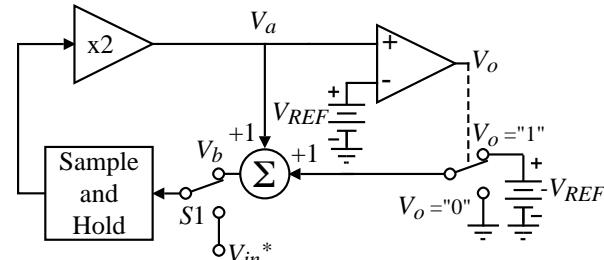
Iterative (Cyclic) Algorithmic Analog-Digital Converter

The pipeline ADC can be reduced to a single stage that cycles the output back to the input.

Implementation:



Iterative algorithm ADC



Different version of iterative algorithm ADC implementation

Fig. 10.7-13

Operation:

- 1.) Sample the input by connecting switch S_1 to V_{in}^* .
- 2.) Multiply V_{in}^* by 2.
- 3.) If $V_a > V_{REF}$, set the corresponding bit = 1 and subtract V_{REF} from V_a .
 If $V_a < V_{REF}$, set the corresponding bit = 0 and add zero to V_a .
- 4.) Repeat until all N bits have been converted.

Example 370-3 - Conversion Process of an Iterative, Algorithmic Analog-Digital Converter

The iterative, algorithmic analog-digital converter is to be used to convert an analog signal of $0.8V_{REF}$. The figure below shows the waveforms for V_a and V_b during the process. T is the time for one iteration cycle.

- 1.) The analog input of $0.8V_{REF}$ gives $V_a = 1.6V_{REF}$ and $V_b = 0.6V_{REF}$ and the MSB as 1.
- 2.) V_b is multiplied by two to give $V_a = 1.2V_{REF}$. The next bit is also 1 and $V_b = 0.2V_{REF}$.
- 3.) The third iteration gives $V_a = 0.4V_{REF}$, making the next bit is 0 and $V_b = 0.4V_{REF}$.
- 4.) The fourth iteration gives $V_a = 0.8V_{REF}$, giving $V_b = 0.8V_{REF}$ and the fourth bit as 0.
- 5.) The fifth iteration gives $V_a = 1.6V_{REF}$, $V_b = 0.6V_{REF}$ and the fifth bit as 1.

The digital word after the fifth iteration is 11001 and is equivalent to an analog voltage of $0.78125V_{REF}$.

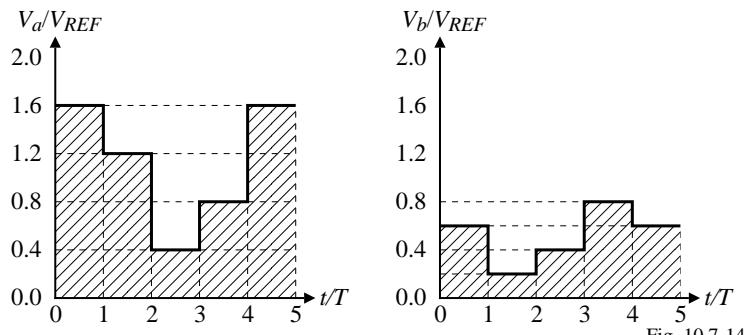
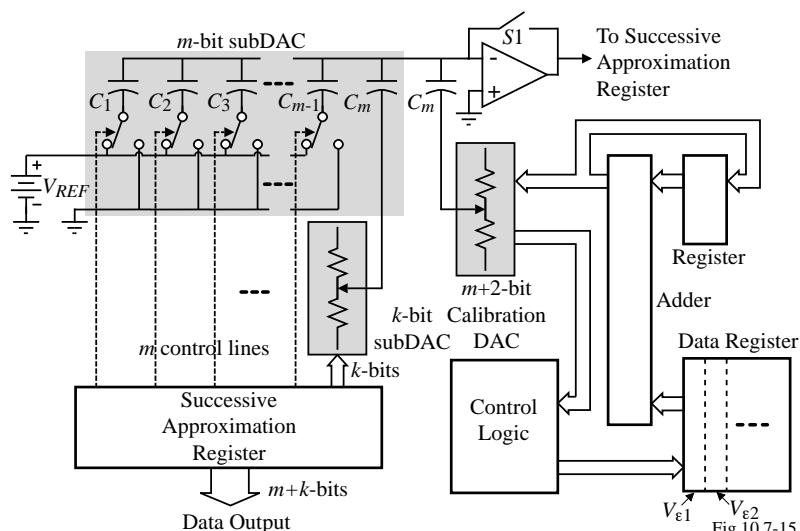


Fig. 10.7-14.

SELF-CALIBRATION TECHNIQUES Self-Calibrating Analog-Digital Converters

Self-calibration architecture for a m -bit charge scaling, k -bit voltage scaling successive approximation ADC



Comments:

- Self-calibration can be accomplished during a calibration cycle or at start-up
- In the above scheme, the LSB bits are not calibrated
- Calibration can extend the resolution to 2-4 bits more than without calibration

Self-Calibrating Analog-Digital Converters - Continued

Self-calibration procedure starting with the *MSB* bit:

1.) Connect C_1 to V_{REF} and the remaining capacitors ($C_2 + C_3 + \dots + C_m + C_m = \overline{C_1}$) to ground and close S_F .

2.) Next, connect C_1 to ground and $\overline{C_1}$ to V_{REF} .

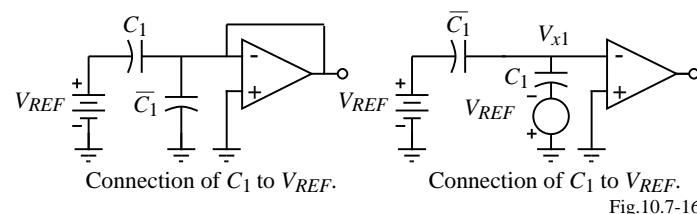


Fig.10.7-16

3.) The result will be $V_{x1} = \left(\frac{\overline{C_1} - C_1}{C_1 + \overline{C_1}} \right) V_{REF}$. If $C_1 = \overline{C_1}$, then $V_{x1} = 0$.

4.) If $V_{x1} \neq 0$, then the comparator output will be either high or low. Depending on the comparator output, the calibration circuitry makes a correction through the calibration DAC until the comparator output changes. At this point the *MSB* is calibrated and the *MSB* correction voltage, $V_{\varepsilon 1}$ is stored.

5.) Proceed to the next *MSB* with C_1 out of the array and repeat for C_2 and $\overline{C_2}$. Store the correction voltage, $V_{\varepsilon 2}$, in the data register.

6.) Repeat for C_3 with C_1 and C_2 out of the array. Continue until all of the capacitors or the *MSB* DAC have been corrected.

Note: For normal operation, the circuit adds the correct *combined* correction voltage.

SUMMARY

- Tests for the ADC include:

- Input-output test
- Spectral test
- FFT test
- Histogram test

- Moderate Speed ADCs:

Type of ADC	Advantage	Disadvantage
Serial ADC	High resolution	Slow
Voltage-scaling, charge-scaling successive approximation ADC	High resolution	Requires considerable digital control circuitry
Successive approximation using a serial DAC	Simple	Slow
Pipeline ADC	Fast after initial latency of NT	Accuracy depends on input
Iterative algorithmic ADC	Simple	Requires other digital circuitry

- Successive approximation ADCs also can be calibrated extending their resolution 2-4 bits more than without calibration.

LECTURE 380 – HIGH SPEED NYQUIST ADCS

LECTURE ORGANIZATION

Outline

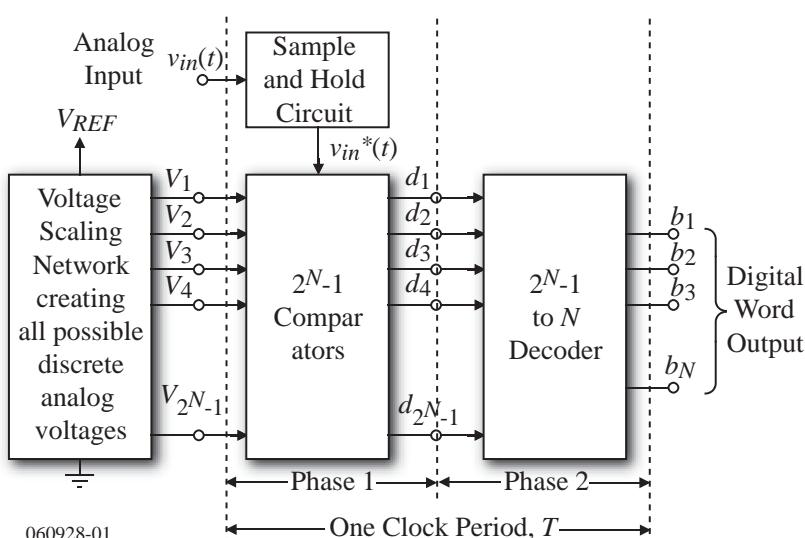
- Parallel/flash ADCs
- Interpolating and averaging
- Folding
- High-speed, high-resolution ADCs
- Time-interleaved ADCs

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 682-697

PARALLEL/FLASH ADCS

Parallel/Flash ADC Architecture



- The notation, $v_{in}^*(t)$, means the signal is sampled and held.
- The sample and hold function can be incorporated into the comparators
- The digital words designated as d_i form a thermometer code

A 3-bit, parallel ADC

General Comments:

- Fast, in the first phase of the clock the analog input is sampled and applied to the comparators. In the second phase, the digital encoding network determines the correct output digital word.
- Number of comparators required is 2^{N-1} which can become large if N is large
- The offset of the comparators must be less than $\pm V_{REF}/2^{N+1}$
- Errors occur as “bubbles” in the thermometer code and can be corrected with additional circuitry
- Typical sampling frequencies can be as high as 1000MHz for 6-bits in sub-micron CMOS technology.

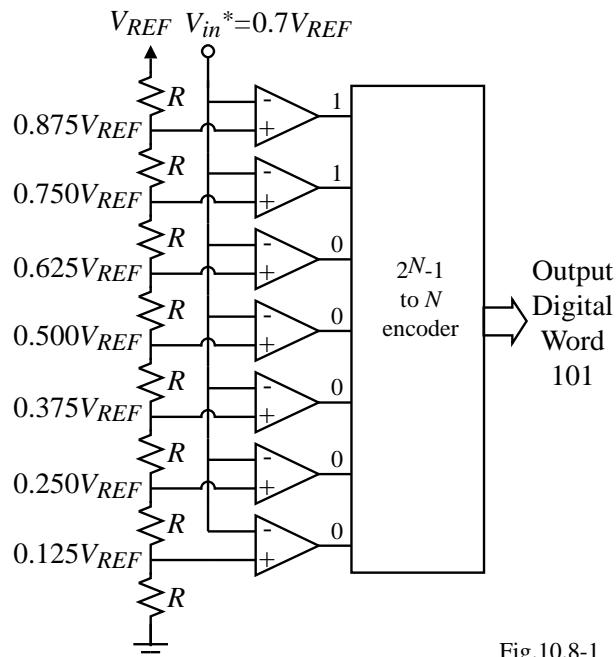


Fig.10.8-1

Example 380-1 - Comparator Bandwidth Limitations on the Flash ADC

The comparators of a 6-bit, flash ADC have a dominant pole at 10^4 radians/sec, a dc gain of 10^4 , a slew rate of $10V/\mu s$, and a binary output voltage of 1V and 0V. Assume that the conversion time is the time required for the comparator to go from its initial state to halfway to its final state. What is the maximum conversion rate of this ADC if $V_{REF} = 1V$? Assume the resistor ladder is ideal.

Solution:

The output of the i -th comparator can be found by taking the inverse Laplace transform of,

$$\mathcal{L}^{-1}\left[V_{out}(s) = \frac{A_o}{(s/10^4) + 1} \cdot \frac{V_{in}^* - V_{Ri}}{s}\right] \rightarrow v_{out}(t) = A_o(1 - e^{-10^4 t})(V_{in}^* - V_{Ri}).$$

The worst case occurs when

$$V_{in}^* - V_{Ri} = 0.5V_{LSB} = V_{REF}/2^7 = 1/128$$

$$\therefore 0.5V = 10^4(1 - e^{-10^4 T})(1/128) \rightarrow 64 \times 10^{-4} = 1 - e^{-10^4 T}$$

$$\text{or, } e^{-10^4 T} = 1 - 64 \times 10^{-4} = 0.9936 \rightarrow T = 10^{-4} \ln(1.0064) = 0.6421 \mu s$$

$$\therefore \text{Maximum conversion rate} = \frac{1}{0.6421 \mu s} = 1.557 \times 10^6 \text{ samples/second}$$

Checking the slew rate shows that it does not influence the maximum conversion rate.

$$SR = 10V/\mu s \rightarrow \frac{\Delta V}{\Delta T} = 10V/\mu s \rightarrow \Delta V = 10V/\mu s(0.6421 \mu s) = 6.421V > 1V$$

Signal Delay in High Speed Converters

Assume that clocked comparators are used in a 500MHz sampling frequency ADC of 8-bits. If the input frequency is 250MHz with a peak-to-peak value of V_{REF} , the clock accuracy must be

$$\Delta t \leq \frac{\Delta V}{\omega V_p} = \frac{V_{REF}/2^{N+1}}{2\pi f(0.5V_{REF})} = \frac{1}{29 \cdot \pi \cdot f} \approx 2.5\text{ps}$$

Since electrical signals travel at approximately $50\mu\text{m}/\text{ps}$ for metal on an IC, each metal path from the clock to each comparator must be equal to within $125\mu\text{m}$ to avoid LSB errors due to clock skew. Therefore, must use careful layout to avoid ADC inaccuracies at high frequencies.

An equal-delay clock distribution system for a 4-bit parallel ADC:

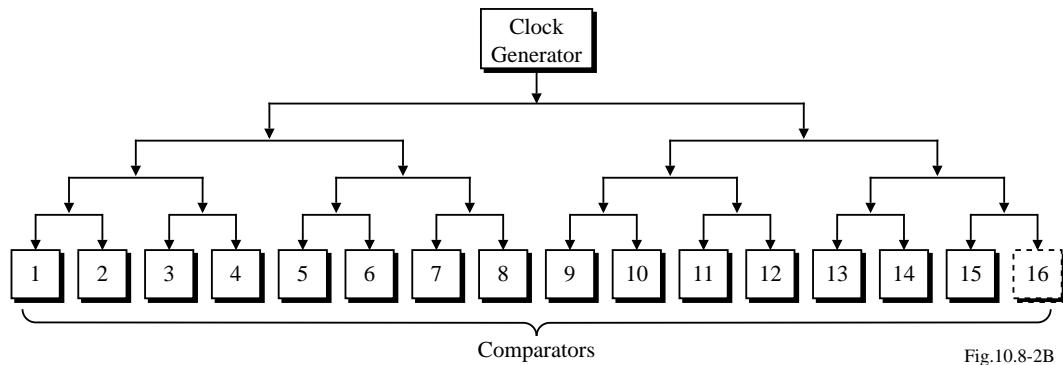


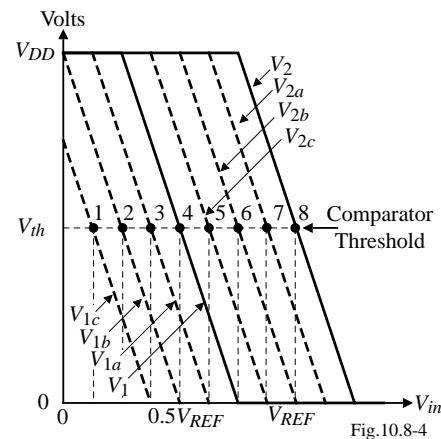
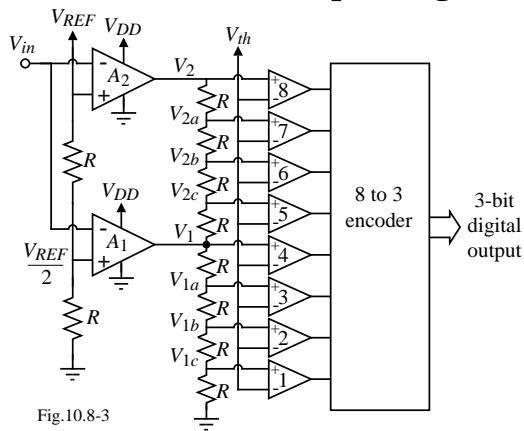
Fig.10.8-2B

Other Errors of the Parallel ADC

- Resistor string error - if current is drawn from the taps to the resistor string this will create a “bowing” effect on the voltage. This can be corrected by applying the correct voltage to various points of the resistor string.
- Input common mode range of the comparators - the comparators at the top of the string must operate with the same performance as the comparators at the bottom of the string.
- Kickback or flashback - influence of rapid transition changes occurring at the input of a comparator. Can be solved by using a preamplifier or buffer in front of the comparator.
- Metastability - uncertainty of the comparator output causing the transition of the thermometer code to be undetermined.

INTERPOLATING AND AVERAGING

Illustration of a 3-bit interpolating ADC using a factor of 4 interpolation



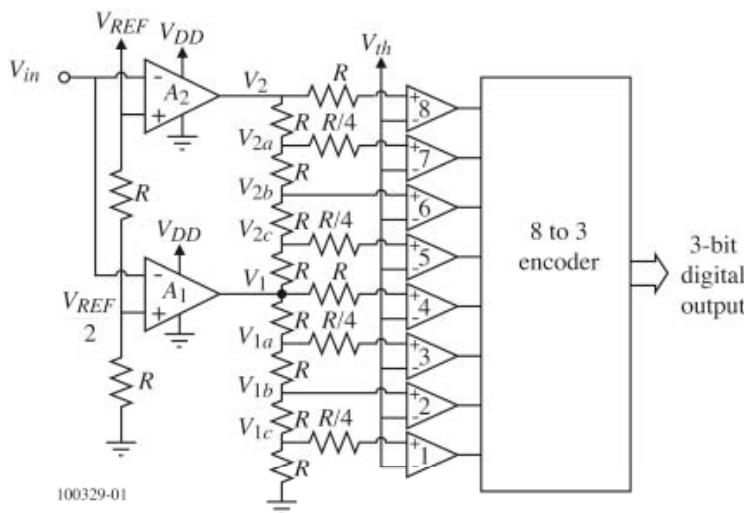
Comments:

- Capacitive loading at the input is reduced from 8 comparators to two amplifiers.
- The comparators no longer need a large *ICMR*
- V_1 and V_2 , are interpolated through the resistor string and applied to the comparators.
- Because of the amplification of the input amplifiers and a single threshold, the comparators can be simple and are often replaced by a latch.
- If the dots in Fig. 10.8-4 are not equally spaced, *INL* and *DNL* will result.

A 3-Bit Interpolating ADC with Equalized Comparator Delays

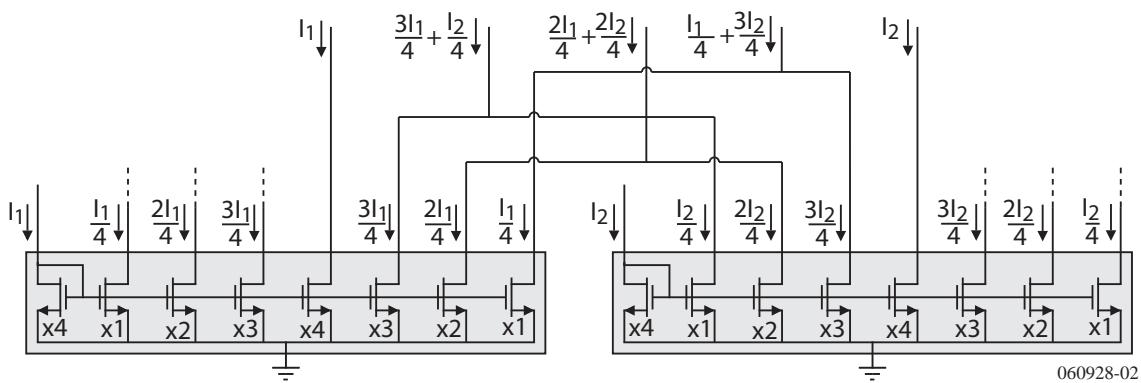
One of the problems in voltage (passive) interpolation is that the delay from the amplifier output to each comparator can be different due to different source resistance.

Solution:



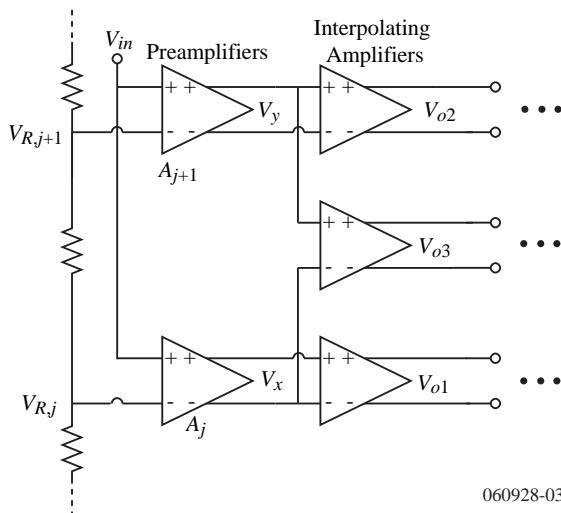
Active Interpolation

Example of a 3 level current interpolation:



This type of interpolation works well with current processing, i.e., current comparators.

Interpolation using Amplifiers

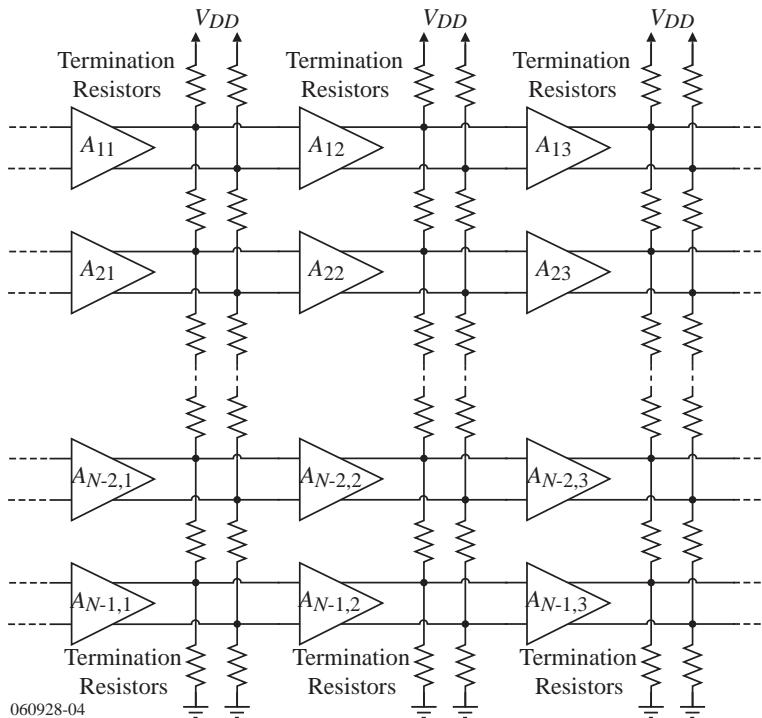


$V_{o3} = K(V_y - V_x)$ which is between V_y and V_x .

Averaging[†]

In many cases, the comparators consist of a number of pre-amplifiers followed by a latch. Averaging is the result of interconnecting the outputs of each stage of amplifiers so that the errors in one amplifier chain are balanced out by adjacent amplifier chains.

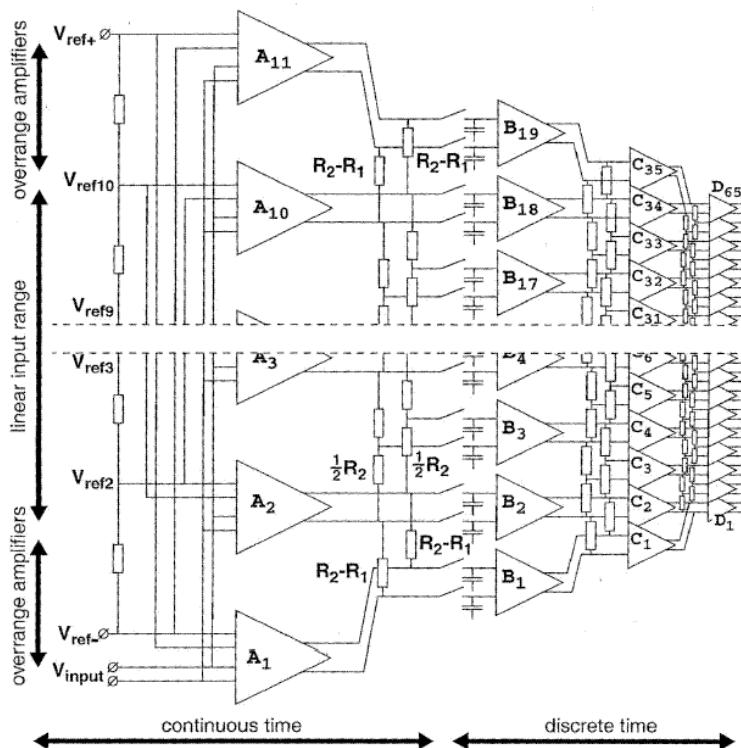
Result: The offsets are reduced allowing the transistors to be made smaller and therefore reducing the parasitics increasing the speed of the ADC.



[†] P.C.S. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18 μ m CMOS Using Averaging Termination, *IEEE J. of Solid-State Circuits*, vol. 37, no. 12, Dec. 2002, pp. 1599-1609.

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Analog Front End of an ADC using Averaging



FOLDING

Folding Analog-Digital Converters

Allows the number of comparators to be reduced below the value of 2^{N-1} .

Architecture for a folded ADC:

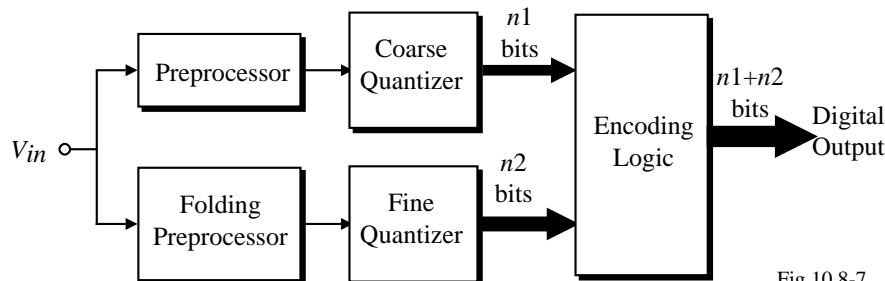


Fig.10.8-7

Operation:

The input is split into two or more parallel paths.

- First path uses a coarse quantizer to quantize the signal into 2^{n1} values
- The second path maps all of the 2^{n1} subranges onto a single subrange and applies this analog signal to a fine quantizer of 2^{n2} subranges.

Thus, the total number of comparators is $2^{n1-1} + 2^{n2-1}$ compared with $2^{n1+n2-1}$ for a parallel ADC.

I.e., if $n1 = 2$ and $n2 = 4$, the folding ADC requires $3 + 15 = 18$ compared with 63 comparators.

Example of a Folding Preprocessor

Folding characteristic for $n1 = 2$ and $n2 = 3$.

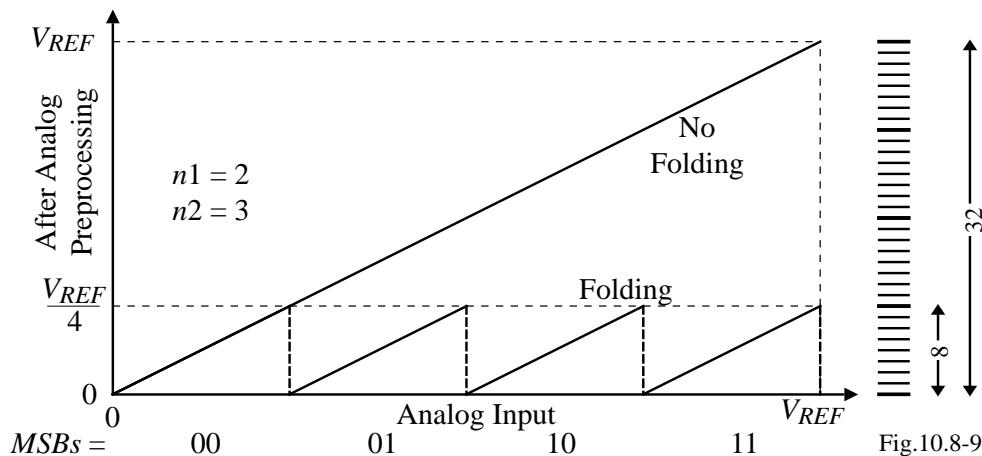


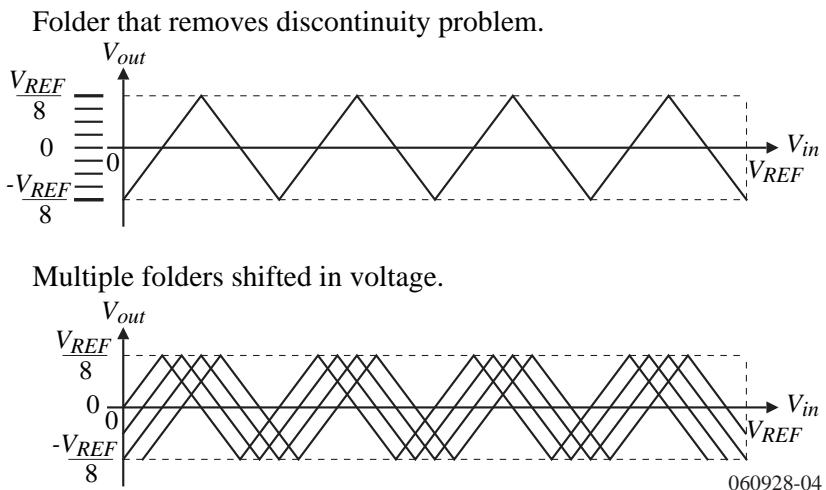
Fig.10.8-9

Problems:

- The sharp discontinuities of the folder are difficult to implement at high speeds.
- Fine quantizer must work at voltages ranging from 0 to $V_{REF}/4$ (subranging).
- The actual frequency of the folding signal is F times the input frequency where F is the number of folds

Modified Folding Preprocessors

The discontinuity problem can be removed by the following folding preprocessors:



In the second case, the reference voltage for all comparators is identical which removes any ICMR problems.

A 5-Bit Folding ADC Using 1-Bit Quantizers (Comparators)

Block diagram:

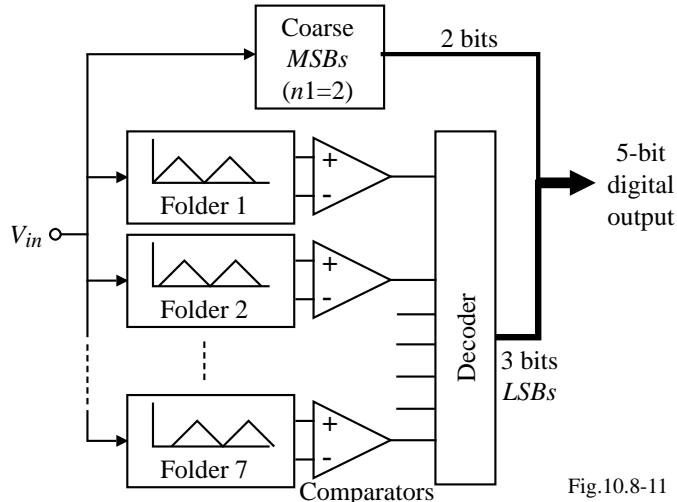


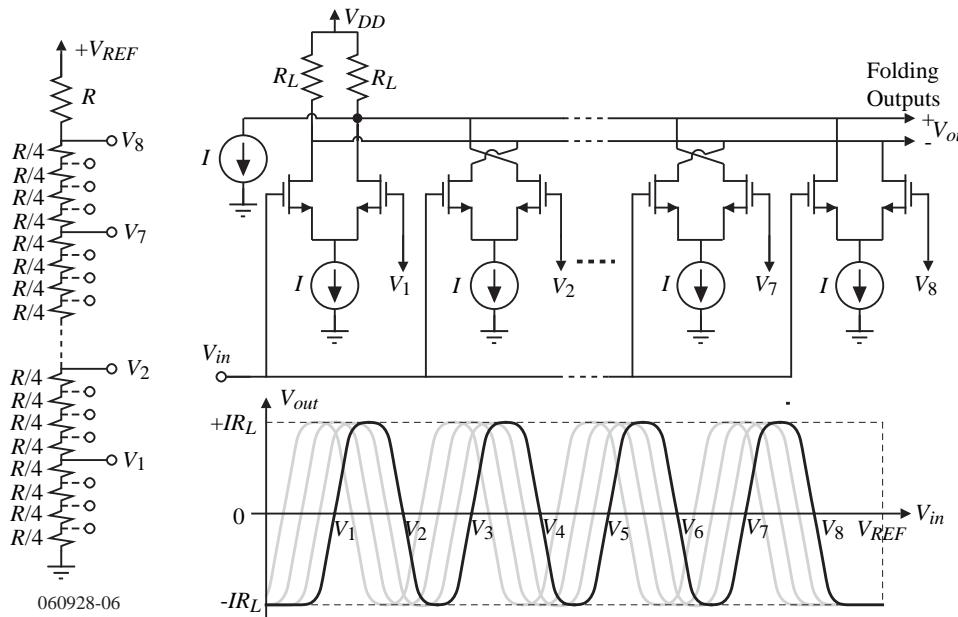
Fig.10.8-11

Comments:

- Number of comparators is 7 for the fine quantizer and 3 for the coarse quantizer
- The zero crossings of the folders must be equally spaced to avoid linearity errors
- The number of folders can be reduced and the comparators simplified by use of interpolation

Folding Circuits

Implementation of a times 4 folder:



Comments:

- Horizontal shifting is achieved by modifying the topmost and bottom resistors of the resistor string
- Folding and interpolation ADCs offer the most resolution at high speeds (≈ 8 bits at 500MHz)

Use of a S/H in Front of the Folding ADC

Benefit of a S/H:

- With no S/H, the folding circuit acts as an amplitude-dependent frequency multiplier.
BW of ADC \geq BW of Folding Circuit
- With S/H, all inputs to the folding circuit arrive at the same time.
 - The folding circuit is no longer an amplitude-dependent frequency multiplier
 - BW of the ADC is now limited by the BW of the S/H circuit
 - Settling time of the folding and interpolating preprocessor is critical

Single S/H versus Distributed S/H:

- Single S/H requires high dynamic range for low THD
- Dynamic range requirement for distributed S/H reduced by the number of S/H stages
- If the coarse quantizer uses the same distributed S/H signals as the fine preprocessor, the coarse/fine synchronization is automatic
- The clock skew between the distributed S/H stages must be small. The clock jitter will have a greater effect on the distributed S/H approach.

Error Sources and Limitations of a Basic Folding ADC

Error Sources:

- Offsets in reference voltages due to resistor mismatch
- Preamp offset (reduced by large W/L for low $V_{GS}-V_T$, with common-centroid geometry)
- v_{in} feedthrough to reference ladder via C_{gs} of input pairs places a maximum value on ladder resistance which is dependent on the input frequency.
- Folder current-source mismatches (gives signal-dependent error \Rightarrow distortion)
- Comparator kickback (driving nodes should be low impedance)
- Comparator metastability condition (uncertainty of comparator output)
- Misalignment between coarse and fine quantization outputs (large code errors possible)

Sampling Speed Limitations:

- Folding output settling time
- Comparator settling time
- Clock distribution and layout
- Clock jitter

Input Bandwidth Limitations:

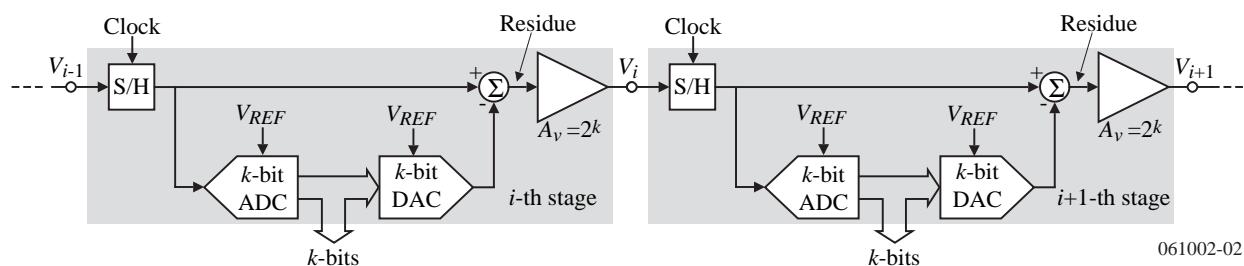
- Maximum folding signal frequency $\geq (F/2) \cdot f_{in}$, unless a S/H is used
- Distortion due to limited preamplifier linear range and frequency dependent delay
- Distortion due to the limited linear range and frequency dependent delay of the folder
- Parasitic capacitance of routing to comparators

HIGH-SPEED, HIGH-RESOLUTION ADCs

Multiple-Bit, Pipeline Analog-Digital Converters

A compromise between speed and resolution is to use a pipeline ADC with multiple bits/stage.

i -th stage of a k -bit per stage pipeline ADC with residue amplification:

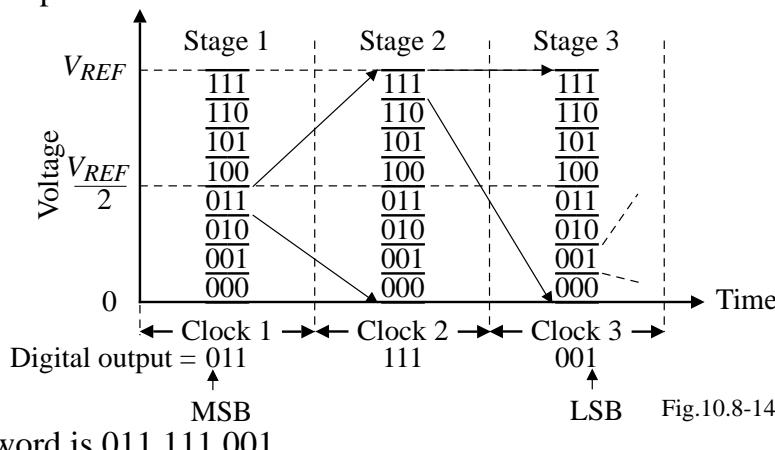


$$\text{Residue voltage} = V_{i-1} - \left(\frac{b_0}{2} + \frac{b_1}{2^2} + \cdots + \frac{b_{k-2}}{2^{k-1}} + \frac{b_{k-1}}{2^k} \right) V_{REF}$$

Potential specifications range from 100-300 Msps and 10 to 14 bits.

A 3-Stage, 3-Bit Per Stage Pipeline ADC

Illustration of the operation:



Converted word is 011 111 001

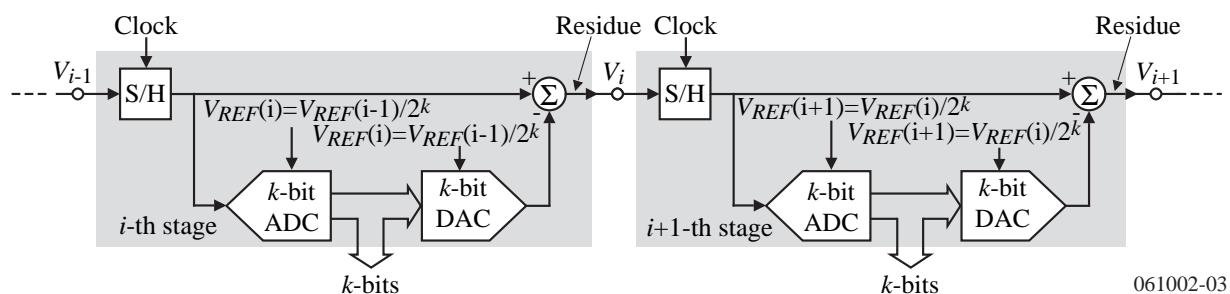
Comments:

- Only 21 comparators are required for this 9-bit ADC
- Conversion occurs in three clock cycles
- The residue amplifier will cause a bandwidth limitation,

$$GB = 50\text{MHz} \rightarrow f_{3\text{dB}} = \frac{50\text{MHz}}{2^3} \approx 6\text{MHz}$$

Multiple-Bit, Pipeline Analog-Digital Converters - Subranging

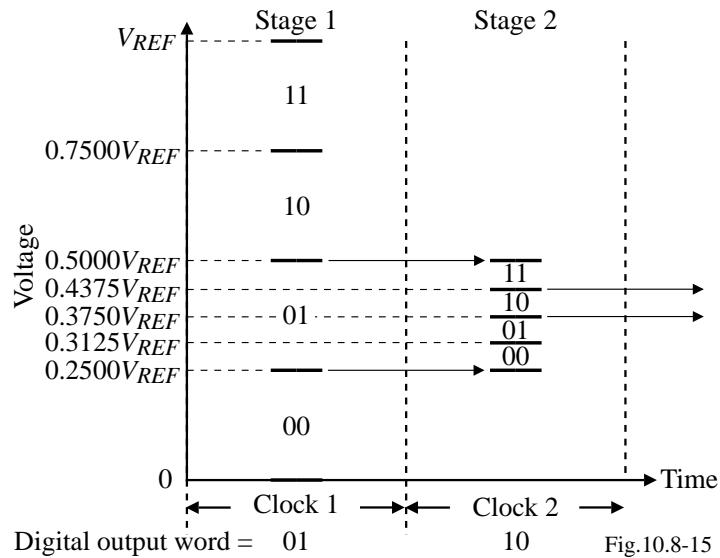
The amplification of $A_v = 2^k$ for each stage places a bandwidth limitation on the converter. The subranging technique shown below eliminates this problem.



Note: the reference voltage of the previous stage ($i-1$) is divided by 2^k to get the reference voltage for the present stage (i), $V_{REF}(i)$, and so forth.

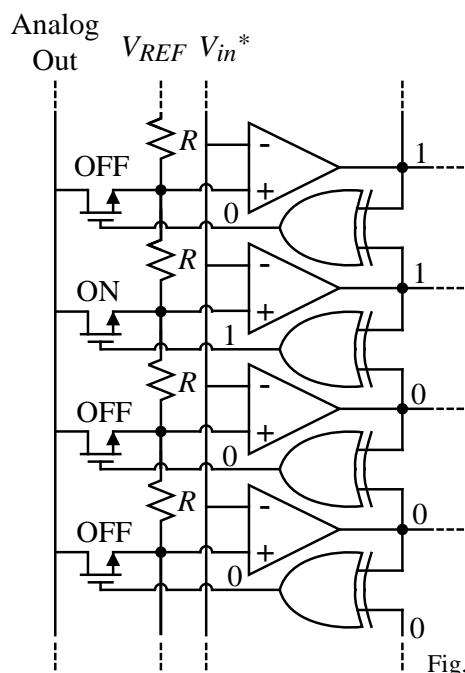
Subranging, Multiple-Bit, Pipeline ADCs

Illustration of a 2-stage, 2-bits/stage pipeline ADC:



Implementation of the DAC in the Multiple-Bit, Pipeline ADC

Circuit:



Comments:

- A good compromise between area and speed
- The ADC does not need to be a flash or parallel if speed is not crucial
- Typical performance is 10 bits at 50Msamples/sec

Example 380-2 - Examination of error in subranging for a 2-stage, 2-bits/stage pipeline ADC

The stages of the 2-stage, 2-bits/stage pipeline ADC shown below are ideal. However, the second stage divides V_{REF} by 2 rather than 4. Find the $\pm INL$ and $\pm DNL$ for this ADC.

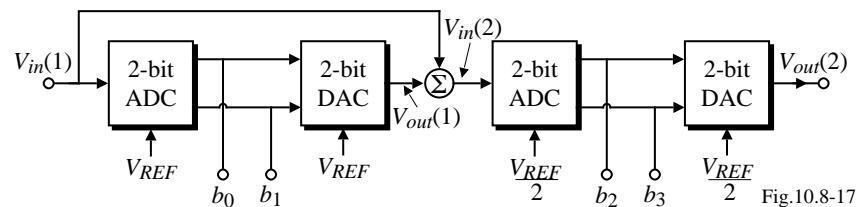


Fig.10.8-17

Solution

Examination of the first stage shows that its output, $V_{out}(1)$ changes at

$$\frac{V_{in}(1)}{V_{REF}} = \frac{1}{4}, \frac{2}{4}, \frac{3}{4}, \text{ and } \frac{4}{4}.$$

The output of the first stage will be

$$\frac{V_{out}(1)}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4}.$$

The second stage changes at

$$\frac{V_{in}(2)}{V_{REF}} = \frac{1}{8}, \frac{2}{8}, \frac{3}{8}, \text{ and } \frac{4}{8}$$

where

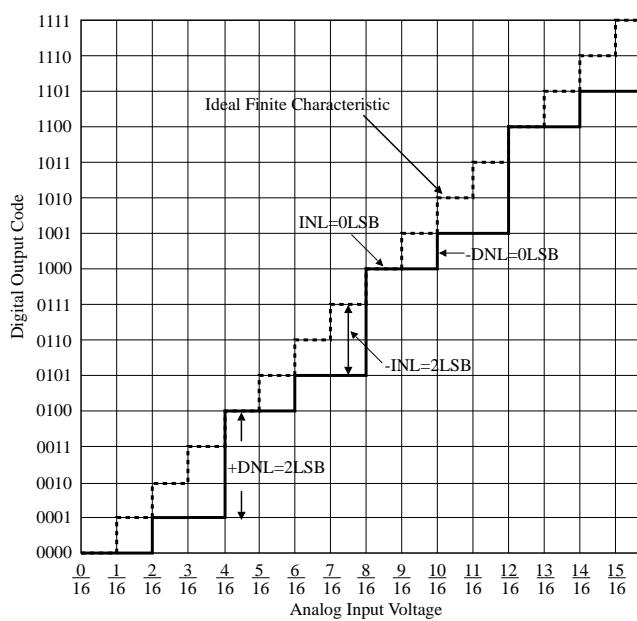
$$V_{in}(2) = V_{in}(1) - V_{out}(1).$$

The above relationships permit the information given in the following table.

Example 380-2 - Continued

Output digital word for Ex. 380-2:

$V_{in}(1)$	b_0	b_1	$V_{out}(1)$	$V_{in}(2)$	b_2	b_3	Ideal Output
V_{REF}			V_{REF}	V_{REF}			$b_0 \ b_1 \ b_2 \ b_3$
0	0	0	0	0	0	0	0 0 0 0
$1/16$	0	0	0	$1/16$	0	0	0 0 0 1
$2/16$	0	0	0	$2/16$	0	1	0 0 1 0
$3/16$	0	0	0	$3/16$	0	1	0 0 1 1
$4/16$	0	1	$4/16$	0	0	0	1 0 0 0
$5/16$	0	1	$4/16$	$1/16$	0	0	0 1 0 1
$6/16$	0	1	$4/16$	$2/16$	0	1	0 1 1 0
$7/16$	0	1	$4/16$	$3/16$	0	1	0 1 1 1
$8/16$	1	0	$8/16$	0	0	1	0 0 0 0
$9/16$	1	0	$8/16$	$1/16$	0	0	1 0 0 1
$10/16$	1	0	$8/16$	$2/16$	0	1	1 0 1 0
$11/16$	1	0	$8/16$	$3/16$	0	1	1 0 1 1
$12/16$	1	1	$12/16$	0	0	1	1 0 0 0
$13/16$	1	1	$12/16$	$1/16$	0	0	1 1 0 1
$14/16$	1	1	$12/16$	$2/16$	0	1	1 1 1 0
$15/16$	1	1	$12/16$	$3/16$	0	1	1 1 1 1

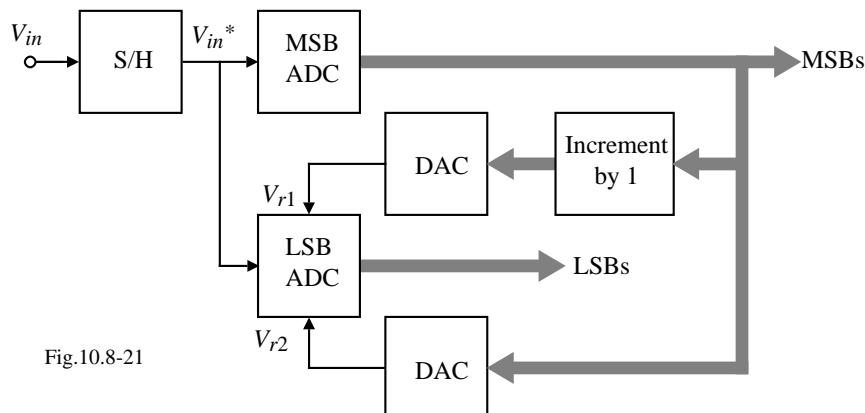


Comparing the actual digital output word with the ideal output word gives the following:
 $+INL = 0LSB$, $-INL = 0111-0101 = -2LSB$, $+DNL = (1000-0101) - 1LSB = +2LSB$, and
 $-DNL = (0101-0100) - 1LSB = 0LSB$.

Example of a Multiple-Bit, Pipeline ADC

Two-stages with 5-bits per stage resulting in a 10-bit ADC with a sampling rate of 5Msamples/second.

Architecture:



Features:

- Requires only $2n/2-1$ comparators
- *LSBs* decoded using 31 preset charge redistribution capacitor arrays
- Reference voltages used in the *LSBs* are generated by the *MSB* ADC
- No op amps are used

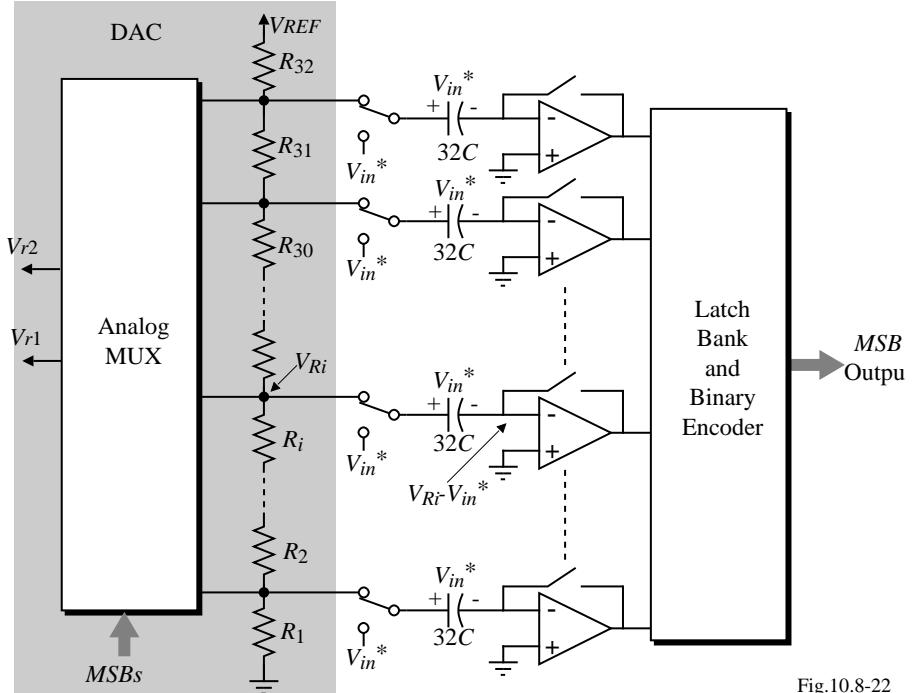
Example of a Multiple-Bit, Pipeline ADC - Continued

MSB Conversion:

Operation:

1.) Sample V_{in}^* on each $32C$ capacitance autozeroing the comparators

2.) Connect each comparator to a node of the resistor string generating a thermometer code.



Example of a Multiple-Bit, Pipeline ADC - Continued

LSB Conversion:

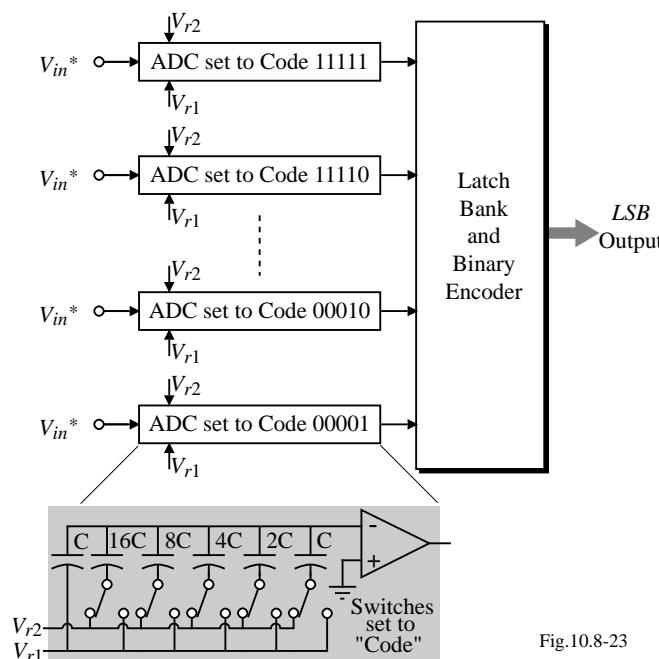


Fig.10.8-23

Operation:

- 1.) MSB comparators are preset to each of the 31 possible digital codes.
- 2.) V_{r1} and V_{r2} are derived from the MSB conversion.
- 3.) Preset comparators will produce a thermometer code to the encoder.

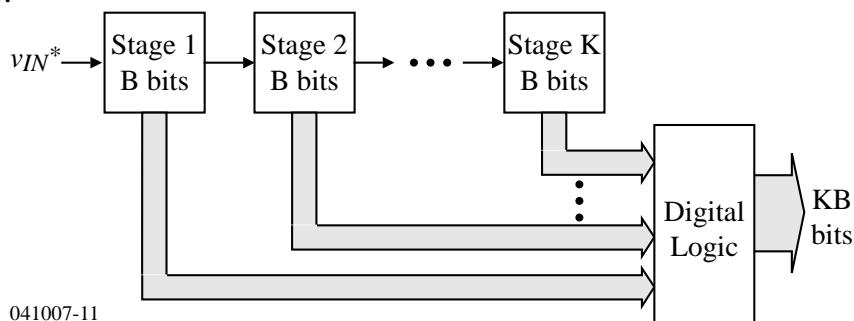
Comments:

- Requires two full clock cycles
- Reuses the comparators
- Accuracy limited by resistor string and its dynamic loading
- Accuracy also limited by the capacitor array
- Comparator is a 3-stage, low-gain, wide-bandwidth, using internal autozeroing

Digital Error Correction

Like many of the accuracy enhancing techniques, there are particular applications where certain correcting techniques are useful. In the pipeline, analog-digital converter, a technique called digital error correction is used to remove the imperfections of the components.

Pipeline ADC:



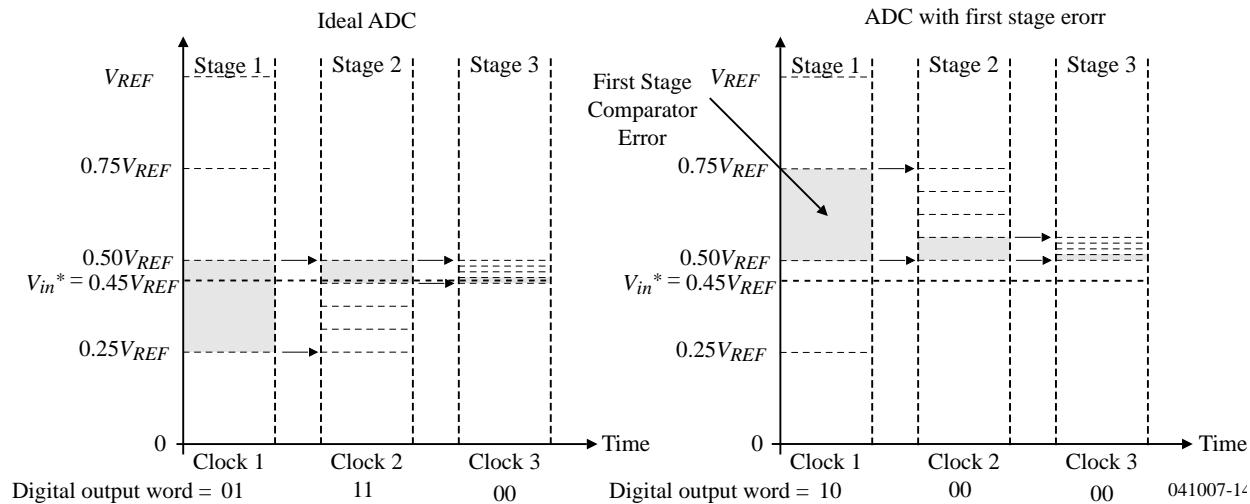
041007-11

Operation:

- 1.) Stage 1 resolves the analog input signal to within one of B subranges which determines the first B bits.
- 2.) Stage 1 then creates the analog residue (analog input – quantized analog output) and passes on to Stage 2 by either amplifying or subranging.
- 3.) Stage 2 repeats this process which ends with Stage K.

Comparator Error in a Pipeline ADC

Subranging Pipeline ADC Example ($B = 2, K = 3$):

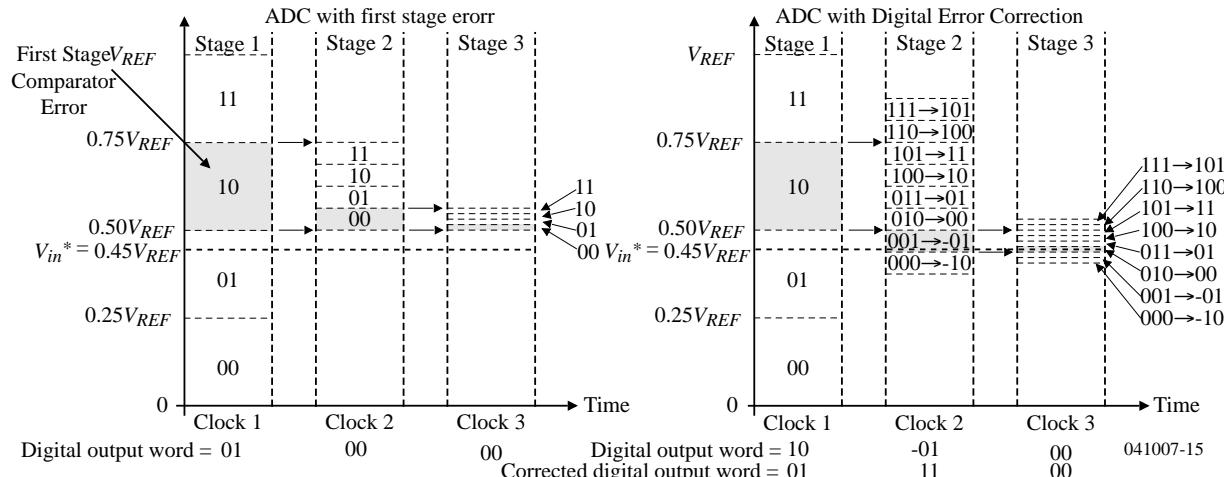


Note that if the comparator in the first stage makes the wrong choice, the converter cannot recover as shown in the example on the right.

Digital Error Correction – Continued

Digital error correction uses one of the bits of each stage (except the first) to correct for any errors caused by the previous stage.

Subranging Pipeline ADC Example ($B = 2, K = 3$) using Digital Error Correction:



Comments:

- Add a correcting bit to the following stage to correct for errors in the previous stage.
- The subranging or amplification of the next stage does not include the correcting bit.
- Correction can be done after all stages of the pipeline ADC have converted or after each individual stage.

12-Bit Pipeline ADC with Digital Error Correction & Self-Calibration[†]

Digital Error Correction:

- Avoids saturation of the next stage
- Reduces the number of missing codes
- Relaxed specifications for the comparators
- Compensates for wrong decisions in the coarse quantizers

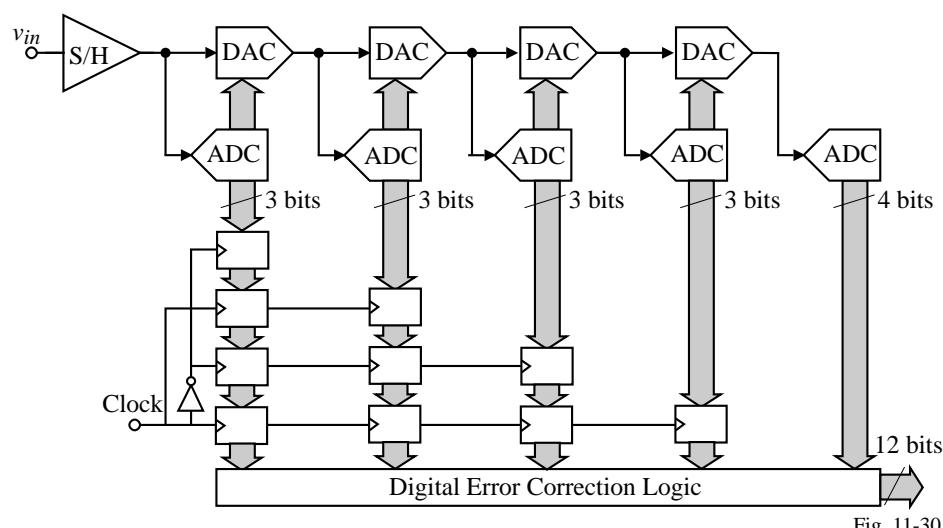


Fig. 11-30

Self-Calibration:

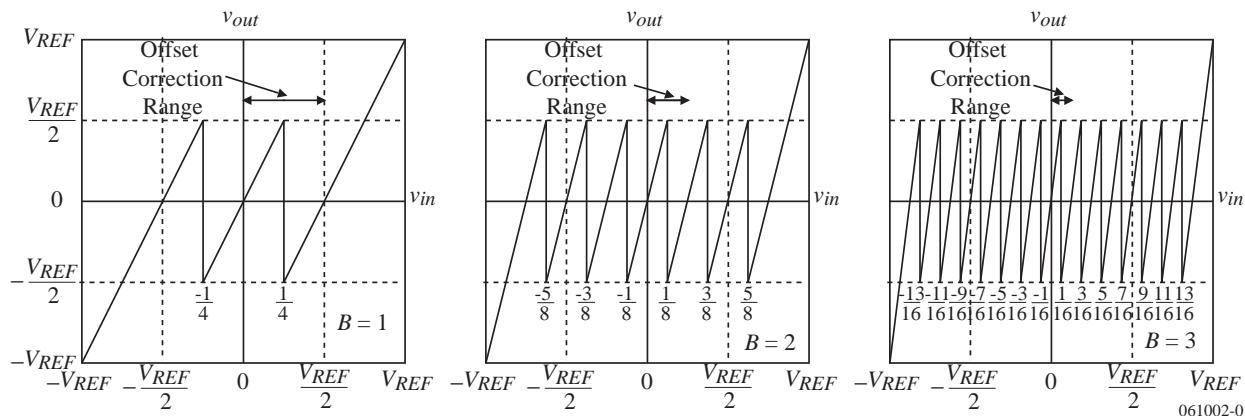
- Can calibrate the effects of the DAC nonlinearity and gain error
- Can be done by digital or analog methods or both

[†] J. Goes, et. al., CICC'96
CMOS Analog Circuit Design

Digital Error Correction using B.5-Bit Pipeline Stages

The top and bottom comparators can be removed to achieve digital error correction more efficiently.

Input-output characteristics for different per-stage resolutions ($B = 1, 2$, and 3):



If all else is ideal, the offset voltage correction range is equal to $\pm \frac{V_{REF}}{2^{B+1}}$.

TIME-INTERLEAVED ADC CONVERTERS

Time-Interleaved Analog-Digital Converters

Slower ADCs are used
in parallel.

Illustration:

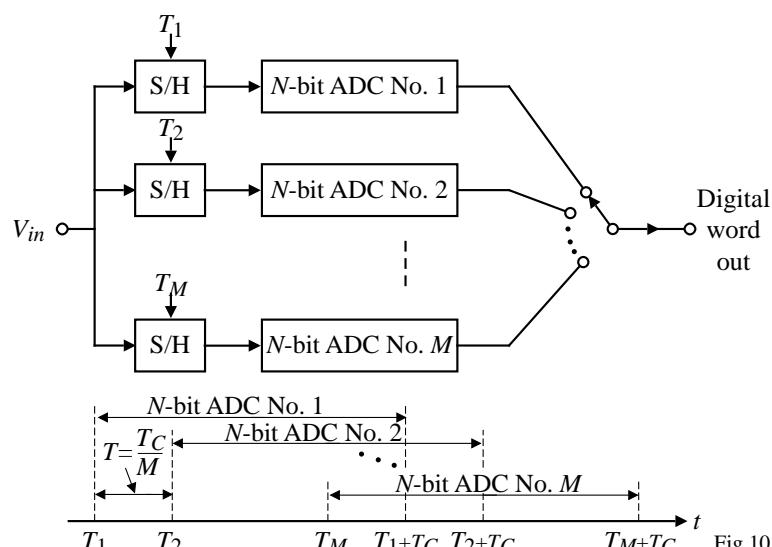


Fig.10.8-20

Comments:

- Can get the same throughput with less chip area
- If $M = N$, then a digital word is converted at every clock cycle
- Multiplexer and timing become challenges at high speeds

SUMMARY

Type of ADC	Primary Advantage	Primary Disadvantage
Flash or parallel	Fast	Area is large if $N > 6$
Interpolating	Fast	Requires accurate interpolation
Folding	Fast	Bandwidth increases if no S/H used
Multiple-Bit, Pipeline	Increased number of bits	Slower than flash
Time-interleaved	Small area with large throughput	Precise timing and fast multiplexer

Typical Performance:

- 6-8 bits
- 500-2000 Msamples/sec.
- The $ENOB$ at the Nyquist frequency is typically 1-2 bits less than the $ENOB$ at low frequencies.
- Power is approximately 0.3 to 1W

LECTURE 390 – OVERSAMPLING ADCS – PART I

LECTURE ORGANIZATION

Outline

- Introduction
- Delta-sigma modulators
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 698-705

INTRODUCTION

What is an oversampling converter?

An oversampling converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve a high degree of resolution.

- What is the range of oversampling?

The oversampling ratio, called M , is a ratio of the clock frequency to the Nyquist frequency of the input signal. This oversampling ratio can vary from 8 to 256.

- The resolution of the oversampled converter is proportional to the oversampled ratio.
- The bandwidth of the input signal is inversely proportional to the oversampled ratio.

- What are the advantages of oversampling converters?

Very compatible with VLSI technology because most of the converter is digital

High resolution

Single-bit quantizers use a one-bit DAC which has no INL or DNL errors

Provide an excellent means of trading precision for speed (16-18 bits at 50ksps to 8-10 bits at sampling rates of 5-10Msps).

- What are the disadvantages of oversampling converters?

Difficult to model and simulate

Limited in bandwidth to the clock frequency divided by the oversampling ratio

Nyquist Versus Oversampled ADCs

Conventional Nyquist ADC Block Diagram:

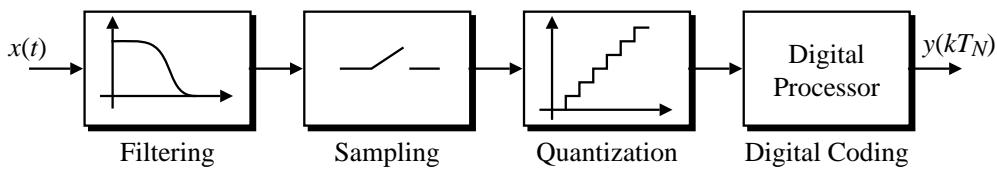


Fig.10.9-01

Oversampled ADC Block Diagram:

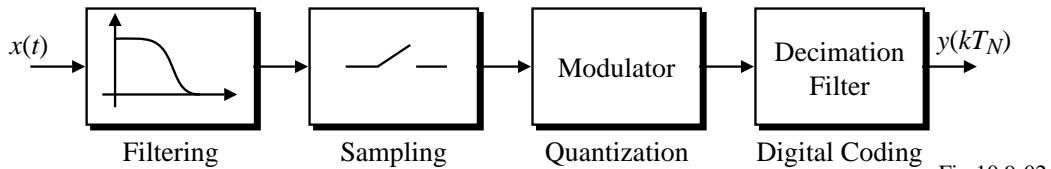


Fig.10.9-02

Components:

- Filter - Prevents possible aliasing of the following sampling step.
- Sampling - Necessary for any analog-to-digital conversion.
- Quantization - Decides the nearest analog voltage to the sampled voltage (determines the resolution).
- Digital Coding - Converts the quantizer information into a digital output signal.

Frequency Spectrum of Nyquist and Oversampled Converters

Definitions:

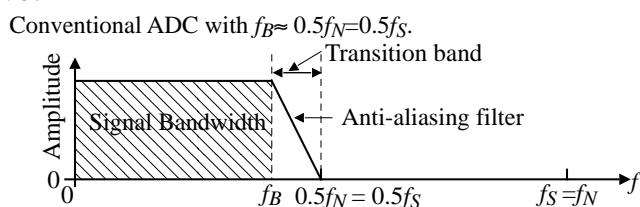
f_B = analog signal bandwidth

f_N = Nyquist frequency (two times f_B)

f_S = sampling or clock frequency

$M = \frac{f_S}{f_N} = \frac{f_S}{2f_B}$ = oversampling ratio

Frequency perspective:



Oversampled ADC with $f_B \approx 0.5f_N < f_S$.

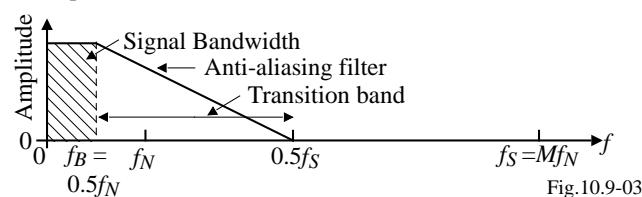
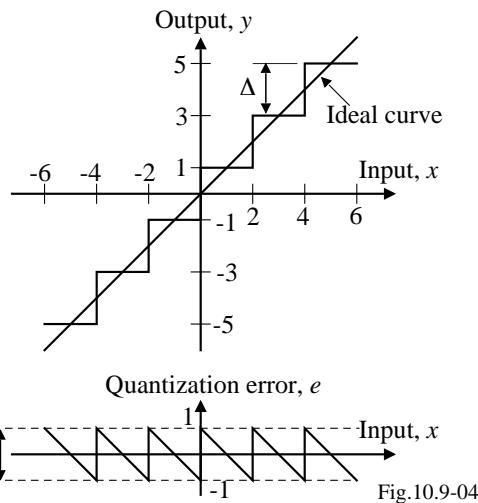


Fig.10.9-03

Quantization Noise of a Conventional (Nyquist) ADC

Multilevel Quantizer:



The quantized signal y can be represented as,

$$y = Gx + e$$

where

G = gain of the ADC, normally 1

e = quantization error

The mean square value of the quantization error is

$$e_{rms}^2 = S_Q = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e(x)^2 dx = \frac{\Delta^2}{12}$$

Quantization Noise of a Conventional (Nyquist) ADC - Continued

Spectral density of the sampled noise:

When a quantized signal is sampled at f_S ($= 1/\tau$), then all of its noise power folds into the frequency band from 0 to $0.5f_S$. Assuming that the noise power is white, the spectral density of the sampled noise is,

$$E(f) = e_{rms} \sqrt{\frac{2}{f_S}} = e_{rms} \sqrt{2\tau}$$

where $\tau = 1/f_S$ and f_S = sampling frequency

The inband noise energy n_o is

$$n_o^2 = \int_0^{f_B} E^2(f) df = e_{rms}^2 (2f_B\tau) = e_{rms}^2 \left(\frac{2f_B}{f_S} \right) = \frac{e_{rms}^2}{M} \Rightarrow n_o = \frac{e_{rms}}{\sqrt{M}}$$

What does all this mean?

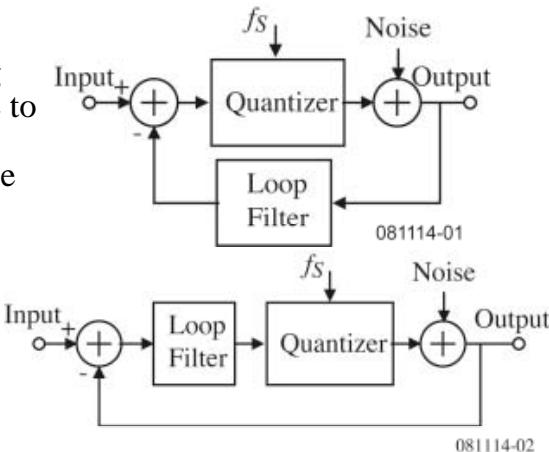
- One way to increase the resolution of an ADC is to make the bandwidth of the signal, f_B , less than the clock frequency, f_S . In other words, give up bandwidth for precision.
- However, it is seen from the above that a doubling of the oversampling ratio M , only gives a decrease of the inband noise, n_o , of $1/\sqrt{2}$ which corresponds to -3dB decrease or an increase of resolution of 0.5 bits

As a result, increasing the oversampling ratio of a Nyquist analog-digital converter is not a very good method of increasing the resolution.

Oversampled Analog-Digital Converters

Classification of oversampled ADCs:

- 1.) Straight-oversampling - The quantization noise is assumed to be equally distributed over the entire frequency range of dc to $0.5f_S$. This type of converter is represented by the Nyquist ADC.
- 2.) Predictive oversampling - Uses noise shaping plus oversampling to reduce the inband noise to a much greater extent than the straight-oversampling ADC. Both the signal and noise quantization spectrums are shaped.
- 3.) Noise-shaping oversampling - Similar to the predictive oversampling except that only the noise quantization spectrum is shaped while the signal spectrum is preserved.



The noise-shaping oversampling ADCs are also known as *delta-sigma* ADCs. We will only consider the delta-sigma type oversampling ADCs.

DELTA-SIGMA MODULATORS

General block diagram of an oversampled ADC

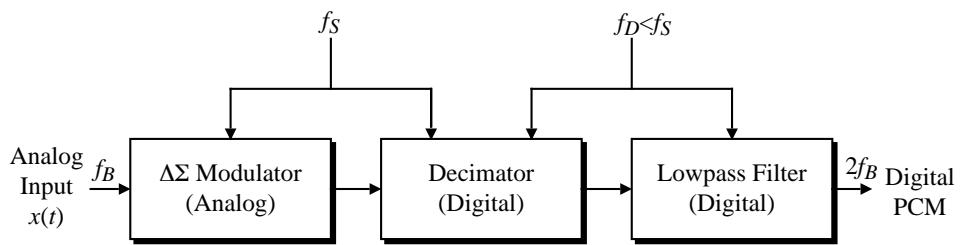


Fig.10.9-07

Components of the Oversampled ADC:

- 1.) $\Delta\Sigma$ Modulator - Also called the noise shaper because it can shape the quantization noise and push the majority of the inband noise to higher frequencies. It modulates the analog input signal to a simple digital code, normally a one-bit serial stream using a sampling rate much higher than the Nyquist rate.
- 2.) Decimator - Also called the down-sampler because it down samples the high frequency modulator output into a low frequency output and does some pre-filtering on the quantization noise.
- 3.) Digital Lowpass Filter - Used to remove the high frequency quantization noise and to preserve the input signal.

Note: Only the modulator is analog, the rest of the circuitry is digital.

First-Order, Delta-Sigma Modulator

Block diagram of a first-order, delta-sigma modulator:

Components:

- Integrator (continuous or discrete time)
- Coarse quantizer (typically two levels)
 - A/D which is a comparator for two levels
 - D/A which is a switch for two levels

First-order modulator output for a sinusoidal input:

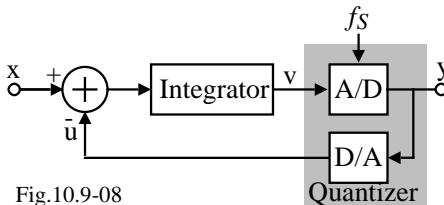
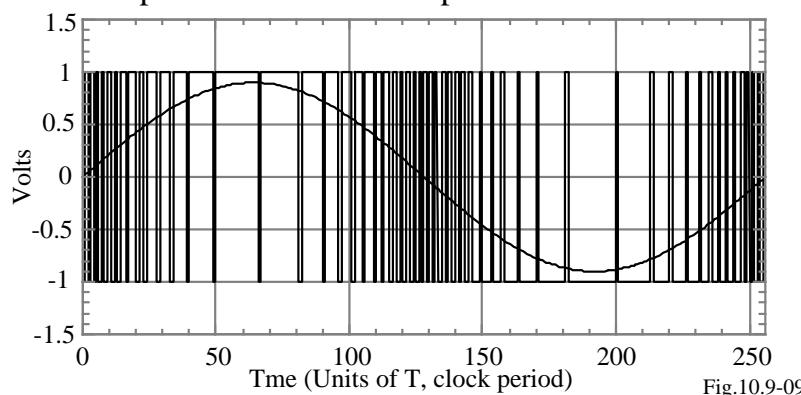


Fig.10.9-08

Sampled-Data Model of a First-Order $\Delta\Sigma$ Modulator

Writing the following relationships,

$$y[nT_s] = q[nT_s] + v[nT_s]$$

$$v[nT_s] = w[(n-1)T_s] + v[(n-1)T_s]$$

$$\therefore y[nT_s] = q[nT_s] + w[(n-1)T_s] + v[(n-1)T_s] = q[nT_s] + \{x[(n-1)T_s] - y[(n-1)T_s]\} + v[(n-1)T_s]$$

But the first equation can be written as

$$y[(n-1)T_s] = q[(n-1)T_s] + v[(n-1)T_s] \rightarrow q[(n-1)T_s] = y[(n-1)T_s] - v[(n-1)T_s]$$

Substituting this relationship into the above gives,

$$y[nT_s] = x[(n-1)T_s] + q[nT_s] - q[(n-1)T_s]$$

Converting this expression to the z -domain gives,

$$Y(z) = z^{-1}X(z) + (1-z^{-1})Q(z)$$

Definitions:

$$\text{Signal Transfer Function} = STF = \frac{Y(z)}{X(z)} = z^{-1}$$

$$\text{Noise Transfer Function} = NTF = \frac{Y(z)}{Q(z)} = 1-z^{-1}$$

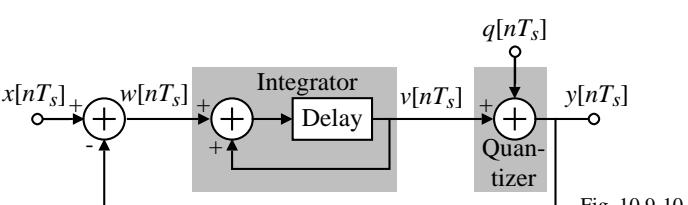
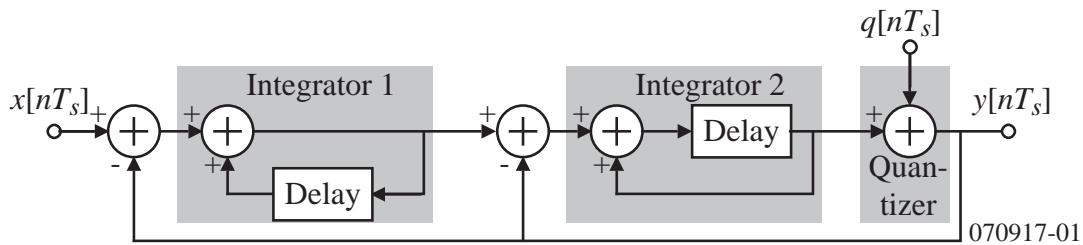


Fig. 10.9-10

Higher-Order $\Delta\Sigma$ Modulators

A second-order, $\Delta\Sigma$ modulator:



070917-01

It can be shown that the z -domain output is,

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^2Q(z)$$

The general, L -th order $\Delta\Sigma$ modulator has the following form,

$$Y(z) = z^{-K}X(z) + (1-z^{-1})^LQ(z)$$

Note that noise transfer function, NTF , has L -zeros at the origin resulting in a high-pass transfer function. K depends on the architecture where $K \leq L$.

This high-pass characteristic reduces the noise at low frequencies which is the key to extending the dynamic range within the bandwidth of the converter.

Noise Transfer Function

The noise transfer function can be written as,

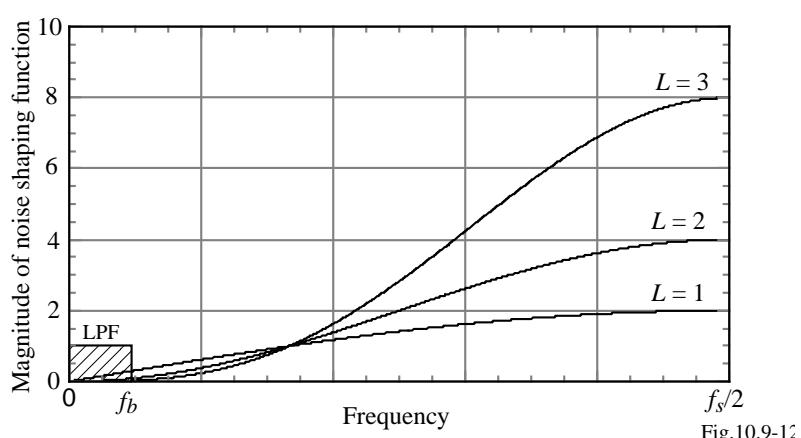
$$NTF_Q(z) = (1-z^{-1})^L$$

Evaluate $(1-z^{-1})$ by replacing z by $e^{j\omega T_s}$ to get

$$(1-z^{-1}) = (1 - e^{-j\pi f/f_s}) \left(\frac{2j}{2j} \right) \frac{e^{j\pi f/f_s}}{e^{-j\pi f/f_s}} = \left(\frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \right) 2j e^{-j\pi f/f_s} = \sin(\pi f T_s) 2j e^{-j\pi f/f_s}$$

$$|1-z^{-1}| = (2 \sin \pi f T_s) \quad \rightarrow \quad |NTF_Q(f)| = (2 \sin \pi f T_s)^L$$

Magnitude of the noise transfer function,



Note: Single-loop modulators having noise shaping characteristics of the form $(1-z^{-1})^L$ are unstable for $L > 2$ unless an L -bit quantizer is used.

In-Band Rms Noise of Single-Loop $\Delta\Sigma$ Modulator

Assuming noise power is white, the power spectral density of the $\Delta\Sigma$ modulator, $S_E(f)$, is

$$S_E(f) = |NTF_Q(f)|^2 \frac{|S_Q(f)|}{f_s}$$

Next, integrate $S_E(f)$ over the signal band to get the inband noise power using $S_Q = \frac{\Delta^2}{12}$

$$\therefore S_B = \frac{1}{f_s} \int_{-f_b}^{f_b} (2\sin\pi f T_s) 2L \frac{\Delta^2}{12} df \approx \left(\frac{\pi^2 L}{2L+1}\right) \left(\frac{1}{M^{2L+1}}\right) \left(\frac{\Delta^2}{12}\right) \quad \text{where } \sin\pi f T_s \approx \pi f T_s \text{ for } M \gg 1.$$

Therefore, the in-band, rms noise is given as

$$n_0 = \sqrt{S_B} = \left(\frac{\pi L}{\sqrt{2L+1}}\right) \left(\frac{1}{M^{L+0.5}}\right) \left(\frac{\Delta}{\sqrt{12}}\right) = \left(\frac{\pi L}{\sqrt{2L+1}}\right) \left(\frac{1}{M^{L+0.5}}\right) e_{rms}$$

Note that as the $\Delta\Sigma$ is a much more efficient way of achieving resolution by increasing M .

$$n_0 \propto \frac{e_{rms}}{M^{L+0.5}} \quad \Rightarrow \quad \text{Doubling of } M \text{ leads to a } 2^{L+0.5} \text{ decrease of in-band noise}$$

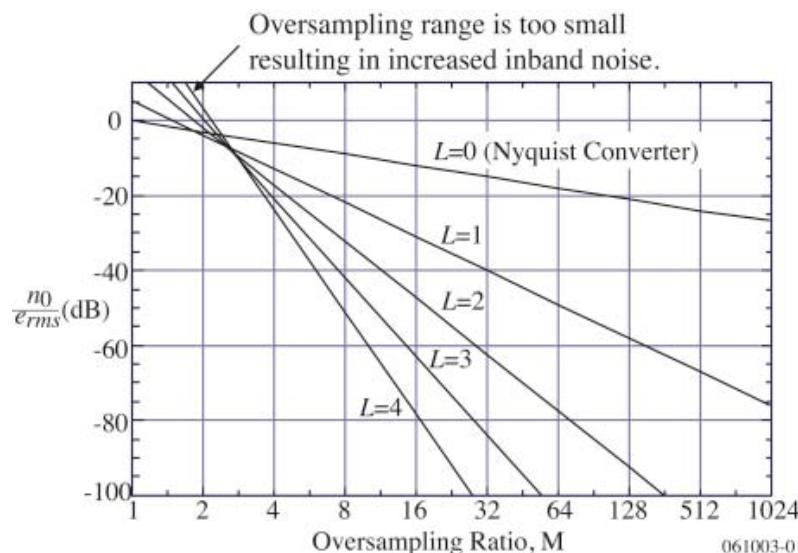
resulting in an extra $L+0.5$ bits of resolution!

∴ The increase of the oversampling ratio is an excellent method of increasing the resolution of a $\Delta\Sigma$ oversampling analog-digital converter.

Illustration of RMS Noise Versus Oversampling Ratio for Single Loop $\Delta\Sigma$ Modulators

Plotting n_0/e_{rms} gives,

$$\frac{n_0}{e_{rms}} = \left(\frac{\pi L}{\sqrt{2L+1}}\right) \left(\frac{1}{M^{L+0.5}}\right)$$



Dynamic Range of $\Delta\Sigma$ Analog-Digital Converters

Oversampled $\Delta\Sigma$ Converter:

The dynamic range, DR , for a 1 bit-quantizer with level spacing $\Delta = V_{REF}$, is

$$DR^2 = \frac{\text{Maximum signal power}}{S_B(f)} = \frac{\left(\frac{\Delta}{2\sqrt{2}}\right)^2}{\left(\frac{\pi^2 L}{2L+1}\right)\left(\frac{1}{M^{2L+1}}\right)\left(\frac{\Delta^2}{12}\right)} = \frac{3}{2} \frac{2L+1}{\pi^2 L} M^{2L+1}$$

Nyquist Converter:

The dynamic range of a N -bit Nyquist rate ADC is (now Δ becomes $\approx V_{REF}$ for large N),

$$DR^2 = \frac{\text{Maximum signal power}}{S_Q} = \frac{(V_{REF}/2\sqrt{2})^2}{\Delta^2/12} = \frac{3}{2} 2^{2N} \rightarrow DR = \sqrt{1.5} 2^N$$

Expressing DR in terms of dB (DR_{dB}) and solving for N , gives

$$N = \frac{DR_{dB} - 1.7609}{6.0206} \quad \text{or} \quad DR_{dB} = (6.0206N + 1.7609) \text{ dB}$$

Example: A 16-bit $\Delta\Sigma$ ADC requires about 98dB of dynamic range. For a second-order modulator, M must be 153 or 256 since we must use powers of 2.

Therefore, if the bandwidth is 20kHz, then the clock frequency must be 10.24MHz.

Multibit Quantizers

A single-bit quantizer:

$$\Delta = V_{REF}$$

Advantage is that the DAC is inherently linear.

Multi-bit quantizer:

Consists of an ADC and DAC of B -bits.

$$\Delta = \frac{V_{REF}}{2^{B-1}}$$

Disadvantage is that the DAC is no longer perfectly linear. To get large resolution delta-sigma ADCs requires highly precise DACs.

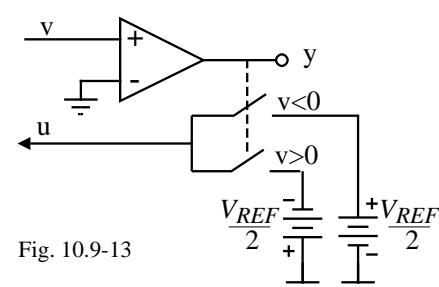
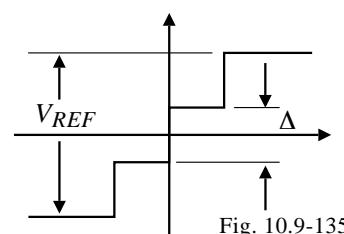


Fig. 10.9-13

Dynamic range of a multibit $\Delta\Sigma$ ADC:

$$DR^2 = \frac{3}{2} \frac{2L+1}{\pi^2 L} M^{2L+1} (2^{B-1})^2$$

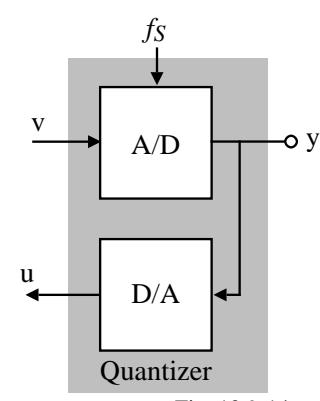


Fig. 10.9-14

Example 390-1 - Tradeoff Between Signal Bandwidth and Accuracy of $\Delta\Sigma$ ADCs

Find the minimum oversampling ratio, M , for a 16-bit oversampled ADC which uses (a.) a 1-bit quantizer and third-order loop, (b.) a 2-bit quantizer and third-order loop, and (c.) a 3-bit quantizer and second-order loop. For each case, find the bandwidth of the ADC if the clock frequency is 10MHz.

Solution

We see that 16-bit ADC corresponds to a dynamic range of approximately 98dB.
 (a.) Solving for M gives

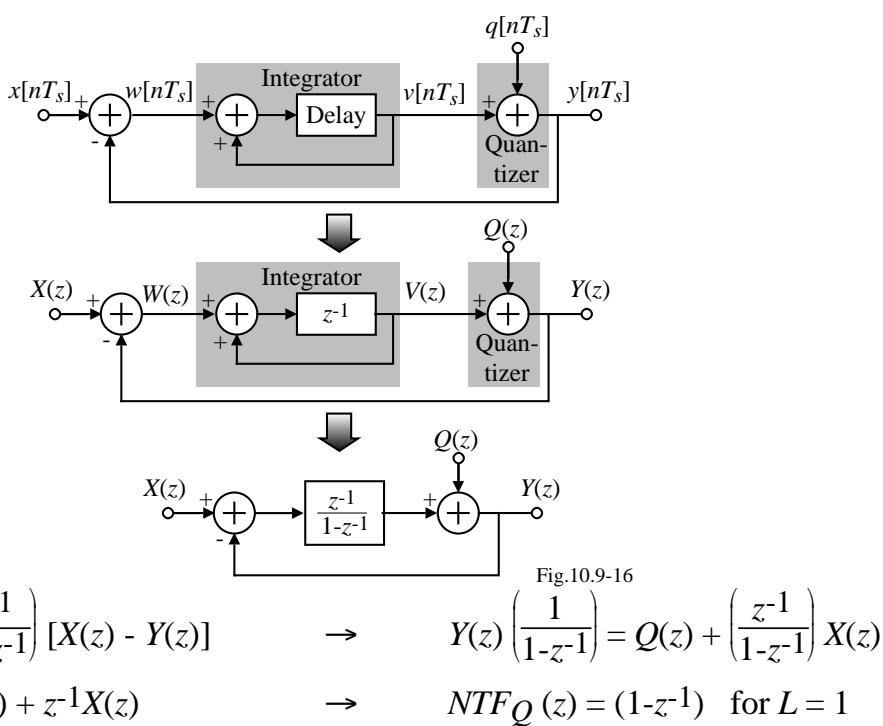
$$M = \left(\frac{2}{3} \frac{DR^2}{2L+1} \frac{\pi^2 L}{(2^{B-1})^2} \right)^{1/(2L+1)}$$

Converting the dynamic range to 79,433 and substituting into the above equation gives a minimum oversampling ratio of $M = 48.03$ which would correspond to an oversampling rate of 64. Using the definition of M as $f_c/2f_B$ gives f_B as $10\text{MHz}/2 \cdot 64 = 78\text{kHz}$.

(b.) and (c.) For part (b.) and (c.) we obtain a minimum oversampling rates of $M = 32.53$ and 96.48, respectively. These values correspond to oversampling rates of 32 and 128, respectively. The bandwidth of the converters is 312kHz for (b.) and 78kHz for (c.).

Z-Domain Equivalent Circuits

The modulator structures are much easier to analyze and interpret in the z-domain.



Cascaded, Second-Order $\Delta\Sigma$ Modulator

Since the single-loop architecture with order higher than 2 are unstable, it is necessary to find alternative architectures that allow stable higher order modulators.

A cascaded, second-order structure:

$$Y_1(z) = (1-z^{-1})Q_1(z) + z^{-1}X(z)$$

$$X_2(z) = \left(\frac{z^{-1}}{1-z^{-1}} \right) (X(z) - Y_1(z))$$

$$= \left(\frac{z^{-1}}{1-z^{-1}} \right) X(z) - \left(\frac{z^{-1}}{1-z^{-1}} \right) [(1-z^{-1})Q_1(z) + z^{-1}X(z)]$$

$$Y_2(z) = (1-z^{-1})Q_2(z) + z^{-1}X_2(z) = (1-z^{-1})Q_2(z) + \left(\frac{z^{-2}}{1-z^{-1}} \right) X(z) - z^{-2}Q_1(z) - \left(\frac{z^{-2}}{1-z^{-1}} \right) X(z)$$

$$= (1-z^{-1})Q_2(z) - z^{-2}Q_1(z)$$

$$Y(z) = Y_2(z) - z^{-1}Y_1(z) + z^{-2}Y_1(z) = (1-z^{-1})Y_2(z) + z^{-2}Y_1(z)$$

$$= (1-z^{-1})^2Q_2(z) - (1-z^{-1})z^{-2}Q_1(z) + (1-z^{-1})z^{-2}Q_1(z) + z^{-3}X(z) = (1-z^{-1})^2Q_2(z) + z^{-3}X(z)$$

$$\therefore Y(z) = (1-z^{-1})^2Q_2(z) + z^{-3}X(z)$$

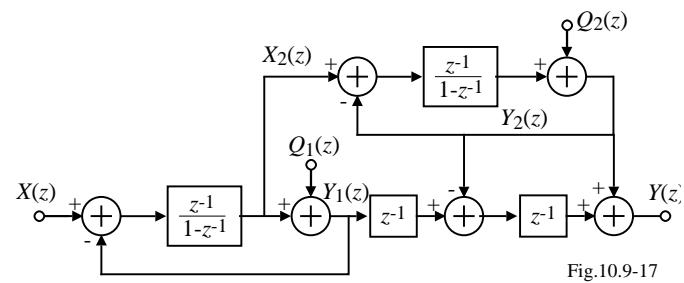


Fig.10.9-17

Third-Order, MASH $\Delta\Sigma$ Modulator

It can be shown that

$$Y(z) = X(z) + (1-z^{-1})^3Q_3(z)$$

This results in a 3rd-order noise shaping and no delay between the input and output.

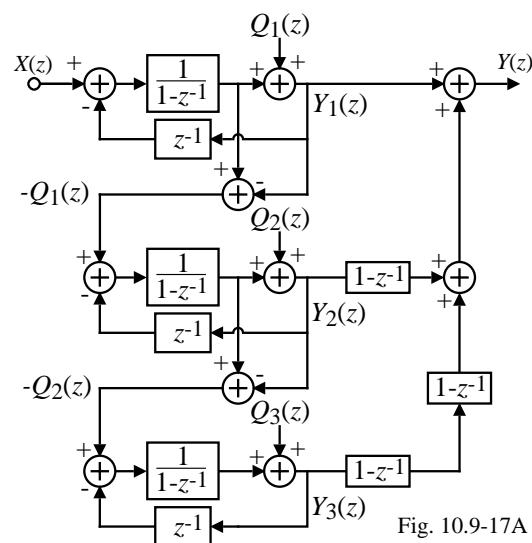
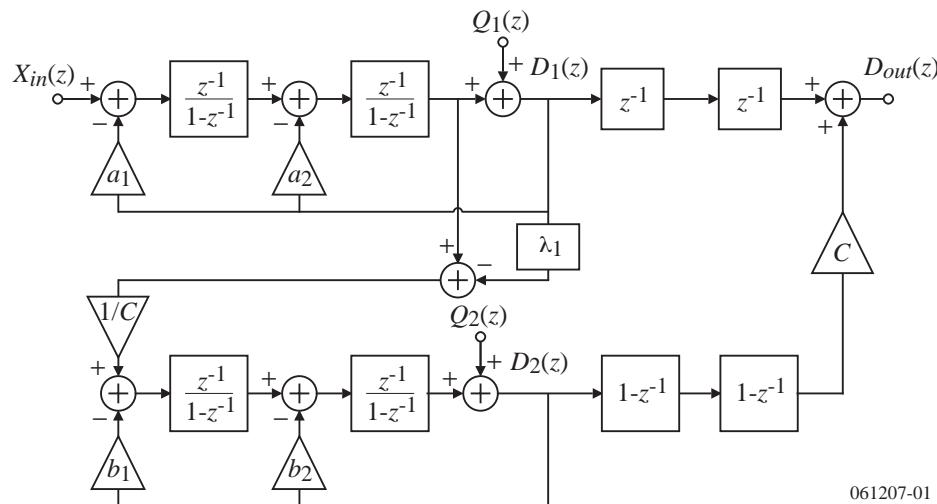


Fig. 10.9-17A

Comments:

- The above structures that eliminate the noise of all quantizers except the last are called **MASH** or multistage architectures.
- Digital error cancellation logic is used to remove the quantization noise of all stages, except that of the last one.

A Fourth-Order, MASH-type Modulator using Scaling of Error Signals[†]

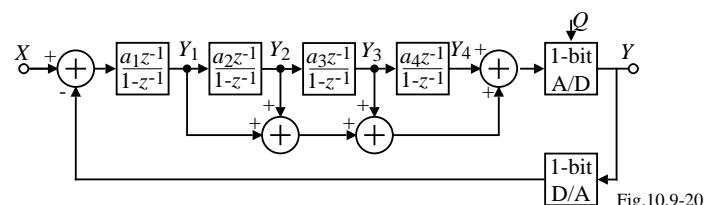


The various transfer functions are ($a_1=1, a_2=2, b_1=1, b_2=2, l_1=2$ and $C = 4$) :

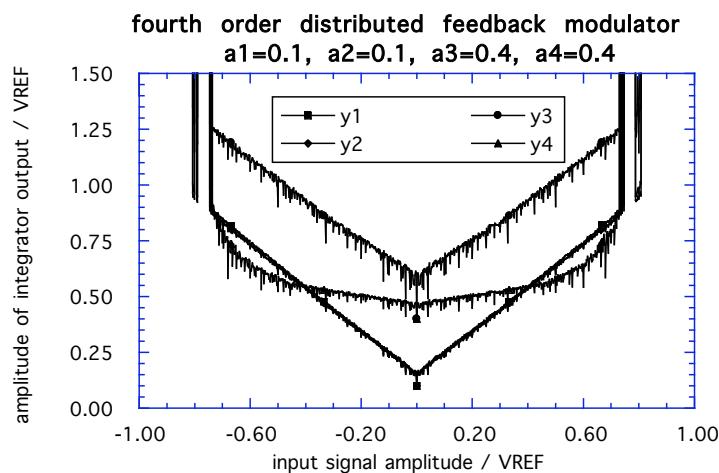
$$\begin{aligned}D_1(z) &= X_{in}(z) + (1-z^{-1})^2 Q_1(z) \\D_2(z) &= (1/C)(-Q_1(z)) + (1-z^{-1})^2 Q_2(z) \\D_{out}(z) &= X_{in}(z) + (1-z^{-1})^4 Q_2(z)\end{aligned}$$

[†] U.S. Patent 5,061,928, Oct. 29, 1991.
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Distributed Feedback $\Delta\Sigma$ Modulator - Fourth-Order



Amplitude of integrator outputs:



Distributed Feedback $\Delta\Sigma$ Modulator - Fourth-Order – Continued

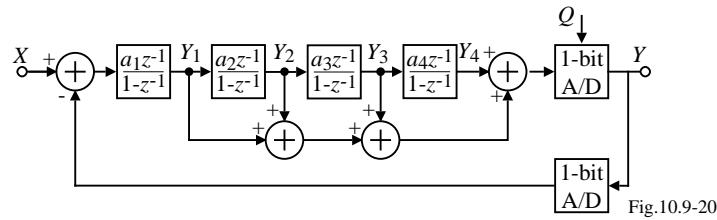
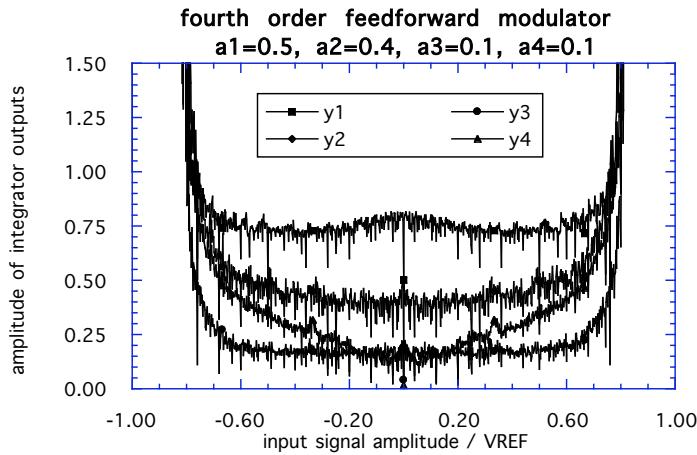


Fig.10.9-20

Amplitude of integrator outputs (Integrator constants have been optimized to minimize the integrator outputs):



Cascaded of a Second-Order Modulator with a First-Order Modulator

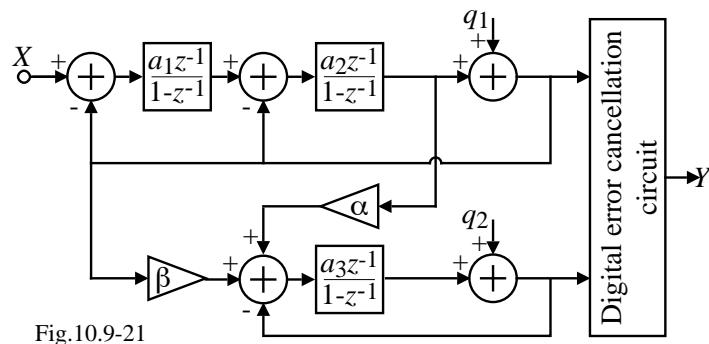


Fig.10.9-21

Comments:

- The stability is guaranteed for cascaded structures
- The maximum input range is almost equal to the reference voltage level for the cascaded structures
- All structures are sensitive to the circuit imperfection of the first stages
- The output of cascaded structures is multi-bit requiring a more complex digital decimator

Integrator Circuits for $\Delta\Sigma$ Modulators

Fundamental block of the $\Delta\Sigma$ modulator:

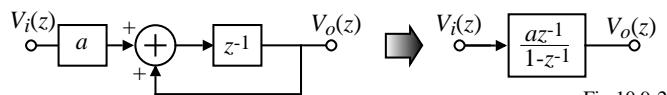


Fig.10.9-22

Fully-Differential, Switched Capacitor Implementation:

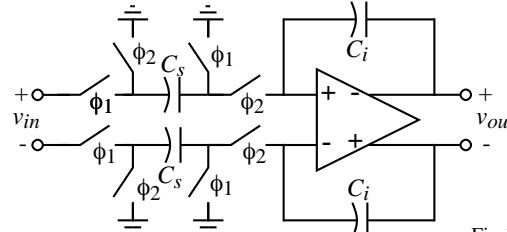


Fig.10.9-23

It can be shown (Chapter 9 of the text) that,

$$\frac{V_{out}(z)}{V_{in}(z)} = \left(\frac{C_s}{C_i} \right) \left(\frac{z^{-1}}{1-z^{-1}} \right) \Rightarrow$$

$$\frac{V_{out}^o(e^{j\omega T})}{V_{in}^o(e^{j\omega T})} = \left(\frac{C_1}{C_2} \right) \frac{e^{-j\omega T/2}}{j2 \sin(\omega T/2)} \left(\frac{\omega T}{\omega T} \right) = \left(\frac{C_1}{j\omega T C_2} \right) \left(\frac{\omega T/2}{\sin(\omega T/2)} \right) (e^{-j\omega T/2})$$

$$\frac{V_{out}^o(e^{j\omega T})}{V_{in}^o(e^{j\omega T})} = (\text{Ideal}) \times (\text{Magnitude error}) \times (\text{Phase error}) \text{ where } \omega_l = \frac{C_1}{T C_2} \Rightarrow \text{Ideal} = \frac{\omega_l}{j\omega}$$

Power Dissipation versus Supply Voltage and Oversampling Ratio

The following is based on the above switched-capacitor integrator:

1.) Dynamic range:

The noise in the band $[-f_s, f_s]$ is kT/C while the noise in the band $[-f_s/2M, f_s/2M]$ is kT/MC . We must multiply this noise by 4; x2 for the sampling and integrating phases and x2 for differential operation.

$$\therefore DR = \frac{V_{DD}^2/2}{4kT/MC_s} = \frac{V_{DD}^2 MC_s}{8kT}$$

2.) Lower bound on the sampling capacitor, C_s : $C_s = \frac{8kT \cdot DR}{V_{DD}^2 M}$

3.) Static power dissipation of the integrator: $P_{int} = I_b V_{DD}$

4.) Settling time for a step input of $V_{o,max}$:

$$I_b = C_i \frac{V_{o,max}}{T_{settle}} = \left(\frac{C_i}{T_{settle}} \right) \left(\frac{C_s}{C_i} V_{DD} \right) = \frac{C_s V_{DD}}{T_{settle}} = C_s V_{DD} (2f_s) = 2Mf_N C_s V_{DD}$$

$$\therefore P_{int} = 2Mf_N C_s V_{DD}^2 = 16kT \cdot DR \cdot f_N$$

Because of additional feedback to the first integrator, the maximum voltage can be $2V_{DD}$.

$$P_{1st-int} = 32kT \cdot DR \cdot f_N$$

SUMMARY

- Oversampled ADCs allow signal bandwidth to be efficiently traded for resolution
- Noise shaping oversampled ADCs preserve the signal spectrum and shape the noise quantization spectrum
- The modulator shapes the noise quantization spectrum with a high pass filter
- The quantizer can be single or multiple bit
 - Single bit quantizers do not require linear DACs because a 1 bit DAC cannot be nonlinear
 - Multiple bit quantizers require ultra linear DACs
- Modulators consist of combined integrators with the goal of high-pass shaping of the noise spectrum and cancellation of all quantizer noise but the last quantizer

LECTURE 400 – OVERSAMPLING ADCS – PART II

LECTURE ORGANIZATION

Outline

- Implementation of $\Delta\Sigma$ modulators
- Decimation and filtering
- Bandpass $\Delta\Sigma$ modulators
- Digital-analog oversampling converters
- Summary

CMOS Analog Circuit Design, 2nd Edition Reference

Pages 705-715

IMPLEMENTATION OF $\Delta\Sigma$ MODULATORS

$\Delta\Sigma$ Modulators – The Analog Part of the Oversampling ADC

Most of today's delta-sigma modulators use fully differential switched capacitor circuits.

Advantages are:

- Doubles the signal swing and increases the dynamic range by 6dB
- Common-mode signals that may couple to the signal through the supply lines and substrate are canceled
- Charge injected by the switches are canceled to a first-order

Example:

First integrator dissipates the most power and requires the most accuracy.

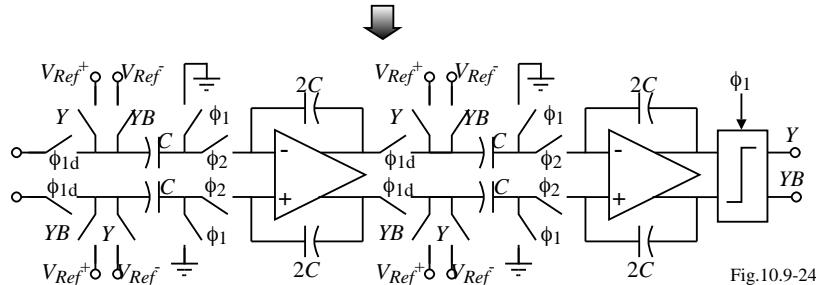
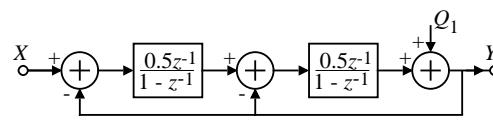


Fig.10.9-24

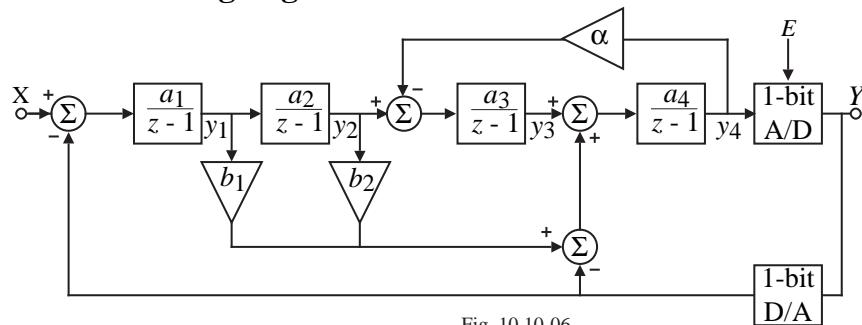
1.5V, 1mW, 98db ΔΣ Analog-Digital Converter[†]

Fig. 10.10-06

where $a_1 = 1/3$, $a_2 = 3/25$, $a_3 = 1/10$, $a_4 = 1/10$, $b_1 = 6/5$, $b_2 = 1$ and $\alpha = 1/6$

Advantages:

- The modulator combines the advantages of both DFB and DFF type modulators:
Only four op amps are required. The 1st integrator's output swing is between $\pm V_{REF}$ for large input signal amplitudes ($0.6V_{REF}$), even if the integrator gain is large (0.5).
- A local resonator is formed by the feedback around the last two integrators to further suppress the quantization noise.
- The modulator is fully pipelined for fast settling.

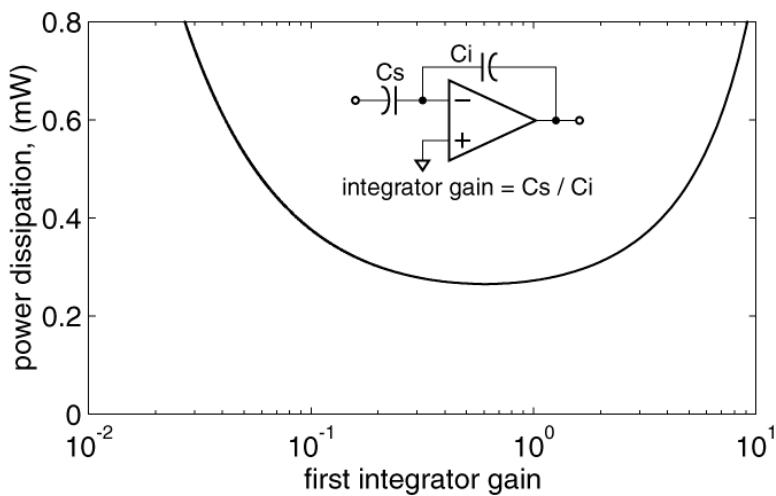
[†] A.L. Coban and P.E. Allen, "A 1.5V, 1mW Audio ΔΣ Modulator with 98dB Dynamic Range," Proc. of 1999 Int. Solid-State Circuits Conf., Feb. 1999, pp. 50-51.

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1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Integrator power dissipation vs. integrator gain



$$DR = 98 \text{ dB}$$

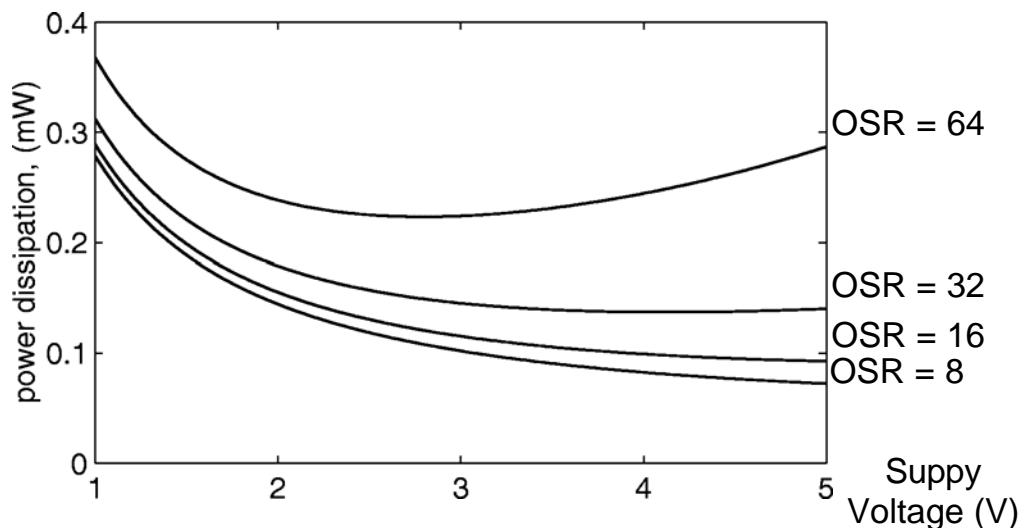
$$BW = 20 \text{ kHz}$$

$$C_S = 5 \text{ pF}$$

$$0.5 \mu\text{m CMOS}$$

1.5V, 1mW, 98db $\Delta\Sigma$ Analog-Digital Converter - Continued

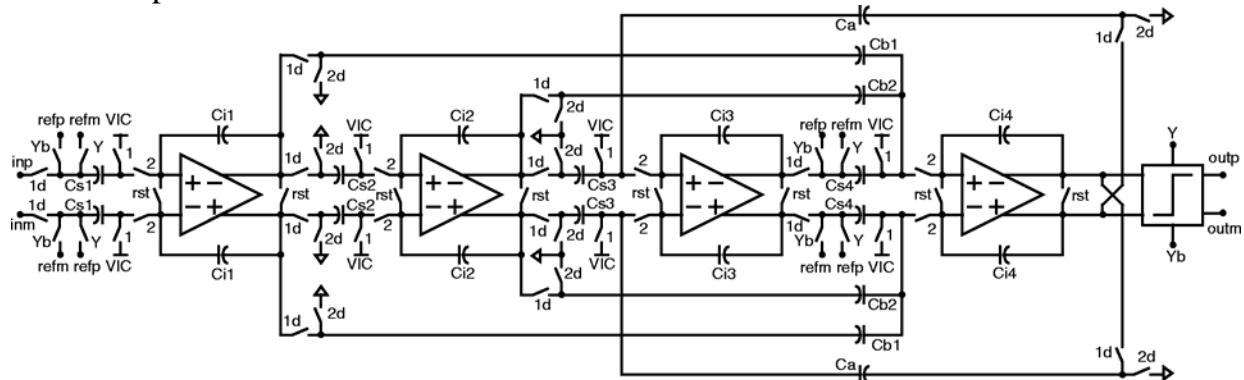
Modulator power dissipation vs. oversampling ratio



$DR = 98 \text{ dB}$
 $BW = 20 \text{ kHz}$
Integrator gain = 1/3
 $0.5\mu\text{m}$ CMOS

1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Circuit Implementation:



Capacitor Values				
Capacitor	Integrator 1	Integrator 2	Integrator 3	Integrator 4
C_s	5.00pF	0.15pF	0.30pF	0.10pF
C_i	15.00pF	1.25pF	3.00pF	1.00pF
C_a	-	-	0.05pF	-
C_{b1}	-	-	-	0.12pF
C_{b2}	-	-	-	0.10pF

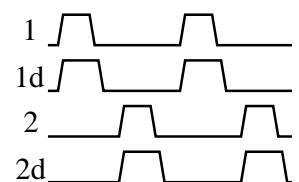
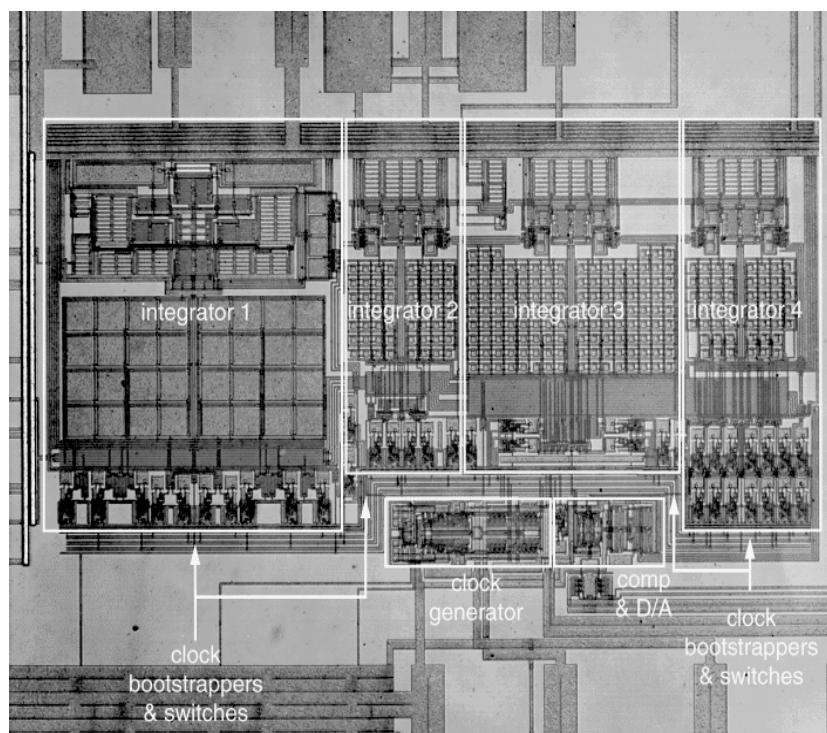


Fig. 10.9-25

1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Microphotograph of the $\Delta\Sigma$ modulator.

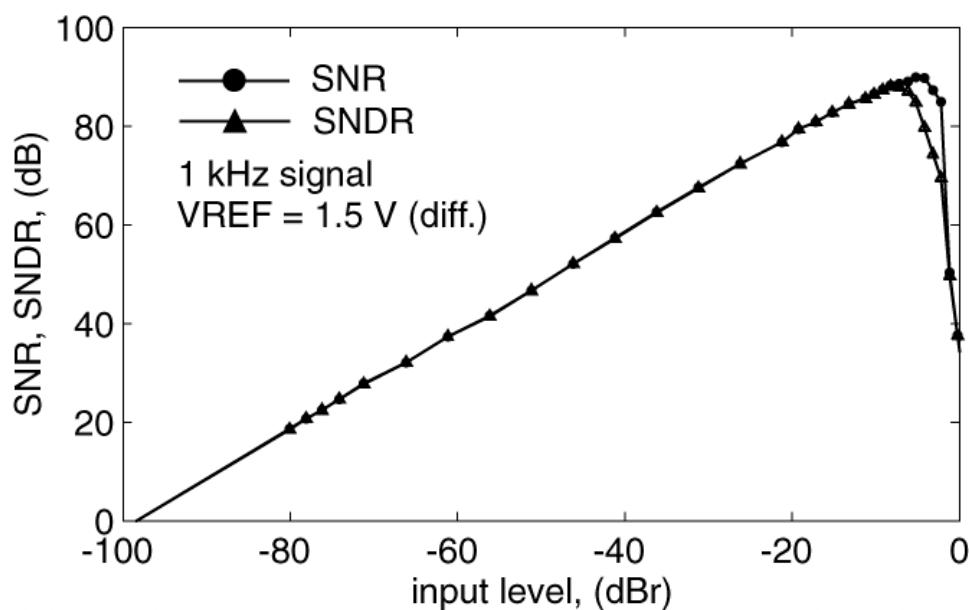


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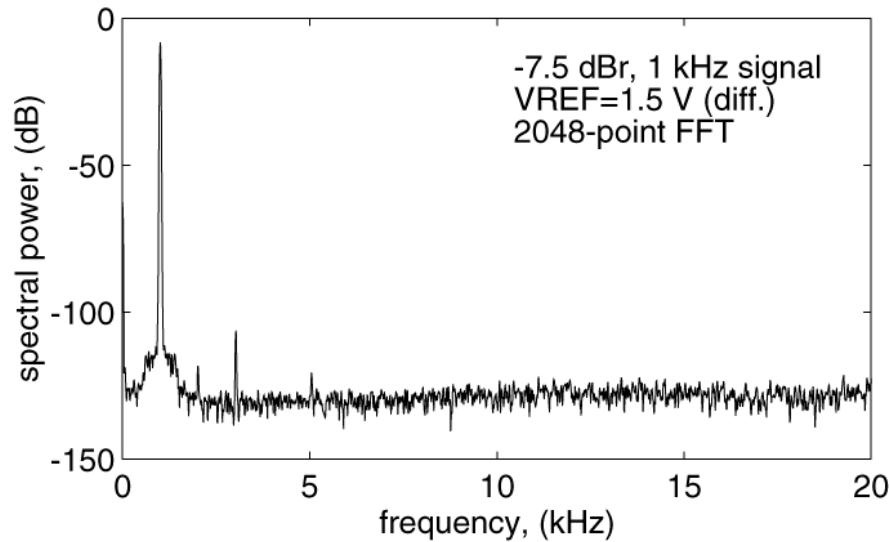
1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Measured SNR and SNDR versus input level of the modulator.



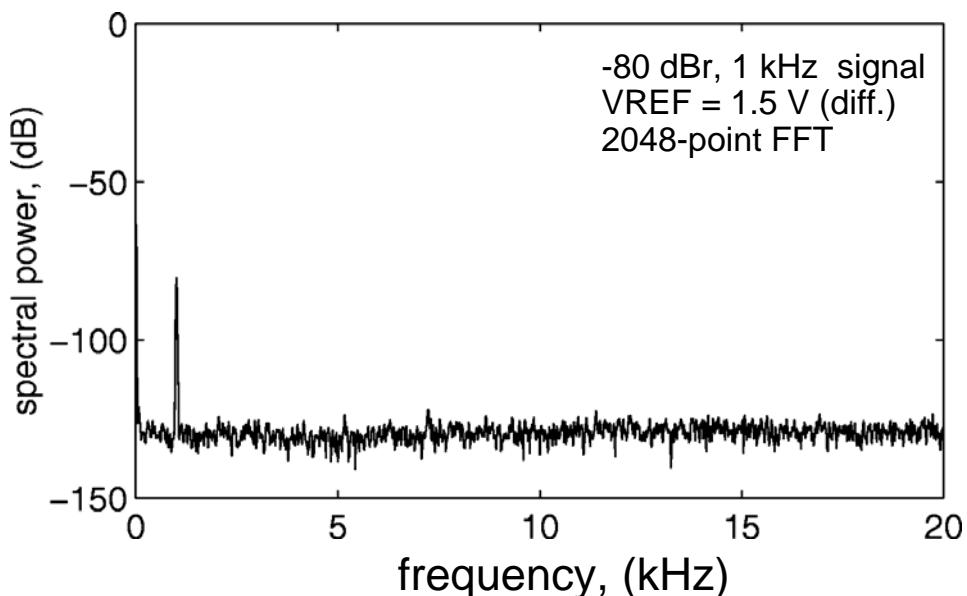
1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Measured baseband spectrum for a -7.5dBr 1kHz input.



1.5V, 1mW, 98dB $\Delta\Sigma$ Analog-Digital Converter - Continued

Measured baseband spectrum for a -80dBr 1kHz input.



1.5V, 1mW, 98dB ΔΣ Analog-Digital Converter - Continued

Measured 4th-Order ΔΣ Modulator Characteristics:

Table 5.4

Measured fourth-order delta-sigma modulator characteristics	
Technology : 0.5 μm triple-metal single-poly n-well CMOS process	
Supply voltage	1.5 V
Die area	1.02 mm x 0.52 mm
Supply current	660 μA
analog part	630 μA
digital part	30 μA
Reference voltage	0.75V
Clock frequency	2.8224MHz
Oversampling ratio	64
Signal bandwidth	20kHz
Peak SNR	89 dB
Peak SNDR	87 dB
Peak S/D	101dB
HD ₃ @ -5dBv 2kHz input	-105dBv
DR	98 dB

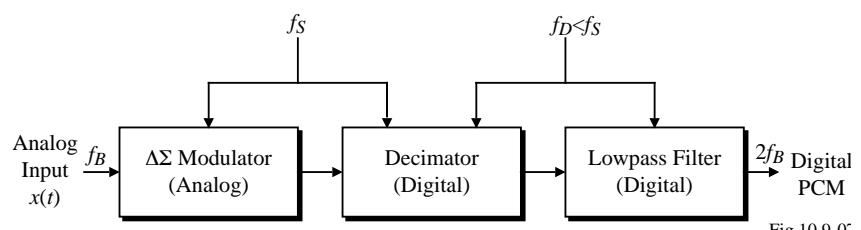
DECIMATION AND FILTERING

Delta-Sigma ADC Block Diagram

The decimator and filter are implemented digitally and consume most of the area and the power.

Function of the decimator and filter are;

- 1.) To attenuate the quantization noise above the baseband
- 2.) Bandlimit the input signal
- 3.) Suppress out-of-band spurious signals and circuit noise



Most of the ΔΣ ADC applications demand decimation filters with linear phase characteristics leading to the use of finite impulse response (FIR) filters.

FIR filters:

For a specified ripple and attenuation,

$$\text{Number of filter coefficients} \propto \frac{f_s}{f_t}$$

where f_s is the input rate to the filter (clock frequency of the quantizer) and f_t is the transition bandwidth.

A Multi-Stage Decimation Filter

To reduce the number of stages, the decimation filters are implemented in several stages. Typical multi-stage decimation filter:

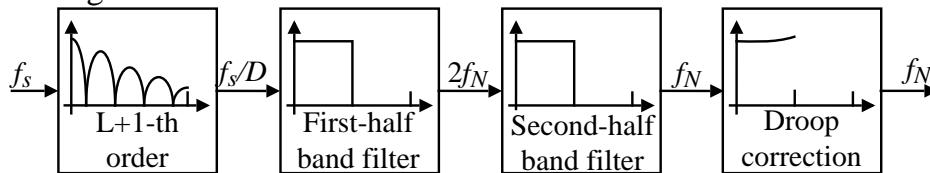


Fig.10.9-26

- 1.) For $\Delta\Sigma$ modulators with $(1-z^{-1})^L$ noise shaping comb filters are very efficient.
 - Comb filters are suitable for reducing the sampling rate to four times the Nyquist rate.
 - Designed to suppress the quantization noise that would otherwise alias into the signal band upon sampling at an intermediate rate of f_{s1} .
- 2.) The remaining filtering is performed by in stages by FIR or IIR filters.
 - Suppresses out-of-band components of the signal
- 3.) Droop correction - may be required depending upon the ADC specifications

Comb Filters

A comb filter that computes a running average of the last D input samples is given as

$$y[n] = \frac{1}{D} \sum_{i=0}^{D-1} x[n-i]$$

where D is the decimation factor given as

$$D = \frac{f_s}{f_{s1}}$$

The corresponding z -domain expression is,

$$H_D(z) = \sum_{i=1}^D z^{-i} = \frac{1}{D} \frac{1 - z^{-D}}{1 - z^{-1}}$$

The frequency response is obtained by evaluating $H_D(z)$ for $z = e^{j2\pi f T_s}$,

$$H_D(f) = \frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} e^{-j2\pi f T_s / D}$$

where T_s is the input sampling period ($=1/f_s$). Note that the phase response is linear.

For an L -th order modulator with a noise shaping function of $(1-z^{-1})^L$, the required number of comb filter stages is $L+1$. The magnitude of such a filter is,

$$|H_D(f)| = \left(\frac{1}{D} \frac{\sin \pi f D T_s}{\sin \pi f T_s} \right)^K$$

Magnitude Response of a Cascaded Comb Filter

$K = 1, 2$ and 3

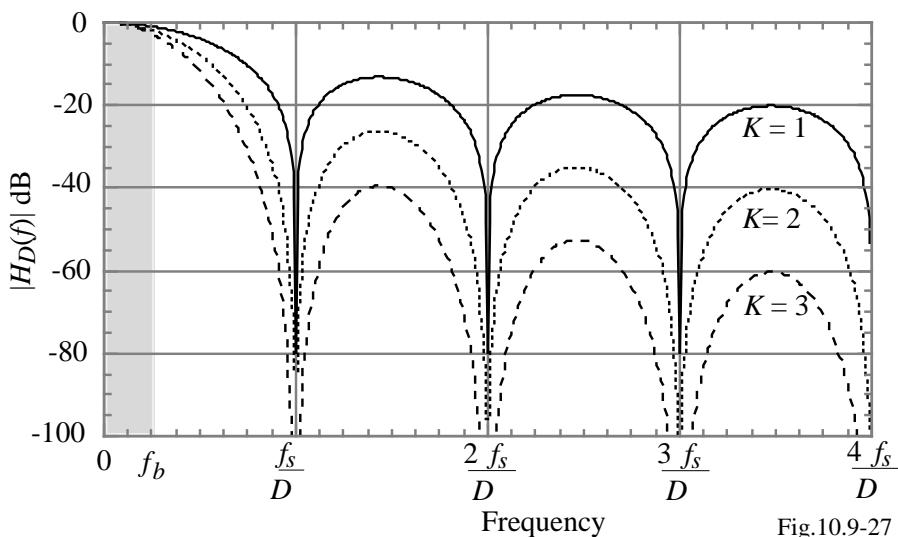


Fig.10.9-27

Implementation of a Cascaded Comb Filter

Implementation:

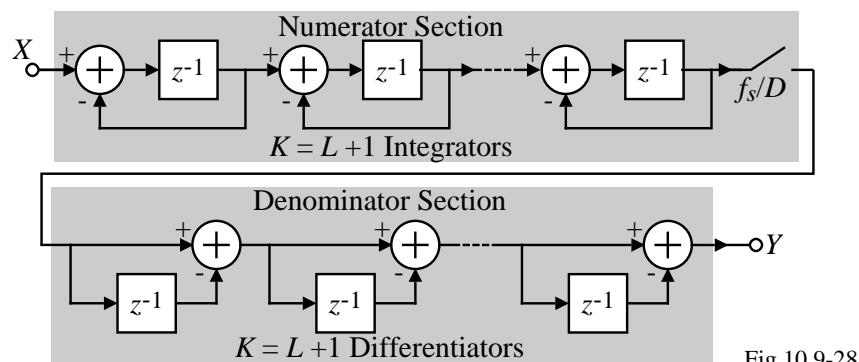


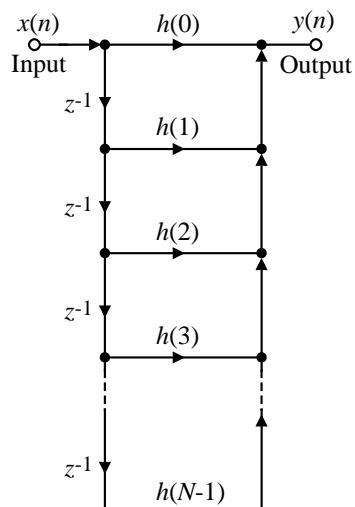
Fig.10.9-28

Comments:

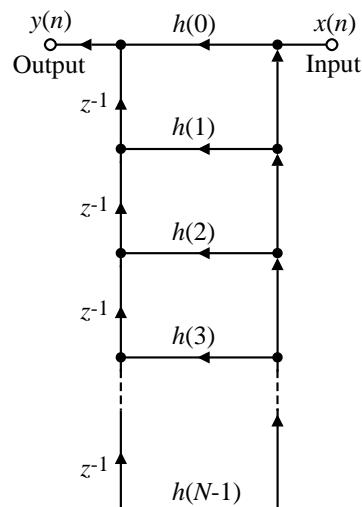
- 1.) The $L+1$ integrators operating at the sampling frequency, f_s , realize the denominator of $H_D(z)$.
- 2.) The $L+1$ differentiators operating at the output rate of f_{s1} ($-f_s/D$) realize the numerator of $H_D(z)$.
- 3.) Placing the integrator delays in the feedforward path reduces the critical path from $L+1$ adder delays to a single adder delay.

Implementation of Digital Filters[†]

Digital filter structures:



Direct-form structure
for an FIR digital filter.



Transposed direct-form
FIR filter structure.

Fig.10.9-29

[†] S.R. Norsworthy, R. Schreier, and G.C. Temes, *Delta-Sigma Data Converters-Theory, Design, and Simulation*, IEEE Press, NY, Chapter 13, 1997.
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Digital Lowpass Filter

Example of a typical digital filter used in removal of the quantization noise at higher frequencies

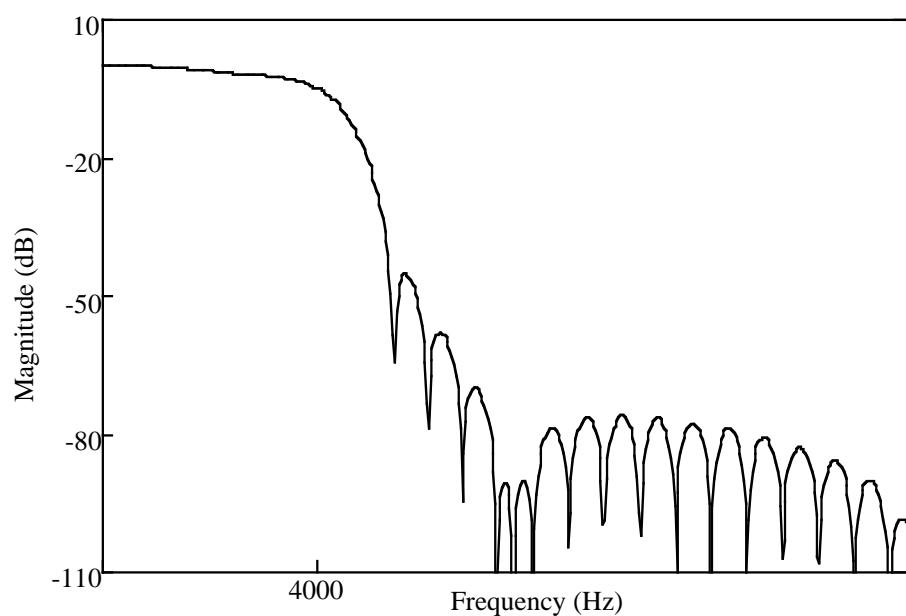
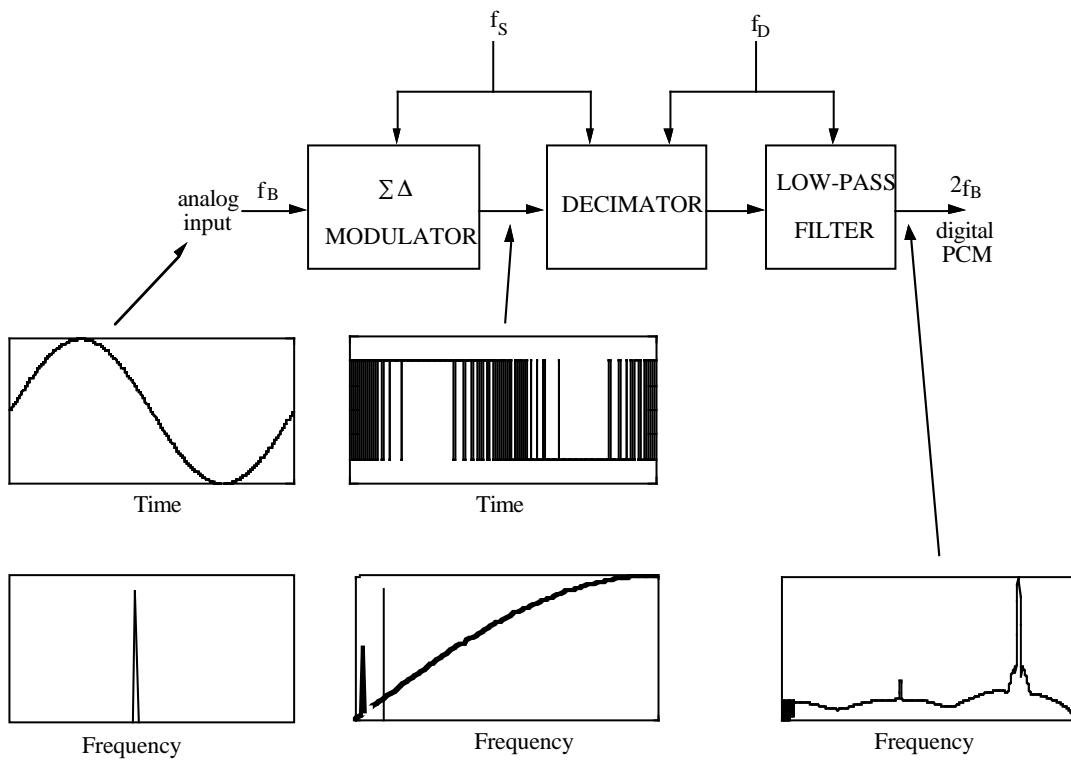


Illustration of the Delta-Sigma ADC in Time and Frequency Domain



BANDPASS DELTA-SIGMA MODULATORS

Bandpass $\Delta\Sigma$ Modulators

Block diagram of a bandpass modulator:

Components:

- Resonator - a bandpass filter of order $2N, N = 1, 2, \dots$
- Coarse quantizer (1 bit or multi-bit)

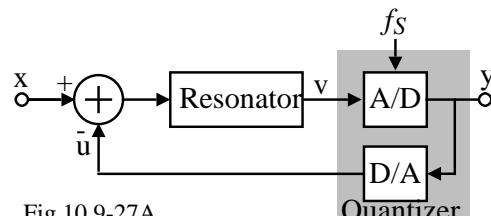


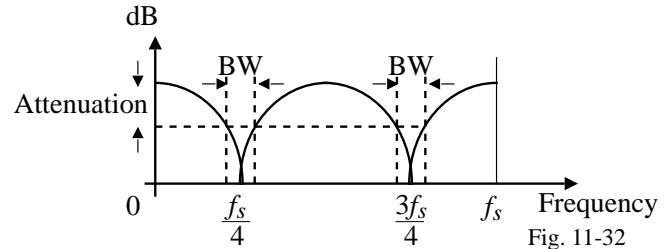
Fig.10.9-27A

The noise-shaping of the bandpass oversampled ADC has the following interesting characteristics:

$$\text{Center frequency} = f_s \cdot (2N-1)/4$$

$$\text{Bandwidth} = \text{BW} = f_s / M$$

Illustration of the Frequency Spectrum ($N=1$):



Application of the bandpass $\Delta\Sigma$ ADC is for systems with narrowband signals (IF frequencies)

A First-Order $\Delta\Sigma$ Bandpass Modulator

Bandpass Resonator:

$$V(z) = z^{-1} [X(z) - z^{-1}V(z)] = z^{-1}X(z) - z^{-2}V(z)$$

$$V(z)(1+z^{-2}) = z^{-1}X(z) \rightarrow \frac{V(z)}{X(z)} = \frac{z^{-1}}{1+z^{-2}}$$

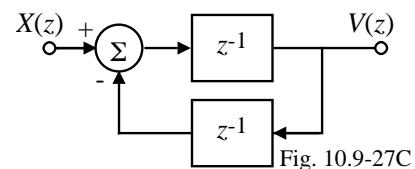


Fig. 10.9-27C

Modulator:

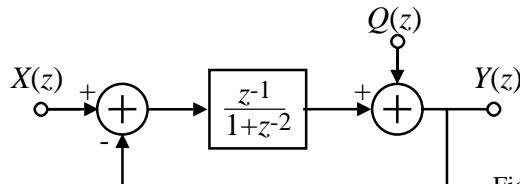


Fig. 10.9-27B

$$Y(z) = Q(z)$$

$$Y(z) = \left(\frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right) Q(z) + \left(\frac{z^{-1}}{1+z^{-1}-z^{-2}} \right) X(z)$$

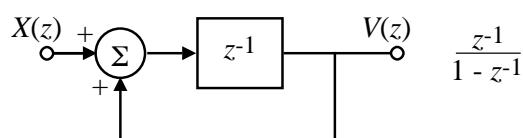
$$NTF_Q(z) = \left(\frac{1+z^{-2}}{1+z^{-1}-z^{-2}} \right)$$

$$+ [X(z) - Y(z)] \left(\frac{z^{-1}}{1+z^{-2}} \right) \rightarrow$$

The $NTF_Q(z)$ has two zeros on the $j\omega$ axis.

Resonator Design

Resonators can be designed by applying a lowpass to bandpass transform as follows:



Replace z^{-1} by $-z^{-2}$

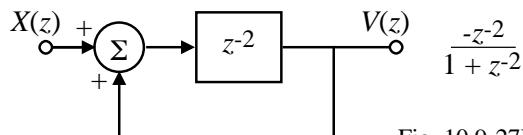


Fig. 10.9-27D

Result:

- Simple way to design the resonator
- Inherits the stability of a lowpass modulator
- Center frequency located at $f_s/4$

Fourth-Order Bandpass $\Delta\Sigma$ Modulator

Block diagram:

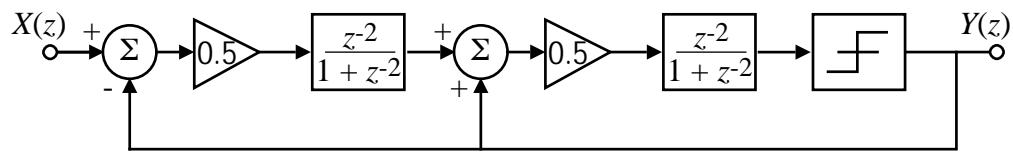


Fig. 10.9-27E

Comments:

- Designed by applying a lowpass to bandpass transform to a second-order lowpass $\Delta\Sigma$ modulator
- The stability and SNR characteristics are the same as those of a second-order lowpass modulator
- The z -domain output is given as,
$$Y(z) = z^{-4}X(z) + (1+z^{-2})^2Q(z)$$
- The zeros are located at $z = \pm j$ which corresponds to notches at $f_s/4$.

Resonator Circuit Implementation

Block diagram of $z^{-2}/(1+z^{-2})$:

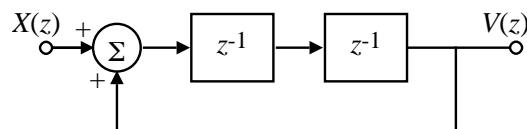


Fig. 10.9-27F

Fully differential switch-capacitor implementation:

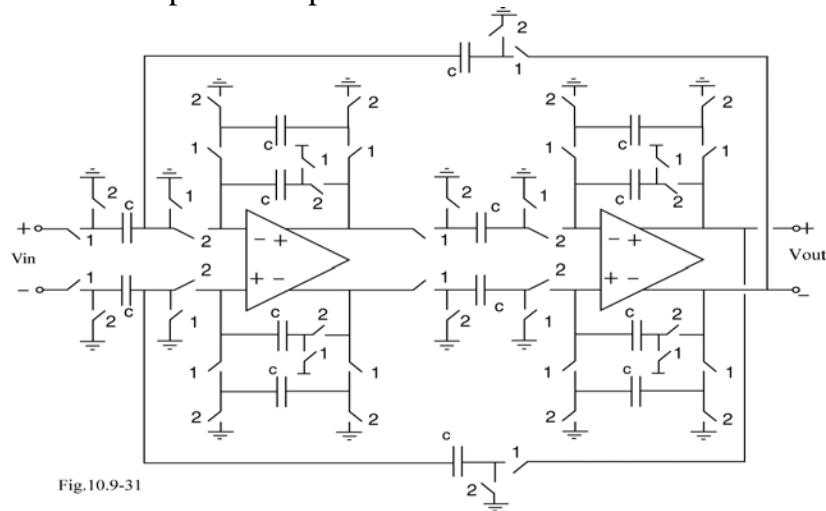
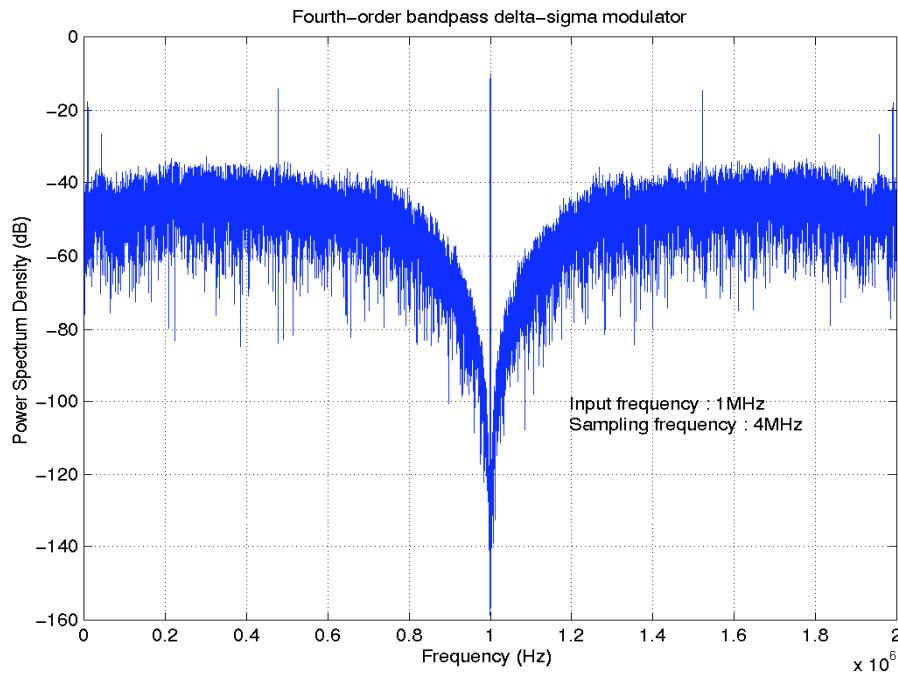


Fig. 10.9-31

Power Spectral Density of the Previous Fourth-Order Bandpass $\Delta\Sigma$ Modulator

Simulated result:



DELTA-SIGMA DIGITAL-TO-ANALOG CONVERTERS

Principles

The principles of oversampling and noise shaping are also widely used in the implementation of $\Delta\Sigma$ DACs.

Simplified block diagram of a delta-sigma DAC:

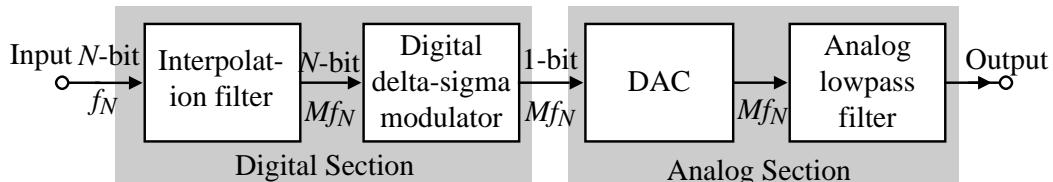
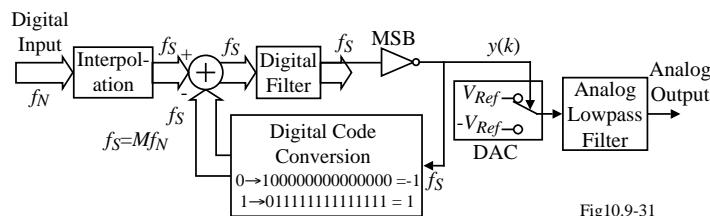


Fig 10.9-29

Operation:

- 1.) A digital signal with N -bits with a data rate of f_N is sampled at a higher rate of Mf_N by means of an interpolator.
- 2.) Interpolation is achieved by inserting “0”s between each input word with a rate of Mf_N and then filtering with a lowpass filter.
- 3.) The MSB of the digital filter is applied to a DAC which is applied to an analog lowpass filter to achieve the analog output.

Block Diagram of a $\Delta\Sigma$ DAC



Operation:

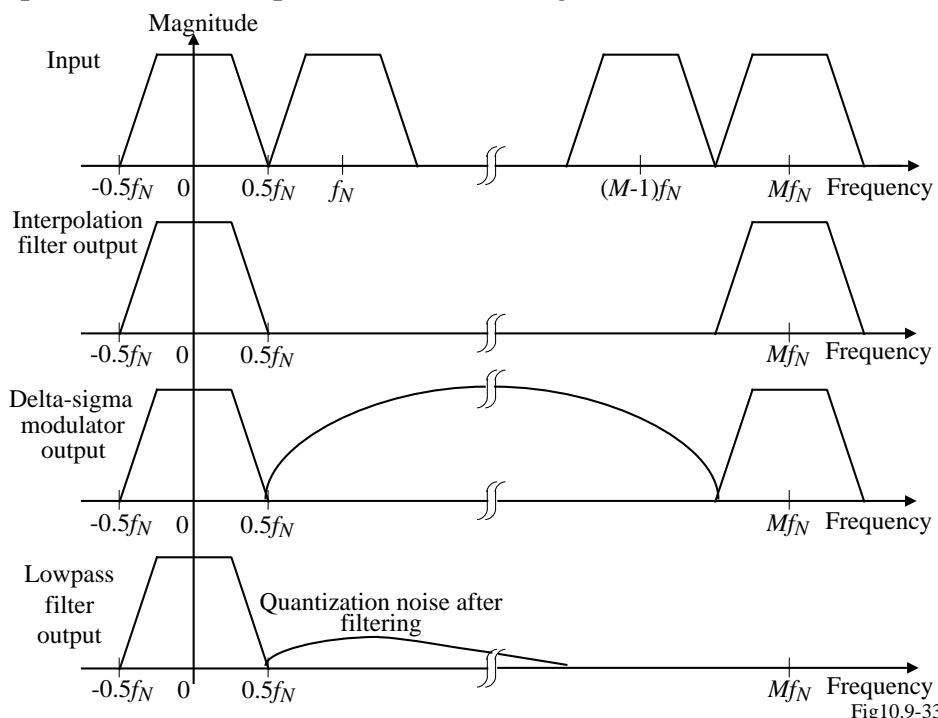
- 1.) Interpolate a digital word at the conversion rate of the converter (f_N) up to the sample frequency, f_s .
- 2.) The word length is then reduced to one bit with a digital sigma-delta modulator.
- 3.) The one bit PDM signal is converted to an analog signal by switching between two reference voltages.
- 4.) The high-frequency quantization noise is removed with an analog lowpass filter yielding the required analog output signal.

Sources of error:

- Device mismatch (causes harmonic distortion rather than DNL or INL)
- Component noise
- Device nonlinearities
- Clock jitter sensitivity
- Inband quantization error from the $\Delta\Sigma$ modulator

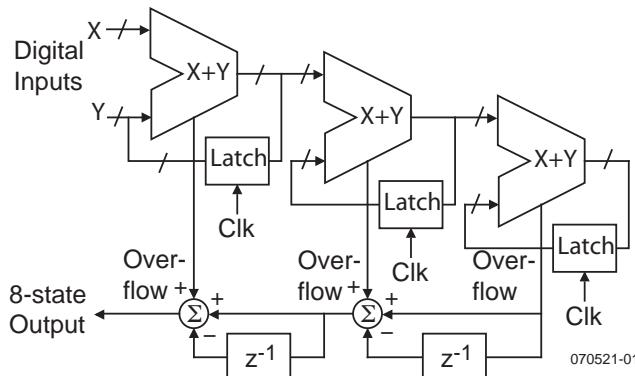
Frequency Viewpoint of the $\Delta\Sigma$ DAC

Frequency spectra at different points of the delta-sigma ADC:



A Third-Order, $\Delta\Sigma$ Modulator for a DAC

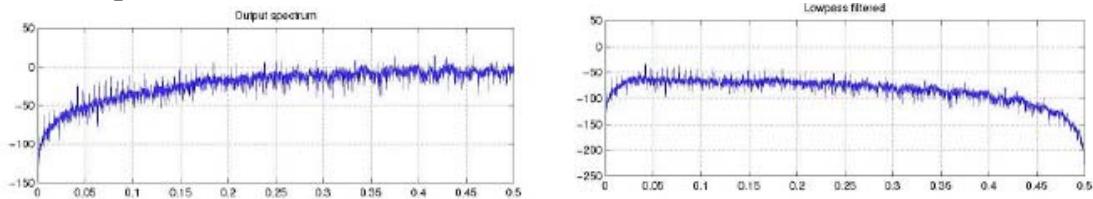
A digital equivalent of the third-order MASH $\Delta\Sigma$ modulator is shown below.



The m -bit accumulators consist of an m -bit adder and m -bit latches.

The 8-state digital output is converted to an analog through means of an analog filter.

Spectral outputs:



1-BitDAC for the $\Delta\Sigma$ Digital-to-Analog Converter - The Analog Part

The MSB output from the digital filter is used to drive a 1-bit DAC.

Possible architectures:

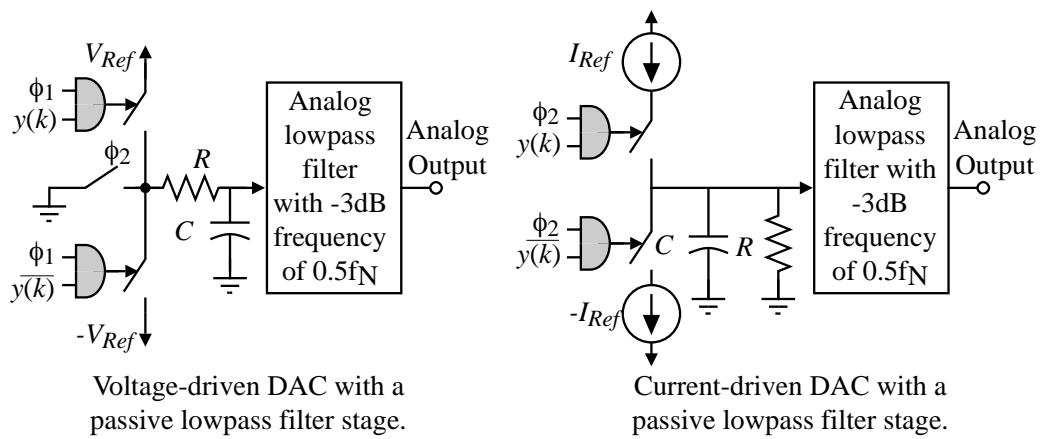


Fig10.9-32

A multi-bit output would consist of more parallel, controlled current sources and sinks.

Switched-Capacitor DAC and Filter

Typically, the DAC and the first stage of the lowpass filter are implemented using switched-capacitor techniques.

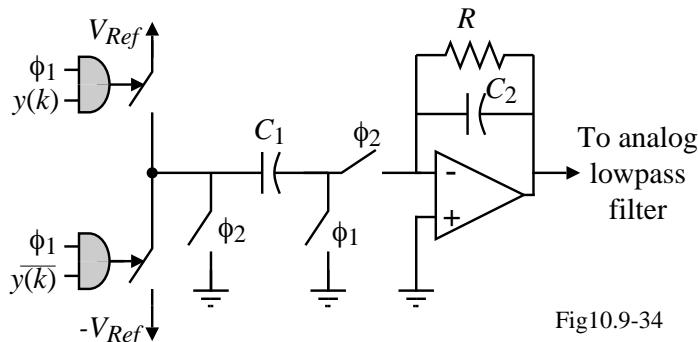


Fig10.9-34

It is necessary to follow the switched-capacitor filter by a continuous time lowpass filter to provide the necessary attenuation of the quantization noise.

SUMMARY

Comparison of the Various Types of ADCs

A/D Converter Type	Maximum Practical Number of Bits (± 1)	Speed (Expressed in terms of T a clock period)	Area Dependence on the number of bits, N , or other ADC parameters
Dual Slope	12-14 bits	$2(2NT)$	Independent
Successive Approximation with self-correction	12-15 bits	NT	$\propto N$
1-Bit Pipeline	10 bits	T (After NT delay)	$\propto N$
Algorithmic	12 bits	NT	Independent
Flash	6 bits	T	$\propto 2N$
Two-step, flash	10-12 bits	$2T$	$\propto 2N/2$
Multiple-bit, M-pipe	12-14 bits	MT	$\propto 2N/M$
$\Delta-\Sigma$ Oversampled (1-bit, L loops and M = oversampling ratio = $f_{clock}/2f_b$)	15-17 bits	MT	$\propto L$

Comparison of Recent ADCs

Resolution versus conversion rate:

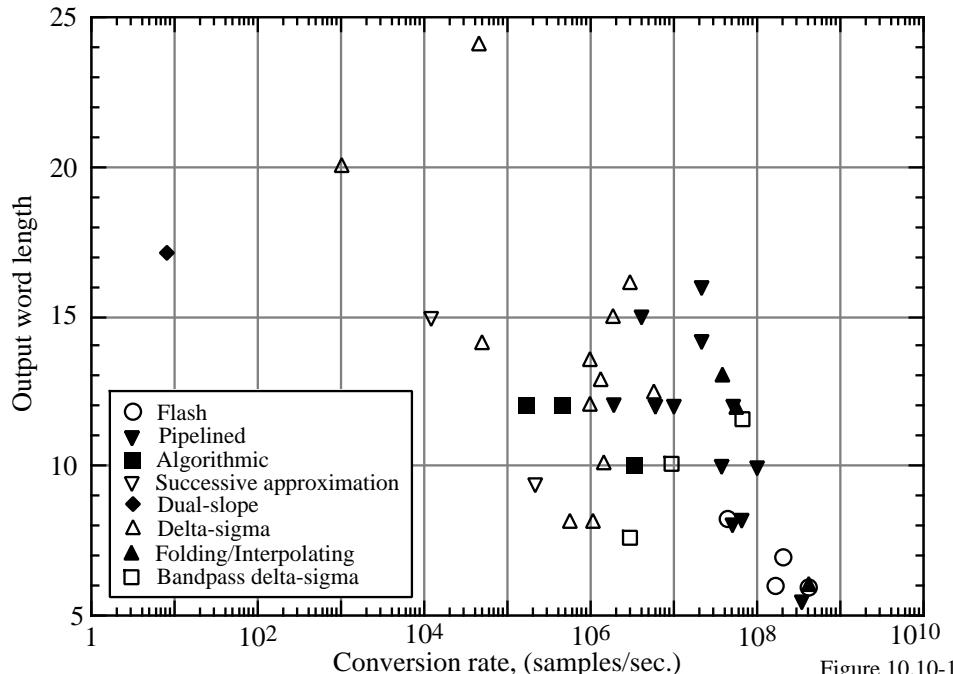


Figure 10.10-1

Comparison of Recent ADCs - Continued

Power dissipation versus conversion rate:

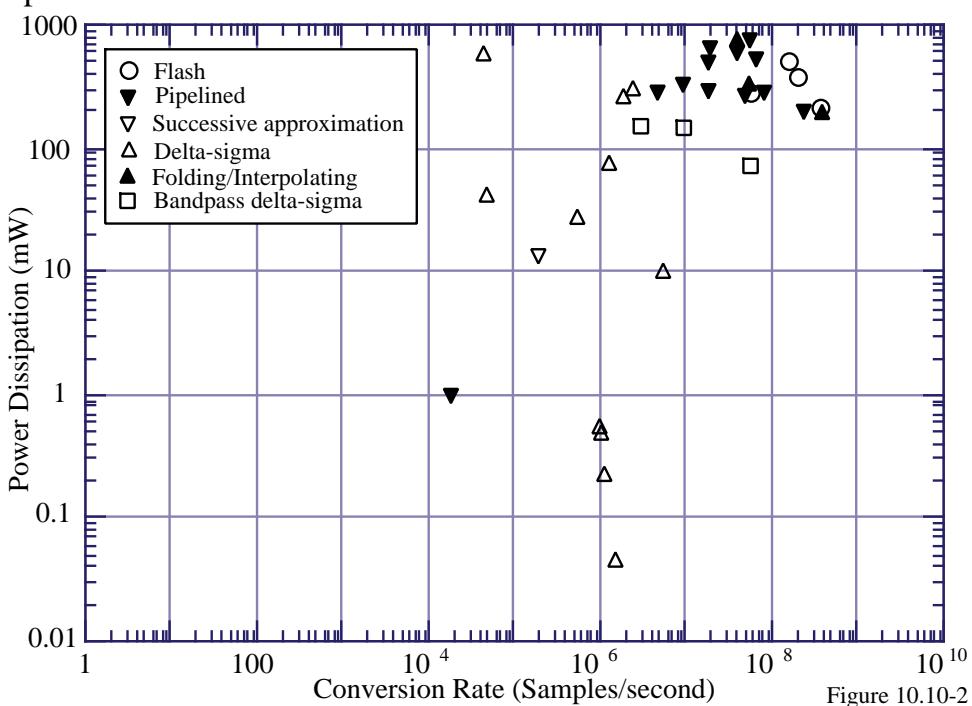


Figure 10.10-2

References for Previous Figures

- [1] A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC. *Vorenkamp, P.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1876-1886
- [2] A 15-b, 5-Msample/s Low-Spurious CMOS ADC. *Kwak, S. -U.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1866-1875
- [3] Error Suppressing Encode Logic of FCDL in a 6-b Flash A/D Converter. *Ono, K.*, IEEE J-SC, vol. 32, no. 9, Sep 97 1460-1464
- [4] A Cascaded Sigma-Delta Pipeline A/D Converter with 1.25 MHz Signal Bandwidth and 89 dB SNR. *Brooks, T. L.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1896-1906
- [5] A 10-b, 100 MS/s CMOS A/D Converter. *Kwang Young Kim*, IEEE J-SC, vol. 32, no. 3, Mar 97 302-311
- [6] A 1.95-V, 0.34-mW, 12-b Sigma-Delta Modulator Stabilized by Local Feedback Loops. *Au, S.*, IEEE J-SC, vol. 32, no. 3, Mar 97 321-328
- [7] A 250-mW, 8-b, 52Msamples/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers. *Nagaraj, K.*, IEEE J-SC, vol. 32, no. 3, Mar 97 312-320
- [8] A DSP-Based Hearing Instrument IC. *Neuteboom, H.*, IEEE J-SC, vol. 32, no. 11, Nov 97 1790-1806
- [9] An Embedded 240-mW 10-b 50MS/s CMOS ADC in 1-mm². *Bult, K.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1887-1895
- [10] Low-Voltage Double-Sampled ΣΔ Converters. *Senderowicz, D.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1907-1919
- [11] Quadrature Bandpass ΔΣ Modulation for Digital Radio. *Jantzi, S. A.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1935-1950
- [12] A Two-Path Bandpass ΣΔ Modulator for Digital IF Extraction at 20 MHz. *Ong, A. K.*, IEEE J-SC, vol. 32, no. 12, Dec 97 1920-1934
- [13] A 240-Mbps, 1-W CMOS EPRML Read-Channel LSI Chip Using an Interleaved Subranging Pipeline A/D Converter. *Matsuura, T.*, IEEE J-SC, vol. 33, no. 11, Nov 98 1840-1850
- [14] A 13-Bit, 1.4 MS/s Sigma-Delta Modulator for RF Baseband Channel Applications. *Feldman, A. R.*, IEEE J-SC, vol. 33, no. 10, Oct 98 1462-1469
- [15] Design and Implementation of an Untrimmed MOSFET-Only 10-Bit A/D Converter with -79-dB THD. *Hammerschmied, C. M.*, IEEE J-SC, vol. 33, no. 8, Aug 98 1148-1157
- [16] A 15-b Resolution 2-MHz Nyquist Rate ΔΣ ADC in a 1-μm CMOS Technology. *Marques, A. M.*, IEEE J-SC, vol. 33, no. 7, Jul 98 1065-1075
- [17] A 950-MHz IF Second-Order Integrated LC Bandpass Delta-Sigma Modulator. *Gao, W.*, IEEE J-SC, vol. 33, no. 5, May 98 723-732
- [18] A 200-MSPS 6-Bit Flash ADC in 0.6μm CMOS. *Dalton, D.*, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 45, no. 11, Nov 98 1433-1444

References - Continued

- [19] A 5-V Single-Chip Delta-Sigma Audio A/D Converter with 111 dB Dynamic Range. *Fujimori, I.*, IEEE J-SC, vol. 32, no. 3, Mar 97 329-336
- [20] A 256 x 256 CMOS Imaging Array with Wide Dynamic Range Pixels and Column-Parallel Digital Output. *Decker, S.*, IEEE J-SC, vol. 33, no. 12, Dec 98 2081-2091
- [21] A 400 Msample/s, 6-b CMOS Folding and Interpolating ADC. *Flynn, M.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1932-1938
- [22] An Analog Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters. *Dyer, K. C.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1912-1919
- [23] A CMOS 6-b, 400-Msample/s ADC with Error Correction. *Tsukamoto, S.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1939-1947
- [24] A Continuously Calibrated 12-b, 10-MS/s, 3.3-V ADC. *Ingino, J. M.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1920-1931
- [25] A Delta-Sigma PLL for 14b, 50 ksamples/s Frequency-to-Digital Conversion of a 10 MHz FM Signal. *Galton, I.*, IEEE J-SC, vol. 33, no. 12, Dec 98 2042-2053
- [26] A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters. *Fu, D.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1904-1911
- [27] An IEEE 1451 Standard Transducer Interface Chip with 12-b ADC, Two 12-b DAC's, 10-kB Flash EEPROM, and 8-b Microcontroller. *Cummins, T.*, IEEE J-SC, vol. 33, no. 12, Dec 98 2112-2120
- [28] A Single-Ended 12-bit 20 Msample/s Self-Calibrating Pipeline A/D Converter. *Opris, I. E.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1898-1903
- [29] A 900-mV Low-Power ΔΣ A/D Converter with 77-dB Dynamic Range. *Peluso, V.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1887-1897
- [30] Third-Order ΔΣ Modulator Using Second-Order Noise-Shaping Dynamic Element Matching. *Yasuda, A.*, IEEE J-SC, vol. 33, no. 12, Dec 98 1879-1886
- [31] R, G, B Acquisition Interface with Line-Locked Clock Generator for Flat Panel Display. *Marie, H.*, IEEE J-SC, vol. 33, no. 7, Jul 98 1009-1013
- [32] A 25 MS/s 8-b - 10 MS/s 10-b CMOS Data Acquisition IC for Digital Storage Oscilloscopes. *Kusayanagi, N.*, IEEE J-SC, vol. 33, no. 3, Mar 98 492-496
- [33] A Multimode Digital Detector Readout for Solid-State Medical Imaging Detectors. *Boles, C. D.*, IEEE J-SC, vol. 33, no. 5, May 98 733-742
- [34] CMOS Charge-Transfer Preamplifier for Offset-Fluctuation Cancellation in Low Power A/D Converters. *Kotani, K.*, IEEE J-SC, vol. 33, no. 5, May 98 762-769
- [35] Design Techniques for a Low-Power Low-Cost CMOS A/D Converter. *Chang, Dong-Young*, IEEE J-SC, vol. 33, no. 8, Aug 98 1244-1248

CONCLUDING THOUGHTS

- What is analog circuit design?

The complex process of creating circuit solutions using analog circuit techniques.

- What is the analog integrated circuit design process?

The even more complex process of combining analog design with IC technology which includes electrical, physical and test design.

- What are the key principles, concepts and techniques for analog IC design?

Key principles – Fundamental laws

Key concepts – Important relationships and ideas

Key techniques – Tools that allow simplification or insight

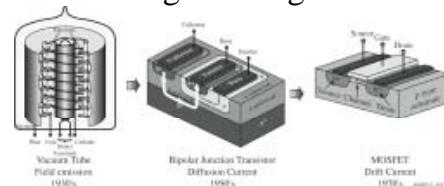
- How can the analog IC designer enhance creativity and solve new problems in today's industrial environment?

Learn the key principles, concepts and techniques of analog circuit design

Learn from mistakes

Learn the technology

Always try to understand the concept and operation of the circuit, never rely on a computer or someone else for this understanding



Technology changes but principles, concepts and techniques remain the same.

