Problem Set 1

Due: Thursday, January 31st, 2019 at 11:59pm

Notes: (1) Please submit your solution as a single PDF file at http://cms.csuglab.cornell.edu
(2) Please put your name and NetID on the top of the first page.

1. Consider an inverter with voltage transfer curve shown below.

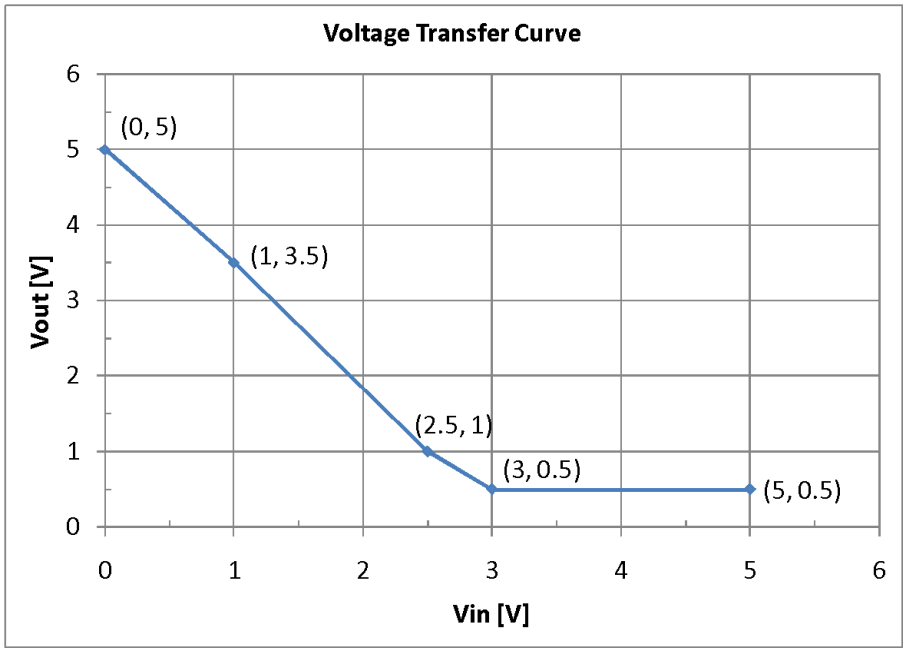

Figure 1: Voltage Transfer Curve

   a. What is the minimum value for V_{IH} given V_{OL} = 0.5 V? Remember that V_{IH} as an input must be able to produce V_{OL} or less as an output.
   b. Given V_{IH} and V_{OL} from part (a), find V_{OH} and V_{IL} that give the noise margin of 0.5V ($NM_H = NM_L$ = 0.5V).

$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

Such that

V_{IH} in generates V_{OL} or less out AND

V_{IL} in generates V_{OH} or more out.

2. Is it possible to assign logic levels so that a device with the voltage transfer characteristics shown in Figure 2 would serve as a reliable inverter with non-zero (positive) noise margins? If so, what are the input and output voltage levels $(V_{IL}, V_{OL}, V_{IH}, V_{OH})$ and noise margins (NM_L and NM_H)? If not, explain why not.

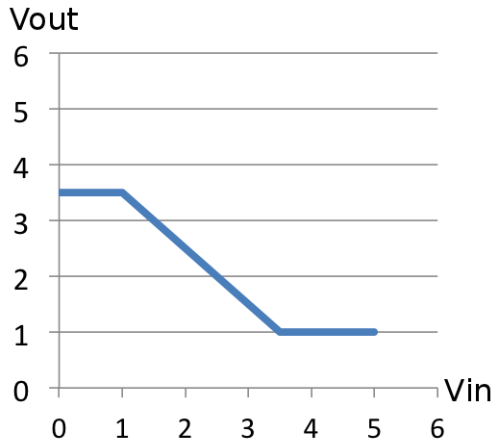

Figure 2: Voltage Transfer Curve

3. In class, it was mentioned that all combinational digital logic can be constructed using 2-input AND gates, 2-input OR gates, and inverters. It was also mentioned that, in fact, the NAND gate alone is sufficient. Given that AND gates, OR gates, and inverters can implement any logic, show that NAND gates can implement any logic function.

4. Design a CMOS circuit that has the functional behavior $\overline{A \cdot (B + C) \cdot D}$. (*Hint: Only 8 transistors are needed.*)