Asynchronous FIFO - [D:/Vivado/fifo/Asynchronous FIFO/Asynchronous FIFO.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Run Linter
- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
- Run Implementation
- Open Implemented Design

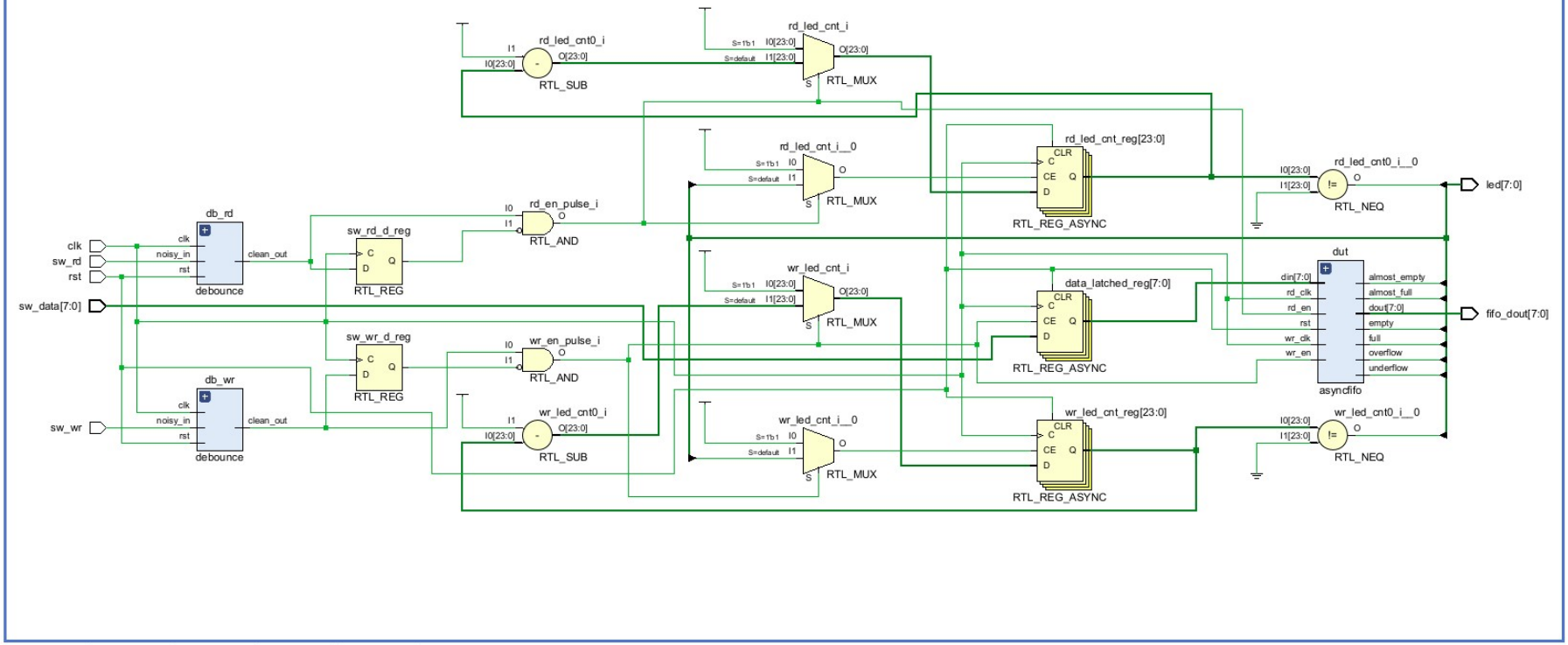
PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager

ELABORATED DESIGN - xc7z020clg484-1

Sources Netlist Properties

Schematic

71 Cells 28 I/O Ports 190 Nets



Tcl Console Messages Log Reports Design Runs