IITK-Mini-MIPS Processor_Dhriti (230364)_Durbasmriti (230393)

1. PDS1

General Purpose Registers (32 registers, 32-bit each)

- $zero (R0): Always contains 0
- $at (R1): Reserved for assembler
- $v0-$v1 (R2-R3): Function return values
- $a0-$a3 (R4-R7): Function arguments
- $t0-$t7 (R8-R15): Temporary registers
- $s0-$s7 (R16-R23): Saved registers
- $t8-$t9 (R24-R25): More temporary registers
- $k0-$k1 (R26-R27): Reserved for OS kernel
- $gp (R28): Global pointer
- $sp (R29): Stack pointer
- $fp (R30): Frame pointer
- $ra (R31): Return address

Floating Point Registers (32 registers, 32-bit each)

- $f0-$f31: Single-precision floating point registers

A 32bit Program counter (PC) was also implemented.

2. PDS2

The instruction size is 1 word = 4 bytes = 32 bits. Every instruction address is a multiple of 4.
The data memory has 256 words capable of storing 256, 32-bit values. The size is 256 x 32.

3. PDS3

R-Type Instructions (Register)

| 6-bit opcode | 5-bit rs | 5-bit rt | 5-bit rd | 5-bit shamt | 6-bit funct
Source registers - rs, rt.
Destination register - rd
Shift amount - shamt, required in sll, srl etc. instructions
Function code :- funct, used to identify the instruction.

I-Type Instructions (Immediate)

| 6-bit opcode | 5-bit rs | 5-bit rt | 16-bit immediate
Source register - rs
Destination register - rt
Constant/Offset - immediate, used to specify exact address.

J-Type Instructions (Jump)

| 6-bit opcode | 26-bit target address

47 functions were encoded in the above format similar to the way taught in the class notes.

NOTE: All further PDS and code for the same are attached.
Verilog codes are attached for Top Module (control unit), ALU, FPU, Branch Unit, Instruction Fetch, Instruction Decode, Register File, Data Memory and test bench. Machine code in binary for insertion sort is also attached.