Kaypro Emergency Monitor ROM
June 2, 2023

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Introduction

The purpose of the monitor is to help debugging a broken Kaypro. Replace the normal boot/BIOS ROM with an EPROM created from this monitor image. The Kaypro will now interact using the serial port (“Serial I/O” on early models, “Serial Data” on later models). No other hardware will be initialized, which means the display and keyboard will not work, nor will the disk. The display will usually be filled with random characters, or at least will not be cleared.

There is also a emergency memory test ROM available, for cases when the monitor ROM won’t even work.

The ROM Image

The monitor binary image may be downloaded here: http://sebhc.durgadas.com/kaypro/monitor.bin. Note that this is a 4K image and will only work in models capable of taking a 2732 (or larger) ROM. There is a 2K ROM image with reduced functionality (Kaypro-II features only), mon2k.bin, which maybe used in a 2716 EPROM. An image may also be put in larger EPROMs (2732 or 2764) for use with models that support larger ROMs. When using larger EPROMs, it should not be necessary to replicate the image throughout the extra space (but see “**Adapting 8K ROMs**” below). Note that the Kaypro IV/83 model (may also apply to some later Kaypro II) has a jumper-selectable ROM socket that takes either 2716 or 2732. Be certain to set the jumpers appropriate for whatever EPROM is being installed. The Kaypro 10/83 has a socket wired exclusively for the 2732. The */84 models should work with either 2732 or 2764 without changing any configuration.

Note that the AT28C16 EEPROM (FLASH) should work in place of the 2716 in Kaypro circuits. The AT28C64 should work in place of the 2764.

Using The Monitor

The monitor ROM does not depend on any hardware besides the SIO1 channel A serial port (and associated baud generator). However, it does provide a “heartbeat” indicator on the drive select LEDs on */84 (and 10) models – provided that the sysport is operating correctly. On */83 models, this heartbeat will be in the form of the first character on the display alternating between ‘A’ and ‘B’ – provided that the video is working. The heartbeat ceases after the first command is entered.

The monitor prompt is the colon character (‘:’). When the system is RESET the monitor will initialize the serial port and print a signon string and then prompt for input. Input lines may be edited using the Backspace key. Ctrl-C will abort the input and go back to the prompt. Upon pressing RETURN, the input line is then parsed by the monitor. Pressing RETURN at the prompt (empty input line) will just re-prompt.

Note that the ROM must be enabled by the sysport in order to operate. Low memory addresses contain the ROM contents and are not writeable. The exact boundary between ROM and RAM depends on the model. Also, the Kaypro II and IV models map the video RAM into addresses 3000-3BFF. In order to access the RAM at low addresses, a special program must be created to transfer control into high memory and update the sysport to turn off ROM (and video RAM). On */83 models, the sysport is implemented in a Z80-PIO which must be initialized before it can be used.

The command ‘?’ will print a brief list of commands with some help text.

The following commands are implemented:

D *start end*

Dump memory in hex. Both *start* and *end* are required, and are interpreted as hexadecimal. Up to 16 bytes are displayed per line, with ASCII representation following the hexadecimal byte values.

S *start*

Substitute memory content interactively. The current address (initially *start*) and byte are displayed in hex and input is accepted. Pressing RETURN will go to the next address (+1) without changing the current byte. Pressing dash (‘-’) will go to the previous (-1) address without changing the current byte. Pressing period (‘.’) will end the command and return to the monitor prompt. Entering hex digits and RETURN will replace the current byte with the new value and advance to the next address (+1).

G *start*

Go (jump) to *start* and begin executing the code there, after prompting for confirmation. If the code executes any RST instruction, control will be returned to the monitor, where the message “*** RST” and the calling address (after the RST instruction) will be printed. No registers are saved and the code may not be resumed.

F *start end data*

Fill memory with the byte *data* repeated throughout the range.

M *start end dest*

Move a block of memory. If *start end* overlaps with *dest* then the results are undefined.

I *port* **[** *num* **]**

Input from *port* and display the value in hex. If *num* is given, then the same port is read that number of times, and each value displayed. Both *port* and *num* are hexadecimal. There is no delay between inputs, other than the time it takes to print the value in hex.

O *port data* **[** *...* **]**

Output *data* to *port*. If more than one data bytes are given, then those values are successively output to *port*. There is no delay between outputs, other than the time it takes to parse the next value.

N *hw*

iNitialize a hardware component. *hw* may be:

KB83 – Initialize the keyboard SIO channel on a */83 model.

KB84 – Initialize the keyboard SIO channel on a */84 or 10 model.

CRTC – Initialize the CRT controller chip on a */84 or 10 model.

HDD – Initialize (perform RESET of) the HDD controller on Kaypro-10 models.

T *hw*

Test a hardware component. *hw* may be:

KBD – Run a simple test for receiving codes from the keyboard. Waits for keys to be pressed on the keyboard and prints the hexadecimal code that is received. To end the test, type any character on the monitor console.

CRTC – Run a simple test for CRTC update status. Tries to detect the status change three times, and prints “Update” for each. The test may be aborted, if hung, by typing any character on the monitor console.

VRT – Run a simple test for CRT vertical retrace activity. Gathers up to 10 transitions of the VRT bit in the status register, then displays results. Output is similar to that for FLPY, but the 6845 status register is being watched instead. Normal VRT rate seems to be about every 20 milliseconds (50Hz).

CRTR – Run a pass/fail integrity test for CRTC register access. Since the only CRTC registers that can be both read and written are the cursor position hi/low registers, this test runs through all possible values 0000-3FFF and checks that the written value can be read back. If fail, prints the expected and actual values for the cursor position of the first failure (test stops).

HDD – Run a test of the HDD system. Issues a command (default Self Test) to the WD1002 and captures the changes in the status register, similar to **FLPY**.

HDRD – Read the WD1002 data buffer into 8000H. If DRQ is not active, reads nothing. Prints final address (last byte + 1). Typically used after “T HDD 20”, with setup of other registers as needed.

FDRD – Do a floppy disk read of one sector into 8000h. User must first turn on motor, select a drive, select DD, select a side, and must have a formatted floppy diskette in the drive. See **Testing FDC** below.

FLPY – Run a test of the FDC system. User must first turn on motor and select a drive, and may need to have a floppy diskette in the drive. See **Testing FDC** below.

V

Display the ROM version. This just prints the ROM signon message again, which contains the version.

Several of the test and initialization commands will watch for changes on their respective “status” registers and display the results as a list of new register values and iteration counter at the time of the change. Each entry is printed in the form “SS NNNN” where “SS” is the register value in hexadecimal and “NNNN” is the iteration counter, also in hexadecimal. The iteration count values are in units of 12uS, i.e. one count represents 12uS on the 4MHz Kaypros (*/84, 10). On the */83 Kaypros (2.5MHz), this changes to 19.2uS. These tests only run until the iteration count wraps (reaches FFFF). When this limit is reached, a sample is always stored regardless of whether the register value changed. The commands using this method are: “T FLPY”, “T HDD”, “T VRT”, and “N HDD”.

Testing The FDC

The floppy disk system may be tested in the following way. The FLPY test command will output a command to the WD1793 and then read the status register for a period of time, tracking any change to the status bits. On each change, the new status register value and iteration count are stored. At the end of the test, the stored changes are printed. The test will end when the iteration counter rolls over (FFFF to 0000) or when the number of changes exceeds the limit (default 256), therefor this command should never hang. Optional parameters may be specified to give the WD1793 command to issue (default D0 – Force Interrupt), and the change count limit. Both are entered in hexadecimal. If the count limit is to be entered, the command must also be entered.

The user must select a drive, and typically turn on the motors. Depending on the desired test (command), it may also be necessary to have a floppy disk in the driver, and that disk may need to be formatted. This is entirely dependent on the desired test. The user is also responsible for turning off motors and deselecting the drive. Note that the Kaypro 10 uses the drive B select signal as the harddrive controller RESET.

The floppy control bits vary with the Kaypro model, and possibly even drive model (quad-density drives especially). Also note that the */83 models use a different system port (Z80-PIO) than the others. See also “Using SysPort on */83 Models” below. Here are the relevant bits (expressed as hexadecimal mask) for the major families:

*/83 (PIO 1CH)	Drive A select	01	0=select
	Drive B select	02	0=select
	Side select	04	0=side-1
	DD enable	20	0=DD
	Motor control	40	0=ON
Kaypro 10 (port 14H)	Drive A select	01	0=select
	WD1002 reset	02	1=reset
	Side select	04	0=side-1
	Motor control	10	1=ON
	DD enable	20	0=DD

*/84 (port 14H)	Drive A select	01	0=select
	Drive B select	02	0=select
	Side select	04	0=side-1
	Motor control	10	1=ON
	DD enable	20	0=DD

Note that the motor control bit is the major difference, with not only the bit location but also the polarity of the bit needed for “Motor ON” changing.

The general practice with SysPort is to read the current value, modify it, then write the new value. In this environment, there should be no hidden changes to the port and so it is reasonable to just know what the right value is without reading the port.

On a 4MHz Z80 Kaypro, each iteration count represents about 12 microseconds. On a 2.5MHz Z80 Kaypro, one iteration is about 19.2 microseconds.

The full syntax of the floppy test command is:

T FLPY [*cmd* [*limit*]]

Where *cmd* defaults to D0 (Force Interrupt) and *limit* defaults to 00 which means 256. See documentation for the WD1793 for available commands, their dependencies, and their side effects. Remember that STEP, SEEK, and RESTORE commands will require valid step rate bits for the drives being used – although it appears that Keypro software normally uses the fastest step rate (00). Also remember that commands which result in DRQ will not work correctly here.

T FDRD [*sector*]

Where *sector* defaults to 0 (Kaypro formatting numbers sectors 0-9 on side 0, and 10-19 on side 1). Note that *sector* must be entered in hexadecimal. This command prints the contents of the status register when finished.

Kaypro floppies reserve one track for the boot area, with that extended to include one block after the directory. The CP/M directory is on logical track 1, which on double-sided floppies is track 0 side 1 (sectors 10-13). The data blocks begin on logical track 1 with last two sectors (½ block). Note that sectors are formatted with a skew factor, so sectors are accessed by CP/M in order (0,1,2,...).

Testing The HDD

Similar to the FDC tests, the output is a list of changes observed in the status register, along with the time reference (iterations) where change occurred. This is followed by the (final) contents of the error register. The initialization command (“N HDD”) performs the RESET function and then captures status register changes. The test command (“T HDD [*cmd* [*limit*]]” issues the command (default is Self Test) and captures status register changes.

Note that this interface to the HDD does not differentiate between the A: and B: logical drives, it accesses the disk as one large image. Depending on the ROM version used to setup the system, the locations of the directories change. The primary boot sector is always at head 0, cylinder 0, sector 0.

The standard SDH (register/port 86H) value used by Kaypro is 101001hhhB, where “hhh” are the head select bits (e.g. A8H for head 0). The disk on Kaypro is always unit 1 (not 0).

The harddisk used by Kaypro has 306 cylinders, 4 heads, and 17 sectors per track, 512B sectors. Cylinder 305 is not used for data, as that is where the heads are parked when shutting down the system. Logical drive A: uses heads 0 and 1, logical drive B: uses heads 2 and 3. The logical order of tracks on drive A: is C0H0, C0H1, C1H0, … and similarly for B:. The boot image is contained in C0H0.

With the 81-302 ROM, the CP/M directory for drive A: is in C2H0, C3H1, C4H0, C5H1 with the interleaving tracks serving as a mirror image of the directory (for possible recovery purposes). Similarly, drive B: directory is C2H2, C3H3, C4H2, C5H3. The data blocks of drive A: start at C6H0 and B: at C6H2. There is no mirroring of data blocks. The boot area is mirrored to C0H1.

With the 81-478 ROM, the CP/M directory for A: is in C7H0, C7H1, C8H0, C8H1 and for B: is in C7H2, C7H3, C8H2, C8H3. The directories (and boot area?) are not mirrored. There are spare tracks reserved between the boot area and the directories. The spares table (C0H0S16) also contains partitioning information.

Examples

In the examples, characters typed by the user are underlined. *(CR)* means pressing the RETURN key.

Getting Help

This shows the signon message and how to display the help menu.

```
Kaypro Monitor v2.2

: ?(CR)
D <start> <end> - display memory in HEX
S <start> - set/view memory
    (CR) = skip fwd, '-' = skip bkwd, '.' = done
G <start> - go to address
F <start> <end> <data> - fill memory
M <start> <end> <dest> - Move data
I <port> [num] - Input from port
O <port> <value> [...] - Output to port
N <hw> - iNitialize hardware (KB83, KB84, CRTC, HDD)
T <hw> - Test hardware
  (KBD, CRTC, VRT, CRTR, HDD, HDRD, FDRD, FLPY)
V - Show ROM version
^C aborts command entry
:
```

Executing Code and Breakpoints

Set a RST 7 instruction into memory and jump to it.

```
: S8000(CR)
8000 00 FF
```

```
8001 00 .
: D8000 800F(CR)
8000 FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
: G8000(CR)
GO 8000 ?Y
*** RST 8001

:
```

*Using SysPort on */83 Models*

Initializes the PIO channel A for use as the sysport, then alternately selects drive B and drive A.

```
: O 1C 81(CR)       (make certain BANK stays on)

: O 1D CF 08(CR)    (init and activate PIO ch A)

: O 1C 82(CR)       (turn on drive B LED)

: O 1C 81(CR)       (turn on drive A LED)

: O 1C 80(CR)       (turn off both LEDs)
```

CRTC 6545 Testing

The CRT Controller chip, 6545 or sometimes 6845E, exists only on models */84 and 10. It powers-on and RESETs to a state where the video is disabled. The following commands may be used to initialize the core video functionality, and test for the “update” status (which is used to read/write the video RAM). The first command initializes the CRTC and enables video. After this command, the display should light up and be filled with random/garbage characters (whatever is in the video RAM after power-up). The second command runs a quick test to see if the video update status bit is working. In the case that it is not working, the command will hang. Pressing any key should abort and get back to the monitor prompt.

```
: N CRTC(CR)        (display should light up)
: T CRTC(CR)
Wait... Update Update Update
:
```

An additional test is to check that vertical retrace is happening, and at about 50Hz. With the CRT initialized:

```
: T VRT(CR)
80 001C
A0 064B
80 06AF
A0 0CDE
80 0D42
A0 1371
80 13D5
A0 1A03
80 1A68
A0 2096
```

```
:
```

The VRT bit mask is 20 (hex), and we see that we get a pulse about every 0693H iterations (1683 decimal). At 12 uS per iteration, this computes to approximately 20 mS which is 50Hz.

Keyboard Testing

The keyboard uses SIO channel B on the same Z80-SIO chip as this monitor port is using, so that part is likely to also work. However, the keyboard itself may be tested by initializing the SIO port and running a test that will show the received codes for keys pressed on the keyboard. The keyboard initialization is slightly different for */83 models, so use the appropriate command syntax for the Kaypro model being tested. The Kaypro keyboard contains the "beep" functionality, which is activated by sending a Ctrl-D character out to the keyboard. This can be tested using the Output command as shown in the example.

```
: N KB84(CR)        (initialize keyboard port on */84 and 10 models)
: T KBD(CR)         (start keyboard test, press keys on keyboard)
Wait... 61 73 64 66 77 65 65 72 F3 F4 (CR)Abort
: O 05 04(CR)
                    (keyboard beeps)
:
```

Floppy Testing (Index hole)

Here is a simple operational test for the floppy subsystem. This examples first selects drive A and turns on the motor (also, the user is expected to insert a floppy disk). Then the test is run to track the index pulse coming from the spinning floppy diskette. This example is for running on models */84 and 10.

```
: I 14(CR)          (get current value of SysPort)
Input 14 = AF

: O 14 BE(CR)       (select A and motor on)

: T FLPY(CR)        (run test and dump changes)
04 0000
06 3901
04 39E6
06 7A17
04 7AFC
06 BB2C
04 BC11
06 FC41
04 FD26

: O 14 AF(CR)       (motor and select off)

:
```

In this example, you can see that the TRK00 bit is on and the INDEX bit is cycling (indicating that the drive is spinning the floppy and sending index pulses to the WD1793). Also, a crude calculation of the motor speed can be made. Subtracting the first two adjacent "06" statuses gives 4116H or 16662 iterations. At 12 uS per iteration this computes to 199.944 milliseconds, where the perfect result would be 200 mS to exactly match the 5 RPM speed of the standard floppy motor.

More sophisticated tests may be done by setting up WD1793 registers and using a more complex FDC command. Note that performing actual disk I/O is not practical with this interface, but SEEK with verify commands will read sector headers to verify the track, and so do a modicum of I/O internally.

Floppy Testing (Stepping)

This test checks the ability of the drive to step in/out, and the FDC management of that. There is no need to have a floppy in the drive for this test (unless the Verify bit is set in the commands), but the head protector should be removed and the drive door left open. SEEK and RESTORE commands are set to 30mS per step, and each should span 5 tracks, so total time should be about 150mS. When issuing the SEEK and RESTORE commands, listen for the head stepping noise.

```
: I 14(CR)
Input 14 = EF      (current sysport)

: O 14 FE(CR)      (motor on, select A)

: O 10 03(CR)      (RESTORE - make sure drive is at track 0)

: O 13 05(CR)      (set destination track to 5)

: T FLPY 13(CR)    (send SEEK command)
45 0002            (24uS: command starts, BUSY on, TRK00 on)
41 00A4            (1.9mS: TRK00 goes off)
40 30D7            (150mS: command done)

: I 11(CR)
Input 11 = 05      (check current track = 5)

: T FLPY 03(CR)    (send RESTORE command)
41 0002            (24uS: command starts, BUSY on)
45 28C4            (125mS: TRK00 on)
44 30FD            (150mS: command done)

: O 14 EF(CR)      (motor off, drive select off)

:
```

Floppy Testing (Reading media)

For this test, a formatted floppy is required to be in the drive. The SysPort value is chosen for the density and side, as well as drive and motor-on. This examples reads the first directory sector (sector 0A on side 1) of a DD floppy:

```
: I 14(CR)
Input 14 = EF

: O 14 DA(CR)      (motor on, DDEN, side 1, drive A)

: T FDRD 0A(CR)    (read sector 10)
00                 (no errors)
: D 8000 81FF(CR)
8000 00 50 49 50 20 20 20 20 20 43 4F 4D 00 00 00 3A   .PIP     COM...:
8010 02 03 04 05 00 00 00 00 00 00 00 00 00 00 00 00   ................
```

```
8020 00 45 44 49 54 20 20 20 20 43 4F 4D 00 00 00 80   .EDIT    COM....
8030 06 07 08 09 0A 0B 0C 0D 00 00 00 00 00 00 00 00   ................
8040 00 53 54 41 54 20 20 20 20 43 4F 4D 00 00 00 29   .STAT    COM...)
8050 0E 0F 10 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8060 00 43 20 20 20 20 20 20 20 43 4F 4D 01 00 00 80   .C       COM....
8070 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20   ...............
8080 00 43 20 20 20 20 20 20 20 43 4F 4D 02 00 00 34   .C       COM...4
8090 21 22 23 24 00 00 00 00 00 00 00 00 00 00 00 00   !"#$............
80A0 00 52 4D 41 43 20 20 20 20 43 4F 4D 00 00 00 6A   .RMAC    COM...j
80B0 25 26 27 28 29 2A 2B 00 00 00 00 00 00 00 00 00   %&'()*+.........
80C0 00 4C 49 4E 4B 20 20 20 20 43 4F 4D 00 00 00 7B   .LINK    COM...{
80D0 2C 2D 2E 2F 30 31 32 33 00 00 00 00 00 00 00 00   ,-./0123........
80E0 00 4C 49 42 20 20 20 20 20 43 4F 4D 00 00 00 38   .LIB     COM...8
80F0 34 35 36 37 00 00 00 00 00 00 00 00 00 00 00 00   4567............
8100 00 2F 20 20 20 20 20 20 20 43 4F 4D 00 00 00 0A   ./       COM....
8110 38 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   8...............
8120 00 4D 41 4B 45 4C 49 42 20 53 55 42 00 00 00 04   .MAKELIB SUB....
8130 39 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   9...............
8140 00 4A 55 4E 4B 20 20 20 20 53 55 42 00 00 00 01   .JUNK    SUB....
8150 3A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   :...............
8160 00 42 45 4C 4C 20 20 20 20 41 53 4D 00 00 00 01   .BELL    ASM....
8170 3B 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ;...............
8180 00 43 4F 4D 50 4C 49 42 20 53 55 42 00 00 00 0D   .COMPLIB SUB....
8190 3F 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ?...............
81A0 00 49 4E 44 45 58 20 20 20 52 45 4C 00 00 00 01   .INDEX   REL....
81B0 3C 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   <...............
81C0 00 43 4F 4D 4D 41 4E 44 20 52 45 4C 00 00 00 09   .COMMAND REL....
81D0 45 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   E...............
81E0 00 45 58 45 43 20 20 20 20 52 45 4C 00 00 00 04   .EXEC    REL....
81F0 46 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   F...............
: O 14 EF(CR)      (motor, etc, off)

:
```

HDD Testing

Here is an example of the commands needed to test reading of the first boot sector. This example is taken from a run on the Kaypro simulator, so the timings of the commands is not what would be seen on real hardware. This example is for a disk SYSGEN'ed with CP/M 2.2u (ROM 81-478).

```
: N HDD(CR)        (reset WD1002)
D0 0000
50 0003
01                 (normal error, Kaypro WD1002 has no floppy controller)
: O 86 A8(CR)      (set SDH value for head 0)

: O 82 01(CR)      (set sector count 1)

: O 83 00(CR)      (set sector 0)

: O 84 00(CR)      (set cylinder low 0)

: O 85 00(CR)      (set cylinder high 0)

: T HDD 20(CR)     (issue READ command)
58 0000            (status bit 08 is DRQ)
00
```

```
: T HDRD(CR)        (load WD1002 data buffer into 8000H)
8200
: D 8000 81FF(CR) (dump buffer, CP/M 2.2u boot sector)
8000 18 FE 00 D8 00 EE 37 00 00 00 00 00 00 00 00 00   ......7.........
8010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 13 03   ................
8080 C3 5C DB C3 58 DB 7F 00 20 20 20 20 20 20 20 00   .\..X...        .
8090 20 4D 41 53 4D 45 4E 55 00 43 4F 50 59 52 49 47    MASMENU.COPYRIG
80A0 48 54 20 28 43 29 20 31 39 37 39 2C 20 44 49 47   HT (C) 1979, DIG
80B0 49 54 41 4C 20 52 45 53 45 41 52 43 48 20 00 00   ITAL RESEARCH ..
80C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
80F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00   ................
8100 00 00 00 00 00 00 00 00 08 D8 00 00 5F 0E 02 C3   ............_...
8110 05 00 C5 CD 8C D8 C1 C9 3E 0D CD 92 D8 3E 0A C3   ........>....>..
8120 92 D8 3E 20 C3 92 D8 C5 CD 98 D8 E1 7E B7 C8 23   ..> ........~..#
8130 E5 CD 8C D8 E1 C3 AC D8 0E 0D C3 05 00 5F 0E 0E   ............._..
8140 C3 05 00 CD 05 00 32 EE DF 3C C9 0E 0F C3 C3 D8   ......2..<......
8150 AF 32 ED DF 11 CD DF C3 3F EE 0E 10 C3 C3 D8 0E   .2......?.......
8160 11 C3 C3 D8 0E 12 C3 C3 D8 11 CD DF C3 DF D8 0E   ................
8170 13 C3 05 00 CD 05 00 B7 C9 0E 14 C3 F4 D8 11 CD   ................
8180 DF C3 F9 D8 0E 15 C3 F4 D8 0E 16 C3 C3 D8 0E 17   ................
8190 C3 05 00 1E FF 0E 20 C3 05 00 CD 13 D9 87 87 87   ...... .........
81A0 87 21 EF DF B6 32 04 00 C9 3A EF DF 32 04 00 C9   .!...2...:..2...
81B0 FE 61 D8 FE 7B D0 E6 5F C9 3A AB DF B7 CA 96 D9   .a..{.._.:......
81C0 3A EF DF B7 3E 00 C4 BD D8 11 AC DF CD CB D8 CA   :...>...........
81D0 96 D9 3A BB DF 3D 32 CC DF 11 AC DF CD F9 D8 C2   ..:..=2.........
81E0 96 D9 11 07 D8 21 80 00 06 80 CD 42 DC 21 BA DF   .....!.....B.!..
81F0 36 00 23 35 11 AC DF CD DA D8 CA 96 D9 3A EF DF   6.#5.........:..
:
```

Memory Test ROM

The memory test binary image may be downloaded here:

http://sebhc.durgadas.com/kaypro/memtest.bin

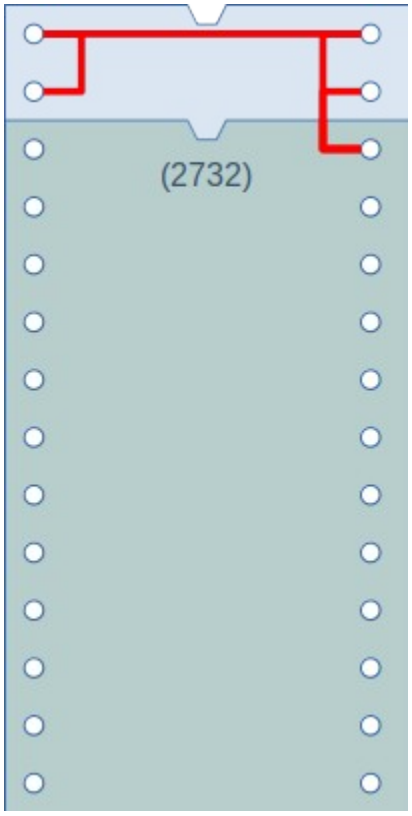
This image does not depend on RAM to operate (uses no stack or RAM variables) but it does use the serial port for progress (output) only. It does a memory test in the range 8000H-FFFFH and will alternate drive A and B LEDs (*/84 and 10 models) or cycle through ‘0’ to ‘9’ in the first character of the display (*/83 models). If a memory error is detected, it will flash the drive A LED or alternate ‘E’ and ‘R’ in the first character of the display (depending on the Kaypro model).

Serial port output begins with a signon message showing the test version. During the test, it will output the current “seed” value being run (00-99 BCD). If an error is encountered, it will print the error address, expected value, and actual value (and “Error”).

The test method is to write a BCD value 00-99H to each memory location. The seed value dictates the value put in location 8000H, with each successive location receiving the previous value +1 (BCD). On each pass, the seed value is incremented (BCD).

Adapting 8K ROMs

Using an 8K ROM (2764, 28C64, etc) on a Kaypro that requires a 2732 may be done using an adapter. There are adapter kits available online, or you may build one from a 28-pin socket (machined pins recommended). The following diagram shows how to wire the socket, which is inserted into the 2732 socket with the top overhanging (aligned on bottom pins). Note that the wire soldered to pin 26 must not interfere with insertion into the 2732 socket. Pins 1, 2, 27, and 28 may need to be clipped to avoid interference with components on the mainboard.



Using a socket adapter requires that the 28C64 be programmed with the image in the upper half (1000H-1FFFH), or else replicated in both halves.

This same adapter could be used to put a 28C64 in a 2716 socket, but only a 2K image can be used and must be programmed into the upper quarter (1800H-1FFFH) of the 28C64 (or replicated into all quarters).