Datasheet

MM32W0xxBnc

32-bit Micro controller based on ARM Cortex M0

Ver: 1.81_n

Content

Onyx Components & Systems (P) Ltd.,6-1-85/4,Saifabad,Hyderabad-500004,Ph:040-23237230/Fax:040-66631800,Email:onyx@onyxindia.com

Onyx Components & Systems (P) Ltd.,6-1-85/4,Saifabad,Hyderabad-500004,Ph:040-23237230/Fax:040-66631800,Email:onyx@onyxindia.com

List of Figures

List of Tables

Onyx Components & Systems (P) Ltd.,6-1-85/4,Saifabad,Hyderabad-500004,Ph:040-23237230/Fax:040-66631800,Email:onyx@onyxindia.com

1 Introduction

Introduction

1.1 Description

This product is an ultra-low-power single-mode Bluetooth chip with a frequency of 2.4 GHz ISM band and a 2 MHz channel spacing, which complies with the Bluetooth specification. MM32W0xxBnc(named as ”the device” throughout this document) is ARM® Cortex™-M0 32-bit RISC core based micro controller family. The device has high speed embedded memory and the CPU, memory and AHB bus subsystem speed can attain up to 48MHz. The device also has integrated with extensive range of enhanced I/Os, two APB buses peripherals, 1 12-bit ADC, 2 Comparators, 2 general purpose 16-bit timers, 1 general purpose 32-bit timer, 3 Basic timers, 1 Advanced 16-bit timer, and standard communication interfaces device: 1 I2C, 1 SPI, 1 USB, 1 CAN, and 2 UARTs.

The device operates from a 2.3V to 3.6V power supply. They are available in both the -40°C to +85°C temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The devices are available in 2 different packages: LQFP48 and QFN32. Depending on the device chosen, different sets of peripherals are included.

The abundant peripheral configurations enable the device to fit wide range of applications in difference industries, Few examples are as follows:

- Beacon
- Wireless keyboard, mouse
- Industrial applications: industrial remote control, telemetry
- Alarm system, access control system, data acquisition and transmission system

1.2 Product Features

- Core and system
  - ARM® Cortex™-M0 CPU
  - Maximum operating frequency is up to 48MHz
  - Single instruction cycle 32-bit hardware multiplier
- Memories
  - 128K Bytes of Flash memory
  - 8K Bytes of SRAM
  - Boot loader support Chip Flash and ISP (In-System Programming)

- Single mode BLE RF transceiver
  - Packet processing engine
  - GFSK coding method
  - Internal voltage regulator guarantees PSRR
  - Programmable transmit power range: -28dBm to +4dBm
  - 1Mbps air data transmission
  - Excellent RF link budget: up to -80dBm
- Clock, reset and power management
  - 2.3V to 3.6V application supply
  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - External 16MHz high speed crystal oscillator
  - Embedded factory-tuned 48MHz high speed oscillator
  - Embedded 40KHz low speed oscillator
  - PLL supports CPU running at 48MHz
- Low-power
  - Sleep, Stop and Standby modes
- 1 12-bit ADC, 1μS A/D converters (up to 10 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
- 2 Comparators
- 5 DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI, ADC and USB
- Up to 28 fast I/Os:
  - All mappable on 16 external interrupt vectors
  - Partial port can work on 5V
- Debug mode
  - Serial wire debug (SWD)
- Up to 9 timers
  - 1 16-bit 4-channel advanced-control timer for 4 channels PWM output, with deadtime generation and emergency stop
  - 2 16-bit timer and 1 32-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - 2 16-bit timer, with 1 IC/OC, 1 OCN, deadtime generation and emergency stop and modulator gate for IR control
  - 1 16-bit timer, with 1 IC/OC
  - 2 watchdog timers (independent and window type)
  - SysTick timer: 24-bit downcounter
- Up to 6 Communication interfaces
  - 2 UARTs
  - 1 I2C
  - 1 SPI
  - 1 CAN

    - 1 USB
- Low cost peripheral component BOM cost
- 96-bit unique ID (UID)
- Packages LQFP48 and QFN32

For more information about the complete product, refer to Section 2.2 of the data sheet. The relevant information about the Cortex^{TM}-M0, please refer to Cortex^{TM}-M0 technical reference manual.

2 Specification

Specification

2.1 Device contrast

Table 1. Device features and peripheral counts

Peripheral \ Device		MM32W051/062/073PFB	MM32W051/062/073NTB
Flash memory -K Bytes		32/64/128	32/64/128
SRAM -K Bytes		4/8/8	4/8/8
Timers	General purpose (16 bit)	4	4
	General purpose (32 bit)	1	1
	Advanced control	1	1
Common interfaces	UART	2	2
	I2C	1	1
	SPI	1	1
	USB	0/1/1	0/1/1
	CAN	0/1/1	0/1/1
GPIOs		28	22
12-bit ADC (number of channels)		1 10 channels	1 7 channels
Comparators		2	
Max CPU frequency		48 MHz	
AES		YES	
Operating voltage		2.3V ~ 3.6V	
Packages		LQFP48	QFP32

2.2 Summary

2.2.1 ARM® Cortex™-M0 and SRAM

The ARM® Cortex™-M0 is a generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex™-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The devices have embedded ARM core and are compatible with all ARM tools and software.

2.2.2 Memory

128K Bytes of embedded Flash memory.

2.2.3 SRAM

8K Bytes of embedded SRAM.

2.2.4 Clocks and startup

When the system is powered up, the default clock is from PLL with the resource from HSE 48 MHz oscillator. An external 2 ~ 24 MHz clock can also be configured to monitor the system during power up phases.

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48MHzz.Refer to figure 3 for the clock drive block diagram.

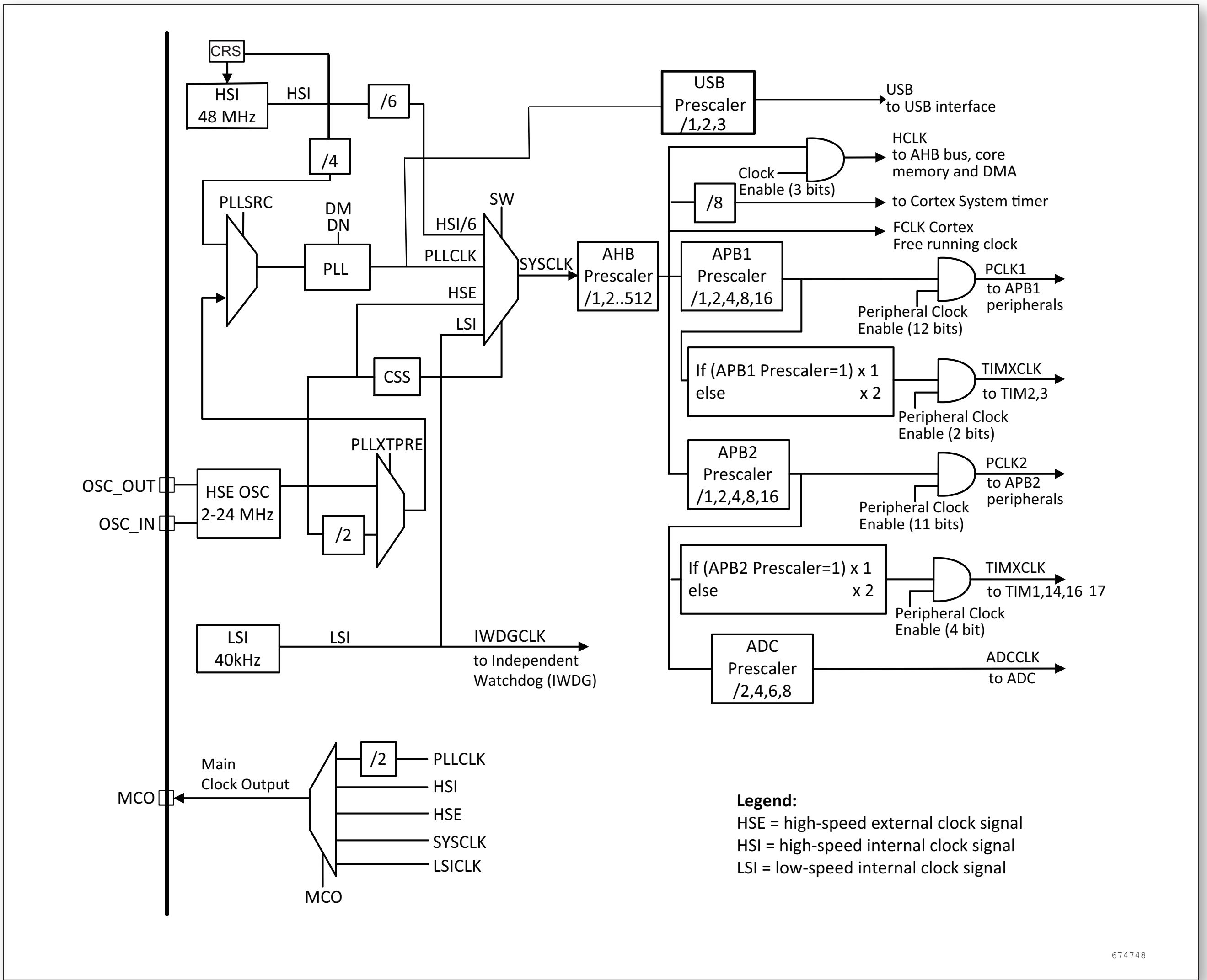

Figure 1. Clock tree

2.2.5 Nested vectored interrupt controller (NVIC)

The device embeds a nested vectored interrupt controller and is able to handle up to 68 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) with 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.6 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of many edge detector lines are used to generate interrupt/event requests for waking up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal APB2 clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using UART1.

2.2.8 Power supply schemes

- V_{DD} = 2.3V ~ 3.6V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA}= 2.3V ~ 3.6V: external analog power supply for reset blocks, oscillators and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

2.2.9 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 1.8V. The device remains in reset mode when the monitored supply voltage is below a specified threshold $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold.The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.10 Voltage regulator

The voltage regulator converts the external voltage to the internal digital logic and it is always enabled after reset.

2.2.11 Low-power modes

The device support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. the HSI and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

Standby mode

Standby mode achieves the lowest power consumption of the system. This mode turns off the voltage regulator in CPU deep sleep mode. The entire 1.5V power supply area is powered down. PLL、HSI and HSE oscillators are also powered down. SRAM and register contents are missing. Only the backup registers and standby circuits remain powered.

2.2.12 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: UART、I2C、SPI、USB、CAN、ADC general-purpose and advanced-control timers TIMx.

2.2.13 Backup register (BKP)

The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are still powered by V_{BAT}. They are also not reset when the system is woken up in standby mode, or when the system is reset or power is reset.

2.2.14 Timers and watchdogs

Medium capacity device include 1 advanced control、5 general-purpose timers 、2 watchdog timers and 1 SysTick timer.

The following table compares the features of the different timers:

Table 2. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/-compare channels	Complem-entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to $2^{32}-1$	Yes	4	No
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
basic	TIM14	16-bit	Up	integer from 1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	Yes

Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for：

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are 5 synchronizable general-purpose timers (TIM2、TIM3).

General-purpose timers 32-bit

The timer is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

General-purpose timers 16-bit

The timer is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

The timer can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output. Their counter can be frozen in debug mode.

TIM16/TIM17

Every timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. They each have a single channel for input capture/output compare, PWM or one-pulse mode output. TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.15 Universal asynchronous receiver/transmitter (UART)

UART provides hardware management of the CTS, RTS.

Support LIN master-slave function.

All UART interface can be served by the DMA controller.

2.2.16 I2C interface

The I2C interface can operate in multimaster or slave modes. It can support Standard mode,and Fast Mode.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask).

2.2.17 Serial peripheral interface (SPI)

The SPI interface, in slave or master mode, can be configured to 1 ~ 32 bits per frame.

All SPI interface can be served by the DMA controller.

2.2.18 Universal serial bus (USB)

The microcontroller embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface.The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.2.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0 A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

2.2.20 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.21 Analog-to-digital converter (ADC)

The one 12-bit analog-to-digital converters is embedded into microcontrollers and the ADC shares up to 10 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs. The ADC can be served by the DMA controller.

The analog watchdog function allows very precise monitoring of all the way, multiple or all selected channels, and an interruption occurs when the monitored signal exceeds the preset threshold. The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger to allow the application to synchronize A/D conversion and timers.

2.2.22 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel which is used to convert the sensor output voltage into a digital value.

2.2.23 Serial single line SWD debug port (SW-DP)

Built-in ARM two-wire serial debug port (SW-DP) .

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

2.2.24 Comparator (COMP)

The devices embed 2 general purpose comparators. that can be used either as standalone devices (all terminal are available on I/Os) or combined with the timers. The comparators can be used for a variety of functions including：

- Wake-up from low-power mode triggered by an analog signal,
- Analog signal conditioning,
- Cycle-by-cycle current control loop when combined with the PWM output from a timer.

- Rail-to-rail comparators
- Each comparator has positive and configurable negative inputs used for flexible voltage
- Selection:
  - Reusable I/O pins

– Internal comparison voltage CRV selects the voltage divider value of AVDD or internal reference voltage
- Programmable hysteresis
- Programmable speed/consumption
- The outputs can be redirected to an I/O or to timer inputs for triggering:
  – Capture events
  – OCref_clr events (for cycle-by-cycle current control)
  – Break events for fast PWM shutdowns

The chip integrates the Bluetooth specification and RF transceiver and is compatible with the 2.4GHz ISM band defined by the International Telecommunications Union Radiocommunication Bureau.

After the chip is powered, the RF transceiver can be wirelessly transceived by simply building a simple peripheral component. It offers an excellent RF link budget of up to -80dBm with a shutdown current of less than 250uA for the entire chip.

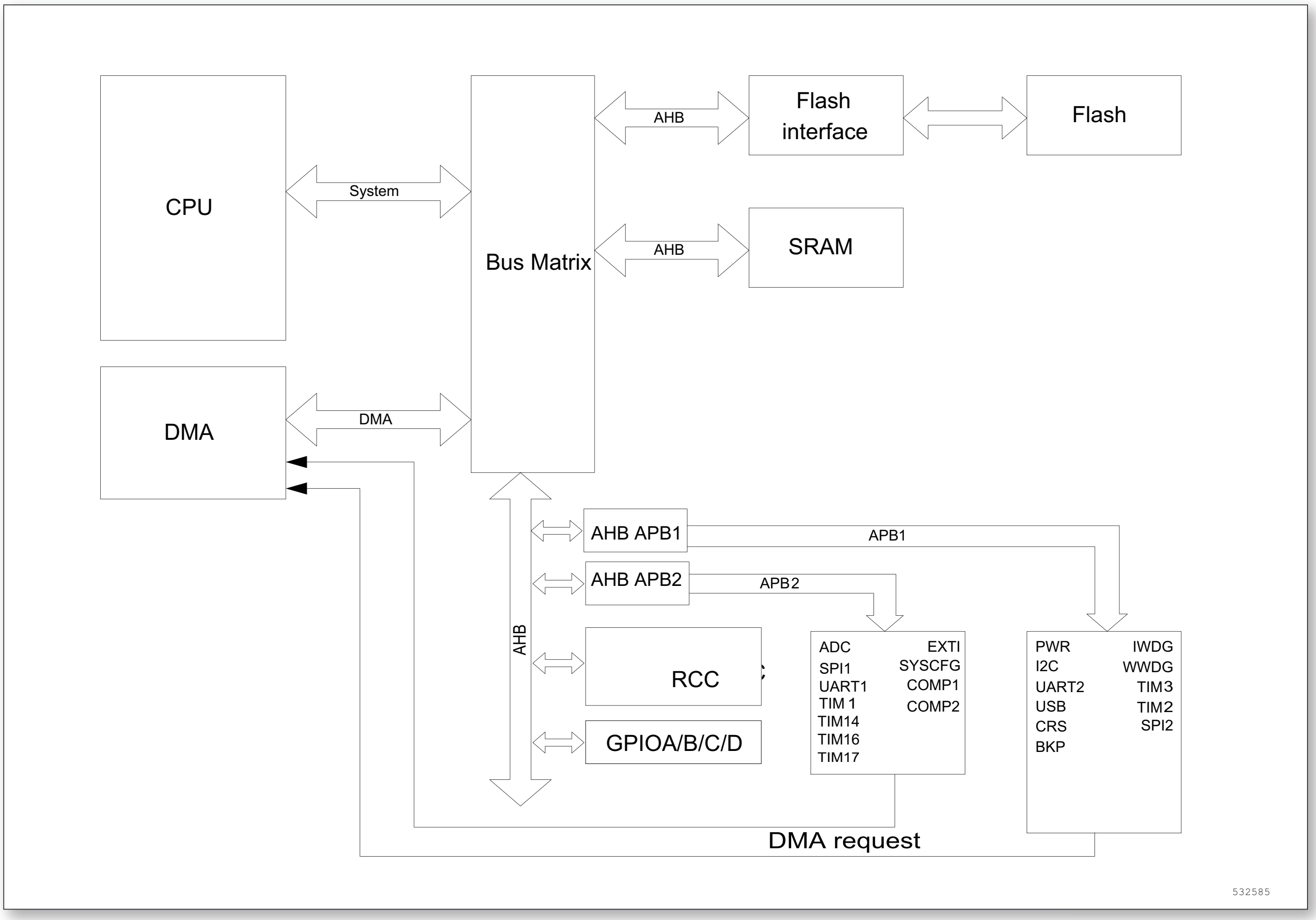

Figure 2. Block diagram

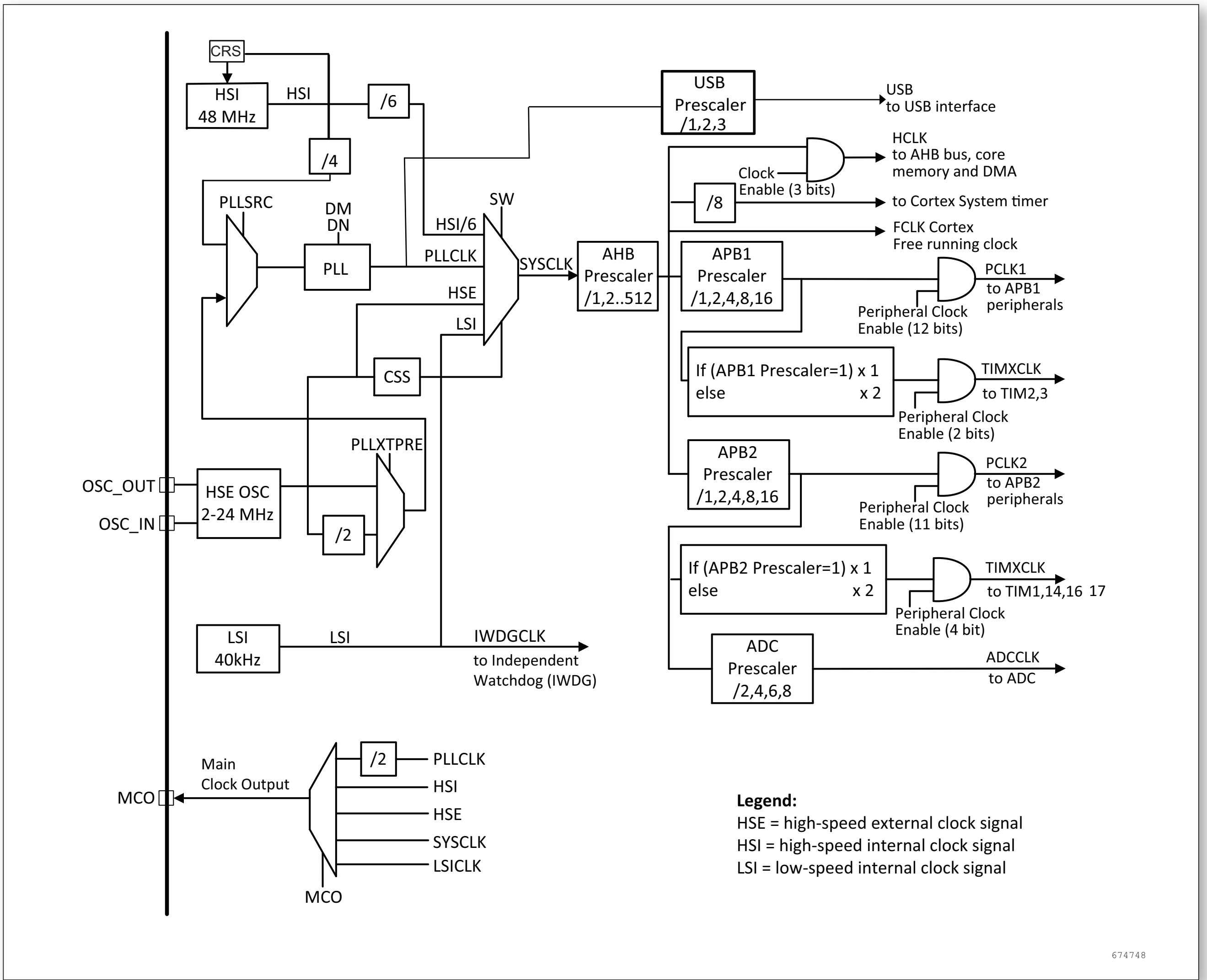

Figure 3. Clock tree

3 Pin definition

Pin definition

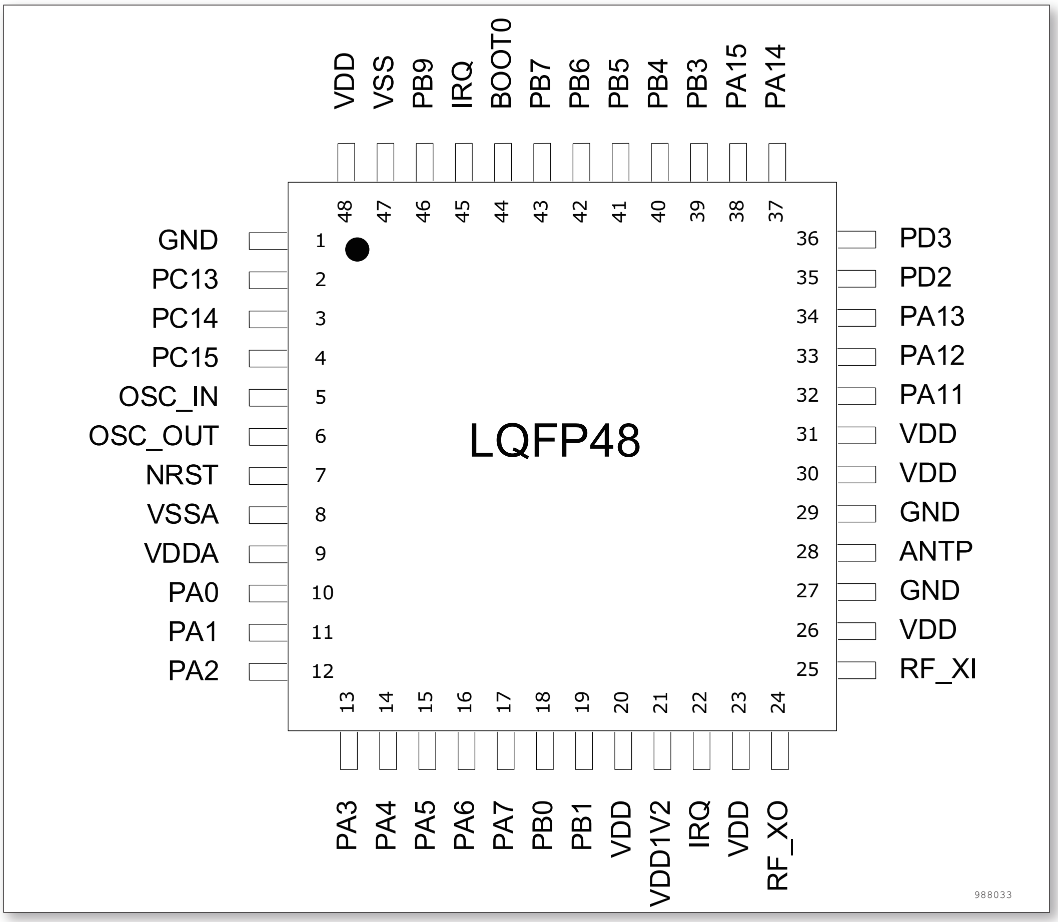

Figure 4. LQFP48 packet pinout

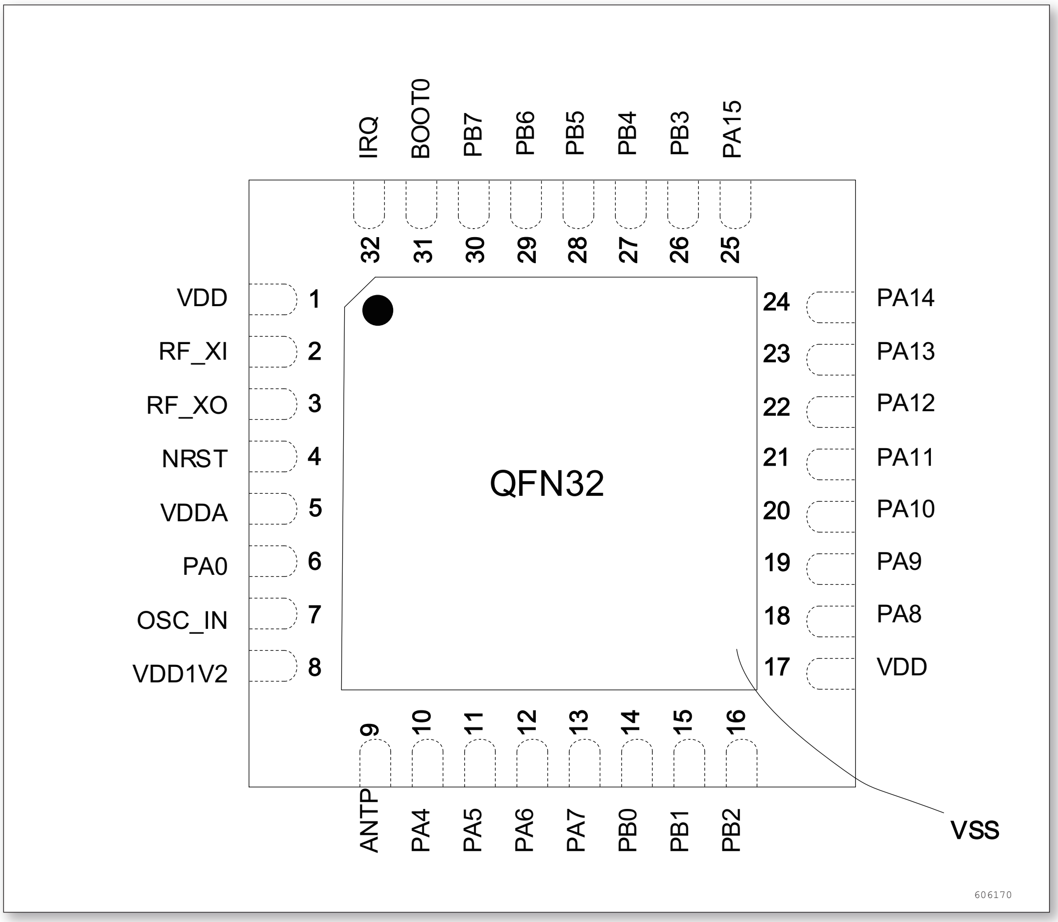

Figure 5. QFN32 packet pinout

Table 3. LQFP48 Pin definitions

Pin number LQFP48	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
1	GND	S	-	NC	-	-
2	PC13	I/O	-	PC13	-	-
3	PC14	I/O	-	PC14	-	-
4	PC15	I/O	-	PC15	-	-
5	OSC_IN	I	-	OSC_IN	-	OSC_IN
6	OSC_OUT	O	-	OSC_OUT	-	OSC_OUT
7	NRST	I/O	-	NRST	-	-
8	VSSA	S	-	VSSA	-	-
9	VDDA	S	-	VDDA	-	-
10	PA0-WKUP	I/O	-	PA0	TIM2_CH1_ ETR/ UART2_CTS/ ADC_VIN[0]	WKUP/ COMP1_OUT
11	PA1	I/O	-	PA1	TIM2_CH2/ UART2_RTS/ ADC_VIN[1]	-

Pin number LQFP48	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
12	PA2	I/O	-	PA2	TIM2_CH3/ UART2_TX/ ADC_VIN[2]	COMP2_OUT
13	PA3	I/O	-	PA3	TIM2_CH4/ UART2_RX/ ADC_VIN[3]	-
14	PA4	I/O	-	PA4	SPI1_NSS/ TIM14_CH1/ ADC_VIN[4]	-
15	PA5	I/O	-	PA5	SPI1_SCK/ TIM2_CH1_ETR/ ADC_VIN[5]	-
16	PA6	I/O	-	PA6	SPI1_MISO/ TIM3_CH1/ TIM16_CH1/ TIM1_BKIN/ ADC_VIN[6]	COMP1_OUT
17	PA7	I/O	-	PA7	SPI1_MOSI/ TIM3_CH2/ TIM1_CH1N/ TIM14_CH1/ TIM17_CH1/ ADC_VIN[7]	COMP2_OUT
18	PB0	I/O	-	PB0	TIM3_CH3/ TIM1_CH2N/ ADC_VIN[8]	-
19	PB1	I/O	-	PB1	TIM14_CH1/ TIM3_CH4/ TIM1_CH3N/ ADC_VIN[9]	-
20	VDD	S	-	VDD	-	-
21	VDD1V2	S	-	RF_$V_{DVDD1.2}$	-	-
22	IRQ	I/O	-	RF_IRQ	-	-
23	VDD	S	-	RF_V_{VDD}	-	-
24	RF_XO	O	-	RF_XO	-	-
25	RF_XI	I	-	RF_XI	-	-
26	VDD	S	-	RF_V_{VDD}	-	-

Pin number LQFP48	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
27	GND	S	-	-	-	-
28	ANTP	-	-	ANTP	-	-
29	GND	S	-	-	-	-
30	VDD	S	-	RF_V_{VDD}	-	-
31	VDD	S	-	RF_V_{VDD}	-	-
32	PA11	I/O	FT	PA11	UART1_CTS/ TIM1_CH4/ CAN_RX/ I2C1_SCL/ USBDM	COMP1_OUT
33	PA12	I/O	FT	PA12	UART1_RTS/ TIM1_ETR/ CAN_TX/ I2C1_SDA/ USBDP	COMP2_OUT
34	PA13	I/O	FT	PA13	SWDIO	-
35	PD2	I/O	FT	PD2	-	-
36	PD3	I/O	FT	PD3	-	-
37	PA14	I/O	FT	PA14	SWDCLK/ UART2_TX	-
38	PA15	I/O	FT	PA15	SPI1_NSS/ UART2_RX/ TIM2_CH1_ETR	-
39	PB3	I/O	FT	PB3	SPI1_SCK/ TIM2_CH2	-
40	PB4	I/O	FT	PB4	SPI1_MISO/ TIM3_CH1	-
41	PB5	I/O	FT	PB5	SPI1_MOSI/ TIM3_CH2/ TIM16_BKIN	-
42	PB6	I/O	FT	PB6	UART1_TX/ I2C1_SCL/ TIM16_CH1N	-
43	PB7	I/O	FT	PB7	UART1_RX/ I2C1_SDA/ TIM17_CH1N	-
44	BOOT0	I	FT	BOOT0	-	-

Pin number LQFP48	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
45	IRQ	I	FT	IRQ	-	-
46	PB9	I/O	FT	PB9	I2C1_SDA/ TIM17_CH1	-
47	VSS	S	-	VSS	-	-
48	VDD	S	-	VDD	-	-

Table 4. QFN32 Pin definitions

Pin number QFN32	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
0	VSS	S	-	VSS	-	-
1	VDD	S	-	VDD	-	-
2	RF_XI	I	FT	RF_OSC_IN	-	RF_OSC_IN
3	RF_XO	O	FT	RF_OSC_OUT	-	RF_OSC_OUT
4	NRST	I/O	FT	NRST	-	-
5	VDDA	S	FT	VDDA		-
6	PA0-WKUP	I/O	-	PA0	UART2_CTS/ TIM2_CH1_ ETR/ ADC_VIN[0]	WKUP/ COMP1_OUT
7	OSC_IN	I	FT	OSC_IN	-	OSC_IN
8	VDD1V2	S	-	RF_V_{VDD1V2}	-	-
9	ANTP	-	-	ANTP	-	-
10	PA4	I/O	FT	PA4	SPI1_NSS/ TIM14_CH1/ ADC_VIN[4]	-
11	PA5	I/O	FT	PA5	SPI1_SCK/ TIM2_CH1_ETR/ ADC_VIN[5]	COMP1_OUT
12	PA6	I/O	FT	PA6	SPI1_MISO/ TIM3_CH1/ TIM1_BKIN/ TIM16_CH1/ ADC_VIN[6]	COMP2_OUT

Pin number QFN32	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
13	PA7	I/O	FT	PA7	SPI1_MOSI/ TIM3_CH2/ TIM1_CH1N/ TIM14_CH1/ TIM17_CH1/ ADC_VIN[7]	-
14	PB0	I/O	FT	PB0	TIM3_CH3/ TIM1_CH2N/ ADC_VIN[8]	-
15	PB1	I/O	FT	PB1	TIM14_CH1/ TIM3_CH4/ TIM1_CH3N/ ADC_VIN[9]	-
16	PB2	I/O	FT	PB2	-	-
17	VDD	S	FT	RF_V_{VDD}	-	-
18	PA8	I/O	FT	PA8	TIM1_CH1/ MCO	-
19	PA9	I/O	FT	PA9	UART1_TX/ TIM1_CH2/ UART1_RX/ I2C1_SCL/ MCO	-
20	PA10	I/O	FT	PA10	TIM17_BKIN/ UART1_RX/ TIM1_CH3/ UART1_TX/ I2C1_SDA	-
21	PA11	I/O	FT	PA11	UART1_CTS/ TIM1_CH4/ CAN_RX/ I2C1_SCL/ USBDM	COMP1_OUT
22	PA12	I/O	FT	PA12	UART1_RTS/ TIM1_ETR/ CAN_TX/ I2C_SDA/ USBDP	COMP2_OUT

Pin number QFN32	Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
23	PA13	I/O	-	PA13	SWDIO	-
24	PA14	I/O	-	PA14	SWCLK/ UART2_TX	-
25	PA15	I/O	FT	PA15	TIM2_CH1_ETR/ SPI1_NSS/ UART2_RX	-
26	PB3	I/O	FT	PB3	TIM2_CH2/ SPI1_SCK	-
27	PB4	I/O	FT	PB4	TIM3_CH1/ SPI1_MISO	-
28	PB5	I/O	FT	PB5	TIM3_CH2/ SPI1_MOSI/ TIM16_CH1N	-
29	PB6	I/O	FT	PB6	UART1_TX/ I2C_SCL/ TIM16_CH1N	-
30	PB7	I/O	FT	PB7	UART1_RX/ I2C_SDA/ TIM17_CH1N	-
31	BOOT0	I	FT	PB8	-	-
32	IRQ	I/O	FT	RF_IRQ	-	-

1. I = input, O = output, S = power supply, HiZ = high resistance.
2. FT: 5V tolerant, Input signal should be between VDD and 5V.

Table 5. Alternate functions for port A

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1 _ ETR	-	-	-	-	COMP1_OUT
PA4	SPI1_NSS	-	-	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK	-	TIM2_CH1 _ETR	-	-	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	COMP1_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	-	COMP2_OUT
PA8	MCO	-	TIM1_CH1	-	CRS_SYNC	-	-	-
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	-	-	-
PA11	-	UART1_CTS	TIM1_CH4	-	CAN_RX	I2C1_SCL	-	COMP1_OUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA12	-	UART1_RTS	TIM1_ETR	-	CAN_TX	I2C1_SDA	-	COMP2_OUT
PA13	SWDIO	-	-	-	-	-	-	-
PA14	SWDCLK	UART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1 _ETR	-	-	-	-	-

Table 6. Alternate functions for port B

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	-	-	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	-	-	-	-
PB2	-	-	-	-	-	-	-	-
PB3	SPI1_SCK	-	TIM2_CH2	-	-	-	-	-
PB4	SPI1_MISO	TIM3_CH1	-	-	-	TIM17_BKIN	-	-
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	-	-
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	-	-	-	-
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	-	-
PB8	-	-	-	-	-	-	-	-
PB9	-	I2C1_SDA	TIM17_CH1	-	-		-	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-		-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-
PB12	-	-	TIM1_BKIN	-	SPI2_MISO	-	-	-
PB13	-	-	TIM1_CH1N	-	SPI2_MOSI	I2C1_SCL	-	-
PB14	-	-	TIM1_CH2N	SPI2_SCK	-	I2C1_SDA	-	-
PB15	-	SPI2_NSS	TIM1_CH3N	-	-	-	-	-

Table 7. Alternate functions for port C and D

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-
PD0	CRS_SYNC	I2C1_SDA	-	-	-	-	-	-
PD1	-	I2C1_SCL	-	-	-	-	-	-
PD2	-	-	-	-	-	-	-	-
PD3	-	-	-	-	-	-	-	-

4 Memory mapping

Memory mapping

Table 8. memory mapping

Bus	Boundaryaddress	Size	Peripheral	Notes
Flash	0x0000 0000 -0x0001 FFFF	128 KB	Main flash memory, system memory, or SRAM, depends on the configuration of BOOT	
	0x0002 0000 -0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000 -0x0801 FFFF	128 KB	Main Flash memory	
	0x0802 0000 -0x 1FFDFFFF	~ 256 MB	Reserved	
	0x1FFE 0000 -0x1FFE 01FF	0.5 KB	Protect bytes	
	0x1FFE 0200 -0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 -0x1FFE 1BFF	3 KB	Security space	
	0x1FFE 1C00 -0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400 -0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 -0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 -0x1FFF FFFF	~2 KB	Reserved	
SRAM	0x2000 0000 -0x2000 1FFF	8 KB	SRAM	
	0x2000 2000 -0x2FFF FFFF	~ 512 MB	Reserved	
APB1	0x4000 0000 -0x4000 03FF	1 KB	TIM2	
	0x4000 0400 -0x4000 07FF	1 KB	TIM3	
	0x4000 0800 -0x4000 0BFF	8 KB	Reserved	
	0x4000 2800 -0x4000 2BFF	1 KB	BKP	
	0x4000 2C00 -0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 -0x4000 33FF	1 KB	IWDG	
	0x4000 3400 -0x4000 37FF	1 KB	Reserved	
	0x4000 3800 -0x4000 3BFF	1 KB	SPI2	
	0x4000 4000 -0x4000 43FF	1 KB	Reserved	
	0x4000 4400 -0x4000 47FF	1 KB	UART2	
	0x4000 4800 -0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 -0x4000 57FF	1 KB	I2C	
	0x4000 5800 -0x4000 5BFF	1 KB	Reserved	
	0x4000 5C00 -0x4000 5FFF	1 KB	USB	
	0x4000 6000 -0x4000 63FF	1 KB	Reserved	
	0x4000 6400 -0x4000 67FF	1 KB	CAN	

Bus	Boundaryaddress	Size	Peripheral	Notes
APB1	0x4000 6800 –0x4000 6BFF	1 KB	Reserved	
	0x4000 6C00 –0x4000 6FFF	1 KB	CRS	
	0x4000 7000 –0x4000 73FF	1 KB	PWR	
	0x4000 7400 –0x4000 FFFF	35 KB	Reserved	
APB2	0x4001 0000 –0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 –0x4001 07FF	1 KB	EXTI	
	0x4001 0800 –0x4001 23FF	7 KB	Reserved	
	0x4001 2400 –0x4001 27FF	1 KB	ADC	
	0x4001 2800 –0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00 –0x4001 2FFF	1 KB	TIM1	
	0x4001 3000 –0x4001 33FF	1 KB	SPI1	
	0x4001 3400 –0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800 –0x4001 3BFF	1 KB	UART1	
	0x4001 3C00 –0x4001 3FFF	1 KB	COMP	
	0x4001 4000 –0x4001 43FF	1 KB	TIM14	
	0x4001 4400 –0x4001 47FF	1 KB	TIM16	
	0x4001 4800 –0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 –0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000 –0x4002 03FF	1 KB	DMA	
	0x4002 0400 –0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 –0x4002 13FF	1 KB	RCC	
	0x4002 1400 –0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 –0x4002 23FF	1 KB	Flash interface	
	0x4002 2400 –0x4002 5FFF	15 KB	Reserved	
	0x4002 6000 –0x4002 63FF	1 KB	Reserved	
	0x4002 6400 –0x47FF FFFF	~ 128 MB	Reserved	
	0x4800 0000 –0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 –0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 –0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 –0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 –0x5FFF FFFF	~ 384 MB	Reserved	

5 Typical application circuit

Typical application circuit

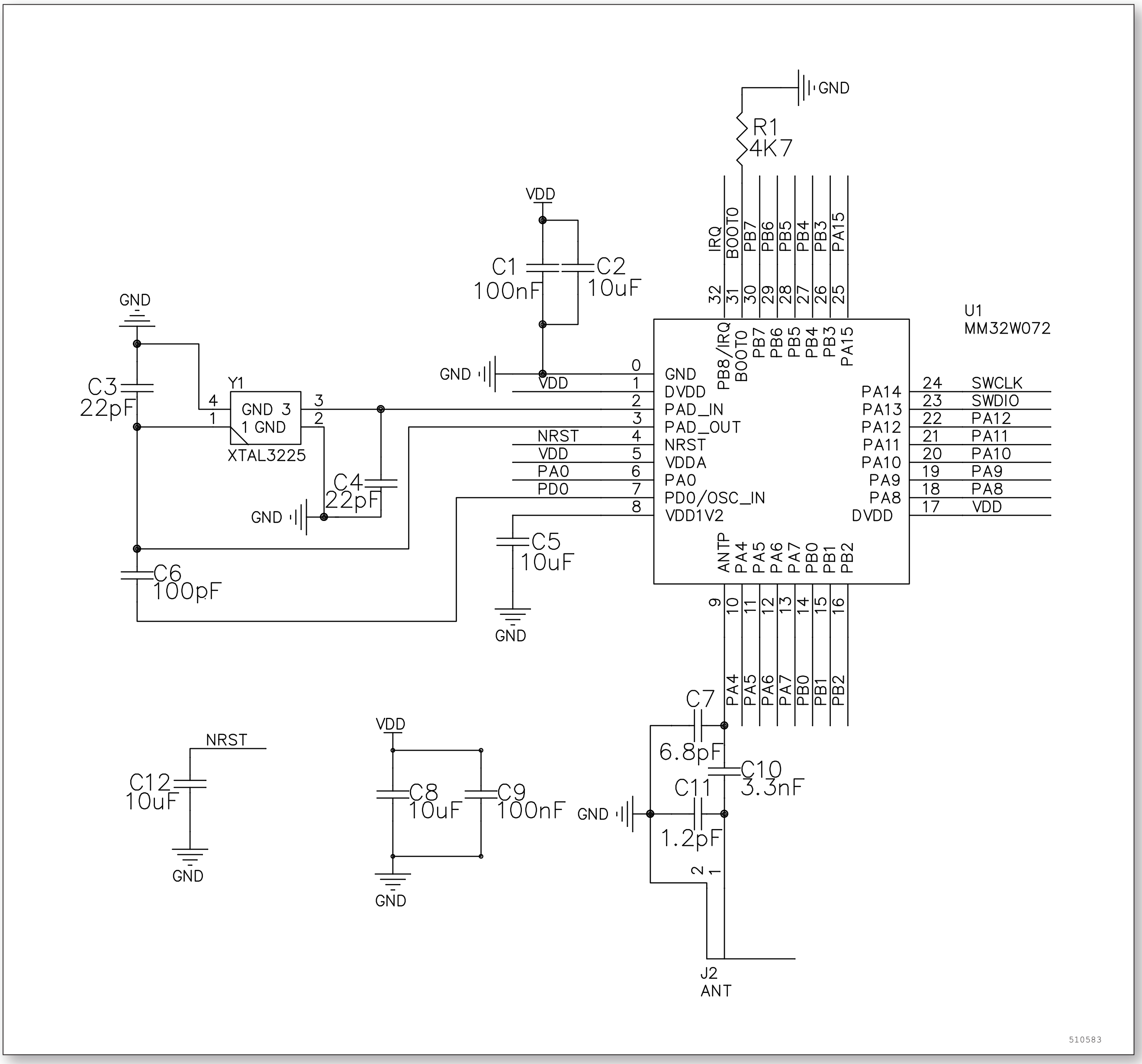

Figure 6. Typical application circuit

Note: This typical application circuit uses a radio frequency module and a control module to share a crystal oscillator solution. If the customer uses the internal clock of the control module, there is no need to add C6, and Pin7 can be used as GPIO.

Table 9. External component list

C1、C2、C8、C9	Decoupling filter capacitor
C3、C4	Crystal loading capacitor
C6	Shared clock capacitor
C5	1.2V digital regulator decoupling capacitor
C7、C11	RF Transformer / Matching Network Capacitor
C10	Through resistance coupling capacitor
R1	Start mode selection resistor
Y1	16MHz crystal oscillator (clock source for RF modules and control modules)
J2	2.4G RF antenna

6 Absolute maximum rating operating conditions

Absolute maximum rating operating conditions

Table 10. Absolute maximum rating

Pin	Parameter	Value	Unit
1、5、17	Control module DC-DC converter supply voltage input and output	-0.3 to +3.6	V
2、3	RF module DC voltage crystal oscillator pin	-0.3 to +3.6	V
4	Control module reset pin	-0.3 to +5.5	V
7	Control module DC voltage crystal oscillator pin	-0.3 to +5.5	V
8	RF module digital power supply 1.2V voltage output	-0.3 to +1.5	V
9	RF Module 2.4G Antenna Pin		V
31	Control module startup mode control pin	-0.3 to +5.5	V
32	RF module interrupt control pin	-0.3 to +3.6	V
6、10、11、12、13、14、15、16、18、19、20、21、22、23、24、25、26、27、28、29、30	Control module DC voltage digital input and output pin	-0.3 to +5.5	V

7 Electrical characteristics

Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.All performance is measured under the 50Ω antenna connector.

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed with an ambient temperature at T_A = 25°C, V_{DD} = 3.3V.

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C and V_{DD} = 3.3V. They are given only as design guidelines and are not tested.

7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The load conditions used for pin parameter measurement are shown in the figure below.

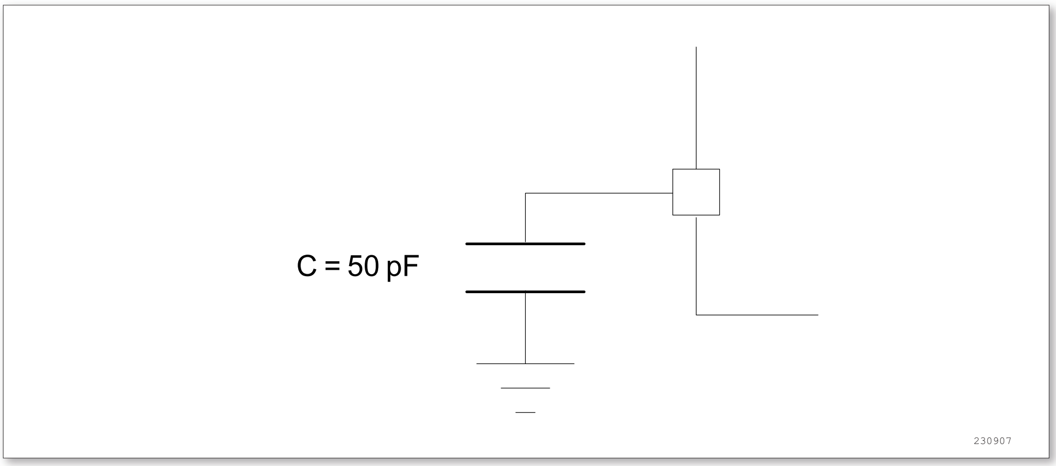

Figure 7. Pin loading conditions

Onyx Components & Systems (P) Ltd.,6-1-85/4,Saifabad,Hyderabad-500004,Ph:040-23237230/Fax:040-66631800,Email:onyx@onyxindia.com

7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is shown in the figure below.

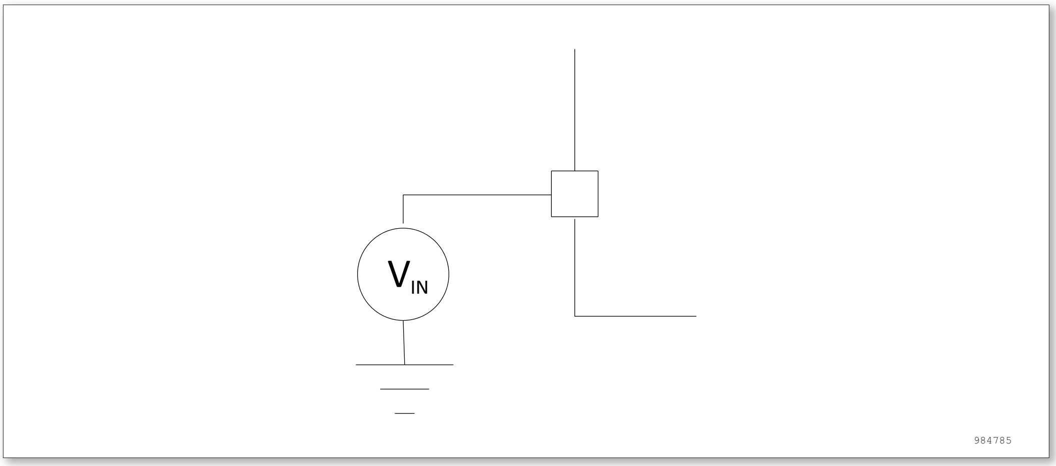

Figure 8. Pin input voltage

7.1.6 Power supply scheme

The power supply design scheme is shown in the figure below.

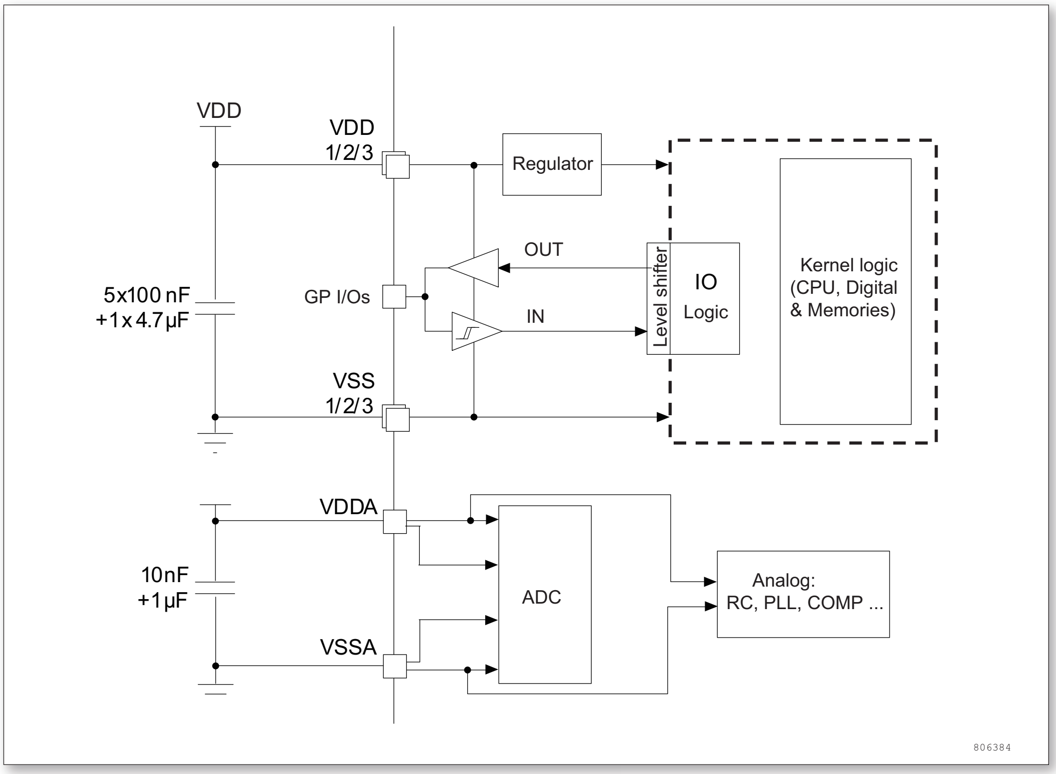

Figure 9. Power supply scheme

Note: The 4.7 μF*capacitor in the above figure must be connected to* V_{DD3}

7.1.7 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

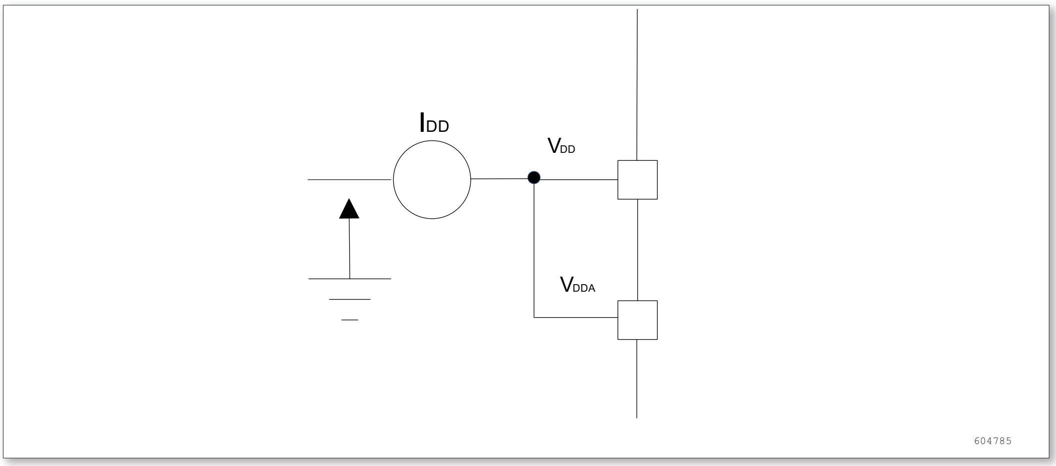

Figure 10. Current consumption measurement scheme

7.2 RF general characteristics

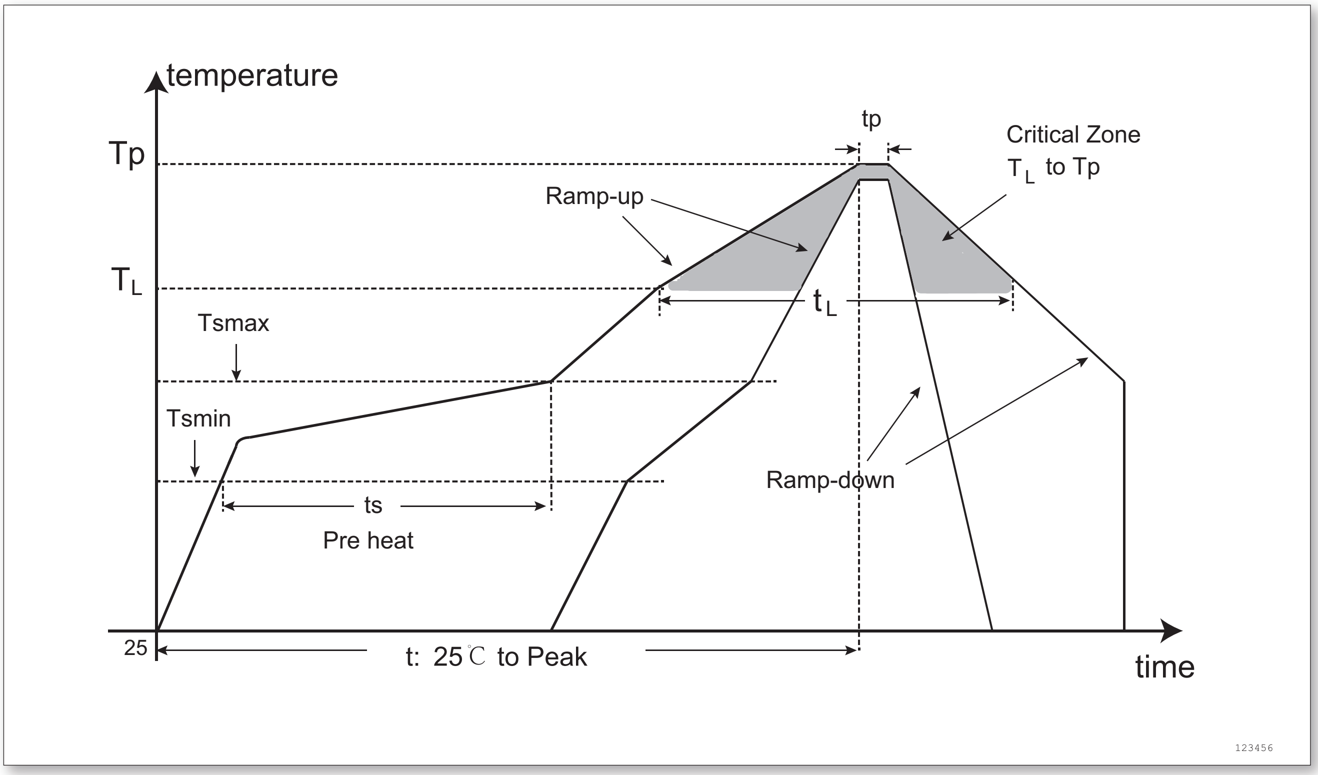

Figure 11. RF performance parameters

Table 11. RF general characteristics

Label	Parameter	Test Conditions	Minimum value	Typical value	Maximum	Unit
FREQ	Frequency change	V_{DD} = 3.0V，T_A = 25°C	2400		2483.5	MHz
FC	Channel spacing	V_{DD} = 3.0V，T_A = 25°C		2		MHz
RFch	RF channel center	V_{DD} = 3.0V，T_A = 25°C	2402		2480	MHz

7.3 RF transmitter characteristics

Table 12. RF Transmitter Characteristics Table

Label	Parameter	Test Conditions	Minimum value	Typical value	Maximum	Unit
MOD	Modulation	GFSK				
BT	Bandwidth			0.5		
M_{index}	Modulation index		0.45	0.5	0.55	
DR	Air transmission index			1		Mbps
P_{max}	Maximum transmission power				+4	dBm
P_{BW1M}	6dB bandwidth modulated carrier (1Mbps)		500			KHz
P_{SPUR}	Spurious emission				-41	dBm
CF_{dev}	Center frequency offset				±150	KHz
$Freq_{drift}$	Frequency drift				±50	KHz
$IFreq_{drift}$	Initial carrier frequency drift				±20	KHz

7.4 RF receiver characteristics

Table 13. RF receiver characteristics

Label	Parameter	Test Conditions	Minimum value	Typical value	Maximum	Unit
RX_{SENS}	Receiving sensitivity	BER < 0.1%		-80		dBm

7.5 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Tables(Table 14、Table 15、Table 16) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Definition	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage(including V_{DDA} and V_{SSA})(1)	- 0.3	3.6	V
V_{IN}	Input voltage on FT and FTf pins(2)	V_{SS} - 0.3	3.6	
	Input voltage on other pins(2)	V_{SS} - 0.3	3.6	
$\|\triangle V_{DDx}\|$	Variations between different V_{DD} power pins		50	mV
$\|V_{SSx} - V_{SS}\|$	Variations between all the different ground pins		50	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to Table below for maximum allowed injected current values.

Table 15. Current characteristics

Symbol	Definition	Max	Unit
I_{VDD}	Total current into sum of all V_{DD}/V_{DDA} power lines(source)(1)	150	mA
I_{VSS}	Total current out of sum of all V_{SS} ground lines(sink)(1)	150	mA
I_{IO}	Output current sunk by any I/O and control pin	20	mA
I_{IO}	Output current source by any I/O and control pin	-18	mA
$I_{INJ(PIN)}$ (2)(3)	Injected current on NRST pins	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injected current on OSC_IN pin of HSE and OSC_IN pin of LSE	±5	mA
$I_{INJ(PIN)}$ (2)(3)	Injected current on other pins(4)	±5	mA
Σ $I_{INJ(PIN)}$ (2)	Total injected current(sum of all I/O and control pins)(4)	±25	mA

1. All main power(V_{DD}, V_{DDA}) and ground(V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ cannot exceed its limit, that is, to ensure that the V_{IN} does not exceed its maximum value. If V_{IN} does not guarantee that its maximum value is not exceeded, ensure that $I_{INJ(PIN)}$ does not exceed its maximum value under external restrictions. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.
3. Negative injection disturbs the analog performance of the device.
4. When several inputs are submitted to a current injection, the maximum $I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Definition	Max	Unit
T_{STG}	Storage temperature range	- 45 ~ + 150	°C
T_J	Maximum junction temperature	125	°C

7.6 Operating conditions

7.6.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	MHz
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	MHz
V_{DD}	Standard operating voltage		2.0	5.5	V
V_{DDA} (1)	Analog operating voltage	Must be the same voltage as V_{DD}	2.5	5.5	V
P_D	Power dissipation temperature:T_A=85°C (2)	LQFP48		594	mW
		QFN32			
T_A	Ambient temperature：T_A = 85°C	Maximum power dissipation	-40	85	°C
		Low power dissipation (3)	-40	105	
	Ambient temperature：T_A = 105°C	Maximum power dissipation	-40	95	°C
		Low power dissipation (3)	-40	125	

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}.
2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (See subsec 7.1).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (See subsec 7.1).

7.6.2 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 18. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{VDD}rise time rate	T_A = 27°C	0	∞	μS/V
	V_{VDD}fall time rate		20	∞	

7.6.3 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 17.

Table 19. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)	1.813	1.819	1.831	V
		PLS[3：0]=0000 (Falling edge)		1.705		V
		PLS[3：0]=0001 (Rising edge)	2.112	2.116	2.124	V
		PLS[3：0]=0001 (Falling edge)		2.0		V
		PLS[3：0]=0010 (Rising edge)	2.411	2.414	2.421	V
		PLS[3：0]=0010 (Falling edge)		2.297		V
		PLS[3：0]=0011 (Rising edge)	2.711	2.714	2.719	V
		PLS[3：0]=0011 (Falling edge)		2.597		V
		PLS[3：0]=0100 (Rising edge)	3.011	3.013	3.018	V
		PLS[3：0]=0100 (Falling edge)		2.895		V
		PLS[3：0]=0101 (Rising edge)	3.311	3.313	3.317	V
		PLS[3：0]=0101 (Falling edge)		3.194		V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge	1.63(1)	1.66	1.68	V
		Rising edge		1.75		V
V_{PDRhys}(2)	PDR hysteresis			100		mV
$T_{RSTTEMPO}$(2)	Reset duration			20		ms

1. The product behavior is guaranteed by design down to the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on (POR reset) to the time when the user application code reads the first instruction.

7.6.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

Description of the measurement method of current consumption, see figure 10。

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period).
- The instruction prefetching function is on. When the peripherals are enabled：f_{PCLK1} = f_{HCLK}.

Note：*The instruction prefetching function must be set before setting the clock and bus divider.*

Table 20. Power consumption parameter

Externally supplied 3.3V DC voltage							
Label	**Parameter**	**Test Conditions**		**Minimum value**	**Typical value**	**Maximum**	**Unit**
I	Supply Current	MCU @ STANDBY mode, RF block @ STANDBY mode		0.008	0.019	0.022	mA
		MCU @ STOP mode, RF block @ STANDBY mode			0.195	0.200	
		MCU @ STOP mode, RF block @ STOP mode		0.242	0.258	0.269	
		MCU @ SLEEP mode, RF block @ STOP mode			4.8	5.3	
		MCU @ ACTIVE mode, RF block @ RX mode		29.07	29.612	30.54	
		MCU @ ACTIVE, RF block @ TX mode	-3dBm		23		
			0dBm		28		
			+3dBm		33.84		
			+4dBm		35.15		

1. The power consumption parameter measured by TX and RX is the clock source using

HSI and configured as f_{HCLK} = 48MHZ, f_{APB1} = f_{HCLK}/ 2, f_{APB2} = f_{HCLK}, based on T_A = 25°C and V_{DD} = 3.3V measured value.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 21. The MCU is placed under the following conditions:

- all I/O pins are in analog input mode, and are connected to a static level — V_{DD} or V_{SS} (no load)
- all peripherals are disabled except when explicitly mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked OFF
  - with only one peripheral clocked on
- ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 17

Table 21. Peripheral current consumption

Peripheral	**Typical current consumption**	**Unit**
	V_{DD} = 3.0V, T_A = 25°C	
GPIOA	0.26	mA
GPIOB	1.0	
GPIOD	0.14	
UART1	0.45	
USB	1.9	
I2C	0.71	

7.6.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of General operating conditions.

Table 22. High-speed external user clock characteristics

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			

nS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	uA

Table 23. RF module high speed crystal clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{NOM}	Nominal frequency			16		MHz
V_{TOL}	Frequency tolerance	Load capacitance, temperature			±50	ppm
ESR	Equivalent series				100	Ω
PD	Drive level				20	mA

1. Guaranteed by design, not tested in production.

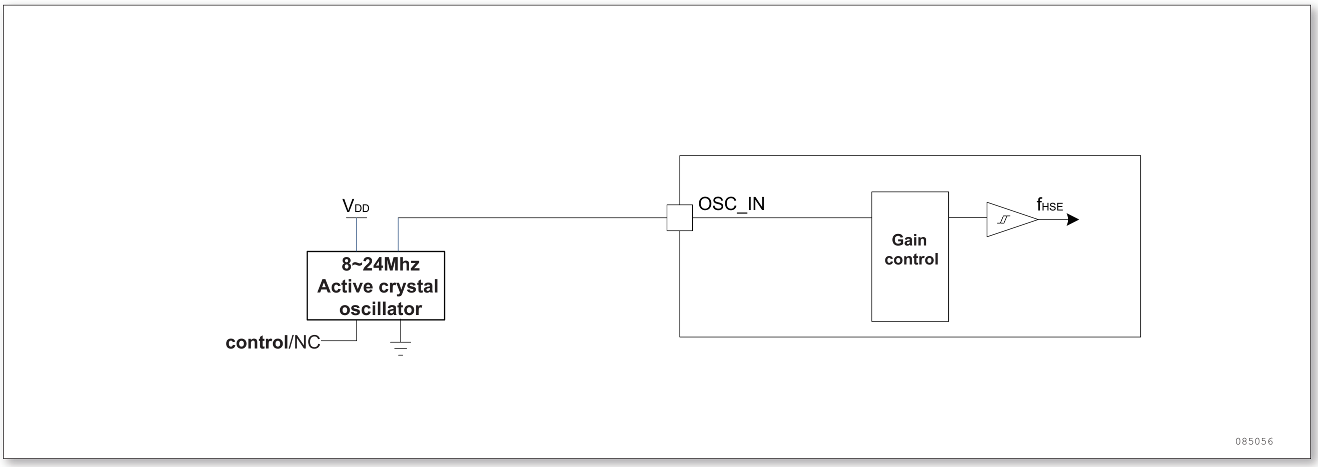

Figure 12. Typical application of the control module using 8 ~ 24MHz crystal

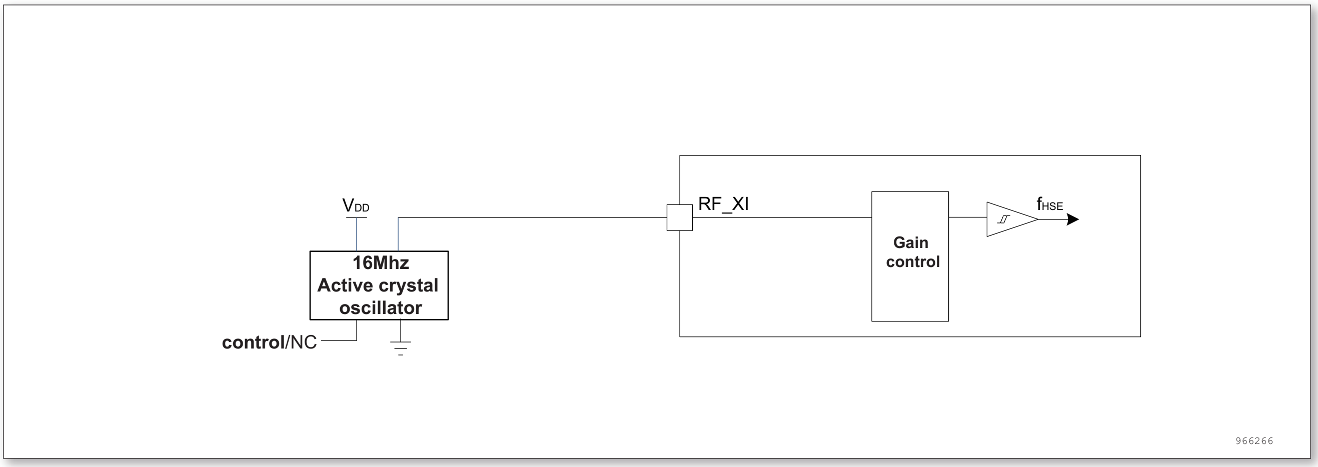

Figure 13. Typical application of RF modules using 16MHz crystals

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 24. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	振荡器频率			16		MHz
R_F	反馈电阻	R_S = 30Ω		1000		kΩ
C_{L1} C_{L2} (3)	建议的负载电容与对应的晶体串行阻抗 (R_S)(4)	V_{DD} = 3.3V V_{IN} = V_{SS} 30pF 负载		30		pF
I_2	HSE 驱动电流	启动			1	mA
g_m	振荡器的跨导	V_{DD} 是稳定的	25			mA/V
$t_{SU(HSE)}$ (5)	启动时间	R_S = 30Ω		2		mS

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer characteristics Parameter.
2. Guaranteed by design, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.) , designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistance can be used to avoid problems arising from the use of wet conditions to provide protection, this environment resulting in leakage and bias conditions have changed. However, if the MCU is applied in bad wet conditions, the design needs to take this parameter into account.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

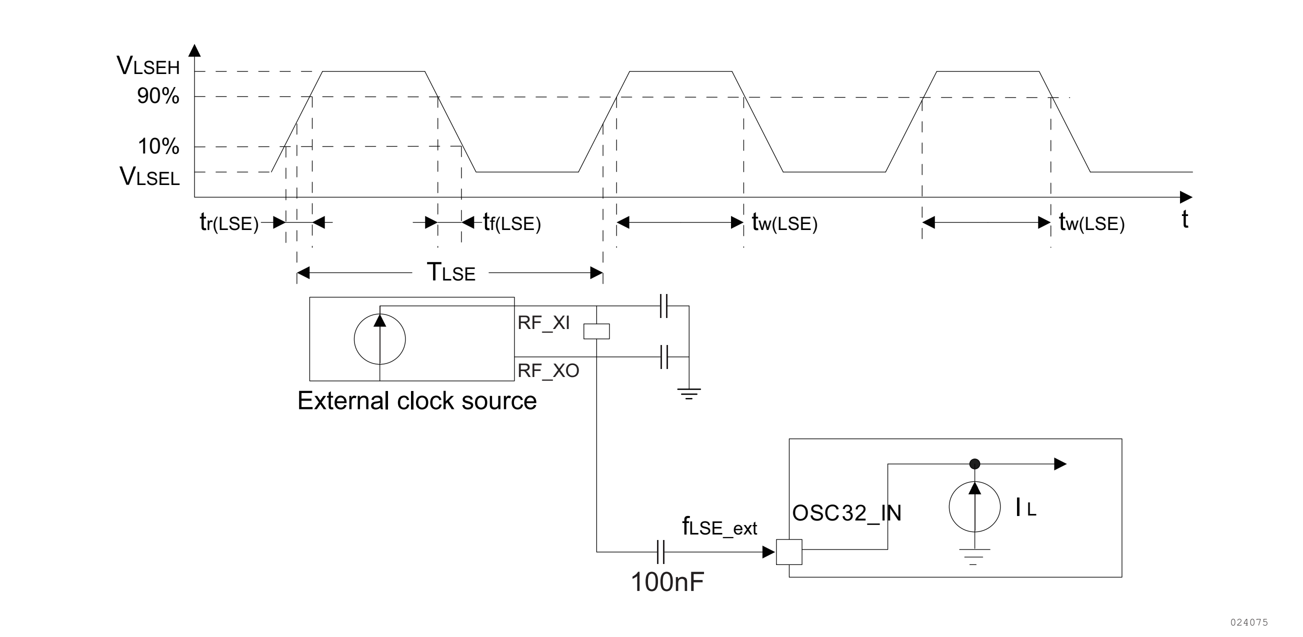

Figure 14. AC timing diagram for external high speed clock source

注：1. The AC timing diagram of the external high-speed clock source indicates that the control module and the RF module share a 16MHz crystal/ceramic resonator. The 16MHz crystal/ceramic resonator mainly provides a high-speed clock for the RF module, and also a series of 100nF capacitors to provide high speed for the control module. clock.

2. If the user uses the internal clock source of the control module, the 16MHz crystal/ceramic resonator alone provides the RF module with a clock.

7.6.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 25. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency		39.94	48.26	64.14	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40°C ~ 105°C	-10		9	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -10°C ~ 85°C				%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 0°C ~ 70°C				%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time				2	μS
$I_{DD(HSI)}$	HSI oscillator power consumption			80.53	122	μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 26. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI} (2)	Frequency		31.3	50.58	74.83	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time				1	µS
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption			1.082	1.652	µA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, Unless otherwise stated
2. Comprehensive assessment, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$ (1)	Wakeup from Sleep mode	HSI clock wakeup	4	µS
t_{WUSTOP} (1)	Wakeup from Stop mode (The regulator is in run mode)	HSI clock wakeup = 2µS	8	
$t_{WUSTDBY}$ (1)	Wakeup from Standby mode	HSI clock wakeup = 2µS The regulator wakes up from the off mode = 38µS	20	mS

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

7.6.7 PLL characteristics

The parameters listed in the table below are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 28. PLL characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	8		24	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	40		100	MHz
t_{LOCK}	PLL lock time			100	μS

1. Guaranteed by design, not tested in production.
2. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.

7.6.8 Memory characteristics

Flash memory

The characteristics are given at T_A = - 40°C ~ 105°Cunless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	8-bit programming time	T_A = -40°C ~ 125°C	4			μS
t_{ERASE}	Page (512K bytes) erase time	T_A = -40°C ~ 125°C		4	5	mS
t_{ME}	Mass erase time	T_A = -40°C ~ 125°C	20		40	mS
I_{DD}	Supply current	Read mode, f_{HCLK} = 48MHz		5	6	mA
		Write mode,f_{HCLK} = 48MHz			7	mA
		Erase mode, f_{HCLK} = 48MHz			2	mA
I_{SB}	Standby current			1@25°C	50@125°C	μA
I_{DEP}	Deep Standby current			0.5	15@125°C	μA

Table 30. Flash memory endurance and data retention(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (Annotation: Erase number of times)	T_A = - 40°C ~ 85°C T_A = - 40°C ~ 105°C	10			K cycle
t_{RET}	Data retention	1 K cycle(2) at T_A = 85°C	30			Year
		1 K cycle(1)(2) at T_A = 105°C	10			
		10 K cycle(1)(2) at T_A = 55°C	20			

1. Guaranteed by design, not tested in production.
2. Cycle tests are carried out in the whole temperature range.

7.6.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB：A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table. They are based on the EMS levels and classes defined in application note.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transientvoltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V,T_A=+25°C, f_{HCLK}=48MHz.Conformingto IEC 1000-4-4	

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

7.6.10 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78A IC latch-up standard.

Table 32. ESD characteristics

Symbol	Parameter	Conditions	Max[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25°C, Conforming to JESD22-A114	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = +25°C, Conforming to JESD22-C101	500	
I_{LU}	Latch-up current	T_A = +25°C, Conforming to JESD78A	200	mA

1. Guaranteed by design, not tested in production.

7.6.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 14 are derived from tests.

Table 33. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	3.3V CMOS Port	-0.5		1.1	V
V_{IL}	Low level input voltage	5V CMOS Port	-0.5		1.5	V
V_{IH}	High level input voltage	3.3V CMOS Port	2.08			V
V_{IH}	High level input voltage	5V CMOS Port	3.5			V
V_{hy}	Schmitt trigger hysteresis[1]	3.3V	500	700	800	mV
V_{hy}	Schmitt trigger hysteresis[1]	5V	500	700	800	mV
I_{lkg}	Input leakage current[2]	3.3V			1	µA
I_{lkg}	Input leakage current[2]	5V			1	µA
R_{PU}	Weak pull-up equivalent resistor[3]	3.3V V_{IN} = V_{SS}	30	50	100	kΩ
R_{PU}	Weak pull-up equivalent resistor[3]	5V V_{IN} = V_{SS}	30	50	100	kΩ
R_{PD}	Weak pull-down equivalent resistor[3]	3.3V V_{IN} = V_{DD}	30	50	100	kΩ
R_{PD}	Weak pull-down equivalent resistor[3]	5V V_{IN} = V_{DD}	30	50	100	kΩ
C_{IO}	I/O pin capacitance	3.3V		5		pF
C_{IO}	I/O pin capacitance	5V		5		pF

1. Schmitt Trigger switching hysteresis voltage level.Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (10% order).

All I/Os are CMOS (no software configuration required). Their characteristics cover more than the strict CMOS-technology.

- For V_{IH}：
  - If V_{DD} is between [2.50V~ 3.08V]; use CMOS features.
  - If V_{DD} is between [3.08V~ 3.60V]; include CMOS.
- For V_{IL}：
  - Use CMOS features.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

n the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in 7.5：

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 17. All I/O ports are CMOS compatible.

Table 34. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin,when 8 pins absorb current	CMOS Port,I_{IO} = +8mA 2.7V < V_{DD} < 3.6V		0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin,when 8 pins output current	CMOS Port,I_{IO} = +8mA 2.7V < V_{DD} < 3.6V	$0.8V_{DD}$		V

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(3)	Output low level voltage for an I/O pin,when 8 pins absorb current	I_{IO} = +20mA 2.7V < V_{DD} < 3.6V		0.4	V
V_{OH} (2)(3)	Output high level voltage for an I/O pin,when 8 pins output current	I_{IO} = +20mA 2.7V < V_{DD} < 3.6V	0.8V_{DD}		V
V_{OL} (2)(3)	Output low level voltage for an I/O pin,when 8 pins absorb current	I_{IO} = +6mA 2V < V_{DD} < 2.7V		TBD	V
V_{OH} (2)(3)	Output high level voltage for an I/O pin,when 8 pins output current	I_{IO} = +6mA 2V < V_{DD} < 2.7V	TBD		V

1. The current absorbed by the chip I_{IO} must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O feet and control pins) must not exceed I_{VSS}.
2. The current output I_{IO} of the chip must always follow the absolute maximum rating given in the table, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.
3. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 15 and Table 35, respectively.

Unless otherwise stated, the parameters listed in Table 35 are measured using the ambient temperature and supply voltage in accordance with the condition Table 14.

Table 35. I/O AC characteristics(1)

OSPEEDRy [1:0] value (1)	Symbol	Parameter	Conditions	Min	Max	Unit
01 (50MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30pF, V_{DD} = 2.7V ~ 3.6V		50	MHz
01 (50MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50pF, V_{DD} = 2.7V ~ 3.6V		30	MHz
			C_L = 50pF, V_{DD} = 2V ~ 2.7V		20	

OSPEEDRy [1:0] value (1)	Symbol	Parameter	Conditions	Min	Max	Unit
	$t_{f(IO)out}$	Output fall time	C_L = 30pF, V_{DD} = 2.7V ~ 3.6V		5	nS
			C_L = 50pF, V_{DD} = 2.7V ~ 3.6V		8	
01 (50MHz)	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 2.7V		12	nS
01 (50MHz)	$t_{r(IO)out}$	Output rise time	C_L = 30pF, V_{DD} = 2.7V ~ 3.6V		5	nS
01 (50MHz)	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2.7V ~ 3.6V		8	nS
01 (50MHz)	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2V ~ 2.7V		12	nS
10 (20MHz)	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50pF, V_{DD} = 2V ~ 3.6V		20	MHz
	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 3.6V		25(3)	nS
	$t_{r(IO)out}$	Output rise time			25(3)	
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		nS

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.
2. The maximum frequency is defined in figure 15.
3. Guaranteed by design, not tested in production.

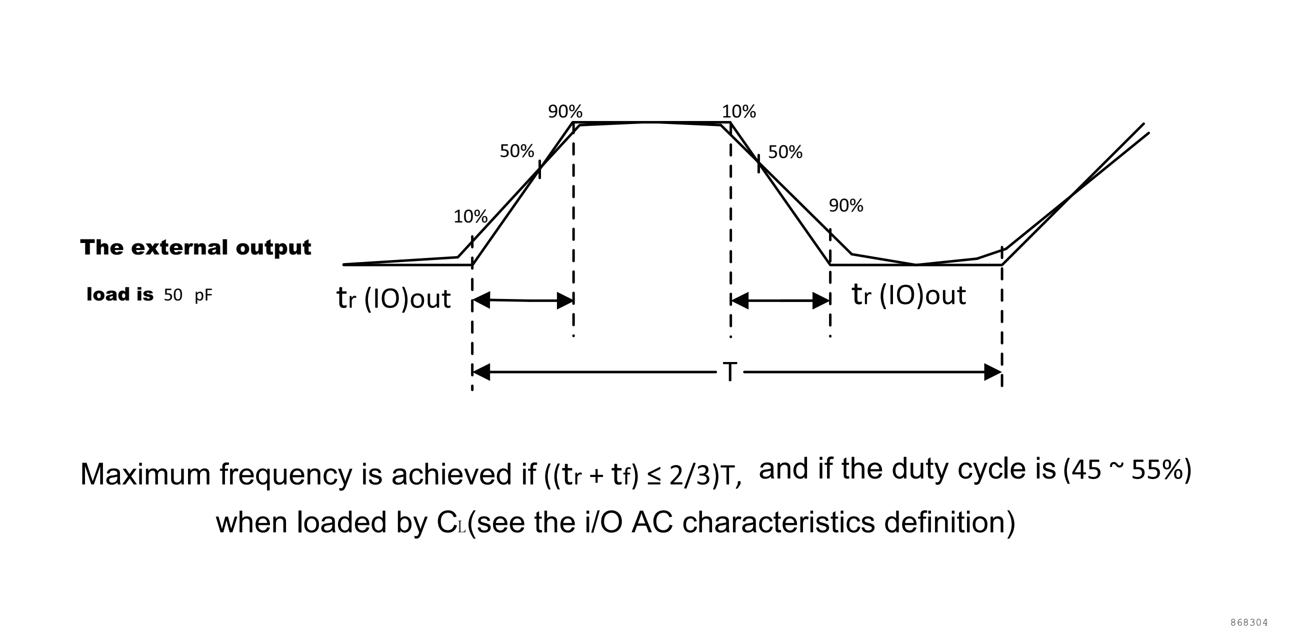

Figure 15. I/O AC characteristics

7.6.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 17.

Table 36. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		2		V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			$0.2V_{DD}$		V
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$		15		kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse				100	ns
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse		300			

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (10% order).

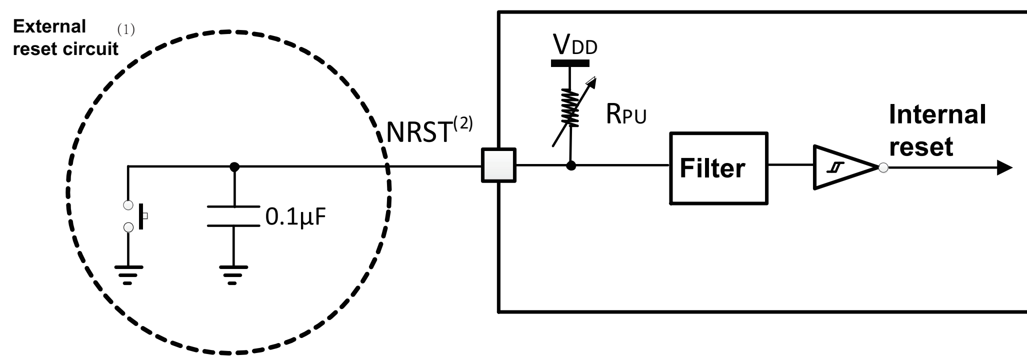

Figure 16. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 36, otherwise the MCU cannot be reset.

7.6.13 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 7.6.11.

Table 37. TIMx[1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 48MHz	10.4		nS
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16-bit timer maximum period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0104	682	μS
t_{MAX_COUNT}	The maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		44.7	S

1. TIMx is a generic name, representing TIM1,2,3,14,16,17.

7.6.14 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 38 are derived from tests performed under the ambient temperature, f_{PCLK1}frequency and supply voltage conditions summarized in Table 17: General operating conditions.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} Was closed but still exists.

The I2C I/Os characteristics are listed in Table 38, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 7.6.11.

Table 38. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock fall time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock rise time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition	4.7		1.3		
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1}must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300nS.

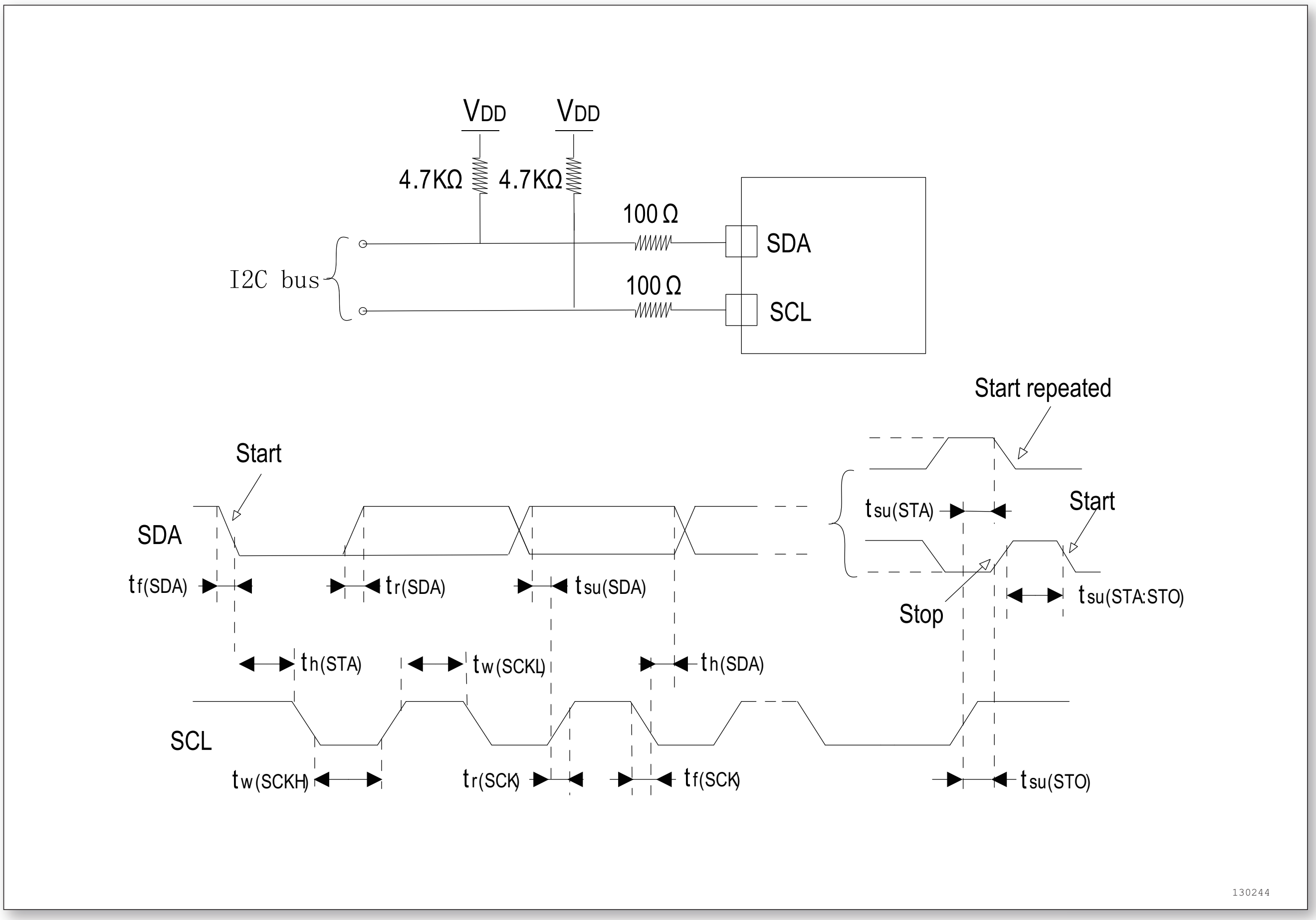

Figure 17. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 39 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 17.

Refer to subsubsec 7.6.11 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 39. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4t_{PCLK}$		
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	73		

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time, Master mode	SPI1	1		ns
$t_{su(SI)}$ (2)	Data input setup time, Slave mode		1		
$t_{h(MI)}$ (2)	Data input hold time, Master mode	SPI1	1		
$t_{h(SI)}$ (2)	Data input hold time, Slave mode		3		
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$ (2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$ (2)		Master mode (after enable edge)	4		

1. Remapping SPI1 characteristics needs to be further determined.
2. Data based on characterization results. Not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

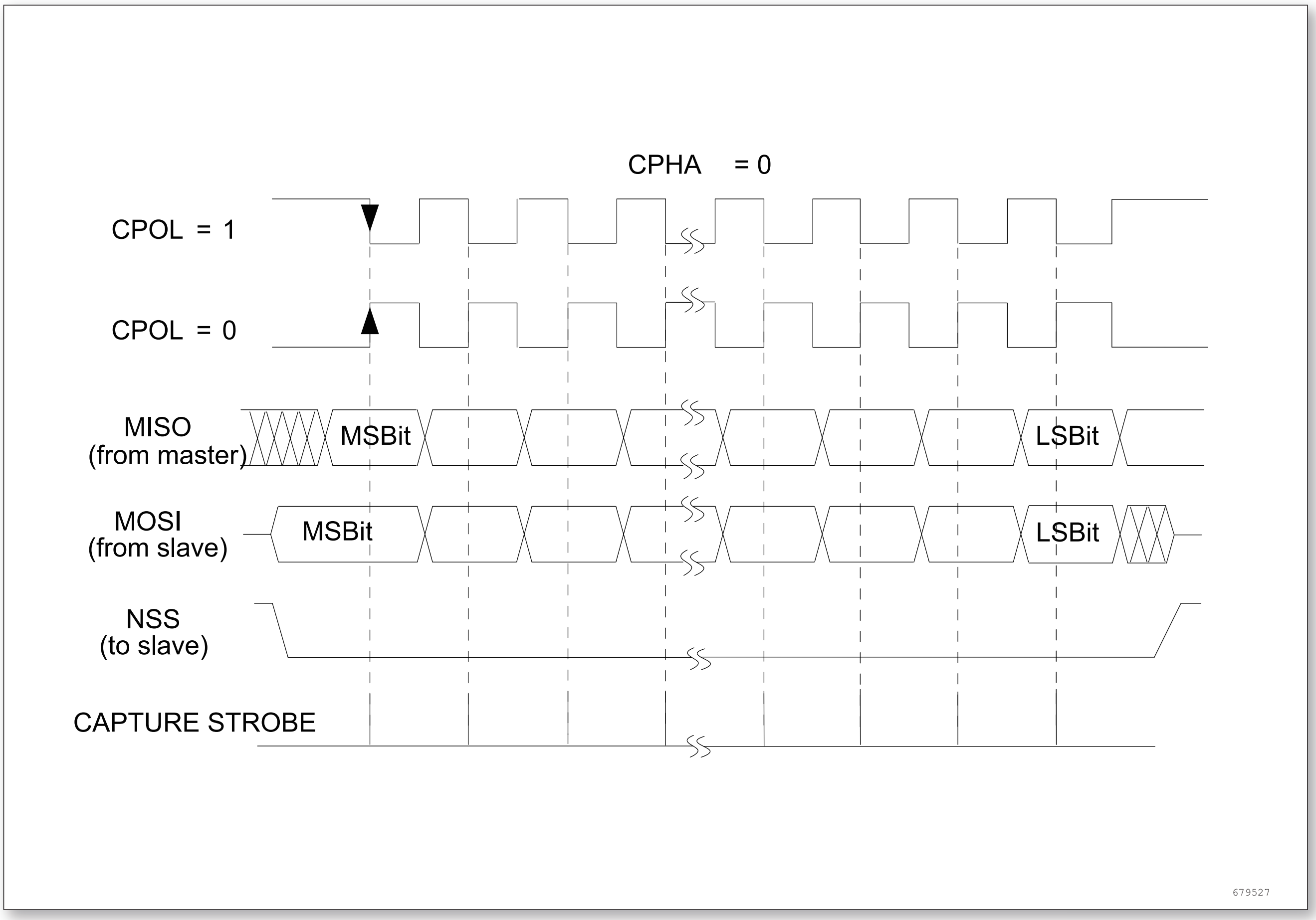

Figure 18. SPI timing diagram-slave mode and CPHA = 0

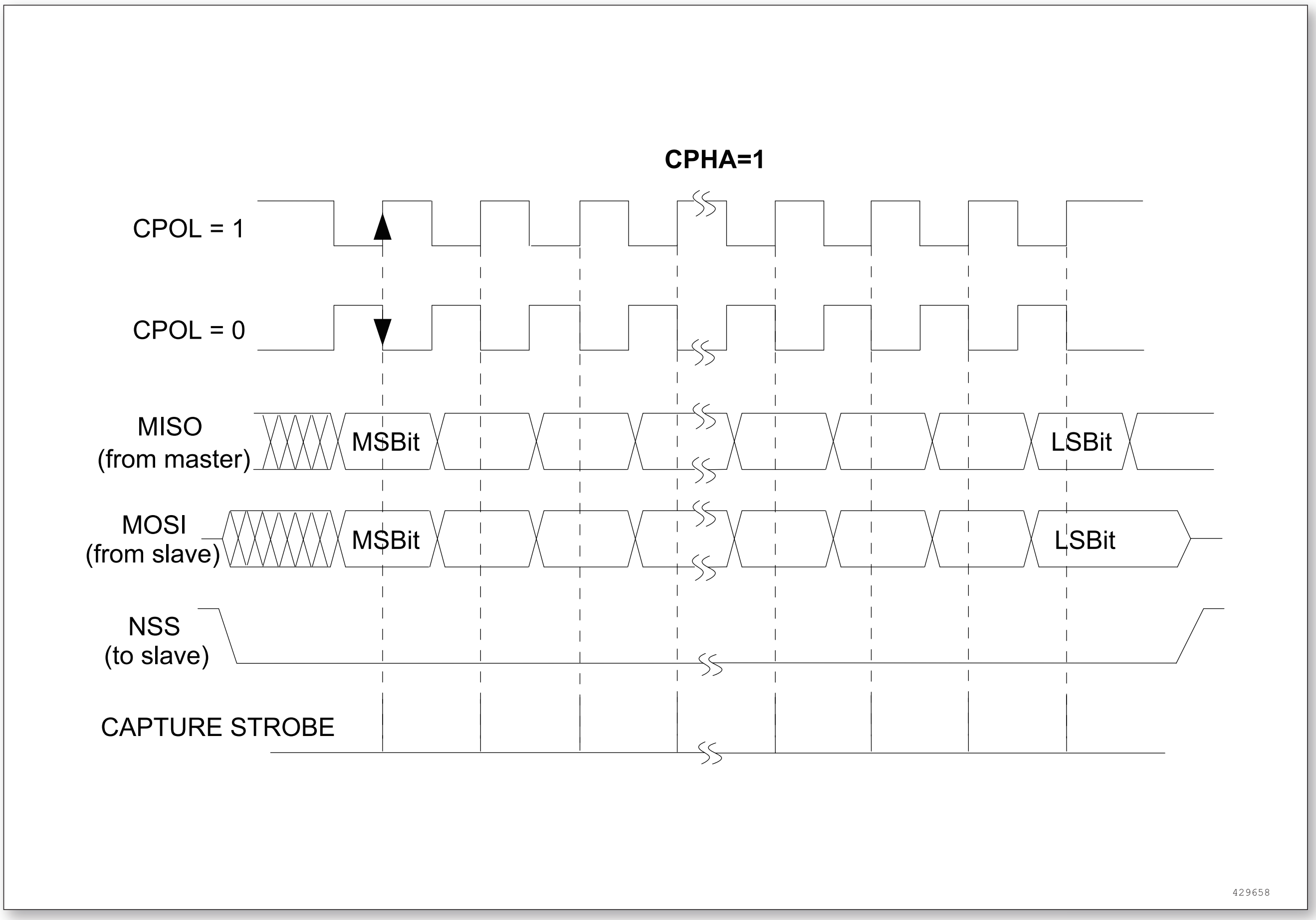

Figure 19. SPI timing diagram-slave mode and CPHA = 1[1]

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

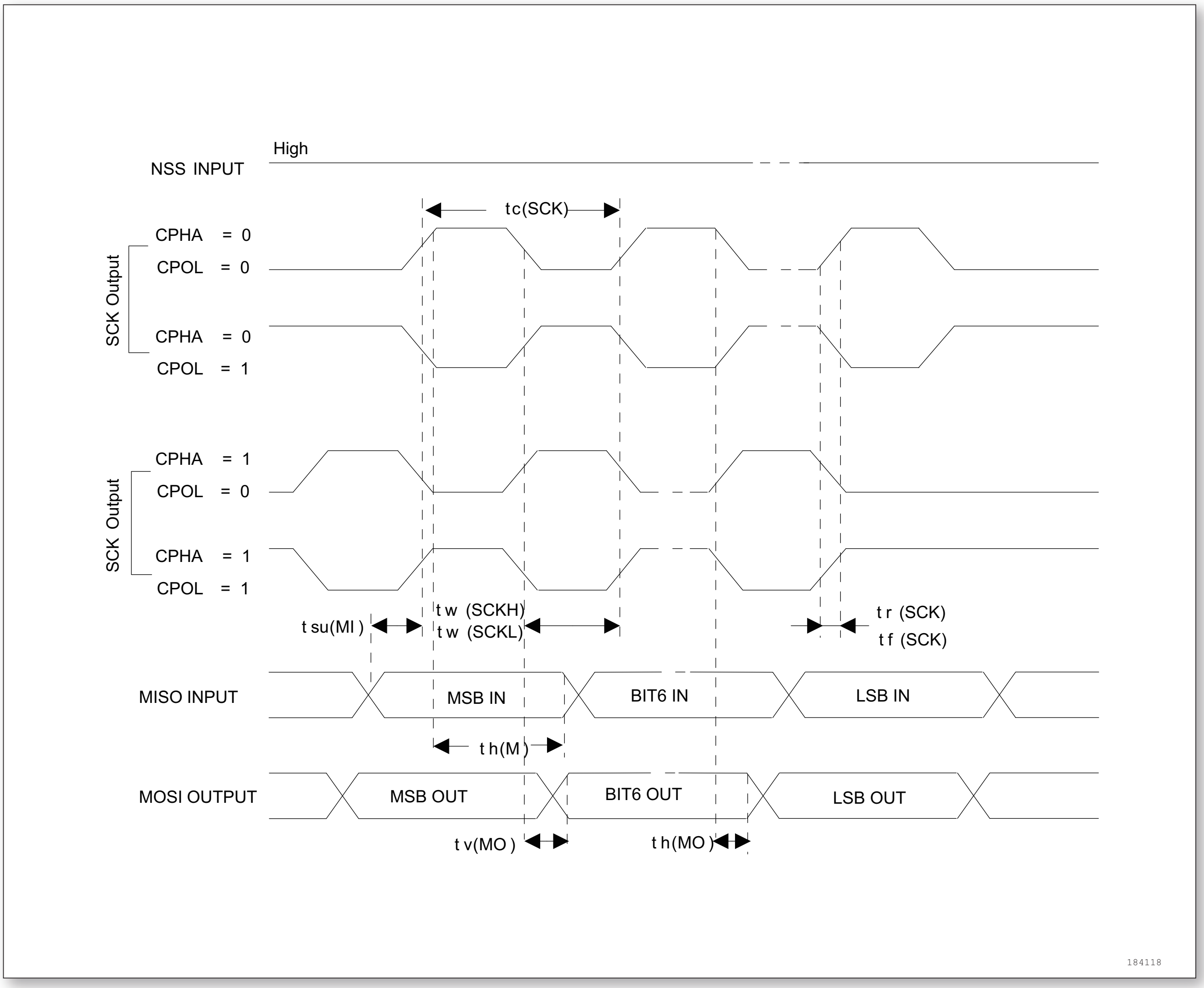

Figure 20. SPI timing diagram-master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

Table 40. USB startup time

Symbol	Parameter	Max	Unit
t_{START}(1)	USB transceiver startup time	1	µs

1. Guaranteed by design. Not tested in production.

Table 41. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)		3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP，USBDM)	0.2		V

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold		1.3	2	
Output levels					
V_{OL}	Static output level low	R_L of 1.5kΩ to 3.6V(5)		0.3	V
V_{OH}	Static output level high	R_L of 15kΩ to V_{SS} (5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, USBDP (D +) pin has a built-in 1.5kΩ resistor connected to the V_{DD}, no need to external connect.
3. The USB functionality is ensured down to 2.7V but not the full USB electrical characteristics which are degraded in the 2.7V ~ 3.6V V_{DD} voltage range.
4. Guaranteed by design. Not tested in production.
5. R_L is the load connected on the USB drivers

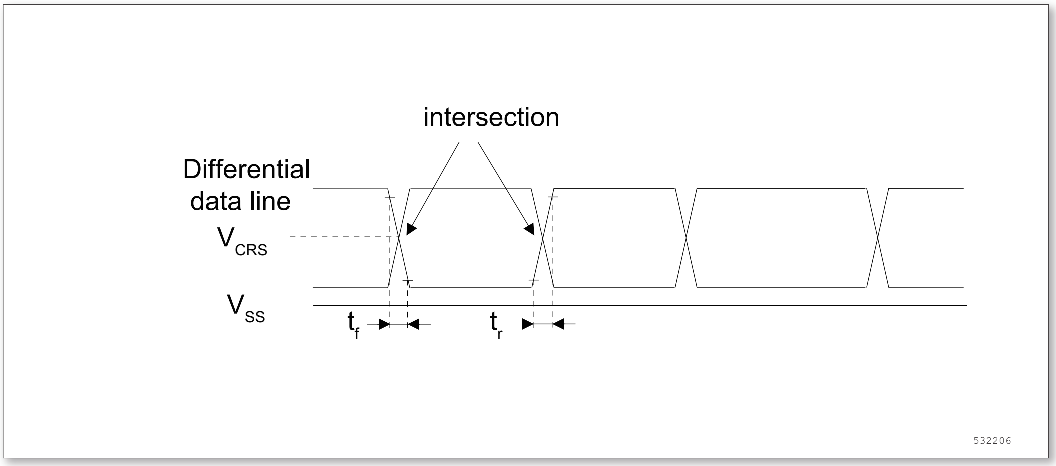

Figure 21. USB timing diagram: definition of data signal rise and fall time

Table 42. USB Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time(2)	C_L <= 50pF	7.041	23.13	ns
t_f	Fall time(2)	C_L <= 50pF	6.866	26.76	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	96.52	125.1	%
V_{CRS}	Output signal crossover voltage		1.391	2.967	V

1. Guaranteed by design. Not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification - Section 7 (version 2.0).

7.6.15 CAN (controller area network) interface

Refer to subsubsec 7.6.11 for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7.6.16 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 17.

Note: It is recommended to perform a calibration after each power-up

Table 43. ADC characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2	5	5.5	V
V_{REF+}	Positive reference voltage			V_{DDA}		V
$f_{ADC}{}^{(1)(3)}$	ADC clock frequency				15	MHz
$f_S{}^{(1)(3)}$	Sampling rate				1	MHz
$f_{TRIG}{}^{(1)}$	External trigger frequency	f_{ADC} = 15MHz				KHz
						$1/f_{ADC}$
$V_{AIN}{}^{(2)}$	Conversion voltage range		0 (V_{SSA} or V_{REF-} connected to ground)		V_{REF+}	V
$R_{AIN}{}^{(1)}$	External sample and hold capactor		See Formulas 1 and Table 44			kΩ
$R_{ADC}{}^{(1)}$	Sampling switch resistance				1	kΩ
$C_{ADC}{}^{(1)}$	Internal sample and hold capacitor			10		pF
$t_S{}^{(1)}$	Sampling time	f_{ADC} = 15MHz	0.1		16	μs
			1.5		239.5	$1/f_{ADC}$
$t_{STAB}{}^{(1)}$	Stabilization time			1		μs
$t_{conv}{}^{(1)}$	Total conversion time (including Sampling time)	f_{ADC} = 15MHz	1		16.9	μs
			15 ~ 253 (sampling t_{S+}) stepwise approximation 13.5			$1/f_{ADC}$

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. In this series of products, V_{REF+} is internally connected to $_{DDA}$, V_{REF-} is internally connected to $_{SSA}$.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times In(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution) .

Table 44. Maximum R_{AIN} at f_{ADC} = 15MHz[1]

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)
1.5	0.1	1.2
7.5	0.5	10
13.5	0.9	19
28.5	1.9	41
41.5	2.76	60
55.5	3.7	80
71.5	4.77	104
239.5	16.0	350

1. Guaranteed by design. Not tested in production.

Table 45. ADC Accuracy - Limit Test Conditions[1][2]

Symbol	Parameter	Test Conditions	Type	Max[3]	Unit
ET	Comprehensive error	f_{PCLK2} = 60MHz,f_{ADC} = 15MHz,R_{AIN} < 10KΩ,V_{DDA} = 5V，T_A = 25°C	±11	±12	LSB
EO	Offset error		±8	±9	
EG	Gain error		±7.5	±9	
ED	Differential linearity error		±3	±3	
EL	Integral linearity error		±11	±11	

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in subsubsec 7.6.12 does not affect the ADC accuracy.
2. Guaranteed based on test during characterization. Not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

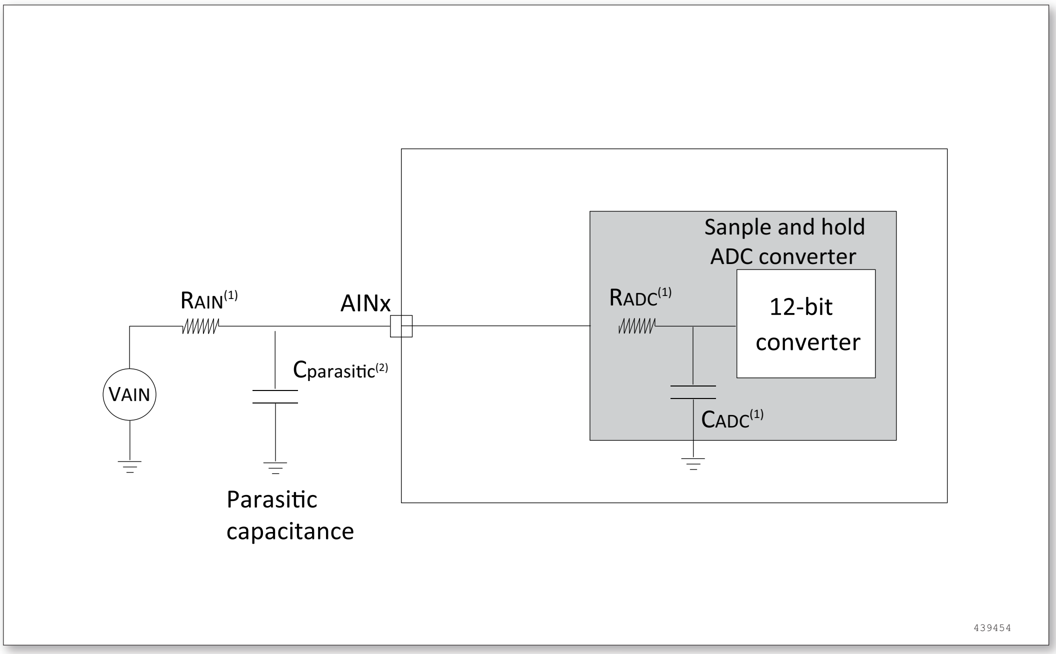

Figure 22. Typical connection diagram using the ADC

1. See Table 45 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nFcapacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

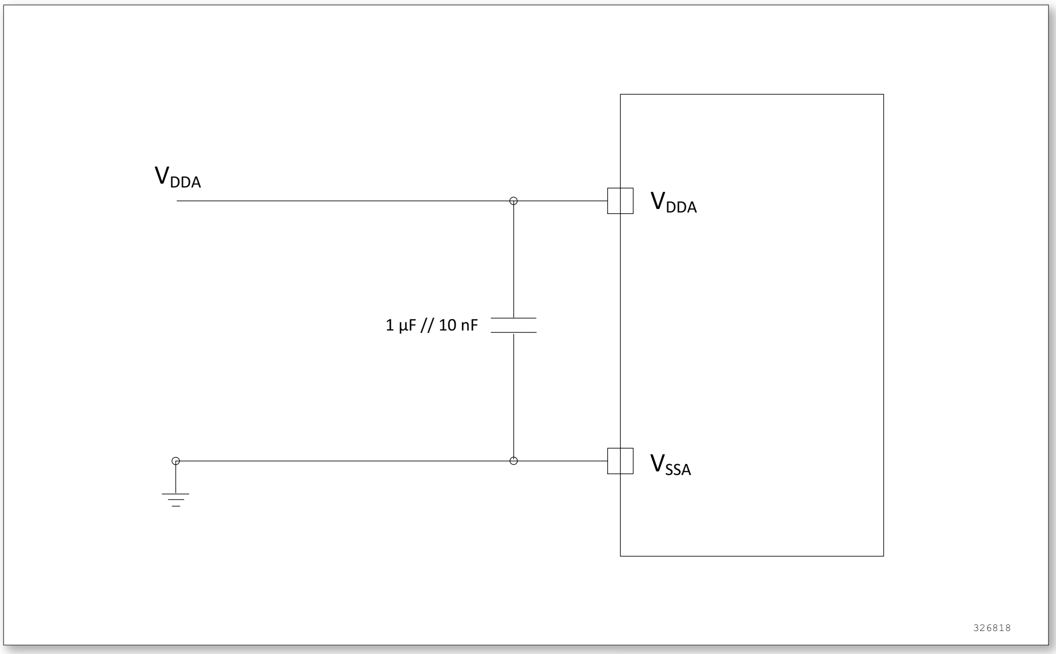

Figure 23. Power supply and reference power supply decoupling circuit

7.6.17 Temperature sensor characteristics

Table 46. Temperature sensor characteristics(3) (4)

Symbol	Parameter	Min	Type	Max	Unit
T_L (1)	V_{SENSE} linearity with respect to temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25} (1)	Voltage at 25°C	1.433	1.451	1.467	V
t_{start} (2)	Setup time			10	µs
T_{S_temp} (2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. The shortest Sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

7.6.18 Comparator characteristics

Table 47. Comparator characteristics

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	00		0		mV
		01		15		mV
		10		30		mV

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
		11		90		mV
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
		01	3.23	7.51	12.08	mV
		10	9.79	15	20.8	mV
		11	34.25	47.4	62.22	mV
DELAY(1)	Propagation delay	00		80		nS
		01		51		nS
		10		26		nS
		11		9		nS
I_q(2)	Operating current mean	00		4.5		uA
		01		4.4		uA
		10		4.4		uA
		11		4.4		uA

1. The output flips 50% of the time and the time difference between the input and the flip.
2. Total current consumption, operating current.

8 PCB design recommendations

PCB design recommendations

8.1 Power supply design recommendations

The power supply must be connected as shown below. The 10nF capacitors in the figure must be ceramic dielectric capacitors (good quality) and they should be as close as possible to the MCU chip.

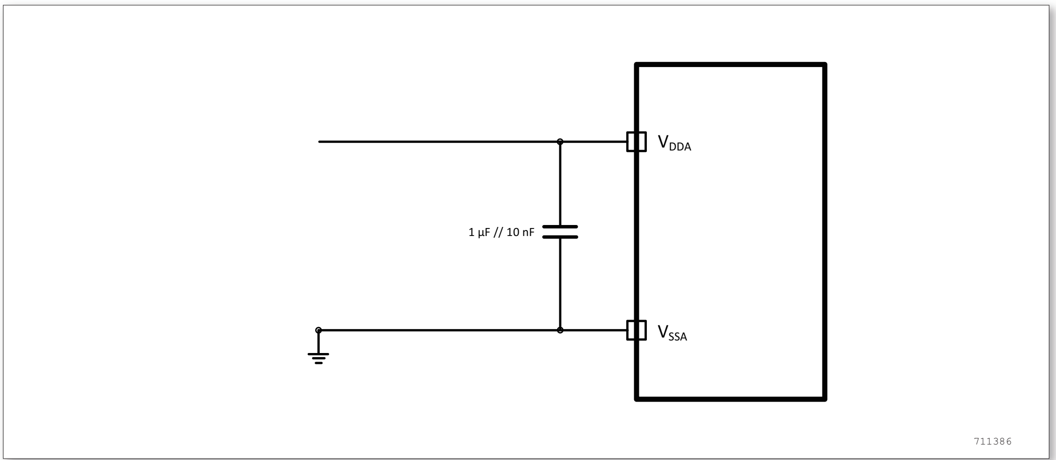

Figure 24. Power supply and reference power supply

8.2 PCB considerations

Bluetooth works in the 2.4G wireless frequency band, and should avoid the influence of various factors on the wireless transceiver. Pay attention to the following points:

- The product enclosure surrounding the Bluetooth module avoids the use of metal. When using a part of the metal casing, try to keep the module antenna part away from the metal part.
- The internal metal wire or metal screw of the product should be as far as possible from the antenna part of the module.
- The antenna part of the module should be placed around the carrier PCB. It is not allowed to be placed in the board, and the carrier board under the antenna is slotted. In the direction parallel to the antenna, copper or wiring is not allowed. It is also a good choice to directly expose the antenna part directly to the carrier board.
- Place a large GND under the module as far as possible, and extend the trace as far as possible to the outside.
- It is recommended to use insulating materials for isolation at the module mounting posi-

tion on the substrate, for example by placing a single screen print (TopOverLay) at this position.

- The wiring of the power supply line and ground line is directly related to the performance of the product, and the noise interference is minimized. When wiring, try to widen the ground wire, power cable width, ground wire > power wire > signal wire, usually the signal line width is 0.2 0.3mm, the power line width is 1.2 2.5mm, and the large-area copper layer is used for grounding. The unused space on the PCB is paved.
- Power supply plus two decoupling filter capacitors: If using LDO power supply, the values are 1uF and 0.1uF respectively for filtering; if using button battery power, the values are 10uF and 10uF respectively for voltage regulation.
- The trace between the chip ANT and the antenna should not be too long. The line width should consider the impedance matching requirements.

8.3 2.4G RF antenna design

Small antenna sizes can cause large changes due to performance. Therefore, it is highly recommended to make an accurate reference design for optimum performance. When drawing a PCB antenna, draw the antenna with reference to the dimensions given in the figure below.

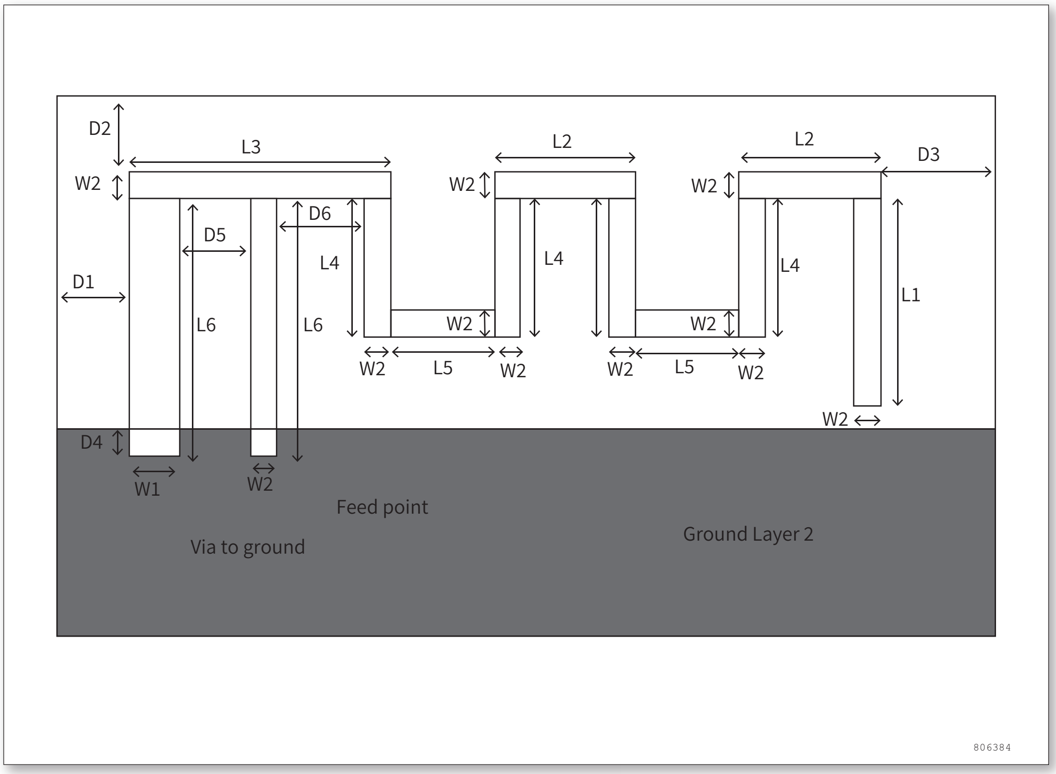

Figure 25. Antenna size

Table 48. Antenna size

No.	Typical value(mm)
L1	3.94
L2	2.70

No.	Typical value(mm)
L3	5.00
L4	2.64
L5	2.00
L6	4.90
W1	0.90
W2	0.50
D1	0.50
D2	0.30
D3	0.30
D4	0.50
D5	1.40
D6	1.70

9 Package information

Package information

9.1 LQFP48 Package information

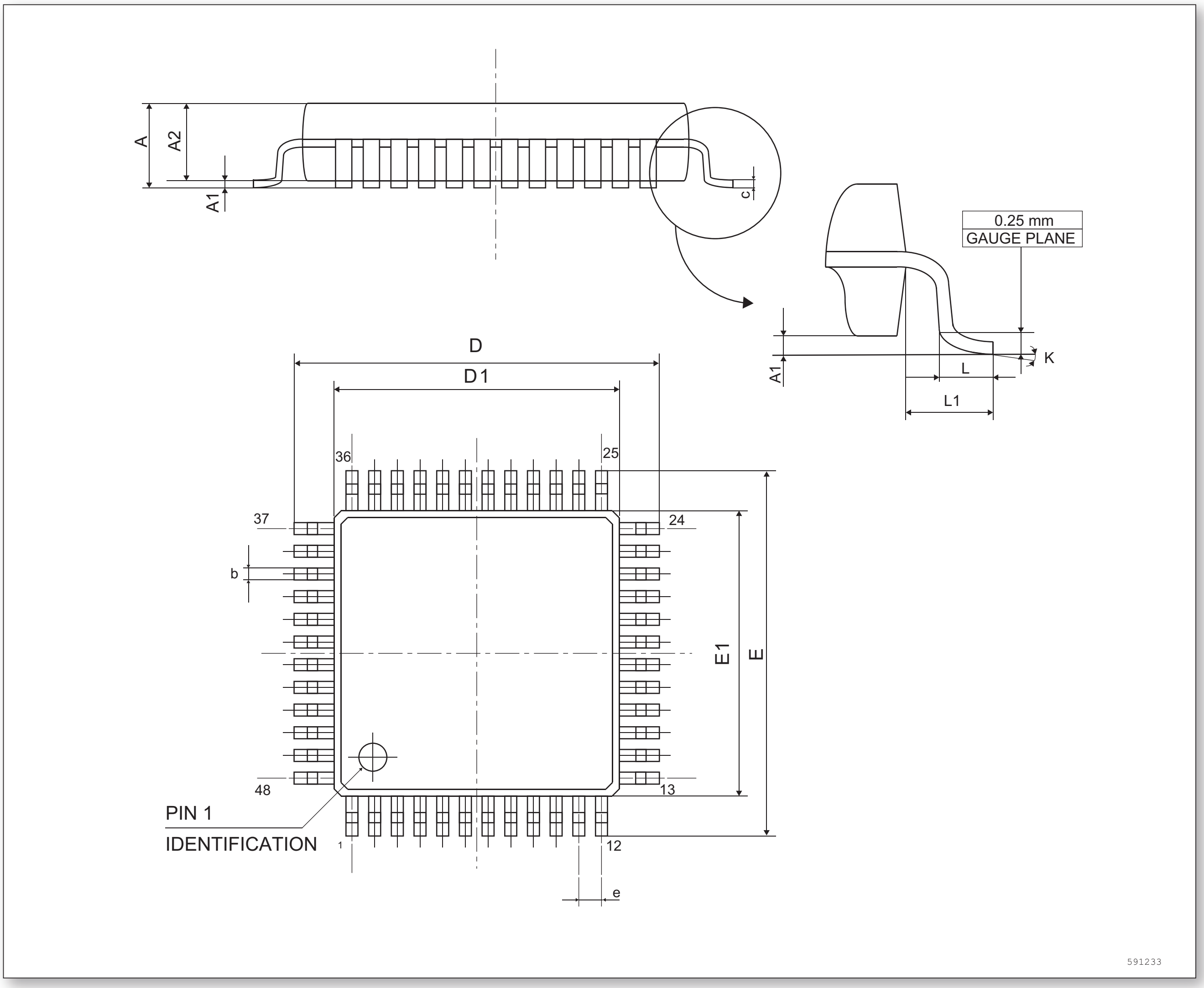

Figure 26. LQFP48 - 48-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 49. LQFP48 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09		0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	6.10
e		0.5	
K	0°	3.5°	7°
L	0.45	0.60	0.65
L1		1.00	
N	Number of pins = 48		

9.2 QFN32 Package information

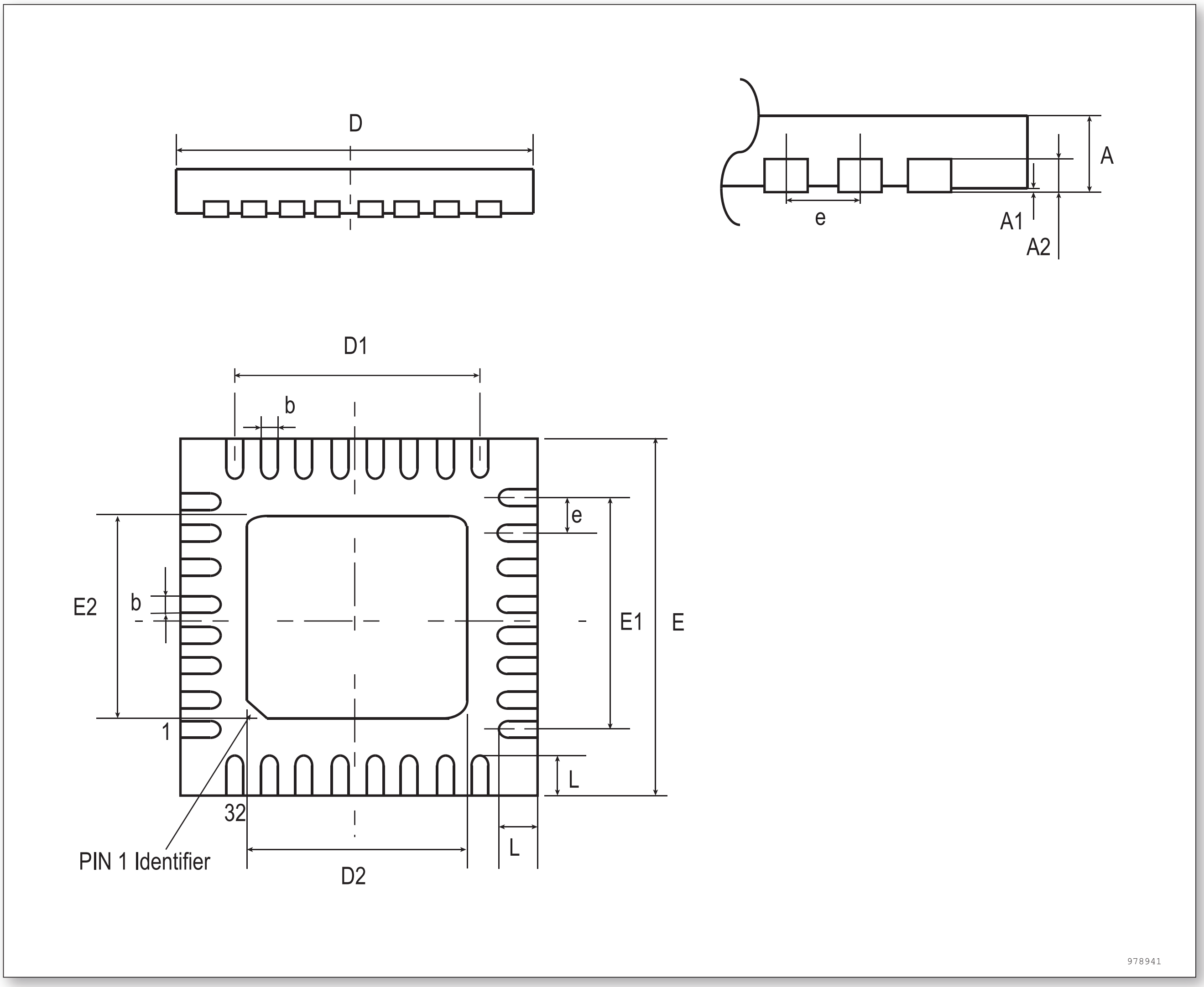

Figure 27. QFN32 - 32-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 50. QFN32 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.80
A1	0.00	0.035	0.05
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D1		3.50	
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E1		3.50	

Symbol	Millimeters		
	Min	**Typ**	**Max**
E2	3.40	3.50	3.60
e		0.5	
L	0.30	0.40	0.50
N	Number of pins = 32		

10 Ordering information

Ordering information

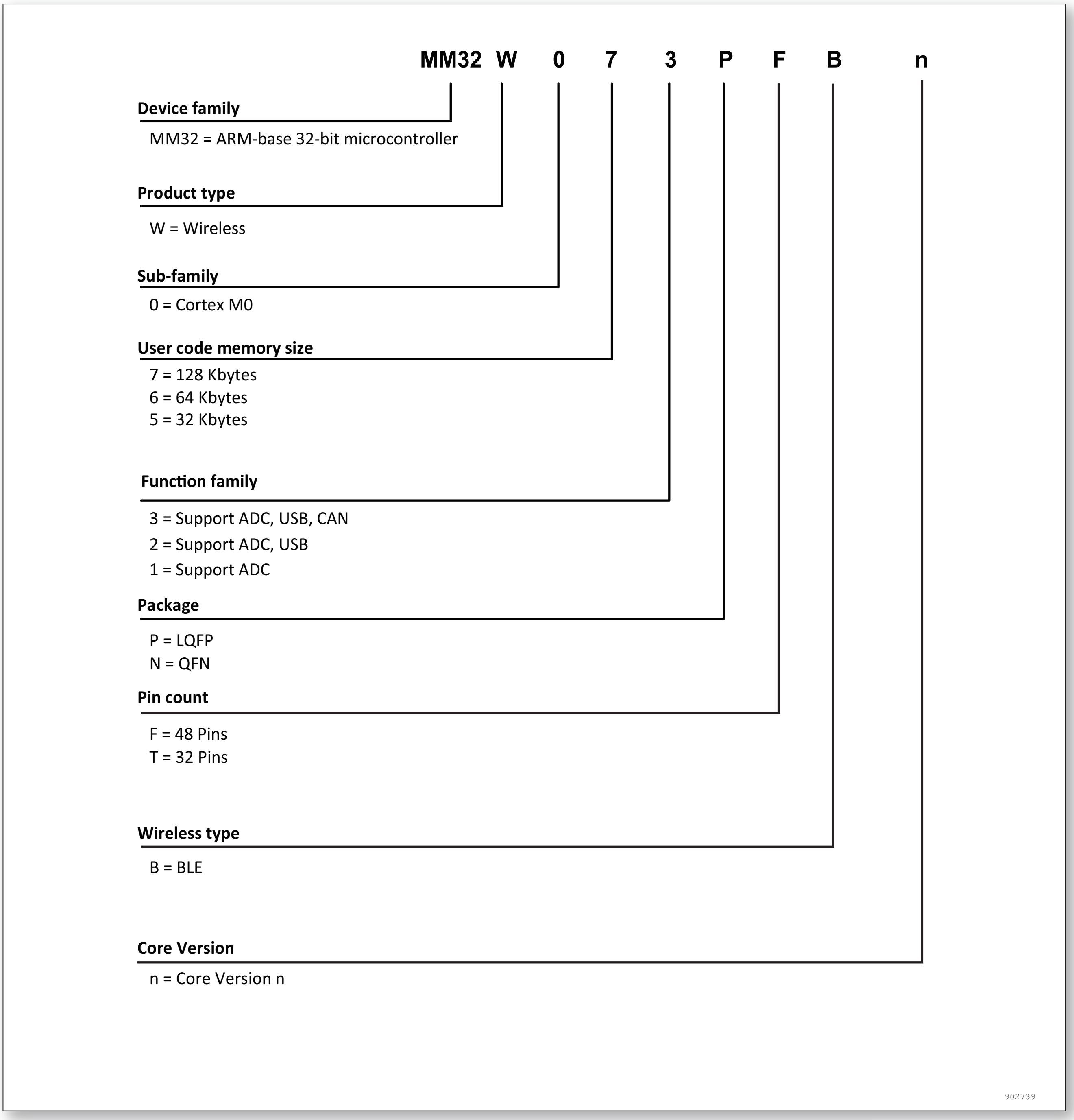

Figure 28. Ordering information scheme

Onyx Components & Systems (P) Ltd.,6-1-85/4,Saifabad,Hyderabad-500004,Ph:040-23237230/Fax:040-66631800,Email:onyx@onyxindia.com

11 Revision history

Revision history

Table 51. Document revision history

Revision	Changes	Date
Rev1.0	Initial release.	2017/5/31
Rev1.1	Modify the working voltage and clock map.	2017/6/13
Rev1.2	Modify the typical application circuit diagram.	2017/6/21
Rev1.7	Revise the capacitance value of the matching crystal in the application circuit diagram and the capacitance value in the reset circuit, and the power consumption parameters of Table 10.	2018/2/23
Rev1.8	Change parameters	2018/12/3
Rev1.9	Modify ADC electrical parameters.	2019/1/7