Datasheet

MM32F013x

32-Bit Microcontroller Based on ARM® Cortex® M0

Version: 1.00

Content

List of Figures

List of Tables

1 General Introduction

General Introduction

1.1 Introduction

This product is a 32-bit microcontroller using the high-performance ARM® Cortex®-M0 as the kernel. The highest operating frequency is up to 72MHz. It has built-in high speed memory, rich enhanced I/O ports and peripherals which are connected to the external bus. 1 x 12-bit ADC, 2 x Comparators, 1 x 16-bit universal timer, 1 x 32-bit universal timer, 3 x 16-bit basic timers, 1 x 16-bit advanced timer, It also contains standard communication interfaces: 1 x I2C, 2 x SPIs, 1 x USB, 1 x CAN, and 2 x UARTs.

The operating voltage of this product series is 2.0V ~ 5.5V. The operating temperature range of conventional type is -40°C ~ +85°C. Multiple power-down modes are provided to ensure the requirements of low-power applications.

The product is available for four types of packages: LQFP64, LQFP48, LQFP32 and QFN32.

The configuration of peripherals for the product varies according to different packages.

Rich peripherals make the microcontroller suitable for a variety of applications:

- Motor drive and application control
- Medical and handheld devices
- PC game peripherals and GPS platforms
- Industrial applications: programmable logic controllers (PLC), frequency converters, printers and scanners
- Alarm systems, video intercom systems, heating, ventilation and air conditioning systems

1.2 Product Characteristics

- Kernel and system
  - 32-bit ARM® Cortex®-M0 processor as the kernel
  - Highest operating frequency up to 72MHz
- Memory
  - 64K Bytes of Flash memory
  - 16K Bytes of SRAM
  - Boot loader supports embedded flash and UART In Application Programming (IAP)/In System Programming (ISP)

- Clock, reset and power management
  - Power supply 2.0V ~ 5.5V
  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
  - POR reset voltage is as low as 1.7V
  - PVD voltage threshold can be as low as 1.8V
  - External 8 ~ 24MHz high speed crystal oscillator
  - Embedded 48 MHZ high speed oscillator with factory calibration
  - Embedded 40KHz low speed oscillator
  - PLL supports CPU running up to 72MHz
  - External 32.768K low speed oscillator
- Low power consumption
  - Sleep, Stop and Standby modes
- 1 x 12-bit ADC, 1μS A/D converters (up to 10 channels)
  - Conversion range: 0 ~ V_{DDA}
  - Support the configuration of sampling time and resolution
  - On-chip temperature sensor
  - On-chip voltage sensor
- 2 x Comparators
- 5 x Channel DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI, USB and ADC
- Up to 56 fast I/Os:
  - All mappable on 16 external interrupt vectors
- Debug mode
  - Serial wire debug (SWD)
- Up to 9 timers
  - One 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead zone generation and emergency stop functions
  - One 16-bit timer and one 32-bit timer providing up to 4 input captures/output comparisons, which can be used for IR control decoding
  - Two 16-bit timers providing 1 input capture/output comparison and 1 OCN, with functions of dead zone generation, emergency stop and modulator gate circuit for IR control
  - One 16-bit timer providing 1 input capture/output comparison
  - Two watchdog timers (independent type and window type)
  - One system time timer: 24-bit downcounter
- Up to 7 Communication interfaces
  - 2 x UARTs
  - 1 x I2C
  - 2 x SPIs
  - 1 x CAN
  - 1 x USB
- 96-bit unique ID (UID)
- Packages LQFP64, LQFP48, LQFP32 and QFN32.

For more information about the complete product, refer to Section 2.2 of this Datasheet. The relevant information about the Cortex®-M0, please refer to *Cortex®-M0 Technical Reference Manual.*

2 Specification

Specification

2.1 Device Comparison

Table 1. MM32F0131 Function and Peripheral Configuration

Peripheral \ Device		MM32F0131C7P	MM32F0131C6P	MM32F0131C4P	MM32F0131C4N
Flash - K Bytes		64	64	64	64
SRAM - K Bytes		16	16	16	16
Timer	Universal (16-bit)	1	1	1	1
	Universal (32-bit)	1	1	1	1
	Basic	3	3	3	3
	Advanced	1	1	1	1
Communication interface	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	2	1	1
GPIO Ports		55	39	25	27
12-bit ADC	Number	1	1	1	1
	Channels	10	10	10	10
Comparator		2			
CPU frequency		72 MHz			
RTC		√			
Operating Voltage		2.0V ~ 5.5V			
Packages		LQFP64	LQFP48	LQFP32	QFN32

Table 2. MM32F0132 Function and Peripheral Configuration

Peripheral \ Device		MM32F0132C7P	MM32F0132C6P	MM32F0132C4P/B4P	MM32F0132C4N/B4N
Flash - K Bytes		64	64	64/32	64/32
SRAM - K Bytes		16	16	16/8	16/8
Timer	Universal (16-bit)	1	1	1	1
	Universal (32-bit)	1	1	1	1
	Basic	3	3	3	3

Peripheral \ Device		MM32F0132C7P	MM32F0132C6P	MM32F0132C4P/B4P	MM32F0132C4N/B4N
Timer	Advanced	1	1	1	1
Communication interface	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	2	1	1
	USB	1	1	1	1
GPIO Ports		56	39	25	27
12-bit ADC	Number	1	1	1	1
	Channels	10	10	10	10
Comparator		2			
CPU frequency		72 MHz			
RTC		√			
Operating Voltage		2.0V ~ 5.5V			
Packages		LQFP64	LQFP48	LQFP32	QFN32

Table 3. MM32F0133 Function and Peripheral Configuration

Peripheral \ Device		MM32F0133C7P	MM32F0133C6P	MM32F0133C4P	MM32F0133C4N
Flash - K Bytes		64	64	64	64
SRAM - K Bytes		16	16	16	16
Timer	Universal (16-bit)	1	1	1	1
	Universal (32-bit)	1	1	1	1
	Basic	3	3	3	3
	Advanced	1	1	1	1
Communication interface	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	2	1	1
	USB	1	1	1	1
	CAN	1	1	1	1
GPIO Ports		56	39	25	27
12-bit ADC	Number	1	1	1	1
	Channels	10	10	10	10
Comparator		2			
CPU frequency		72 MHz			
RTC		√			
Operating Voltage		2.0V ~ 5.5V			
Packages		LQFP64	LQFP48	LQFP32	QFN32

2.2 Introduction

2.2.1 ARM Cortex-M0 as the Kernel with Embedded Flash Memory and SRAM

The ARM® Cortex®-M0 processor is the latest embedded ARM processor. It provides a low-cost platform, reduced pins, decreased system power consumption, superior computing performance and advanced interrupt servicing system to realize the requirements of MCU.

The ARM® Cortex®-M0 is a 32-bit RISC processor that improves the code efficiency and makes full use of the high-performance ARM kernel in the storage space of common 8- and 16-bit systems.

This product has a built-in ARM core, so it is compatible with all ARM tools and software.

2.2.2 Embedded Flash Memory

Embedded flash memory up to 64K bytes for storing programs and data.

2.2.3 Embedded SRAM

Embedded SRAM up to 16K bytes.

2.2.4 CRC (Cyclical Redundancy Check) Computing Unit

The CRC (Cyclic Redundancy check) computing unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. The CRC-based technique is used to verify the consistency of data transfer or storage in its numerous applications.

Within the scope of the EN/IEC60335-1 standard, it provides a method of detecting flash memory errors. CRC computing unit can be used to calculate the software signature in real time and compare it to the signature generated when linking to and generating the software.

2.2.5 Nested Vectored Interrupt Controller (NVIC)

This product has a built-in nested vectored interrupt controller, which can process multiple maskable interrupting channels (excluding 16 Cortex™-M0interrupt lines) and 16 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry address directly enters into the kernel
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher-priority interrupts that arrive late
- Support tail link of interrupts
- Automatically save the processor state

- Offer automatic recovery when the interrupt returns with no additional instruction

This module provides flexible interrupt management with minimal interrupt latency.

2.2.6 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains multiple edge detectors which are used to generate interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge or falling edge or double edge) and can be screened separately. A pending register maintains the states of all interrupt requests.

EXTI can detect clock cycles whose pulse width is smaller than the internal APB2. All universal I/O ports are connected to 16 external interrupt lines.

2.2.7 Clock and Startup

The system clock is selected during startup. The internal 48 MHz oscillator with 6 fractional frequencies is selected as the default CPU clock after reset. Then external 2~24 MHz clocks with failure monitoring function can be selected. When an external clock failure is detected, the clock will be isolated. The system automatically switches to an internal oscillator. If an interrupt is enabled, the software can receive the corresponding interrupt. Similarly, complete interrupt management of the PLL clock can be taken when needed (e.g., when an external indirectly-used oscillator fails to work).

Multiple prescalers are used to configure AHB frequency and high-speed APB(APB2 and APB1) areas. The highest frequency of AHB and high-speed APB is 72MHz. Please refer to the clock drive diagram in figure 2.

2.2.8 Boot Mode

During startup, one of three boot modes can be selected through the boot pin:

- Boot from the Flash memory
- Boot from the System Memory
- Boot from the internal SRAM

Boot loader resides in the system memory. The flash memory can be reprogrammed through UART1.

2.2.9 Scheme of Power Supply

- V_{DD} = 2.0V ~ 5.5V: The VDD pin supplies power to the I/O pins and the internal voltage regulator.
- V_{DD} = 2.5V ~ 5.5V: It supplies power to the ADC, reset module, oscillator, and analog part of PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.

2.2.10 Power Supply Monitor

This product is integrated with power on reset (POR)/power down reset (PDR) circuit. The circuit remains in the working state to ensure the system works when the power supply exceeds 2.0V. When V_{DD} is below the set threshold ($V_{POR/PDR}$), the device will be placed in the reset state. An external reset circuit is not necessary.

Additionally, there is a programmable voltage monitor (PVD) in the device that monitors the V_{DD}/V_{DDA} power supply and compares it to the threshold V_{PVD}. When V_{DD} is below or above the threshold V_{PVD}, the device will be interrupted. The interrupt handler will send a warning message or switch the microcontroller to safe mode. The PVD function should be enabled by a program.

2.2.11 Voltage Regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low-power modes

The product supports a low power mode that provides the best balance among low power requirements, short startup time, and multiple wake-up events.

Sleep mode

In the sleep mode, only the CPU stops working. All peripherals are working and can wake up the CPU in the event of an interrupt/event.

Stop mode

The shutdown mode minimizes the power consumption while keeping the SRAM and register contents intact. In the shutdown mode, the HSI oscillator and HSE crystal oscillator are shut down. The microcontroller can be woken from the shutdown mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Standby mode

The standby mode can minimize the power consumption of the system. In the standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V section are disconnected. PLL, HSI, and HSE oscillators are also turned off. They can be woken by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. They also can be woken and reset by the watchdog timer.

The contents of SRAM and registers will be lost. Only backup registers and standby circuits remain powered.

2.2.13 DMA

Flexible 5-way universal DMA can manage the data transfer from memory to memory, from device to memory and from memory to device. The DMA controller supports the management of the ring buffer, avoiding the interrupt which occurs during the controller transfer at the end of the buffer.

Each channel has its own hardware DMA request logic and can be triggered by software. The length, the source address, and the destination address of the transfer can be set separately by the software.

DMA can be used for major peripherals: UART, I2C, SPI, ADC, USB, and universal/basic /advanced control timer TIMx.

2.2.14 Real Time Clock (RTC)

The real time clock is a separate timer. RTC module has a set of counters that count continuously, which can provide the function of clock calendar in the corresponding software configuration. The current time and date of the system can be reset by changing values of the counters. The RTC module and the clock configuration system (RCC_BDCR register) resides in the backup area, which means RTC settings and time remain the same.

After the system is reset or the standby mode is awakened.

2.2.15 Backup Register

Backup registers include twenty 16-bit registers that are used to store user application data.

They will not be reset even when the system is woken up in the standby mode, or when the system is reset or when the power is reset.

2.2.16 Timers and Watchdog

The product includes one advanced timer, two universal timers, three basic timers, two watchdog timers and one system tick timer.

The following table compares the functions of advanced control timer, universal timer and basic timer:

Table 4. Timer Function Comparison

Timer type	Name	Counter Resolution	Counter type	Prescaler Coeffi-cient	DMA Request Generation	Capture/ compare channels	Comple -mentary outputs
Advanced	TIM1	16-bit	Up, down, up/down	Any integer between 1~65536	Yes	4	Yes
Universal	TIM2	32-bit	Up, down, up/down	Any integer between 1 $\sim 2^{32}-1$	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1~65536	Yes	4	No
Basic	TIM14	16-bit	Up	Any integer between 1~65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	Any integer between 1~65536	Yes	1	Yes

Advanced control timer (TIM1)

Advanced control timer is composed of one 16-bit counter, 4 capture/comparison channels and three-phase complementary PWM generator. It has complementary PWM output with dead zone insertion and can be used as a complete universal timer. Four separate channels can be used for the followings:

- Input capture
- Output comparison
- PWM generation (edge or center alignment mode)
- Single pulse output

When it is configured as a 16-bit universal timer, it has the same function as a TIMx timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In the debug mode, the counter can be frozen while the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many of its features are the same as the universal TIM timer. Their internal structures are identical. Therefore the advanced control timer can be used in conjunction with the TIM timer to support synchronization or event linking.

Universal timer (TIMx)

Two synchronously running universal timers (TIM2, TIM3) are built into the product. The universal timer has one 32-bit automatic up-down counter, one 16-bit prescaler and four separate channels. Each channel can be used for input capture, output comparison, PWM and single pulse output.

Universal Timer_32-bit

The universal timer has one 32-bit automatic up-down counter, one 16-bit prescaler and four separate channels. Each channel can be used for input capture, output comparison, PWM and single pulse output.

Universal Timer_16-bit

The universal timer has one 16-bit automatic up-down counter, one 16-bit prescaler and four separate channels. Each channel can be used for input capture, output comparison, PWM and single pulse output.

They can also be used in conjunction with the advanced control timer to support synchronization or event linking. Counters can be frozen in the debug mode. Any universal timer can be used to produce PWM output. Each timer has its own DMA request mechanism.

These timers can also handle signals from incremental encoders and digital outputs from 1~4 Hall sensors. Each timer can produce PWM output, or be seen as a simple time reference.

TIM3

The timer is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

The timer can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timer

TIM14

The timer contains one 16-bit automatically reloadable count-up counter and one 16-bit

prescaler. It has a single channel for input capture/output comparison, PWM or single pulse output. Its counter can be frozen in the debug mode.

TIM16/TIM17

Both timers contain one 16-bit automatically reloadable count-up counter and one 16-bit prescaler. Both timers have a single channel for input capture/output comparison, PWM or single pulse output. They have complementary outputs with functions of dead zone generation and independent DMA request generation. In the debug mode, the timers are off.

Independent watchdog (IWDG)

The independent watchdog contains one 12-bit count-down counter and one 8-bit prescaler. There is an internal independent 40KHz clock oscillator. This oscillator is independent of the master clock, so it can work in the shutdown and standby modes. It can be used to reset the entire system in the event of system failure or used as a free timer to provide timeout management for applications. The options can be configured to boot watchdog via software or hardware. In the debug mode, the watchdog is off.

System window watchdog (WWDG)

The window watchdog has one 7-bit count-down counter and can be set to run freely. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. In the debug mode, the watchdog is off.

System Time Base Timer

This timer is dedicated to the real-time operating system and can also be used as a standard count-down counter. It has the following characteristics:

- A 24-bit count-down counter
- Automatic reloading
- A maskable system interrupt can be produced when the counter is 0
- Programmable clock source

2.2.17 Universal Asynchronous Receiver and Transmitter (UART)

The UART interface supports hardware CTS and RTS signal management. It also supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be 5, 6, 7, 8 and 9 bits, which are configurable.

All UART interfaces are compatible with DMA.

2.2.18 I2C Bus

I2C bus interface can operate in the multi-master mode or slave mode and it supports the standard and fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

2.2.19 Serial Peripheral Interface (SPI)

The SPI interface can be configured as 1-32 bits per frame in the slave or master mode.

All SPI interfaces are compatible with DMA.

2.2.20 Universal Serial Bus (USB)

A device controller compatible with full-speed USB is built into the product, following the full-speed USB (12 Mb/s) standard. The endpoints can be configured by the software. The dedicated 48MHz clock for USB is generated directly from the internal PLL or internal clock (HSI) at room temperature.

2.2.21 Controller Area Network (CAN)

The CAN interface is compatible with specifications 2.0A and 2.0B (active), with bit rate up to 1 Mb/s. It can receive and send standard frames with 11-bit identifiers or extended frames with 29-bit identifiers.

2.2.22 General Purpose Input/Output Interface (GPIO)

The product is embedded with a 12-bit analog-to-digital converter (ADC), with up to 10 external channels available for single, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

ADC is compatible with DMA.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by a general timer (TIMx) and an advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can convert the ADC to synchronize with the clock.

2.2.23 Analog-to-Digital Converter(ADC)

The one 12-bit analog-to-digital converters is embedded into microcontrollers and the ADC shares up to 10 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs. The ADC can be served by the DMA controller.

The analog watchdog function allows very precise monitoring of all the way, multiple or all selected channels, and an interruption occurs when the monitored signal exceeds the preset threshold.

Events generated by a general timer (TIMx) and an advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can convert the ADC to synchronize with the clock.

2.2.24 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature in a linear relation. The temperature sensor is internally connected to the ADC input channel to convert the sensor output to a digital value.

2.2.25 Serial Wire Debug Port (SW-DP)

Two-wire serial debug port (SW-DP) is embedded in ARM.

The ARM SW-DP allows to be connected to single-chip microcomputer through serial wire debugging tools.

2.2.26 Comparator (COMP)

The product has two built-in comparators, which can be used independently (suitable for I/O ports on all terminals) or in combination with the timer. It can also be used for a variety of functions, including:

- Trigger wake-up events in the low power mode by analog signals
- Adjust the analog signal
- Combine with PWM from timer to form a cycle-by-cycle current control loop
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - Multiplexed I/O pins
  - The internal comparison voltage CRV can be AVDD or the partial voltage value of the internal reference voltage
- Programmable hysteresis voltage
- Programmable rate and power consumption
- The output terminal can be redirected to an I/O port or multiple timer input terminals, which can trigger the following events:
  - Capture event
  - OCref_clr event (cycle-by-cycle current control)
  - Brake event to shut off PWM rapidly

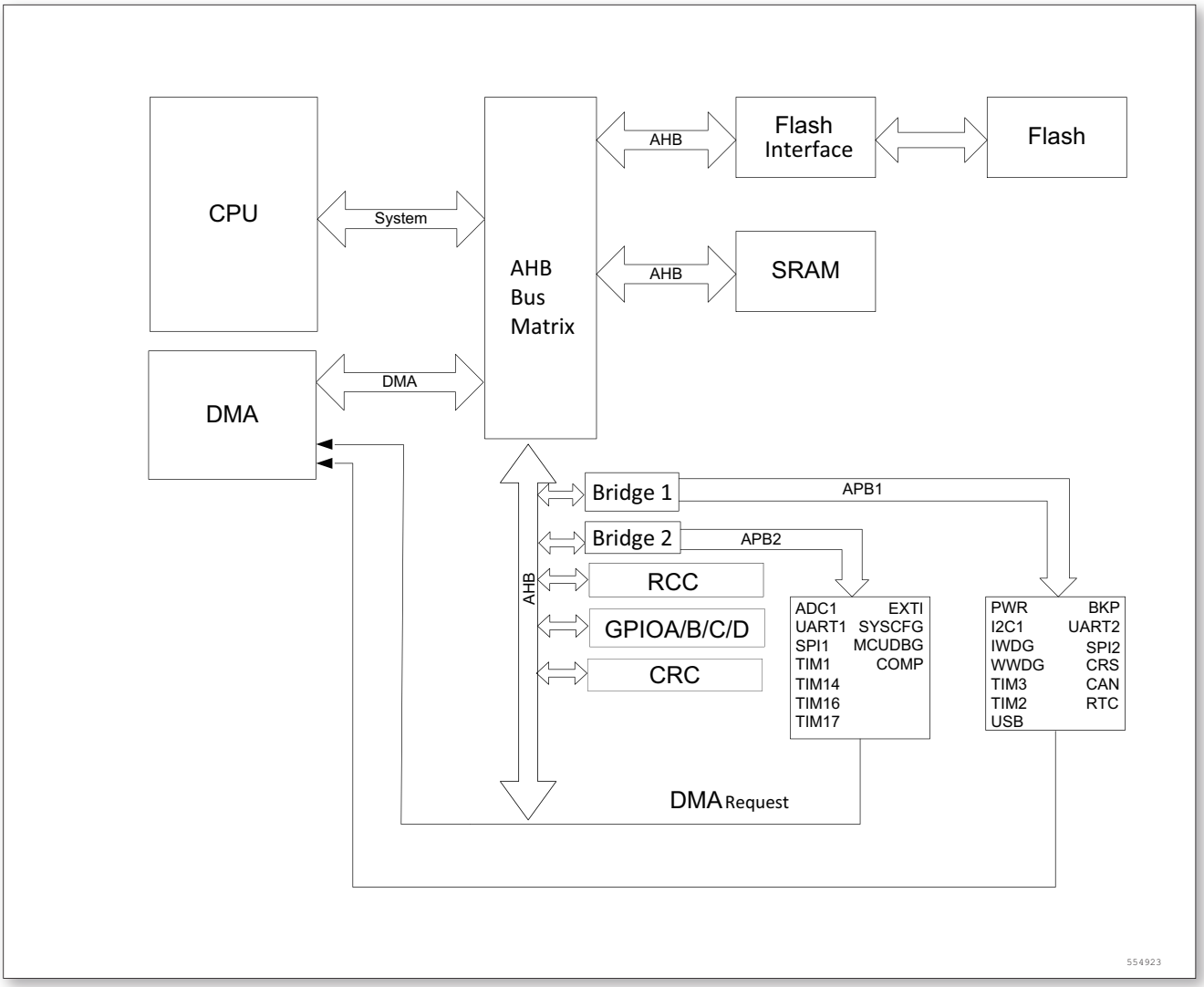

Figure 1. Module Diagram

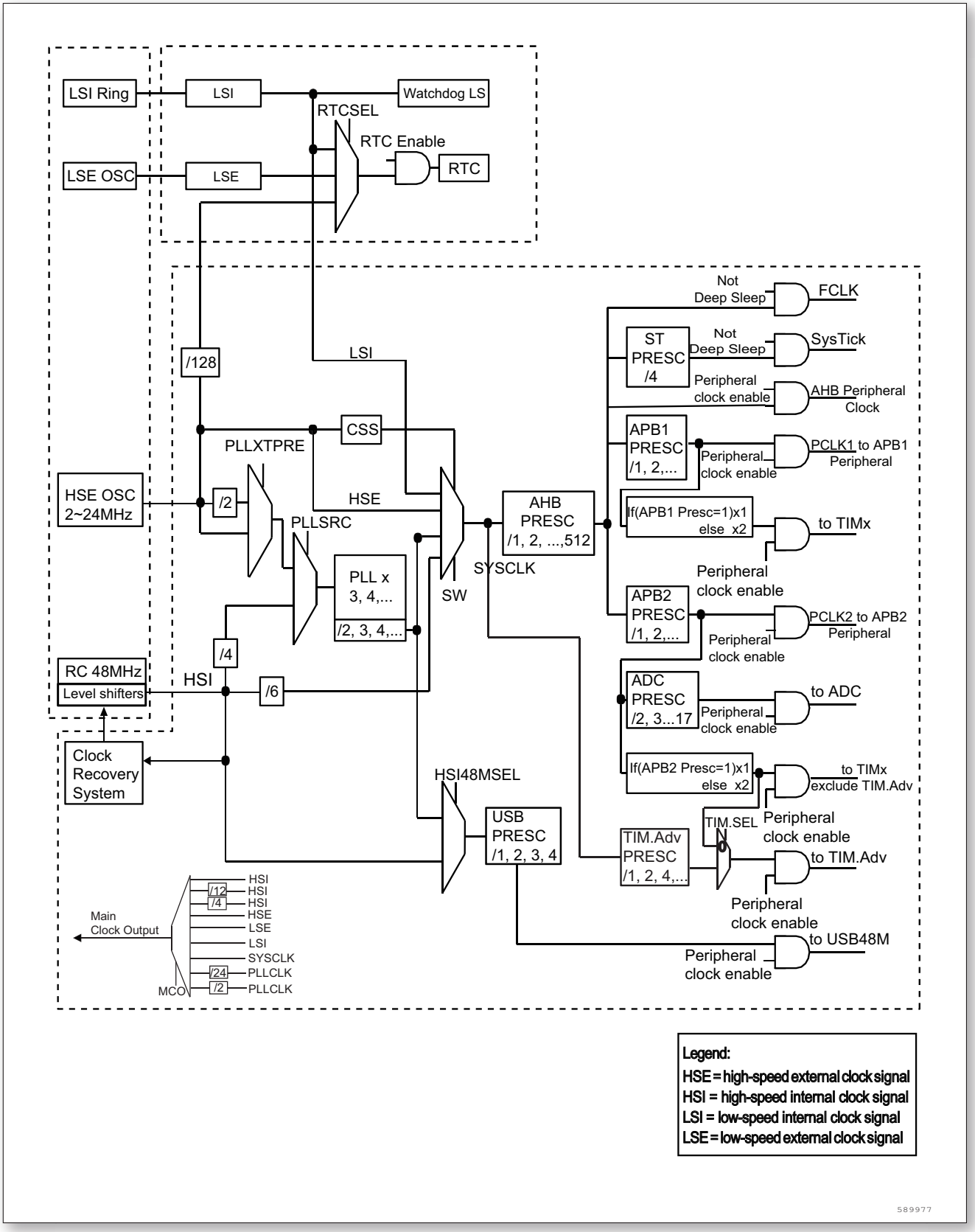

Figure 2. Clock Tree

3 Pin definition

Pin definition

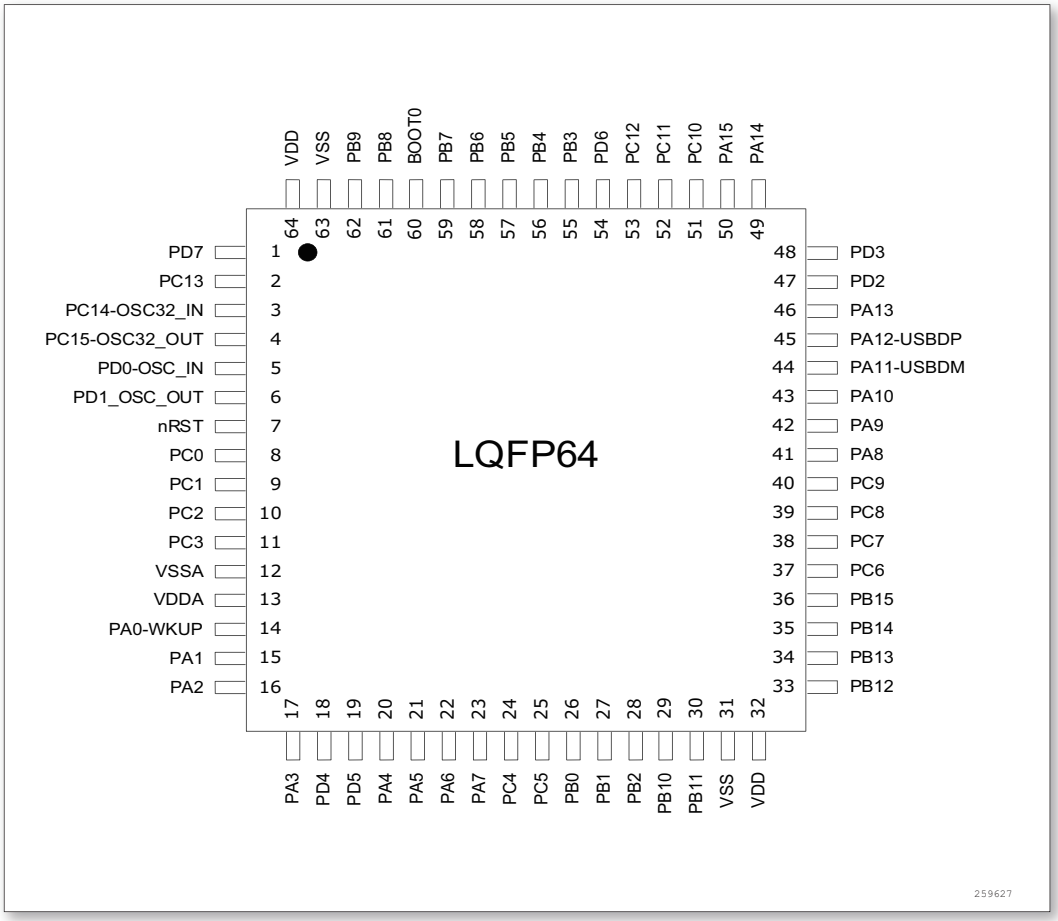

Figure 3. LQFP64 Pin Distribution

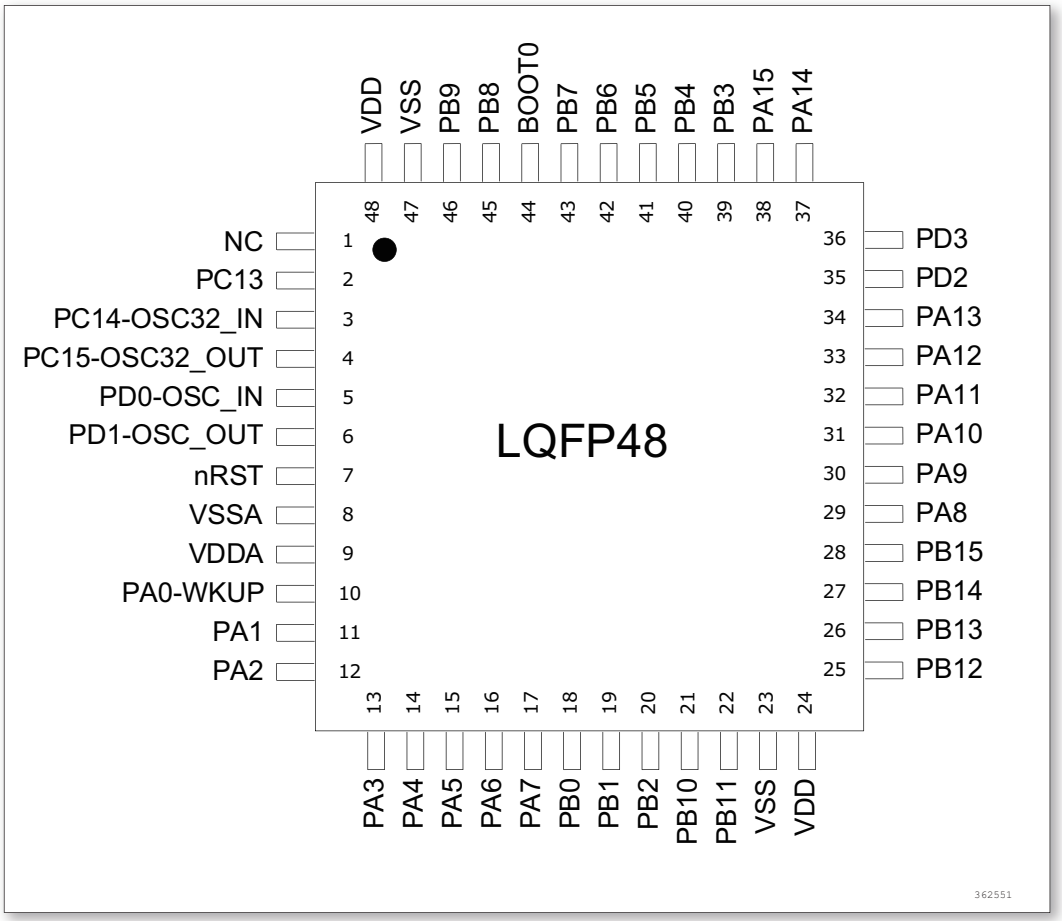

Figure 4. LQFP48 Pin Distribution

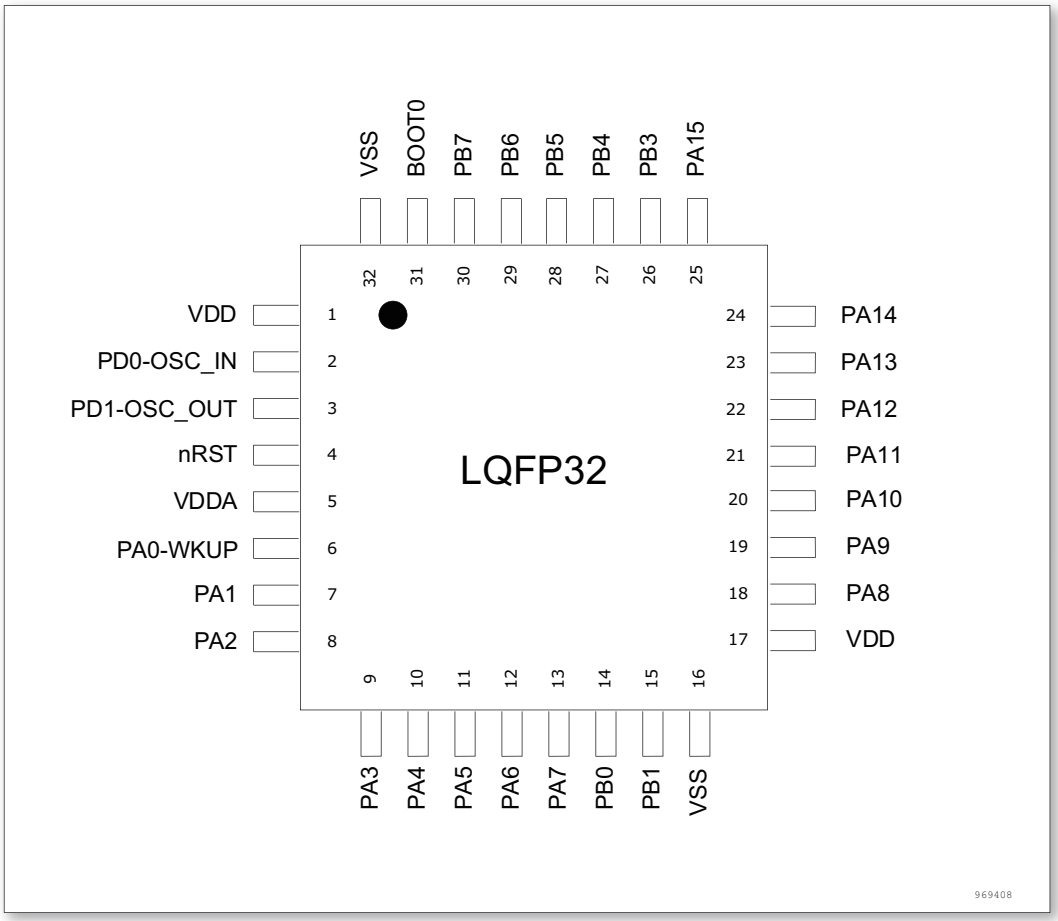

Figure 5. LQFP32 Pin Distribution

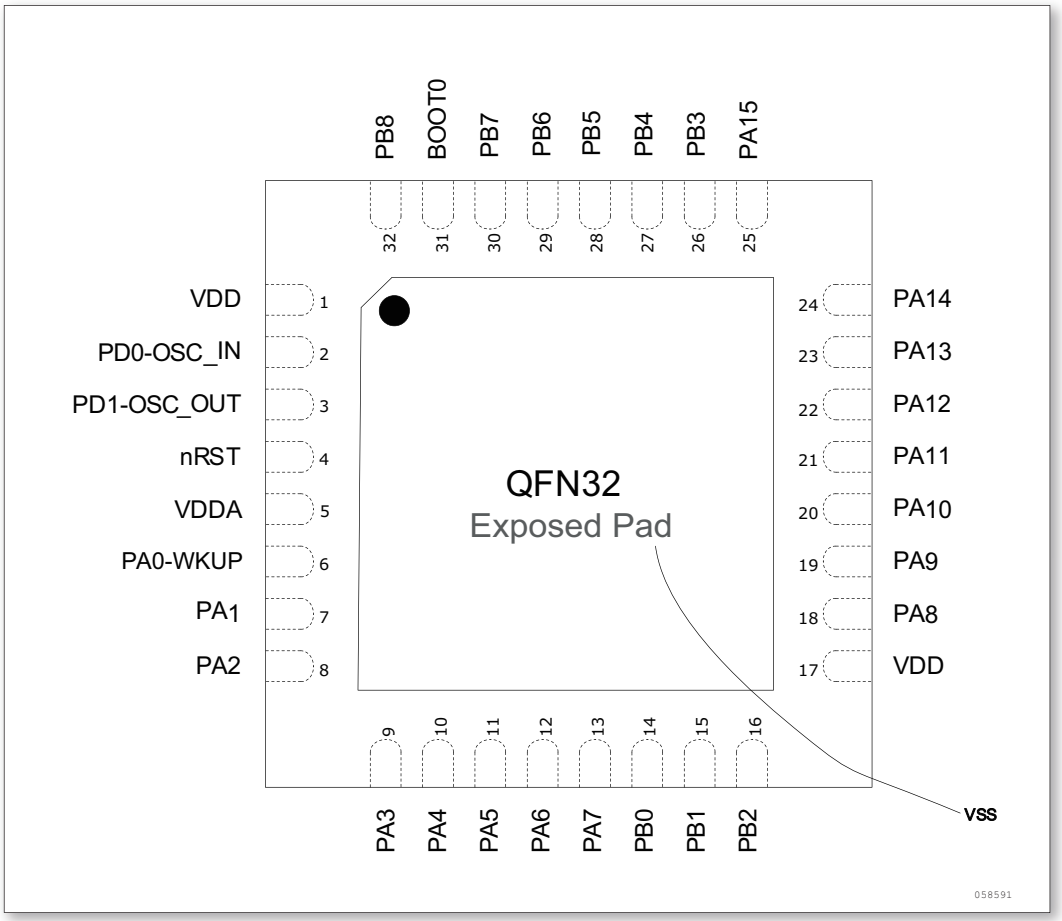

Figure 6. QFN32 Pin Distribution

Note: For details about pin functions, please refer to the product selection table.

Table 5. Pin Definition

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
1	-	-	-	PD7	I/O	TC	PD7	TIM3_CH1 TIM17_CH1	-
2	2	-	-	PC13	I/O	TC	PC13	TIM2_CH1 TIM2_ETR	-
3	3	-	-	PC14 OSC32_IN	I/O	TC	PC14	TIM2_CH2	-
4	4	-	-	PC15 OSC32_OUT	I/O	TC	PC15	TIM2_CH3	-

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
5	5	2	2	PD0 OSC_IN	I/O	TC	PD0	I2C1_SDA TIM1_CH1N UART1_TX TIM1_CH2 SPI1_MOSI	-
6	6	3	3	PD1 OSC_OUT	I/O	TC	PD1	TIM1_BKIN I2C1_SCL TIM1_CH1 UART1_RX TIM1_CH2 SPI1_MISO SPI1_SCK	-
7	7	4	4	nRST	I/O	TC	nRST	-	-
8	-	-	-	PC0	I/O	TC	PC0	-	-
9	-	-	-	PC1	I/O	TC	PC1	-	-
10	-	-	-	PC2	I/O	TC	PC2	SPI2_MISO	-
11	-	-	-	PC3	I/O	TC	PC3	SPI2_MOSI	-
12	8	-	0	VSSA	S	-	VSSA	-	-
13	9	5	5	VDDA	S	-	VDDA	-	-
14	10	6	6	PA0 WKUP	I/O	TC	PA0	UART2_CTS TIM2_CH1 TIM2_ETR UART1_RX TIM14_CH1 COMP1_OUT	ADC1_VIN[0] COMP1_INP[0] COMP2_INP[0] COMP1_INM[2]
15	11	7	7	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2 TIM1_CH2 UART1_TX	ADC1_VIN[1] COMP1_INP[1] COMP2_INP[1]
16	12	8	8	PA2	I/O	TC	PA2	UART2_TX TIM2_CH3 TIM1_CH2N COMP2_OUT	ADC1_VIN[2] COMP1_INP[2] COMP2_INP[2] COMP2_INM[2]
17	13	9	9	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4 TIM1_CH3	ADC1_VIN[3] COMP1_INP[3] COMP2_INP[3]

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
18	-	-	-	PD4	I/O	TC	PD4	SPI1_MISO SPI1_MOSI	-
19	-	-	-	PD5	I/O	TC	PD5	SPI1_MOSI SPI1_MISO	-
20	14	10	10	PA4	I/O	TC	PA4	SPI1_NSS SPI1_SCK TIM1_CH3N TIM14_CH1 TIM1_BKIN	ADC1_VIN[4] COMP1_INM[0] COMP2_INM[0]
21	15	11	11	PA5	I/O	TC	PA5	SPI1_SCK SPI1_NSS TIM2_CH1 TIM2_ETR TIM1_CH3N	ADC1_VIN[5] COMP1_INM[1] COMP2_INM[1]
22	16	12	12	PA6	I/O	TC	PA6	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 TIM1_CH3 COMP1_OUT	ADC1_VIN[6]
23	17	13	13	PA7	I/O	TC	PA7	SPI1_MOSI TIM3_CH2 TIM1_CH1N TIM1_CH3N TIM14_CH1 TIM17_CH1 TIM1_CH2N COMP2_OUT	ADC1_VIN[7]
24	-	-	-	PC4	I/O	TC	PC4	UART2_TX TIM3_CH1 SPI1_MOSI	-
25	-	-	-	PC5	I/O	TC	PC5	UART2_RX TIM3_CH2 SPI1_MISO	-

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
26	18	14	14	PB0	I/O	TC	PB0	TIM3_CH3 TIM1_CH2N TIM1_CH1N TIM1_CH3	ADC1_VIN[8]
27	19	15	15	PB1	I/O	TC	PB1	TIM14_CH1 TIM3_CH4 TIM1_CH3N TIM1_CH2N TIM2_CH3 TIM1_CH2 TIM1_CH1N	ADC1_VIN[9]
28	20	-	16	PB2	I/O	TC	PB2	-	-
29	21	-	-	PB10	I/O	TC	PB10	I2C1_SCL TIM2_CH3 SPI2_SCK	-
30	22	-	-	PB11	I/O	TC	PB11	I2C1_SDA TIM2_CH4	-
31	23	16	0	VSS	S	-	VSS	-	-
32	14	17	17	VDD	S	-	VDD	-	-
33	25	-	-	PB12	I/O	TC	PB12	SPI2_NSS SPI2_SCK TIM1_BKIN SPI2_MOSI SPI2_MISO	-
34	26	-	-	PB13	I/O	TC	PB13	SPI2_SCK SPI2_MISO TIM1_CH1N SPI2_NSS SPI2_MOSI I2C1_SCL TIM17_CH1 TIM1_CH3N	-

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
35	27	-	-	PB14	I/O	TC	PB14	SPI2_MISO SPI2_MOSI TIM1_CH2N SPI2_SCK SPI2_NSS I2C1_SDA TIM1_CH3 TIM1_CH1	-
36	28	-	-	PB15	I/O	TC	PB15	SPI2_MOSI SPI2_NSS TIM1_CH3N SPI2_MISO SPI2_SCK TIM1_CH2N TIM1_CH2	-
37	-	-	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM3_CH3 SPI1_NSS	-
38	-	-	-	PC7	I/O	TC	PC7	TIM3_CH2 TIM2_CH1 TIM2_ETR SPI1_SCK	-
39	-	-	-	PC8	I/O	TC	PC8	TIM3_CH3 TIM2_CH2	-
40	-	-	-	PC9	I/O	TC	PC9	TIM3_CH4 TIM2_CH3	-
41	29	18	18	PA8	I/O	TC	PA8	MCO TIM1_CH1 TIM1_CH2 TIM1_CH3	-
42	30	19	19	PA9	I/O	TC	PA9	UART1_TX TIM1_CH2 UART1_RX I2C1_SCL MCO TIM1_CH1N	-

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
43	31	20	20	PA10	I/O	TC	PA10	TIM17_BKIN UART1_RX TIM1_CH3 UART1_TX I2C1_SDA TIM1_CH1 TIM16_CH1	-
44	32	21	21	PA11	I/O	TC	PA11	UART1_CTS TIM1_CH4 TIM1_CH3 CAN1_RX I2C1_SCL TIM1_BKIN COMP1_OUT	USB_DM
45	33	22	22	PA12	I/O	TC	PA12	UART1_RTS TIM1_ETR TIM1_CH3N CAN1_TX I2C1_SDA TIM1_CH2 COMP2_OUT	USB_DP
46	34	23	23	PA13	I/O	TC	PA13	SWDIO UART1_TX	-
47	35	-	-	PD2	I/O	TC	PD2	I2C1_SCL SPI1_NSS	-
48	36	-	-	PD3	I/O	TC	PD3	I2C1_SDA SPI1_SCK SPI1_MISO	-
49	37	24	24	PA14	I/O	TC	PA14	SWDCLK UART2_TX UART1_RX	-

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
50	38	25	25	PA15	I/O	TC	PA15	SPI1_NSS UART2_RX TIM2_CH1 TIM2_ETR SPI2_SCK SPI2_MOSI SPI2_MISO TIM1_CH1N TIM1_CH3N	-
51	-	-	-	PC10	I/O	TC	PC10	UART1_TX SPI2_MISO SPI2_SCK SPI2_NSS SPI2_MOSI COMP2_OUT	-
52	-	-	-	PC11	I/O	TC	PC11	UART1_RX SPI2_MOSI SPI2_NSS SPI2_SCK SPI2_MISO	-
53	-	-	-	PC12	I/O	TC	PC12	UART1_TX SPI2_SCK SPI2_MISO SPI2_MOSI SPI2_NSS	-
54	-	-	-	PD6	I/O	TC	PD6	TIM3_ETR TIM1_CH3N TIM1_CH1 TIM1_CH1N	-
55	39	26	26	PB3	I/O	TC	PB3	SPI1_SCK TIM2_CH2 TIM1_CH1 TIM1_CH2N TIM1_CH3	-

Pin Code				Pin name	Type(1)	I/O Level (2)	Main Function	Alternate Functions	Additional Functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
56	40	27	27	PB4	I/O	TC	PB4	SPI1_MISO TIM3_CH1 TIM1_CH2 TIM17_BKIN TIM1_CH3N TIM1_CH2N	-
57	41	28	28	PB5	I/O	TC	PB5	SPI1_MOSI TIM3_CH2 TIM16_BKIN TIM1_CH1 TIM1_CH2	-
58	42	29	29	PB6	I/O	TC	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM1_CH2N TIM1_CH2 TIM1_CH1N	-
59	43	30	30	PB7	I/O	TC	PB7	UART1_RX I2C1_SDA TIM17_CH1N TIM1_CH3 TIM1_CH1	-
60	44	31	31	BOOT0	I	-	BOOT0	-	-
61	45	-	32	PB8	I/O	TC	PB8	UART1_RX I2C1_SCL TIM16_CH1 TIM1_CH1 CAN1_RX TIM3_CH2	-
62	46	-	-	PB9	I/O	TC	PB9	UART1_TX I2C1_SDA TIM17_CH1 CAN1_TX SPI2_NSS TIM3_CH3	-
63	47	32	0	VSS	S	-	VSS	-	-
64	48	1	1	VDD	S	-	VDD	-	-

1. I = Input, O = Output, S = Power Supply, HiZ = High Resistance.
2. TC: Standard I/O, Input signal does not exceed VDD voltage.

Table 6. PA Port Alternate Function AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1 TIM2_ETR	-	UART1_RX	-	TIM14_CH1	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	TIM1_CH2	UART1_TX	-	-	-
PA2	-	UART2_TX	TIM2_CH3	TIM1_CH2N	-	-	-	COMP2_OUT
PA3	-	UART2_RX	TIM2_CH4	TIM1_CH3	-	-	-	-
PA4	SPI1_NSS	SPI1_SCK	-	TIM1_CH3N	TIM14_CH1	TIM1_BKIN	-	-
PA5	SPI1_SCK	SPI1_NSS	TIM2_CH1 TIM2_ETR	-	-	-	TIM1_CH3N	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	TIM1_CH3	COMP1_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	TIM1_CH3N	TIM14_CH1	TIM17_CH1	TIM1_CH2N	COMP2_OUT
PA8	MCO	-	TIM1_CH1	-	-	CSM_CH1_ TXRX	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	TIM1_CH1	TIM16_CH1	-
PA11	-	UART1_CTS	TIM1_CH4	TIM1_CH3	CAN1_RX	I2C1_SCL	TIM1_BKIN	COMP1_OUT
PA12	-	UART1_RTS	TIM1_ETR	TIM1_CH3N	CAN1_TX	I2C1_SDA	TIM1_CH2	COMP2_OUT
PA13	SWDIO	-	-	UART1_TX	-	-	-	-
PA14	SWDCLK	UART2_TX	-	UART1_RX	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1 TIM2_ETR	SPI2_SCK	SPI2_MOSI	SPI2_MISO	TIM1_CH1N	TIM1_CH3N

Table 7. PB Port Alternate Function AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH2N	TIM2_CH3	TIM1_CH2	TIM1_CH1N	-
PB3	SPI1_SCK	-	TIM2_CH2	-	TIM1_CH1	-	TIM1_CH2N	TIM1_CH3
PB4	SPI1_MISO	TIM3_CH1	-	-	TIM1_CH2	TIM17_BKIN	TIM1_CH3N	TIM1_CH2N
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	TIM1_CH1	TIM1_CH2
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM1_CH2N	-	TIM1_CH2	TIM1_CH1N
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM1_CH3	TIM1_CH1
PB8	UART1_RX	I2C1_SCL	TIM16_CH1	TIM1_CH1	CAN1_RX	-	TIM3_CH2	-
PB9	UART1_TX	I2C1_SDA	TIM17_CH1	-	CAN1_TX	SPI2_NSS	TIM3_CH3	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM17_CH1	TIM1_CH3N
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	TIM1_CH3	TIM1_CH1
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	-	TIM1_CH2N	TIM1_CH2

Table 8. PC Port Alternate Function AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC2	-	SPI2_MISO	-	-	-	-	-	-
PC3	-	SPI2_MOSI	-	-	-	-	-	-
PC4	-	-	-	UART2_TX	-	TIM3_CH1	SPI1_MOSI	-
PC5	-	-	-	UART2_RX	-	TIM3_CH2	SPI1_MISO	-
PC6	-	TIM3_CH1	-	-	-	TIM3_CH3	SPI1_NSS	-
PC7	-	TIM3_CH2	-	-	-	TIM2_CH1 TIM2_ETR	SPI1_SCK	-
PC8	-	TIM3_CH3	-	-	-	TIM2_CH2	-	-
PC9	-	TIM3_CH4	-	-	-	TIM2_CH3	-	-
PC10	UART1_TX	-	-	SPI2_MISO	SPI2_SCK	SPI2_NSS	SPI2_MOSI	COMP2_OUT
PC11	UART1_RX	-	-	SPI2_MOSI	SPI2_NSS	SPI2_SCK	SPI2_MISO	-
PC12	UART1_TX	-	-	SPI2_SCK	SPI2_MISO	SPI2_MOSI	SPI2_NSS	-
PC13	-	-	-	-	-	-	TIM2_CH1 TIM2_ETR	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 9. PD Port Alternate Function AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	TIM1_CH1N	UART1_TX	TIM1_CH2	SPI1_MOSI	SPI1_MOSI	-
PD1	TIM1_BKIN	I2C1_SCL	TIM1_CH1	UART1_RX	TIM1_CH2	SPI1_MISO	SPI1_SCK	-
PD2	-	I2C1_SCL	-	-	-	SPI1_NSS	SPI1_NSS	-
PD3	-	I2C1_SDA	-	-	-	SPI1_SCK	SPI1_MISO	-
PD4	SPI1_MISO	SPI1_MOSI	-	-	-	-	-	-
PD5	SPI1_MOSI	SPI1_MISO	-	-	-	-	-	-
PD6	-	TIM3_ETR	-	TIM1_CH3N	-	TIM1_CH1	TIM1_CH1N	-
PD7	-	-	-	-	-	TIM3_CH1	TIM17_CH1	-

4 Memory mapping

Memory mapping

Table 10. Memory mapping

Bus	Boundary Address	Size	Peripheral	Remark
Flash	0x0000 0000 -0x0000 FFFF	64 KB	Main flash memory, system memory, or SRAM, depends on the BOOT configuration	
	0x0001 0000 -0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000 -0x0800 FFFF	64 KB	Main Flash memory	
	0x0801 0000 -0x1FFD FFFF	~ 383 MB	Reserved	
	0x1FFE 0000 -0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200 -0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 -0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00 -0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400 -0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 -0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 -0x1FFF FFFF	~2 KB	Reserved	
SRAM	0x2000 0000 -0x2000 3FFF	16 KB	SRAM	
	0x2000 4000 -0x2FFF FFFF	~ 255 MB	Reserved	
APB1	0x4000 0000 -0x4000 03FF	1 KB	TIM2	
	0x4000 0400 -0x4000 07FF	1 KB	TIM3	
	0x4000 0800 -0x4000 0BFF	8 KB	Reserved	
	0x4000 2800 -0x4000 2BFF	1 KB	RTC/BKP	
	0x4000 2C00 -0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 -0x4000 33FF	1 KB	IWDG	
	0x4000 3400 -0x4000 37FF	1 KB	Reserved	
	0x4000 3800 -0x4000 3BFF	1 KB	SPI2	
	0x4000 4000 -0x4000 43FF	1 KB	Reserved	
	0x4000 4400 -0x4000 47FF	1 KB	UART2	
	0x4000 4800 -0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 -0x4000 57FF	1 KB	I2C1	
	0x4000 5800 -0x4000 6BFF	5 KB	Reserved	
	0x4000 5C00 -0x4000 5FFF	1 KB	USB	
	0x4000 6000 -0x4000 63FF	1 KB	Reserved	

Bus	Boundary Address	Size	Peripheral	Remark
APB1	0x4000 6400 -0x4000 67FF	1 KB	CAN	
	0x4000 6800 -0x4000 6BFF	1 KB	Reserved	
	0x4000 6C00 -0x4000 6FFF	1 KB	CSR	
	0x4000 7000 -0x4000 73FF	1 KB	PWR	
APB2	0x4000 7400 -0x4000 FFFF	35 KB	Reserved	
	0x4001 0000 -0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 -0x4001 07FF	1 KB	EXTI	
	0x4001 0800 -0x4001 23FF	7 KB	Reserved	
	0x4001 2400 -0x4001 27FF	1 KB	ADC1	
	0x4001 2800 -0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00 -0x4001 2FFF	1 KB	TIM1	
	0x4001 3000 -0x4001 33FF	1 KB	SPI1	
	0x4001 3400 -0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800 -0x4001 3BFF	1 KB	UART1	
	0x4001 3C00 -0x4001 3FFF	1 KB	COMP	
	0x4001 4000 -0x4001 43FF	1 KB	TIM14	
	0x4001 4400 -0x4001 47FF	1 KB	TIM16	
	0x4001 4800 -0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 -0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000 -0x4002 03FF	1 KB	DMA	
	0x4002 0400 -0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 -0x4002 13FF	1 KB	RCC	
	0x4002 1400 -0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 -0x4002 23FF	1 KB	Flash Interface	
	0x4002 2400 -0x4002 2FFF	3 KB	Reserved	
	0x4002 3000 -0x4002 33FF	1 KB	CRC	
	0x4002 3400 -0x4002 FFFF	47 KB	Reserved	
	0x4003 0000 -0x4003 03FF	1 KB	Reserved	
	0x4003 0400 -0x47FF FFFF	~ 127 MB	Reserved	
	0x4800 0000 -0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 -0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 -0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 -0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 -0x5FFF FFFF	~ 384 MB	Reserved	

5 Electrical characteristics

Electrical characteristics

5.1 Test condition

Unless otherwise specified, V_{SS} is seen as the benchmark of all voltages.

5.1.1 Typical Value

Unless otherwise specified, typical data are based on T_A = 25°C and V_{DD} = 3.3V.These data are only used for design guidance and have not been tested.

5.1.2 Typical curve

Unless otherwise specified, the typical curve is only used for design guidance and has not been tested.

5.1.3 Load Capacitance

The load condition during the measurement of pin parameters is shown in the figure below.

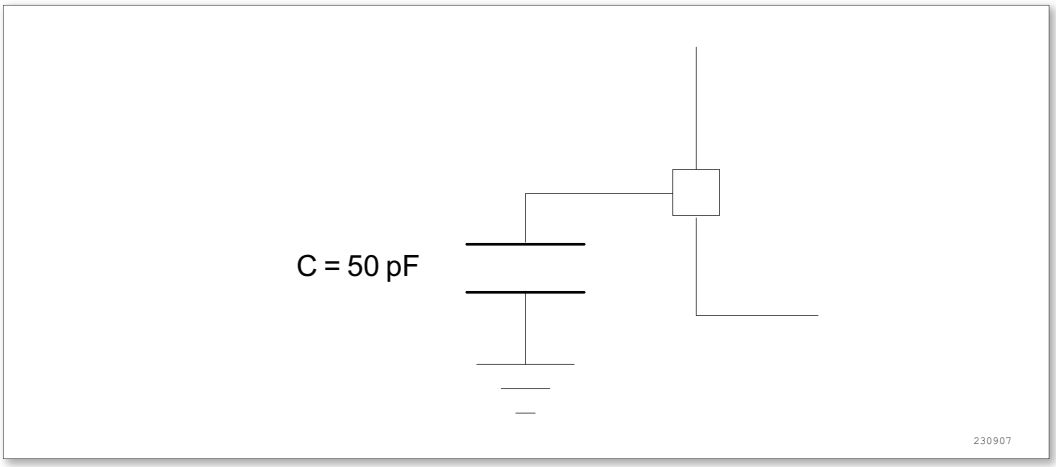

Figure 7. Load Condition of Pin

5.1.4 Input Voltage on Pin

The measurement of input voltage on pin is shown in the figure below.

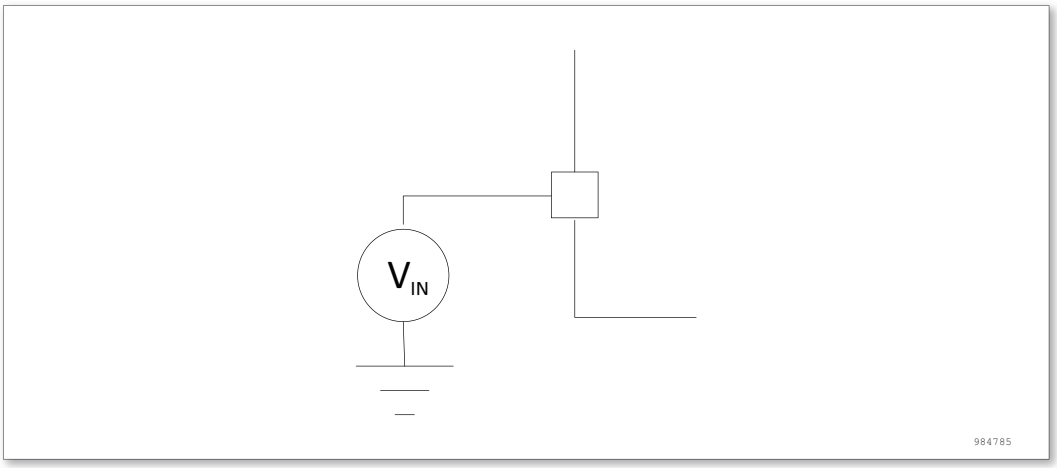

Figure 8. Input Voltage on Pin

5.1.5 Power Supply Scheme

The power supply designing plan is shown in the figure below.

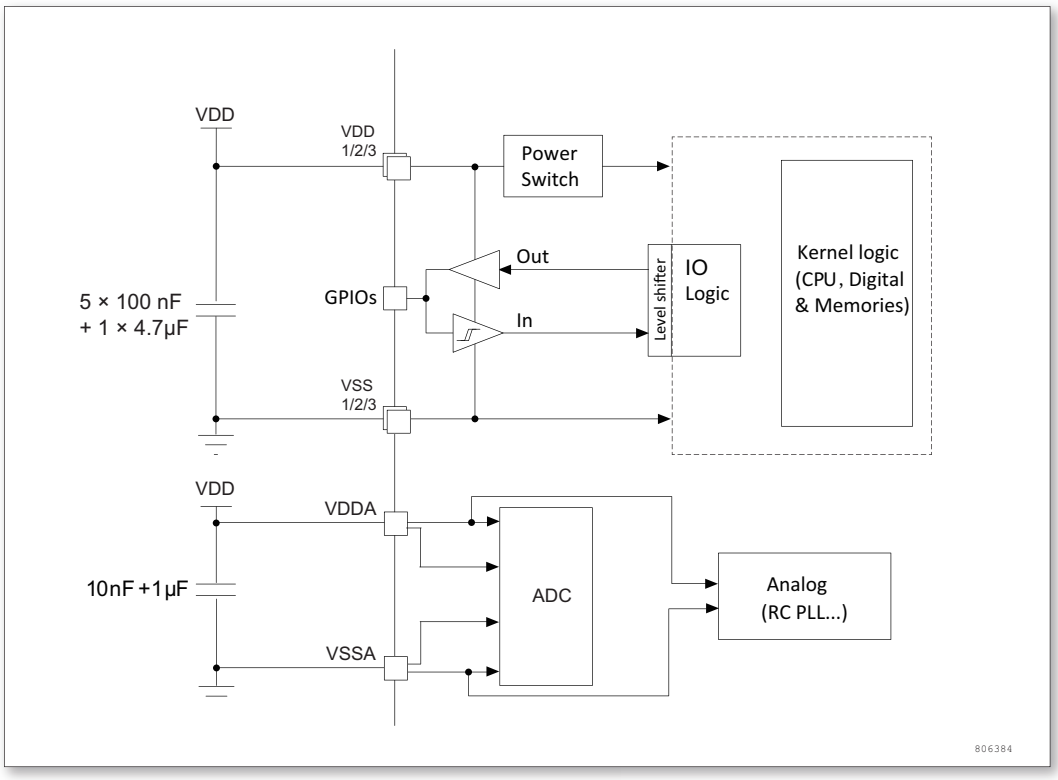

Figure 9. Power Supply Scheme

5.1.6 Measurement of Current Consumption

The measurement of the current consumption on the pin is shown in the figure below.

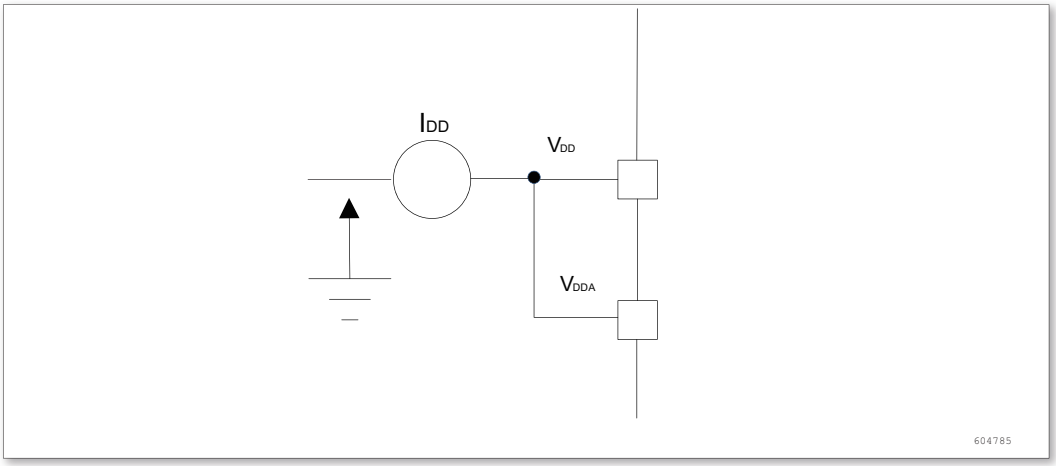

Figure 10. Measurement of Current Consumption

5.2 Absolute Maximum Rating

If the load applied to the device exceeds the value in the list of absolute maximum ratings (Table 11 and Table 12), the device may be damaged permanently. The list shows the maximum load that the device can bear. It does not mean that the functional operation of the device under these conditions is normal. The reliability of the device will be affected if the device works for a long time under the maximum condition.

Table 11. Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{SS})(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins (2)	V_{SS} - 0.3	V_{DD} + 0.3	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within the permissible range.
2. The maximum value of V_{IN}must always be observed. For information about the permitted maximum current values, please see the table below.

Table 12. Current Characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power cord (supply current) (1)	120	mA
I_{VSS}	Total current through V_{SS} ground wire (1)	-120	
I_{IO}	Sink current through any I/O and control pins	25	
	Output current through any I/O and control pins	-25	
$I_{INJ(PIN)}$ (2)(3)	Injection current through nRST pin	±5	
	Injection current through OSC_IN pin of HSE	±5	
$I_{INJ(PIN)}$ (4)	Injection current through other pins (4)	±25	

1. All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA})pins must always be connected to the external power supply system within the permissible range.
2. $I_{INJ(PIN)}$ must not exceed its limit, that is to ensure the V_{IN} does not exceed its maximum. If you cannot guarantee that the V_{IN} does not exceed its maximum value, please make sure that the $I_{INJ(PIN)}$ does not exceed its maximum value under external constraint. When $V_{IN} > V_{DD}$, there is a forward injection current; When $V_{IN} < V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When injection currents go through several I/O ports at the same time, the maximum $\Sigma I_{INJ(PIN)}$ is the sum of absolute values of the forward and reverse injection currents in the real time. The result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on all the I/O ports.

5.3 Operating Condition

5.3.1 General operating conditions

Table 13. General Operating Condition

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72MHz	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Standard operating voltage		2.0	5.5	V
P_D	T_A=85°C				mW
T_A	T_A	Maximum power dissipation	-40	85	°C
		Low power dissipation(2)	-40	105	
T_J	Junction temperature range		-40	105	°C

1. It is recommended to use the same power source for V_{DD} and V_{DDA}.
2. If T_A is low, a higher P_D value are allowed as long as T_J does not exceed T_{Jmax} (See subsec 5.1).

5.3.2 Operating Condition when Power is On and Power is Down

The parameters in the table below are tested under general operating conditions.

Table 14. Operating Condition when Power is On and Power is Down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{VDD}rise speed	T_A = 25°C	1	∞	μS/V
	V_{VDD}fall speed		500	∞	

5.3.3 Characteristics of Embedded Reset and Power-Control Models

The parameters in the table below are tested based on the ambient temperature and VDD supply voltage listed inTable 13.

Table 15. Characteristics of Embedded Reset and Power-Control Models

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[3：0]=0000 (Rising edge)		1.8		V
		PLS[3：0]=0000 (Falling edge)		1.7		V
		PLS[3：0]=0001 (Rising edge)		2.1		V
V_{PVD}	Level selection of programmable voltage detector	PLS[3：0]=0001 (Falling edge)		2.0		V
		PLS[3：0]=0010 (Rising edge)		2.4		V
		PLS[3：0]=0010 (Falling edge)		2.3		V
		PLS[3：0]=0011 (Rising edge)		2.7		V
		PLS[3：0]=0011 (Falling edge)		2.6		V
		PLS[3：0]=0100 (Rising edge)		3.0		V
		PLS[3：0]=0100 (Falling edge)		2.9		V
		PLS[3：0]=0101 (Rising edge)		3.3		V
		PLS[3：0]=0101 (Falling edge)		3.2		V
		PLS[3：0]=0110 (Rising edge)		3.6		V
		PLS[3：0]=0110 (Falling edge)		3.5		V
		PLS[3：0]=0111 (Rising edge)		3.9		V
		PLS[3：0]=0111 (Falling edge)		3.8		V
		PLS[3：0]=1000 (Rising edge)		4.2		V
		PLS[3：0]=1000 (Falling edge)		4.1		V
		PLS[3：0]=1001 (Rising edge)		4.5		V
		PLS[3：0]=1001 (Falling edge)		4.4		V
		PLS[3：0]=1010 (Rising edge)		4.8		V
		PLS[3：0]=1010 (Falling edge)		4.7		V
$V_{POR/PDR}$	POR/PDR threshold	Trigger point		1.65		V
$T_{RSTTEMPO}$	Reset duration			2.7		ms

1. Guaranteed by design, not tested in production. *Note: Reset duration is measured from the power-on moment to the moment the first instruction is read by the user's application code.*

5.3.4 Supply Current Characteristics

Current consumption is an index of multiple parameters and factors, which include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, program location in memory and executed code, etc.

The current consumption readings in all operating modes given in this section execute a set of simple codes.

Maximum Current Consumption

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load)
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the f_{HCLK} (0 ~ 24 MHz ;1 wait cycle at 24 ~ 48 MHz; 2 wait cycles at 48~ 72 MHz).
- The instruction prefetch function is enabled. When the peripheral is enabled: f_{PCLK1} = f_{PCLK2} =f_{HCLK}.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 16. Typical and maximum current consumption in stop and standby modes(2)

Symbol	Parameter	Conditions	Typical Value			Unit
			-40°C	25°C	85°C	
I_{DD}	Supply current in shutdown mode	PWR->CR[0] is set as 1	1.5	5.2	55.9	μA
	Supply current in standby mode	LSI and RTC are on	1.3	1.6	6.0	
		IWDG is on	0.5	0.5	5.1	

1. Drawn from comprehensive evaluation, not tested in production. The IO status is analog input.
2. The maximum value is tested in case of the power supply voltage = 3.3V.

Typical Current Consumption

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level —- V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the f_{HCLK} at (0 ~ 24 MHz 1 wait cycle at 24 ~ 48 MHz; 2 wait cycles at 48 ~ 72 MHz).
- The instruction prefetch function is enabled. When the peripheral is enabled: f_{PCLK1} =f_{PCLK2}= f_{HCLK}.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 17. Maximum Current Consumption in Operating Mode, with Data Processing Code Running from Internal Flash Memory(1)(2)(3)(4)(5)

Symbol	Parameter	Condition	f_{HCLK}	Enable all Peripherals			Disable all Peripherals			Unit
				-40°C	25°C	85°C	-40°C	25°C	85°C	
I_{DD}	Supply current in operating mode	Internal clock	72MHz	21.70	22.10	22.40	10.40	10.20	10.40	mA
			48MHz	15.70	16.00	16.30	8.37	8.07	8.24	
			24MHz	9.50	9.70	9.91	5.29	4.95	5.09	
			8MHz	5.19	5.30	5.42	3.10	2.67	2.75	
			4MHz	4.13	4.22	4.32	2.58	2.13	2.21	
			2MHz	3.62	3.69	3.78	2.32	1.86	1.93	
			1MHz	3.36	3.43	3.51	2.21	1.73	1.79	
			500K	3.23	3.29	3.38	2.14	1.67	1.73	
			125K	3.13	3.20	3.28	2.09	1.62	1.68	

1. All I/O pins are in input mode; V_{DD} or V_{SS} is a static value (no load).
2. All peripherals are disabled, unless otherwise specified.
3. The flash access time conforms to the configuration in the user manual
4. The values are measured when the supply voltage is 3.3V.
5. It’s obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division.

Table 18. Maximum Current Consumption in Sleep Mode, with Data Processing Code Running from Internal Flash Memory(1)(2)(3)(4)(5)

Symbol	Parameter	Condition	f_{HCLK}	Enable all Peripherals			Disable all Peripherals			Unit
				-40°C	25°C	85°C	-40°C	25°C	85°C	
I_{DD}	Supply current in operating mode	Internal clock	72MHz	17.50	17.90	18.20	6.29	5.96	6.07	mA
			48MHz	12.10	12.30	12.50	4.72	4.33	4.42	
			24MHz	7.64	7.79	7.94	3.46	3.04	3.11	
			8MHz	4.58	4.66	4.77	2.48	2.03	2.09	
			4MHz	3.83	3.90	4.00	2.28	1.82	1.87	
			2MHz	3.47	3.53	3.62	2.17	1.71	1.76	
			1MHz	3.28	3.35	3.43	2.11	1.65	1.71	
			500K	3.19	3.26	3.34	2.10	1.63	1.68	
			125K	3.13	3.19	3.27	2.08	1.61	1.66	

1. All I/O pins are in input mode; V_{DD} or V_{SS} is a static value (no load).
2. All peripherals are disabled, unless otherwise specified.
3. The flash access time conforms to the configuration in the user manual.
4. The values are measured when the supply voltage is 3.3V.
5. It’s obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division.

Current Consumption of Built-in Peripherals

The current consumption of built-in peripherals is listed in the Table 19. The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static —- V_{DD} or V_{SS} (no load) .
- All peripherals are turned off, unless otherwise specified.
- The values given are calculated by measuring current consumption.
  - All clocks of peripherals are turned off.
  - Only the clock of one peripheral is turned on.
- The ambient temperature and V_{DD} supply voltage are listed in Table 13.

Table 19. Current Consumption of Built-in Peripherals(1)

Built-in Peripheral		Typical Power consumption at 25 °C	Unit	Built-in Peripheral		Typical Power consumption at 25 °C	Unit
AHB	GPIOD	0.12	mA	APB2	TIM14	0.35	mA
	GPIOC	0.13			TIM16	0.38	
	GPIOB	0.12			TIM17	0.43	
	GPIOA	0.15		APB1	WWDG	0.09	
	CRC	0.20			SPI2	1.03	
	DMA	0.36			UART2	0.77	
APB2	DBG	0.04			I2C1	1.19	
	ADC1	0.28			TIM2	0.97	
	TIM1	1.28			TIM3	0.70	
	SPI1	0.97			PWR	0.23	
	COMP	0.20			CRS	0.13	
	SYSCFG	0.09			CAN	1.64	
	UART1	0.78			USB	3.32	

1. f_{HCLK} = 96Mhz; HSI is used as PLL clock source.

5.3.5 External Clock Source Characteristics

High-Speed External Clock Generated by a Crystal/Ceramic Resonator

The high-speed external clock (HSE) may be generated by an oscillator composed of a 2 ~ 24MHz crystal/ceramic resonator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external elements listed in the table below. In application, the resonator and load capacitor must be maximally close to the oscillator pin to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 20. High-Speed External User Clock Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency(1)			8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		15			ns
$C_{in(HSE)}$	OSC_IN input capacitance reactance (1)			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%

Low-Speed External User Clock from External Oscillator Source

The characteristic parameter given in the following table is measured by a low-speed external clock source, and the ambient temperature and supply voltage conform to the general operating condition.

Table 21. Low-Speed External User Clock Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency(1)		16	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$	OSC32_IN rise time(1)				50	ns
$t_{f(LSE)}$	OSC32_IN fall time (1)				50	ns
$C_{in(LSE)}$	OSC32_IN input capacitive reactance(1)				10	pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-1		1	μA

1. Guaranteed by design, not tested in production.

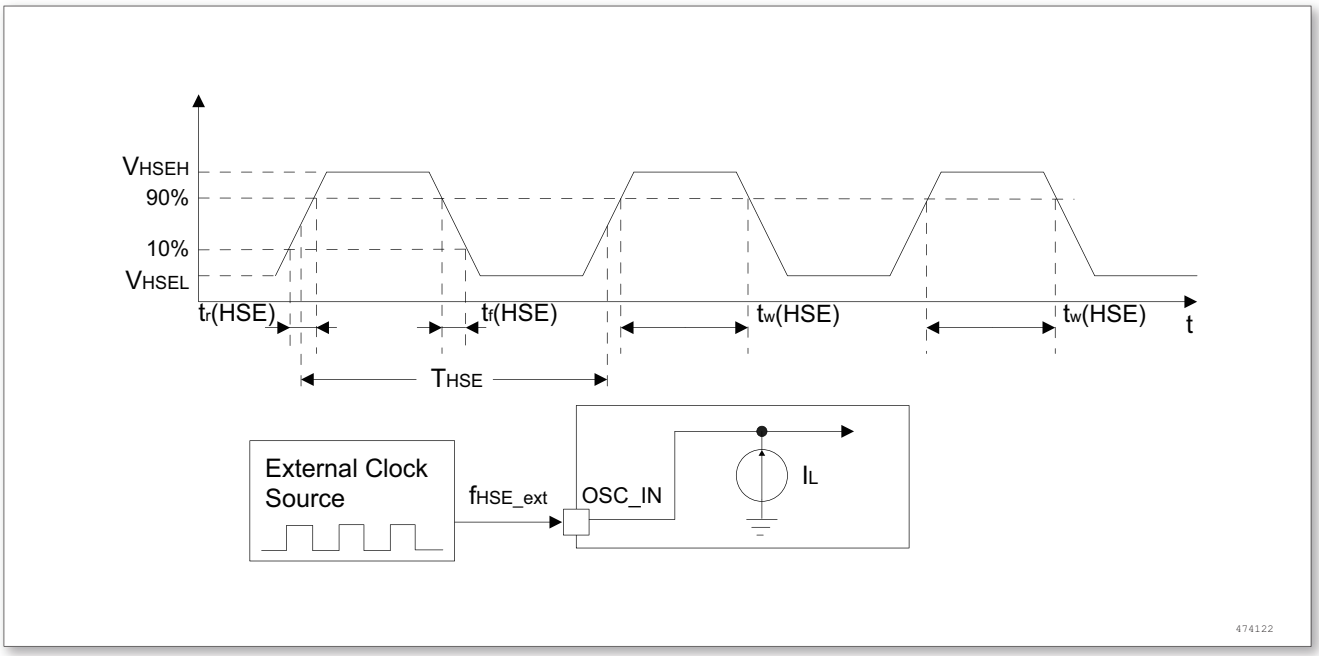

Figure 11. AC Timing Diagram of High-Speed External Clock Source

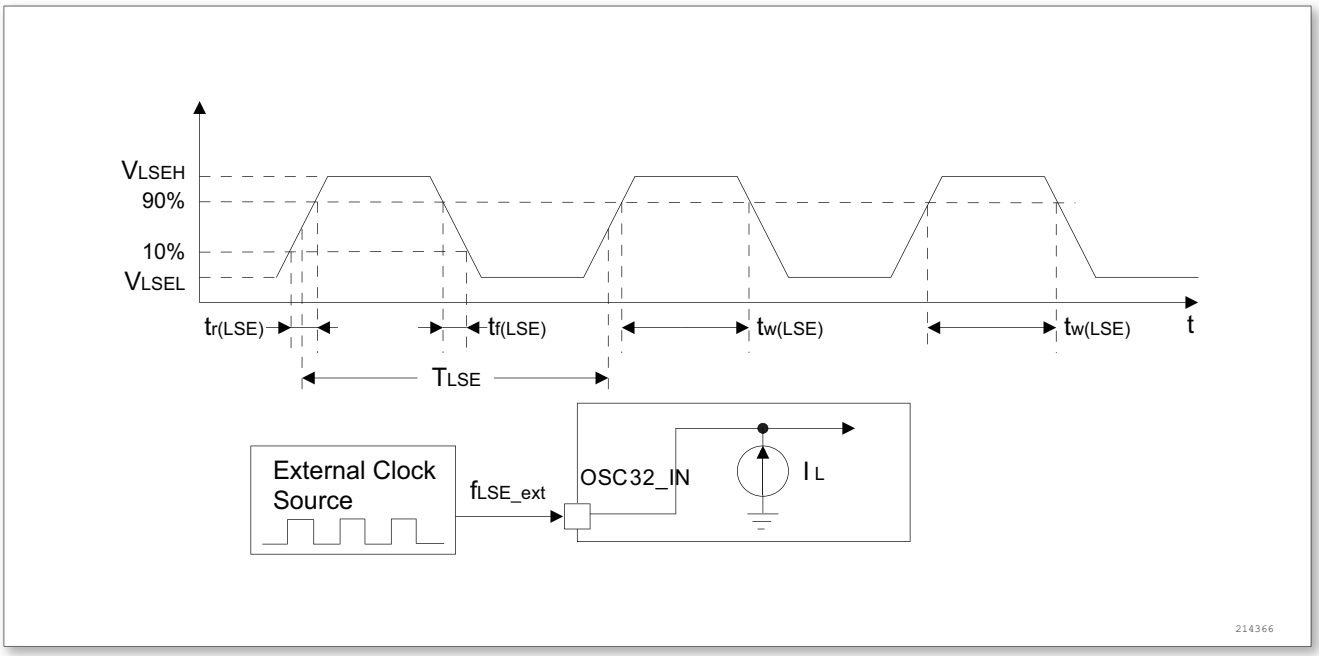

Figure 12. AC Timing Diagram of Low-Speed External Clock Source

High-Speed External Clock Generated by a Crystal/Ceramic Resonator

The high-speed external clock (HSE) may be generated by an oscillator composed of a 2 ~ 24MHz crystal/ceramic resonator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external elements listed in the table below. In application, the resonator and load capacitor must be maximally close to the oscillator pin to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal

resonator, please consult the corresponding manufacturer.

Table 22. HSE 2 ~ 24MHz Oscillator Characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	2.0V<VDD<3.6V	2	8	24	MHz
		3.0V<VDD<5.5V	8	16	24	
R_F	Feedback resistance(4)			510		kΩ
ESR	Support crystal serial impedance ($C_{L1}C_{L2}$(3) is 16pF)	f_{OSC_IN} = 24M V_{DD} = 3.0V			60	Ω
		f_{OSC_IN} = 12M V_{DD} = 2.0V			150	
I_2	HSE driving current	f_{OSC_IN} = 24M V_{DD} = 2.0V ESR=30Ω $C_{L1}C_{L2}$(3) is 20pF		1.5		mA
g_m	Oscillator transconductance	Start up		9		mA/V
$t_{SU(HSE)}$(5)	Start time	V_{DD} is stabe		3		ms

1. The characteristic parameter of the resonator is given by the crystal/ceramic resonator manufacturer.
2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use 5pF ~ 25pF (typical value) high-quality ceramic capacitor designed for high-frequency applications, as well as crystal or resonator that meets the requirements. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the combined pin and the PCB board capacitance can be roughly estimated as 10pF).
4. The relatively low R_F resistance value can provide protection and avoid problems when operating in a humid environment. The leakage and bias conditions generated in this environment have changed. However, if the MCU is used in harsh humid conditions, such parameters need to be taken into account in the design.
5. $t_{SU(HSE)}$ is the start-up time, measured from the moment when the software enables HSE until a stable 8MHz oscillation is obtained. This value is drawn based on readings on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

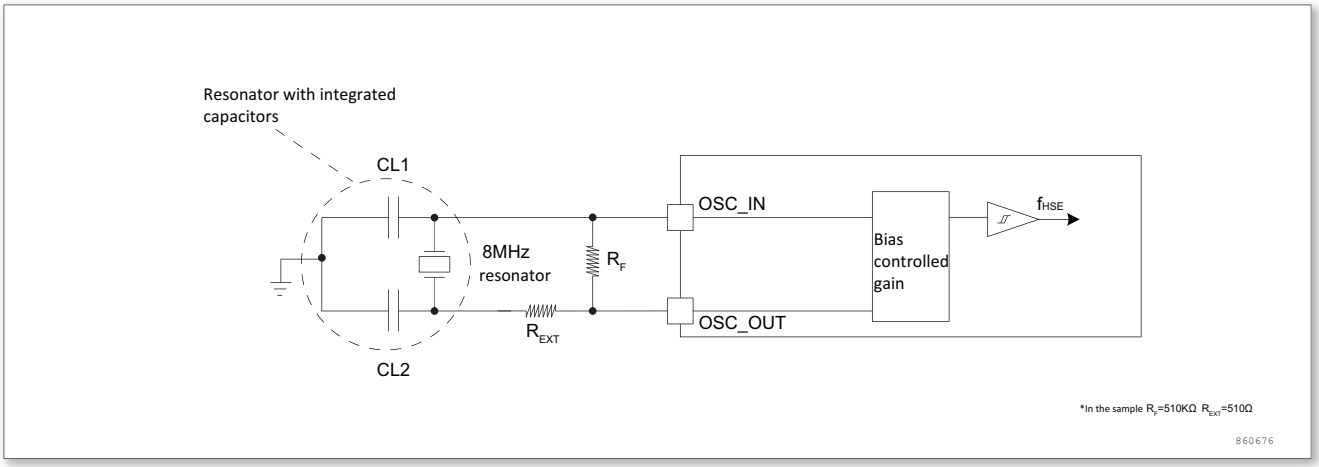

Figure 13. Typical Application with an 8MHz Crystal

Low-Speed External Clock Generated by a Crystal/Ceramic Resonator

The low-speed external clock (LSE) may be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external elements listed in the table below. In application, the resonator and load capacitor must be maximally close to the oscillator pin to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer. (The crystal resonator mentioned here refers to quartz crystal resonator by general speaking.) Note: For C_{L1} and C_{L2}, it is recommended to use 5pF ~ 15pF high-quality ceramic capacitor, as well as crystal or resonator that meets the requirements. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}. Load capacitance CL has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and PCB board or PCB-related capacitance. Typically, it is between 2pF and 7pF. Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2}(15pF),it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$pF. Never use a resonator with a load capacitance of 12.5pF. Example: if a resonator with a load capacitance of CL = 6pF, and Cstray = 2pF is chosen, then $C_{L1} = C_{L2} = 8$pF.

Table 23. LSE Oscillator Characteristics (f_{LSE}=32.768KHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
g_m	Oscillator transconductance			78		μA/V
$t_{SU(LSE)}$ (2)	Start time	R_S = 30kΩ		3		S

1. Drawn from comprehensive evaluation, not tested in production.
2. $t_{SU(LSE)}$ is the start-up time, measured from the moment when the software enables LSE until a stable 32.768KHz oscillation is obtained. This value is drawn based on

readings on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

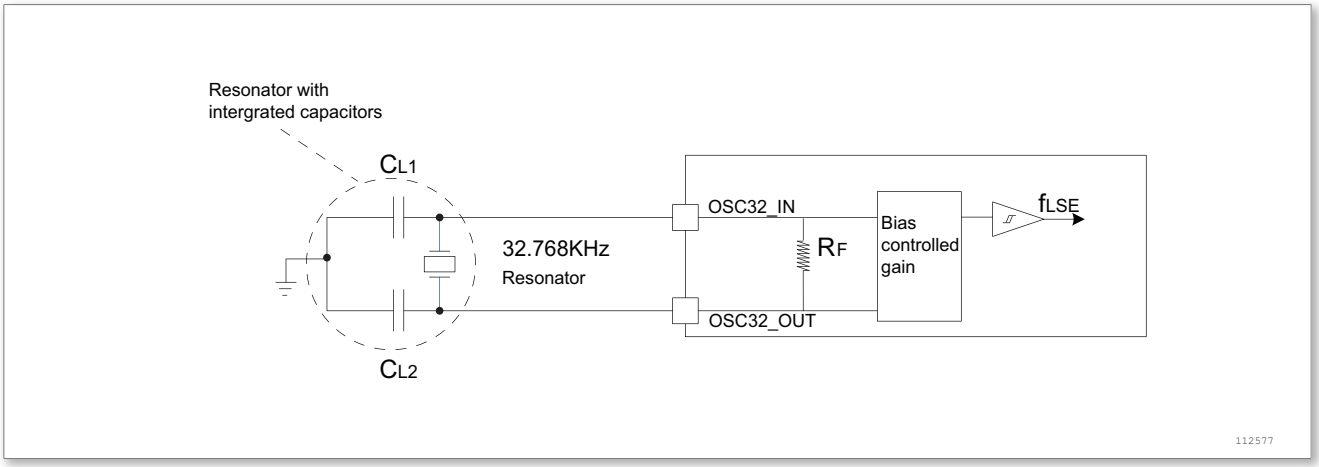

Figure 14. Typical application with a 32.768 kHz Crystal

5.3.6 Internal Clock Source Characteristics

The characteristic parameter given in the following table is measured when ambient temperature and power supply voltage meet with the general operating condition.

High-Speed Internal (HSI) Oscillator

Table 24. HSI Oscillator Characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			48		MHz
ACC_{HSI}	HSI oscillator accuracy	T_A = 25°C	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time			12	16	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			328		μA

1. V_{DD} = 3.3V, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-Speed Internal (LSI) Oscillator

Table 25. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency			40		KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				85	μs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1	1.4	μA

1. V_{DD} = 3.3V,unless otherwise specified.

2. Drawn from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up Time from Low-Power Mode

The wake-up time listed in the following table is measured during the wake-up phase of the Internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times are measured when ambient temperature and supply voltage meet the general operating condition.

Table 26. Wake-up Time in Low Power Mode

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$(1)	Wake up from sleep mode	HSI is the system clock	2.7	μs
t_{WUSTOP}(1)	Wake up from shutdown mode (voltage regulator in operation)	HSI is the system clock	5.5	μs
t_{WUSTOP}(1)	Wake up from shutdown mode (voltage regulator in low power mode)	HSI is the system clock	7.7	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x00	498	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x01	430	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x02	390	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x03	318	μs

1. The wake-up time measurement starts from the wake-up event to the point at which the user application code reads the first instruction.

5.3.7 PLL Characteristics

The characteristic parameter listed in the following table is measured when ambient temperature and power supply voltage meet with the general operating condition.

Table 27. PLL Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	4		24	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	40		200	MHz
t_{LOCK}	PLL lock time			100	μs

1. Guaranteed by design, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock frequency compatible with the range defined by f_{PLL_OUT}.

5.3.8 Memory Characteristics

Flash memory

Table 28. Flash Memory Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	8-bit programming time		6		7.5	μS
t_{ERASE}	Page erasing time		4		5	mS
t_{ME}	Mass erasing time		20		40	mS
I_{DD}	Supply current	Readig mode		4		mA
		Writing mode			7	mA
		Erasing mode			2	mA
V_{prog}	Programming voltage			1.5		V

Table 29. Flash Memory Life and Data Retention Period(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Life (erasing and writing times)		20			Thousand times
t_{RET}	Data retention period	T_A = 25°C	100			Year

1. Drawn from comprehensive evaluation, not tested in production.

5.3.9 EMC Characteristics

Sensitivity testing is carried out by sampling during product comprehensive evaluation.

Design Reliable Software to Avoid Noise

EMC evaluation and optimization at the device level are carried out in a typical application environment. It should be noted that good EMC performance is closely related to user applications and specific software.

Therefore, it is recommended that users implement EMC optimization on the software and conduct EMC-related certification tests.

Software Recommendations

The software flow must include the control of program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data destroyed (control registers, etc...)

Test before Certification

Many common failures (unexpected reset and corrupted program counter) can be reproduced by manually introducing a low level on NRST or introducing a 1-second low level on the crystal oscillator pin.

During ESD test, a voltage exceeding the application requirement can be directly applied to the chip. When an unexpected action is detected, the software needs to be strengthened to prevent unrecoverable errors.

5.3.10 Absolute Maximum Value (Electrical Sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to conduct a strength test on the chip to determine its electrical sensitivity performance.

Electrostatic Discharge (ESD)

Electrostatic discharge (a positive pulse and then a negative pulse after one second interval) is applied to all the pins of all samples. The size of the sample is related to the number of power supply pins on the chip (3 pieces × (n+1) power supply pins). This test complies with the standard JEDEC JS-001-2017/JS-002-2018.

Static Latching

In order to evaluate the latch performance, 2 complementary static latching tests need to be performed on 6 samples:

- Provide a supply voltage exceeding the limit for each power supply pin.
- Inject current into each input, output, and configurable I/O pin.

This test complies with the EIA/JESD78E integrated circuit latching standard.

Table 30. MCU ESD Characteristics

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C, compliance with JEDEC	±8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = 25°C, compliance with JEDEC	±2000	
I_{LU}	Static latching (Latch-up current)	T_A = 25°C, compliance with JESD78E	100	mA

5.3.11 I/O Port Characteristics

General Input/Output Characteristics

Unless otherwise specified, the parameter listed in the table below is measured according to the condition in Table 11All I/O ports are compatible withCMOS.

Table 31. I/O Static Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 3.3V	-0.3		0.8	V
		V_{DD} = 5.0V	-0.3		$0.3V_{DD}$	
V_{IH}	Input high level voltage	V_{DD} = 3.3V	2		3.3	V
		V_{DD} = 5.0V	$0.7V_{DD}$	5	V_{DD}+0.3	
V_{hys}	I/O pin Schmitt trigger voltage hysteresis(1)	V_{DD} = 3.3V			$0.3V_{DD}$	V
		V_{DD} = 5.0V			0.8	
I_{lkg}	Input leakage current(2)	V_{DD} = 3.3V			1	μA
		V_{DD} = 5.0V			1	
R_{PU}	Weak pull-up equivalent resistor(3)	3.3V V_{IN}=V_{SS}	22		100	kΩ
		5.0V V_{IN}=V_{SS}	22		100	
R_{PD}	Weak pull-down equivalent resistor(3)	3.3V V_{IN}=V_{SS}	20		50	kΩ
		5.0V V_{IN}=V_{SS}	20		50	
C_{IO}	I/O pin capacitance	V_{DD} = 3.3V			10	pF
		V_{DD} = 5.0V			10	

1. The hysteresis voltage of Schmitt trigger switching level. Drawn from comprehensive evaluation, not tested in production.
2. In case of reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are MOS resistors.

Output Driving Current

GPIO (General Purpose Input/Output Port) can input or output up to ±20mAcurrent.

In user applications, the number of I/O pins must ensure that the driving current cannot exceed the absolute maximum ratings given in section 5.2：

- The sum of the current drawn by all I/O ports from V_{DD} plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the current drawn by all I/O ports and output from V_{SS}, plus the maximum operating current output by the MCU on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output Voltage

Unless otherwise specified, the parameter listed in the table below is measured by the ambient temperature and supply voltage V_{DD} in accordance with the condition in Table 13.All I/O ports are compatible with CMOS.

Table 32. Output Voltage Characteristics(1)(2)

MODEx[1：0] configuration	Symbol	Parameter	Conditions	Unit	
11	V_{OL}	Output low level	I_{15-50} = 8mA	0.4	V
	t_{OH}	Output high level	V_{DD}=3.3V	V_{DD}-0.4	
	V_{OL}	Output low level	I_{IO} = 20mA	0.3*V_{DD}	
	t_{OH}	Output high level	V_{DD} = 3.3V	0.6*V_{DD}	
	V_{OL}	Output low level	I_{IO} = 6mA	0.4	
	t_{OH}	Output high level	V_{DD} = 3.3V	V_{DD}-0.4	
10	V_{OL}	Output low level	I_{IO} = 8mA	0.4	
	t_{OH}	Output high level	V_{DD} = 3.3V	V_{DD}-0.4	
	V_{OL}	Output low level	I_{IO} = 20mA	0.2*V_{DD}	
	t_{OH}	Output high level	V_{DD} = 3.3V	0.8*V_{DD}	
	V_{OL}	Output low level	I_{IO} = 6mA	0.4	
	t_{OH}	Output high level	V_{DD} = 3.3V	V_{DD}-0.4	
01	V_{OL}	Output low level	I_{IO} = 8mA	0.4	
	t_{OH}	Output high level	V_{DD} = 3.3V	V_{DD}-0.4	
	V_{OL}	Output low level	I_{IO} = 20mA	0.2*V_{DD}	
	t_{OH}	Output high level	V_{DD} = 3.3V	0.8*V_{DD}	
	V_{OL}	Output low level	I_{IO} = 6mA	0.4	
	t_{OH}	Output high level	V_{DD} = 3.3V	V_{DD}-0.4	

1. Drawn from comprehensive evaluation, not tested in production.

Input and Output AC Characteristics

The definitions and values of the input and output AC characteristics are shown in figure 15 and Table 33, respectively.

Unless otherwise specified, the parameter listed in Table 33 is measured by the ambient temperature and supply voltage in accordance with the condition in Table 11.

Table 33. Input and Output AC Characteristics (1)(2)

MODEx [1:0] configuration	Symbol	Parameter	Conditions	Typ	Unit
11	$t_{f(IO)out}$	Output fall time	C_L=50pF, V_{DD}=3.3V	7.20	ns
	$t_{r(IO)out}$	Output rise time		7.20	
10	$t_{f(IO)out}$	Output fall time		4.40	
	$t_{r(IO)out}$	Output rise time		4.40	
01	$t_{f(IO)out}$	Output fall time		3.73	
	$t_{r(IO)out}$	Output rise time		3.73	

1. I/O port speed can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in this manual.
2. Guaranteed by design, not tested in production.

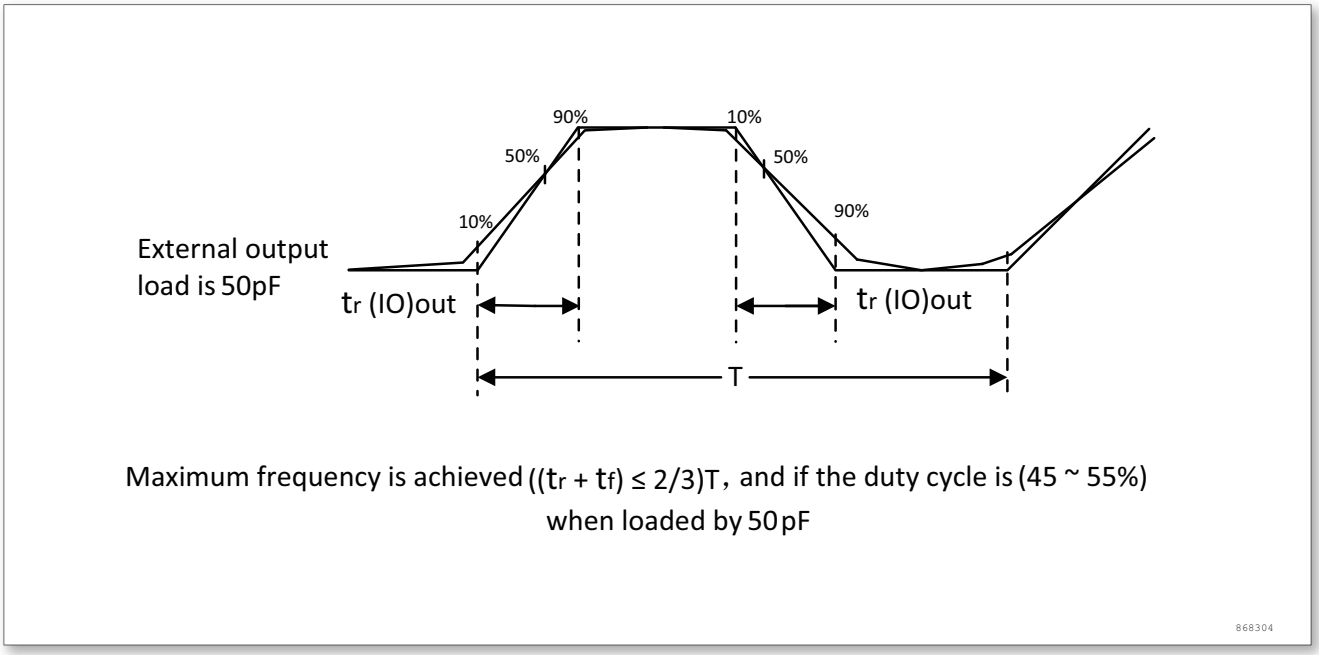

Figure 15. Definiton of I/O AC characteristics

5.3.12 NRST pin Characteristics

NRST pin input driver uses CMOS technology, and it is connected with a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameter listed in the table below is measured by the ambient temperature and supply voltage V_{DD} in accordance with the condition in Table 13.

Table 34. NRST Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.3		0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		2		5.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		0.1*V_{DD}			V
R_{PU}	Weak pull-up equivalent resistor(2)	V_{IN} = V_{SS}	22		100	kΩ
$V_{F(NRST)}$ (1)	NRST input filter pulse				1000	ns
$V_{NF(NRST)}$ (1)	NRST input unfilter pulse		4000			ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is MOS resistor.

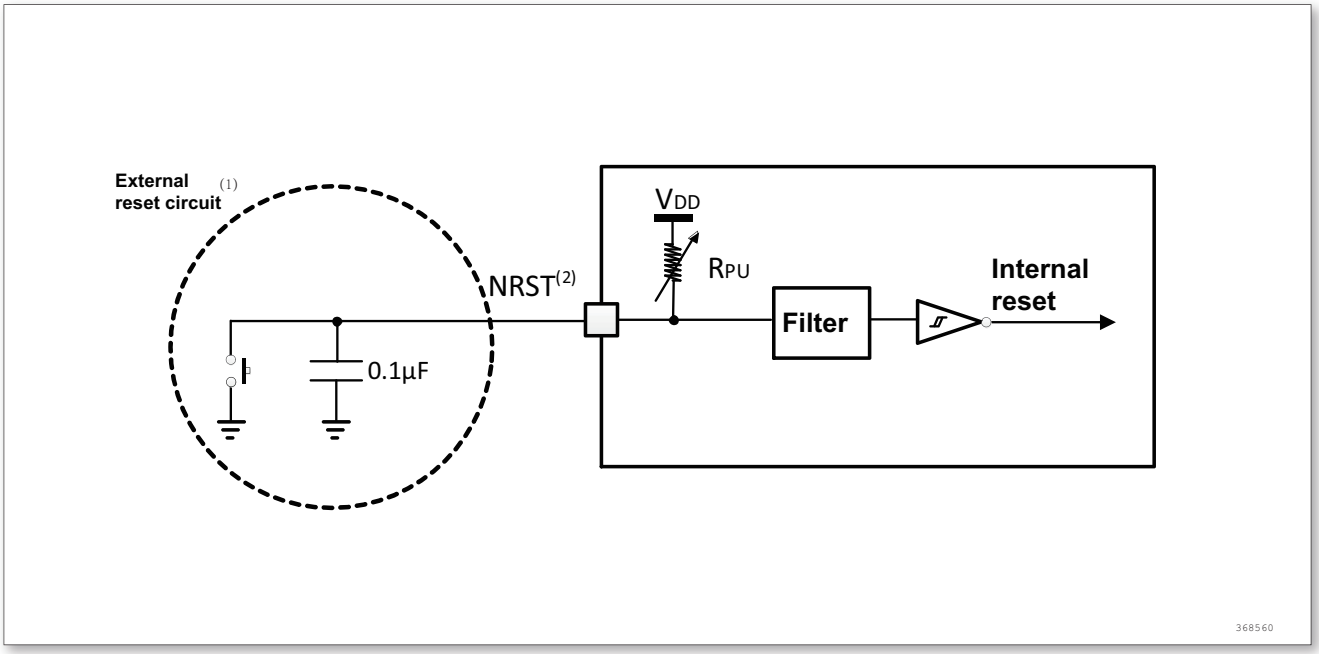

Figure 16. Recommended NRST Pin Protection

1. The reset network is to prevent parasitic reset.
2. The user must ensure that the NRST pin voltage can be lower than the maximum $V_{IL(NRST)}$ listed in Table 34,otherwise the MCU cannot be reset.

5.3.13 TIM Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input/output multiplex function pins (output comparison, input capture, external clock, PWM output), see subsubsec 5.3.11.

Table 35. TIMx(1) Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$=96MHz	10.4		ns
f_{EXT}	CH1 to CH4 timer external clock frequency		0	$f_{TIMxCLK/2}$	MHz
		$f_{TIMxCLK}$=96MHz	0	48	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16-bit counter clock cycle when selecting the internal clock	1	65536	$t_{TIMxCLK}$	
		$f_{TIMxCLK}$=96MHz	0.0104	682.6	
t_{MAX_COUNT}	Maximum possible count			65536 ×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=96MHz		44.7	S

1. TIMx is a generic name.

5.3.14 Communication Interface

I2C

Unless otherwise specified, the parameters listed in Table 36 are measured when the ambient temperature,f_{PCLK1}frequency and and V_{DD} supply voltage meet the condition of Table 13.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: SDA and SCL are not ”true” pins. When it’s configured as open-drain output, the PMOS tube between the pin and V_{DD} is turned off, but it still exists.

I2C interface characteristics are listed in Table 36, For details on the characteristics of input/output multiplex function pins (SDA and SCL), see subsubsec 5.3.11.

Table 36. I2C Characteristics

Symbol	Parameter	Standard I2C(1)		Quick I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	$8*t_{PCLK}$		$8*t_{PCLK}$		μs
$t_{w(SCLH)}$	SCL clock high time	$6*t_{PCLK}$		$6*t_{PCLK}$		μs
$t_{su(SDA)}$	SDA establishment time	$2*t_{PCLK}$		$2*t_{PCLK}$		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	875(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000		300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	$8*t_{PCLK}$		$8*t_{PCLK}$		μs
$t_{su(STA)}$	Repeated start condition setup time	$6*t_{PCLK}$		$6*t_{PCLK}$		

Symbol	Parameter	Standard I2C(1)		Quick I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{su(STO)}$	Stop condition setup time	$6*t_{PCLK}$		$6*t_{PCLK}$		μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (Bus Free)	$5*t_{PCLK}$		$5*t_{PCLK}$		
C_b	Capacitive load of each bus		4.7		1.2	pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of standard mode I2C,f_{PCLK1}must be greater than 3MHz. To reach the maximum frequency of quick mode I2C,f_{PCLK1} must be greater than 12MHz.
3. If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the start condition needs to be met.
4. In order to cross the undefined area of the falling edge of SCL, a hold time of at least 300nS on the SDA signal must be guaranteed inside the MCU.

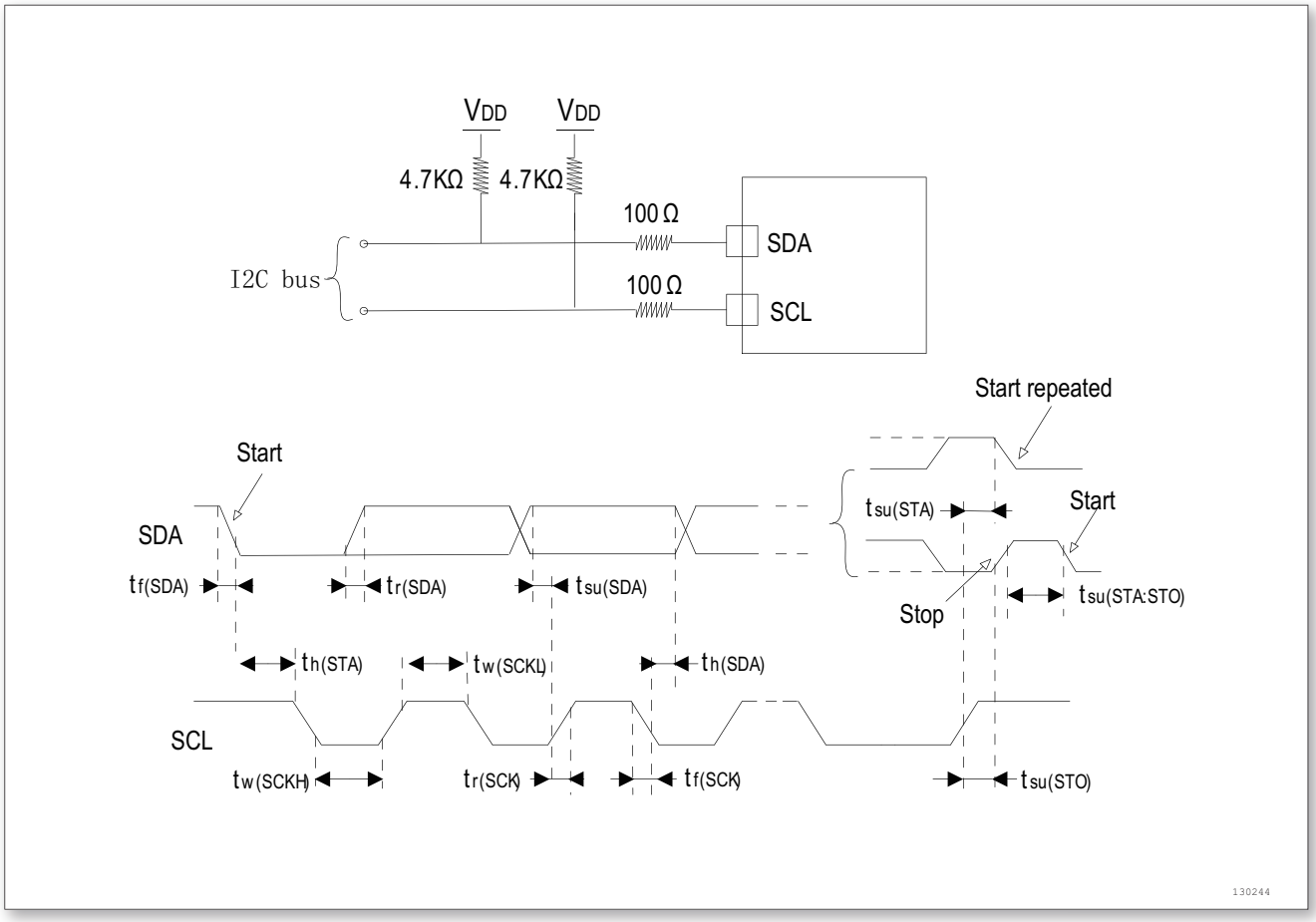

Figure 17. I2C Bus AC Waveform and Measurement Circuit(1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

SPI Interface Characteristics

Unless otherwise specified, the parameters listed inTable 37 are measured when ambient

temperature, f_{PCLKx} frequency and V_{DD} supply voltage meet the condition in Table 13.

For details on the characteristics of input/output multiplex function pins (NSS, SCK, MOSI, MISO), see subsubsec 5.3.11.

Table 37. SPI Characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	24	MHz
		Slave mode	0	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 15pF		6	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	$1T_{PCLK}$		ns
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	$2T_{PCLK}$		ns
$t_{w(SCKH)}$(2)	SCK high time		$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$- 6	ns
$t_{w(SCKL)}$(2)	SCK low time		$t_{c(SCK)/2}$- 6	$t_{c(SCK)/2}$- 6	ns
$t_{su(MI)}$(2)	Data input setup time	Master mode, fPCLK= 48MHz, prescale coefficient = 2 high-speed mode	12		ns
$t_{su(SI)}$(2)	Data input setup time	Slave mode	5		ns
$t_{h(MI)}$(2)	Data input hold time	Master mode, fPCLK= 48MHz, prescale coefficient = 2 highspeed mode	0		ns
$t_{h(SI)}$(2)		Slave mode	6		
$t_{v(SO)}$(2)(1)	Data output valid time	Slave mode (after enabling edge) non-highspeed mode		34	ns
$t_{h(SO)}$(2)		Slave mode (after enabling edge) highspeed mode		13	
$t_{h(MO)}$(2)	Data output valid time	Master mode (after enabling edge)	-0.6	2	ns

1. Drawn from comprehensive evaluation, not tested in production.
2. Minimum value indicates the drive output minimum time, and maximum value indicates the maximum time to obtain data correctly.
3. Minimum value represents the minimum time to close output, and maximum value represents the maximum time to put the data line in the high impedance state.

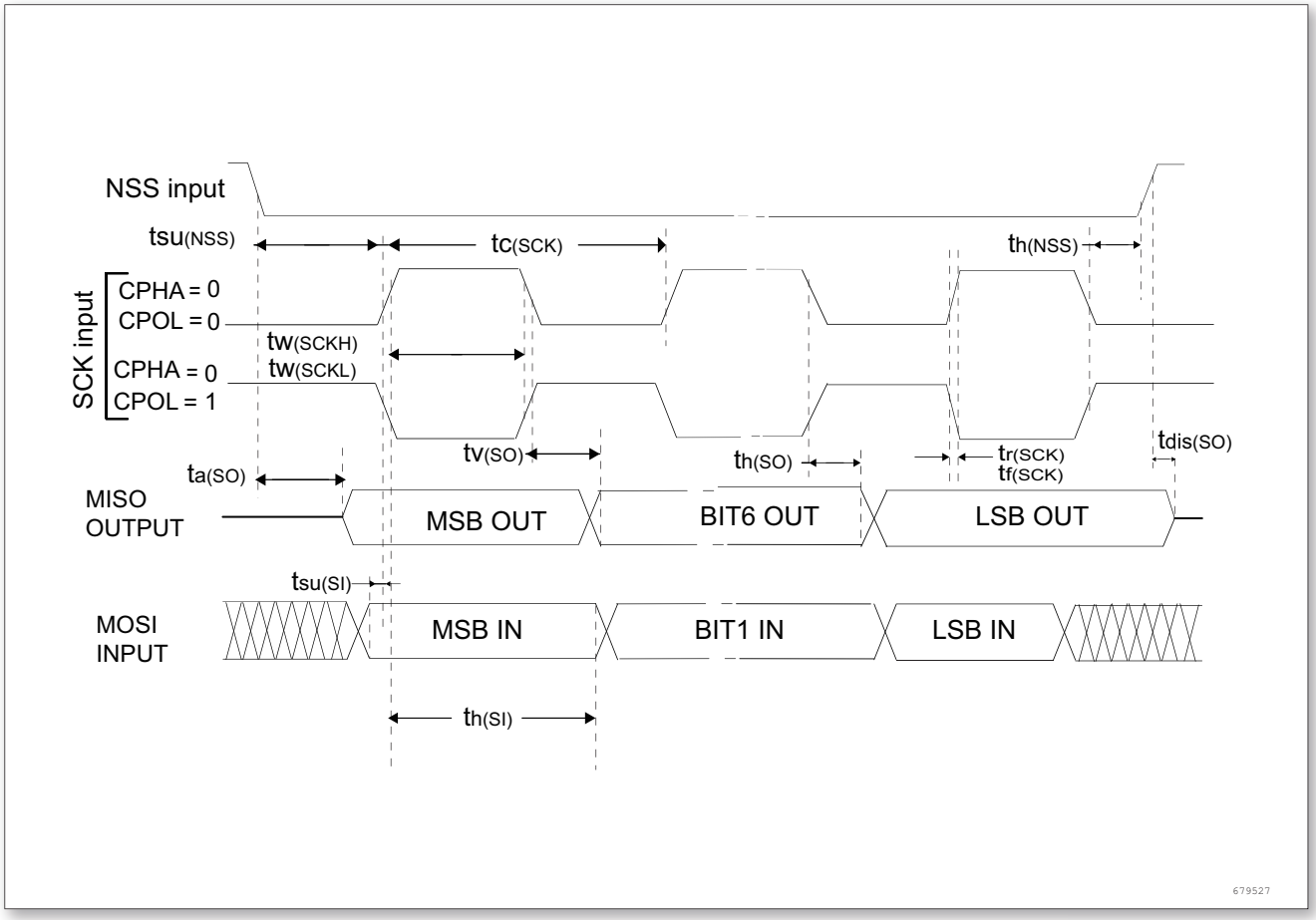

Figure 18. SPI Timing Diagram-Slave Mode and CPHA = 0

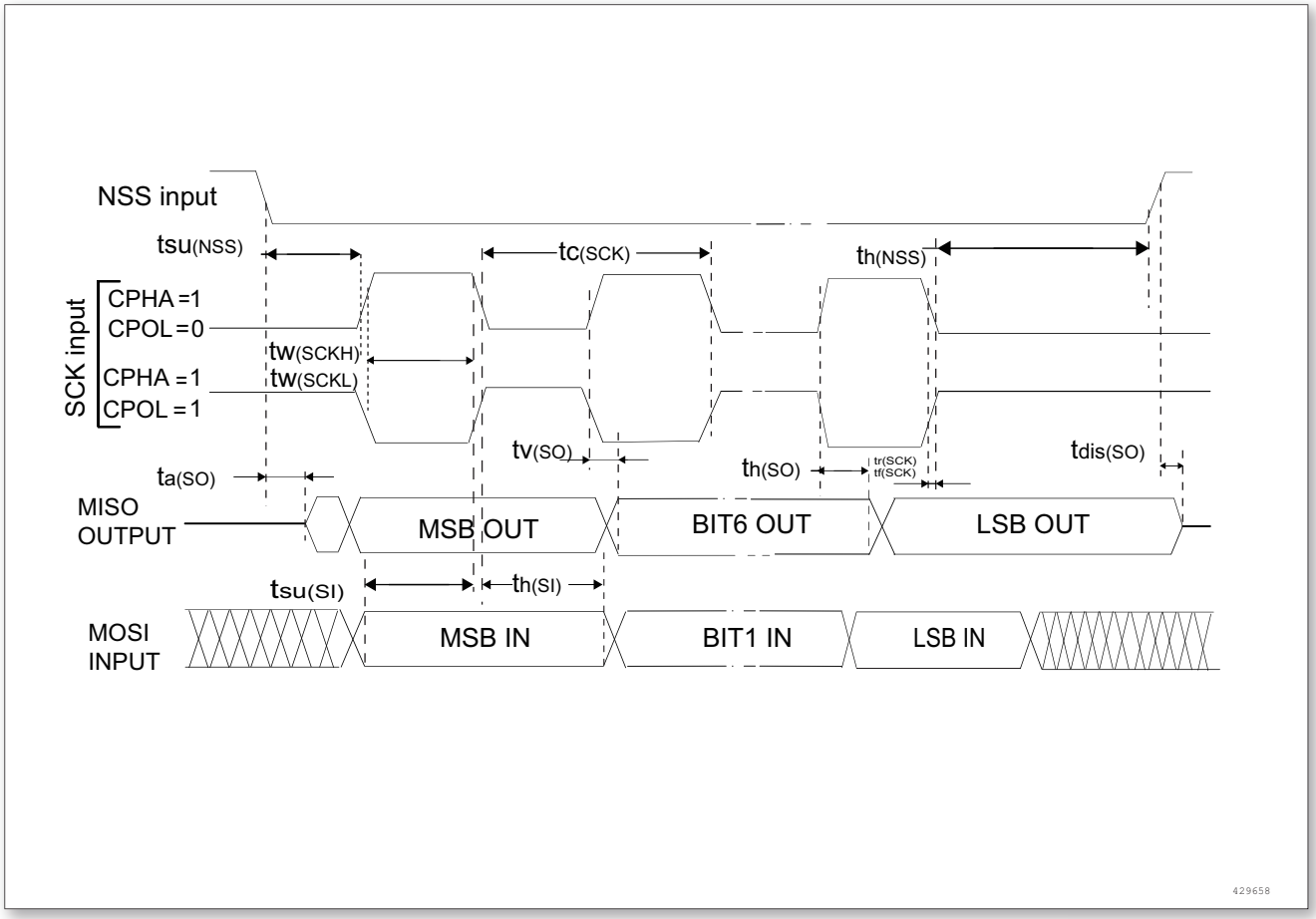

Figure 19. SPI Timing Diagram-Slave Mode and CPHA = 1(1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

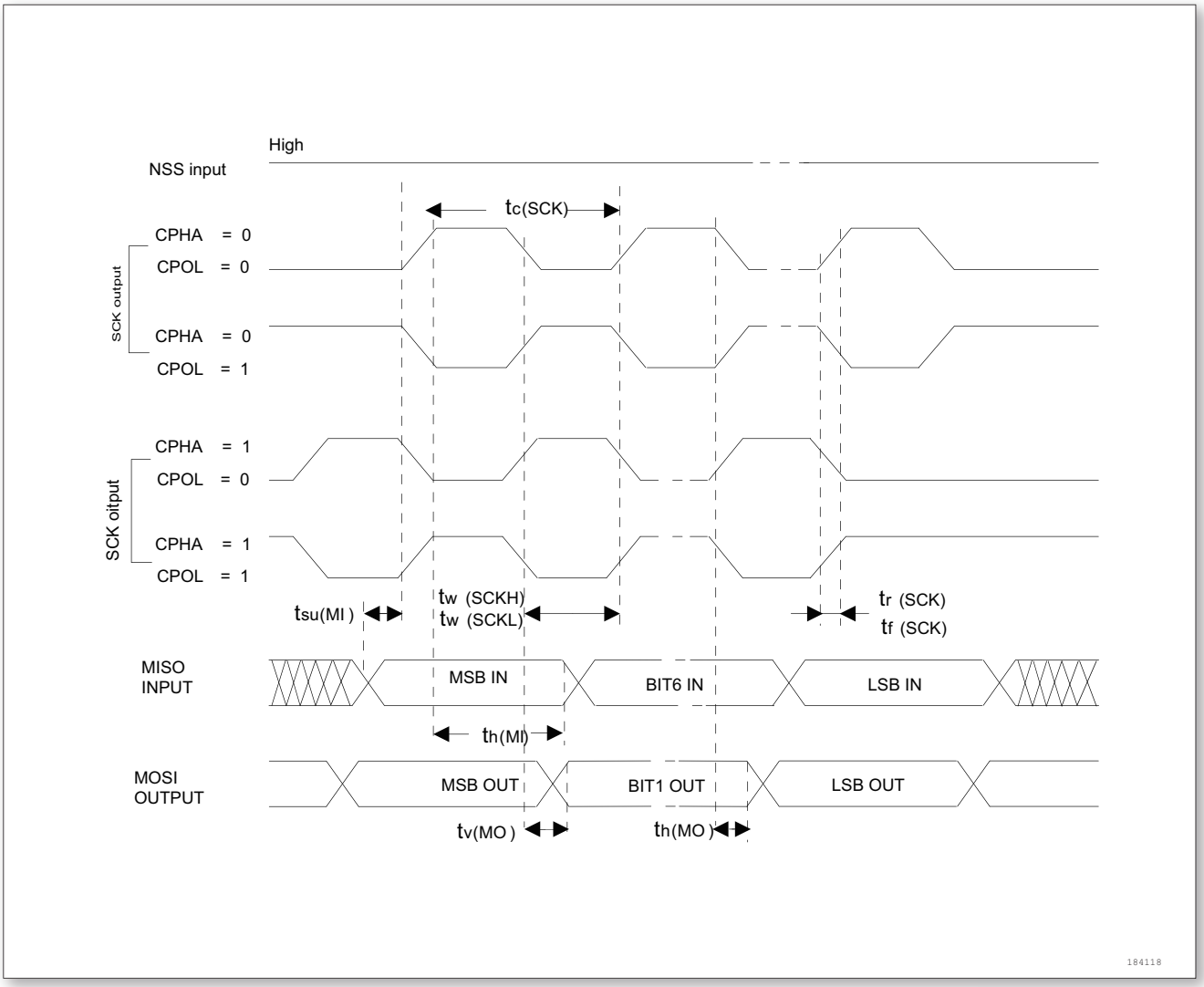

Figure 20. SPI Timing Diagram-Master Mode(1)

1. The measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

USB Characteristics

Table 38. USB DC Characteristics(1)

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
Input Level					
V_{DD}	USB operating voltage(2)		3.0	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP, USBDM)	0.2		
V_{CM}(4)	Range of differential common mode	Include V_{DD}range	0.8	2.5	
V_{SE}(4)	Single-end receiver threshold		1.3	2	
Output Level					

Symbol	Parameter	Conditions	Min(1)	Max(1)	Unit
V_{OL}	Static output low level	1.5k ω R_L connected to 3.6V(5)		0.3	V
V_{OH}	Static output high level	1.5k ω R_L connected to V_{SS}(5)	2.8	3.6	

1. All voltage measurements shall be made on the ground wire of the device.
2. To be compatible with USB 2.0 full-speed electrical specification, the USBDP(D+) pin has built in a 1.5 kω resistor.
3. The normal USB function of the product can be guaranteed at 2.7V. Instead of that, electrical characteristics will degrade between 2.7V and 3.6V voltage.
4. Guaranteed by comprehensive evaluation, not tested in production.
5. R_L is the load attached to the USB drive.

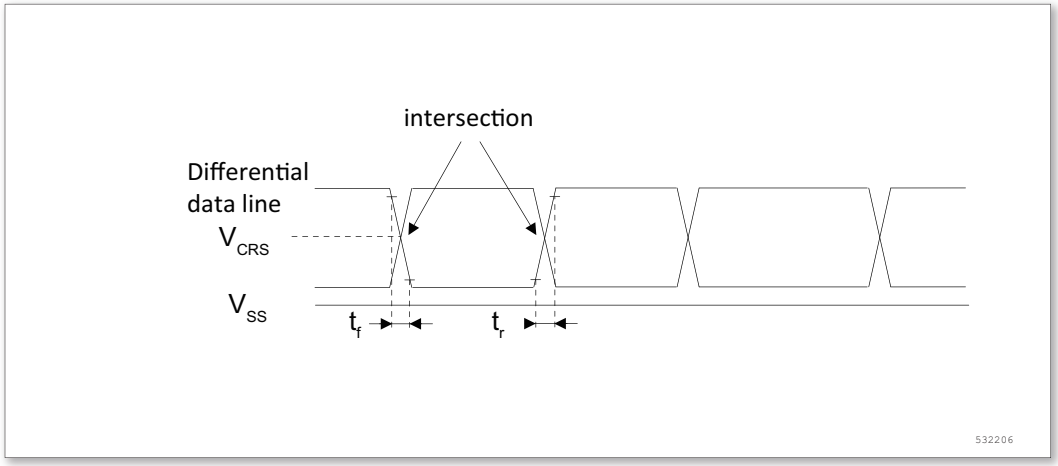

Figure 21. USB Timing: Definition of Data Signal Rise and Fall Times

5.3.15 CAN (Controller Area Network) Interface

For details on the characteristics of input/output multiplex function pins (CAN_TX and CAN_RX), seesubsubsec 5.3.11

5.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters in the following table are measured when ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage meet the condition of Table 13.

Table 39. ADC Characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit
V_{DDA}	Supply voltage		2.5	3.3	5.5	V
f_{ADC}(1)(3)	ADC clock frequency				16	MHz
f_S(1)(3)	Sampling rate				1	MHz

Symbol	Parameter	Conditions	Min	Type	Max	Unit
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 15MHz			937.5	KHz
f_{TRIG}(1)	External trigger frequency				16	$1/f_{ADC}$
V_{AIN}(2)	Conversion voltage range(3)		0		V_{DD}	V
R_{AIN}(1)	External input impedance		See Equation 1 and Table 40			K ω
R_{ADC}(1)	Sampling switch resistance				1.5	Kω
C_{ADC}(1)	Internal sample and hold capacitor				10	pF
t_S(1)	Sampling time	f_{ADC} = 16MHz	0.156		15.031	μs
			2.5		240.5	$1/f_{ADC}$
t_{conv}(1)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	1		15.8125	μs
			15 ~ 253 (sampling t_{S+}) stepwise approximation to 12.5			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this series of products, V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times In(2^{N+2})} - R_{ADC} \quad (1)$$

The above Equation 1 is used to determine the maximum external impedance so that the error can be less than 1/4 LSB, where N = 12 (representing 12-bit resolution).

Table 40. Max R_{AIN} for f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	Max R_{AIN}(kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

Table 41. ADC Accuracy - Limited Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit
Resolution	Resolution		12		BIT
ET	Composite error	f_{PCLK2} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1K ω, V_{DDA} = 3.3V， T_A = 25°C	3.4/-2.3		LSB
EO	Offset error		-2.5		
EG	Gain error		3.7		
ED	Differential linearity error		1/-1		
EL	Integral linearity error		1.8/-3		

1. Correlation between ADC accuracy and reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, because this will significantly reduce the accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current.
   If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in subsub-sec 5.3.12 it will not affect the ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: the maximum deviation between any actual conversion and the endpoint correlation line.

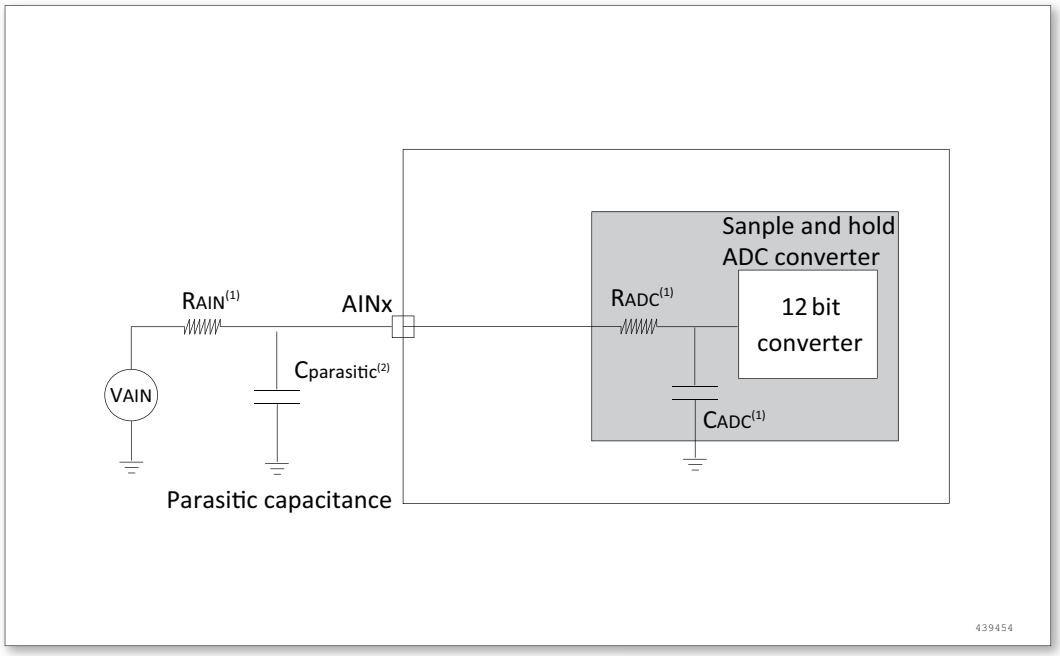

Figure 22. Typical Connection Diagram Using the ADC

1. Refer to Table 41 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ means the parasitic capacitance (about 7pF) on the PCB (related to welding and PCB layout quality) and pad. A larger $C_{parasitic}$ value will reduce the conversion accuracy. The solution is to reduce f_{ADC} .

PCB Design Proposals

The power supply decoupling must be connected according to the diagram below. The 10 nF capacitor in the diagram must be ceramic capacitors, which should be maximally close to the MCU chip.

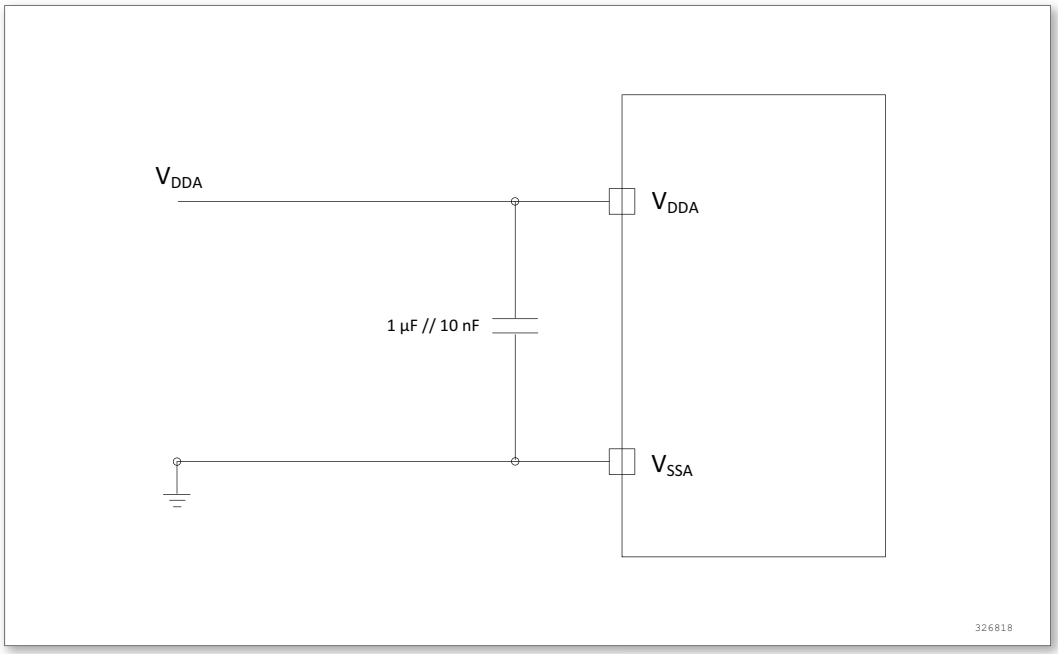

Figure 23. Power Supply and Reference Supply Decoupling Circuit

5.3.17 Temperature Sensor Characteristics

Table 42. Temperature Sensor Characteristics (3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25} (1)	ADC sampling value at 25°C		offset(5)		
t_{start} (2)	Startup time			10	µs
T_{S_temp} (2)	ADC sampling time when reading the temperature	10			µs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.
4. V_{DD} = 3.3V.
5. Temperature formula: TS_adc = 25 + (value * VDDA - offset * 3300)/(4096 * Avg_Slope), where offset is recorded in the low 12 bits of 0x1FFFF7F6 and value is the converted result data of ADC.

5.3.18 Comparator characteristics

Table 43. Comparator characteristics

Symbol	Parameter	Register configuration	Min	Type	Max	Unit
HYST	Hysteresis	00		0		mV
HYST	Hysteresis	01		15		mV
HYST	Hysteresis	10		30		mV
HYST	Hysteresis	11		90		mV
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
OFFSET	Offset voltage	01	3.23	7.51	12.08	mV
OFFSET	Offset voltage	10	9.79	15	20.8	mV
OFFSET	Offset voltage	11	34.25	47.4	62.22	mV
DELAY(1)	Propagation delay	00		80		nS
DELAY(1)	Propagation delay	01		51		nS
DELAY(1)	Propagation delay	10		26		nS
DELAY(1)	Propagation delay	11		9		nS
I_q(2)	Operating current average	00		4.5		uA
I_q(2)	Operating current average	01		4.4		uA
I_q(2)	Operating current average	10		4.4		uA
I_q(2)	Operating current average	11		4.4		uA

1. The time difference between the output switching by 50% and the input switching.
2. The average value of total operating current consumption.

6 Package information

Package information

6.1 Package LQFP64

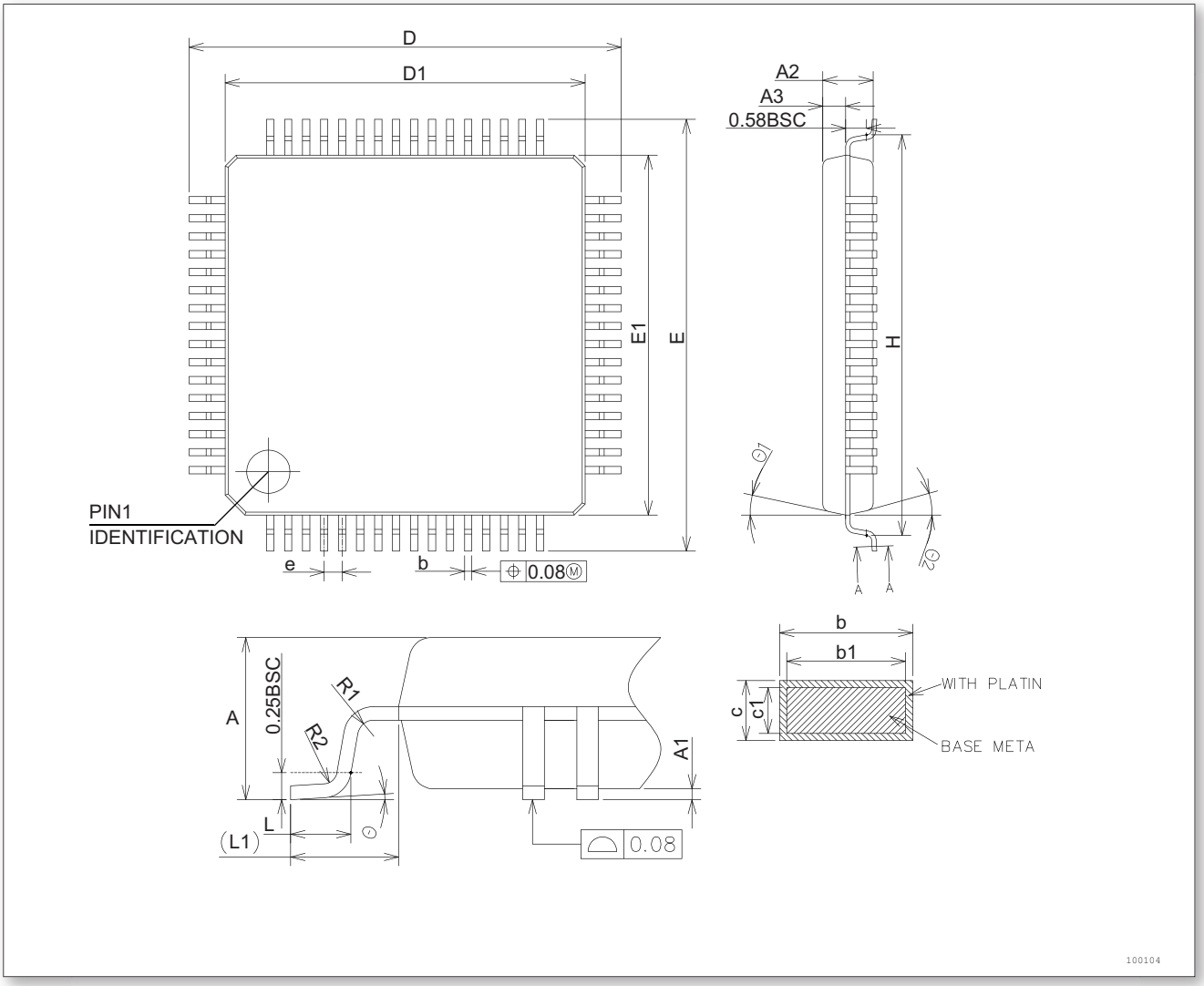

Figure 24. LQFP64, 64-Pin Low-Profile Quad Flat Package Outline

1. The Diagram is not drawn to scale.
2. The size is in mm.

Table 44. LQFP64 Size Description

Lable	Mm		
	Min	Typical	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	-	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.2 Package LQFP48

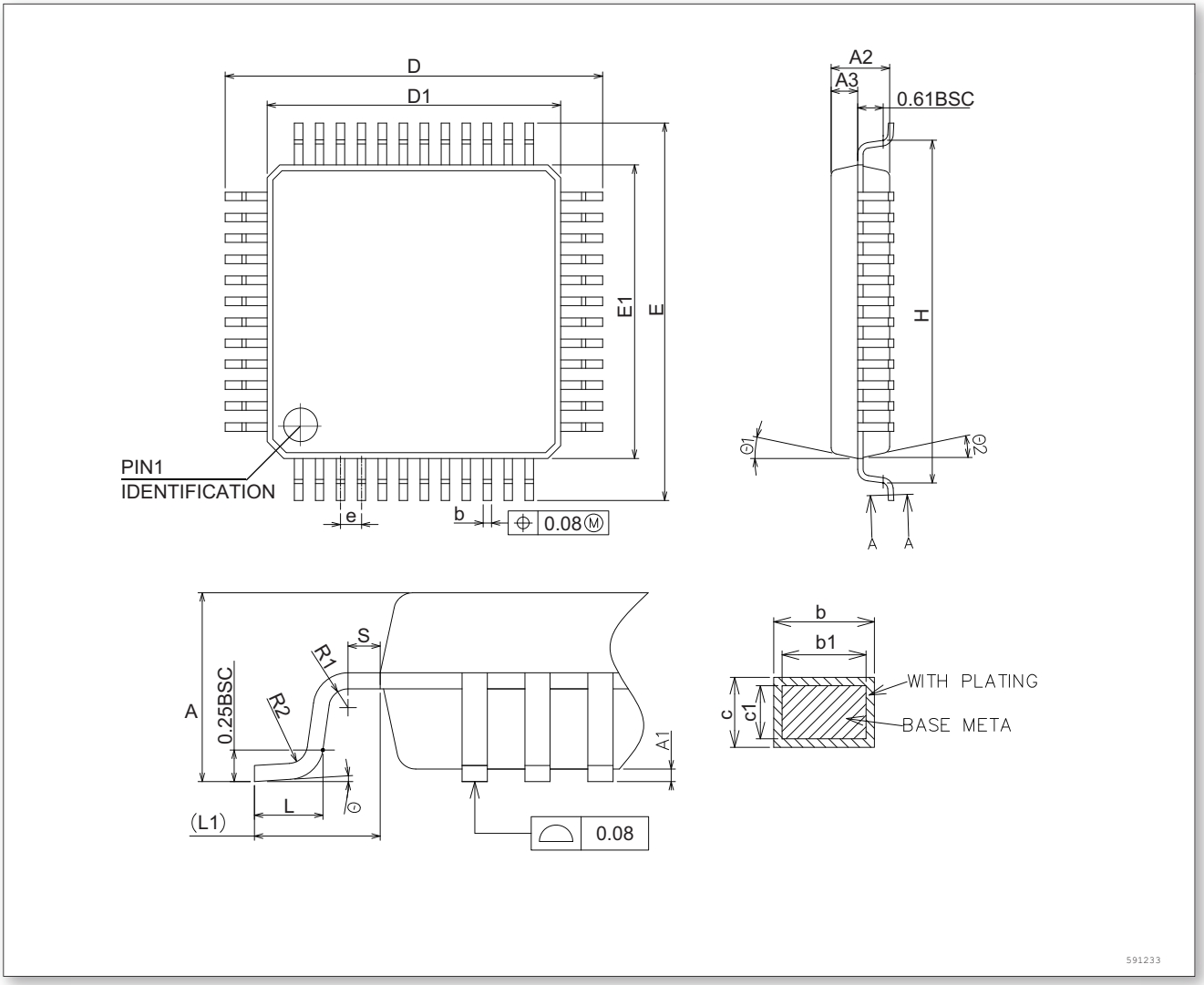

Figure 25. LQFP48, 48-Pin Low-Profile Quad Flat Package Outline

1. The Diagram is not drawn to scale.
2. The size is in mm.

Table 45. LQFP48 Size Description

Lable	Mm		
	Min	Typical	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20

Lable	Mm		
	Min	Typical	Max
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0 °	3.5 °	7 °
θ 1	11 °	12 °	13 °
θ 2	11 °	12 °	13 °

6.3 Package LQFP32

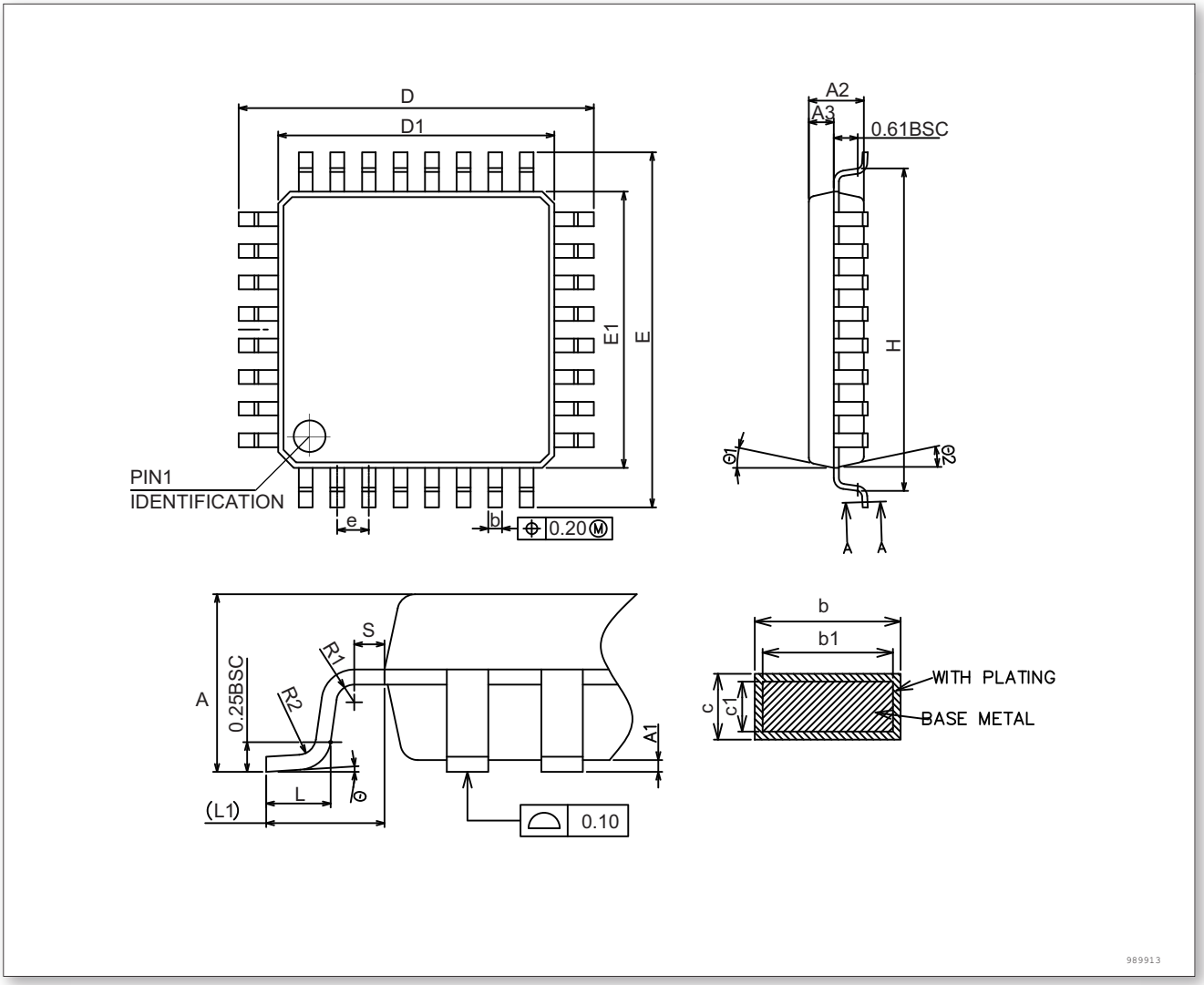

Figure 26. LQFP32, 32-Pin Low-Profile Quad Flat Package Outline

1. The Diagram is not drawn to scale.
2. The size is in mm.

Table 46. LQFP32 Size Description

Lable	Mm		
	Min	Typical	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.42
b1	0.32	0.35	0.38
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20

Lable	Mm		
	Min	Typical	Max
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	-	0.70
L1	1.00REF		
R1	0.08		
R2	0.08		0.20
S	0.20		
θ	0 °	3.5 °	7 °
θ1	11 °	12 °	13 °
θ2	11 °	12 °	13 °

6.4 Package QFN32

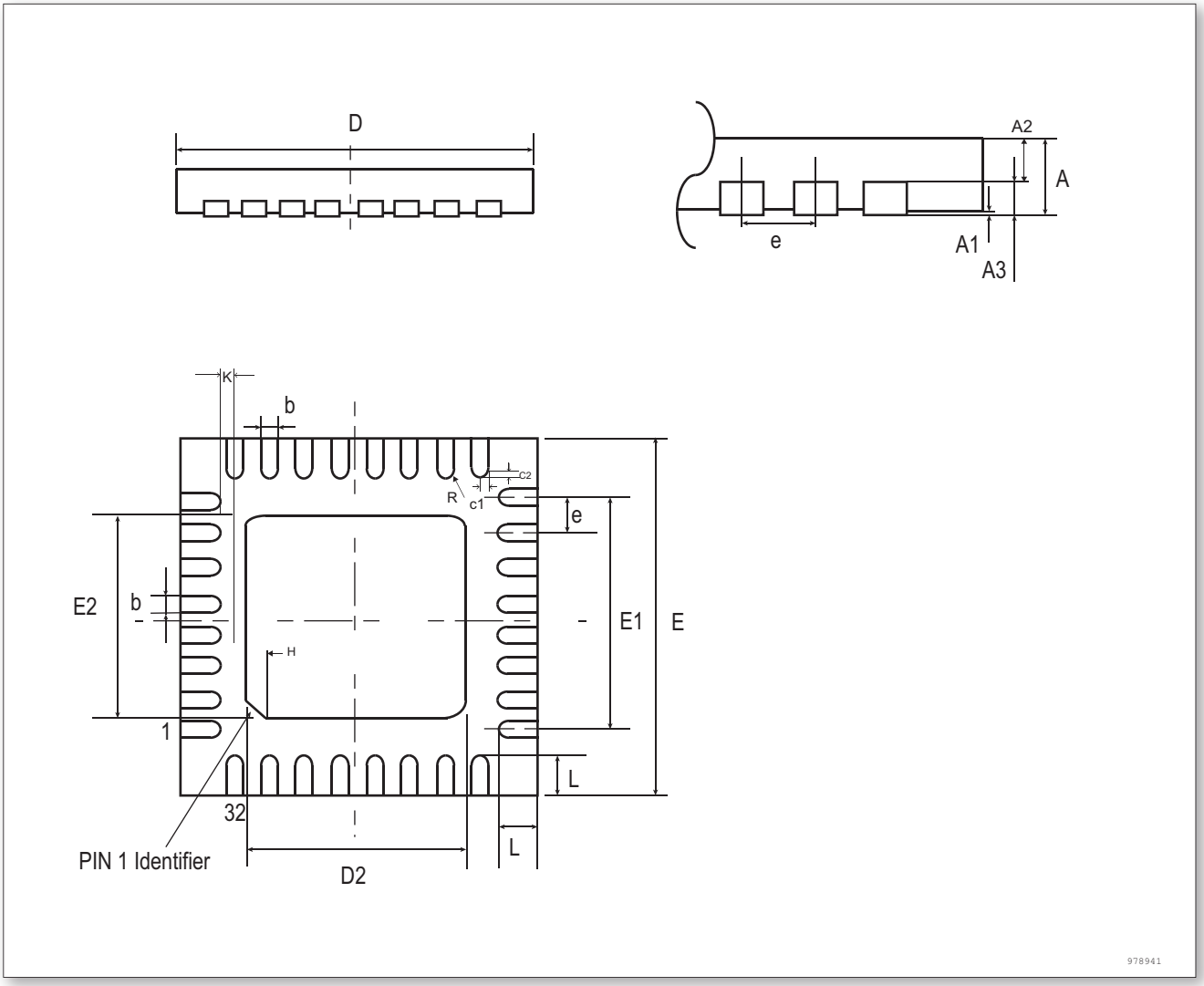

Figure 27. QFN32 , 32-Pin Low-Profile Quad Flat Package Outline

1. The Diagram is not drawn to scale.
2. The size is in mm.

Table 47. QFN32 Size Description

Lable	Mm		
	Min	Typical	Max
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60
E2	3.40	3.50	3.60

Lable	Mm		
	Min	Typical	Max
e		0.5	
H		0.30REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.09		
c1		0.08	
c2		0.08	
N		Number of pins = 32	

7 Model Designation

Model Designation

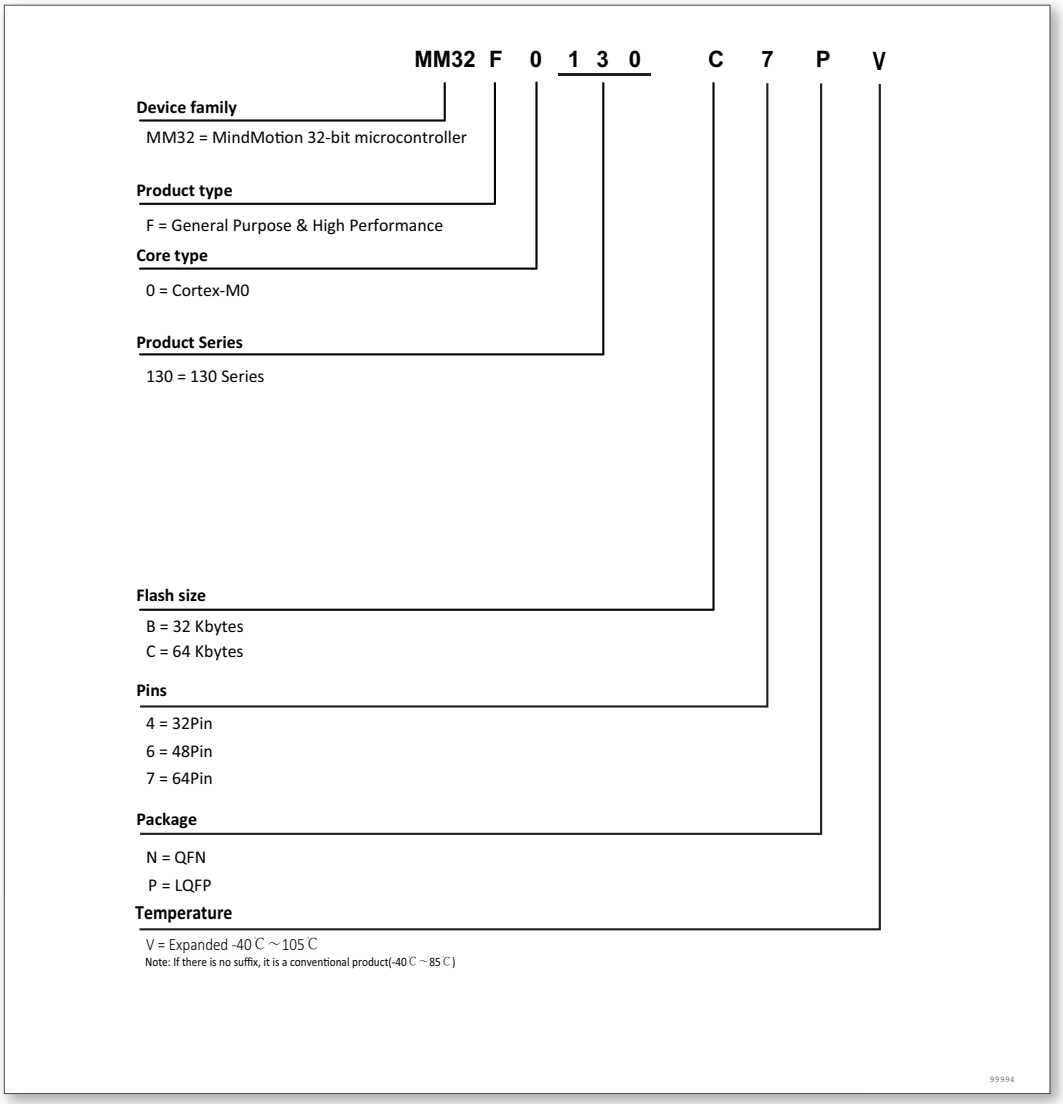

Figure 28: Designation of Model MM32

8 Revision Records

Revision Records

Table 48. Revision Records

Date	Rev.	Content
2020/07/02	Rev1.00	Formal version