Data sheet

Datasheet

MM32W06xxxB

32 ARM® Cortex ® M0

1.00

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1

Sosuke

1.1

This product is a single-mode Bluetooth chip with ultra-low power consumption. The radio frequency uses 2.4GHZ ISM frequency band with 2MHz channel spacing.
Comply with Bluetooth specification. This product uses high-performance ARM ® Cortex ® -M0 is the core 32-bit microcontroller, the highest
The operating frequency can reach 48MHz, built-in high-speed memory, rich enhanced I/O ports and peripherals connected to the external bus. this
The product includes 1 12-bit ADC, 2 comparators, 1 16-bit general-purpose timer, 1 32-bit general-purpose timer,
Three 16-bit basic timers and one 16-bit advanced timer. Also includes standard communication interfaces: 1 I2C interface, 1
One SPI interface, one USB interface and two UART interfaces.

The working voltage of this product series is 2.3V ~ 3.6V, and the working temperature range is -40 ° C ~ 85 ° C Regular type. Multiple power saving
Working mode guarantees the requirements of low-power applications.

This product provides two packages, LQFP48 and QFN32.

According to different packaging forms, the peripheral configuration in the device is not the same.

These rich peripheral configurations make this product microcontroller suitable for a variety of applications:

• Wireless keyboard, mouse
• Industrial applications: industrial remote control, telemetry
• Alarm system, access control system, data acquisition and transmission system

1.2

• Kernel and system
  – 32-bit ARM ® Cortex ® -M0 processor core
  -**The** highest operating frequency can reach 48MHz
  - single-cycle 32-bit hardware multiplier
• Storage
  - Up to 64K bytes of Flash program memory
  - up to 8K bytes of SRAM, 4K bytes available to the user
  – Boot loader supports on-chip Flash, UART online user programming (IAP) / online system programming (ISP)
• Single-mode BLE RF transceiver
  - packet processing engine
  – GFSK encoding method
  - internal voltage regulator ensured PSRR
  - Programmable transmit power range: -28dBm ~ + 4dBm
  – 1Mbps air data transmission
  – RF link budget: up to -80dBm
• Clock, reset and power management

  – 2.3V ~ 3.6V power supply
  -Power - on/power-off reset (POR/PDR), programmable voltage monitor (PVD)
  - RF module external high speed 16MHz crystal oscillator
  - built by the factory tuned high-speed 48MHz oscillator
  - embedded 40KHz low frequency oscillator
  – PLL supports CPU running at up to 48MHz
  - External low-speed oscillator 32.768K
• Low power consumption
  - sleep, shutdown and standby modes
  - Support RTC function and backup registers
• 1 12-bit analog-to-digital converter, 1μS conversion time (up to 10 input channels)
  – Conversion range: 0 ~ V DDA

- support the resolution and sampling time configuration

--On- chip temperature sensor

--On- chip voltage sensor

• 2 comparators

• 5-channel DMA controller

- Supported peripherals: Timer, UART, I2C, SPI , USB and ADC

• Up to 28 fast I/O ports:

- All I / O port 16 may be mapped to external interrupts

• Debug mode

- serial wire debug (SWD)

• Up to 9 timers

– 1 16-bit 4-channel advanced control timer with 4-channel PWM output, as well as dead zone generation and tight Emergency stop function

– 1 16-bit timer and 1 32-bit timer, up to 4 input capture/output compare, available Control decoding in IR

– 2 16-bit timers, 1 input capture/output compare and 1 OCN, dead zone generation, emergency stop Only, the modulator gate is used for IR control

– 1 16-bit timer with 1 input capture/output compare

– 2 watchdog timers (independent and window type)

– 1 System time timer: 24-bit self-decreasing counter

• Up to 5 communication interfaces

– 2 UART interfaces

– 1 I2C interface

– 1 SPI interface

– 1 USB device interface

• BOM cost of low-cost peripheral components

• 96-bit unique chip ID (UID)

• Available in LQFP48 and QFN32 packages

For complete details of this product, please refer to section 2.2 of this product data sheet .

About Cortex ® -M0 core related information, please refer to "Cortex® -M0 Technical Reference Manual.

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2

Specifications

2.1

1.

Product number / Peripheral interface		MM32W062NTB	MM32W062PFB
Flash memory-K bytes		64	64
SRAM-K bytes		8	8
Timer	General (16 bit)	1	
	General (32 bit)	1	
	Basic	3	
	advanced	1	
Communication Interface	UART	2	
	I2C	1	
	SPI	1	
	USB	1	
Number of GPIO ports		twenty two	28
	Number	1	

12-bit ADC	Number of channels	5	10
	Number of comparators	2	
	RTC	√	
	CPU frequency	48 MHz	
	Operating Voltage	2.3V ~ 3.6V	
	Package	QFN32	LQFP48

2.2

2.2.1 ARM Cortex-M0 SRAM

ARM ® The Cortex ® -M0 processor is the latest generation of embedded ARM processor, it is needed to realize MCU
Provides a low-cost platform, reduced number of pins, reduced system power consumption, while providing excellent computing performance and advanced
Incoming interrupt system response.

ARM ® The Cortex ® -M0 is a 32-bit RISC processor, providing additional code efficiency, in the usual 8 and 16-bit
The high performance of the ARM core is exerted on the storage space of the system.

This product has a built-in ARM core, so it is compatible with all ARM tools and software.

2.2.2

The built-in flash memory of up to 64K bytes is used to store programs and data.

2.2.3 SRAM

Built-in SRAM up to 8K bytes.

2.2.4 CRC( )

CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate from a 32-bit data word
A CRC code. In many applications, CRC-based technology is used to verify the consistency of data transmission or storage.
Within the scope of EN/IEC60335-1 standard, it provides a means to detect flash memory errors, CRC calculation
The unit can be used to calculate the signature of the software in real time and compare it with the signature generated when the software is linked and generated.

2.2.5 (NVIC)

This product has a built-in nested vectored interrupt controller that can handle multiple maskable interrupt channels (not including 16
Cortex™-M0 interrupt line) and 16 programmable priority levels.

- Tightly coupled NVIC can achieve low-latency interrupt response processing
- The interrupt vector entry address directly enters the kernel
- Tightly coupled NVIC interface
- Allow early processing of interrupts
- Handle the higher priority interrupts that arrive late
- Support interrupt tail link function
- Automatically save processor state
- Automatic recovery when the interrupt returns, without additional instruction overhead

The module provides flexible interrupt management functions with minimal interrupt delay.

2.2.6 / (EXTI)

The external interrupt/event controller contains multiple edge detectors to generate interrupt/event requests. Each interrupt line can be independent
Configure its trigger event (rising edge or falling edge or both edges), and can be individually shielded; there is a pending register
The register maintains the status of all interrupt requests. EXTI can detect that the pulse width is smaller than the clock period of the internal APB2. So
There are general I/O ports connected to 16 external interrupt lines.

2.2.7

The system clock is selected at startup. The internal 48 MHz oscillator divided by 6 is selected as the default CPU at reset
Clock, then you can select an external 1 ~ 24 MHz clock with failure monitoring. When an external clock failure is detected,
It will be isolated and the system will automatically switch to the internal oscillator. If the interrupt is enabled, the software can receive the corresponding
Interruption. Similarly, complete interrupt management of the PLL clock can be taken when needed (for example, when an indirectly used external

When the oscillator fails).
Multiple prescalers are used to configure the AHB frequency, high-speed APB (APB2 and APB1) area. AHB and high-speed APB
The highest frequency is 48MHz. Refer to Figure 2 for the clock drive block diagram.

2.2.8

At startup, one of three boot modes can be selected through the boot pin:

- Boot from program flash memory
- Boot from system memory
- Boot from internal SRAM

The boot loader is stored in the system memory, and the flash memory can be reprogrammed through UART1.

2.2.9

- V_{DD} = 2.3V ~ 3.6V: The V_{DD} pin supplies power to the I/O pins and the internal voltage regulator.
  V_{DDA} = 2.3V ~ 3.6V: Provide power for the analog part of ADC, reset module, oscillator and PLL. V_{DDA} and
  V_{SSA} must be connected to V_{DD} and V_{SS} respectively .

2.2.10

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in working condition to ensure
Prove that the system works when the power supply exceeds 2.3V; when V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in reset state
State without using an external reset circuit.

There is also a programmable voltage monitor (PVD) in the device, which monitors the V_{DD} /V_{DDA} power supply and compares it with the threshold V_{PVD} .
When V_{DD} is lower or higher than the threshold V_{PVD} , an interrupt is generated. The interrupt handler can issue a warning message or switch the microcontroller to
Enter safe mode. The PVD function needs to be turned on by program.

2.2.11

The voltage regulator converts the external voltage into a voltage for internal digital logic work, and the voltage regulator is always in working state after reset.

2.2.12

The product supports low-power mode, which can achieve the best balance between requirements for low power consumption, short startup time, and multiple wake-up events.
Balance.

In sleep mode, only the CPU is stopped, all peripherals are in working state and can wake up the CPU when an interrupt/event occurs.

Under the condition that the contents of SRAM and registers are not lost, the shutdown mode can achieve the lowest power consumption. Down
In this mode, the HSI oscillator and HSE crystal oscillator are turned off. You can use any signal configured as EXTI to
The controller wakes up from stop mode, EXTI signal can be one of 16 external I/O ports, the wake-up signal of PVD output
number.

Standby mode can achieve the lowest power consumption of the system. This mode turns off the voltage regulator when the CPU is in deep sleep mode. internal
All the power supply areas of the 1.5V part are disconnected. PLL, HSI and HSE oscillators are also turned off, you can use WKUP
The rising edge of the pin, external reset of the NRST pin, IWDG reset wake-up or watchdog timer wake-up and reset.
The contents of SRAM and registers will be lost. Only the backup registers and standby circuits maintain power.

2.2.13 DMA

Flexible 5-channel general-purpose DMA can manage data transfer from memory to memory, device to memory, and memory to device
The DMA controller supports the management of the ring buffer, which avoids the intermediate transfer caused when the controller transfer reaches the end of the buffer
Off.

Each channel has a dedicated hardware DMA request logic, and each channel can be triggered by software at the same time;

Both the source address and destination address of the input can be individually set by software.

DMA can be used for the main peripherals: use UART, I2C, SPI, ADC, USB and general/basic/advanced control
Timer TIMx.

2.2.14 RTC( )

The real-time clock is an independent timer. The RTC module has a set of continuous counting counters. Under the corresponding software configuration,

Can provide clock calendar function. Modifying the counter value can reset the current time and date of the system. RTC module

And the clock configuration system (RCC_BDCR register) is in the backup area, that is, after the system is reset or wakes up from standby mode,

The RTC setting and time remain unchanged.

2.2.15

The backup registers are 20 16-bit registers that can be used to store user application data.

They will not be reset when the system is woken up in standby mode, or when the system is reset or power is reset.

2.2.16

The product includes 1 advanced timer, 2 general timers, and 3 basic timers. And 2 watchdog timers and

1 system tick timer.

The following table compares the functions of advanced control timers, general timers and basic timers:

2.

Timer type	name	Counter resolution	Counter type	Prescaler	**DMA** request generation	Capture / compare channel	Complementary output
advanced	TIM1	16 bits	Increase, pass Decrease, pass Increase/decrease	1 ~ 65536 Any in between Integer	Have	4	Have
Universal	TIM2	32 bit	Increase, pass Decrease, pass Increase/decrease	1 ~ 2_{32} − 1 Any in between Integer	Have	4	no
	TIM3	16 bits	Increase, pass Decrease, pass Increase/decrease	1 ~ 65536 Any in between Integer	Have	4	no
Basic	TIM14	16 bits	Increase	1 ~ 65536 Any in between Integer	Have	1	no
	TIM16 / TIM17	16 bits	Increase	1 ~ 65536 Any in between Integer	Have	1	Have

(TIM1)

The advanced control timer is composed of a 16-bit counter, 4 capture/compare channels and a three-phase complementary PWM generator.

It has complementary PWM output with dead zone insertion and can also be used as a complete general-purpose timer. Four independent channels

Used for:

- Input capture
- Output comparison
- Generate PWM (edge or center aligned mode)
- Single pulse output

When configured as a 16-bit general-purpose timer, it has the same function as the TIMx timer. Configured as 16-bit PWM generation

It has full modulation capability (0 ~ 100%) when the device is used.

In debug mode, the counter can be frozen and the PWM output is disabled, thereby cutting off the control by these outputs

Switch.

Many functions are the same as the general TIM timer, and the internal structure is also the same, so the advanced control timer can be set
The timer link function cooperates with the TIM timer to provide synchronization or event link function.

(TIMx)

In the product, up to 2 general-purpose timers (TIM2, TIM3) that can run synchronously are built-in. The timer has a 32-bit
Automatic loading up/down counter, a 16-bit prescaler and 4 independent channels, each channel is available
For input capture, output comparison, PWM and single pulse mode output.

_32

The timer has a 32-bit autoload up/down counter, a 16-bit prescaler and 4 independent communication channels.
Each channel can be used for input capture, output comparison, PWM and single pulse mode output.

_16

Each timer has a 16-bit auto-loading up/down counter, a 16-bit prescaler and 4 independent
Each channel can be used for input capture, output comparison, PWM and single pulse mode output.

They can also work with advanced control timers through the timer link function to provide synchronization or event link functions. in
In debug mode, the counter can be frozen. Any general-purpose timer can be used to generate PWM output. Every timer
All have independent DMA request mechanism.

These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 4 Hall sensors. each
Both timers have PWM output, or as a simple time base.

TIM14

The timer is based on a 16-bit auto-reload increment counter and a 16-bit prescaler. Has a single channel, with
For input capture/output comparison, PWM or single pulse mode output. In debug mode, its counter can be frozen.

TIM16 / TIM17

The timers are based on a 16-bit auto-reload increment counter and a 16-bit prescaler. There is a single channel for
Input capture/output comparison, PWM or single pulse mode output. Complementary output, with dead zone generation and independent DMA
Seek generation function. In debug mode, the timer is off.

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler, which consists of an internal independent
40KHz oscillator provides the clock; because this oscillator is independent of the main clock, it can run in shutdown and standby
mode. It can be used to reset the whole system when a problem occurs in the system or as a free timer to provide super

Time management. The option byte can be configured to enable the watchdog by software or hardware. In debug mode, the watchdog is turned off
close.

There is a 7-bit down counter in the window watchdog, and it can be set to free running. It can be used as a watchdog
To reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in the debug mode,
The watchdog is closed.

This timer is dedicated to the real-time operating system and can also be used as a standard down counter. It has the following characteristics:

- 24-bit down counter
- Auto reload function
- A maskable system interrupt can be generated when the counter is 0
- Programmable clock source

2.2.17 (UART)

The UART interface has hardware CTS and RTS signal management. Support LIN master-slave function. Compatible with ISO7816 smart
Card mode. The UART interface supports output data length that can be configured as 5 bits, 6 bits, 7 bits, 8 bits, and 9 bits.

All UART interfaces can use DMA operation.

2.2.18 I2C

The I2C bus interface can work in multi-master mode or slave mode, and supports standard and fast modes.

The I2C interface supports 7-bit or 10-bit addressing.

2.2.19 (SPI)

SPI interface, in slave or master mode, can be configured as 1 to 32 bits per frame.

All SPI interfaces can use DMA operation.

2.2.20 (USB)

A device controller compatible with full-speed USB is embedded in the product, which follows the standard of full-speed USB device (12 Mbit/s).

Points can be configured by software. The 48MHz clock dedicated to USB is directly generated by the internal PLL or the internal clock at room temperature (HSI).

2.2.21 (GPIO)

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplex

The peripheral function port used. Most GPIO pins are shared with digital or analog multiplexed peripherals. All GPIO pins

All have high current passing capacity.

When needed, the peripheral functions of I/O pins can be locked by a specific operation to avoid accidental writing

I/O register.

2.2.22 ADC(/ Number)

The product is embedded with a 12-bit analog/digital converter (ADC), ADC can use up to 10 external channels, which can be realized

Single, single cycle and continuous scan conversion. In scan mode, automatic acquisition on a selected set of analog inputs

Value conversion.

ADC can use DMA operation.

The analog watchdog function allows very precise monitoring of one channel or all selected channels, when the monitored signal exceeds the preset

When the threshold is reached, an interrupt will be generated.

The events generated by the general-purpose timer (TIMx) and the advanced control timer can be internally cascaded to the ADC trigger respectively.

The application program can synchronize the ADC conversion with the clock.

2.2.23

The temperature sensor generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input

On the road, it is used to convert the output of the sensor to a digital value.

2.2.24 SWD (SW-DP)

Embedded ARM's two-wire serial debug port (SW-DP).

ARM's SW-DP interface allows to connect to the microcontroller through a serial wire debugging tool.

2.2.25 (COMP)

The product has two built-in comparators, which can be used independently (applicable to I/O ports on all terminals) or combined with timers. and also

Can be used for multiple functions, including:

- Low-power mode wake-up event triggered by analog signal
- Adjust the analog signal
- The PWM output of the timer is combined to form a cycle-by-cycle current control loop
- Rail-to-rail comparator
- Each comparator has an optional threshold
  - the I reusable / O pin
  - **The** internal comparison voltage CRV can select AVDD or the divided voltage value of the internal reference voltage
- Programmable hysteresis voltage
- Programmable rate and power consumption
- The output can be redirected to one I/O port or multiple timer inputs, and the following events can be triggered:
  - Capture Event
  - – OCref_clr event (cycle-by-cycle current control)
  - For fast PWM off braking event

2.2.26

This chip integrates Bluetooth specification and radio frequency transceiver, compatible with the definition of the International Communication Union Radio Communication B

Available 2.4GHz ISM frequency band.

After supplying power to the chip, the RF transceiver peripheral only needs to build simple peripheral components to achieve wireless transceiver functions. It provides high Excellent RF link budget up to -80dBm.

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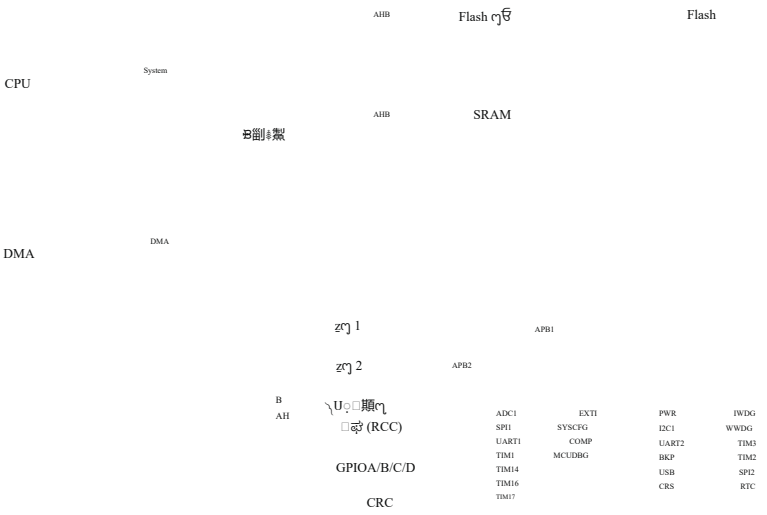
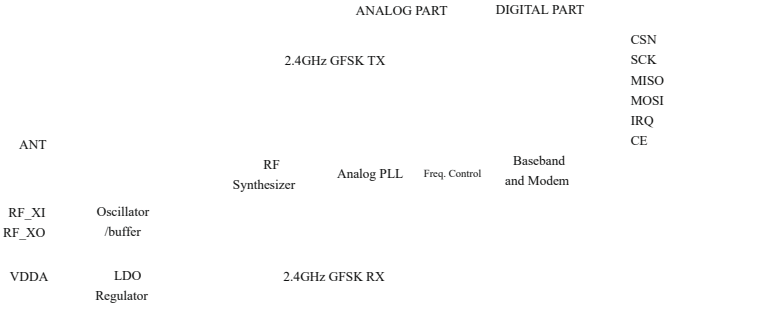


DMA



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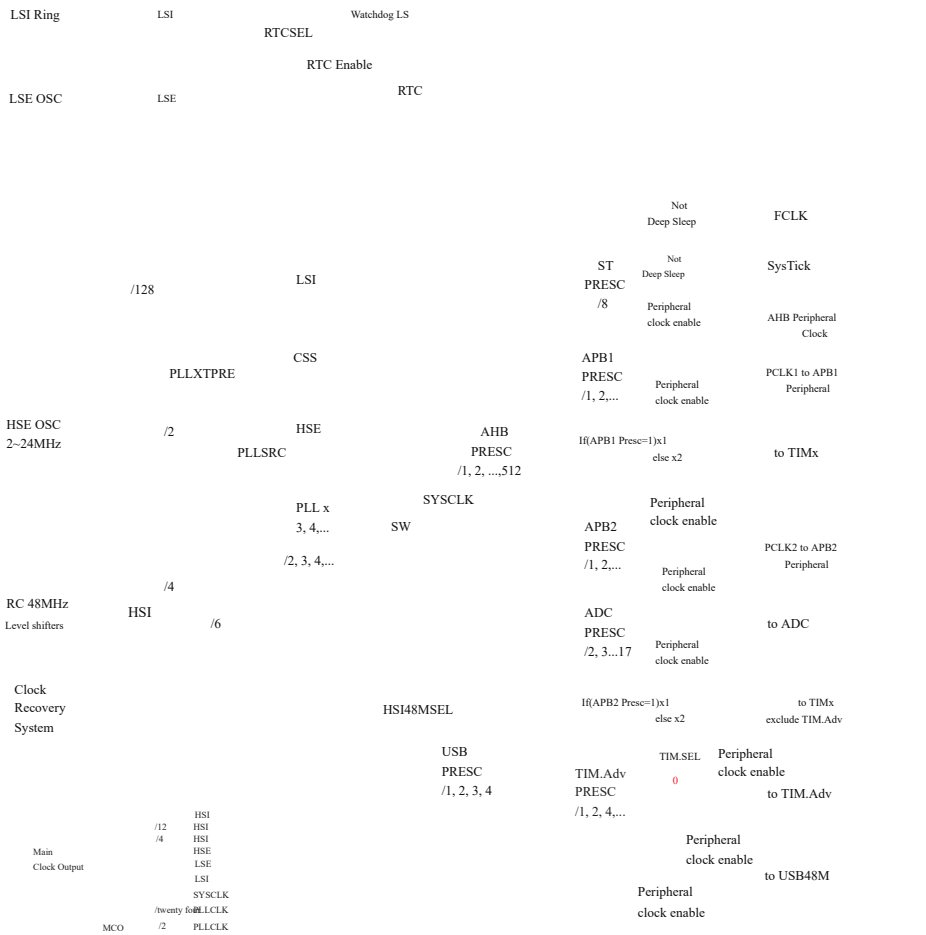

2.

3

Pin definition

0
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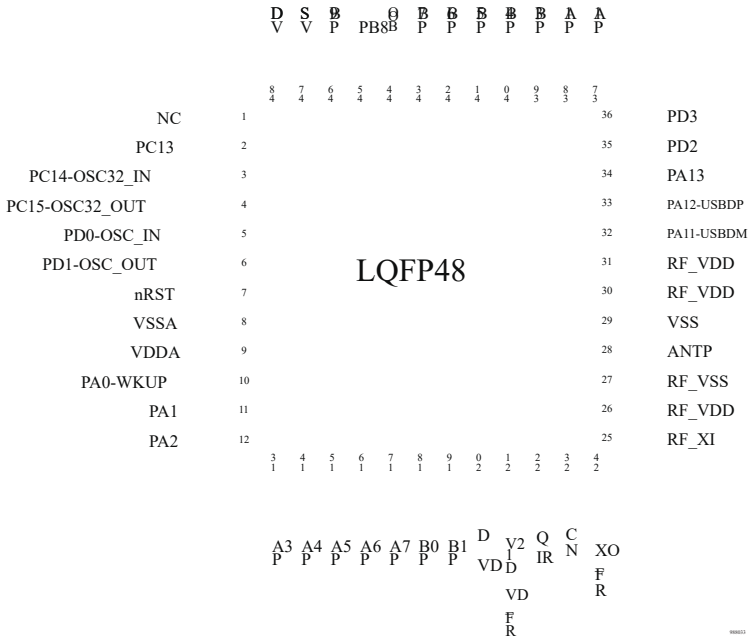

3. LQFP48

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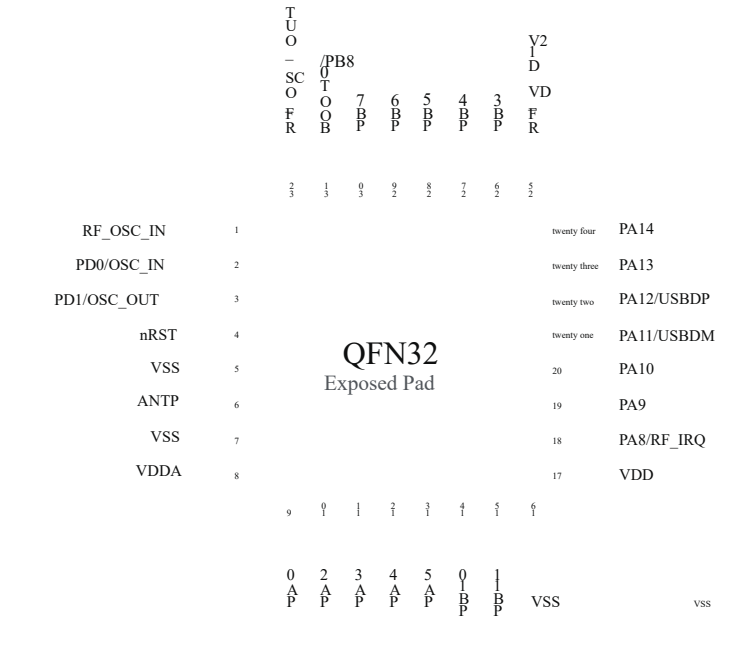

4. QFN32

3.

Pin code		Pin name	Type (1)	I/O level (2)	Main function	Optional multiplexing function	Add function
LQFP48	**QFN32**						
1	-	NC	-	-	NC	-	-
2	-	PC13	I/O	TC	PC13	TIM2_CH1 TIM2_ETR	-
3	-	PC14 OSC32_IN	I/O	TC	PC14	TIM2_CH2	-
4	-	PC15 OSC32_OUT	I/O	TC	PC15	TIM2_CH3	-
5	2	PD0 OSC_IN	I/O	TC	PD0	I2C1_SDA TIM1_CH1N UART1_TX TIM1_CH2 SPI1_MOSI	-

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Pin code		Pin name	Type (1)	I/O level (2)	Main function	Optional multiplexing function	Add function
LQFP48	**QFN32**						
6	3	PD1 OSC_OUT	I/O	TC	PD1	TIM1_BKIN I2C1_SCL TIM1_CH1 UART1_RX TIM1_CH2 SPI1_MISO SPI1_SCK	-
7	4	nRST	I/O	TC	nRST	-	-
8	-	VSSA	S	-	VSSA	-	-
9	8	VDDA	S	-	VDDA	-	-
10	9	PA0 WKUP	I/O	TC	PA0	UART2_CTS TIM2_CH1 TIM2_ETR UART1_RX TIM14_CH1 COMP1_OUT	ADC1_VIN[0] COMP1_INP[0] COMP2_INP[0] COMP1_INM[2]
11	-	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2 TIM1_CH2 UART1_TX	ADC1_VIN[1] COMP1_INP[1] COMP2_INP[1]
12	10	PA2	I/O	TC	PA2	UART2_TX TIM2_CH3 TIM1_CH2N COMP2_OUT	ADC1_VIN[2] COMP1_INP[2] COMP2_INP[2] COMP2_INM[2]
13	11	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4 TIM1_CH3	ADC1_VIN[3] COMP1_INP[3] COMP2_INP[3]
14	12	PA4	I/O	TC	PA4	SPI1_NSS SPI1_SCK TIM1_CH3N	ADC1_VIN[4] COMP1_INM[0]

						TIM14_CH1	COMP2_INM[0]
						TIM1_BKIN	
						SPI1_SCK	
						SPI1_NSS	ADC1_VIN[5]
15	13	PA5	I/O	TC	PA5	TIM2_CH1	COMP1_INM[1]
						TIM2_ETR	COMP2_INM[1]
						TIM1_CH3N	

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Pin code		Pin name	Type (1)	**I/O** level (2)	Main function	Optional multiplexing function	Add function
LQFP48	**QFN32**						
						SPI1_MISO	
						TIM3_CH1	
16	-	PA6	I/O	TC	PA6	TIM1_BKIN	ADC1_VIN[6]
						TIM16_CH1	
						TIM1_CH3	
						COMP1_OUT	
						SPI1_MOSI	
						TIM3_CH2	
						TIM1_CH1N	
17	-	PA7	I/O	TC	PA7	TIM1_CH3N	ADC1_VIN[7]
						TIM14_CH1	
						TIM17_CH1	
						TIM1_CH2N	
						COMP2_OUT	
						TIM3_CH3	
18	-	PB0	I/O	TC	PB0	TIM1_CH2N	ADC1_VIN[8]
						TIM1_CH1N	
						TIM1_CH3	
						TIM14_CH1	
						TIM3_CH4	
						TIM1_CH3N	
19	-	PB1	I/O	TC	PB1	TIM1_CH2N	ADC1_VIN[9]
						TIM2_CH3	
						TIM1_CH2	
						TIM1_CH1N	
20	17	VDD	S	-	VDD	-	-
twenty one	25	RF_VDD1V2	S	-	RF_VDD1V2	-	-
twenty two	-	IRQ	S	-	IRQ	-	-
twenty three	-	NC	S	-	NC	-	-
twenty four	-	RF_XO	O	-	RF_XO	-	-
25	-	RF_XI	I	-	RF_XI	-	-
26	-	RF_VDD	S	-	RF_VDD	-	-
27	-	RF_VSS	S	-	RF_VSS	-	-
28	6	ANTP	-	-	ANTP	-	-
29	5	VSS	S	-	VSS	-	-
30	-	RF_VDD	S	-	RF_VDD	-	-
31	-	RF_VDD	S	-	RF_VDD	-	-

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Pin code		Pin name	Type (1)	**I/O** level (2)	Main function	Optional multiplexing function	Add function
LQFP48	**QFN32**						
						UART1_CTS	
						TIM1_CH4	
						TIM1_CH3	
32	twenty one	PA11	I/O	TC	PA11	CAN1_RX	-
						I2C1_SCL	
						TIM1_BKIN	
						COMP1_OUT	
						UART1_RTS	
						TIM1_ETR	
						TIM1_CH3N	
33	twenty two	PA12	I/O	TC	PA12	CAN1_TX	-
						I2C1_SDA	
						TIM1_CH2	
						COMP2_OUT	
34	twenty three	PA13	I/O	TC	PA13	SWDIO	-
						UART1_TX	
35	-	PD2	I/O	TC	PD2	I2C1_SCL	-
						SPI1_NSS	
						I2C1_SDA	
36	-	PD3	I/O	TC	PD3	SPI1_SCK	-
						SPI1_MISO	
						SWDCLK	
37	twenty four	PA14	I/O	TC	PA14	UART2_TX	-
						UART1_RX	
						SPI1_NSS	
						UART2_RX	
38	-	PA15	I/O	TC	PA15	TIM2_CH1	-
						TIM2_ETR	
						TIM1_CH1N	
						TIM1_CH3N	
						SPI1_SCK	
						TIM2_CH2	
39	26	PB3	I/O	TC	PB3	TIM1_CH1	-
						TIM1_CH2N	
						TIM1_CH3	

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Pin code		Pin name	Type (1)	**I/O** level (2)	Main function	Optional multiplexing function	Add function
LQFP48	**QFN32**						
						SPI1_MISO	
						TIM3_CH1	
						TIM1_CH2	
40	27	PB4	I/O	TC	PB4	TIM17_BKIN	-
						TIM1_CH3N	

						TIM1_CH2N	
						SPI1_MOSI	
						TIM3_CH2	
41	28	PB5	I/O	TC	PB5	TIM16_BKIN	-
						TIM1_CH1	
						TIM1_CH2	
						UART1_TX	
						I2C1_SCL	
42	29	PB6	I/O	TC	PB6	TIM16_CH1N	-
						TIM1_CH2N	
						TIM1_CH2	
						TIM1_CH1N	
						UART1_RX	
						I2C1_SDA	
43	30	PB7	I/O	TC	PB7	TIM17_CH1N	-
						TIM1_CH3	
						TIM1_CH1	
44	31	BOOT0	I	-	BOOT0	-	-
						UART1_RX	
						I2C1_SCL	
45	31	PB8	I/O	TC	PB8	TIM16_CH1	-
						TIM1_CH1	
						CAN1_RX	
						TIM3_CH2	
						UART1_TX	
46	-	PB9	I/O	TC	PB9	I2C1_SDA	-
						TIM17_CH1	
						TIM3_CH3	
47	7	VSS	S	-	VSS	-	-
48	-	VDD	S	-	VDD	-	-
-	1	RF_OSC_IN	I	-	RF_OSC_IN	-	-

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Pin code		Pin name	Type (1)	**I/O** level (2)	Main function	Optional multiplexing function	Add function
LQFP48	**QFN32**						
-	14	PB10	I/O	TC	PB10	I2C1_SCL	-
						TIM2_CH3	
-	15	PB11	I/O	TC	PB11	I2C1_SDA	-
						TIM2_CH4	
-	16	VSS	I/O	TC	VSS	I2C1_SDA	-
						TIM2_CH4	
						MCO	
-	18	PA8	I/O	TC	PA8	TIM1_CH1	-
		RF_IRQ				TIM1_CH2	
						TIM1_CH3	
						UART1_TX	
						TIM1_CH2	
-	19	PA9	I/O	TC	PA9	UART1_RX	-
						I2C1_SCL	
						MCO	
						TIM1_CH1N	

						TIM17_BKIN UART1_RX TIM1_CH3	
-	20	PA10	I/O	TC	PA10	UART1_TX I2C1_SDA TIM1_CH1 TIM16_CH1	-
-	32	RF_OSC_OUT	O	-	RF_OSC_OUT	-	-

1. I = input, O = output, S = power, HiZ = high impedance

2. TC: Standard IO, the input signal does not exceed the VDD voltage

4. PA AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1 TIM2_ETR	-	UART1_RX	-	TIM14_CH1	COMP1_OUT
PA1	-	UART2_RTS	TIM2_CH2	TIM1_CH2	UART1_TX	-	-	-
PA2	-	UART2_TX	TIM2_CH3	TIM1_CH2N	-	-	-	COMP2_OUT
PA3	-	UART2_RX	TIM2_CH4	TIM1_CH3	-	-	-	-
PA4	SPI1_NSS	SPI1_SCK	-	TIM1_CH3N	TIM14_CH1	TIM1_BKIN	-	-
PA5	SPI1_SCK	SPI1_NSS	TIM2_CH1 TIM2_ETR	-	-	-	TIM1_CH3N	-

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	TIM1_CH3	COMP1_OUT
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	TIM1_CH3N	TIM14_CH1	TIM17_CH1	TIM1_CH2N	COMP2_OUT
PA8	MCO	-	TIM1_CH1	-	-	-	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	TIM1_CH1	TIM16_CH1	-
PA11	-	UART1_CTS	TIM1_CH4	TIM1_CH3	CAN1_RX	I2C1_SCL	TIM1_BKIN	COMP1_OUT
PA12	-	UART1_RTS	TIM1_ETR	TIM1_CH3N	CAN1_TX	I2C1_SDA	TIM1_CH2	COMP2_OUT
PA13	SWDIO	-	-	UART1_TX	-	-	-	-
PA14	SWDCLK	UART2_TX	-	UART1_RX	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1 TIM2_ETR	-	-	-	TIM1_CH1N	TIM1_CH3N

5. PB AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH2N	TIM2_CH3	TIM1_CH2	TIM1_CH1N	-
PB3	SPI1_SCK	-	TIM2_CH2	-	TIM1_CH1	-	TIM1_CH2N	TIM1_CH3
PB4	SPI1_MISO	TIM3_CH1	-	-	TIM1_CH2	TIM17_BKIN	TIM1_CH3N	TIM1_CH2N
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	TIM1_CH1	TIM1_CH2
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM1_CH2N	-	TIM1_CH2	TIM1_CH1N
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM1_CH3	TIM1_CH1
PB8	UART1_RX	I2C1_SCL	TIM16_CH1	TIM1_CH1	CAN1_RX	-	TIM3_CH2	-
PB9	UART1_TX	I2C1_SDA	TIM17_CH1	-	CAN1_TX	-	TIM3_CH3	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-	-	-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-

6. PC AF0-AF7

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7

Name								
PC13	-	-	-	-	-	-	TIM2_CH1 TIM2_ETR	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

7. PD AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	TIM1_CH1N	UART1_TX	TIM1_CH2	SPI1_MOSI	SPI1_MOSI	-

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Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD1	TIM1_BKIN	I2C1_SCL	TIM1_CH1	UART1_RX	TIM1_CH2	SPI1_MISO	SPI1_SCK	-
PD2	-	I2C1_SCL	-	-	-	SPI1_NSS	SPI1_NSS	-
PD3	-	I2C1_SDA	-	-	-	SPI1_SCK	SPI1_MISO	-

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4 Memory map

8.

bus	Address range	size	Peripherals	Remarks
Flash	0x0000 0000–0x0000 FFFF	64 KB	Main flash memory, system memory or SRAM depends on BOOT configuration	
	0x0001 0000–0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000–0x0800 FFFF	64 KB	Main Flash memory	
	0x0801 0000–0x1FFD FFFF	~ 383 MB	Reserved	
	0x1FFE 0000–0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200–0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000–0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00–0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400–0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800–0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810–0x1FFF FFFF	~2 KB	Reserved	
SRAM	0x2000 0000–0x2000 1FFF	8 KB	SRAM	
	0x2000 2000–0x2FFF FFFF	~ 255 MB	Reserved	
APB1	0x4000 0000–0x4000 03FF	1 KB	TIM2	
	0x4000 0400–0x4000 07FF	1 KB	TIM3	
	0x4000 0800–0x4000 0BFF	8 KB	Reserved	
	0x4000 2800–0x4000 2BFF	1 KB	RTC/BKP	
	0x4000 2C00–0x4000 2FFF	1 KB	WWDG	
	0x4000 3000–0x4000 33FF	1 KB	IWDG	
	0x4000 3400–0x4000 37FF	1 KB	Reserved	
	0x4000 3800–0x4000 3BFF	1 KB	Reserved	
	0x4000 4000–0x4000 43FF	1 KB	Reserved	
	0x4000 4400–0x4000 47FF	1 KB	UART2	
	0x4000 4800–0x4000 4BFF	3 KB	Reserved	
	0x4000 5400–0x4000 57FF	1 KB	I2C1	
	0x4000 5800–0x4000 5BFF	1 KB	Reserved	
	0x4000 5C00–0x4000 5FFF	1 KB	USB	
	0x4000 6000–0x4000 63FF	1 KB	Reserved	

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bus	Address range	size	Peripherals	Remarks
APB1	0x4000 6400–0x4000 67FF	1 KB	Reserved	
	0x4000 6800–0x4000 6BFF	1 KB	Reserved	
	0x4000 6C00–0x4000 6FFF	1 KB	CSR	
	0x4000 7000–0x4000 73FF	1 KB	PWR	

	0x4000 7400–0x4000 FFFF	35 KB	Reserved
	0x4001 0000–0x4001 03FF	1 KB	SYSCFG
	0x4001 0400–0x4001 07FF	1 KB	EXTI
	0x4001 0800–0x4001 23FF	7 KB	Reserved
	0x4001 2400–0x4001 27FF	1 KB	ADC1
	0x4001 2800–0x4001 2BFF	1 KB	Reserved
	0x4001 2C00–0x4001 2FFF	1 KB	TIM1
APB2	0x4001 3000–0x4001 33FF	1 KB	SPI1
	0x4001 3400–0x4001 37FF	1 KB	DBGMCU
	0x4001 3800–0x4001 3BFF	1 KB	UART1
	0x4001 3C00–0x4001 3FFF	1 KB	COMP
	0x4001 4000–0x4001 43FF	1 KB	TIM14
	0x4001 4400–0x4001 47FF	1 KB	TIM16
	0x4001 4800–0x4001 4BFF	1 KB	TIM17
	0x4001 4C00–0x4001 7FFF	13 KB	Reserved
	0x4002 0000–0x4002 03FF	1 KB	DMA
	0x4002 0400–0x4002 0FFF	3 KB	Reserved
	0x4002 1000–0x4002 13FF	1 KB	RCC
	0x4002 1400–0x4002 1FFF	3 KB	Reserved
	0x4002 2000–0x4002 23FF	1 KB	Flash Interface
	0x4002 2400–0x4002 2FFF	3 KB	Reserved
	0x4002 3000–0x4002 33FF	1 KB	CRC
AHB	0x4002 3400–0x4002 FFFF	47 KB	Reserved
	0x4003 0000–0x4003 03FF	1 KB	Reserved
	0x4003 0400–0x47FF FFFF	~ 127 MB	Reserved
	0x4800 0000–0x4800 03FF	1 KB	GPIOA
	0x4800 0400–0x4800 07FF	1 KB	GPIOB
	0x4800 0800–0x4800 0BFF	1 KB	GPIOC
	0x4800 0C00–0x4800 0FFF	1 KB	GPIOD
	0x4800 1000–0x5FFF FFFF	~ 384 MB	Reserved

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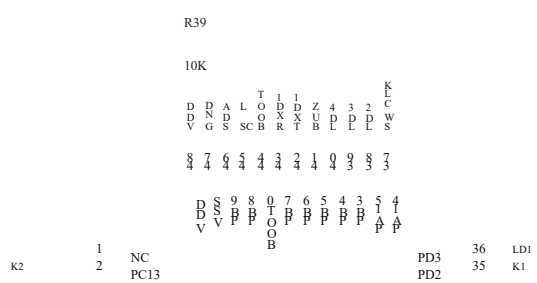
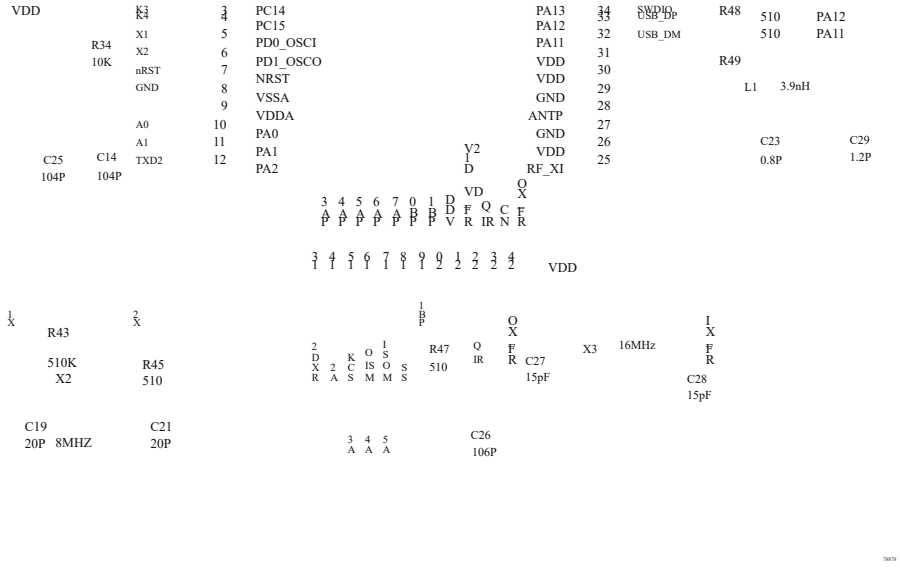
5

Typical application circuit





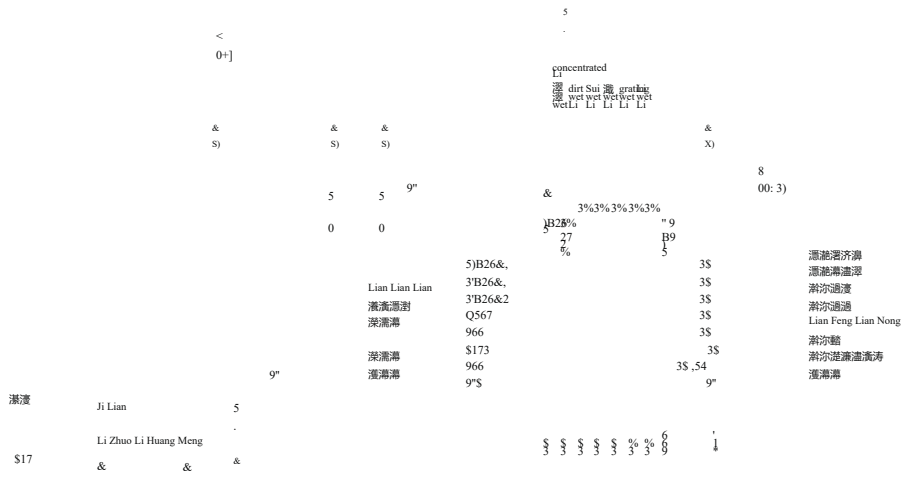
5. LQFP48

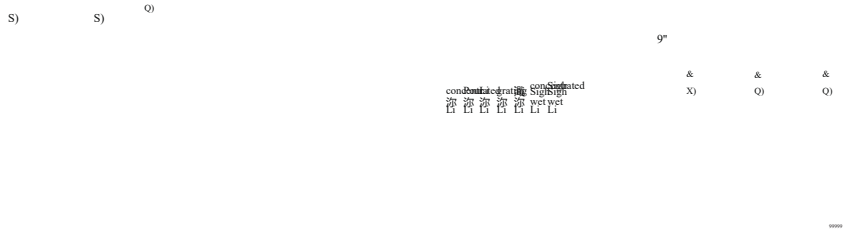
9.

R34, C14	Reset circuit
C25	Decoupling capacitor
R39	Start selection resistance
R43	Amplifier negative feedback resistance

Page 30

R45	Clock impedance matching resistance
X2	Main oscillator resistance
C19, C21	Crystal loading capacitor
C26	Internal regulator decoupling capacitor
C27, C28	Crystal loading capacitor
X3	RF clock crystal
C23, C29, L1	RF matching capacitor
R48, R49	USB impedance matching resistance





6. QFN32

Note: This typical application circuit uses the RF module and the control module to share a crystal oscillator solution. If the customer uses the internal clock of the control module, There is no need to add C1, and Pin2 can be used as GPIO.

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10.

C5, C8, C9	Decoupling filter capacitor
C2, C3	Crystal loading capacitor
C1	Shared clock capacitor
C4	1.2V digital regulator decoupling capacitor
C6, C11, L1	RF matching network capacitor
R4, C10	Reset circuit
R1	Start mode selection resistance
Y1	16MHz crystal oscillator (provided for RF module and control module Clock source)
J2	2.4G RF antenna

6

Electrical characteristics

6.1

Unless otherwise specified, all voltages are based on V SS .

6.1.1 number

Unless otherwise specified, typical data is based on T Å C and V DD = 3.3V. These data are only used for design guidance and not After testing.

6.1.2

Unless otherwise specified, typical curves are only for design guidance and not tested.

6.1.3

The load conditions when measuring pin parameters are shown in the figure below.

C = 50 pF

7.

6.1.4

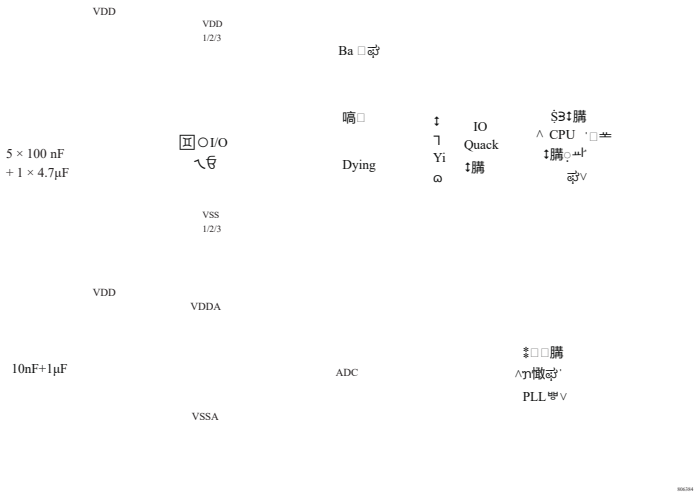
The measurement method of the input voltage on the pin is shown in the figure below.

V IN

8.

6.1.5

The power supply design scheme is shown in the figure below.



9.

6.1.6

The measurement method of current consumption on the pin is shown in the figure below.

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I DD

V DD

V DDA

10.

6.2 RF

11. RF

Label	parameter	Test Conditions	Minimum	Typical value	Max	unit
FREQ	Frequency change	V_{DD} = 3.0V, T_A = 25 ° C	2400		2,483.5	MHz
FC	Channel spacing	V_{DD} = 3.0V, T_A = 25 ° C		2		MHz
RFch	RF channel center	V_{DD} = 3.0V, T_A = 25 ° C	2402		2480	MHz

6.3 RF

12.

Label	parameter	Test Conditions	Minimum	Typical value	Max	unit
MOD	Modulation		GFSK			
BT	bandwidth			0.5		
M_{index}	Modulation index		0.45	0.5	0.55	
DR	Air transmission index			1		Mbps
P_{max}	Maximum transmission power				+4	dBm
P_{BW1M}	6dB bandwidth modulated carrier (1Mbps)		500			KHz
P_{SPUR}	Spurious emission				-41	dBm
CF_{dev}	Center frequency deviation				±150	KHz
$Freq_{drift}$	Frequency drift				±50	KHz
$IFreq_{drift}$	Initial carrier frequency drift				±20	KHz

6.4 RF

13. RF

Label	parameter	Test Conditions	Minimum	Typical value	Max	unit
RX_{SENS}	Receiving sensitivity	BER <0.1%		-80		dBm

6.5

If the load on the device exceeds the value given in the “Absolute Group Maximum Ra le 14, Table 15), it may
Will cause permanent damage to the device. Here is only the maximum load that can w..., ... does not mean that the device under this condition
Functional operation is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

14.

symbol	description	Minimum	Max	unit
V_{DD} -V_{SS}	External main supply voltage (including V_{DDA} and V_{SS}) (1)	-0.3	4.0	V
V_{IN}	Input voltage on other pins (2)	V_{SS} -0.3	V_{DD} + 0.3	

1. All power supply (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply within the allowable range System.
2. The maximum value of V_{IN} must always be observed . See the table below for the maximum allowable injection current value.

15.

symbol	description	Max	unit
I_{VDD}	Total current (supply current) through the V_{DD} /V_{DDA} power line (1)	120	mA
I_{VSS}	Total current (outgoing current) through the V_{SS} ground wire (1)	-120	
I_{IO}	Output sink current on any I/O and control pin	25	
	Output current on any I/O and control pin	-25	
$I_{INJ(PIN)}$ (2)(3)	Injection current of nRST pin	±5	

$I_{INJ(PIN)}$ (4)	The injection current of the OSC_IN pin of HSE	±5
	Injection current of other pins (4)	±25

1. All the power supply (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply within the allowable range System.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If you can not guarantee $V_{the\ IN}$ is not If it exceeds its maximum value, it is also necessary to ensure that the external limit $I_{INJ\ (PIN)}$ does not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a There is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\Sigma I_{INJ(PIN)}$ is the forward injection current and the reverse injection current The sum of the real-time absolute value of. This result is based on the characteristics of the maximum value of $\Sigma I_{INJ(PIN)}$ on all I/O ports of the device.

6.6

6.6.1

16.

symbol	parameter	condition	Minimum	Max	unit
f_{HCLK}	Internal AHB clock frequency		0	48MHz	
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	MHz
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Standard working voltage		2.3	3.6	V
P_D	T_A =85 ◦ C (1)				mW
T_A	T_A	Maximum power dissipation	-40	85	◦C
		Low power dissipation (2)	-40	105	
T_J	Junction temperature range		-40	105	◦C

1. It is recommended to use the same power supply to power V_{DD} and V_{DDA} .
2. If T_A is low, as long as T_J does not exceed T_{Jmax} (see Section 6. The 1), allowing a higher P_D value.

6.6.2

The parameters given in the following table are tested under general working conditions.

17.

symbol	parameter	condition	Minimum	Max	unit
t_{VDD}	V_{DD} rise rate	T_A = 25 ◦ C	1	∞	µS/V
	V_{DD} falling rate		500	∞	

6.6.3

The parameters given in the following table are based on testing under the ambient temperature and V_{DD} supply voltage listed in Table 16 .

18.

symbol	parameter	condition	Minimum	Typical value	Max	unit
V_{PVD}	Programmable voltage detection Detector level selection	PLS[3:0]=0000 (rising edge)		1.8		V
		PLS[3:0]=0000 (falling edge)		1.7		V
		PLS[3:0]=0001 (rising edge)		2.1		V
		PLS[3:0]=0001 (falling edge)		2.0		V
		PLS[3:0]=0010 (rising edge)		2.4		V
		PLS[3:0]=0010 (falling edge)		2.3		V
		PLS[3:0]=0011 (rising edge)		2.7		V
		PLS[3:0]=0011 (falling edge)		2.6		V
		PLS[3:0]=0100 (rising edge)		3.0		V
		PLS[3:0]=0100 (falling edge)		2.9		V
		PLS[3:0]=0101 (rising edge)		3.3		V

		PLS[3:0]=0101 (falling edge)		3.2		V

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symbol	parameter	condition	Minimum	Typical value	Max	unit
		PLS[3:0]=0110 (rising edge)		3.6		V
		PLS[3:0]=0110 (falling edge)		3.5		V
		PLS[3:0]=0111 (rising edge)		3.9		V
		PLS[3:0]=0111 (falling edge)		3.8		V
V_{PVD}	Programmable voltage detection Detector level selection	PLS[3:0]=1000 (rising edge)		4.2		V
		PLS[3:0]=1000 (falling edge)		4.1		V
		PLS[3:0]=1001 (rising edge)		4.5		V
		PLS[3:0]=1001 (falling edge)		4.4		V
		PLS[3:0]=1010 (rising edge)		4.8		V
		PLS[3:0]=1010 (falling edge)		4.7		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Flip point		1.65		V
$T_{RSTTEMPO}$	Reset duration			2.7		ms

1. Guaranteed by design, not tested in production.

Note: The reset duration is measured from power-on to the moment when the user application code reads the first instruction.

6.6.4

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include working voltage, ambient temperature, I/O Pin load, product software configuration, operating frequency, I/O pin flip rate, program location in memory and execution Lines of code, etc.

Refer to Figure 10 for the description of the current consumption measurement method .

The current consumption measurements in all operating modes given in this section are all executing a set of simplified codes.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 ~ 24 MHz is 0 wait cycles, 24 ~ 48 1 wait period at MHz).
- The instruction prefetch function is turned on. When the peripheral is turned on: $f_{PCLK1} = f_{PCLK2} = f_{HCLK}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

19. number

Externally provide **3.3V** DC voltage

Label	parameter	Test Conditions	Minimum	Typical value	Max	unit
I	Supply Current	MCU @ STANDBY mode, RF block @ STANDBY mode		3.5		uA
		MCU @ STOP mode, RF block @ STANDBY mode		5.8		

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Externally provide **3.3V** DC voltage

Label	parameter	Test Conditions	Minimum	Typical value	Max	unit

I	Supply Current	MCU @ STOP mode, RF block @ STOP mode		53.8	uA
		MCU @ SLEEP mode, RF block @ STOP mode		14.8 15.3	mA
		MCU @ ACTIVE mode, RF block @ RX mode		28	mA
		MCU @ ACTIVE, RF block @ TX mode	-3dBm	28	mA
			0dBm	30	
			+3dBm	36	

1. The measured power consumption parameters for TX and RX use HSI as the clock source and are configured as f_{HCLK} = 48MHZ, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, based on T_A = 25 °C and V_{DD} = the measured value of 3.3V.

20. (1)(2)

symbol	parameter	condition	Typical value			unit
			-40 ◦ C	25 ◦ C	85 ◦ C	
I_{DD}	Supply current in shutdown mode	PWR->CR[0] is set to 1	1.5	5.2	55.9	µA
	Supply current in standby mode	LSI and RTC are on	1.3	1.6	6.0	
		IWDG is on	0.5	0.5	5.1	

1. Resulted from comprehensive evaluation, not tested in production. The IO status is analog input.
2. The maximum value is tested when the power supply voltage is 3.3V.

The MCU is under the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 ~ 24 MHz is 0 wait cycles, 24 ~ 48 1 wait cycle at MHz
- The instruction prefetch function is turned on. When the peripheral is turned on: $f_{PCLK1} = f_{PCLK2} = f_{HCLK}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

twenty one. Data (1)(2)(3)(4)(5)

symbol	parameter	condition	f_{HCLK}	Enable all peripherals			Turn off all peripherals			unit
				-40 ◦ C	25 ◦ C	85 ◦ C	-40 ◦ C	25 ◦ C	85 ◦ C	
I_{DD}	run mode Down supply Current	internal clock	48MHz	15.70	16.00	16.30	8.37	8.07	8.24	mA
			24MHz	9.50	9.70	9.91	5.29	4.95	5.09	
			8MHz	5.19	5.30	5.42	3.10	2.67	2.75	
			4MHz	4.13	4.22	4.32	2.58	2.13	2.21	
			2MHz	3.62	3.69	3.78	2.32	1.86	1.93	
			1MHz	3.36	3.43	3.51	2.21	1.73	1.79	
			500K	3.23	3.29	3.38	2.14	1.67	1.73	
			125K	3.13	3.20	3.28	2.09	1.62	1.68	

1. All I/O pins are in input mode, and V_{DD} or V_{SS} are static values (no load);
2. All peripherals are in a prohibited state, unless explicitly stated
3. The FLASH access time complies with the user manual configuration

4. Tested when the power supply voltage is 3.3V

5. When the HCLK frequency is less than 8MHz, the system clock is obtained by dividing the HSI frequency

twenty two. Data (1)(2)(3)(4)(5)

symbol	parameter	condition	f_{HCLK}	Enable all peripherals			Turn off all peripherals			unit
				-40 ◦ C	25 ◦ C	85 ◦ C	-40 ◦ C	25 ◦ C	85 ◦ C	
I_{DD}	run mode Down supply Current	internal clock	48MHz	12.10	12.30	12.50	4.72	4.33	4.42	mA
			24MHz	7.64	7.79	7.94	3.46	3.04	3.11	
			8MHz	4.58	4.66	4.77	2.48	2.03	2.09	
			4MHz	3.83	3.90	4.00	2.28	1.82	1.87	
			2MHz	3.47	3.53	3.62	2.17	1.71	1.76	
			1MHz	3.28	3.35	3.43	2.11	1.65	1.71	
			500K	3.19	3.26	3.34	2.10	1.63	1.68	
			125K	3.13	3.19	3.27	2.08	1.61	1.66	

1. All I/O pins are in input mode, and V_{DD} or V_{SS} are static values (no load);

2. All peripherals are in a prohibited state, unless explicitly stated

3. The FLASH access time complies with the user manual configuration

4. Tested when the power supply voltage is 3.3V

5. When the HCLK frequency is less than 8MHz, the system clock is obtained by dividing the HSI frequency

The current consumption of the built-in peripherals is listed in Table 23, and the working conditions of the MCU are as follows:

• All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).

• All peripherals are turned off, unless otherwise specified.

• The value given is calculated by measuring current consumption

-Turn off the clock of all peripherals

- open only a peripheral clock

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• The ambient temperature and V_{DD} supply voltage conditions are listed in Table 16 .

twenty three. (1)

Built-in peripherals		**25** ◦ Classic at C Power consumption	unit	Built-in peripherals		**25** ◦ Classic at C Power consumption	unit
AHB	GPIOD	0.12	mA	APB2	TIM14	0.35	mA
	GPIOC	0.13			TIM16	0.38	
	GPIOB	0.12			TIM17	0.43	
	GPIOA	0.15			WWDG	0.09	
	CRC	0.20			SPI2	1.03	
	DMA	0.36		APB1	UART2	0.77	
	DBG	0.04			I2C1	1.19	
APB2	ADC1	0.28			TIM2	0.97	
	TIM1	1.28			TIM3	0.70	
	SPI1	0.97			PWR	0.23	
	COMP	0.20			CRS	0.13	
	SYSCFG	0.09					
APB2	UART1	0.78		APB1	USB	3.32	

1. f_{HCLK} = 96MHz, HSI is used as the PLL clock source.

6.6.5

The characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and power supply voltage confor Working conditions.

twenty four.

symbol	parameter	condition	Minimum	Typical value	Max	unit

f_{HSE_ext}	User external clock frequency (1)		8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low voltage	V_{SS}		$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time (1)	15			ns
$C_{in(HSE)}$	OSC_IN Input capacitive reactance (1)		5		pF
$DuCy_{(HSE)}$	Duty cycle		50		%

25.

symbol	parameter	condition	Minimum	Typical value	Max	unit
f_{NOM}	Nominal frequency			16		MHz
V_{TOL}	Frequency tolerance	Load capacitance, temperature			±50	ppm
ESR	Equivalent series				100	Ω
PD	Drive level				20	mA

1. Guaranteed by design, not tested in production.

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11. 2 ~ 24MHz

12. 16MHz

The characteristic parameters given in the following table are measured using a low-speed external clock source. The ambient temperature and power supply voltage conform to Working conditions.

26.

symbol	parameter	condition	Minimum	Typical value	Max	unit
f_{LSE_ext}	User external clock frequency (1)		16	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage	$0.7V_{DD}$			V_{DD}	V
V_{LSEL}	OSC_IN input pin low voltage	V_{SS}			$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time (1)	450				ns
$t_{r(LSE)}$	OSC_IN rising time (1)				50	ns
$t_{f(LSE)}$	OSC_IN falling time (1)				50	ns
$C_{in(LSE)}$	OSC_IN Input capacitive reactance (1)				10	pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-1		1	µA

1. Guaranteed by design, not tested in production.

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V LSEH
90%

10%
V LSEL

t r(LSE) t f(LSE) t w(LSE) t w(LSE) t

T LSE

f LSE_ext OSC32_IN I L

13.

/

The high-speed external clock (HSE) can be generated by an oscillator composed of a 2 ~ 24MHz crystal/ceramic resonator. this
The information given in the section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table be
fruit. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and start-up.
Stability time when moving. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding production
Vendor.

27. HSE 2 ~ 24MHz (1)(2)

symbol	parameter	condition	Minimum	Typical value	Max	unit
f OSC_IN	Oscillator frequency	2.0V<VDD<3.6V	2	8	12	MHz
		3.0V<VDD<3.6V	12	16	twenty four	
R F	Feedback resistance (4)			510		kΩ
ESR	Support crystal serial impedance (C L1 C L2 (3) is 16pF)	f OSC_IN = 24M V DD = 3.0V			60	Ω
		f OSC_IN = 12M V DD = 2.0V			150	
I 2	HSE drive current	f OSC_IN = 24M V DD = 2.0V ESR=30Ω C L1 C L2 (3) is 20pF		1.5		mA
g m	Transconductance of the oscillator	start up		9		mA/V
t SU(HSE) (5)	Start Time	V DD is stable		3		ms

1. The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
2. Resulted from comprehensive evaluation, not tested in production.

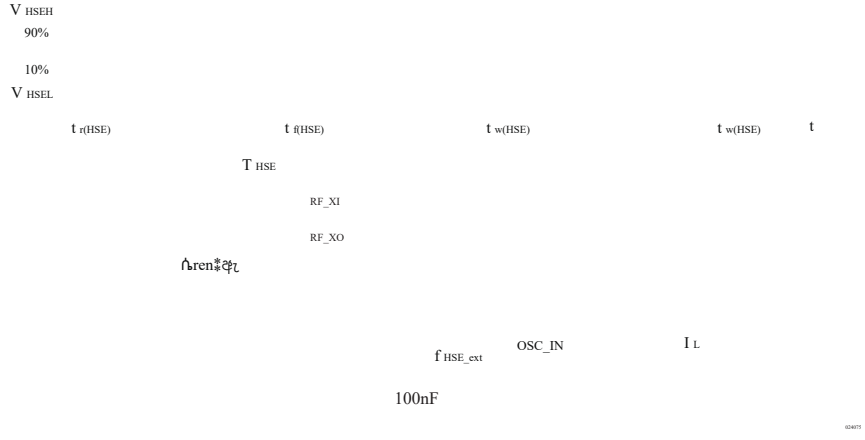
Page 43

3. For C L1 and C L2 , it is recommended to use high quality, designed for high frequency applications (typical value) between 5pF ~ 25pF

Ceramic capacitors, and choose a crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystals
The manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2} . When choosing C_{L1} and C_{L2} , PCB
The capacitive reactance with the MCU pin should be taken into account (the capacitance between the pin and the PCB board can be roughly estimated as 10pF).

4. The relatively low R_F resistance value can provide protection to avoid problems caused by use in a humid environment.
The leakage and bias conditions generated in this environment have changed. However, if the MCU is used in harsh tides
In wet conditions, this parameter needs to be taken into consideration when designing.

5. $t_{SU(HSE)}$ is the start-up time, which is measured from the software enabling HSE until a stable 8MHz oscillation is obtained
time. This value is measured on a standard crystal resonator, it may vary depending on the crystal manufacturer
big change.



14.

Note: 1. The AC timing diagram of the external high-speed clock source indicates that the control module and the RF module share a 16MHz crystal/ceramic
Porcelain resonator, 16MHz crystal/ceramic resonator mainly provides high-speed clock for RF module, and a 100nF is also connected in series
The capacitor provides a high-speed clock for the control module.

2. If the user uses the internal clock source of the control module, a 16MHz crystal/ceramic resonator is provided separately for the RF module
bell.

/

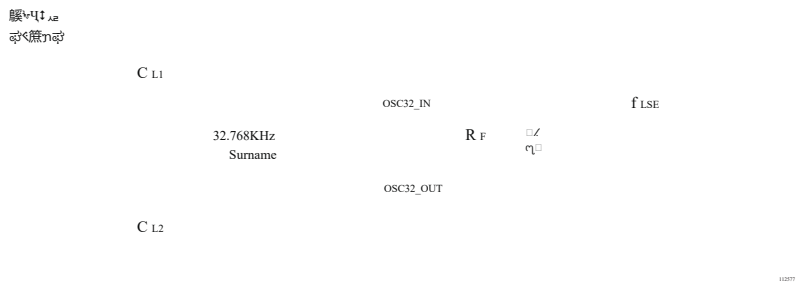
The low-speed external clock (LSE) can be generated by an oscillator composed of a 32.768KHz crystal/ceramic resonator. this
The information given in the section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table be
fruit. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and start-up.
Stability time when moving. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding production
Vendor. (Annotation: The crystal resonator mentioned here is what we usually call a passive crystal oscillator) Note: For C_{L1} and C_{L2} ,
It is recommended to use high-quality ceramic capacitors between 5pF ~ 15pF, and choose a crystal or resonator that meets the requirements. through
Often C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give the load capacitance in the serial combination of C_{L1} and C_{L2}
parameter. The load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin
The typical value of the capacitance is between 2pF ~ 7pF and the capacitance related to the PCB board or PCB. Warning: To avoid

Avoid exceeding the maximum value of C_{L1} and C_{L2} (15pF). It is strongly recommended to use a resonator with a load capacitance CL ≤ 7pF.
Use a resonator with a load capacitance of 12.5pF. For example: If a resonator with a load capacitance CL = 6pF is selected and
C_{stray} = 2pF, then $C_{L1} = C_{L2}$ = 8pF.

28. LSE (f_{LSE} =32.768KHz) (1)

symbol	parameter	condition	Minimum	Typical value	Max	unit
g_m	Transconductance of the oscillator			78		μA/V
$t_{SU(HSE)}$ (2)	Start Time	R_S = 30kΩ		3		S

1. Resulted from comprehensive evaluation, not tested in production.
2. $t_{SU(HSE)}$ is the start-up time, which is measured from the software enable HSE until a stable 8MHz oscillation is obtained
time. This value is measured on a standard crystal resonator, it may vary depending on the crystal manufacturer
big change.



15. 32.768KHz

6.6.6

The characteristic parameters given in the following table are measured when the ambient temperature and supply voltage meet the general working conditions.

(HSI)

29. HSI (1)(2)

symbol	parameter	condition	Minimum	Typical value	Max	unit
f_{HSI}	frequency			48		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = 25	-1		1	%
$t_{SU(HSI)}$	HSI oscillator start time			12	16	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			328		µA

1. V_{DD} = 3.3V, unless otherwise specified.
2. Guaranteed by design, not tested in production.

(LSI)

30. LSI (1)

symbol	parameter	condition	Minimum	Typical value	Max	unit
f_{LSI} (2)	frequency			40		KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time				85	µs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption			1	1.4	µA

1. V_{DD} = 3.3V unless otherwise specified.
2. Resulted from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

The wake-up time listed in the table below is measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current Depending on the mode of operation:

- Stop or standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and power supply voltage in accordance with general working conditions.

31.

symbol	parameter	condition	Max	unit
$t_{WUSLEEP}$ (1)	Wake up from sleep mode	HSI is the system clock	2.7	µs
t_{WUSTOP} (1)	Wake up from stop mode (Voltage regulator is in operation)	HSI is the system clock	5.5	µs
t_{WUSTOP} (1)	Wake up from stop mode (Voltage regulator is in low power consumption state)	HSI is the system clock	7.7	µs
$t_{WUSTDBY}$ (1)	Wake up from standby mode	PWR->CR[15:14]=0x00	498	µs

$t_{WUSTDBY}$ (1)	Wake up from standby mode	PWR->CR[15:14]=0x01	430		µs
$t_{WUSTDBY}$ (1)	Wake up from standby mode	PWR->CR[15:14]=0x02	390		µs
$t_{WUSTDBY}$ (1)	Wake up from standby mode	PWR->CR[15:14]=0x03	318		µs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

6.6.7 PLL

The parameters listed in the following table are measured using ambient temperature and power supply voltage in accordance with general working conditions.

32. PLL (1)

symbol	parameter	Minimum	Typical value	Max	unit
f_{PLL_IN}	PLL input clock (2)	4		twenty four	MHz
f_{PLL_IN}	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	40		200	MHz
t_{LOCK}	PLL lock time			100	µs

1. Guaranteed by design, not tested in production.

2. It is necessary to pay attention to using the correct frequency multiplication factor, so that f_{PLL_OUT} is in the allowable range according to the PLL input clock frequency. Inside.

6.6.8

33.

symbol	parameter	condition	Minimum	Typical value	Max	unit
t_{prog}	8-bit programming time		6		7.5	µs
t_{ERASE}	Page erase time		4		5	ms
t_{ME}	Whole chip erase time		20		40	ms
I_{DD}	Supply current	Read mode		4		mA
		Write mode			7	mA
		Erase mode			2	mA
V_{prog}	Programming voltage			1.5		V

34. Data (1)(2)

symbol	parameter	condition	Minimum	Typical value	Max	unit
NEND	Life (erasable frequency)		20			Thousand times
t_{RET}	Data retention period	T_A = 25 ° C	100			year

1. Resulted from comprehensive evaluation, not tested in production.

6.6.9 EMC

Sensitivity testing is carried out by sampling during the comprehensive evaluation of the product.

EMC evaluation and optimization at the device level are carried out in a typical application environment. It should be noted that good EMC performance is closely related to user applications and specific software.

Therefore, it is recommended that users implement EMC optimization on the software and conduct certification tests related to EMC.

The software flow must include the control of program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc...)

Many common failures (unexpected resets and program counters are destroyed) can be manually introduced on NRST
Low level or introduce a low level on the crystal oscillator pin for 1 second to reproduce.

During the ESD test, the voltage exceeding the application requirements can be directly applied to the chip. When an unexpected action is detected
Locally, the software part needs to be strengthened to prevent unrecoverable errors.

6.6.10 ( )

Based on three different tests (ESD, LU), using specific measurement methods, the chip strength test to determine its
Performance in terms of electrical sensitivity.

(ESD)

Electrostatic discharge (a positive pulse and then a negative pulse after one second interval) is applied to all the pins of all samples,
The size of the sample is related to the number of power supply pins on the chip (3 pieces x (n + 1) power supply pins). This test complies with JEDEC
JS-001-2017/JS-002-2018 standard.

In order to evaluate the latching performance, 2 complementary static latching tests need to be performed on 6 samples:

- Provide a supply voltage exceeding the limit for each power supply pin.
- Inject current into each input, output, and configurable I/O pin.

This test complies with the EIA/JESD78E integrated circuit latch standard.

35. MCU ESD

symbol	parameter	condition	Max	unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 ◦ C, in line with JEDEC JS-001-2017	±8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = 25 ◦ C, in line with JEDEC JS-002-2018	±2000	V
I_{LU}	Static latch type (Latch-up current)	T_A = 25 ◦ C, in line with JESD78E	±100	mA

6.6.11 I/O

/

Unless otherwise specified, the parameters listed in the following table are in accordance with the table The condition of 14 is measured. All I/O ports are compatible
CMOS.

36. I/O

symbol	parameter	condition	Minimum	Typical value	Max	unit
V_{IL}	Input low level voltage	V_{DD} = 3.3V	-0.3		0.8	V
V_{IH}	Input high level voltage	V_{DD} = 3.3V	2.3		3.6	V
V_{hys}	I/O pin Schmitt trigger voltage hysteresis (1)	V_{DD} = 3.3V	0.1V_{DD}			V
I_{lkg}	Input leakage current (2)	V_{DD} = 3.3V			1	µA
R_{PU}	Weak pull-up equivalent resistance (3)	3.3V V_{IN} =V_{SS}	twenty two		100	kΩ
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V V_{IN} =V_{SS}	20		50	kΩ
C_{IO}	I/O pin capacitance	3.3V			10	pF

1. The hysteresis voltage of Schmitt trigger switching level. Resulted from comprehensive evaluation, not tested in production.

2. If there is reverse current in the adjacent pin, the leakage current may be higher than the maximum value.

3. The pull-up and pull-down resistors are MOS resistors.

GPIO (General Purpose Input/Output Port) can sink or output up to ±20mA current.

In the user application, the number of I / O pins must ensure that the drive current does not exceed 6 . Absolute maximum ratings given in Section 5:

- The sum of the currents obtained by all I/O ports from V_{DD} , plus the maximum operating current obtained by the MCU on V_{DD} , does not Can exceed the absolute maximum rating I_{VDD} .
- The sum of the current absorbed by all I/O ports and flowing out of V_{SS} , plus the maximum operating current of the MCU on V_{SS} Current, cannot exceed the absolute maximum rating I_{VSS} .

Unless otherwise specified, the parameters listed in the following table are measured using ambient temperature and V_{DD} supply voltage in accordance with the conditions in Ta To. All I/O ports are CMOS compatible.

37. (1)(2)

MODEx[1 : 0] Configuration	symbol	parameter	condition	Typical value	unit
11	V_{OL}	Output low level	I_{IO} =8mA,	0.4	V
	t_{OH}	Output high level	V_{DD} =3.3V	V_{DD} -0.4	
	V_{OL}	Output low level	I_{IO} =20mA,	0.3*V_{DD}	
	t_{OH}	Output high level	V_{DD} =3.3V	0.6*V_{DD}	
10	V_{OL}	Output low level	I_{IO} =6mA,	0.4	
	t_{OH}	Output high level	V_{DD} =3.3V	V_{DD} -0.4	
	V_{OL}	Output low level	I_{IO} =8mA,	0.4	
	t_{OH}	Output high level	V_{DD} =3.3V	V_{DD} -0.4	
	V_{OL}	Output low level	I_{IO} =20mA,	0.2*V_{DD}	
	t_{OH}	Output high level	V_{DD} =3.3V	0.8*V_{DD}	
01	V_{OL}	Output low level	I_{IO} =6mA,	0.4	
	t_{OH}	Output high level	V_{DD} =3.3V	V_{DD} -0.4	
	V_{OL}	Output low level	I_{IO} =8mA,	0.4	
	t_{OH}	Output high level	V_{DD} =3.3V	V_{DD} -0.4	
	V_{OL}	Output low level	I_{IO} =20mA,	0.2*V_{DD}	
	t_{OH}	Output high level	V_{DD} =3.3V	0.8*V_{DD}	
	V_{OL}	Output low level	I_{IO} =6mA,	0.4	
	t_{OH}	Output high level	V_{DD} =3.3V	V_{DD} -0.4	

1. Resulted from comprehensive evaluation, not tested in production.

The definitions and values of the input and output AC characte ı in Figure 16 and Table 38 , respectively .

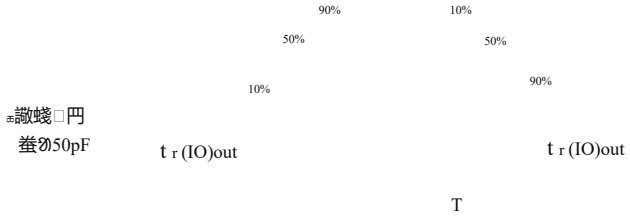
Unless otherwise specified, the parameters listed in Table 38 are measured when the aml re and supply voltage meet the conditions in Table 14.

38. (1)(2)

MODEx[1 : 0] Configuration	symbol	parameter	condition	Typical value	unit
11	$t_{f(IO)out}$	Output fall time	C_L =50pF, V_{DD} =3.3V	7.20	ns
	$t_{r(IO)out}$	Output rise time		7.20	
10	$t_{f(IO)out}$	Output fall time		4.40	
	$t_{r(IO)out}$	Output rise time		4.40	
01	$t_{f(IO)out}$	Output fall time		3.73	
	$t_{r(IO)out}$	Output rise time		3.73	

1. The speed of the I/O port can be configured through MODEx[1:0]. Refer to the GPIO port in this chip reference manual Description of configuration registers.

2. Guaranteed by design, not tested in production.



□□((t r + t f) ≤ 2/3)T'Γфϑオヨϑ(45 ~ 55%)
It's 50pF, and it's not too much.

16.

6.6.12 NRST

The NRST pin input driver uses CMOS technology, which is connected with a pull-up resistor, R PU , which cannot be disconnected .

Unless otherwise specified, the parameters listed in the following table are measured using ambient temperature and V DD supply voltage in accordance with the conditions in Ta
To.

39. NRST

symbol	parameter	condition	Minimum	Typical value	Max	unit
V IL(NRST) (1)	NRST input low level voltage		-0.3		0.8	V
V IH(NRST) (1)	NRST input high level voltage		2.3		3.6	
V hys(NRST)	NRST Schmitt trigger voltage delay Stagnation		0.1*V DD			V
R PU	Weak pull-up equivalent resistance (2)	V IN = V SS	twenty two		100	kΩ

symbol	parameter	condition	Minimum	Typical value	Max	unit
V F(NRST) (1)	NRST input filter pulse				1000	ns
V NF(NRST) (1)	NRST input unfiltered pulse		4000			ns

1. Guaranteed by design, not tested in production.
2. The pull-up resistor is a MOS resistor.

(1)
V DD
R PU
NRST (2)
0.1μF

17. NRST

1. The reset network is to prevent parasitic reset.

2. The user must ensure that the potential of the NRST pin can be lower than the maximum V IL (NRST) listed in Table 39 , otherwise the MCU Can't get reset.

6.6.13 TIM

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input/output multiplex function pins (output compare, input capture, external clock, PWM output), refer to See subsection 6.6.11 .

40. TIMx (1)

symbol	parameter	condition	Minimum	Max	unit
t res(TIM)	Timer to distinguish time		1		t TIMxCLK
t res(TIM)	Timer to distinguish time	f TIMxCLK =96MHz	10.4		ns
f EXT	When the timer of CH1 to CH4 is external Clock frequency	f TIMxCLK =96MHz	0 0	f TIMxCLK/2 48	MHz
Res TIM	Timer resolution			16	Bit
t COUNTER	When the internal clock is selected, 16-bit Counter clock period	f TIMxCLK 96MHz	1 0.0104	65536 682.6	t TIMxCLK µs

symbol	parameter	condition	Minimum	Max	unit
t MAX_COUNT	Maximum possible count	f TIMxCLK 96MHz		65536 ×65536 44.7	t TIMxCLK s

1. TIMx is a common name.

6.6.14

I2C

Unless otherwise specified, the parameters listed in Table 41 are the operating environment temperature, f PCLK1 frequency and V DD supply voltage meet the requirements of Tal The conditions are measured.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not'true' pins, when configured When it is an open-drain output, the PMOS tube between the pin and V DD is turned off, but it still exists.

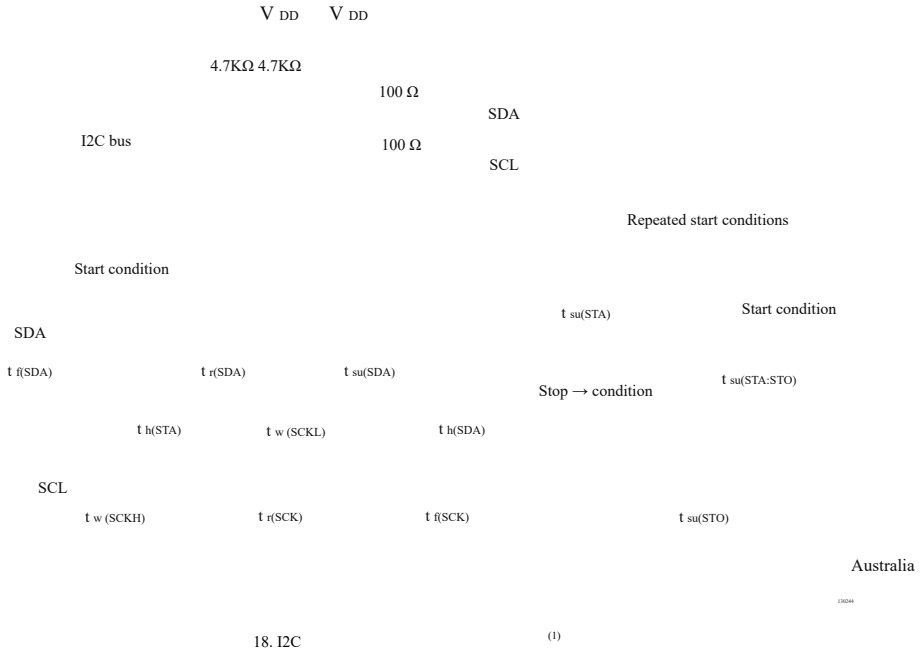
The characteristics of the I2C interface are listed in Table 41. For details on the characteristics of the input and output ıte function pins (SDA and SCL), see the Section 6.6.11 .

41. I2C

symbol	parameter	Standard **I2C** (1)		Fast **I2C** (1)(2)		unit
		Minimum	Max	Minimum	Max	
t w(SCLL)	SCL clock low time	8*t PCLK		8*t PCLK		µs
t w(SCLH)	SCL clock high time	6*t PCLK		6*t PCLK		µs
t su(SDA)	SDA establishment time	2*t PCLK		2*t PCLK		ns
t h(SDA)	SDA data retention time	0 (3)		0 (4)	875 (3)	ns
t r(SDA) t r(SDL)	SDA and SCL rise time		1000		300	ns
t f(SDA) t f(SDL)	SDA and SCL fall time		300		300	ns
t h(STA)	Start condition hold time	8*t PCLK		8*t PCLK		µs
t su(STA)	Repeated start condition establishment time	6*t PCLK		6*t PCLK		µs
t su(STO)	Stop condition establishment time	6*t PCLK		6*t PCLK		µs
t w(STO:STA)	From the stop condition to the start condition Time (bus free)	5*t PCLK		5*t PCLK		µs
C b	Capacitive load of each bus	4.7		1.2		pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of standard mode I2C, f PCLK1 must be greater than 3MHz. To reach the maximum of I2C in fast mode The frequency, f PCLK1 must be greater than 12MHz.
3. If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the start condition is required.
4. In order to cross the undefined area on the falling edge of SCL, the MCU must ensure that the SDA signal is at least 300nS

The hold time.



18. I2C (1)

1. The measurement points are set at CMOS level: 0.3V DD and 0.7V DD .

SPI

Unless otherwise indicated in Table 42 lists the parameters are ambient temperature, F PCLKx frequency and V DD supply voltage in accordance with Table 16 is The conditions are measured.

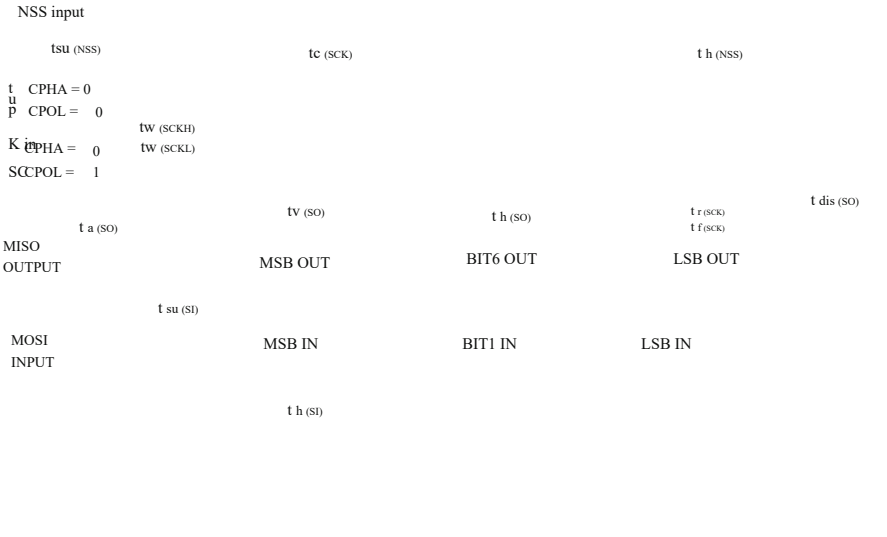
For details on the characteristics of the input and output alternate function pins (NSS, SCK, MOSI, MISO), see section 6.6.11 .

42. SPI (1)

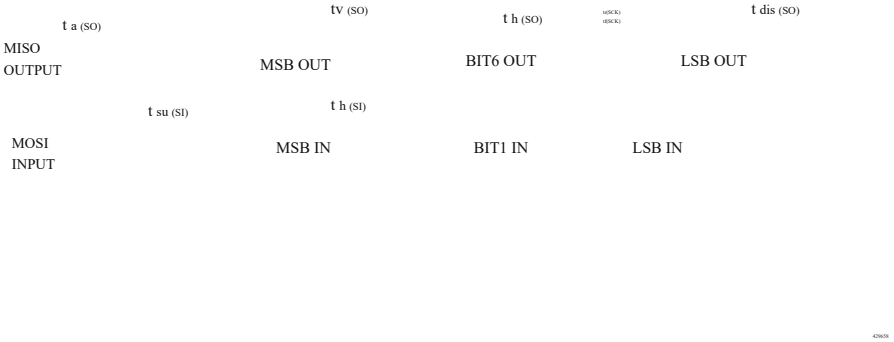
symbol	parameter	condition	Minimum	Max	unit
f SCK 1/t c(SCK)	SPI clock frequency	Master mode		twenty four	MHz
f SCK 1/t c(SCK)	SPI clock frequency	Slave mode		12	MHz
t r(SCK)	SPI clock rise and fall time	Load capacitance: C= 15pF		6	ns
t f(SCK)	SPI clock rise and fall time	Load capacitance: C= 15pF		6	ns
t su(NSS) (2)	NSS establishment time	Slave mode	1T PCLK		ns
t h(NSS) (2)	NSS hold time	Slave mode	2T PCLK		ns
t w(SCKH) (2)	SCK high time		t c(SCK)/ 2-6	t c(SCK)/ 2-6	ns
t w(SCKL) (2)	SCK low time		t c(SCK)/ 2-6	t c(SCK)/ 2-6	ns
t su(MI) (2)	Data input establishment time	Master mode, f PCLK = 48MHz, Prescaler factor = 2 high speed mode	12		ns

symbol	parameter	condition	Minimum	Max	unit
$t_{su(SI)}$ (2)	Data input establishment time	Slave mode	5		ns
$t_{h(MI)}$ (2)	Data input hold time	Master mode, f_{PCLK} = 48MHz, Prescaler factor = 2 high speed mode	0		ns
$t_{h(SI)}$ (2)		Slave mode	6		ns
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge) Non-high speed mode		34	ns
$t_{h(SO)}$ (2)		Slave mode (after enable edge) High speed mode		13	
$t_{h(MO)}$ (2)	Data output valid time	Master mode (after enabling edge)	-0.6	2	ns

1. Resulted from comprehensive evaluation, not tested in production.
2. The minimum value indicates the minimum time to drive the output, and the maximum value indicates the maximum time to obtain the data correctly.
3. The minimum value represents the minimum time to turn off the output, and the maximum value represents the maximum time to put the data line in a high impedance state.



19. SPI -CPHA = 0



20. SPI -CPHA = 1 (1)

1. The measurement points are set at CMOS level: 0.3V DD and 0.7V DD .

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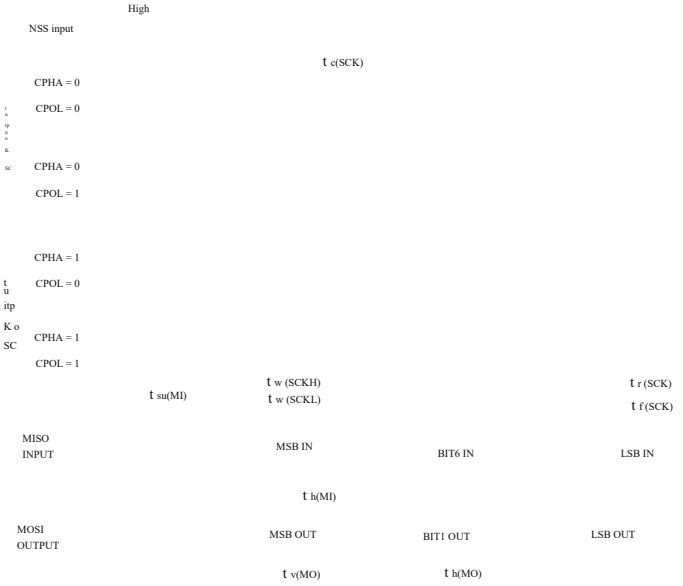

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21. SPI - (1)

1. The measurement points are set at CMOS level: 0.3V DD and 0.7V DD .

USB

43. USB

symbol	parameter	condition	Minimum (1)	Maximum (1)	unit
		Input level			
V DD	USB operating voltage (2)		3.0 (3)	3.6	V
V DI (4)	Differential input sensitivity	I(USBDP, USBDM)	0.2		
V CM (4)	Differential common mode range	Include V DI range	0.8	2.5	
V SE (4)	Single-ended receiver threshold		1.3	2	
		Output level			
V OL	Static output low level	1.5kΩ R L is connected to 3.6V (5)		0.3	V
V OH	Static output high level	15kΩ R L is connected to V SS (5)	2.8	3.6	

1. All voltage measurements are based on the ground wire of the device terminal.
2. In order to be compatible with USB 2.0 full-speed electrical specifications, a 1.5 kΩ resistor has been built into the USBDP(D+) pin

Connect to V DD , no need to connect externally.

3. The correct USB function of this product can be guaranteed at 2.7 V, instead of falling in the voltage range of 2.7 V to 3.6 V Electrical characteristics.
4. Guaranteed by comprehensive evaluation, not tested in production.
5. RL is the load connected to the USB drive.

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V_{CRS}

V_{SS} t_f t_r

512206

22. USB data Australia

6.6.15 12 ADC

Unless otherwise specified, the parameters in the following table are to use ambient temperature, f PCLK2 frequency and V DDA power supply that meet the conditions in Table 16 The voltage is measured.

44. ADC

symbol	parameter	condition	Minimum	Typical value	Max	unit
V DDA	Supply voltage		2.5	3.3	3.6	V
f ADC (1)(3)	ADC clock frequency				16	MHz
f S (1)(3)	Sampling rate				1	MHz
f TRIG (1)	External trigger frequency	f ADC = 15MHz			937.5	KHz
f TRIG (1)	External trigger frequency				16	1/f ADC
V AIN (2)	Conversion voltage range (3)		0		V DD	V
R AIN (1)	External input impedance			See formula 1 and table 45		kΩ
R ADC (1)	Sampling switch resistance				1.5	kΩ
C ADC (1)	Internal sample and hold power Content				10	pF
t S (1)	sampling time	f ADC = 16MHz	0.156		15.031	µs

			2.5	240.5	1/f ADC
t_{conv} (1)	Total conversion time	f_{ADC} = 16MHz	1	15.8125	μs
	(Including sampling time)		15 ~ 253 (sampling t_S) gradually approach	12.5	1/f ADC

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. In this series of products, V_{REF+} is internally connected to V_{DDA} , and V_{REF-} is internally connected to V_{SSA} .

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times In(2^{N+2})} - R_{ADC}$$

The above formula (Equation 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N = 12 (table Shows 12-bit resolution).

45. f_{ADC} =15MHz (1) R_{AIN}

T_S (period)	**t_S (μs)**	Maximum **R_{AIN} (kΩ)**
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

46. ADC - (1)(2)

symbol	parameter	Test Conditions	Typical value	Max	unit
Resoluion	Resolution		12		BIT
ET	Composite error		3.4/-2.3		
EO	Offset error	f_{PCLK2} = 24MHz,	-2.5		
EG	Gain error	f_{ADC} = 12MHz, R_{AIN} <0.1KΩ,	3.7		LSB
ED	Differential linearity error	V_{DDA} = 3.3V, T_A = 25 ° C	1/-1		
EL	Integral linearity error		1.8/-3		

1. The relationship between ADC accuracy and reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin. Flow, because this will significantly reduce the accuracy of the conversion being performed on the other analog input pin. It is recommended to produce Add a Schottky diode to the standard analog pin that generates reverse injection current (between the pin and ground).
   If the forward injection current, as long as the section is 6.6. The I given in 12 $I_{INJ(PIN)}$, and [Sigma] $I_{INJ(PIN)}$ within range, it Will not affect ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

ET = total unadjusted error: the maximum deviation between the actual and ideal transmission curves.

EO = Offset error: the deviation between the first actual conversion and the first ideal conversion.

EG = gain error: the deviation between the last ideal conversion and the last actual conversion.

ED = Differential linearity error: the maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: the maximum deviation between any actual conversion and the endpoint correlation line.

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R AIN (1) AINx R ADC (1) 12u

Surname

C parasi c (2)

V AIN

C ADC (1)

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twenty threeADC

1. For the values of R_{AIN} , R_{ADC} and C_{ADC} , see Table 46 .
2. $C_{parasitic}$ represents the parasitic capacitance (about 7pF) on the PCB (related to soldering and PCB layout quality) and pads. More A large $C_{parasitic}$ value will reduce the accuracy of the conversion. The solution is to reduce f_{ADC} .

PCB

The decoupling of the power supply must be connected according to the following figure. The 10 nF capacitors in the picture must be ceramic capacitors, and they should be as Near the MCU chip.

V_{DDA}

V_{DDA}

1 μF // 10 nF

V_{SSA}

Australia

twenty four.

6.6.16

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47. (3)(4)

symbol	parameter	Minimum	Typical value	Max	unit
T_L (1)	Linearity of V_{SENSE} with respect to temperature		±5		◦C
Avg_Slope (1)	Average slope	4.571	4.801	5.984	mV/ ◦ C
V_{25} (1)	ADC sampling value at 25 ◦ C		offset (5)		
t_{start} (2)	Establishment time			10	μs
T_{S_temp} (2)	When reading temperature, ADC sampling time	10			μs

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined by the application through multiple cycles.
4. V_{DD} = 3.3V.
5. Temperature formula: TS_adc = 25 + (value * V_{DDA} -offset * 3300)/(4096 * Avg_Slope), offset is recorded
   Recorded in the lower 12 bits of 0x1FFFF7F6, value is the conversion result data of ADC.

6.6.17

48.

symbol	parameter	Register configuration	Minimum	Typical value	Max	unit
HYST	Hysteresis	00		0		mV
HYST	Hysteresis	01		15		mV
HYST	Hysteresis	10		30		mV
HYST	Hysteresis	11		90		mV
OFFSET	Offset voltage	00	0.091	0.213	0.358	mV
OFFSET	Offset voltage	01	3.23	7.51	12.08	mV
OFFSET	Offset voltage	10	9.79	15	20.8	mV
OFFSET	Offset voltage	11	34.25	47.4	62.22	mV
DELAY (1)	Propagation delay	00		80		ns
DELAY (1)	Propagation delay	01		51		ns
DELAY (1)	Propagation delay	10		26		ns
DELAY (1)	Propagation delay	11		9		ns
I_q (2)	Average working current	00		4.5		µA
I_q (2)	Average working current	01		4.4		µA
I_q (2)	Average working current	10		4.4		µA
I_q (2)	Average working current	11		4.4		µA

1. The time difference between the 50% output flip and the input flip.
2. Average value of total current consumption, working current.

7 PCB

PCB design recommendations

7.1

The decoupling of the power supply must be connected according to the following figure. The 10nF capacitors in the picture must be ceramic capacitors, and they should be as c
Near the MCU chip.

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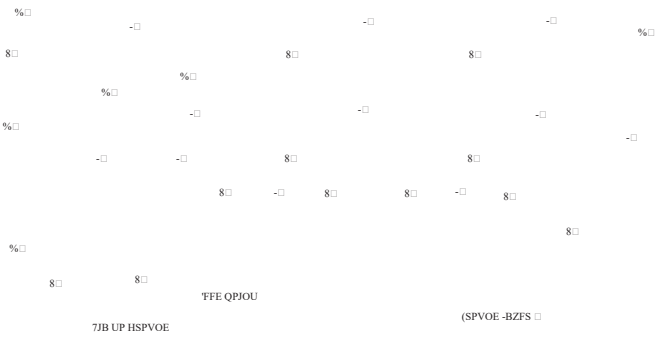
7.2 PCB

Bluetooth works in the 2.4G wireless frequency band, and should try to avoid the influence of various factors on wireless transmission and reception, pay attention to the follow

- Avoid using metal in the product shell surrounding the Bluetooth module. When using a partial metal shell, try to keep the antenna part of the module Keep away from metal parts.
- The metal connecting wires or metal screws inside the product should be as far away from the antenna part of the module as possible.
- The antenna part of the module should be placed around the PCB of the carrier board. It is not allowed to be placed in the board, and the carrier board under the antenna is mil In the parallel direction, copper laying or routing is not allowed. It is also a better choice to expose the antenna part directly to the carrier board.
- Try to spread a large piece of GND under the module, and try to extend the wiring to the periphery.
- It is recommended to use insulating material to isolate the module mounting position on the substrate, such as placing a whole piece of silk screen at this position (TopOverLay).
- The wiring of the power cord and ground wire is directly related to the performance of the product and minimizes noise interference. Try your best when wiring Widen the width of ground wire and power wire, ground wire> power wire> signal wire, usually signal wire width is 0.2 ~ 0.3mm, power wire The width is 1.2 ~ 2.5mm, and a large area of copper layer is used as the ground wire, and the useless space is laid out on the PCB.
- The power supply plus two decoupling filter capacitors: if using LDO power supply, the values are 1uF and 0.1uF respectively for filtering; If it is powered by a button battery, the values are 10uF and 10uF respectively for voltage stabilization.
- The trace between the chip ANT and the antenna should not be too long, and the line width should consider impedance matching requirements.

7.3 2.4G

The size of a small antenna may change significantly due to the impact of performance. Therefore, it is strongly recommended to Accurate reference design to achieve the best performance. When drawing a PCB antenna, refer to the dimensions given in the figure below to draw the antenna.



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Label	Typical value **(mm)**
L1	3.94
L2	2.70
L3	5.00
L4	2.64
L5	2.00
L6	4.90
W1	0.90

W2	0.50
D1	0.50
D2	0.30
D3	0.30
D4	0.50
D5	1.40
D6	1.70

8 Package characteristics

8.1 LQFP48

27. LQFP48, 48

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

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50. LQFP48

Label	Mm		
	Minimum	Typical value	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.27
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	-	0.70
L1		1.00REF	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
θ	0°	3.5°	7°
θ 1	11°	12°	13°
θ 2	11°	12°	13°

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8.2 QFN32

D A2

A

28. QFN32, 32

1. The figure is not drawn to scale.
2. The dimensions are in millimeters.

51. QFN32

Label	Mm		
	Minimum	Typical value	Max
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60

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Label	Mm		
	Minimum	Typical value	Max
E2	3.40	3.50	3.60
e		0.5	
H		0.30REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.09		
c1		0.08	
c2		0.08	
N		Number of pins = 32	

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9 Model naming

MM32 W 0 6 2 P F B

Device family

MM32 = ARM-base 32-bit microcontroller

Product type

W = Wireless

Sub-family

0 = Cortex M0

User code memory size

6 = 64 Kbytes

Func on family

2 = Support ADC, USB
1 = Support ADC

Package

P = LQFP
N = QFN

Pin count

F = 48 Pins
T = 32 Pins

Wireless type

B = BLE

902739

29. MM32

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10

Modify record

52.

date	version	content
2020/07/02	Rev 1.00	formal edition