Datasheet

MM32F0010

32-Bit Microcontroller Based on ARM® Cortex® M0

Version: 1.00

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1 General Introduction

General Introduction

1.1 Introduction

This product is a 32-bit microcontroller using the high-performance ARM® Cortex®-M0 as the kernel. The highest operating frequency is up to 72MHz. It has built-in high speed memory, rich enhanced I/O ports and peripherals which are connected to the external bus. This product contains one 12-bit ADC, one 16-bit universal timer, one 16-bit basic timer and one 16-bit advanced timer. It also contains standard communication interfaces: one I2C interface, one SPI interface and two UART interfaces.

The operating voltage of this product series is 2.0V~5.5V. The operating temperature range of conventional type is -40°C~+85°C. Multiple power-down modes are provided to ensure the requirements of low-power applications.

The product is available for two types of packages: QFN20 and TSSOP20.

The configuration of peripherals for the product varies according to different packages.

Rich peripherals make the microcontroller suitable for a variety of applications:

- Motor drive and application control
- Medical and hand-hold devices
- PC game peripherals and GPS platforms
- Industrial applications: programmable logic controllers (PLC), frequency converters, printers and scanners
- Alarm systems, video intercom systems, heating, ventilation and air conditioning systems

1.2 Product Characteristics

- Kernel and system
  - 32-bit ARM® Cortex®-M0 processor as the kernel
  - Highest operating frequency up to 72MHz
  - Single instruction cycle 32-bit hardware multiplier
- Memory
  - Flash memory up to 16K bytes
  - SRAM up to 2K bytes
  - Boot loader supports embedded flash and In System Programming (ISP)
- Clock, reset, and power management

  - Power supply 2.0V~5.5V
  - Power-on reset/Power down reset (POR/PDR), programmable voltage detector (PVD)
  - POR reset voltage as low as 1.7V.
  - PVD voltage threshold as low as 1.8V.
  - External 2~24MHz high speed crystal oscillator
  - Embedded 48 MHZ high speed oscillator with factory calibration
  - Embedded 32.768K low speed oscillator
- Low power consumption
  - Sleep mode, shutdown mode and standby mode
- One 12-bit analog-to-digital converter, 1μS transit time (up to 10 input channels)
  - Conversion range: 0~VDD
  - Support the configuration of sampling time and resolution
  - On-chip voltage sensor
- Up to 18 fast I/O ports:
  - All I/O ports can be mapped to 16 external interrupts
  - All ports can input and output 5V signals
- Debug mode
  - Serial wire debug (SWD)
- Up to 6 timers
  - One 16-bit 4-channel advanced control timer providing 4-channel PWM output, with dead zone generation and emergency stop functions
  - One 16-bit timer providing up to 3 input captures/output comparisons, which can be used for IR control decoding
  - One 16-bit timer providing 1 input capture/output comparison
  - Two watchdog timers (independent type and window type)
  - One system time timer: 24-bit autodecrement counter
- Up to 4 communication interfaces
  - Two UART interfaces
  - One I2C interface
  - One SPI interface
- 96-bit unique ID (UID) of the chip
- Adopt QFN20 and TSSOP20 packages

For more information about the product, please refer to subsec 2.2 of this Datasheet.
For relevant information about Cortex®-M0, please refer to the *Cortex®-M0 Technical Reference Manual.*

2 Specification

Specification

2.1 Device Comparison

Table 1. Functions and Periphery Configurations

Peripheral port \ Model		MM32F0010A1N	MM32F0010A1T
Flash memory-K byte		16	16
SRAM-K byte		2	2
Timer	Universal (16-bit)	1	1
	Basic	1	1
	Advanced	1	1
Communication interface	UART	2	2
	I2C	1	1
	SPI	1	1
Number of GPIO pins		18	18
12-bit ADC	Number	1	1
	No. of channels	8	8
CPU frequency		48 MHz	
Operating voltage		2.0V~5.5v	
Package		QFN20	TSSOP20

2.2 Introduction

2.2.1 ARM Cortex-M0 as the Kernel with Embedded Flash Memory and SRAM

Cortex®-M0 processor is the latest embedded ARM processor. It provides a low-cost platform, reduced pins, decreased system power consumption, superior computing performance and advanced interrupt servicing system to realize the requirements of MCU.

The ARM® Cortex®-M0 is a 32-bit RISC processor that improves the code efficiency and makes full use of the high-performance ARM kernel in the storage space of common 8- and 16-bit systems.

This product has a built-in ARM core, so it is compatible with all ARM tools and software.

2.2.2 Embedded Flash Memory

Embedded flash memory up to 16K bytes for storing programs and data.

2.2.3 Embedded SRAM

Embedded SRAM up to 2K bytes.

2.2.4 CRC (Cyclical Redundancy Check) Computing Unit

The CRC (Cyclic Redundancy check) computing unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. The CRC-based technique is used to verify the consistency of data transfer or storage in its numerous applications.

Within the scope of the EN/IEC60335-1 standard, it provides a method of detecting flash memory errors. CRC computing unit can be used to calculate the software signature in real time and compare it to the signature generated when linking to and generating the software.

2.2.5 Nested Vectored Interrupt Controller (NVIC)

This product has a built-in nested vectored interrupt controller, which can process multiple maskable interrupting channels (excluding 16 Cortex™-M0 interrupt lines) and 16 programmable priorities.

- Tightly coupled NVIC enables low latency interrupt response
- Interrupt vector entry addresses directly enters into the kernel
- Tightly coupled NVIC interfaces
- Allow early processing of interrupts
- Handle higher-priority interrupts that arrive late
- Support tail link of interrupts
- Automatically save the processor state
- Offer automatic recovery when the interrupt returns with no additional instruction

This module provides flexible interrupt management with minimal interrupt latency.

2.2.6 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains multiple edge detectors which are used to generate interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge or falling edge or double edge) and can be screened separately. A pending register maintains the states of all interrupt requests. EXTI can detect clock cycles whose pulse width is smaller than the internal APB1. All universal I/O ports are connected to 16 external interrupt lines.

2.2.7 Clock and Startup

Multiple prescalers are used to configure AHB frequency and high-speed APB areas. The highest frequency of AHB and high-speed APB is 48MHz. Please refer to the clock drive diagram in figure 2.

2.2.8 Boot Mode

During startup, one of three boot modes can be selected through the boot pin:

- Boot from the flash memory
- Boot from the system memory
- Boot from the internal SRAM

Boot loader resides in the system memory. The flash memory can be reprogrammed through UART1.

2.2.9 Power Supply Scheme

- V_{DD} = 2.0V ~ 5.5V: the V_{DD} pin supplies power to the I/O pins and the internal voltage regulator.

2.2.10 Power Supply Monitor

This product is integrated with power on reset (POR)/power down reset (PDR) circuit. The circuit remains in the working state to ensure the system works when the power supply exceeds 2.0V. When VDD is below the set threshold ($V_{POR/PDR}$), the device will be placed in the reset state. An external reset circuit is not necessary.

Additionally, there is a programmable voltage monitor (PVD) in the device that monitors the V_{DD} power supply and compares it to the threshold V_{PVD}4. When V_{DD} is below or above the threshold V_{PVD}, the device will be interrupted. The interrupt handler will send a warning message or switch the microcontroller to safe mode. The PVD function should be enabled by a program.

2.2.11 Voltage Regulator

The voltage regulator converts the external voltage into the internal digital logic operating voltage. The voltage regulator remains in the working state after reset.

2.2.12 Low Power Mode

The product supports a low power mode that provides the best balance among low power requirements, short startup time, and multiple wake-up events.

Sleep Mode

In the sleep mode, only the CPU stops working. All peripherals are working and can wake

up the CPU in the event of an interrupt/event.

Shutdown Mode

The shutdown mode minimizes the power consumption while keeping the SRAM and register contents intact. In the shutdown mode, the HSI oscillator and HSE crystal oscillator are shut down. The microcontroller can be woken from the shutdown mode by any signal configured as EXTI. The EXTI signal can be a wake-up signal from one of the 16 external I/O ports and the output of the PVD.

Standby Mode

The standby mode can minimize the power consumption of the system. In the standby mode, the voltage regulator turns off when the CPU is in the deep sleep mode. All internal power supply areas in the 1.5V section are disconnected. HSI, and HSE oscillators are also turned off. They can be woken by the rising edge of WKUP pin, external reset of NRST pin, and IWDG reset. They also can be woken and reset by the watchdog timer. The contents of SRAM and registers will be lost.

2.2.13 Timer and Watchdog

The product includes one advanced timer, one universal timer, one basic timer, two watchdog timers and one system tick timer.

The following table compares the functions of advanced control timer, universal timer and basic timer:

大表

Table 2. Timer Function Comparison

Timer type	Name	Counter Resolution	Counter Type	Prescaler Coefficient	DMA Request Generation	Capture/ Comparison Channel	Comple -mentary Output
Advanced	TIM1	16-bit	Up, down, up/down	Any integer between 1~65536	None	4	Yes
Universal	TIM3	16-bit	Up, down, up/down	Any integer between 1~65536	None	3	None
Basic	TIM14	16-bit	Up	Any integer between 1~65536	None	1	None

Advanced Control Timer (TIM1)

Advanced control timer is composed of one 16-bit counter, 4 capture/comparison channels and three-phase complementary PWM generator. It has complementary PWM output with dead zone insertion and can be used as a complete universal timer. Four separate channels can be used for the followings:

- Input capture
- Output comparison
- PWM generation (edge or center alignment mode)
- Single pulse output

When it is configured as a 16-bit universal timer, it has the same function as a TIMx timer. When it is configured as a 16-bit PWM generator, it has full modulation capability (0~100%).

In the debug mode, the counter can be frozen while the PWM output is disabled. Therefore, switches controlled by these outputs are cut off.

Many of its features are the same as the universal TIM timer. Their internal structures are identical. Therefore, the advanced control timer can be used in conjunction with the TIM timer to support synchronization or event linking.

Universal Timer (TIMx)

One synchronously running universal timer (TIM3) is built into the product. The universal timer has one 32-bit automatic up-down counter, one 16-bit prescaler and four separate channels. Each channel can be used for input capture, output comparison, PWM and single pulse output.

Universal Timer_16-bit

The universal timer has one 16-bit automatic up-down counter, one 16-bit prescaler and four separate channels. Each channel can be used for input capture, output comparison, PWM and single pulse output.

They can also be used in conjunction with the advanced control timer to support synchronization or event linking. Counters can be frozen in the debug mode. Any universal timer can be used to produce PWM output.

These timers can also handle signals from incremental encoders and digital outputs from 1~4 Hall sensors. Each timer can produce PWM output, or be seen as a simple time reference.

Basic Timer

TIM14

The timer contains one 16-bit automatically reloadable count-up counter and one 16-bit prescaler. It has a single channel for input capture/output comparison, PWM or single

pulse output. Its counter can be frozen in the debug mode.

Independent Watchdog

The independent watchdog contains one 12-bit count-down counter and one 8-bit prescaler. There is an internal independent 40KHz clock oscillator. This oscillator is independent of the master clock, so it can work in the shutdown and standby modes. It can be used to reset the entire system in the event of system failure or used as a free timer to provide timeout management for applications. The options can be configured to boot watchdog via software or hardware. In the debug mode, the watchdog is off.

Window Watchdog

The window watchdog has one 7-bit count-down counter and can be set to run freely. It can be used as a watchdog to reset the entire system in the event of a problem. It is driven by the master clock, providing the early warning of an interrupt. In the debug mode, the watchdog is off.

System Time Base Timer

This timer is dedicated to the real-time operating system and can also be used as a standard count-down counter. It has the following characteristics:

- a 24-bit count-down counter
- automatic reloading
- a maskable system interrupt can be produced when the counter is 0
- programmable clock source

2.2.14 Universal Asynchronous Receiver and Transmitter (UART)

The UART interface supports LIN master-slave function and it is compatible with ISO7816 smart card mode. The supported length of output data from UART interface can be 5, 6, 7, 8 and 9 bits, which are configurable.

2.2.15 I2C Bus

I2C bus interface can operate in the multi-master mode or slave mode and it supports the standard and fast mode.

The I2C interface supports 7-bit or 10-bit addressing.

2.2.16 Serial Peripheral Interface (SPI)

The SPI interface can be configured as 1-32 bits per frame in the slave or master mode.

2.2.17 General Purpose Input/Output Interface (GPIO)

Each GPIO pin can be set as an output (push-pull or open-drain), an input (with or without pull-up/pull-down), or a multiplexed port of peripherals via software. Most GPIO pins are

shared with digital or analog multiplexed peripherals. All GPIO pins allow large passing current.

If required, the peripheral function of the I/O pins can be locked with a specific operation to avoid accidental writing into the I/O register.

2.2.18 ADC (Analog-to-Digital Converter)

The product is embedded with a 12-bit analog-to-digital converter (ADC), with up to 8 external channels available for single, one-cycle and continuous scan conversion. In the scan mode, the acquisition value conversion is automatically performed on a selected set of analog inputs.

The analog watchdog function allows to monitor one or all selected channels precisely. An interrupt will occur when the monitored signal exceeds a preset threshold.

Events generated by a general timer (TIMx) and an advanced control timer can be cascaded internally to the trigger of the ADC respectively. The application can convert the ADC to synchronize with the clock.

2.2.19 Serial Wire Debug Port (SW-DP)

Two-wire serial debug port (SW-DP) is embedded in ARM.

The ARM SW-DP allows to be connected to single-chip microcomputer through serial wire debugging tools.

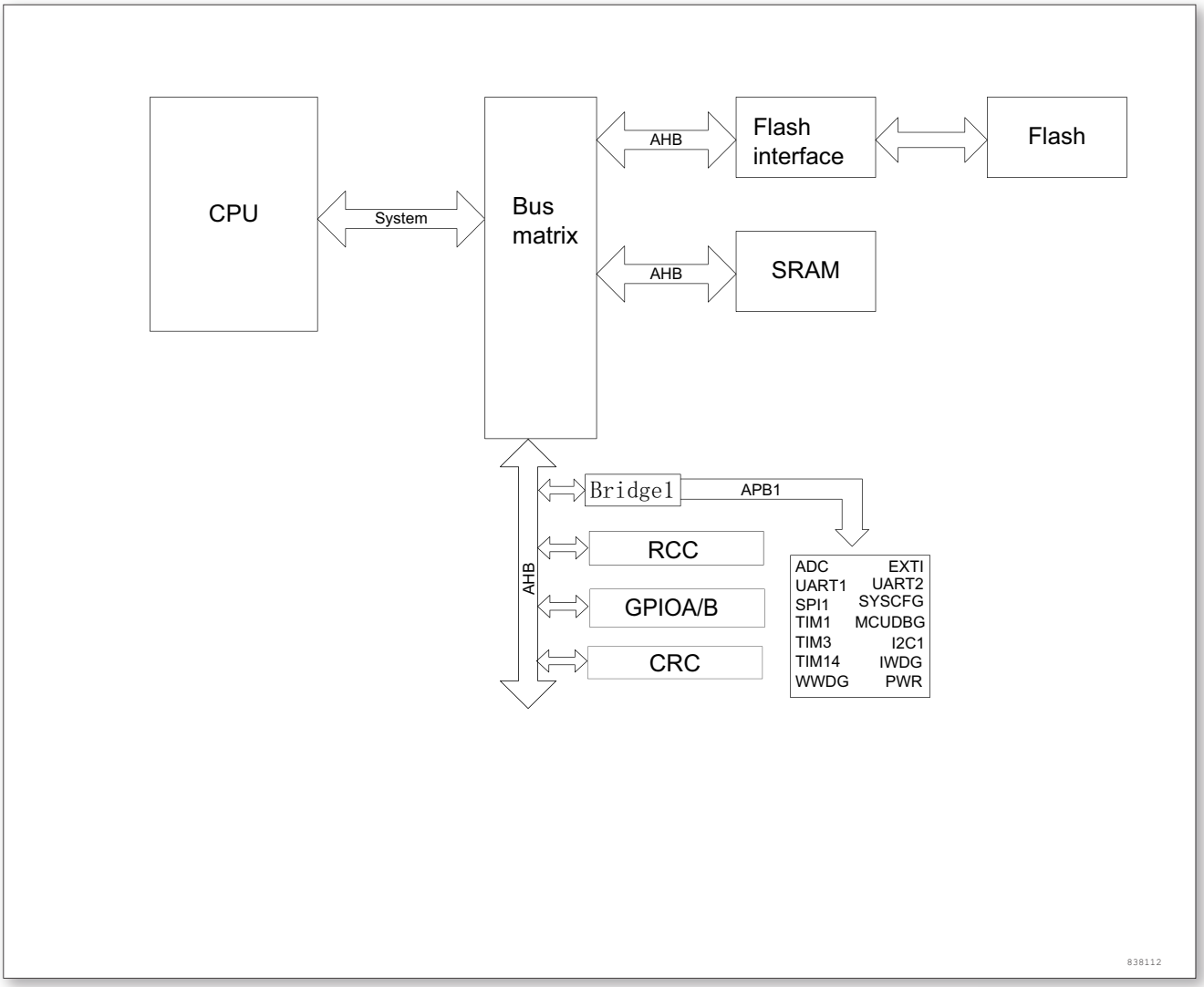

Figure 1. Block Diagram

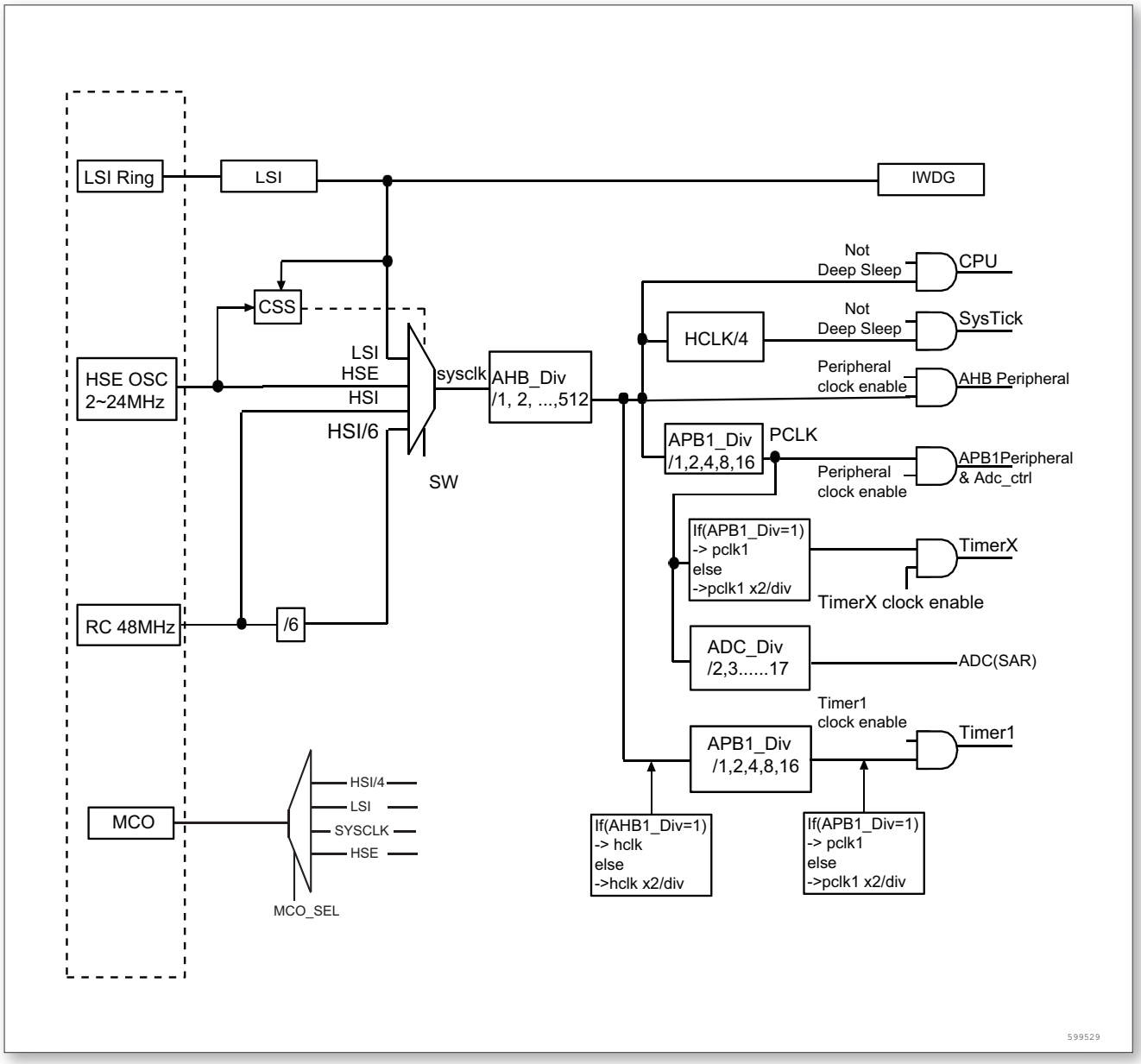

Figure 2. Clock structure

3 Pin definition

Pin definition

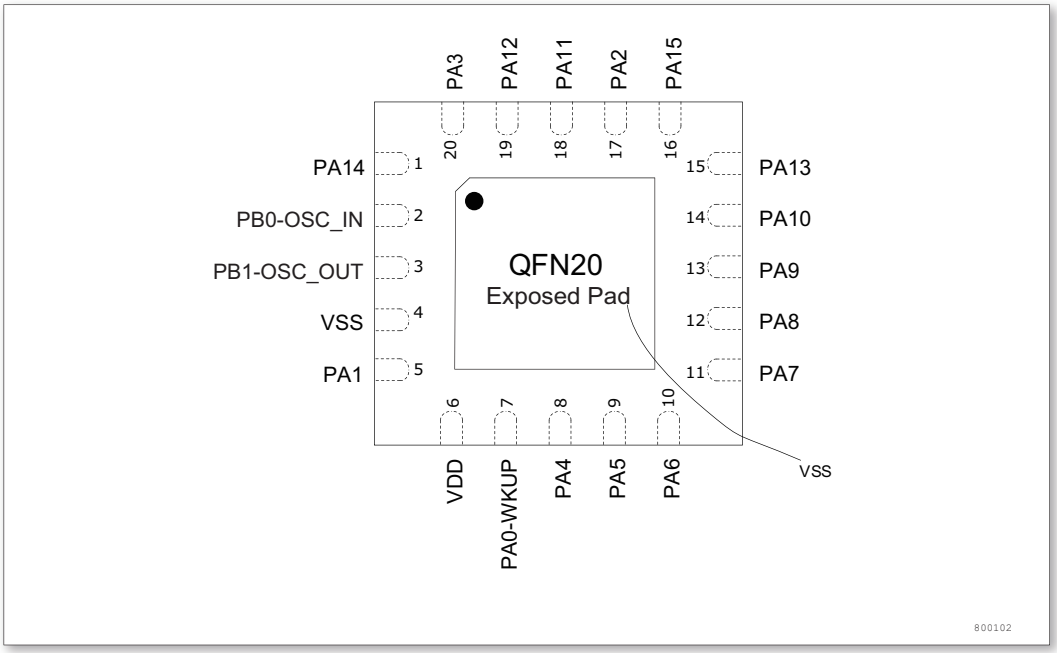

Figure 3. QFN20 Pinout

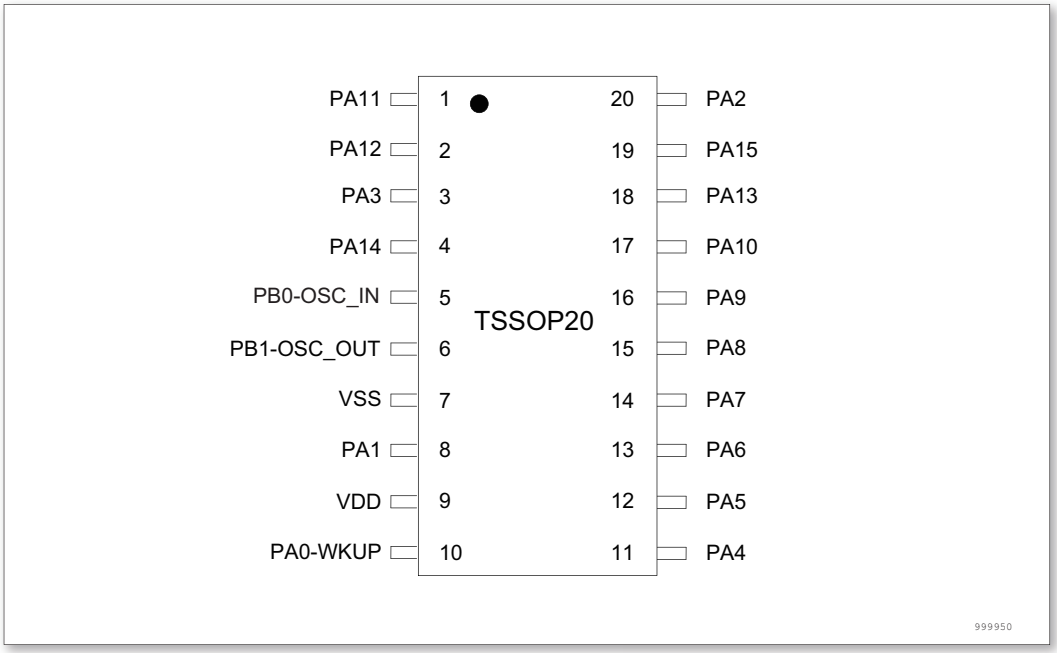

Figure 4. TSSOP20 pinout

Table 3. Pin definition

Pin Code		Pin name	Type(1)	I/O Level(2)	Main Function	Optional Multiplex Function	Additional Function
QFN20	TSSOP20						
1	4	PA14	I/O	TC	PA14	SWDCLK/ UART1_TX	-
2	5	PB0 OSC_IN	I/O	TC	PB0	-	ADC1_VIN[1]
3	6	PB1 OSC_IN	I/O	TC	PB1	-	ADC1_VIN[0]
4	7	VSS	S	-	VSS	-	-
5	8	PA1	I/O	TC	PA1	UART2_TX/ I2C1_SDA	-
6	9	VDD	S	-	VDD	-	-
7	10	PA0	I/O	TC	PA0	SPI1_NSS/ UART1_RX/ TIM1_CH3N/ I2C_SCL/ TIM3_CH3	-
8	11	PA4	I/O	TC	PA4	I2C1_SDA/ TIM1_BKIN	-
9	12	PA5	I/O	TC	PA5	SPI1_SCK/ I2C1_SCL	-
10	13	PA6	I/O	TC	PA6	SPI1_MOSI/ TIM1_CH1/ TIM1_CH1N/ TIM1_CH3	WKUP
11	14	PA7	I/O	TC	PA7	SPI1_MISO/ TIM1_CH1N/ TIM1_CH2N/ TIM1_CH4	ADC1_VIN[7]
12	15	PA8	I/O	TC	PA8	SPI1_SCK/ TIM1_CH2/ TIM3_CH1	-
13	16	PA9	I/O	TC	PA9	SPI1_MOSI/ TIM1_CH2N/ TIM1_CH1/ TIM14_CH1	-
14	17	PA10	I/O	TC	PA10	SPI1_MISO/ TIM1_CH3/ TIM1_CH2	-

Pin Code		Pin name	Type(1)	I/O Level(2)	Main Function	Optional Multiplex Function	Additional Function
QFN20	TSSOP20						
15	18	PA13	I/O	TC	PA13	SWDIO/ UART1_RX/ UART2_RX/ I2C1_SCL	-
16	19	PA15	I/O	TC	PA15	SPI1_NSS/ TIM1_CH3N/ TIM3_CH3	ADC1_VIN[6]
17	20	PA2	I/O	TC	PA2	TIM1_CH2N/ TIM3_CH2	ADC1_VIN[5]
18	1	PA11	I/O	TC	PA11	TIM1_CH2/ TIM14_CH1/ TIM3_CH1	ADC1_VIN[4]
19	2	PA12	I/O	TC	PA12	UART1_TX	ADC1_VIN[3]
20	3	PA3	I/O	TC	PA3	UART1_RX	ADC1_VIN[2]

1. I = Input, O = Output，S = Power Supply, HiZ = High Resistance
2. TC: Standard IO, input signal does not exceed VDD voltage

Table 4. PA Port Function Multiplex AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	SPI1_NSS	UART1_RX	TIM1_CH3N	I2C1_SCL	TIM3_CH3	-	-	-
PA1	-	-	UART2_TX	I2C1_SDA	-	-	-	-
PA2	-	-	TIM1_CH2N	-	TIM3_CH2	-	-	-
PA3	-	UART1_RX	-	-	-	-	-	-
PA4	-	-	TIM1_BKIN	I2C1_SDA	-	-	-	-
PA5	SPI1_SCK	-	-	I2C1_SCL	-	-	-	-
PA6	SPI1_MOSI	TIM1_CH1	TIM1_CH1N	-	TIM1_CH3	-	-	-
PA7	SPI1_MISO	TIM1_CH1N	TIM1_CH2N	MCO	TIM1_CH4	-	-	-
PA8	SPI1_SCK	TIM1_CH2	-	-	TIM3_CH1	-	-	-
PA9	SPI1_MOSI	TIM1_CH2N	TIM1_CH1	TIM14_CH1	-	-	-	-
PA10	SPI1_MISO	TIM1_CH3	TIM1_CH2	-	-	-	-	-
PA11	-	-	TIM1_CH2	TIM14_CH1	TIM3_CH1	-	-	-
PA12	-	UART1_TX	-	-	-	-	-	-
PA13	SWDIO	UART1_RX	UART2_RX	I2C1_SCL	-	-	-	-
PA14	SWDCLK	UART1_TX	-	-	-	-	-	-
PA15	SPI1_NSS	TIM1_CH3N	-	-	TIM3_CH3	-	-	-

Table 5. PB Port Function Multiplex AF0-AF7

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	-	-	-	-	-	-	-
PB1	-	-	-	-	-	-	-	-

4 Memory Image

Memory Image

Table 6. Memory Image

Bus	Addressing Range	Size	Peripheral	Remark
Flash	0x0000 0000-0x0000 3FFF	16 KB	Main flash memory, system memory or SRAM depends on BOOT configuration	
	0x0000 4000-0x07FF FFFF	~127 MB	Reserved	
	0x0800 0000-0x0800 3FFF	16 KB	Main Flash memory	
	0x0800 0000-0x1FFD FFFF	~383 MB	Reserved	
	0x1FFE 0000-0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200-0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000-0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00-0x1FFF F3FF	~256 MB	Reserved	
	0x1FFF F400-0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800-0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810-0x1FFF FFFF	~2 KB	Reserved	
SRAM	0x2000 0000-0x2000 07FF	2 KB	SRAM	
	0x2000 0700-0x2FFF FFFF	~255 MB	Reserved	
APB1	0x4000 0000-0x4000 03FF	1 KB	Reserved	
	0x4000 0400-0x4000 07FF	1 KB	TIM3	
	0x4000 0800-0x4000 0BFF	8 KB	Reserved	
	0x4000 2800-0x4000 2BFF	1 KB	Reserved	
	0x4000 2C00-0x4000 2FFF	1 KB	WWDG	
	0x4000 3000-0x4000 33FF	1 KB	IWDG	
	0x4000 3400-0x4000 37FF	1 KB	Reserved	
	0x4000 3800-0x4000 3BFF	1 KB	Reserved	
	0x4000 4000-0x4000 43FF	1 KB	Reserved	
	0x4000 4400-0x4000 47FF	1 KB	UART2	
	0x4000 4800-0x4000 4BFF	3 KB	Reserved	
	0x4000 5400-0x4000 57FF	1 KB	I2C1	
	0x4000 5800-0x4000 6BFF	5 KB	Reserved	
	0x4000 6C00-0x4000 6FFF	1 KB	Reserved	
	0x4000 7000-0x4000 73FF	1 KB	PWR	
	0x4000 7400-0x4000 FFFF	35 KB	Reserved	
	0x4001 0000-0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400-0x4001 07FF	1 KB	EXTI	
	0x4001 0800-0x4001 23FF	7 KB	Reserved	

Bus	Addressing Range	Size	Peripheral	Remark
APB1	0x4001 2400-0x4001 27FF	1 KB	ADC1	
	0x4001 2800-0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00-0x4001 2FFF	1 KB	TIM1	
	0x4001 3000-0x4001 33FF	1 KB	SPI1	
	0x4001 3400-0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800-0x4001 3BFF	1 KB	UART1	
	0x4001 3C00-0x4001 3FFF	1 KB	Reserved	
	0x4001 4000-0x4001 43FF	1 KB	Reserved	
	0x4001 4400-0x4001 47FF	1 KB	Reserved	
	0x4001 4800-0x4001 4BFF	1 KB	Reserved	
	0x4001 4C00-0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000-0x4002 03FF	1 KB	Reserved	
	0x4002 0400-0x4002 0FFF	3 KB	Reserved	
	0x4002 1000-0x4002 13FF	1 KB	RCC	
	0x4002 1400-0x4002 1FFF	3 KB	Reserved	
	0x4002 2000-0x4002 23FF	1 KB	Flash Interface	
	0x4002 2400-0x4002 2FFF	3 KB	Reserved	
	0x4002 3000-0x4002 33FF	1 KB	CRC	
	0x4002 3400-0x47FF FFFF	~127 MB	Reserved	
	0x4800 0000-0x4800 03FF	1 KB	GPIOA	
	0x4800 0400-0x4800 07FF	1 KB	GPIOB	
	0x4800 0800-0x4800 0BFF	1 KB	Reserved	
	0x4800 0C00-0x4800 0FFF	1 KB	Reserved	
	0x4800 1000-0x5FFF FFFF	384 MB	Reserved	

5 Electrical Characteristics

Electrical Characteristics

5.1 Test condition

Unless otherwise specified, VSS is seen as the benchmark of all voltages.

5.1.1 Typical Value

Unless otherwise specified, typical data are based on TA = 25°Cand VDD = 3.3V. These data are only used for design guidance and have not been tested.

5.1.2 Typical Curve

Unless otherwise specified, the typical curve is only used for design guidance and has not been tested.

5.1.3 Load Capacitance

The load condition during the measurement of pin parameters is shown in the figure below.

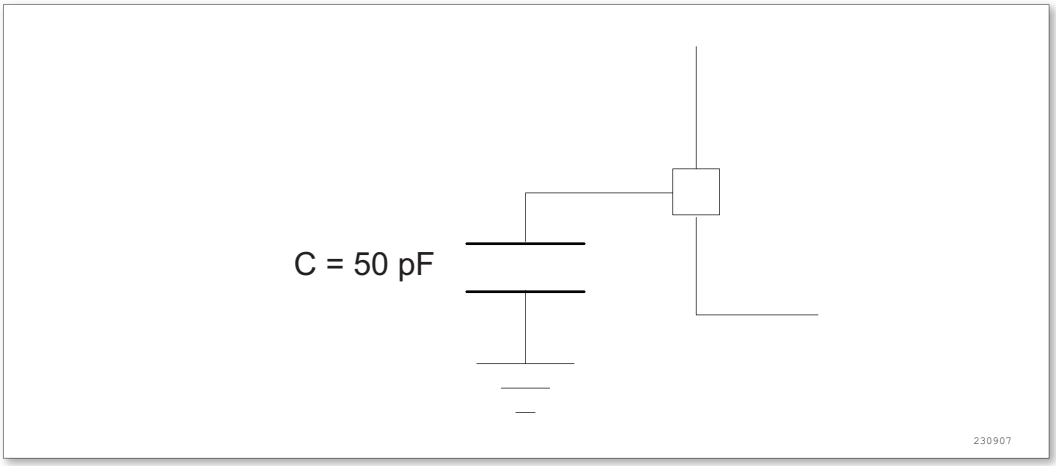

Figure 5. Pin load condition

5.1.4 Input Voltage on Pin

The measurement of input voltage on pin is shown in the figure below.

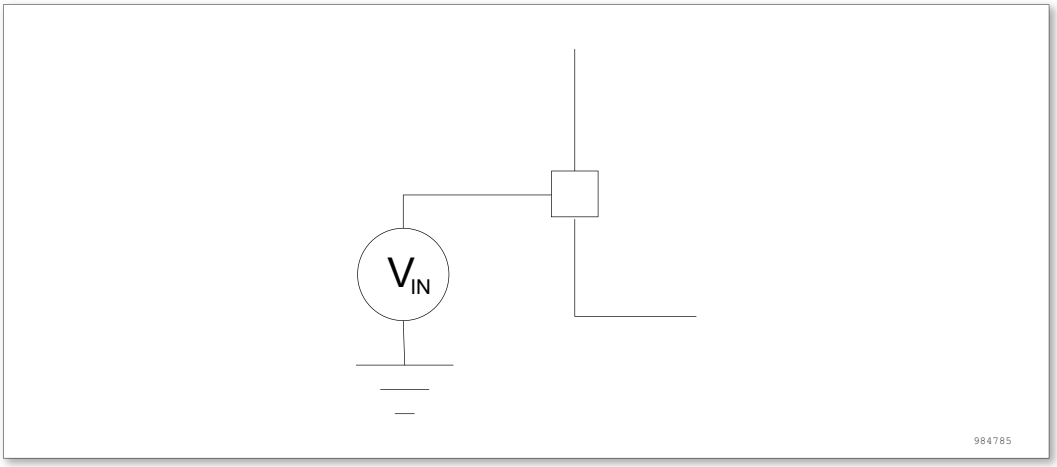

Figure 6. Pin input voltage

5.1.5 Power Supply Scheme

The power supply designing plan is shown in the figure below.

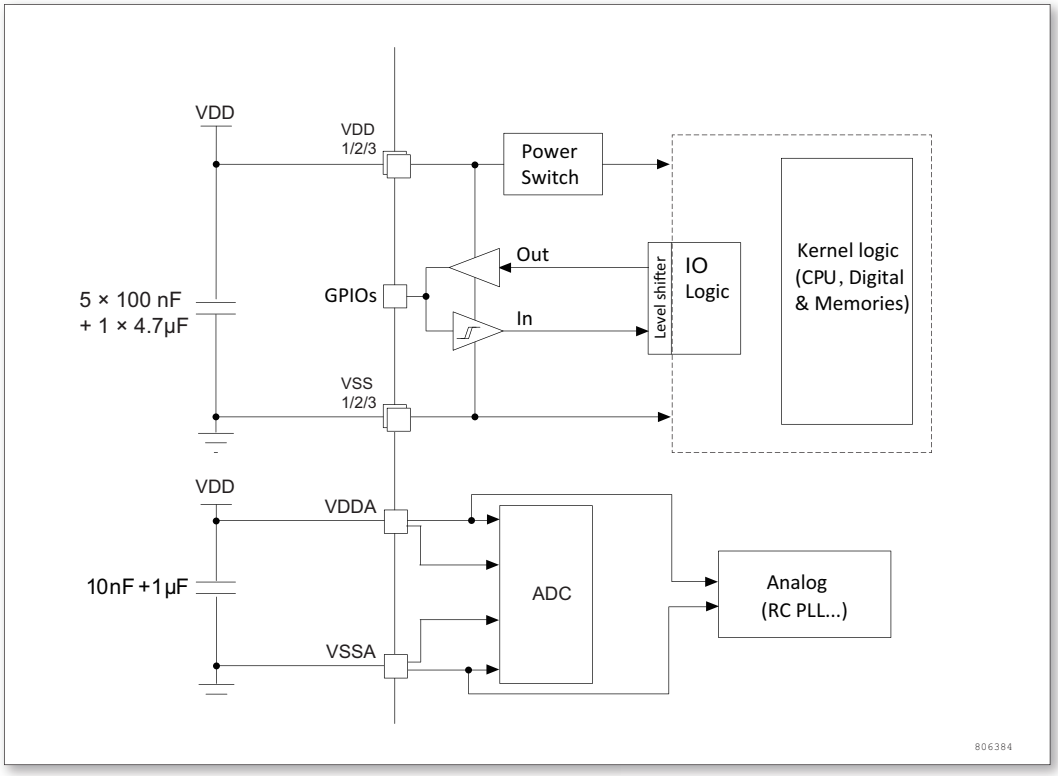

Figure 7. Power Supply Scheme

5.1.6 Measurement of Current Consumption

The measurement of current consumption on pin is shown in the figure below.

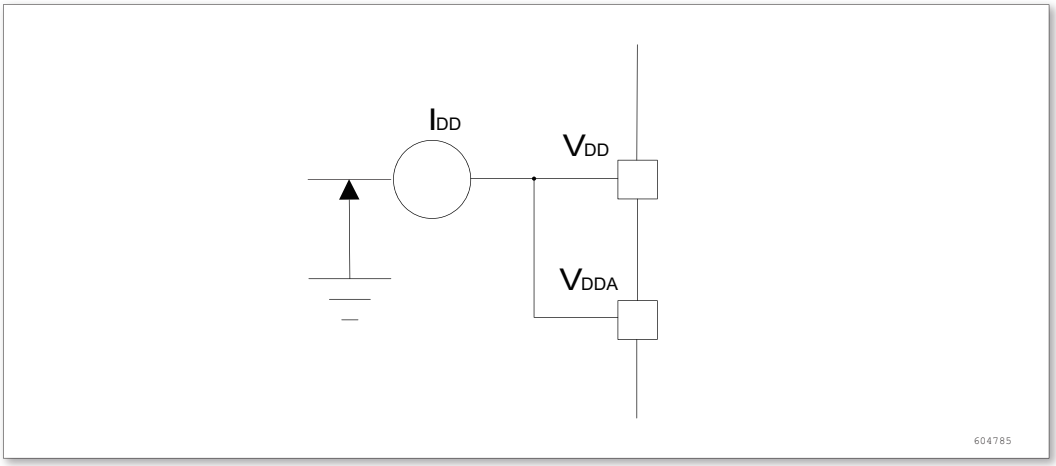

Figure 8. Current consumption measurement scheme

5.2 Absolute Maximum Rating

If the load applied to the device exceeds the value in the list of absolute maximum ratings (Table 7,Table 8,Table 9), the device may be damaged permanently. The list shows the maximum load that the device can bear. It does not mean that the functional operation of the device under these conditions is normal. The reliability of the device will be affected if the device works for a long time under the maximum condition.

Table 7. Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
V_{DD} - V_{SS}	External main supply voltage(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	V_{SS} - 0.3	V_{DD} + 0.3	

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply system within the permissible range.
2. The maximum value of VIN must always be observed. For information about the permitted maximum current values, please see the table below.

Table 8. Current Characteristics

Symbol	Description	Maximum value	Unit
I_{VDD}	Total current through VDD power cord (supply current)(1)	60	mA
I_{VSS}	Total current through VSS ground wire (outflow current)(1)	-60	
I_{IO}	Sink current through any I/O and control pins	25	
	Output current through any I/O and control pins	-25	
$I_{INJ(PIN)}$(2)(3)	Injection current through nRST pin	±5	
	Injection current through OSC_IN pin of HSE	±5	
	Injection current through other pins(4)	±5	
$\Sigma I_{INJ(PIN)}$(4)	Total injection current on all I/O and control pins(4)	±25	

1. All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply system within the permissible range.
2. $I_{INJ(PIN)}$ must not exceed its limit, that is to ensure the V_{IN} does not exceed its maximum. If you cannot guarantee that the V_{IN} does not exceed its maximum value, please make sure that the $I_{INJ(PIN)}$ does not exceed its maximum value under external constraint. When $V_{IN} > V_{DD}$, there is a forward injection current; When $V_{IN} < V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When injection currents go through several I/O ports at the same time, the maximum $\Sigma I_{INJ(PIN)}$ is the sum of absolute values of the forward and reverse injection currents in the real time. The result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on all the I/O ports.

Table 9. Temperature Characteristics

Symbol	Description	Maximum value	Unit
T_{STG}	Storage temperature range	- 45 ~ 150	°C
T_J	Maximum junction temperature		°C

5.3 Operating Condition

5.3.1 General Operating Condition

Table 10. General Operating Condition

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency		0	48MHz	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	48	
V_{DD}	Standard operating voltage		2.0	5.5	V
P_D	T_A=85°C(1)(3)	QFN20			°C
	T_A=105°C(1)(4)	TSSOP20			
T_A	T_A	Maximum power dissipation	-40	85	°C
		Low power dissipation (2)	-40	105	
T_J	Junction temperature range		-40	105	°C

1. If T_A is low, a higher P_D value is allowed as long as T_J does not exceed T_{Jmax} (see

subsec 5.1).

2. In the state of lower power dissipation, as long as T_J does not exceed T_{Jmax} (see subsec 5.1), T_A can be extended to this range

5.3.2 Operating Condition when Power is On and Power is Down

The parameters in the table below are tested under general operating conditions.

Table 11. Operating Condition when Power is On and Power is Down

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
t_{VDD}	V_{VDD}rise rise speed	T_A = 25°C	1	∞	μS/V
	V_{VDD}fall decline speed		500	∞	

5.3.3 Characteristics of Embedded Reset and Power-Control Models

The parameters in the table below are tested based on the ambient temperature and V_{DD} supply voltage listed in Table 10.

Table 12. Characteristics of Embedded Reset and Power-Control Models

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[3:0]=0000(rising edge)		1.8		V
		PLS[3:0]=0000(falling edge)		1.7		V
		PLS[3:0]=0001(rising edge)		2.1		V
		PLS[3:0]=0001(falling edge)		2.0		V
		PLS[3:0]=0010(rising edge)		2.4		V
		PLS[3:0]=0010(falling edge)		2.3		V
		PLS[3:0]=0011(rising edge)		2.7		V
		PLS[3:0]=0011(falling edge)		2.6		V
		PLS[3:0]=0100(rising edge)		3.0		V
		PLS[3:0]=0100(falling edge)		2.9		V
		PLS[3:0]=0101(rising edge)		3.3		V
		PLS[3:0]=0101(falling edge)		3.2		V
		PLS[3:0]=0110(rising edge)		3.6		V
		PLS[3:0]=0110(falling edge)		3.5		V
		PLS[3:0]=0111(rising edge)		3.9		V
		PLS[3:0]=0111(falling edge)		3.8		V
		PLS[3:0]=1000(rising edge)		4.2		V
		PLS[3:0]=1000(falling edge)		4.1		V
		PLS[3:0]=1001(rising edge)		4.5		V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{PVD}	Level selection of programmable voltage detector	PLS[3:0]=1001(falling edge)		4.4		V
		PLS[3:0]=1010(rising edge)		4.8		V
		PLS[3:0]=1010(falling edge)		4.7		V
$V_{POR/PDR}$	POR/PDR threshold	falling edge		1.65		V
		rising edge		1.65		V
$V_{PVDhyst}$	PVD hysteresis			100		mV
$T_{RSTTEMPO}$	Reset duration			2.5		ms

1. Product characteristics are guaranteed by design to be the minimum value $V_{POR/PDR}$.
2. Guaranteed by design, not tested in production.

Note: Reset duration is measured from the power-on moment to the moment the first instruction is read by the user's application code.

5.3.4 Supply current characteristics

Current consumption is an index of multiple parameters and factors, which include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, program location in memory and executed code, etc.

The current consumption readings in all operating modes given in this section execute a set of simple codes.

Maximum current consumption:

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 wait cycle at 0~24 MHz; 1 wait cycle at 24~48 MHz).
- The instruction prefetch function is enabled. When the peripheral is enabled: f_{PCLK1} = f_{HCLK}.

Note：The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 14. Typical and maximum current consumption in shutdown and standby mode (2)

Symbol	Parameter	Condition	Maximum value(1)	Unit
			T_A=25°C	
IDD	Supply current in shutdown mode	PWR->CR[0]=0	90.5	μA
		PWR->CR[0]=1	1.8	
	Supply current in standby mode	LSI, IWDG are off	0.3	

1. The maximum value is tested in case of the power supply voltage =3.3V and T_A = 25°C.
2. It comes from comprehensive evaluation, and is not tested in production. The IO status is analog input.

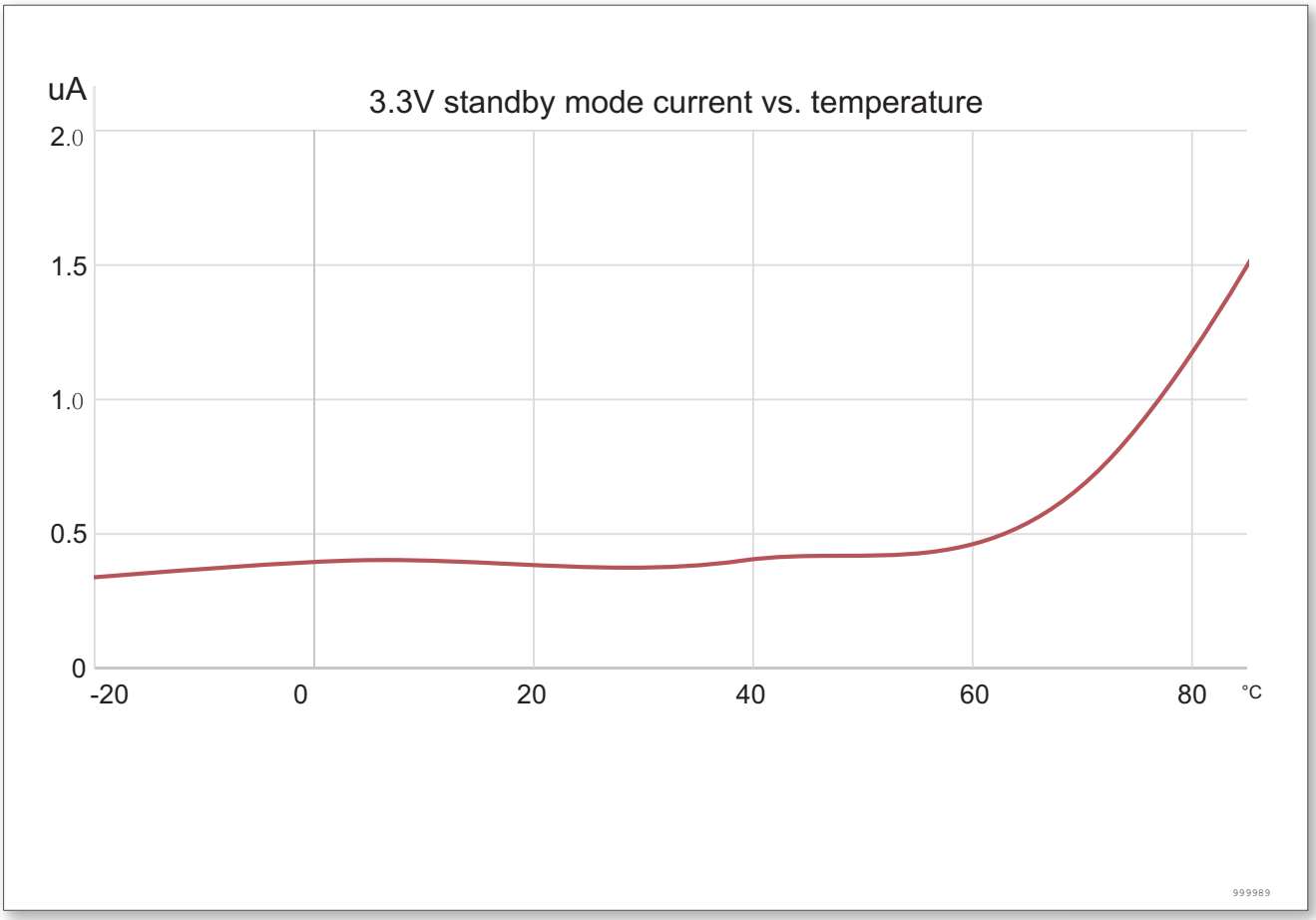

Figure 9. Typical current consumption vs. temperature at VDD = 3.3V in standby mode

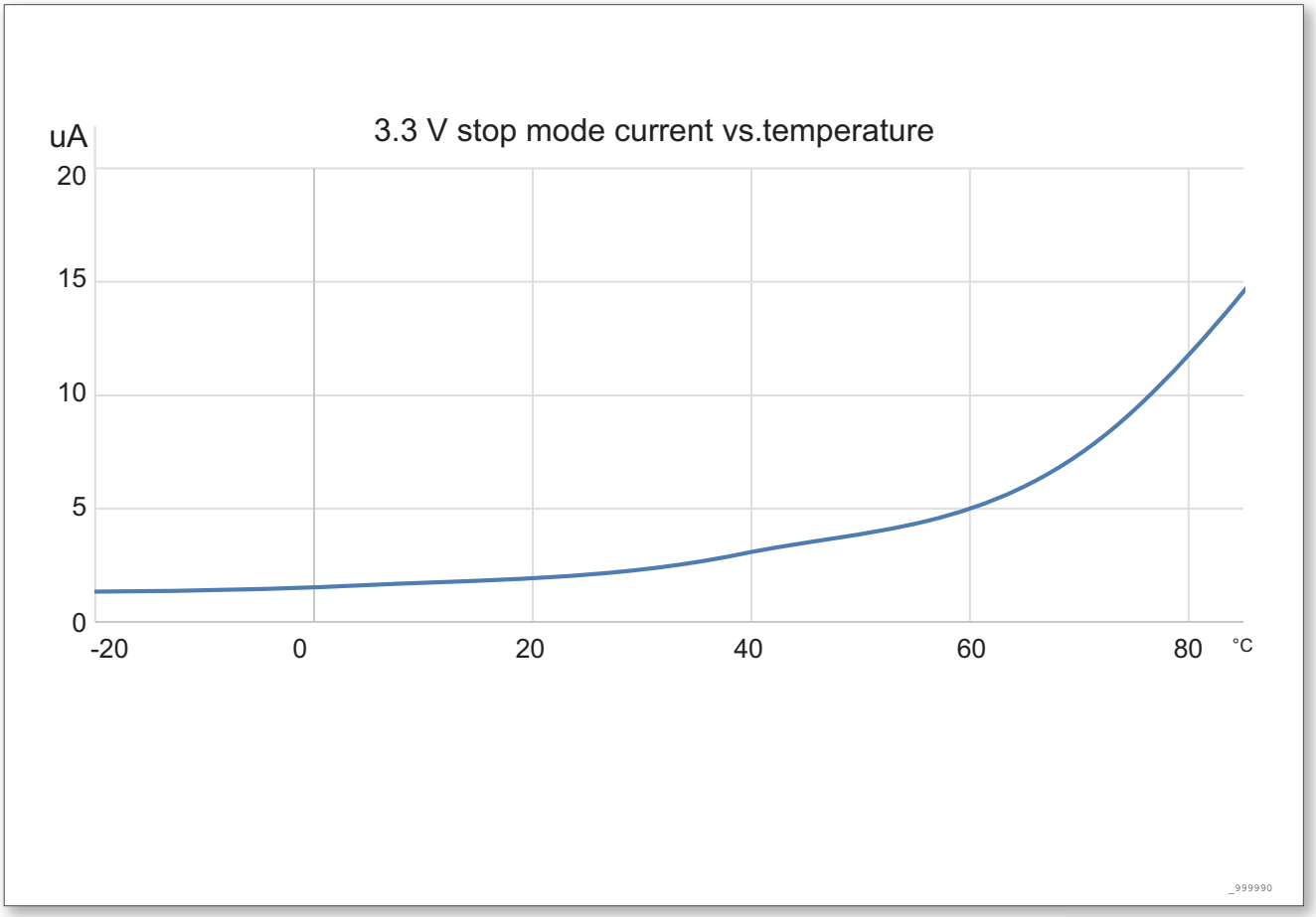

Figure 10. Typical current consumption vs. temperature at VDD = 3.3V in stop mode

Typical current consumption

The MCU is in the following conditions:

- All I/O pins are in input mode and connected to a static level—V_{DD} or V_{SS} (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the f_{HCLK} frequency (0 wait cycle at 0~24 MHz; 1 wait cycle at 24~48 MHz).
- Ambient temperature and VDD supply voltage conditions are listed in Table 10.
- The instruction prefetch function enabled. When the peripheral is enabled: $f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetch function must be set before setting the clock and bus frequency division.

Table 15. Maximum current consumption in operating mode, data processing code running from internal flash memory

Symbol	Parameter	Condition	f_{HCLK}[4]	Typcal value[1][2][3]		Unit
				Enable all peripherals[5]	Disable all peripherals	
I_{DD}	Supply current in operating mode	Internal clock	48MHz	6.84	3.99	mA
		Internal clock	24MHz	4.18	2.45	
		Internal clock	8MHz	1.83	1.35	
		Internal clock	4MHz[2]	1.29	1.01	
		Internal clock	2MHz[2]	0.98	0.84	
	Supply current in operating mode	Internal clock	1MHz[2]	0.82	0.76	
		Internal clock	500KHz[2]	0.75	0.71	
		Internal clock	125KHz[2]	0.69	0.68	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. It’s obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division.

Table 16. Typical current consumption under sleep mode at high and low temperature, data processing code runs from internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Peripheral clock fully open in case of typical value V_{DD}=3.3V			Peripheral clock fully close in case of typical value V_{DD}=3.3V			Unit
				-40°C	25°C	85°C	-40°C	25°C	85°C	
IDD	Supply current is in run mode, execute code from FLASH	HSI is used as the system clock, and HCLK is divided to the specified frequency	48MHz	6.64	6.79	6.94	3.86	3.96	4.07	mA
			24MHz	4.05	4.15	4.26	2.36	2.43	2.52	
			8MHz	1.69	1.79	1.86	1.23	1.33	1.38	
			4MHz	1.2	1.26	1.36	0.92	0.99	1.06	
			2MHz	0.91	0.96	1.03	0.77	0.82	0.89	
			1MHz	0.76	0.81	0.87	0.69	0.74	0.8	
			500KHz	0.69	0.73	0.79	0.66	0.7	0.75	
			125KHz	0.64	0.68	0.73	0.63	0.67	0.72	

Table 17. Maximum current consumption in sleep mode, the code runs in flash

Symbol	Parameter	Condition	f_{HCLK}[4]	Typcal value[1][2][3]		Unit
				Enable all peripherals[5]	Disable all peripherals	
I_{DD}	Supply current in sleep mode	Internal clock	48MHz	4.63	1.76	mA
		Internal clock	24MHz	2.97	1.23	
		Internal clock	8MHz	1.33	0.85	
		Internal clock	4MHz[2]	1.05	0.76	
		Internal clock	2MHz[2]	0.86	0.72	
		Internal clock	1MHz[2]	0.76	0.69	
		Internal clock	500KHz[2]	0.72	0.68	

Symbol	Parameter	Condition	f_{HCLK}[4]	Typcal value[1][2][3]		Unit
				Enable all peripherals[5]	Disable all peripherals	
I_{DD}	Supply current in sleep mode	Internal clock	125KHz[2]	0.68	0.67	mA

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. It’s obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division.

Table 18. Typical current consumption under sleep mode at high and low temperature, data processing code runs from internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Peripheral clock fully open in case of typical value V_{DD}=3.3V			Peripheral clock fully close in case of typical value V_{DD}=3.3V			Unit
				-40°C	25°C	85°C	-40°C	25°C	85°C	
IDD	Supply current is in run mode, execute code from FLASH	HSI is used as the system clock, and HCLK is divided to the specified frequency	48MHz	4.5	4.6	4.71	1.68	1.74	1.81	mA
			24MHz	2.87	2.95	3.03	1.16	1.22	1.27	
			8MHz	1.26	1.31	1.37	0.79	0.84	0.89	
			4MHz	0.99	1.04	1.09	0.7	0.75	0.8	
			2MHz	0.8	0.85	0.9	0.66	0.7	0.76	
			1MHz	0.71	0.75	0.8	0.64	0.68	0.73	
			500KHz	0.66	0.71	0.76	0.63	0.67	0.72	
			125KHz	0.63	0.67	0.72	0.62	0.66	0.71	

1. The typical value is tested at T_A = 25°Cand V_{DD} = 3.3V.
2. It’s obtained when the HCLK frequency is less than 8MHz, and the system clock is HSI frequency division

5.3.5 External clock source characteristics

High-speed external user clock from external oscillator source

The characteristic parameter given in the following table is measured by a high-speed external clock source, and the ambient temperature and supply voltage conform to the general operating condition.

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSE_ext}	User external clock frequency[1]			8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7VDD		VDD	V

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{HSEL}	OSC_IN input pin low level voltage		VSS		0.3VDD	V
$t_{w(HSE)}$	OSC_IN high or low time (1)		15			ns
$C_{in(HSE)}$	OSC_IN input capacitive reactance (1)			5		pF
$DuCy_{(HSE)}$	Duty cycle			50		%

1. Guaranteed by design, not tested in production.

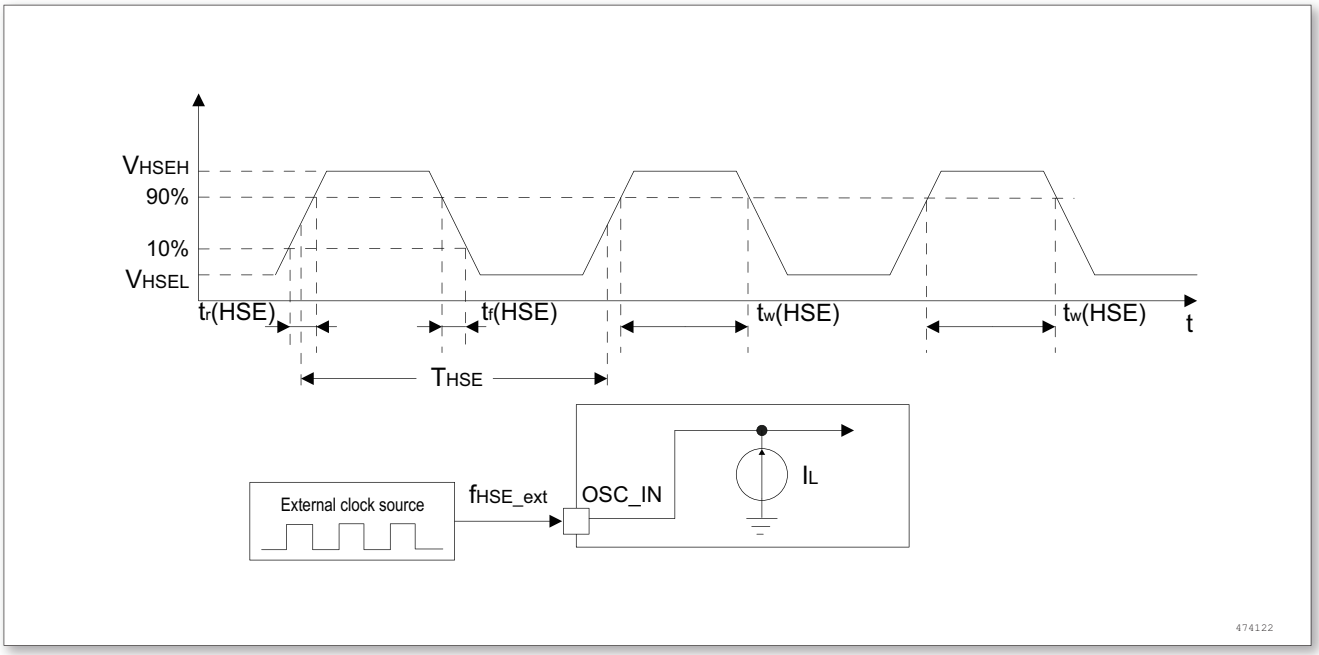

Figure 11. AC timing diagram of external high-speed clock source

High-speed external clock generated by a crystal/ceramic resonator

The high-speed external clock (HSE) may be generated by an oscillator composed of a 2~24MHz crystal/ceramic resonator. The information given in this section is drawn based on the results obtained through comprehensive characteristic evaluation with the typical external elements listed in the table below. In application, the resonator and load capacitor must be mostly close to the oscillator pin to reduce output distortion and stabilization time at startup. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 20. HSE 2~24MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{OSC_IN}	Oscillator frequency	2.0V<VDD<3.6V	2	8	12	MHz
		3.0V<VDD<5.5V	8	16	24	
R_F	Feedback resistance(4)			510		kΩ

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
ESR	Support crystal serial impedance(C_{L1} C_{L2}[3] 16pF)	f_{OSC_IN} = 24M V_{DD} = 3.0V			60	Ω
		f_{OSC_IN} = 12M V_{DD} = 2.0V			150	
I_2	HSE drive current	f_{OSC_IN} = 24M V_{DD} = 2.0V ESR=30Ω C_{L1} C_{L2}[3] 20pF		1.5		mA
g_m	Oscillator transconductance	Start up		9		mA/V
$t_{SU(HSE)}$[5]	Start time	V_{DD} stable		3		ms

1. The characteristic parameter of the resonator is given by the crystal/ceramic resonator manufacturer.
2. Drawn from comprehensive evaluation, not tested in production.
3. For C_{L1} and C_{L2}, it is recommended to use 5pF~25pF (typical value) high-quality ceramic capacitor designed for high-frequency applications, as well as crystal or resonator that meets the requirements. Usually, C_{L1} and C_{L2} have the same parameter. The crystal manufacturer usually gives the parameter of the load capacitance in the serial combination of C_{L1} and C_{L2}. When choosing C_{L1} and C_{L2}, the capacitive reactance of the PCB and MCU pins should be taken into account (the capacitance between the pins and the PCB board can be roughly estimated as 10pF).
4. The relatively low RF resistance value can provide protection and avoid problems when operating in a humid environment. The leakage and bias conditions generated in this environment have changed. However, if the MCU is used in harsh humid conditions, such parameters need to be taken into account in the design.
5. $t_{SU(HSE)}$ is the start-up time, which is the time duration with the measurement starting when the software enables HSE until a stable 8MHz oscillation is obtained. This value is drawn based on readings on a standard crystal resonator, and it may vary greatly depending on the crystal manufacturer.

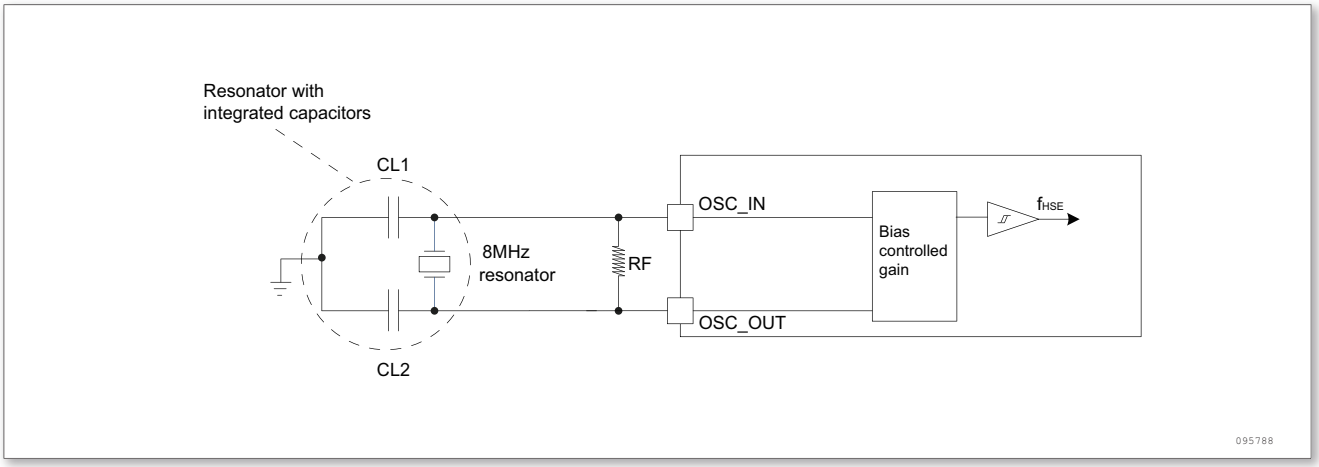

Figure 12. Typical application using 8MHz crystal

5.3.6 Internal clock source characteristics

The characteristic parameter given in the following table is measured when ambient temperature and power supply voltage meet with the general operating condition.

High-speed internal (HSI) oscillator

Table 21. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{HSI}	Frequency			48		MHz
ACC_{HSI}	HSI oscillator accuracy	T_A = 25	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time			12	16	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			328		μA

1. V_{DD} = 3.3V,unless otherwise specified.
2. Guaranteed by design, not tested in production.

LSI

Table 22. LSI (1)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f_{LSI}(2)	Frequency			40		KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				85	μs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			0.75	1.4	μA

1. V_{DD} = 3.3V, unless otherwise specified.
2. Drawn from comprehensive evaluation, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up time in low power mode

The wake-up time listed in the following table is measured during the wake-up phase of the Internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Shutdown or standby mode: the clock source is the oscillator
- Sleep mode: the clock source is the clock used when entering sleep mode

All times are measured when ambient temperature and supply voltage meet the general operating condition.

Table 23. Wake-up time in low power mode

Symbol	Parameter	Condition	Maximum value	Unit
$t_{WUSLEEP}$(1)	Wake up from sleep mode	HSI is the system clock	0.8	μs
t_{WUSTOP}(1)	Wake up from shutdown mode (Voltage regulator in operation)	HSI is the system clock	9.8	μs
t_{WUSTOP}(1)	Wake up from shutdown mode (Voltage regulator in low power mode)	HSI is the system clock	12.6	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x00	260	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x01	220	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x02	170	μs
$t_{WUSTDBY}$(1)	Wake up from standby mode	PWR->CR[15:14]=0x03	140	μs

1. The wake-up time measurement starts from the wake-up event to the user program reading the first instruction.

5.3.7 Memory characteristics

Flash memory

Table 24. Flash memory characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
t_{prog}	8-bit programming time		6		7.5	μs
t_{ERASE}	Page (512K bytes) erasing time		4		5	ms
t_{ME}	Full erasing time		20		40	ms
I_{DD}	Supply current	Reading mode, f_{HCLK} =40MHz			4.5	mA
		Writing mode			3.5	
		Erasing mode			2	
V_{prog}	Programming voltage			1.5		V

Table 25. Flash memory life and data retention period(1)(2)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
NEND	Life (erasing and writing times)			20		Thousand times
t_{RET}	Data retention period	T_A = 25°C	100			Year

1. Drawn from comprehensive evaluation, not tested in production.

5.3.8 EMC characteristics

Sensitivity testing is carried out by sampling during product comprehensive evaluation.

Design reliable software to avoid noise

EMC evaluation and optimization at the device level are carried out in a typical application environment. It should be noted that good EMC performance is closely related to user applications and specific software.

Therefore, it is recommended that users implement EMC optimization on the software and conduct EMC-related certification tests.

Software recommendations

The software flow must include the control of program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data destroyed (control registers, etc...)

Test before certification

Many common failures (unexpected reset and corrupted program counter) can be reproduced by manually introducing a low level on NRST or introducing a 1-second low level on the crystal oscillator pin.

During ESD test, a voltage exceeding the application requirement can be directly applied to the chip. When an unexpected action is detected, the software part needs to be strengthened to prevent unrecoverable errors.

5.3.9 Absolute maximum value (electrical sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to conduct a strength test on the chip to determine its electrical sensitivity performance.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse and then a negative pulse after one second interval) is applied to all the pins of all samples. The size of the sample is related to the number of power supply pins on the chip (3 pieces (n + 1) power supply pin). This test complies with the standard JEDEC JS-001-2017/JS-002-2018.

Static latching

In order to evaluate the latch performance, 2 complementary static latching tests need to be performed on 6 samples:

- Provide a supply voltage exceeding the limit for each power supply pin.
- Inject current into each input, output, and configurable I/O pin.

This test complies with the EIA/JESD78E integrated circuit latching standard.

Table 26. MCU ESD characteristics

Symbol	Parameter	Condition	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C, compliance with JEDEC JS-001-2017	±8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model)	T_A = 25°C, compliance with JEDEC JS-002-2018	±2000	
I_{LU}	Static latching (Latch-up current)	T_A = 25°C, compliance with JESD78E	100	mA

1. Drawn from comprehensive evaluation, not tested in production.

5.3.10 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameter listed in the table below is measured according to the condition in Table 7. All I/O ports are compatible with CMOS.

Table 27. I/O static characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	3.3V CMOS port	-0.3		0.8	V
		5.0V CMOS port	-0.3		0.3 x V_{DD}	
V_{IH}	Input high level voltage	3.3V CMOS port	2		5.5	V
		5.0V CMOS port	0.7 x V_{DD}		5.5	
V_{hy}	I/O pin Schmitt trigger voltage hysteresis(1)	3.3V	0.1 x V_{DD}			mV
		5.0V	0.1 x V_{DD}			
I_{lkg}	Input leakage current (2)	3.3V			1	μA
		5.0V			1	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
R_{PU}	Weak pull-up equivalent resistance (3)	3.3V $V_{IN}=V_{SS}$	22		50	kΩ
		5.0V $V_{IN}=V_{SS}$	22		50	
R_{PD}	Weak pull-down equivalent resistance (3)	3.3V $V_{IN}=V_{SS}$	20		100	kΩ
		5.0V $V_{IN}=V_{SS}$	20		100	
C_{IO}	I/O pin capacitance	3.3V			10	pF
		5.0V			10	

1. The hysteresis voltage of Schmitt trigger switching level. Drawn from comprehensive evaluation, not tested in production.
2. In case of reverse current in the adjacent pin, the leakage current may be higher than the maximum value.
3. The pull-up and pull-down resistors are MOS resistors.

Output drive current

GPIO (General Purpose Input /Output Port) can input or output up to ±20mA current.

In user applications, the number of I/O pins must ensure that the drive current cannot exceed the absolute maximum ratings given in subsec 5.2

- The sum of the current drawn by all I/O ports from V_{DD}, plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the current drawn by all I/O ports and output from V_{SS}, plus the maximum operating current output by the MCU on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage

Table 28. Output voltage characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OL} (1)	Output low level, when 8 pins input current at the same time	CMOS port,I_{IO} = +8mA 2.7V< V_{DD} < 3.6V	0.4		V
V_{OH} (2)	Output high level, when 8 pins output current at the same time	V_{DD} - 0.4			
V_{OL} (1)(3)	Output low level, when 8 pins input current at the same time	I_{IO} = +20mA 2.7V< V_{DD} < 3.6V		0.3 V_{DD}	
V_{OH} (2)(3)	Output high level, when 8 pins output current at the same time	I_{IO} = +20mA 2.7V< V_{DD} < 3.6V	0.7 V_{DD}		V
V_{OL} (2)(3)	Output low level, when 8 pins input current at the same time	I_{IO} = +6mA 2V< V_{DD} < 2.7V		0.4	

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V_{OH} (2)(3)	Output high level, when 8 pins output current at the same time	I_{IO} = +6mA 2V< V_{DD} < 2.7V	V_{DD} - 0.4		V

1. The current IIO input by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VSS}.
2. The current IIO output by the chip must always follow the absolute maximum ratings given in the table, and the sum of I_{IO} (all I/O pins and control pins) cannot exceed I_{VDD}.
3. Drawn from comprehensive evaluation, not tested in production.

Input and output AC characteristics

The definitions and values of the input and output AC characteristics are shown in figure 13 and Table 29, respectively. Unless otherwise specified, the parameter listed in Table 29 is measured by the ambient temperature and supply voltage in accordance with the condition in Table 7.

Table 29. Input and output AC characteristics(1)

MODEx[1:0] configuration	Symbol	Parameter	Condition	Typical value	Unit
11	$f_{maxr(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=3.3V	30	MHz
	$t_{f(IO)out}$	Output fall time	C_L=50pF, V_{DD}=3.3V	6.4	ns
	$t_{r(IO)out}$	Output rise time	C_L=50pF, V_{DD}=3.3V	8.7	ns
10	$f_{maxr(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=3.3V	50	MHz
	$t_{f(IO)out}$	Output fall time	C_L=50pF, V_{DD}=3.3V	4.8	ns
	$t_{r(IO)out}$	Output rise time	C_L=50pF, V_{DD}=3.3V	4.8	ns
01	$f_{maxr(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=3.3V	50	MHz
	$t_{f(IO)out}$	Output fall time	C_L=50pF, V_{DD}=3.3V	4.3	ns
	$t_{r(IO)out}$	Output rise time	C_L=50pF, V_{DD}=3.3V	4.7	ns

1. I/O port speed can be configured through MODEx[1:0]. Refer to the description of the GPIO port configuration register in the Chip Reference Manual.
2. Guaranteed by design, not tested in production

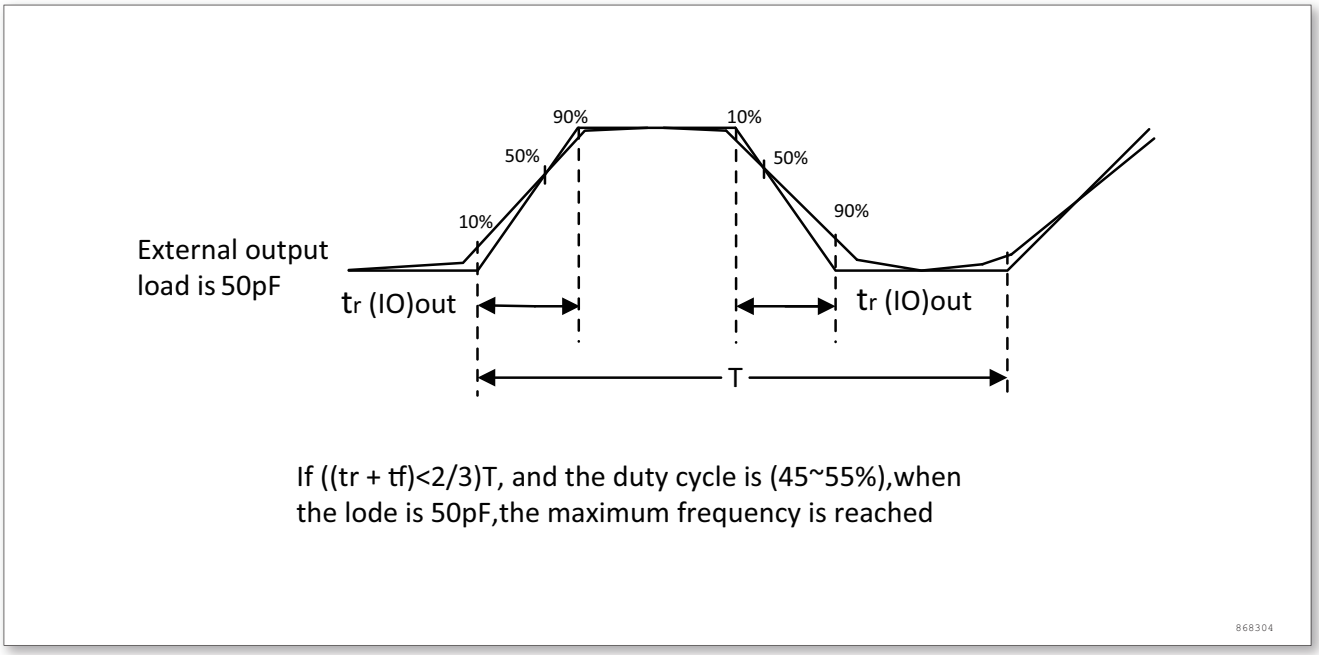

Figure 13. Definition of input and output AC characteristics

5.3.11 NRST pin characteristics

NRST pin input driver uses CMOS technology, and it is connected with a pull-up resistor, R_{PU}.

Table 30. NRST pin characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		-0.3		0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		2		5.5	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis		0.1 V_{DD}			V
R_{PU}	Weak pull-up equivalent resistance (2)	$V_{IN} = V_{SS}$	22		50	kΩ
$V_{F(NRST)}$ (1)	NRST input filter pulse		4.0			μs
$V_{NF(NRST)}$ (1)	NRST input unfiltered pulse				1.0	μs

1. Guaranteed by design, not tested in production
2. The pull-up resistor is a MOS resistor.

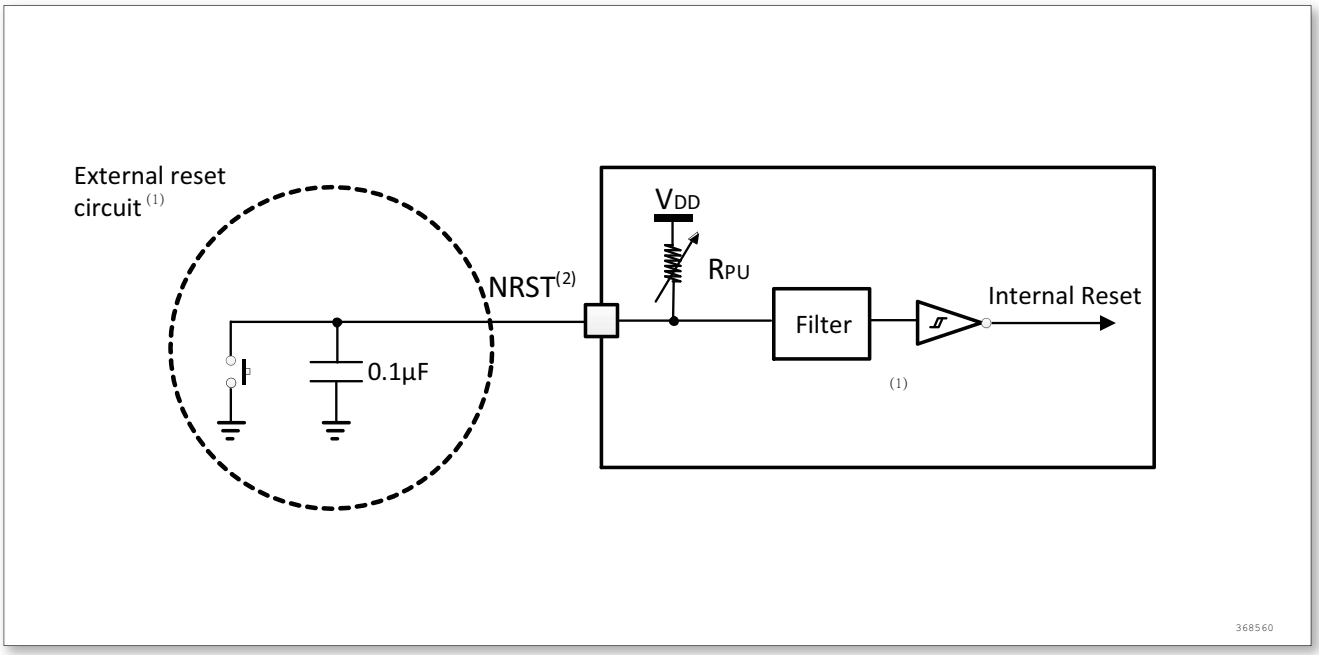

Figure 14. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset.
2. The user must ensure that the NRST pin voltage can be lower than the maximum $V_{IL(NRST)}$ listed in Table 30, otherwise the MCU cannot be reset.

5.3.12 Timer characteristics

The parameters listed in the following table are guaranteed by design.

For details on the characteristics of the input/output multiplex function pins (output comparison, input capture, external clock, PWM output), see subsubsec 5.3.10.

Table 31. TIMx(1) characteristics

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$ ns
		$f_{TIMxCLK}$=48MHz	20.8		
f_{EXT}	CH1 to CH4 timer external clock frequency		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$=48MHz	0	24	
R_{esTIM}	Timer resolution			16	Bit
$t_{COUNTER}$	When selecting the internal clock, the 16-bit counter clock cycle		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz	0.0208	1365	µS
$t_{MAXCOUNT}$	Maximum possible count			65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz		0.01365	S

1. TIMx is a generic name.

5.3.13 Communication Interface

I2C

Unless otherwise specified, the parameters listed in Table 32 are measured when the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage meet the condition of Table 10.

The I2C interface complies with the standard I2C communication protocol, but has the following limitations: SDA and SCL are not "true" pins. When it's configured as open-drain output, the PMOS tube between the pin and V_{DD} is turned off, but it still exists.

I2C interface characteristics are listed in Table 32. For details on the characteristics of input/output multiplex function pins (SDA and SCL), see subsubsec 5.3.10.

Table 32. I2C interface characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.2		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.5		μs
$t_{su(SDA)}$	SDA establishment time	$2*t_{PCLK}$		$2*t_{PCLK}$		ns
$t_{h(SDA)}$	SDA data retention time	0(3)		0(4)	875(3)	ns
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000		300	ns
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	ns
$t_{h(STA)}$	Start condition hold time	4.0		0.5		μs
$t_{su(STA)}$	Repeated start condition establishment time	4.7		0.5		μs
$t_{su(STO)}$	Stop condition establishment time	4.0		0.5		μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (Bus Free)	4.7		1.2		μs
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.
2. To reach the maximum frequency of standard mode I2C, ft_{PCLK1} must be greater than 3MHz. To reach the maximum frequency of fast mode I2C, ft_{PCLK1} must be greater than 12MHz.
3. If the low-level time of the SCL signal is not required to be lengthened, only the maximum hold time of the start condition needs to be met.
4. In order to cross the undefined area of the falling edge of SCL, a hold time of at least 300nS on the SDA signal must be guaranteed inside the MCU.

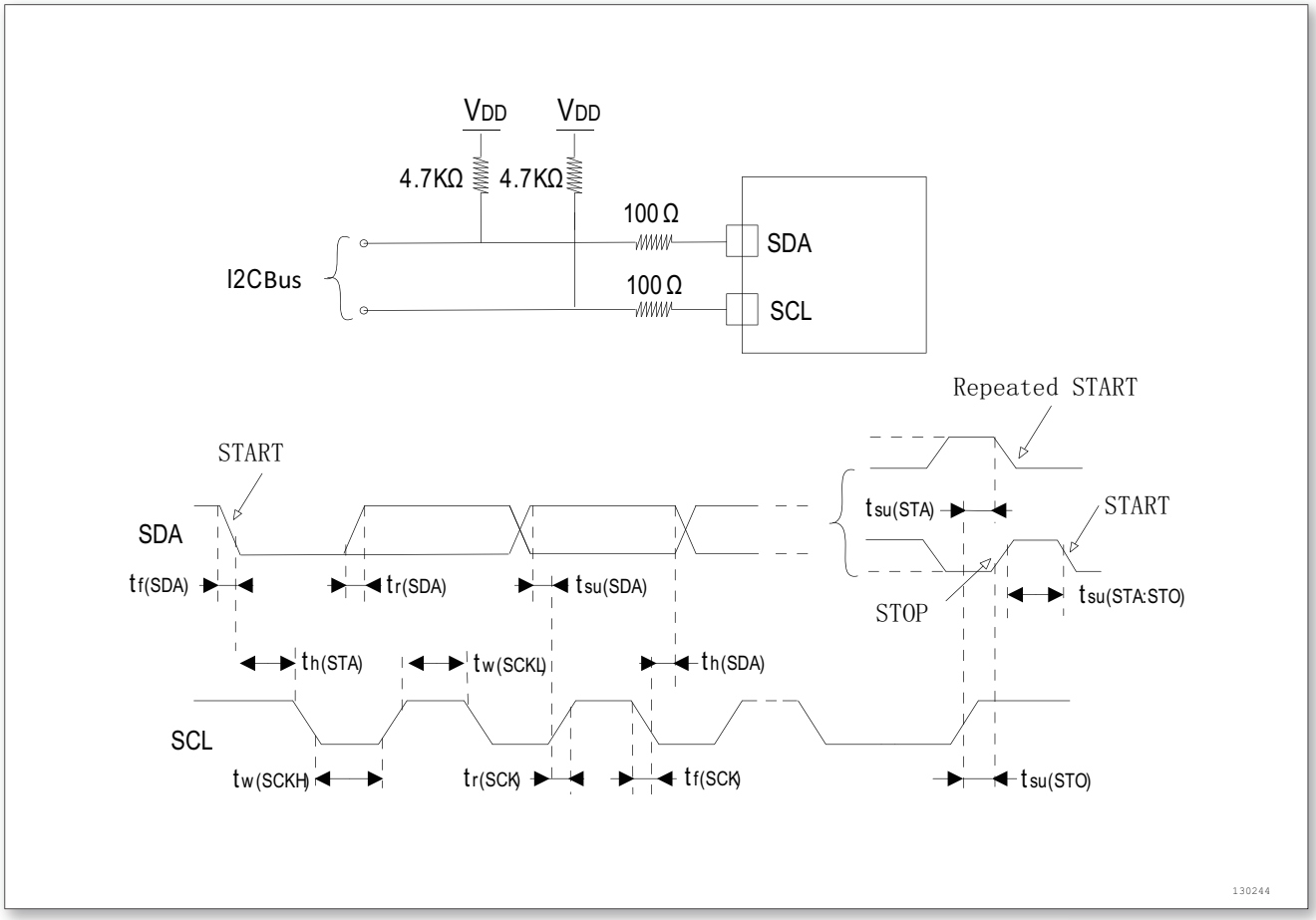

Figure 15. 12C bus AC waveform and measurement circuit(1)

1. The measurement points are set at CMOS level:0.3V_{DD} and 0.7V_{DD}.

SPI interface characteristics

Unless otherwise specified, the parameters listed in Table 33 are measured when ambient temperature, f_{PCLKx} frequency and VDD supply voltage meet the condition in Table 10.

For details on the characteristics of input/output multiplex function pins (NSS, SCK, MOSI, MISO),see subsubsec 5.3.10.

Table 33. SPI characteristics(1)

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$f_{SCK1/tc(SCK)}$	SPI clock frequency	Main mode		24	MHz
		Auxiliary mode		12	
$t_{r(SCK}$	SPI clock rise time	Load capacitance: C= 15pF		6	ns
$t_{f(SCK)}$	SPI clock fall time				
$t_{su(NSS)}$ (2)	NSS establishment time	Main mode	1TPCLK		ns
$t_{h(NSS)}$ (2)	NSS hold time	Auxiliary mode	2TPCLK		ns

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
$t_{w(SCKH)}$ (2)	SCK high time	Main mode, f_{PCLK} = 48MHz, prescaler coefficient = 2	t_{PCLK}- $t_{r(SCK/2)}$- $t_{f(SCK/2)}$	t_{PCLK} +$t_{r(SCK/2)}$ +$t_{f(SCK/2)}$	ns
$t_{w(SCKL)}$ (2)	SCK low time	Main mode, f_{PCLK}= 48MHz, prescaler coefficient = 2	t_{PCLK}- $t_{r(SCK/2)}$- $t_{f(SCK/2)}$	t_{PCLK} +$t_{r(SCK/2)}$ +$t_{f(SCK/2)}$	ns
$t_{su(MI)}$ (2)	Data input establishment time	Main mode	2		ns
$t_{su(SI)}$ (2)		Auxiliary mode	1		
$t_{h(MI)}$ (2)	Data input hold time	Main mode	5		ns
$t_{h(SI)}$ (2)		Auxiliary mode	1		
$t_{a(SO)}$ (2)(3)	Data output access time	Auxiliary mode, f_{PCLK}= 48MHz, prescaler coefficient = 4	1	$2T_{PCLK}$	ns
$t_{dis(SO)}$ (2)	Data output inhibition time	Auxiliary mode	1	$1T_{PCLK}$	
$t_{v(SO)}$ (2)(1)	Data output valid time	Auxiliary mode (after enabling edge)		20	
$t_{v(MO)}$ (2)(1)		Main mode (after enabling edge)		20	
$t_{h(SO)}$ (2)	Data output hold time	Auxiliary mode (after enabling edge)	1		ns
$t_{h(MO)}$ (2)		Main mode (after enabling edge)	1		

1. Drawn from comprehensive evaluation, not tested in production.
2. Minimum value indicates the drive output minimum time, and maximum value indicates the maximum time to obtain data correctly.
3. Minimum value represents the minimum time to close output, and maximum value represents the maximum time to put the data line in the high impedance state.

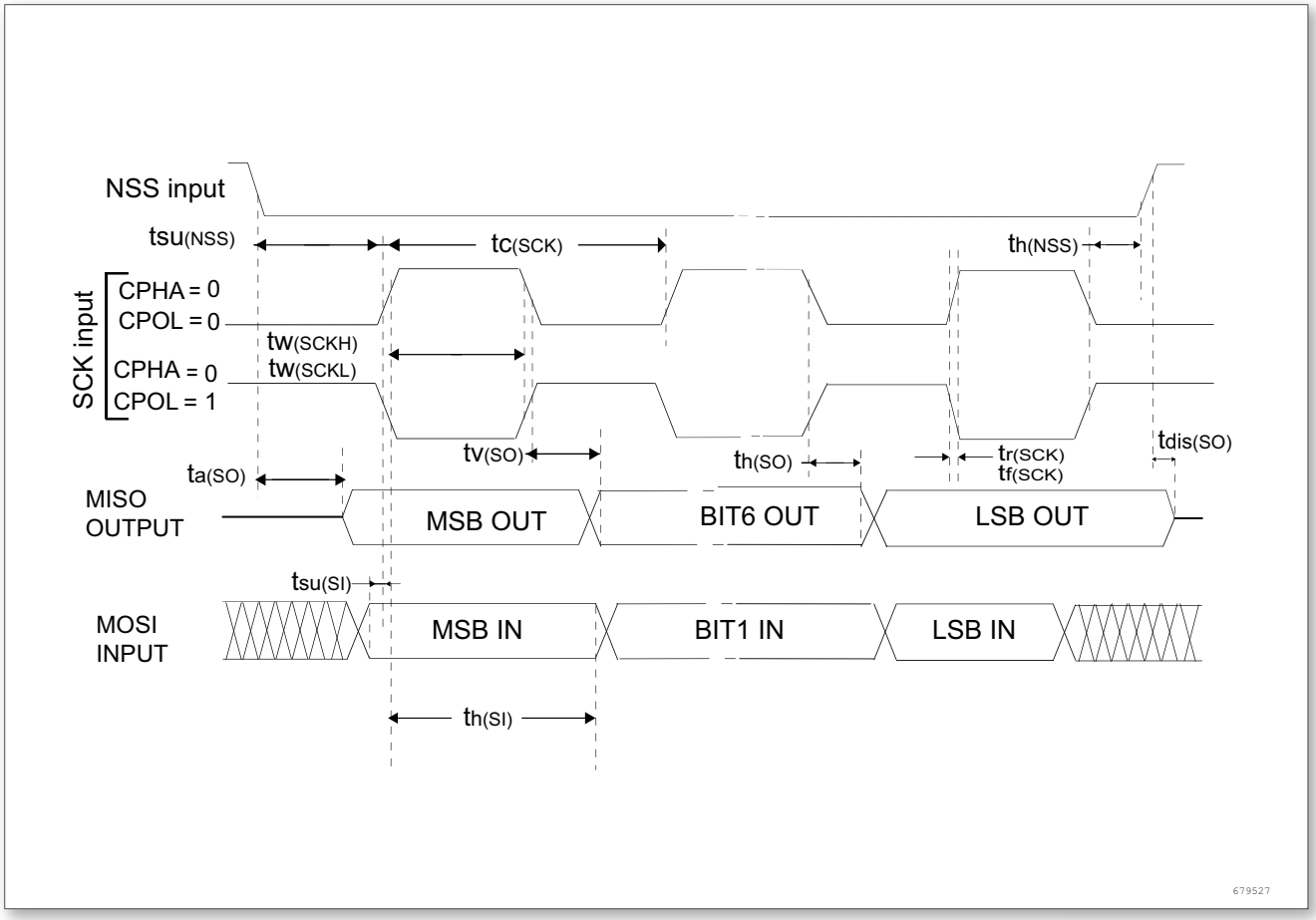

Figure 16. SPI timing diagram-slave mode and CPHA = 0

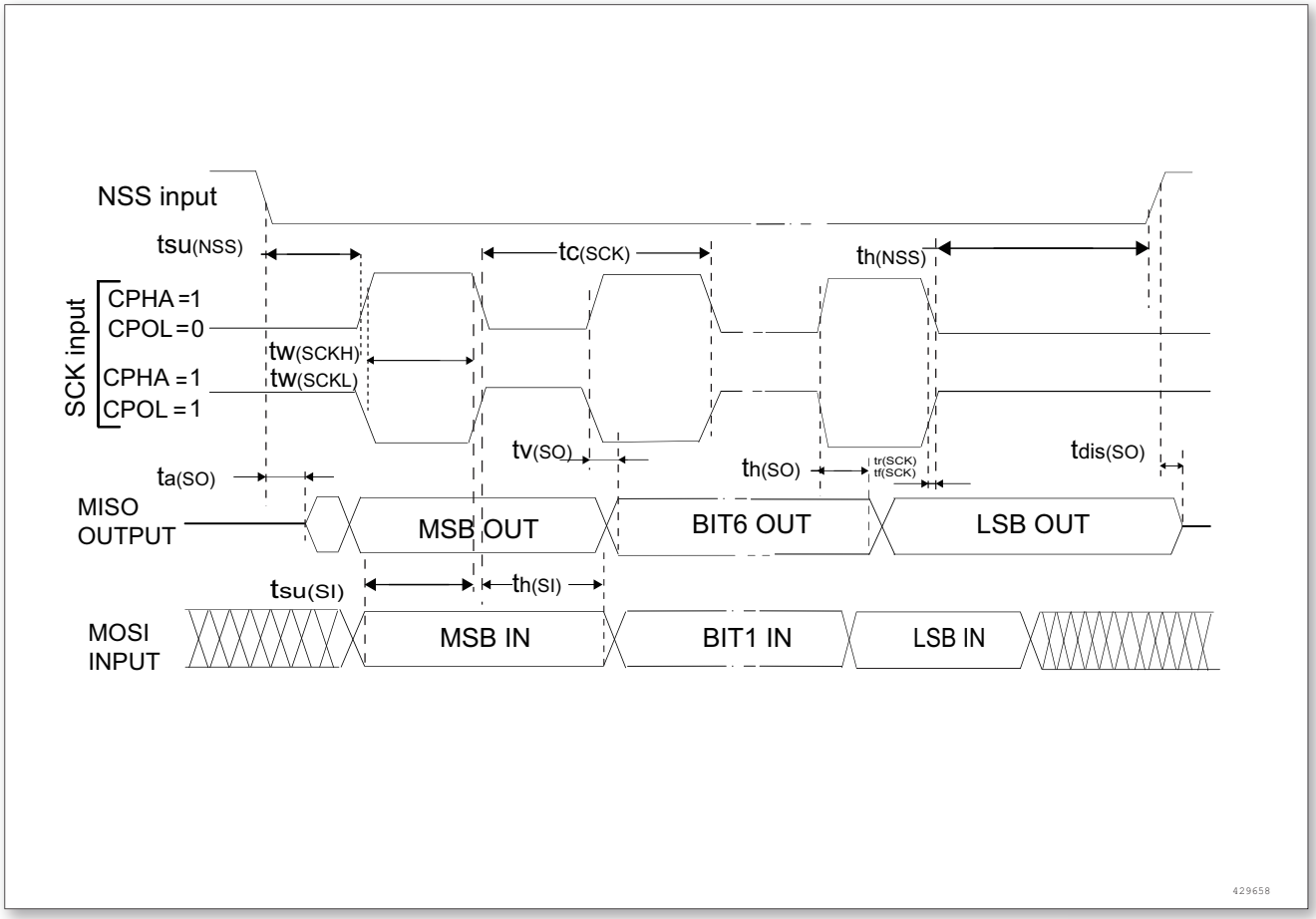

Figure 17. SPI timing diagram-slave mode and CPHA =1 (1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

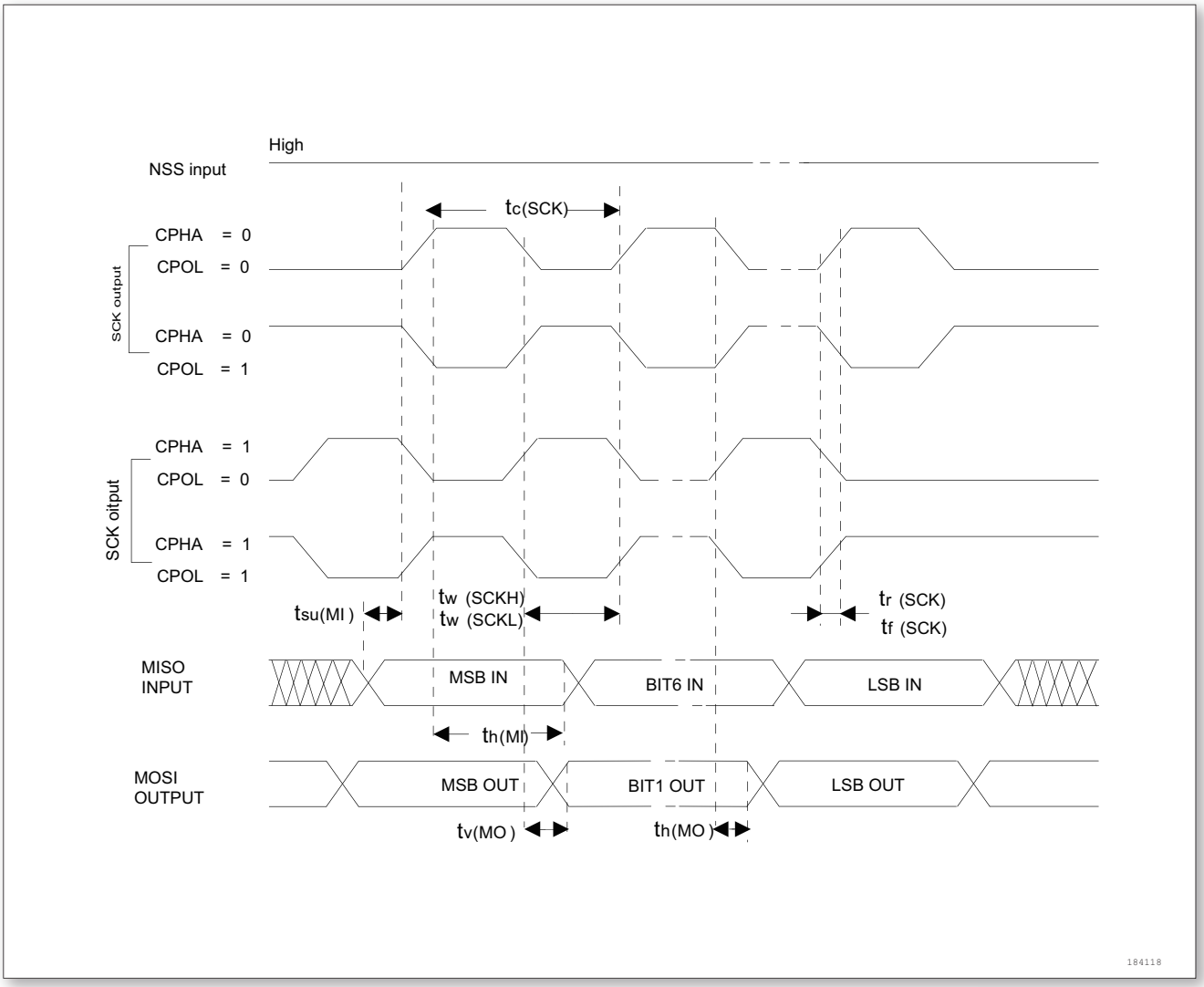

Figure 18. SPI timing diagram-master mode(1)

1. Measurement points are set at CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.14 12 bit ADC characteristics

Unless otherwise specified, the parameters in the following table are measured when ambient temperature, f_{PCLK1} frequency and VDD supply voltage meet the condition of Table 10.

Table 34. ADC characteristics

Symbol	Parameter	Conditions	Minimum value	Typeical value	Maximum value	Unit
V_{DD}	Supply voltage		2.0	3.3	5.5	V
f_{ADC}(1)(3)	ADC clock frequency				16	MHz
f_S(1)(3)	Sampling rate				1	MHz
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 15MHz			937.5	kHz
					16	$1/f_{ADC}$

Symbol	Parameter	Conditions	Minimum value	Typeical value	Maximum value	Unit
V_{AIN}(2)	Conversion voltage range		0		VDD	V
R_{AIN}(2)	External input impedance		See Equation 1 and Table 35			kΩ
R_{ADC}(1)	Sampling switch resistance				1.5	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				10	pF
t_S(1)	Sampling time	f_{ADC}= 16MHz	0.156		15.031	μS
			2.5		240.5	$1/f_{ADC}$
t_{STAB}(1)	Power-on time			1		μS
t_{CONV}(1)	Total conversion time (Including sampling time)	f_{ADC} = 16MHz	1		15.8125	μS
			15~253 (sampling t_S + stepwise approximation to 12.5)			$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production
2. Guaranteed by design, not tested in production.
3. For external trigger, a delay of $1/f_{ADC}$ must be added to the delay.

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times In(2^{N+2})} - R_{ADC} \quad (1)$$

The above formula (Equation 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB, where N = 12 (representing 12-bit resolution).

Table 35. Maximum R_{AIN} when f_{ADC} = 15MHz(1)

T_S (cycle)	t_S (μs)	Maximum R_{AIN} (kΩ)
2.5	0.156	0.1
8.5	0.531	4.0
14.5	0.906	7.8
29.5	1.844	17.5
42.5	2.656	25.9
56.5	3.531	34.9
72.5	4.531	45.2
240.5	15.031	153.4

1. Guaranteed by design, not tested in production.

Table 36. ADC accuracy—Limited testing conditions[1][2]

Symbol	Parameter	Test Conditions	Type	Max	Unit
ET	Composite error	f_{PCLK1} = 24MHz, f_{ADC} = 12MHz, R_{AIN} < 0.1KΩ, V_{DD} = 3.3V, T_A = 25°C	-7.5/+3		LSB
EO	Offset error		-3/+5		
EG	Gain error		±3		
ED	Differential linearity error		-1/+4		
EL	Integral linearity error		-4/+5		

1. Correlation between ADC accuracy and reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, because this will significantly reduce the accuracy of the ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) on the standard analog pin that may produce reverse injection current. If the forward injection current is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in subsubsec 5.3.11, it will not affect the ADC accuracy.
2. Guaranteed by comprehensive evaluation, not tested in production.

ET = Total unadjusted error: the maximum deviation between the actual and ideal transmission curves.

EO = Offset error: the deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: the deviation between the last ideal conversion and the last actual conversion.

ED = Differential linearity error: the maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: the maximum deviation between any actual conversion and the endpoint correlation line.

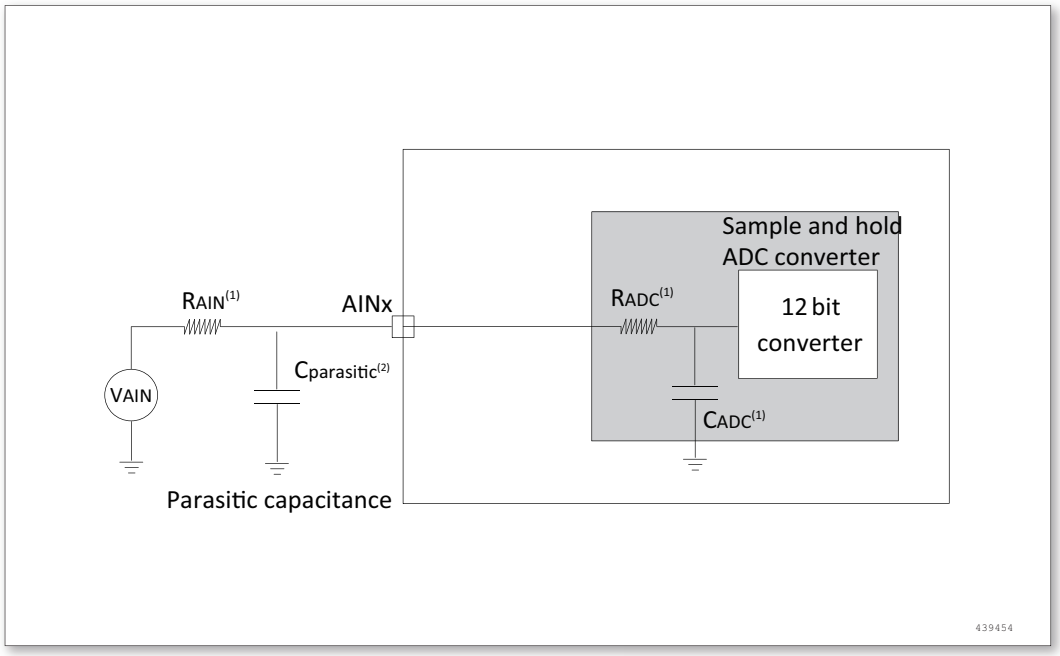

Figure 19. Typical connection diagram using ADC

1. Refer to Table 36 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ means the parasitic capacitance (about 7pF) on the PCB (related to welding and PCB layout quality) and pad. A larger $C_{parasitic}$ value will reduce the conversion accuracy. The solution is to reduce f_{ADC} .

PCB design proposals

The power supply decoupling must be connected according to the diagram below. The 10 nF capacitor in the diagram must be ceramic capacitors, which should be maximally to the MCU chip.

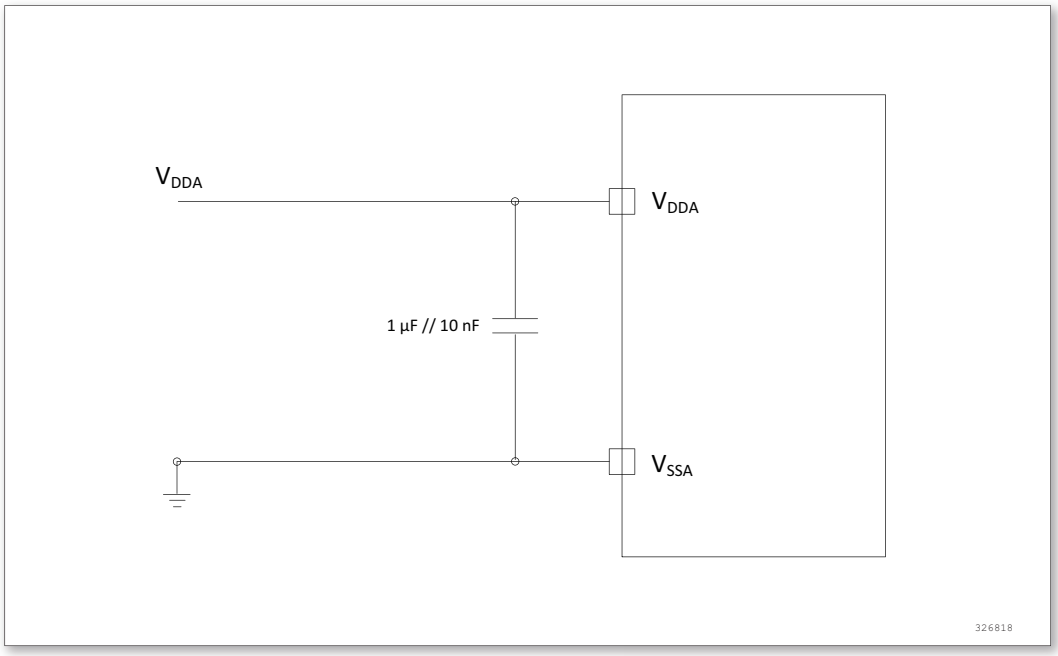

Figure 20. Decoupling circuit of power supply and reference power supply

6 Package Characteristics

Package Characteristics

6.1 Package QFN20

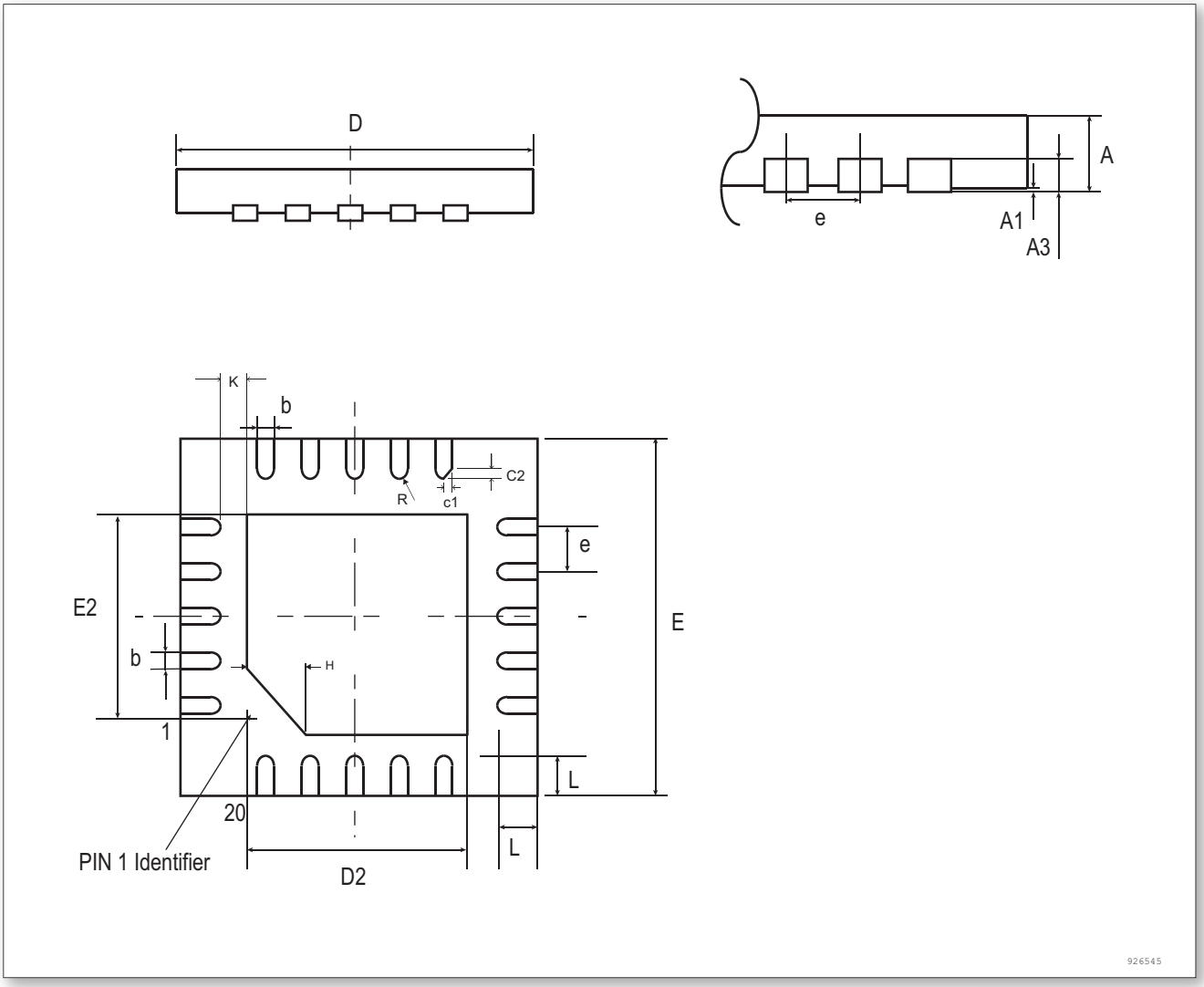

Figure 21. QFN20, 20-pin square flat cordless package exterior

1. The Diagram is not drawn to scale.
2. The size is in mm.

Table 37. size description

Label	Mm		
	Minimum value	Typical value	Maximum value
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.152REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e		0.40	
H	0.35REF		
K	0.40REF		
L	0.25	0.35	0.45
R	0.075		
N	Number of pins = 20		

6.2 Package TSSOP20

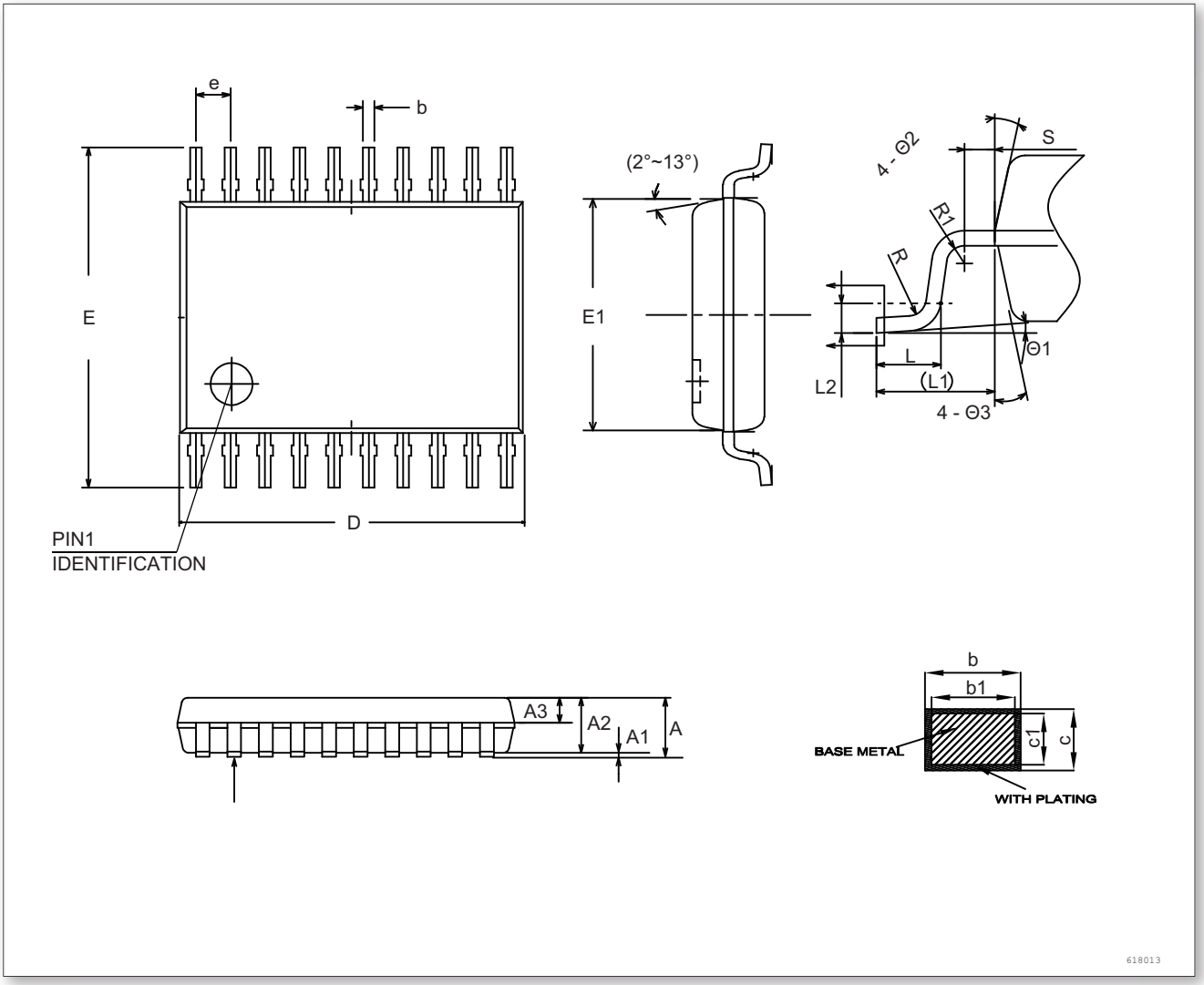

Figure 22. TSSOP20, 20-pin low profile rectangular flat package

1. The Diagram is not drawn to scale.
2. The size is in mm.

Table 38. TSSOP20 mechanical data

Label	Mm		
	Minimum value	Typical value	Maximum value
A	1.0	-	1.10
A1	0.05	-	0.15
A2	-	-	0.95
A3	0.39	-	0.40
b	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	-	0.15
D	6.40	6.45	6.50
E	6.25	6.40	6.55

Label	Mm		
	Minimum value	Typical value	Maximum value
E1	-	4.35	4.40
e	0.55	0.65	0.75
L	0.50	0.60	0.70
L2	0.25BSC		
L1	1.0REF		
R	0.09	-	-
θ1	0°	-	8°

7 Model Naming

Model Naming

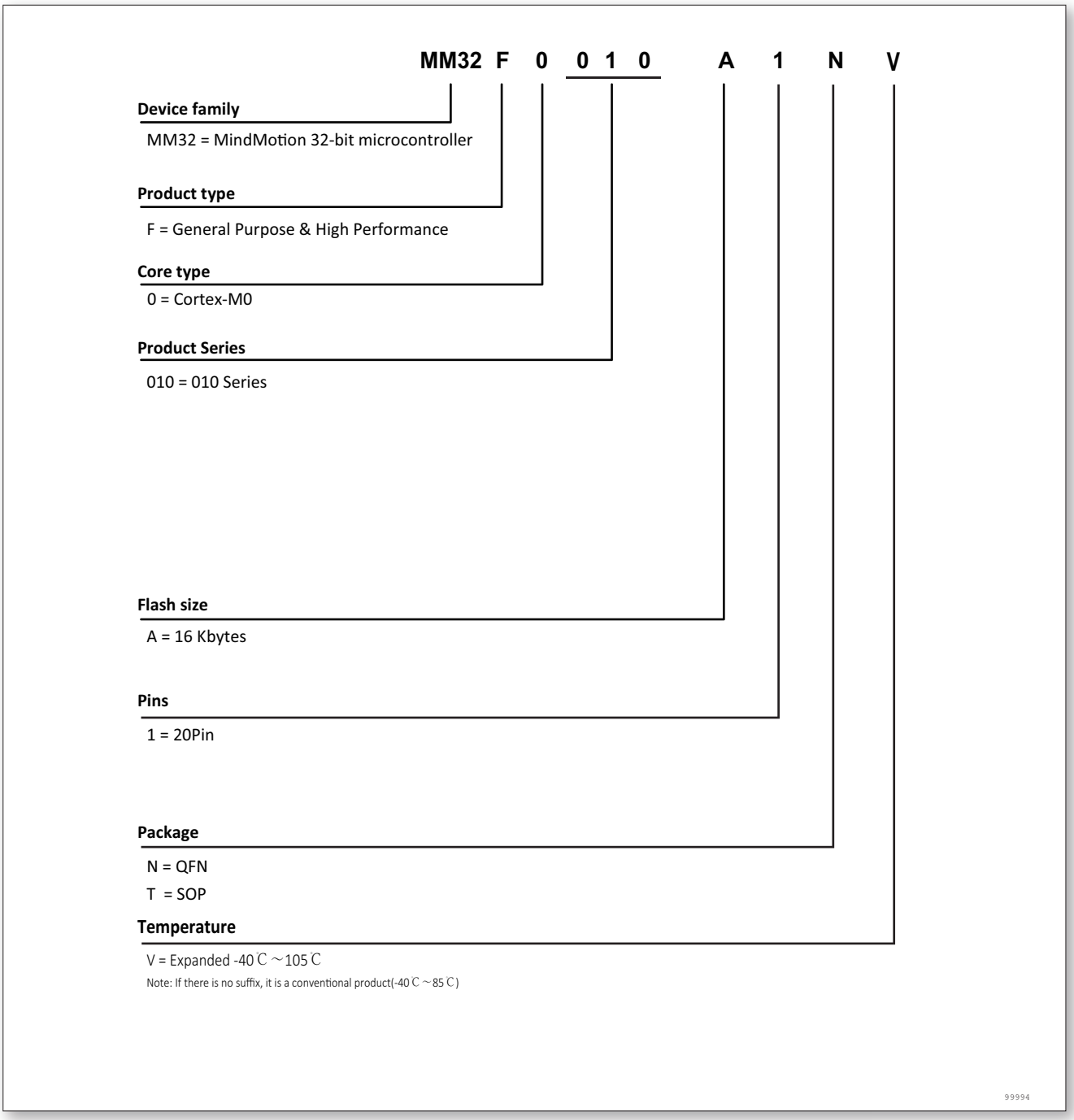

Figure 23. MM32 model naming

8 Revision Records

Revision Records

Table 39. Revision records

Date	Rev.	Content
2020/09/17	Rev1.00	Formal version