Datasheet

MM32F032xx

32-Bit Micro controller based on ARM® Cortex® M0

Ver: 1.00_s

Content

List of Figures

List of Tables

1 Introduction

Introduction

1.1 Description

The highest operating frequency is up to 72MHz, with built-in high-speed memory, a rich set of enhanced I/O ports and peripherals connected to the external bus. This product contains 1 x 12-bit ADC, 1 x general purpose 16-bit timer, 1 x general purpose 32-bit timer, 3 x Basic timers, 1 x Advanced 16-bit timer, and standard communication interfaces device: 1 x I2C, 2 x SPIs, and 2 x UARTs.

The device works between 2.0V to 5.5V range. The regular temperature for the device is -40°C to +85°C. A comprehensive set of power-saving mode allows the design of low-power applications.

The devices are available in 4 different packages: LQFP64, LQFP48, LQFP32 and QFN32. Depending on the device chosen, different sets of peripherals are included.

The abundant peripheral configurations enable the device to fit wide range of applications in difference industries, Few examples are as follows:

- Motor drive and application control
- Healthcare and fitness equipment
- PC peripherals, gaming, GPS equipment
- Industrial Applications: Programmable Controllers (PLCs), Inverters, Printers and Scanners
- Alarm system, wired and wireless sensors, video intercom

1.2 Product Features

- Core and system
  - ARM® Cortex®-M0 CPU
  - Maximum operating frequency is up to 72MHz
- Memories
  - 64K Bytes of Flash memory
  - 16K Bytes of SRAM
  - Boot loader support Chip Flash and ISP (In-System Programming)
- Clock, reset and power management
  - 2.0V to 5.5V application supply
  - Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)

  - POR reset voltage is low to 1.7V
  - PVD voltage threshold can be as low as 1.8V
  - External 1 ~ 24MHz high speed crystal oscillator
  - External 32.768K low speed oscillator
- Low-power
  - Sleep, Stop and Standby modes
- 1 x 12-bit ADC, 1μS A/D converters (up to 10 channels)
  - Conversion range: 0 to V_{DDA}
  - Support sampling time and resolution configuration
  - On-chip temperature sensor
  - On-chip voltage sensor
- 5 x DMA controller
  - Supported peripherals: Timer, UART, I2C, SPI and ADC
- Up to 56 fast I/Os:
  - All mappable on 16 external interrupt vectors
- Debug mode
  - Serial wire debug (SWD)
- Up to 9 timers
  - 1 x 16-bit 4-channel advanced-control timer for 4 channels PWM output, with deadtime generation and emergency stop
  - 1 x 16-bit timer and 1 32-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - 2 x 16-bit timer, with 1 IC/OC, 1 OCN, deadtime generation and emergency stop and modulator gate for IR control
  - 1 x 16-bit timer, with 1 IC/OC
  - 2 x watchdog timers (independent and window type)
  - SysTick timer: 24-bit downcounter
- Up to 5 Communication interfaces
  - 2 x UARTs
  - 1 x I2C
  - 2 x SPIs
- 96-bit unique ID (UID)
- Packages LQFP64, LQFP48, LQFP32 and QFN32

For more information about the complete product, refer to Section 2.2 of the data sheet. The relevant information about the Cortex®-M0, please refer to Cortex®-M0 technical reference manual.

2 Specification

Specification

2.1 Device contrast

Table 1. MM32F032xx device features and peripheral counts

Peripheral \ Device		MM32F032R6/8T6	MM32F032C6/8T6	MM32F032K6/8T6	MM32F032K6/8U6
Flash memory - KBytes		32/64	32/64	32/64	32/64
SRAM - KBytes		8/16	8/16	8/16	8/16
Timers	General (16 bit)	1	1	1	1
	General (32 bit)	1	1	1	1
	Base	3	3	3	3
	Advanced	1	1	1	1
Communications	UART	2	2	2	2
	I2C	1	1	1	1
	SPI	2	2	1	1
GPIO Ports		55	38	24	26
A/D Converters 12-bit	Number	1	1	1	1
	Channels	10	10	10	10
RTC		√			
Max CPU frequency		72 MHz			
Supply Voltage		2.0V ~ 5.5V			
Packages		LQFP64	LQFP48	LQFP32	QFN32

2.2 Summary

2.2.1 ARM® Cortex®-M0 and SRAM

The ARM® Cortex®-M0 is a generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high

performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The devices have embedded ARM core and are compatible with all ARM tools and software.

2.2.2 Memory

64K Bytes of embedded Flash memory.

2.2.3 SRAM

16K Bytes of embedded SRAM.

2.2.4 Clocks and startup

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 72MHz.Refer to figure 2 for the clock drive block diagram.

2.2.5 Cyclic Redundancy Check (CRC)

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word.

In many applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors that can be used to compute the signature of the software in real time and to compare the generated signatures when linking and generating the software.

2.2.6 Nested vectored interrupt controller (NVIC)

The device embeds a nested vectored interrupt controller and is able to handle up to 68 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) with 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.7 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of many edge detector lines are used to generate interrupt/event requests for waking up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal APB2 clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.2.8 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using UART1.

2.2.9 Power supply schemes

- V_{DD} = 2.0V ~ 5.5V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.5V ~ 5.5V: external analog power supply for ADC, reset blocks, oscillators and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}.

2.2.10 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 1.8V. The device remains in reset mode when the monitored supply voltage is below a specified threshold $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when VDD drops below the V_{PVD} threshold and/or when VDD is higher than the V_{PVD} threshold.The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.11 Voltage regulator

The voltage regulator converts the external voltage to the internal digital logic and it is always enabled after reset.

2.2.12 Low-power modes

The device support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. the HSI and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

Standby mode

Standby mode achieves the lowest power consumption of the system. This mode turns off the voltage regulator in CPU deep sleep mode. The entire 1.5V power supply area is powered down. HSI and HSE oscillators are also powered down. SRAM and register contents are missing. Only the backup registers and standby circuits remain powered.

2.2.13 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: UART、I2C、SPI、ADC、general-purpose and advanced-control timers TIMx.

2.2.14 real-time clock register (RTC)

The real time clock is an independent timer. The RTC module has a set of counters that count continuously and provides the clock calendar function in the appropriate software configuration. Modify the value of the counter to reset the current time and date of the system. The RTC module and the clock configuration system (RCC_BDCR register) are in the backup area, ie the RTC settings and time remain unchanged after a system reset or wake-up in standby mode.

2.2.15 Backup register (BKP)

The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are still powered by V_{BAT}. They are also not reset when the system is woken up in standby mode, or when the system is reset or power is reset.

2.2.16 Timers and watchdogs

Medium capacity device include 1 advanced control、2 general-purpose timers 、3 base-timer 、2 watchdog timers and 1 SysTick timer.

The following table compares the features of the different timers:

Table 2. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/-compare channels	Complem-entary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	integer from 1 to $2^{32}-1$	Yes	4	No
	TIM3	16-bit	Up, down, up/down	integer from 1 to 65536	Yes	4	No
Basic	TIM14	16-bit	Up	integer from 1 to 65536	Yes	1	No
	TIM16 / TIM17	16-bit	Up	integer from 1 to 65536	Yes	1	Yes

Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for：

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)

- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are 2 synchronizable general-purpose timers (TIM2、TIM3).

General-purpose timers 32-bit

The timer is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

General-purpose timers 16-bit

TIM3

The timer is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

The timer can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Basic timer

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output. Their counter can be frozen in debug mode.

TIM16/TIM17

Every timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. They each have a single channel for input capture/output compare, PWM or one-pulse mode output. TIM16 and TIM17 have a complementary output with dead-time generation and indepen-

dent DMA request generation. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.2.17 Universal asynchronous receiver/transmitter (UART)

UART provides hardware management of the CTS, RTS.

All UART interface can be served by the DMA controller.

2.2.18 I2C interface

The I2C interface can operate in multimaster or slave modes. It can support Standard mode,and Fast Mode.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask).

2.2.19 Serial peripheral interface (SPI)

The SPI interface, in slave or master mode, can be configured to 1 ~ 32 bits per frame.

All SPI interface can be served by the DMA controller.

2.2.20 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.21 Analog-to-digital converter (ADC)

The one 12-bit analog-to-digital converters is embedded into microcontrollers and the ADC shares up to 10 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs. The ADC can be served by the DMA controller.

The analog watchdog function allows very precise monitoring of all the way, multiple or all selected channels, and an interruption occurs when the monitored signal exceeds the preset threshold. The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger to allow the application to synchronize A/D conversion and timers.

2.2.22 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the input channel which is used to convert the sensor output voltage into a digital value.

2.2.23 Serial single line SWD debug port (SW-DP)

Built-in ARM two-wire serial debug port (SW-DP).

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

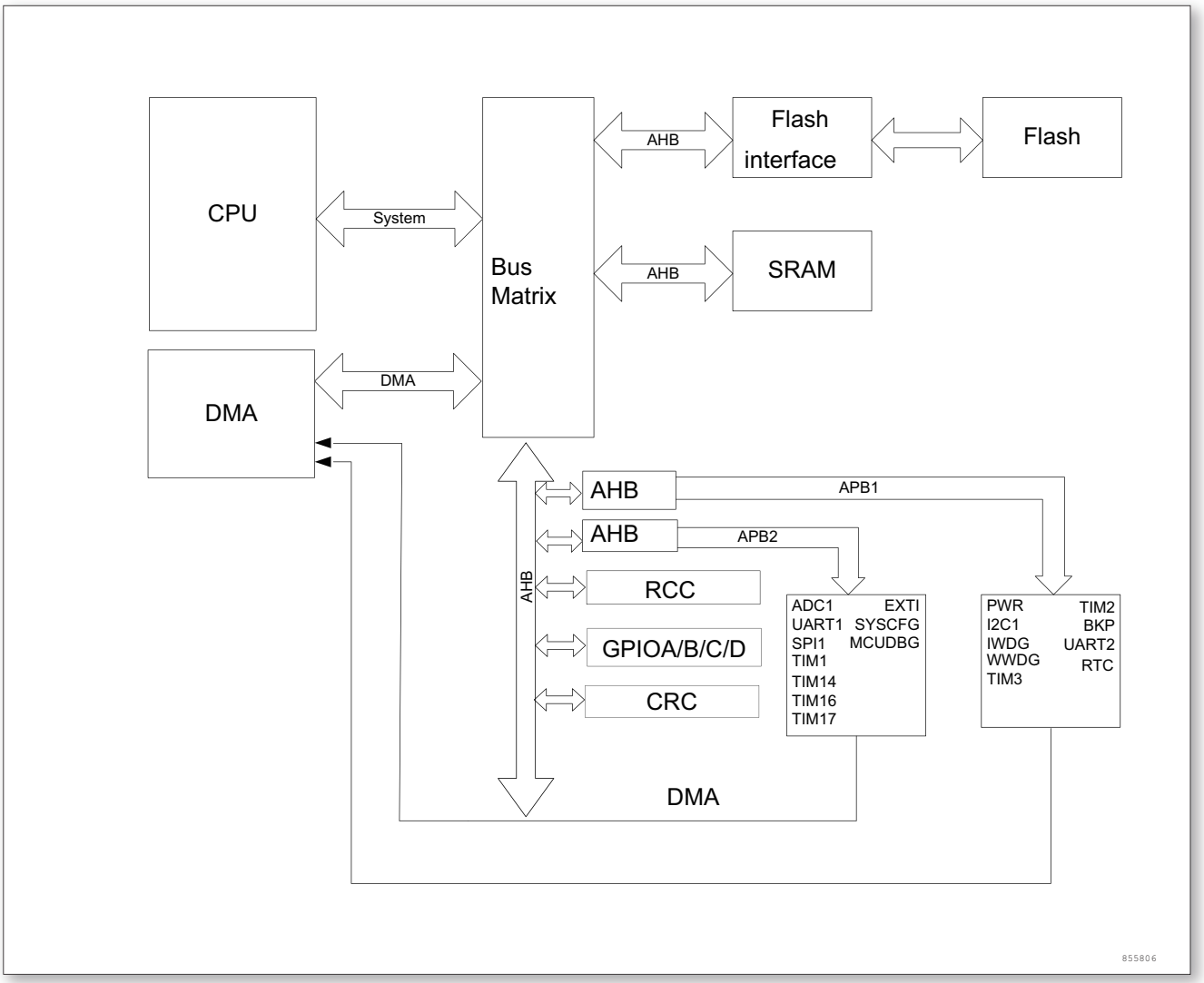

Figure 1. Block diagram

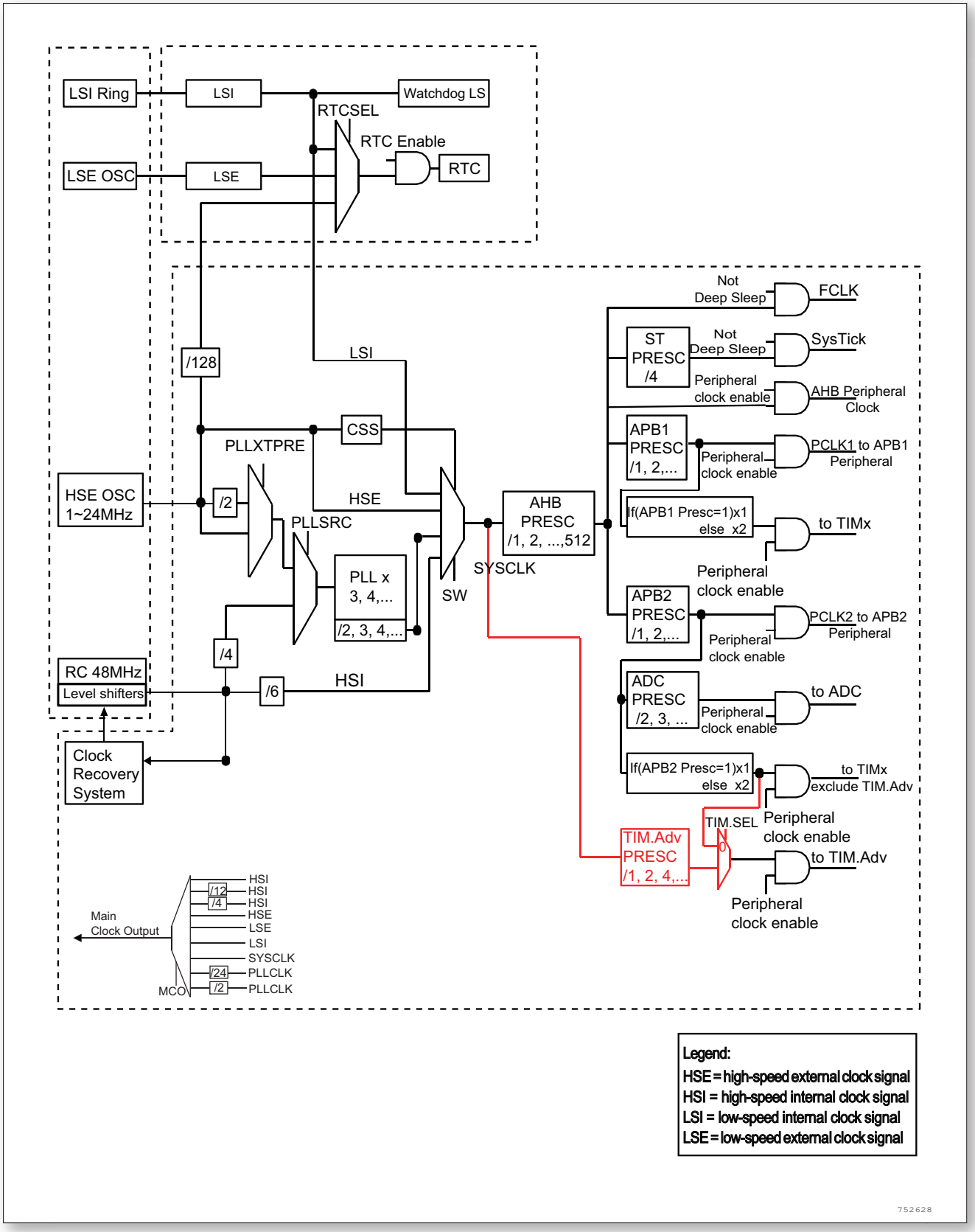

Figure 2. Clock tree

3 Pin definition

Pin definition

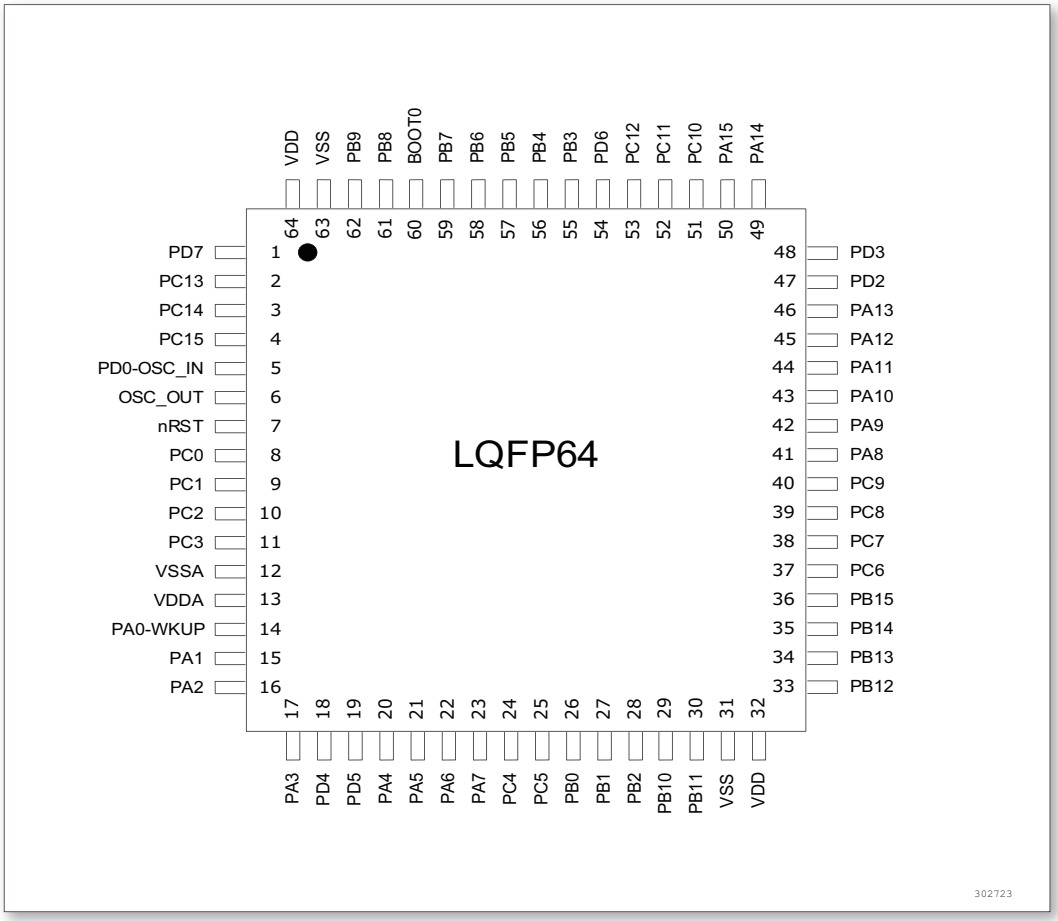

Figure 3. LQFP64 packet pinout

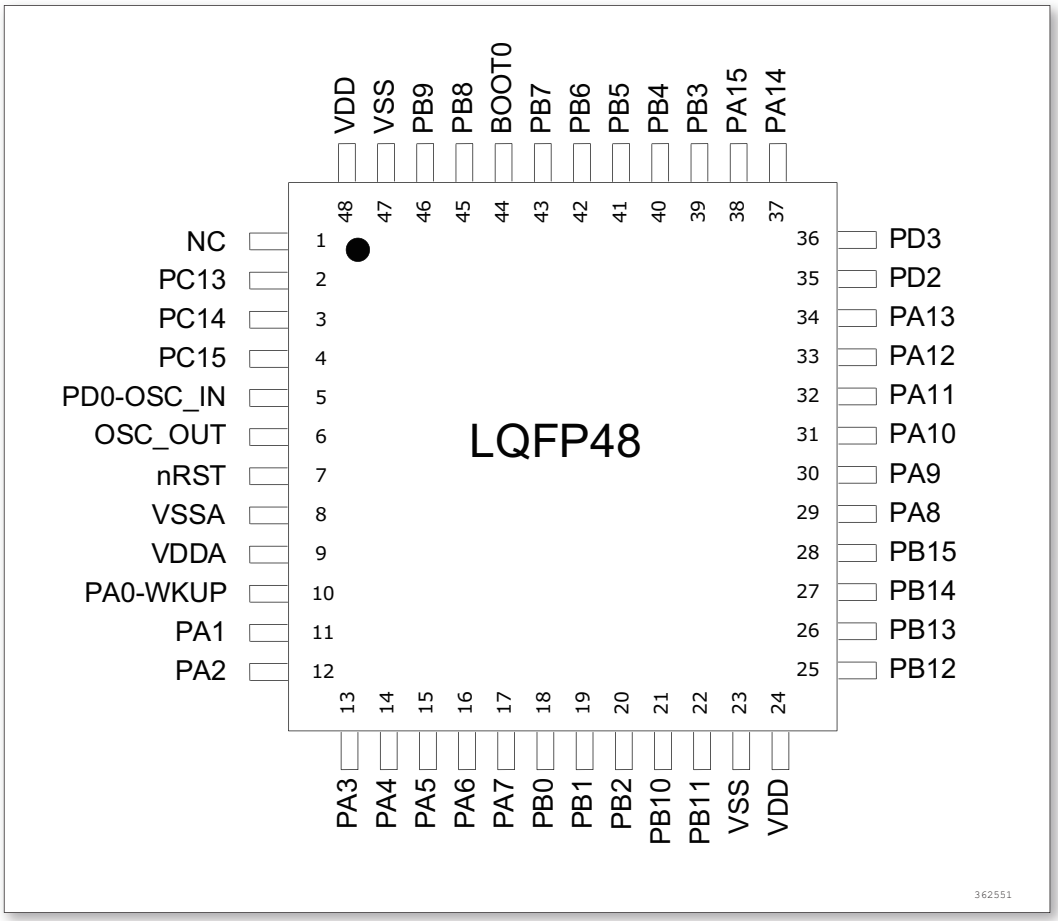

Figure 4. LQFP48 packet pinout

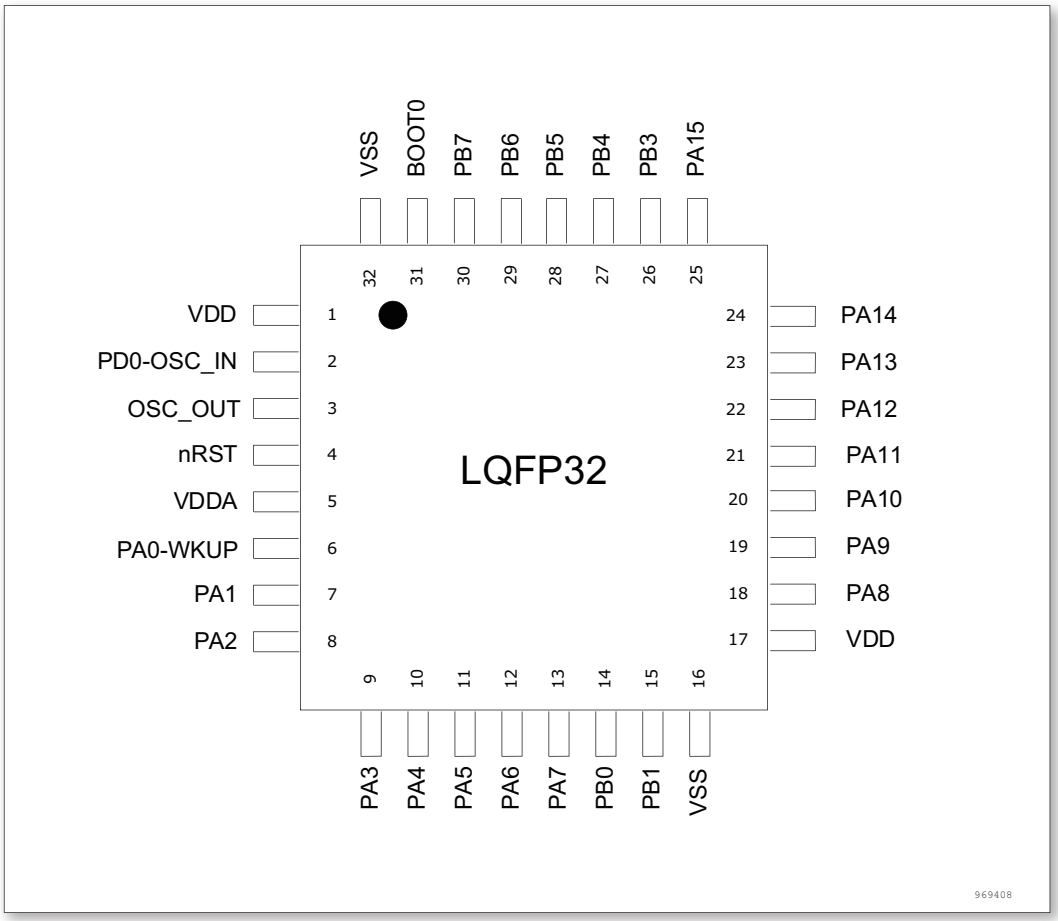

Figure 5. LQFP32 packet pinout

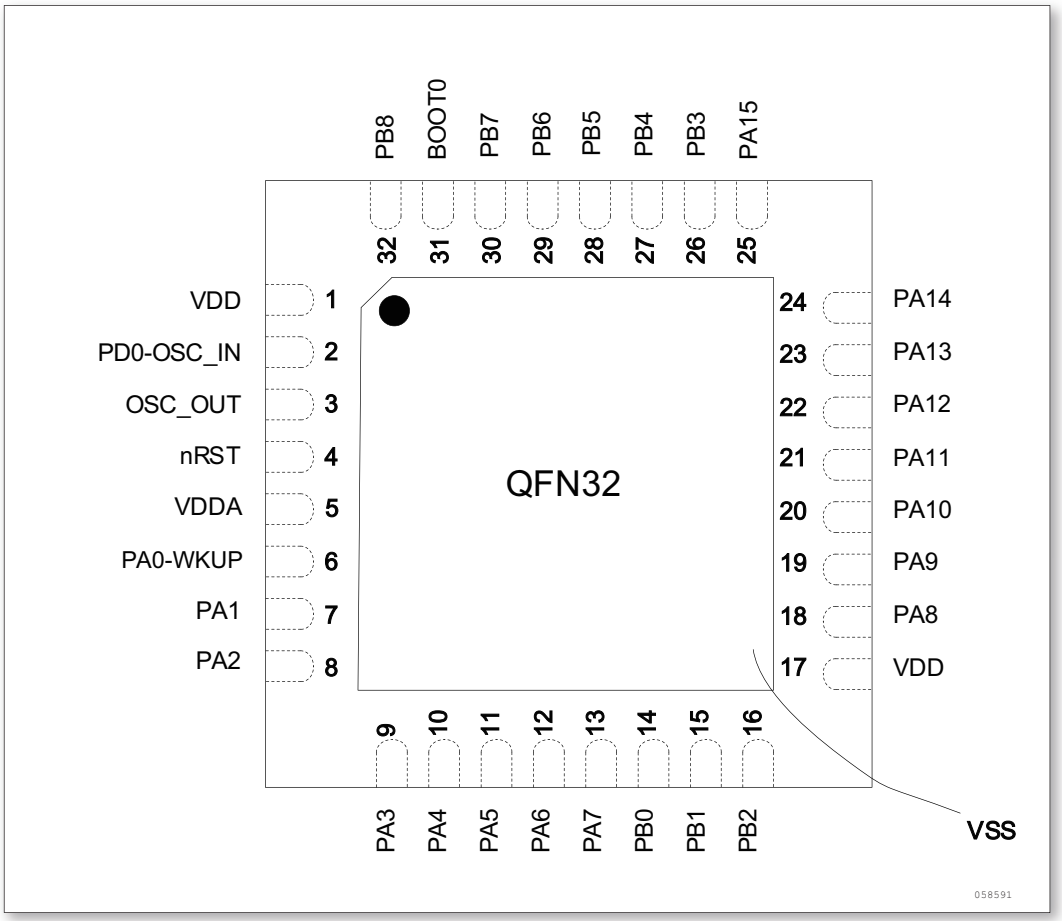

Figure 6. QFN32packet pinout

Table 3. Pin definitions

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
1	-	-	-	PD7	I/O	TC	PD7	TIM3_CH1 TIM17_CH1	-
2	2	-	-	PC13	I/O	TC	PC13	TIM2_CH1 TIM2_ETR	-
3	3	-	-	PC14 OSC32_IN	I/O	TC	PC14	TIM2_CH2	-
4	4	-	-	PC15 OSC32_OUT	I/O	TC	PC15	TIM2_CH3	-
5	5	2	2	PD0 OSC_IN	I/O	TC	PD0	I2C1_SDA TIM1_CH1N UART1_TX TIM1_CH2 SPI1_MOSI	-
6	6	3	3	OSC_OUT	O	-	-	-	-

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
7	7	4	4	nRST	I/O	TC	nRST	-	-
8	-	-	-	PC0	I/O	TC	PC0	-	-
9	-	-	-	PC1	I/O	TC	PC1	-	-
10	-	-	-	PC2	I/O	TC	PC2	SPI2_MISO	-
11	-	-	-	PC3	I/O	TC	PC3	SPI2_MOSI	-
12	8	16	0	VSSA	S	-	VSSA	-	-
13	9	5	5	VDDA	S	-	VDDA	-	-
14	10	6	6	PA0 WKUP	I/O	TC	PA0	UART2_CTS TIM2_CH1_ETR UART1_RX TIM14_CH1	ADC1_VIN[0]
15	11	7	7	PA1	I/O	TC	PA1	UART2_RTS TIM2_CH2 TIM1_CH2 UART1_TX	ADC1_VIN[1]
16	12	8	8	PA2	I/O	TC	PA2	UART2_TX TIM2_CH3 TIM1_CH2N	ADC1_VIN[2]
17	13	9	9	PA3	I/O	TC	PA3	UART2_RX TIM2_CH4 TIM1_CH3	ADC1_VIN[3]
18	-	-	-	PD4	I/O	TC	PD4	SPI1_MISO SPI1_MOSI	-
19	-	-	-	PD5	I/O	TC	PD5	SPI1_MOSI SPI1_MISO	-
20	14	10	10	PA4	I/O	TC	PA4	SPI1_NSS SPI1_SCK TIM1_CH3N TIM14_CH1 TIM1_BKIN	ADC1_VIN[4]
21	15	11	11	PA5	I/O	TC	PA5	SPI1_SCK SPI1_NSS TIM2_CH1_ETR TIM1_CH3N	ADC1_VIN[5]

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
22	16	12	12	PA6	I/O	TC	PA6	SPI1_MISO TIM3_CH1 TIM1_BKIN TIM16_CH1 TIM1_CH3	ADC1_VIN[6]
23	17	13	13	PA7	I/O	TC	PA7	SPI1_MOSI TIM3_CH2 TIM1_CH1N TIM1_CH3N TIM14_CH1 TIM17_CH1 TIM1_CH2N	ADC1_VIN[7]
24	-	-	-	PC4	I/O	TC	PC4	UART2_TX TIM3_CH1 SPI1_MOSI	-
25	-	-	-	PC5	I/O	TC	PC5	UART2_RX TIM3_CH2 SPI1_MISO	-
26	18	14	14	PB0	I/O	TC	PB0	TIM3_CH3 TIM1_CH2N TIM1_CH1N TIM1_CH3	ADC1_VIN[8]
27	19	15	15	PB1	I/O	TC	PB1	TIM14_CH1 TIM3_CH4 TIM1_CH3N TIM1_CH2N TIM2_CH3 TIM1_CH2 TIM1_CH1N	ADC1_VIN[9]
28	20	-	16	PB2	I/O	TC	PB2	-	-
29	21	-	-	PB10	I/O	TC	PB10	I2C1_SCL TIM2_CH3 SPI2_SCK	-
30	22	-	-	PB11	I/O	TC	PB11	I2C1_SDA TIM2_CH4	-
31	23	16	0	VSS	S	-	VSS	-	-

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
32	14	17	17	VDD	S	-	VDD	-	-
33	25	-	-	PB12	I/O	TC	PB12	SPI2_NSS SPI2_SCK TIM1_BKIN SPI2_MOSI SPI2_MISO	-
34	26	-	-	PB13	I/O	TC	PB13	SPI2_SCK SPI2_MISO TIM1_CH1N SPI2_NSS SPI2_MOSI I2C1_SCL TIM17_CH1 TIM1_CH3N	-
35	27	-	-	PB14	I/O	TC	PB14	SPI2_MISO SPI2_MOSI TIM1_CH2N SPI2_SCK SPI2_NSS I2C1_SDA TIM1_CH3 TIM1_CH1	-
36	28	-	-	PB15	I/O	TC	PB15	SPI2_MOSI SPI2_NSS TIM1_CH3N SPI2_MISO SPI2_SCK CSM_CH2_TXRX TIM1_CH2N TIM1_CH2	-
37	-	-	-	PC6	I/O	TC	PC6	TIM3_CH1 TIM3_CH3 SPI1_NSS	-
38	-	-	-	PC7	I/O	TC	PC7	TIM3_CH2 TIM2_CH1_ETR SPI1_SCK	-

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
39	-	-	-	PC8	I/O	TC	PC8	TIM3_CH3 TIM2_CH2	-
40	-	-	-	PC9	I/O	TC	PC9	TIM3_CH4 TIM2_CH3	-
41	29	18	18	PA8	I/O	TC	PA8	MCO TIM1_CH1 CSM_CH1_TXRX TIM1_CH2 TIM1_CH3	-
42	30	19	19	PA9	I/O	TC	PA9	UART1_TX TIM1_CH2 UART1_RX I2C1_SCL MCO TIM1_CH1N	-
43	31	20	20	PA10	I/O	TC	PA10	TIM17_BKIN UART1_RX TIM1_CH3 UART1_TX I2C1_SDA TIM1_CH1 TIM16_CH1	-
44	32	21	21	PA11	I/O	TC	PA11	UART1_CTS TIM1_CH4 TIM1_CH3 I2C1_SCL TIM1_BKIN	-
45	33	22	22	PA12	I/O	TC	PA12	UART1_RTS TIM1_ETR TIM1_CH3N I2C1_SDA TIM1_CH2	-
46	34	23	23	PA13	I/O	TC	PA13	SWDIO UART1_TX	-
47	35	-	-	PD2	I/O	TC	PD2	I2C1_SCL SPI1_NSS	-

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
48	36	-	-	PD3	I/O	TC	PD3	I2C1_SDA SPI1_SCK SPI1_MISO	-
49	37	24	24	PA14	I/O	TC	PA14	SWDCLK UART2_TX UART1_RX	-
50	38	25	25	PA15	I/O	TC	PA15	SPI1_NSS UART2_RX TIM2_CH1_ETR SPI2_SCK SPI2_MOSI SPI2_MISO TIM1_CH1N TIM1_CH3N	-
51	-	-	-	PC10	I/O	TC	PC10	UART1_TX SPI2_MISO SPI2_SCK SPI2_NSS SPI2_MOSI	-
52	-	-	-	PC11	I/O	TC	PC11	UART1_RX SPI2_MOSI SPI2_NSS SPI2_SCK SPI2_MISO	-
53	-	-	-	PC12	I/O	TC	PC12	UART1_TX SPI2_SCK SPI2_MISO SPI2_MOSI SPI2_NSS	-
54	-	-	-	PD6	I/O	TC	PD6	TIM3_ETR TIM1_CH3N TIM1_CH1 TIM1_CH1N	-

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
55	39	26	26	PB3	I/O	TC	PB3	SPI1_SCK TIM2_CH2 TIM1_CH1 TIM1_CH2N TIM1_CH3	-
56	40	27	27	PB4	I/O	TC	PB4	SPI1_MISO TIM3_CH1 TIM1_CH2 TIM17_BKIN TIM1_CH3N TIM1_CH2N	-
57	41	28	28	PB5	I/O	TC	PB5	SPI1_MOSI TIM3_CH2 TIM16_BKIN TIM1_CH1 TIM1_CH2	-
58	42	29	29	PB6	I/O	TC	PB6	UART1_TX I2C1_SCL TIM16_CH1N TIM1_CH2N TIM1_CH2 TIM1_CH1N	-
59	43	30	30	PB7	I/O	TC	PB7	UART1_RX I2C1_SDA TIM17_CH1N TIM1_CH3 TIM1_CH1	-
60	44	31	31	BOOT0	I	-	BOOT0	-	-
61	45	-	32	PB8	I/O	TC	PB8	UART1_RX I2C1_SCL TIM16_CH1 TIM1_CH1 TIM3_CH2	-

Pin number				Pin name	Type(1)	I/O structure(2)	Main function	Alternate functions	Additional functions
LQFP 64	LQFP 48	LQFP 32	QFN 32						
62	46	-	-	PB9	I/O	TC	PB9	UART1_TX I2C1_SDA TIM17_CH1 SPI2_NSS TIM3_CH3	-
63	47	32	0	VSS	S	-	VSS	-	-
64	48	1	1	VDD	S	-	VDD	-	-

1. I = input, O = output, S = power supply, HiZ = high resistance.
2. TC: Standard I/O, Input signal does not exceed VDD.

Table 4. Alternate functions for port A

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART2_CTS	TIM2_CH1 TIM2_ETR	-	UART1_RX	-	TIM14_CH1	-
PA1	-	UART2_RTS	TIM2_CH2	TIM1_CH2	UART1_TX	-	-	-
PA2	-	UART2_TX	TIM2_CH3	TIM1_CH2N	-	-	-	-
PA3	-	UART2_RX	TIM2_CH4	TIM1_CH3	-	-	-	-
PA4	SPI1_NSS	SPI1_SCK	-	TIM1_CH3N	TIM14_CH1	TIM1_BKIN	-	-
PA5	SPI1_SCK	SPI1_NSS	TIM2_CH1 TIM2_ETR	-	-	-	TIM1_CH3N	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	TIM1_CH3	-
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	TIM1_CH3N	TIM14_CH1	TIM17_CH1	TIM1_CH2N	-
PA8	MCO	-	TIM1_CH1	-	-	CSM_CH1_ TXRX	TIM1_CH2	TIM1_CH3
PA9	-	UART1_TX	TIM1_CH2	UART1_RX	I2C1_SCL	MCO	TIM1_CH1N	-
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C1_SDA	TIM1_CH1	TIM16_CH1	-
PA11	-	UART1_CTS	TIM1_CH4	TIM1_CH3	-	I2C1_SCL	TIM1_BKIN	-
PA12	-	UART1_RTS	TIM1_ETR	TIM1_CH3N	-	I2C1_SDA	TIM1_CH2	-
PA13	SWDIO	-	-	UART1_TX	-	-	-	-
PA14	SWDCLK	UART2_TX	-	UART1_RX	-	-	-	-
PA15	SPI1_NSS	UART2_RX	TIM2_CH1 TIM2_ETR	SPI2_SCK	SPI2_MOSI	SPI2_MISO	TIM1_CH1N	TIM1_CH3N

Table 5. Alternate functions for port B

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	-	TIM3_CH3	TIM1_CH2N	TIM1_CH1N	TIM1_CH3	-	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TIM1_CH2N	TIM2_CH3	TIM1_CH2	TIM1_CH1N	-
PB3	SPI1_SCK	-	TIM2_CH2	-	TIM1_CH1	-	TIM1_CH2N	TIM1_CH3
PB4	SPI1_MISO	TIM3_CH1	-	-	TIM1_CH2	TIM17_BKIN	TIM1_CH3N	TIM1_CH2N
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN	-	-	-	TIM1_CH1	TIM1_CH2
PB6	UART1_TX	I2C1_SCL	TIM16_CH1N	-	TIM1_CH2N	-	TIM1_CH2	TIM1_CH1N
PB7	UART1_RX	I2C1_SDA	TIM17_CH1N	-	-	-	TIM1_CH3	TIM1_CH1
PB8	UART1_RX	I2C1_SCL	TIM16_CH1	TIM1_CH1	-	-	TIM3_CH2	-
PB9	UART1_TX	I2C1_SDA	TIM17_CH1	-	-	SPI2_NSS	TIM3_CH3	-
PB10	-	I2C1_SCL	TIM2_CH3	-	-	SPI2_SCK	-	-
PB11	-	I2C1_SDA	TIM2_CH4	-	-	-	-	-
PB12	SPI2_NSS	SPI2_SCK	TIM1_BKIN	SPI2_MOSI	SPI2_MISO	-	-	-
PB13	SPI2_SCK	SPI2_MISO	TIM1_CH1N	SPI2_NSS	SPI2_MOSI	I2C1_SCL	TIM17_CH1	TIM1_CH3N
PB14	SPI2_MISO	SPI2_MOSI	TIM1_CH2N	SPI2_SCK	SPI2_NSS	I2C1_SDA	TIM1_CH3	TIM1_CH1

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB15	SPI2_MOSI	SPI2_NSS	TIM1_CH3N	SPI2_MISO	SPI2_SCK	CSM_CH2_ TXRX	TIM1_CH2N	TIM1_CH2

Table 6. Alternate functions for port C

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC2	-	SPI2_MISO	-	-	-	-	-	-
PC3	-	SPI2_MOSI	-	-	-	-	-	-
PC4	-	-	-	UART2_TX	-	TIM3_CH1	SPI1_MOSI	-
PC5	-	-	-	UART2_RX	-	TIM3_CH2	SPI1_MISO	-
PC6	-	TIM3_CH1	-	-	-	TIM3_CH3	SPI1_NSS	-
PC7	-	TIM3_CH2	-	-	-	TIM2_CH1 TIM2_ETR	SPI1_SCK	-
PC8	-	TIM3_CH3	-	-	-	TIM2_CH2	-	-
PC9	-	TIM3_CH4	-	-	-	TIM2_CH3	-	-
PC10	UART1_TX	-	-	SPI2_MISO	SPI2_SCK	SPI2_NSS	SPI2_MOSI	-
PC11	UART1_RX	-	-	SPI2_MOSI	SPI2_NSS	SPI2_SCK	SPI2_MISO	-
PC12	UART1_TX	-	-	SPI2_SCK	SPI2_MISO	SPI2_MOSI	SPI2_NSS	-
PC13	-	-	-	-	-	-	TIM2_CH1 TIM2_ETR	-
PC14	-	-	-	-	-	-	TIM2_CH2	-
PC15	-	-	-	-	-	-	TIM2_CH3	-

Table 7. Alternate functions for port D

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	I2C1_SDA	TIM1_CH1N	UART1_TX	TIM1_CH2	SPI1_MOSI	SPI1_MOSI	-
PD2	-	I2C1_SCL	-	-	-	SPI1_NSS	SPI1_NSS	-
PD3	-	I2C1_SDA	-	-	-	SPI1_SCK	SPI1_MISO	-
PD4	SPI1_MISO	SPI1_MOSI	-	-	-	-	-	-
PD5	SPI1_MOSI	SPI1_MISO	-	-	-	-	-	-
PD6	-	TIM3_ETR	-	TIM1_CH3N	-	TIM1_CH1	TIM1_CH1N	-
PD7	-	-	-	-	-	TIM3_CH1	TIM17_CH1	-

4 Memory mapping

Memory mapping

Table 8. Memory mapping

Bus	Boundaryaddress	Size	Peripheral	Notes
Flash	0x0000 0000 -0x0000 FFFF	64 KB	Main flash memory, system memory, or SRAM, depends on the configuration of BOOT	
	0x0001 0000 -0x07FF FFFF	~ 128 MB	Reserved	
	0x0800 0000 -0x0800 FFFF	64 KB	Main Flash memory	
	0x0801 0000 -0x1FFD FFFF	~ 383 MB	Reserved	
	0x1FFE 0000 -0x1FFE 01FF	0.5 KB	Reserved	
	0x1FFE 0200 -0x1FFE 0FFF	3 KB	Reserved	
	0x1FFE 1000 -0x1FFE 1BFF	3 KB	Reserved	
	0x1FFE 1C00 -0x1FFF F3FF	~ 256 MB	Reserved	
	0x1FFF F400 -0x1FFF F7FF	1 KB	System memory	
	0x1FFF F800 -0x1FFF F80F	16 B	Option bytes	
	0x1FFF F810 -0x1FFF FFFF	~2 KB	Reserved	
SRAM	0x2000 0000 -0x2000 3FFF	16 KB	SRAM	
	0x2000 4000 -0x2FFF FFFF	~ 255 MB	Reserved	
APB1	0x4000 0000 -0x4000 03FF	1 KB	TIM2	
	0x4000 0400 -0x4000 07FF	1 KB	TIM3	
	0x4000 0800 -0x4000 0BFF	8 KB	Reserved	
	0x4000 2800 -0x4000 2BFF	1 KB	RTC/BKP	
	0x4000 2C00 -0x4000 2FFF	1 KB	WWDG	
	0x4000 3000 -0x4000 33FF	1 KB	IWDG	
	0x4000 3400 -0x4000 37FF	1 KB	Reserved	
	0x4000 3800 -0x4000 3BFF	1 KB	SPI2	
	0x4000 4000 -0x4000 43FF	1 KB	Reserved	
	0x4000 4400 -0x4000 47FF	1 KB	UART2	
	0x4000 4800 -0x4000 4BFF	3 KB	Reserved	
	0x4000 5400 -0x4000 57FF	1 KB	I2C1	
	0x4000 5800 -0x4000 6BFF	5 KB	Reserved	
	0x4000 6C00 -0x4000 6FFF	1 KB	Reserved	
	0x4000 7000 -0x4000 73FF	1 KB	PWR	

Bus	Boundaryaddress	Size	Peripheral	Notes
APB1	0x4000 7400 -0x4000 FFFF	35 KB	Reserved	
APB2	0x4001 0000 -0x4001 03FF	1 KB	SYSCFG	
	0x4001 0400 -0x4001 07FF	1 KB	EXTI	
	0x4001 0800 -0x4001 23FF	7 KB	Reserved	
	0x4001 2400 -0x4001 27FF	1 KB	ADC1	
	0x4001 2800 -0x4001 2BFF	1 KB	Reserved	
	0x4001 2C00 -0x4001 2FFF	1 KB	TIM1	
	0x4001 3000 -0x4001 33FF	1 KB	SPI1	
	0x4001 3400 -0x4001 37FF	1 KB	DBGMCU	
	0x4001 3800 -0x4001 3BFF	1 KB	UART1	
	0x4001 3C00 -0x4001 3FFF	1 KB	Reserved	
	0x4001 4000 -0x4001 43FF	1 KB	TIM14	
	0x4001 4400 -0x4001 47FF	1 KB	TIM16	
	0x4001 4800 -0x4001 4BFF	1 KB	TIM17	
	0x4001 4C00 -0x4001 7FFF	13 KB	Reserved	
AHB	0x4002 0000 -0x4002 03FF	1 KB	DMA	
	0x4002 0400 -0x4002 0FFF	3 KB	Reserved	
	0x4002 1000 -0x4002 13FF	1 KB	RCC	
	0x4002 1400 -0x4002 1FFF	3 KB	Reserved	
	0x4002 2000 -0x4002 23FF	1 KB	Flash Interface	
	0x4002 2400 -0x4002 2FFF	3 KB	Reserved	
	0x4002 3000 -0x4002 33FF	1 KB	CRC	
	0x4002 3400 -0x47FF FFFF	~ 127 MB	Reserved	
	0x4800 0000 -0x4800 03FF	1 KB	GPIOA	
	0x4800 0400 -0x4800 07FF	1 KB	GPIOB	
	0x4800 0800 -0x4800 0BFF	1 KB	GPIOC	
	0x4800 0C00 -0x4800 0FFF	1 KB	GPIOD	
	0x4800 1000 -0x5FFF FFFF	~ 384 MB	Reserved	

5 Electrical characteristics

Electrical characteristics

5.1 Test condition

All voltages are based on V_{SS} unless otherwise stated.

5.1.1 Minimum and maximum

Unless otherwise stated, the minimum and maximum performed at ambient temperature T_A = 25°C,V_{DD} = 3.3V.

5.1.2 Typical value

Unless otherwise stated, typical data is based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and have not been tested.

5.1.3 Typical Curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

5.1.4 Load Capacitor

The load conditions when measuring the pin parameters are shown in the figure below.

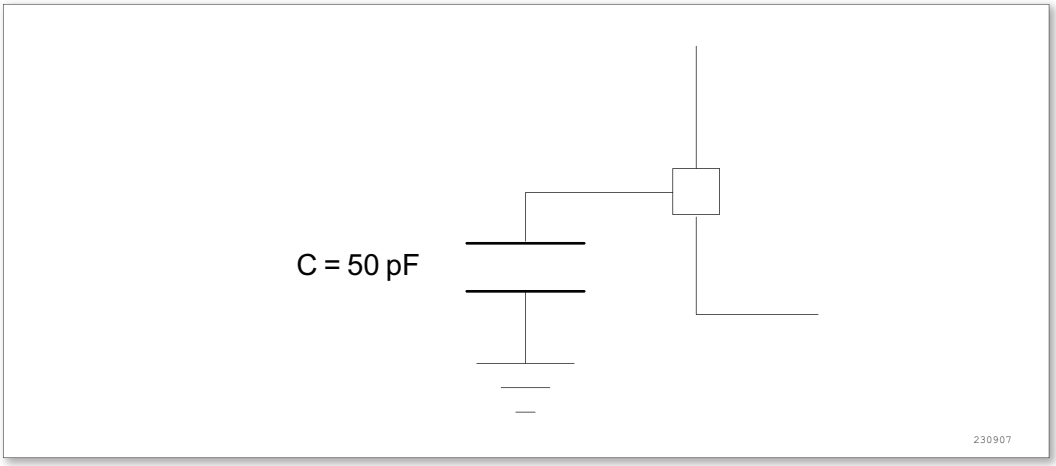

Figure 7. Load condition of the pin

5.1.5 Pin input voltage

The measurement of the input voltage on the pin is shown in the figure below.

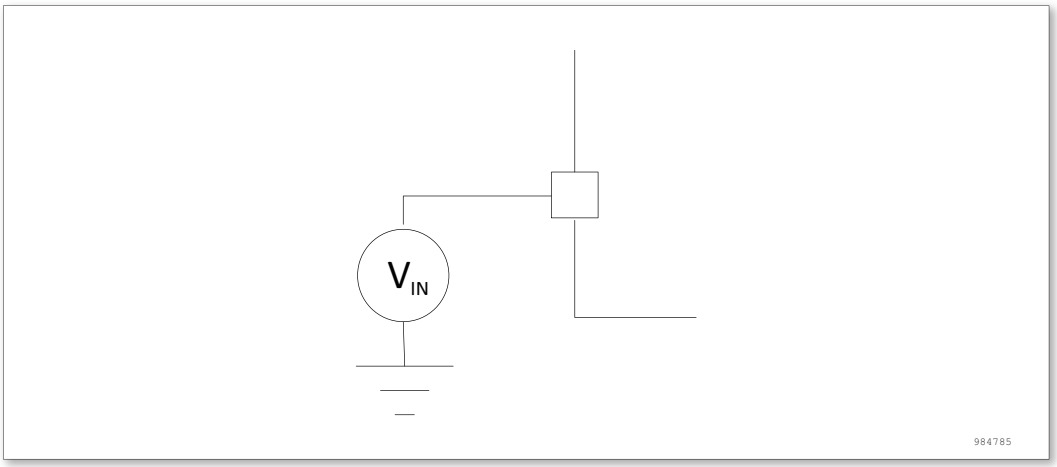

Figure 8. Pin input voltage

5.1.6 Power scheme

The power supply design scheme is shown in the figure below.

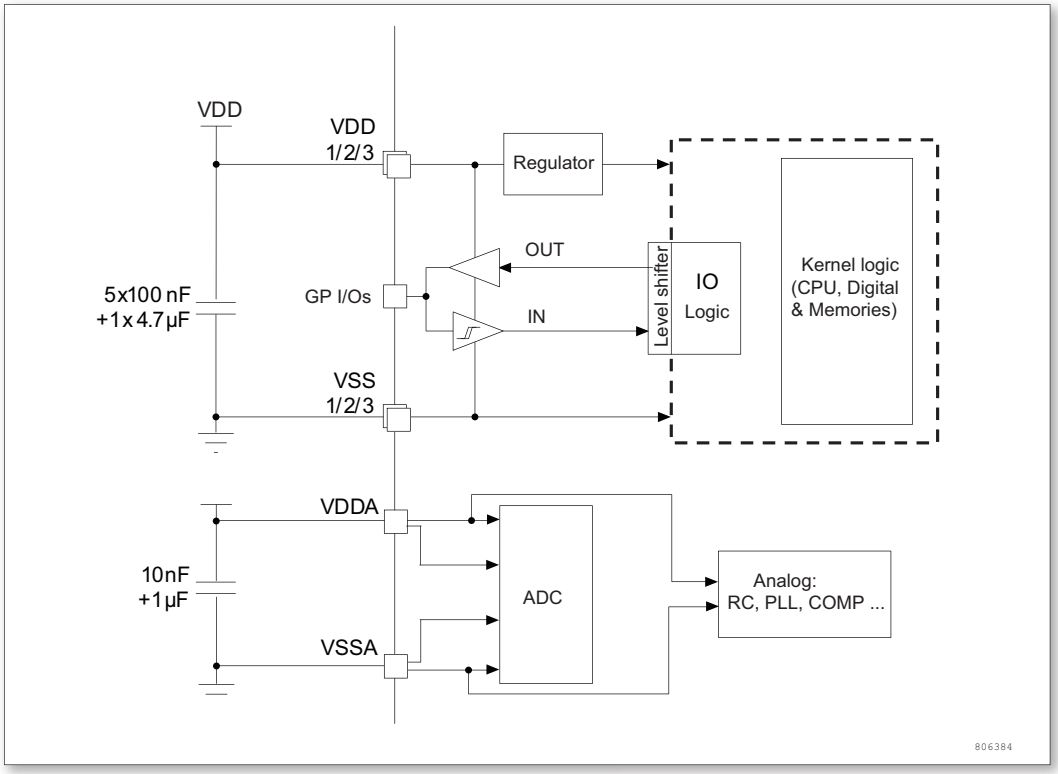

Figure 9. Power scheme

5.1.7 Current consumption measurement

The measurement of the current consumption on the pin is shown in the figure below.

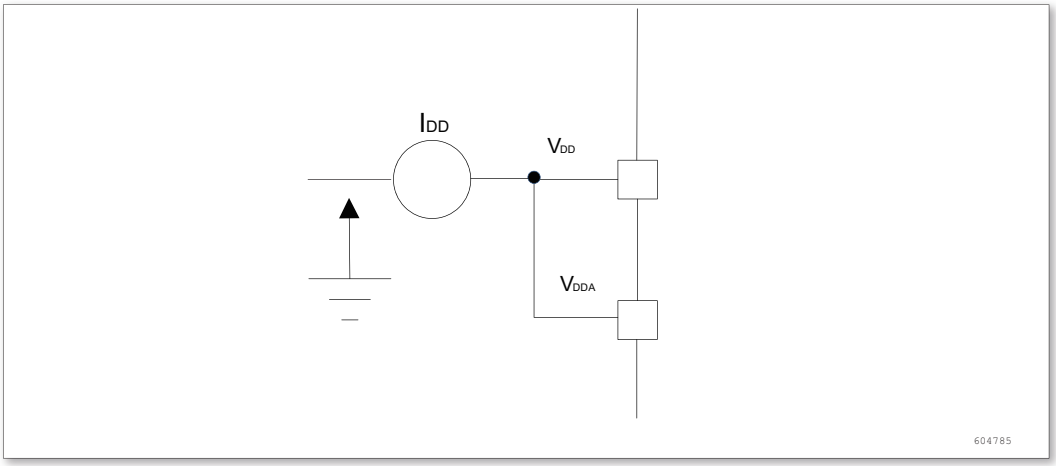

Figure 10. Current consumption measurement scheme

5.2 Absolute maximum rating

If the load applied to the device exceeds the value given in the ”Absolute Group Maximum Ratings” list (Table 9, Table 10, Table 11), it may result in the device is permanently damaged. This is just to give the maximum load that can be tolerated, and does not mean that the functional operation of the device is correct under these conditions. Long-term operation of the device under maximum conditions can affect device reliability.

Table 9. Voltage characteristics

Symbol	Description	min	max	units
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA} and V_{SS})(1)	2	5.5	V
V_{IN}	Input voltage on other pins (2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert \triangle V_{DDx} \rvert$	Voltage Difference Between Different Supply Pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage difference between different ground pins		50	

1. All power supplies (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) The foot must always be connected to the power supply system within the external allowable range.
2. must always follow the maximum value of V_{IN}. See the table below for information on the maximum allowable injection current values.

Table 10. Current characteristics

Symbol	Description	Maximum	Units
I_{VDD}	After V_{DD}/V_{DDA} total current of the power line (supply current) (1)	120	mA
I_{VSS}	Total current (outflow current) after V_{SS} ground line (1)	-120	

Symbol	Description	Maximum	Units
I_{IO}	Output sink current on any I/O and control pins ($0.9V_{DD}$)	20	
	Output current on any I/O and control pin ($0.1V_{DD}$)	-18	
$I_{INJ(PIN)}$ (2)(3)	HSE's OSC_IN pin and LSE's OSC_IN pin injection current	±5	mA
$I_{INJ(PIN)}$ (2)(3)	injection current for other pins (4)	±5	mA
$\Sigma I_{INJ(PIN)}$ (2)	Total injection current on all I/O and control pins (5)	±25	mA

1. Within the allowed range, all main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pin must always be connected to an external power supply.
2. This current consumption must be correctly distributed to all I/O and control pins. The total output current must not be sink/pull between the two consecutive power supply pins of the reference high pin count LQFP package. The
3. reverse injection current can interfere with the analog performance of the device.
4. When $V_{IN} > V_{DDA}$, a positive injection current is generated; when $V_{IN} < V_{SS}$, a reverse injection current is generated. Do not exceed $I_{INJ(PIN)}$.
5. When there is simultaneous injection current for multiple inputs, the maximum value of $\Sigma I_{INJ(PIN)}$ is equal to the sum of the absolute values of the forward injection current and the reverse injection current (instantaneous value) .

Table 11. Temperature characteristics

Symbol	Description	Maximum	Units
T_{STG}	Storage Temperature Range	- 55 ~ + 150	°C
T_J	maximum junction temperature	125	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 12. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PCLK1}	Internal APB1 clock frequency		0	f_{HCLK}	
f_{PCLK2}	Internal APB2 clock frequency		0	f_{HCLK}	
V_{DD}	Standard operating voltage		2.0	5.5	V

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA} (1)	Analog partial operating voltage (not use ADC)	Must be the same voltage as V_{DD}	2.0	5.5	V
	Analog partial operating voltage (use ADC)		2.5	5.5	
P	(Ambient temperature：T_A=85°C (2)(3))	Maximum power dissipation LQFP64	434		mW
		Maximum power dissipation LQFP48	355		
		Maximum power dissipation LQFP32	346		

1. It is recommended to use the same power supply for V_{DD} and V_{DDA}.
2. If T_A is low, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (See subsec 5.1).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (See subsec 5.1).
4. In the state of low power dissipation, as long as T_J does not exceed T_{Jmax} (see subsec 5.1), T_A can be extended to this range.
5. The chip reaches the junction temperature power consumption, and the normal operation must be lower than this power consumption.

5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are based on tests under normal operating conditions.

Table 13. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{VDD}rise time rate	T_A = 27°C	300	∞	μS/V
	V_{VDD}fall time rate		300	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are based on the ambient temperature and the V_{DD} supply voltage listed in Table 12.

Table 14. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=0000 (Rising edge)		1.8		V
		PLS[3：0]=0000 (Falling edge)		1.7		V
		PLS[3：0]=0001 (Rising edge)		2.1		V
		PLS[3：0]=0001 (Falling edge)		2.0		V
		PLS[3：0]=0010 (Rising edge)		2.4		V
		PLS[3：0]=0010 (Falling edge)		2.3		V
		PLS[3：0]=0011 (Rising edge)		2.7		V
		PLS[3：0]=0011 (Falling edge)		2.6		V
		PLS[3：0]=0100 (Rising edge)		3.0		V
		PLS[3：0]=0100 (Falling edge)		2.9		V
		PLS[3：0]=0101 (Rising edge)		3.3		V
		PLS[3：0]=0101 (Falling edge)		3.2		V
		PLS[3：0]=0110 (Rising edge)		3.6		V
		PLS[3：0]=0110 (Falling edge)		3.5		V
		PLS[3：0]=0111 (Rising edge)		3.9		V
		PLS[3：0]=0111 (Falling edge)		3.8		V
V_{PVD}	Level selection of programmable voltage detectors	PLS[3：0]=1000 (Rising edge)		4.2		V
		PLS[3：0]=1000 (Falling edge)		4.1		V
		PLS[3：0]=1001 (Rising edge)		4.5		V
		PLS[3：0]=1001 (Falling edge)		4.4		V
		PLS[3：0]=1010 (Rising edge)		4.8		V
		PLS[3：0]=1010 (Falling edge)		4.7		V
$V_{PVDhyst}$	PVD hysteresis			110		mV
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge		1.65		V
		Rising edge		1.75		V
V_{PDRhys} (2)	PDR hysteresis				mV	
$T_{RSTTEMPO}$	Reset duration			2		ms

Note: The reset duration is measured from power-on to the time when the user application code reads the first instruction.

5.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting period).
- The instruction prefetching function is on. When the peripherals are enabled：$f_{PCLK1} = f_{HCLK}$.

Note：The instruction prefetching function must be set before setting the clock and bus divider.

Table 15. Typical and maximum current consumption in stop and standby modes(2)

Symbol	Parameter	Conditions	Max(1)	Unit
			T_A=25°C	
I_{DD}	Supply current in Stop mode	Enter the stop mode after reset,V_{DD} = 3.3V	7	μA
	Supply current in Stop mode	Enter the stop mode after reset,V_{DD} = 3.3V	0.4	
		LSI and RTC on, V_{DD} = 3.3V	1.5	
		LSE and RTC on, V_{DD} = 3.3V	3.5	

1. Maximum values are tested at T_A = 25°C.
2. Data based on characterization results, not tested in production.The IO state is an analog input.

Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration, and are connected to a static level —- V_{DD} or V_{SS} (no load).
- All the peripherals are closed, unless otherwise specified.
- The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period, 48 ~ 72 MHz is 2 waiting period).
- The ambient temperature and V_{DD} supply voltage conditions are summarized in Table 12.
- The instruction prefetching function is on. When the peripherals are enabled：$f_{PCLK1} = f_{HCLK}$.

Note: The instruction prefetch function must be set before the clock is set and the bus is divided.

Table 16. Maximum current consumption in Run mode, code executing from flash memory

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in run mode	External clock(2)	72MHz	39.3	20.5	mA
			48MHz	28.1	15.5	
			36MHz	21.8	12.3	
			24MHz	15.3	8.9	
			8MHz	6.1	4.1	

1. All I/O pins are in input mode, static value (no load) on V_{DD} or V_{SS};
2. All peripherals are disabled, except when explicitly stated;
3. The FLASH access time is in accordance with the user manual configuration;
4. The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/1$,$f_{PCLK2} = f_{HCLK}/1$;
5. The external clock frequency is 8MHz, and when $f_{HCLK} > 8MHz$, the PLL is turned on.

Table 17. Maximum current consumption in sleep mode, code executing from flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(2)	72MHz	28.5	10.7	mA
			48MHz	19.9	7.9	
			36MHz	15.5	6.6	
			24MHz	11.2	5.2	
			8MHz	4.5	2.8	

1. All I/O pins are in input mode, static value (no load) on V_{DD} or V_{SS};
2. All peripherals are disabled, except when explicitly stated;
3. The FLASH access time is in accordance with the user manual configuration;
4. The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/1$,$f_{PCLK2} = f_{HCLK}/1$;
5. The external clock frequency is 8MHz, and when $f_{HCLK} > 8MHz$, the PLL is turned on.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 18. The MCU is placed under the following conditions:

- All I/O pins are in analog input mode, and are connected to a static level —- V_{DD} or V_{SS} (no load) .
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption.
  - With all peripherals clocked OFF
  - With only one peripheral clocked on

- Ambient operating temperature and supply voltage conditions V_{DD} summarized in Table 12.

Table 18. On-chip peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit	Peripheral		Typical consumption at 25 °C	Unit
AHB	DMA	3.1	mA/MHz	APB2	TIM16	0.75	mA/MHz
	GPIOD	0.53			TIM17	0.72	
	GPIOC	0.53			TIM14	0.72	
	GPIOB	0.53		APB1	TIM3	1.3	
	GPIOA	0.53			WWDG	0.16	
	CRC	0.31			SPI2	0.86	
APB2	ADC1	0.38			I2C1	1.68	
	TIM1	1.44			TIM2	1.6	
	SPI1	1.1			UART2	1.6	
	UART1	1.6			PWR	0.21	

1. f_{HCLK} = 72MHz，$f_{APB1} = f_{HCLK}$，$f_{APB2} = f_{HCLK}$, the prescale coefficient for each device is the default value.

5.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristic parameters given in the following table are measured using a high-speed external clock source, ambient temperature and power supply voltage meet the conditions of General operating conditions.

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		2	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$	OSC_IN rise time(1)				20	ns
$t_{f(HSE)}$	OSC_IN fall time(1)				20	ns
$C_{in(HSE)}$	OSC_IN input capacitance(1)				10	pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	μA

1. Guaranteed by design, not tested in production.

Low-speed external user clock characteristics

The characteristic parameters given in the following table are measured using a low-speed external clock source, ambient temperature and power supply voltage meet the conditions of General operating conditions.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)		16	32.768	1000	KHz
V_{LSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	V
$t_{w(LSE)}$	OSC_IN high or low time(1)		450			ns
$t_{r(LSE)}$	OSC_IN rise time(1)				50	ns
$t_{f(LSE)}$	OSC_IN fall time(1)				50	ns
$C_{in(LSE)}$	OSC_IN input capacitance(1)				10	pF
$DuCy_{(LSE)}$	Duty cycle			50		%
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-1		1	μA

1. Guaranteed by design, not tested in production.

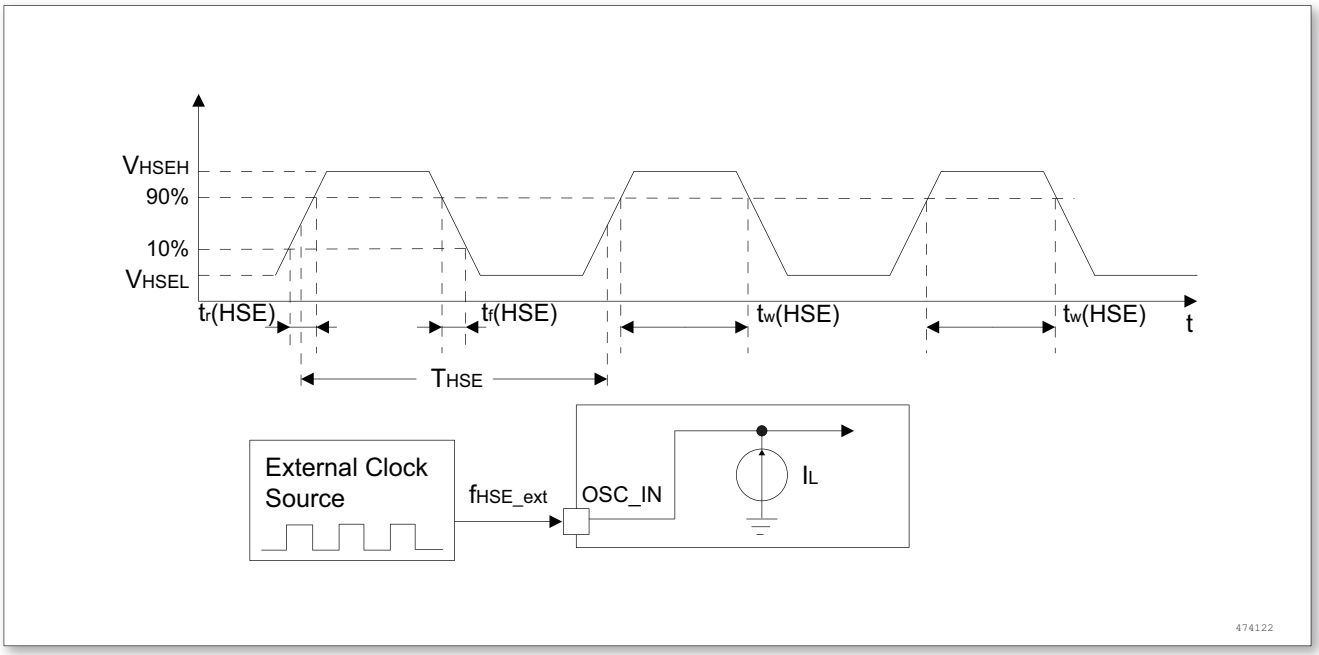

Figure 11. High-speed external clock source AC timing diagram

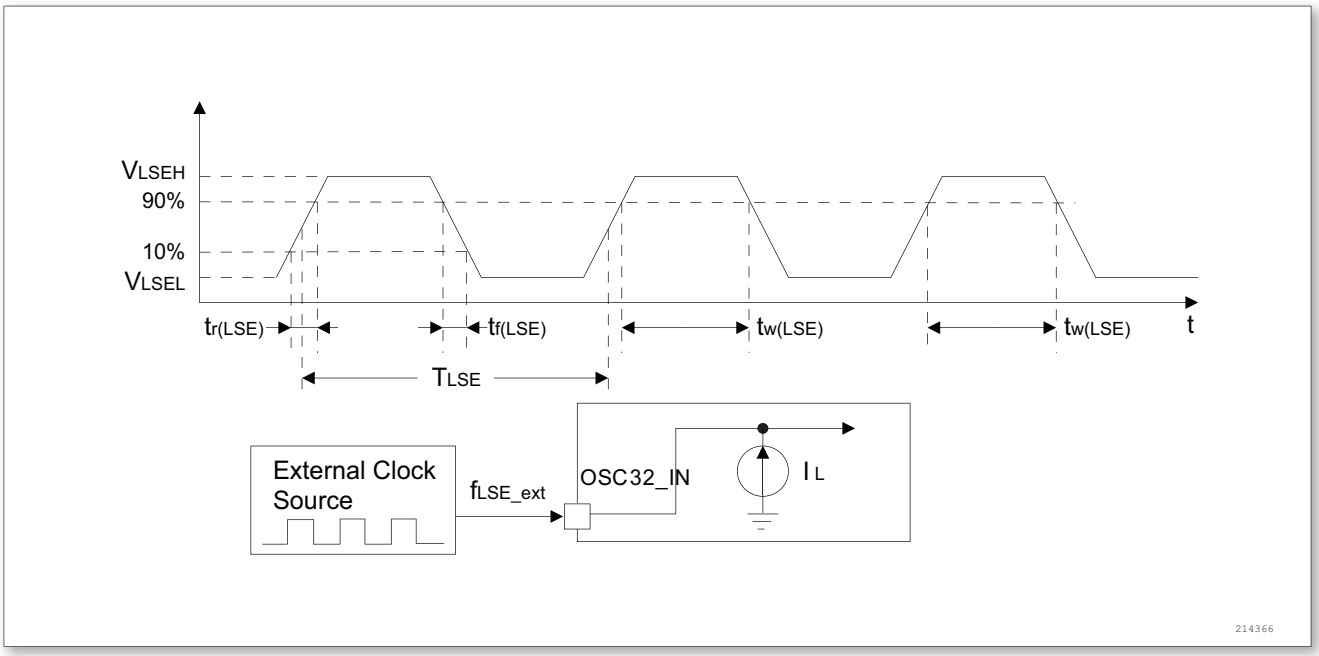

Figure 12. Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with an 2 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy...).

Table 21. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		2	8	24	MHz
R_F	Feedback resistor	R_S = 30Ω		200		kΩ
I_{dd}	HSE current consumption	Startup			8.5	mA
I_{dd}	HSE current consumption	V_{DD} = 3.3V R_m = 45Ω CL = 10pF@8MHZ		0.5		mA
I_{dd}	HSE current consumption	V_{DD} = 3.3V R_m = 30Ω CL = 20pF@8MHZ		1.5		mA
g_m	Oscillator transconductance	Startup	10			mA/V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(HSE)}$ (3)	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer characteristics Parameter.
2. Guaranteed by design, not tested in production.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

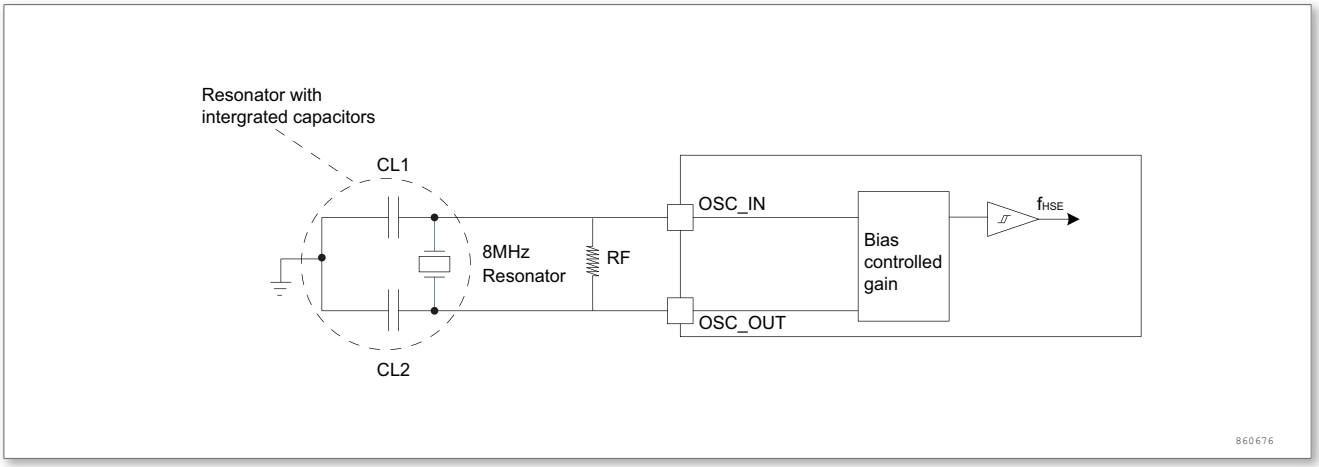

Figure 13. Typical application with an 8 MHz crystal

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy). Note: For C_{L1} and C_{L2}, it is recommended to use a high quality ceramic capacitor between 5pF and 15pF and select the crystal or resonator that meets the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers typically give the parameters of the load capacitance in a serial combination of C_{L1} and C_{L2}. The load capacitance C_L is calculated by: $C_L = C_{L1} \times C_{L2}/(C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the capacitance associated with the PCB or PCB. Its typical value is between 2pF and 7pF. WARNING: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15pF) , it is highly recommended to use a resonator with a load capacitance of $C_L \leq 7$pF. A resonator with a load capacitance of 12.5pF cannot be used. For example, if a resonator with a load capacitance of $C_L = 6$pF is selected and $C_{stray} = 2$pF, then $C_{L1} = C_{L2} = 8$pF.

Table 22. LSI oscillator characteristics (f_{LSE}=32.768KHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
g_m	Oscillator transconductance			5		μA/V
$t_{SU(HSE)}$ (2)	Startup time	R_S = 30kΩ		3		S

1. Guaranteed by design, not tested in production.
2. $t_{SU(HSE)}$ is the start-up time, which is measured from the time the software enables HSE until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator, which may vary greatly depending on the crystal manufacturer.

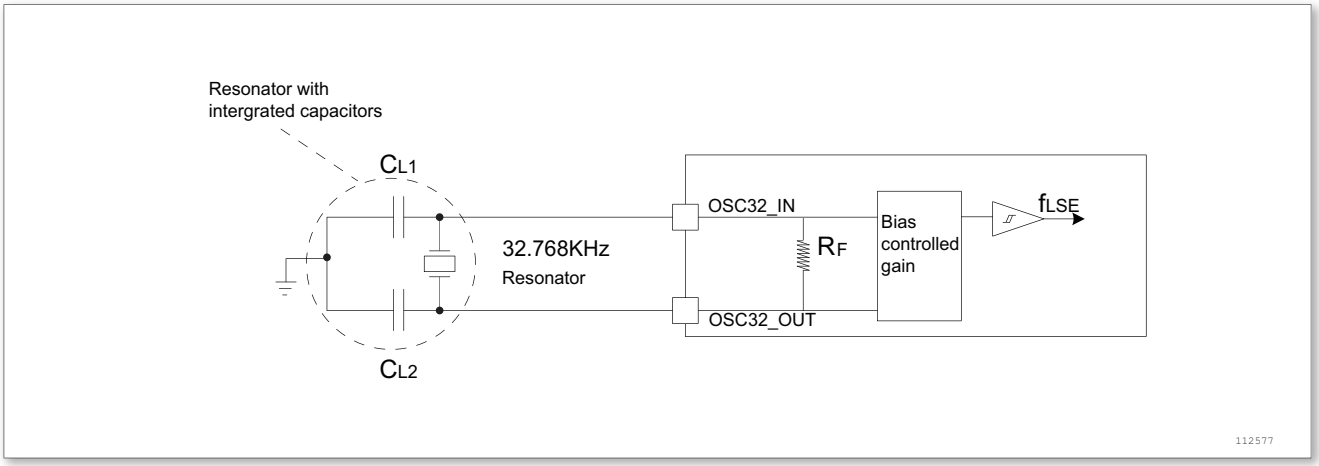

Figure 14. Typical application with a 32.768 kHz crystal

5.3.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal (HSI) oscillator

Table 23. HSI oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			48		MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40°C~ 105°C	-3		3	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -10°C~ 85°C	-2		2	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 0°C~ 70°C	-1.5		1.5	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = 25	-1		1	%
$t_{SU(HSI)}$	HSI oscillator startup time				15	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			300		μA

1. V_{DD} = 3.3V, T_A = - 40°C ~ 105°C, unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) oscillator

Table 24. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency			40		KHz
$t_{SU(LSI)}$(2)	LSI oscillator startup time				100	μs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption			1	2	μA

1. V_{DD} = 3.3V, T_A = -40°C ~ 105°C, Unless otherwise stated
2. Comprehensive assessment, not tested in production.
3. Guaranteed by design, not tested in production.

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

- Stop or Standby mode: The clock source is the oscillator
- Sleep mode: The clock source is the clock used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Max	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	HSI clock wakeup	4.5	μs
t_{WUSTOP}(1)	Wakeup from Stop mode	HSI clock wakeup < 2μS	8.3	μs
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI clock wakeup < 2μS The regulator wakes up from the off mode < 30μS	490	μs

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

5.3.7 PLL characteristics

The parameters listed in the table below are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 26. PLL characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	2		24	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	40		200	MHz
t_{LOCK}	PLL lock time			100	μS

1. Guaranteed by design, not tested in production.
2. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.8 Memory characteristics

Flash memory

The characteristics are given at T_A = - 40°C ~ 105°Cunless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	8-bit programming time			6	7.5	μS
t_{ERASE}	Page (512K bytes) erase time			4	5	mS
t_{ME}	Mass erase time			30	40	mS
I_{DD}	Supply current	Read mode		9		mA
		Write mode			7	mA
		Erase mode			2	mA
V_{prog}	Programming voltage			1.5		V

Table 28. Flash memory endurance and data retention(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance (Annotation: Erase number of times)		20			K cycle
t_{RET}	Data retention	T_A = 105°C	20			Year
		T_A = 25°C	100			

1. Guaranteed by design, not tested in production.
2. Cycle tests are carried out in the whole temperature range.

5.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) , the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB：A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table. They are based on the EMS levels and classes defined in application note.

Table 29. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transientvoltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pinsto induce a functional disturbance	V_{DD} = 3.3V,T_A=+25°C, f_{HCLK}=72MHz.Conformingto IEC 1000-4-4	2A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

5.3.10 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78A IC latch-up standard.

Table 30. ESD characteristics

Symbol	Parameter	Conditions	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25°C, Conforming to JESD22-A114	8000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = +25°C, Conforming to JESD22-C101	500	
I_{LU}	Latch-up current	T_A = +25°C, Conforming to JESD78A	100	mA

5.3.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 9 are derived from tests.

Table 31. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage	V_{DD} = 5V	0.7V_{DD}		V_{DD}+0.3	V
		V_{DD} = 3.3V	2		V_{DD}+0.3	V
V_{IH}	High level input voltage	V_{DD} = 2.0V	0.65V_{DD}		V_{DD}+0.3	V
V_{IL}	Low level input voltage	V_{DD} = 5V	0		0.3V_{DD}	V
		V_{DD} = 3.3V	0		0.8	V
		V_{DD} = 2.0V	0		0.35V_{DD}	V
V_{OH}	High level output voltage	V_{DD} = 5V	V_{DD}-0.8			V
		V_{DD} = 3.3V	2.4			V
		V_{DD} = 2.0V	V_{DD}-0.45			V
V_{OL}	Low level output voltage	V_{DD} = 5V			0.5	V
		V_{DD} = 3.3V			0.4	V
		V_{DD} = 2.0V			0.45	V
V_{hys}	Schmitt trigger hysteresis(1)		0.1V_{DD}			V
I_{lkg}	Input leakage current(2)				±1	μA
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN}=V_{SS}	22		50	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	V_{IN}=V_{DD}	20		100	kΩ
C_{IO}	I/O pin capacitance				10	pF

1. Schmitt Trigger switching hysteresis voltage level.Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (10% order).

All I/Os are CMOS (no software configuration required). Their characteristics cover more than the strict CMOS-technology.

- For V_{IH}:
  - If V_{DD} is between [2.50V~ 3.08V]; use CMOS features.
  - If V_{DD} is between [3.08V~ 3.60V]; include CMOS.
- For V_{IL}:
  - Use CMOS features.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

n the user application, the number of I/O pins which can drive current must be limited to

respect the absolute maximum rating specified in 5.2：

- The sum of the currents obtained from V_{DD} for all I/O ports, plus the maximum operating current that the MCU obtains on V_{DD}, cannot exceed the absolute maximum rating I_{VDD}.
- The sum of the currents drawn by all I/O ports and flowing out of V_{SS}, plus the maximum operating current of the MCU flowing out on V_{SS}, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Table 32. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output high level voltage	V_{DD} = 5V	V_{DD}-0.8		V
V_{OL}	Output low level voltage	V_{DD} = 5V		0.5	V
V_{OH}	Output high level voltage	V_{DD} = 3.3V	2.4		V
V_{OL}	Output low level voltage	V_{DD} = 3.3V		0.4	V
V_{OH}	Output high level voltage	V_{DD} = 2.0V	V_{DD}-0.45		V
V_{OL}	Output low level voltage	V_{DD} = 2.0V		0.45	V

1. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure 15 and Table 33, respectively.

Unless otherwise stated, the parameters listed in Table 33 are measured using the ambient temperature and supply voltage in accordance with the condition Table 9.

Table 33. I/O AC characteristics(1)(3)

OSPEEDRy [1:0] value	Symbol	Parameter	Conditions	Min	Max	Unit
01	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		44	nS
01	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		44	nS
10	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		24	nS
10	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		24	nS
11	$t_{f(IO)out}$	Output fall time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		24	nS
11	$t_{r(IO)out}$	Output rise time	C_L = 50pF, V_{DD} = 2V ~ 5.5V		24	nS

OSPEEDRy [1:0] value	Symbol	Parameter	Conditions	Min	Max	Unit
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		nS

1. The speed of the I/O port can be configured via MODEx[1:0]. See the description of the GPIO Port Configuration Register in this chip reference manual.
2. Guaranteed by design, not tested in production.

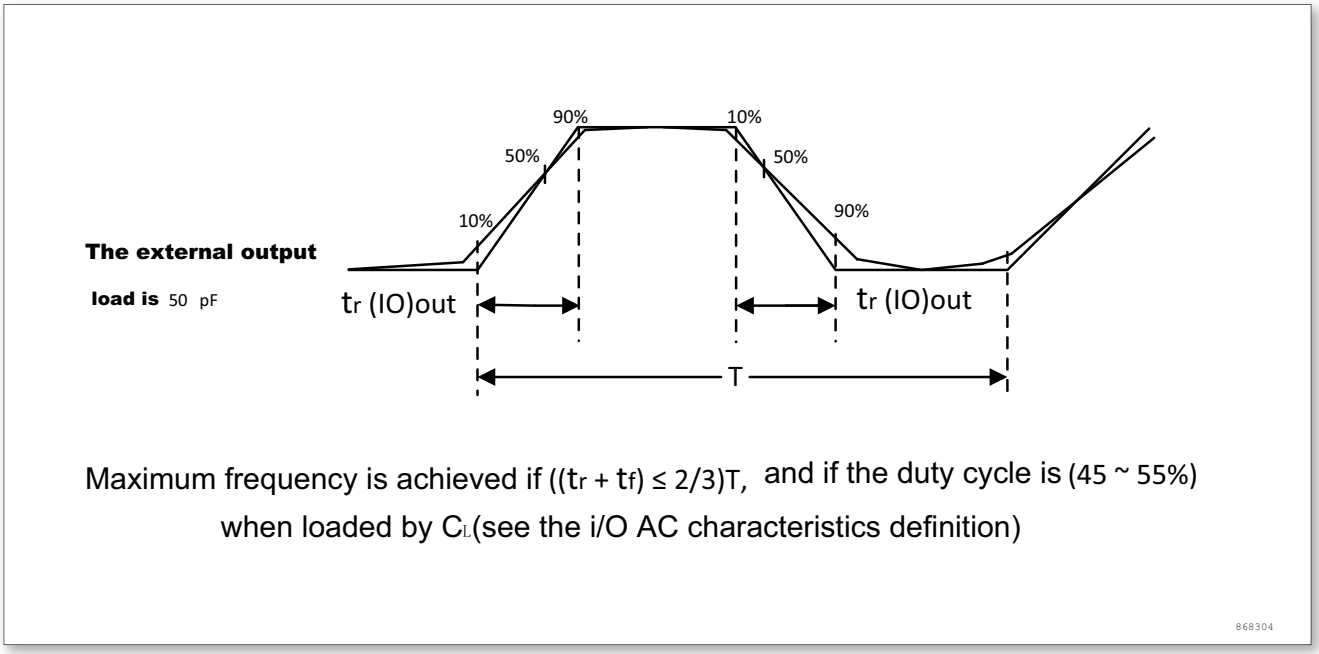

Figure 15. I/O AC characteristics

5.3.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, R_{PU}.

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and V_{DD} supply voltage in accordance with the condition of Table 12.

Table 34. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST input low level voltage		0		0.8	V
$V_{IH(NRST)}$ (1)	NRST input high level voltage		2		5.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			$0.1V_{DD}$		V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	22	50		kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse				3000	ns
$V_{NF(NRST)}$ (1)	NRST input not filtered pulse		4000			ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (10% order).

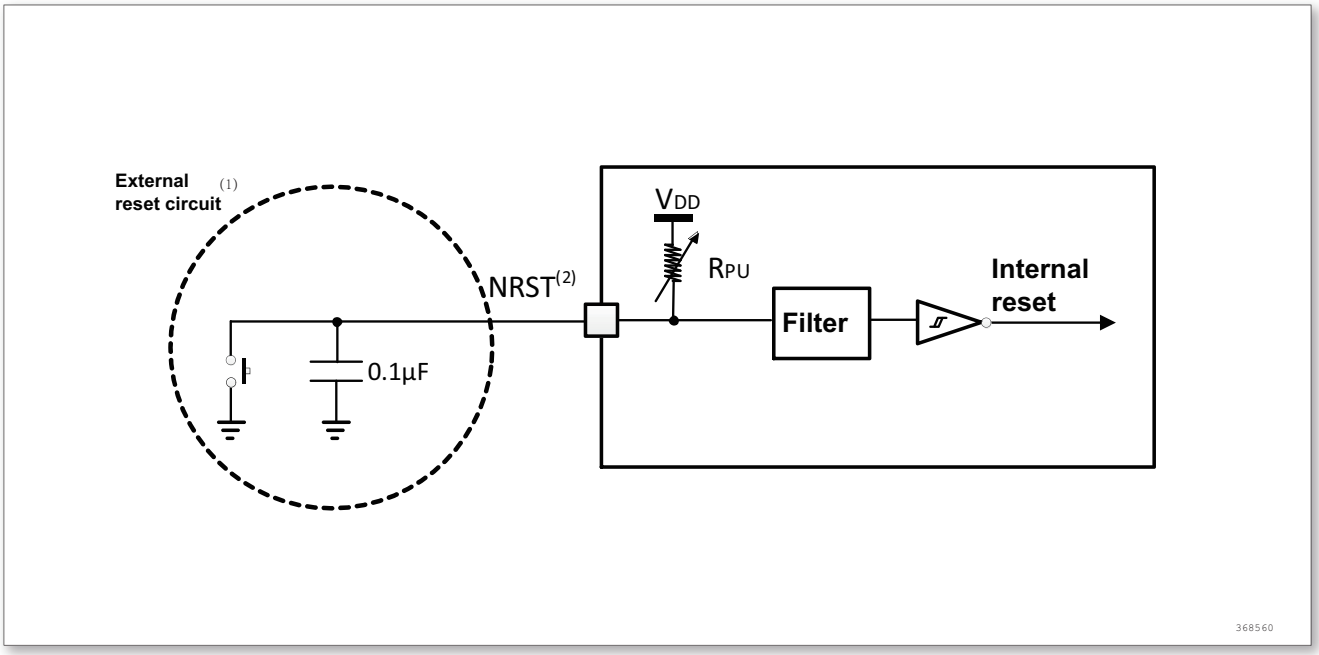

Figure 16. Recommended NRST pin protection

1. The reset network is to prevent parasitic reset
2. The user must ensure that the potential of the NRST pin is below the maximum $V_{IL(NRST)}$ listed in Table 34, otherwise the MCU cannot be reset.

5.3.13 Timer characteristics

The parameters given in the following tables are guaranteed by design.

For details on the characteristics of the I/O multiplexing function pins (output compare, input capture, external clock, PWM output) , see subsubsec 5.3.11.

Table 35. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 72MHz	10.4		nS

Symbol	Parameter	Conditions	Min	Max	Unit
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$	MHz
		$f_{TIMxCLK}$ = 72MHz	0	72	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16-bit timer maximum period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$72MHz	0.0104	682	μS
t_{MAX_COUNT}	The maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$72MHz		44.7	S

1. TIMx is a generic name, representing TIM4.

5.3.14 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table 36 are derived from tests performed under the ambient temperature, f_{PCLK1}frequency and supply voltage conditions summarized in Table 12: General operating conditions.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and V_{DD} Was closed but still exists.

The I2C I/Os characteristics are listed in Table 36, the alternate function characteristics of I/Os (SDA and SCL) refer to subsubsec 5.3.11.

Table 36. I2C characteristics

Symbol	Parameter	Standard I2C(1)		Fast I2C (1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock fall time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock rise time	4.0		0.6		μs
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SDL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SDL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from Stop condition to Start condition	4.7		1.3		
C_b	Capacitive load of each bus		400		400	pF

1. Guaranteed by design, not tested in production.

2. f_{PCLK1} must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. In order to span the undefined area of the falling edge of SCL, it must ensure that the SDA signal has a hold time of at least 300nS.

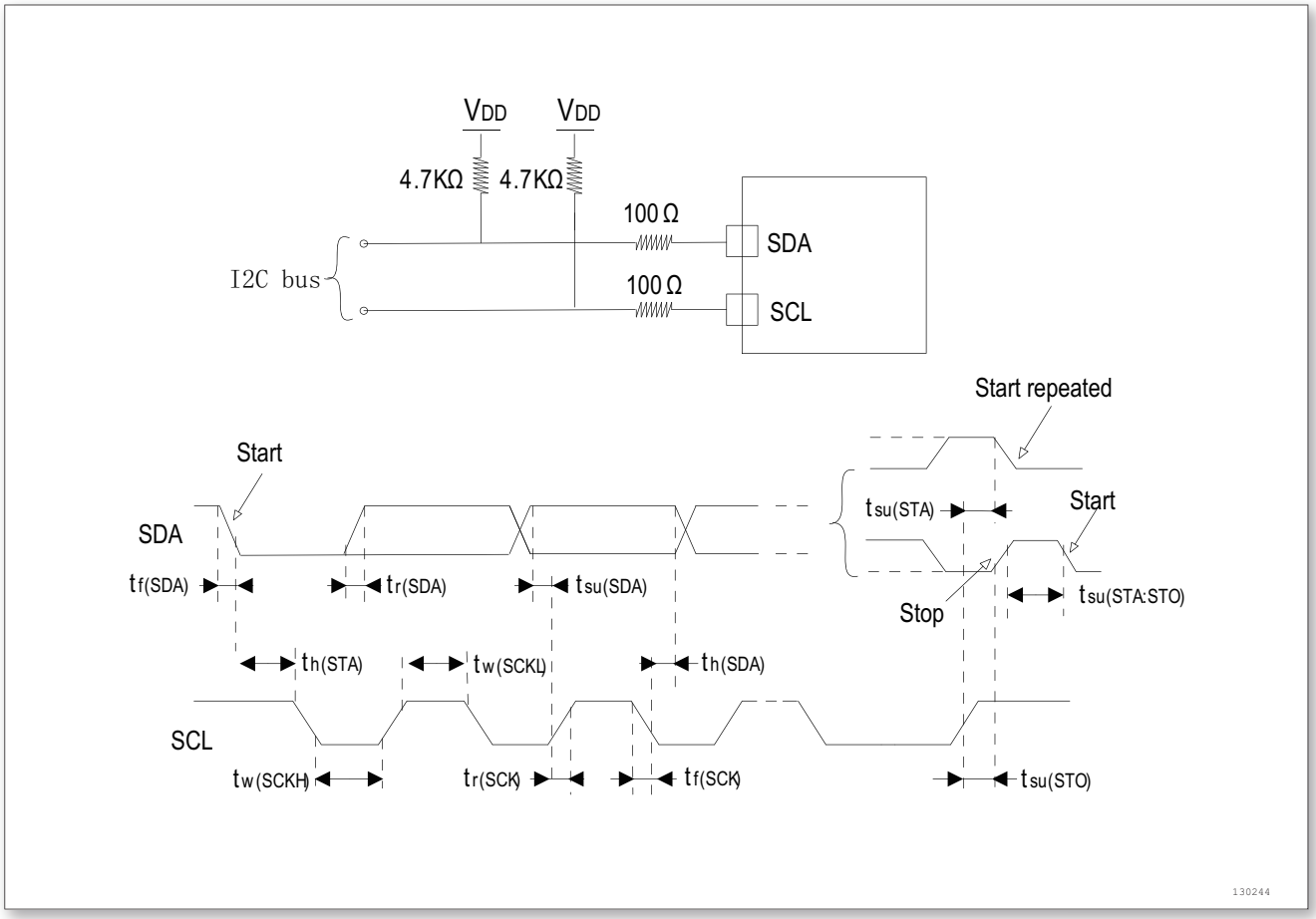

Figure 17. I2C bus AC waveform and measurement circuit(1)

1. Measurement point is set to the CMOS level：$0.3V_{DD}$ and $0.7V_{DD}$.

SPI characteristics

Unless otherwise specified, the parameters given in Table 37 are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table 12.

Refer to subsubsec 5.3.11 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 37. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		8	ns
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4t_{PCLK}$		ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	73		ns
$t_{w(SCKH)}$ (2) $t_{w(SCKL)}$ (2)	SCK high and low time	Master mode，f_{PCLK} = 36MHz，prescale coefficient = 4	50	60	ns
$t_{su(SI)}$ (2)	Data input setup time, Slave mode		1		ns
$t_{h(SI)}$ (2)	Data input hold time, Slave mode		3		ns
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode，f_{PCLK} = 36MHz，prescale coefficient = 4	0	55	ns
		Slave mode，f_{PCLK} = 24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$ (2)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$ (2)		Master mode (after enable edge)	4		

1. Data based on characterization results. Not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

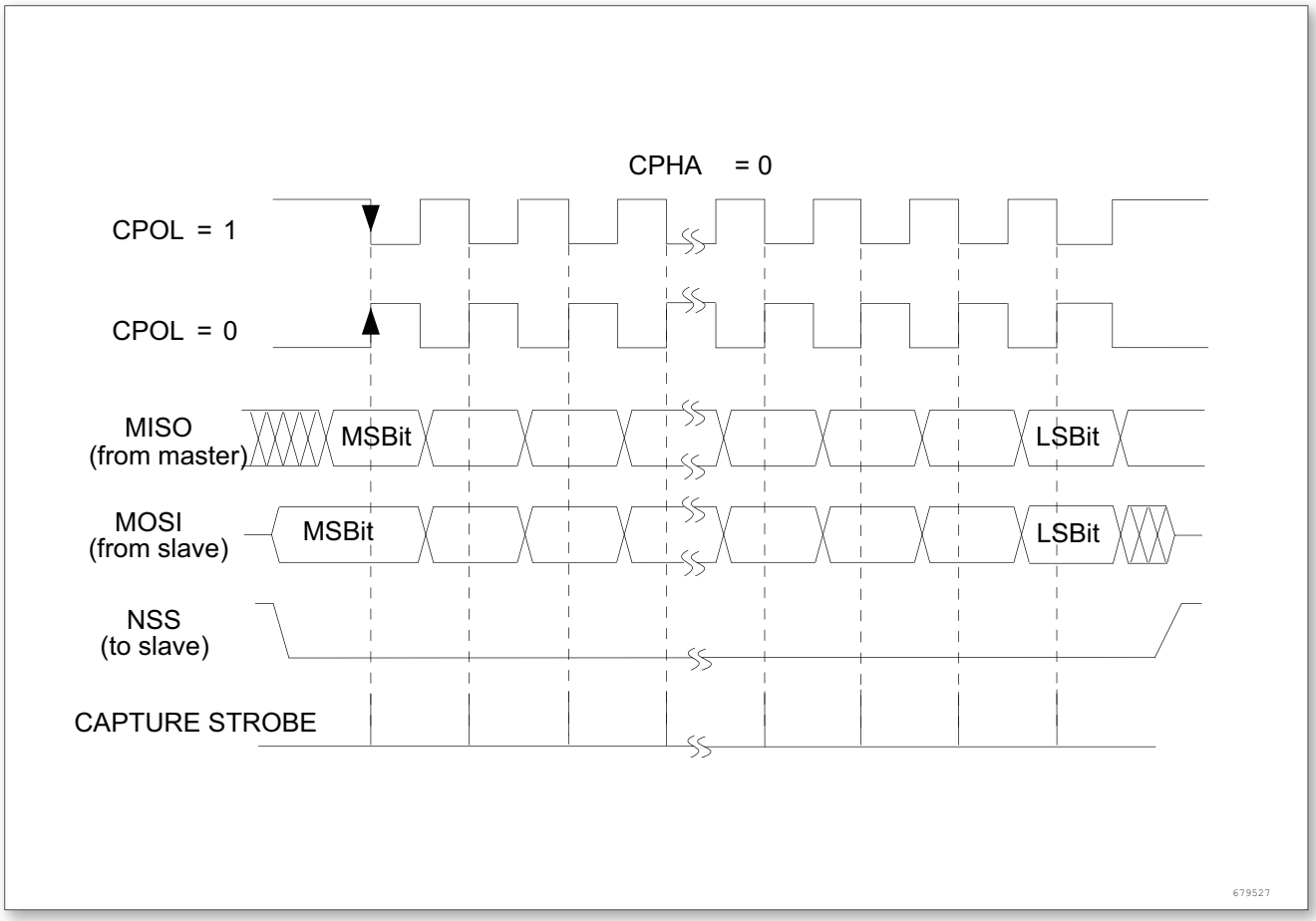

Figure 18. SPI timing diagram-slave mode and CPHA = 0

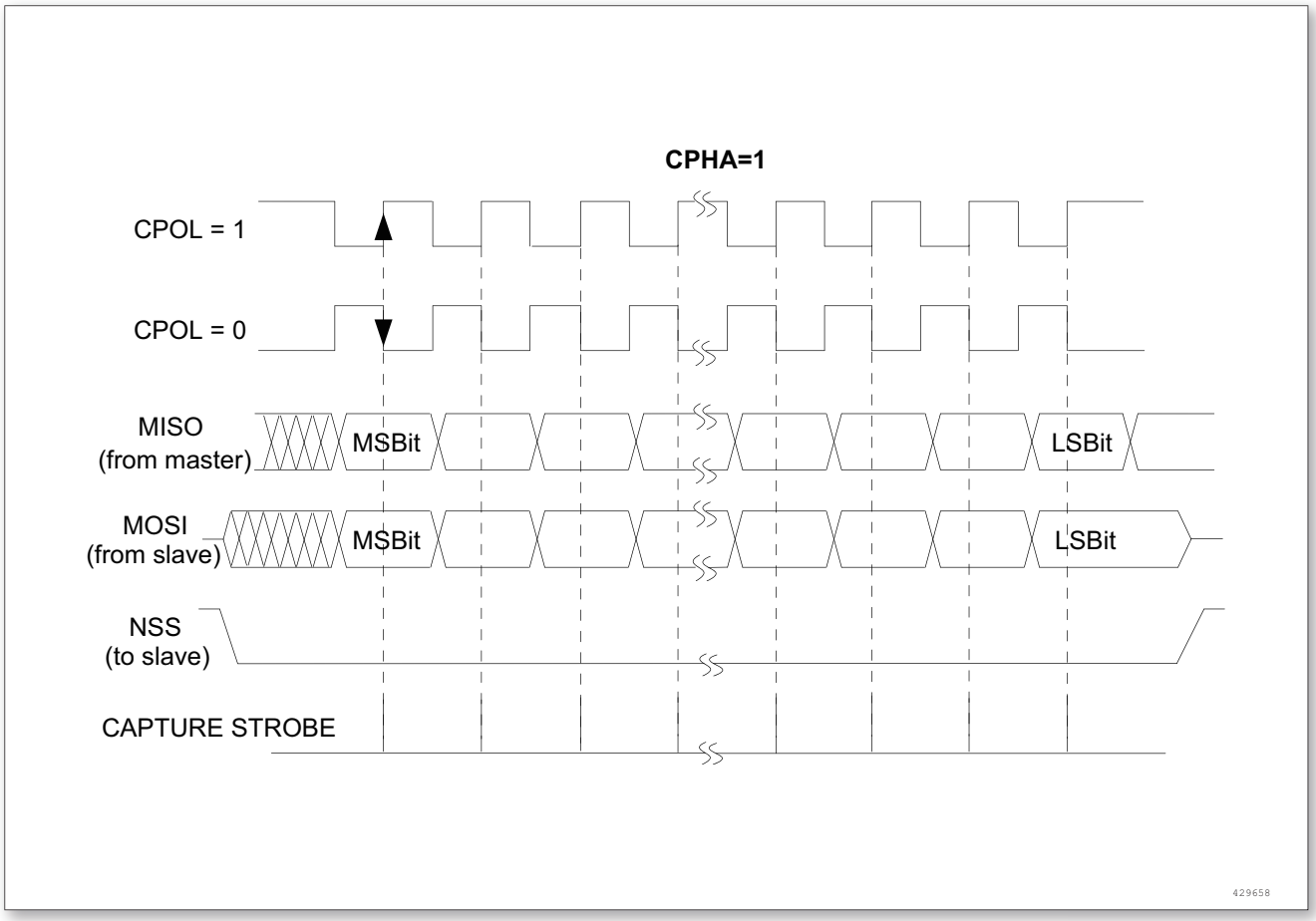

Figure 19. SPI timing diagram-slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

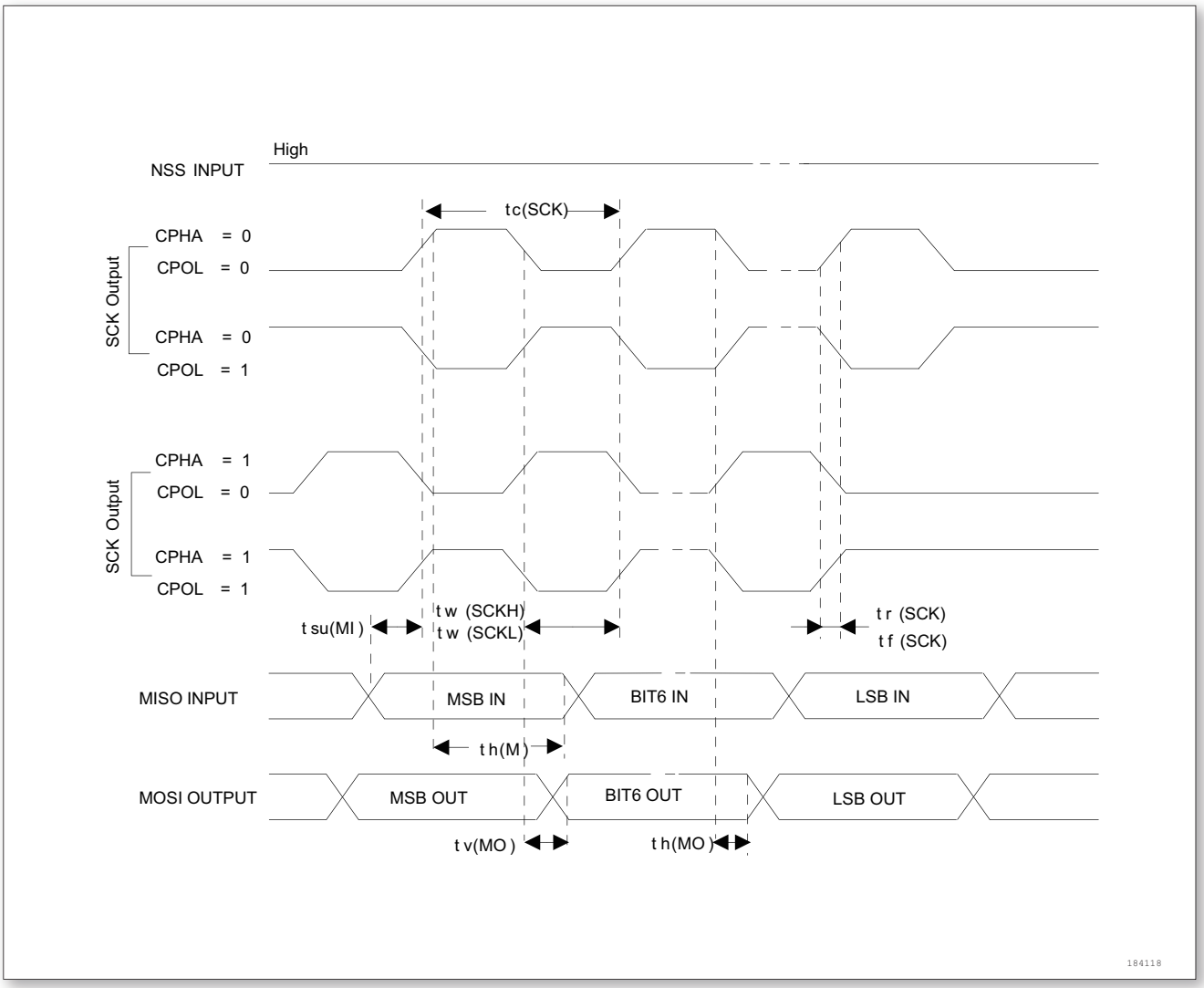

Figure 20. SPI timing diagram-master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

5.3.15 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage in accordance with the conditions of Table 12.

Note: It is recommended to perform a calibration after each power-up

Table 38. ADC characteristics

Symbol	Parameter	Conditions	Min	Type	Max	Unit

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. In this series of products, V_{REF+} is internally connected to $_{DDA}$, V_{REF-} is internally connected to $_{SSA}$.

Table 39. Maximum R_{AIN} at f_{ADC} = 15MHz(1)

T_S (cycles)	t_S (μs)	R_{AIN} max (kΩ)

1. Guaranteed by design. Not tested in production.

Table 40. ADC Accuracy - Limit Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Type	Max	Unit

1. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in subsubsec 5.3.12 does not affect the ADC accuracy.
2. Guaranteed based on test during characterization. Not tested in production.

ET = Total unadjusted error: The maximum deviation between the actual and ideal transmission curves.

EO = Offset error: The deviation between the first actual conversion and the first ideal conversion.

EG = Gain error: The deviation between the last ideal transition and the last actual transition.

ED = Differential linearity error: The maximum deviation between the actual step and the ideal value.

EL = Integral linearity error: The maximum deviation between any actual conversion and the associated line of the endpoint.

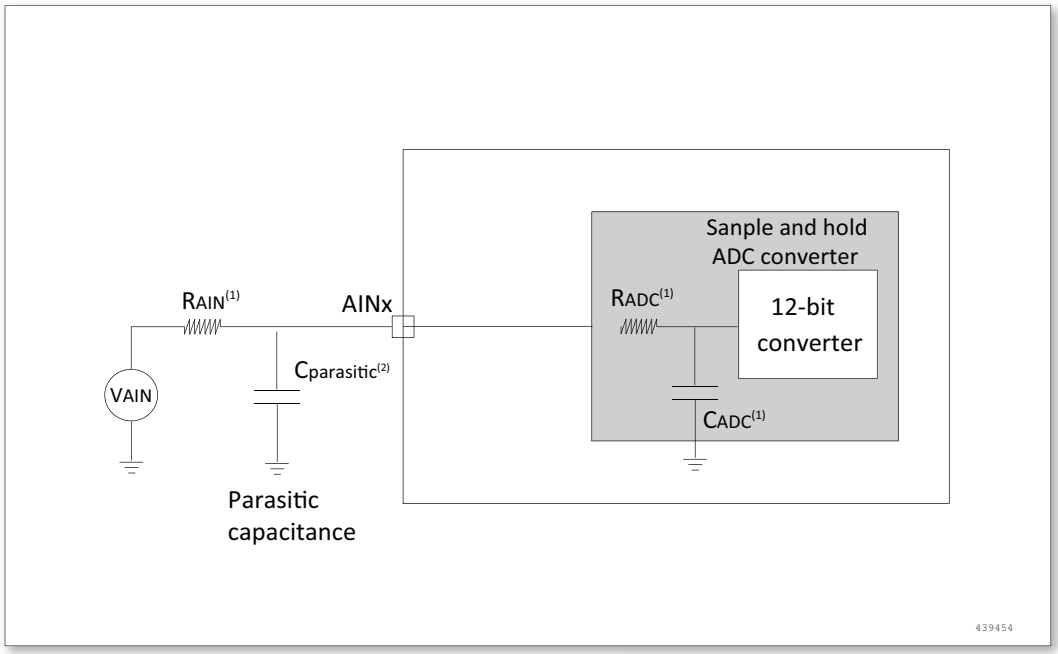

Figure 21. Typical connection diagram using the ADC

1. See Table 40 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF) . A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

PCB design recommendations

The power supply must be connected as shown below. The 10nFcapacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

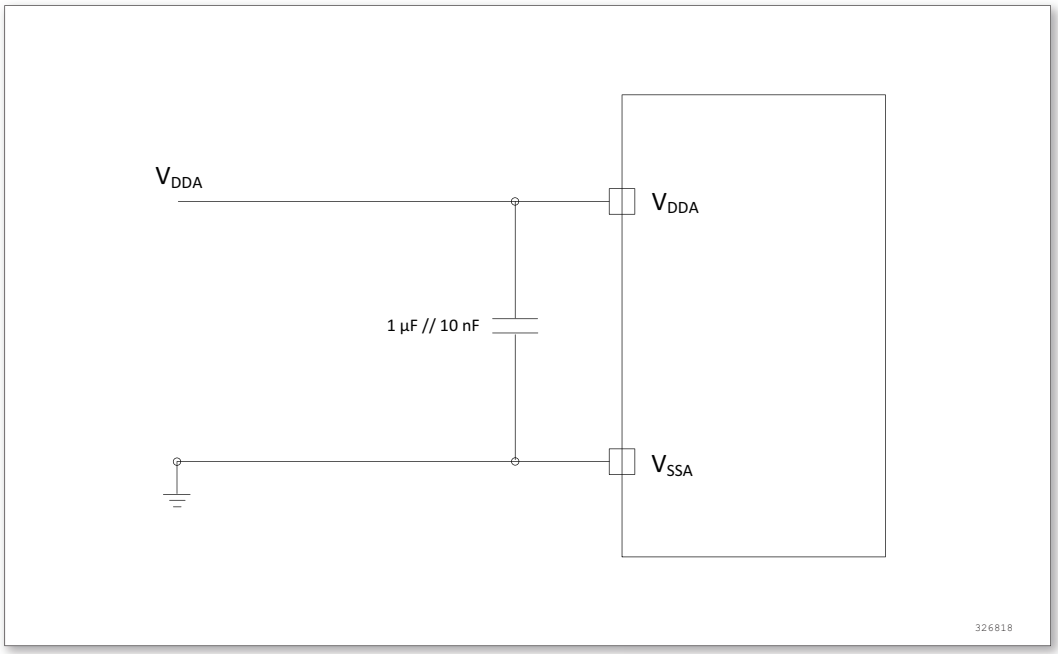

Figure 22. Power supply and reference power supply decoupling circuit

5.3.16 Temperature sensor characteristics

Table 41. Temperature sensor characteristics(3)(4)

Symbol	Parameter	Min	Type	Max	Unit
T_L(1)	V_{SENSE} linearity with respect to temperature		±5		°C
Avg_Slope(1)	Average slope	4.571	4.801	5.984	mV/°C
V_{25}(1)	Voltage at 25°C	1.433	1.451	1.467	V
t_{start}(2)	Setup time			10	µs
T_{S_temp}(2)	ADC sampling time when reading temperature	10			µs

1. Guaranteed based on test during characterization. Not tested in production.
2. Guaranteed by design. Not tested in production.
3. The shortest Sampling time can be determined by the application through multiple iterations.
4. V_{DD} = 3.3V.

6 Package information

Package information

6.1 LQFP64 Package information

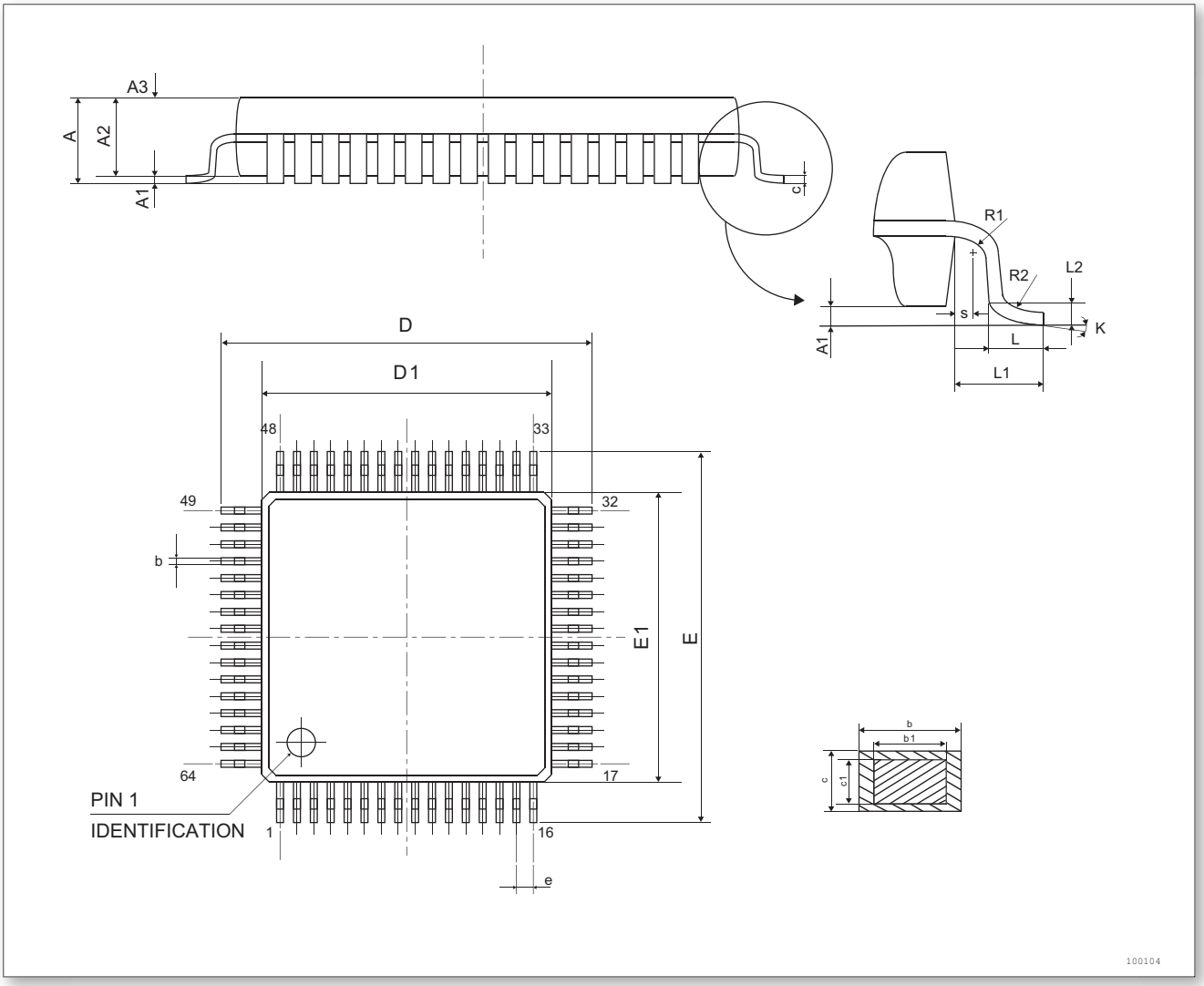

Figure 23. LQFP64 - 64-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 42. LQFP64 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18		0.27
b1	0.17	0.20	0.23
c	0.13		0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e		0.50	
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08		
R2	0.08		0.20
S	0.20		
N	Number of pins = 64		

6.2 LQFP48 Package information

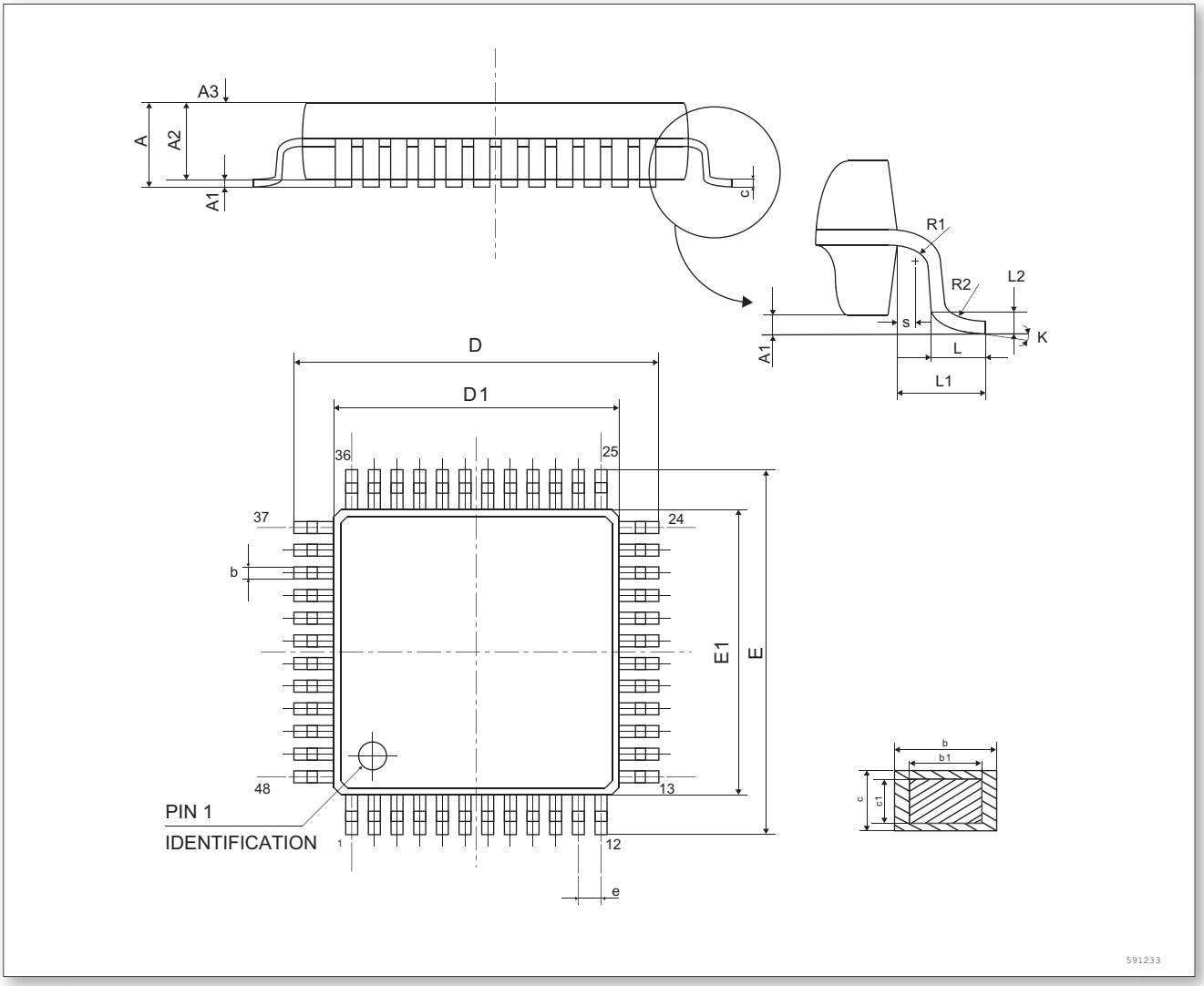

Figure 24. LQFP48 - 48-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 43. LQFP48 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18		0.27
b1	0.17	0.20	0.23
c	0.13		0.18
c1	0.12	0.127	0.134

Symbol	Millimeters		
	Min	Typ	Max
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50	
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08		
R2	0.08		0.20
S	0.20		
N	Number of pins = 48		

6.3 LQFP32 Package information

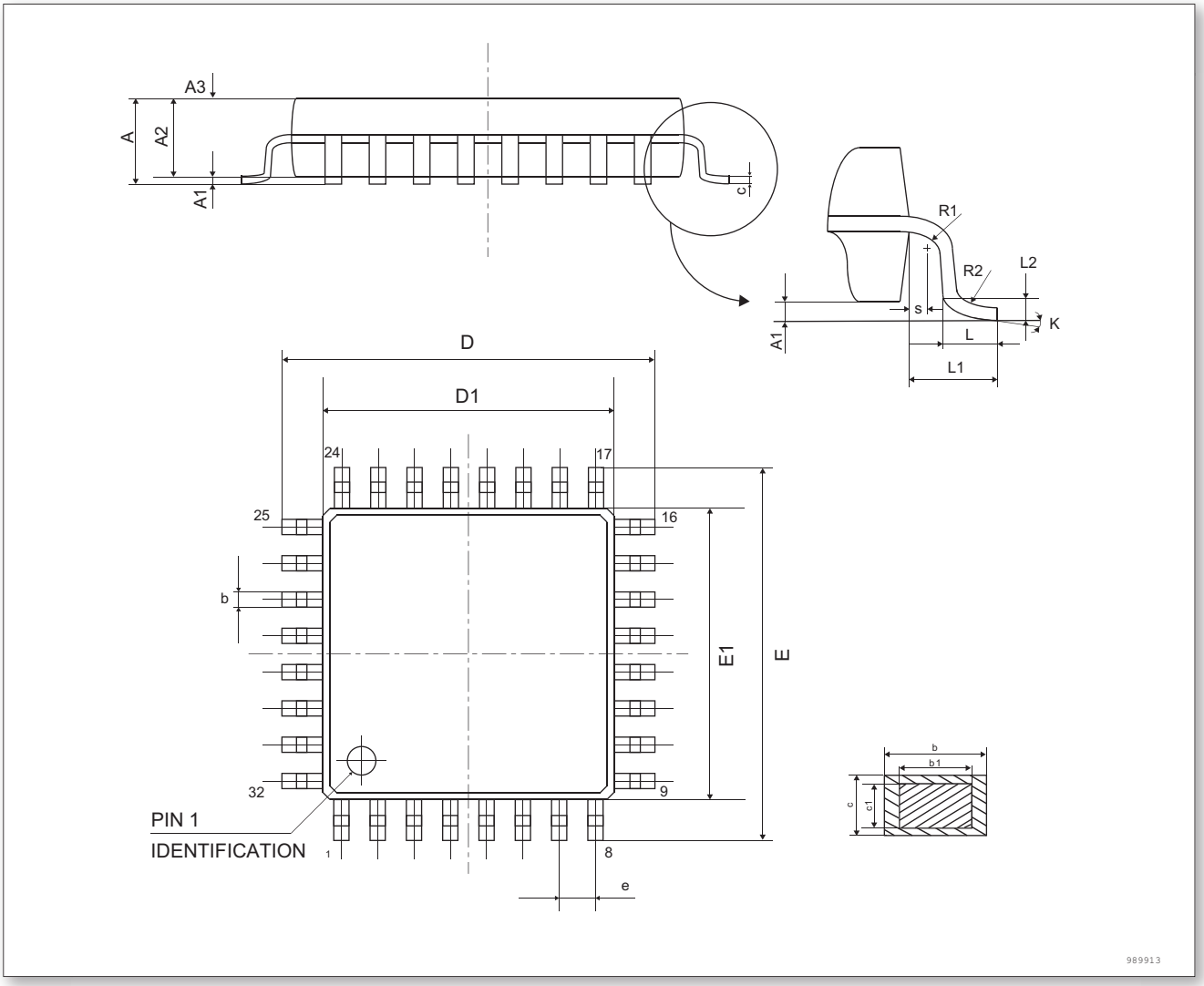

Figure 25. LQFP32 - 32-pin low-profile quad flat package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 44. LQFP32 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32		0.43
b1	0.31	0.35	0.39
c	0.13		0.18
c1	0.12	0.127	0.134

Symbol	Millimeters		
	Min	Typ	Max
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80	
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08		
R2	0.08		0.20
S	0.20		
N	Number of pins = 32		

6.4 QFN32 Package information

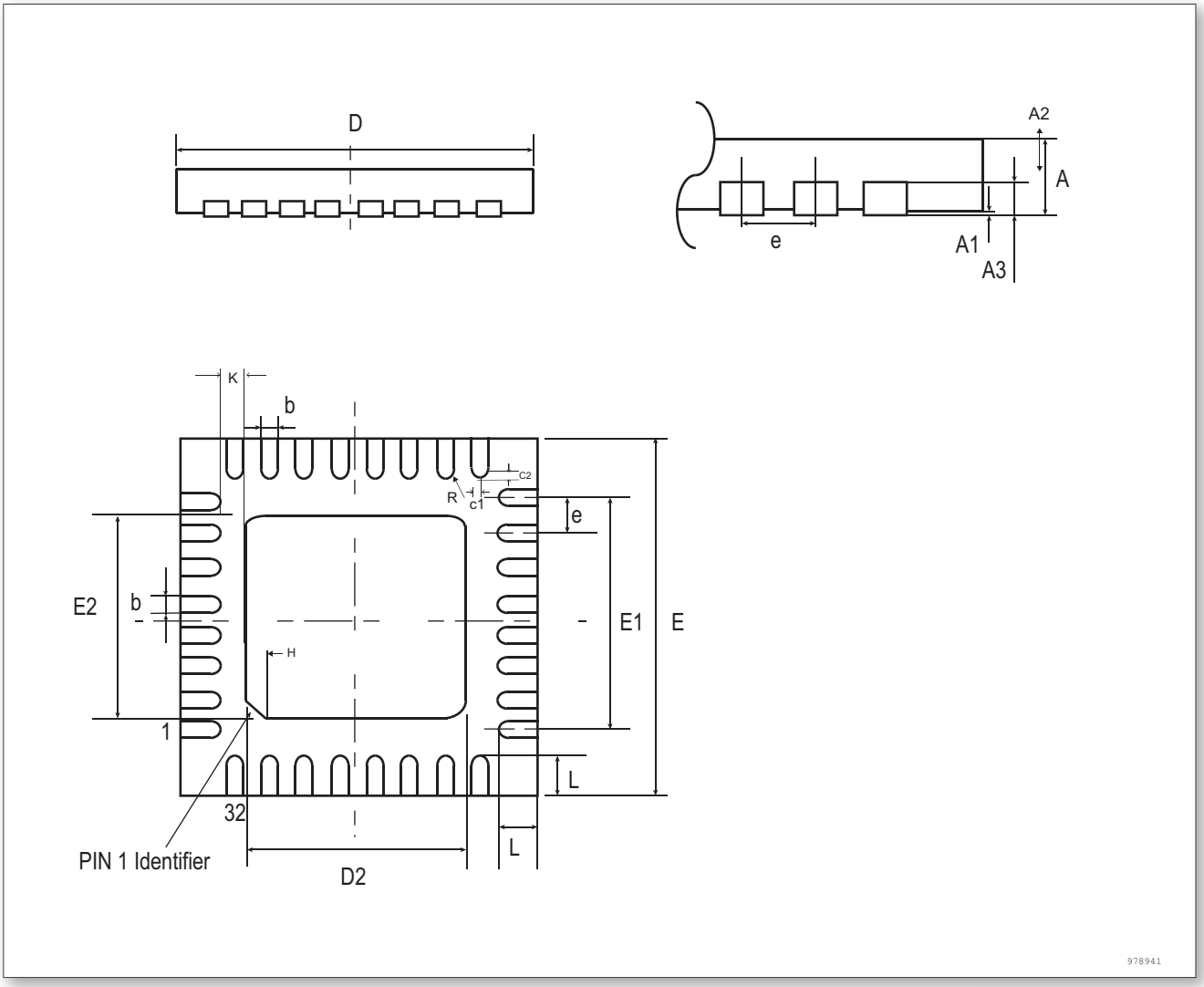

Figure 26. QFN32 - 32-pin quad flat no-leads package outline

1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Table 45. QFN32 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.7	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.40	3.50	3.60

Symbol	Millimeters		
	Min	Typ	Max
E2	3.40	3.50	3.60
e		0.5	
H		0.30REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.09		
c1		0.08	
c2		0.08	
N		Number of pins = 32	

7 Ordering information

Ordering information

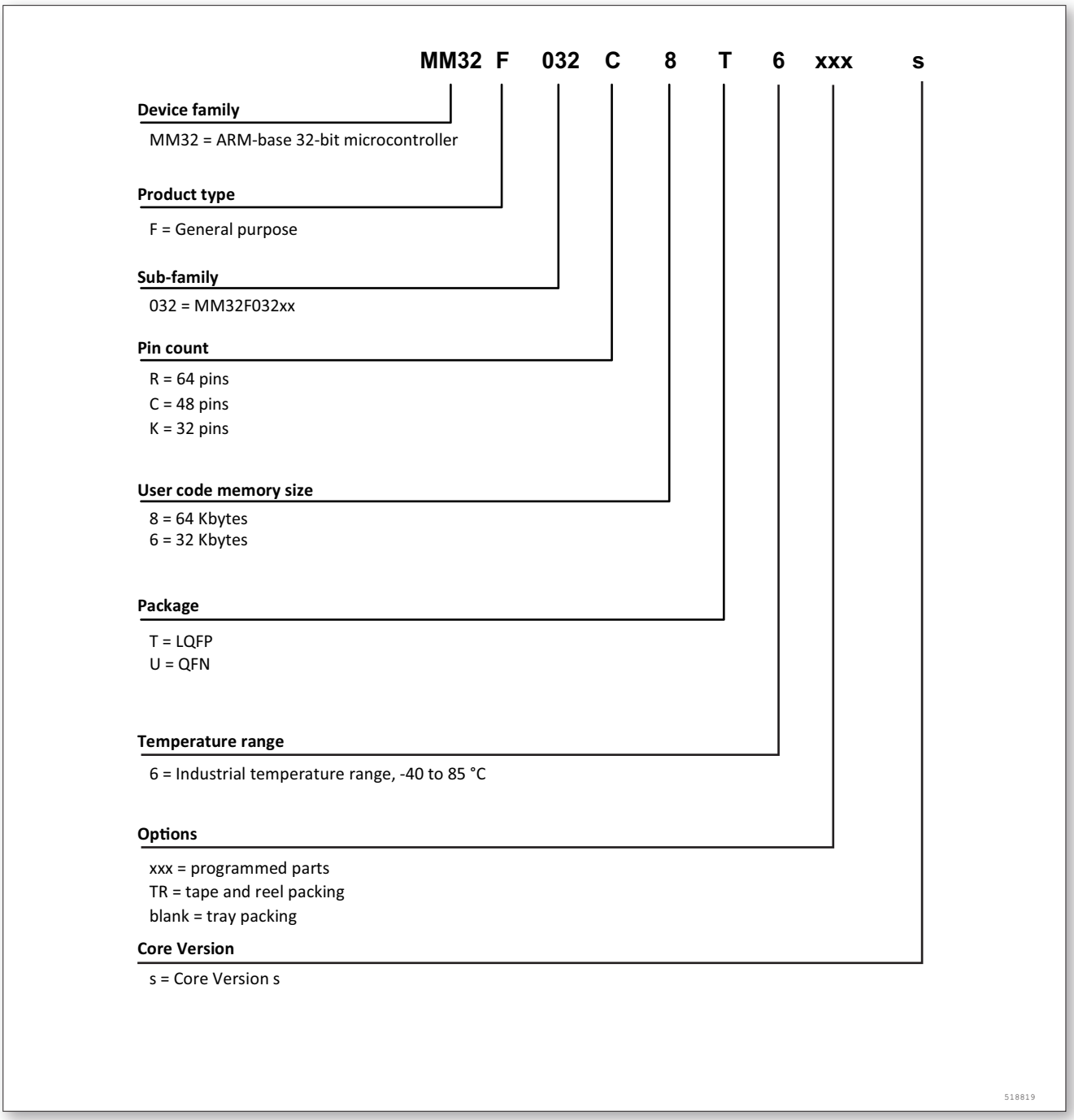

Figure 27. Ordering information scheme

8 Revision history

Revision history

Table 46. Document revision history

Date	Revision	Changes
2019/09/10	Rev1.00	Initial release.