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Operation and Control of an Improved Performance Interactive DSTATCOM

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***Abstract*—This paper proposes an improved performance interactive distribution static compensator (DSTATCOM) to address limitations of conventional current control mode (CCM) and voltage control mode (VCM) operations. The proposed interactive scheme provides smooth transfer of modes of operation while remaining connected in the distribution system. In normal operation, the DSTATCOM operates in CCM to make source currents balanced, sinusoidal, and at unity power factor. During voltage disturbances, the CCM operation cannot improve load voltage. In that case, DSTATCOM operation is changed to VCM which maintains a constant voltage across the sensitive loads. Hence, this interactive DSTATCOM ensures continuous, flexible, and robust operation of the load. Also, the filter current requirements are reduced in proposed scheme which reduces the losses in filter and feeder, improves inverter efficiency, and requires reduced rating inverter for sag mitigation. The principle of operation and control for both the operating mode are analyzed. The detailed process of the flexible transfer between the two modes is derived. Deadbeat predictive control algorithms for CCM as well as VCM operation are developed for fast operation during mode transfers. The performance of the proposed scheme is validated by both simulation and experimental results.**

***Index Terms*—Voltage control mode, current control mode, power factor.**

I. Introduction

Switching devices in combination with unbalanced reactive loads produce current related power quality (PQ) problems by making source currents distorted and unbalanced [1], [2]. A distribution static compensator (DSTATCOM) operating in current control mode (CCM) is used to mitigate current related PQ problems [3]–[9]. In CCM operation, the DSTATCOM supplies reactive and harmonic component of load currents to make source currents balanced, sinusoidal, and in-phase with respective phase load voltages.

Generally, faults in power system and energization of larger loads create voltage disturbances like sag and swell. Also, integration of intermittent distributed generation causes voltage fluctuations in the distribution system. These voltage disturbances significantly affect the power transfer from the source to load and degrade the performance of sensitive loads [10]. However, conventional CCM operation of DSTATCOM cannot improve the load voltage. This is major limitation of CCM operation of DSTATCOM which considerably restricts its utilization.

A DSTATCOM, when operated in voltage control mode (VCM), is one of the most effective device used for load voltage regulation [10]–[14]. In VCM operation, the DSTATCOM regulates load voltage at a constant reference value by supplying appropriate fundamental reactive current into the source. Therefore, VCM operation of DSTATCOM provides stable and continuous operation of the load.

However, conventional VCM operation of DSTATCOM maintains an arbitrary chosen voltage of 1.0 p.u. at the load terminal. For this voltage at load terminal, source exchanges reactive power even at normal operating conditions [10]–[13]. This continuous reactive power exchange results in more reactive current flow in the voltage source inverter (VSI) as well as feeder. Consequently, losses in the VSI and feeder increase. Therefore, VCM operation of DSTATCOM is not required during normal supply conditions.

Aforementioned analysis brings the fact that the conventional CCM and VCM operations of DSTATCOM are not required during voltage disturbances and normal disturbances, respectively. This greatly limits utilization of the DSTATCOM. Moreover, recent advancements in device topologies and control algorithms have encouraged customers to look for devices which can provide various operational characteristics with less number of components, reduced cost, weight, and space. A possible solution to improve utilization of DSTATCOM is to operate the device in different modes during normal operation and voltage disturbances. However, feasibility and advantages of interactive DSTATCOM operation, where it has capability to transfer modes of operation while remaining connected to the distribution system has not been explored in the literature.

This paper proposes operation and control of an improved performance interactive DSTATCOM for continuous and stable load operation while addressing aforementioned issues. In this work, a control algorithm is proposed to compute range of source voltage within which a DSTATCOM should operate in CCM. This algorithm depends upon the supply voltage, maximum and minimum feeder impedance, and load current. Outside this range, operational mode of DSTATCOM is transferred to VCM. This interactive DSTATCOM provides several operational features which are not possible in conventional DSTATCOM operation i.e., 1) Advantages of CCM during normal supply conditions, 2) Advantages of VCM during voltage disturbances, 3) Unlike conventional VCM, no reactive power exchanges with the supply during normal supply conditions, 4) Reduced losses in VSI and feeder compared to conventional VCM, and 5) Requires reduced rating VSI for sag mitigation compared to conventional VCM.

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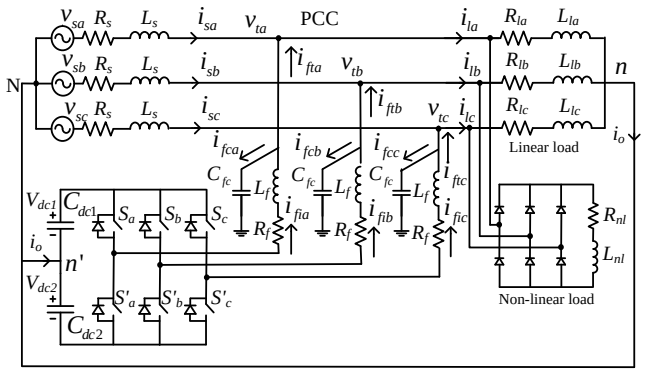

Fig. 1. Three phase circuit of DSTATCOM in a distribution system.

Deadbeat predictive control algorithms for CCM as well as VCM operation are developed for fast operation during mode transfers [15], [16].

II. DSTATCOM Structure and Controller Design in CCM and VCM

Fig. 1 shows the power circuit diagram of a DSTATCOM connected at point of common coupling (PCC). It is realized by a three-phase, four-wire VSI with two dc link capacitors [11]. An LC filter is connected between the VSI and PCC. Shunt capacitor, C_{fc}, connected across PCC helps in elimination of high-switching frequency components and prohibits them to enter into the source. Voltages across both the dc capacitors C_{dc1} = C_{dc2} = C_{dc} are maintained at a constant value V_{dc1} = V_{dc2} = V_{dc}. Source voltages, PCC voltages, load currents, source currents, and filter currents are v_{sj}, v_{lj}, i_{lj}, i_{sj}, and i_{ftj}, respectively with j = a, b, c as three phases.

A. System Modeling and Development of Switching Strategy

The VSI topology used in this work provides an independent control of each leg of the VSI [17]. This makes modelling of single phase circuit shown in Fig. 2 sufficient to explain the operation. Output voltage of the VSI is represented by $u\,V_{dc}$. The term, u, is a switching control variable (with value +1 or -1). State space equation for this circuit is given as follows:

$$\dot{x} = A\,x + B\,z \tag{1}$$

where

$$A = \begin{bmatrix} 0 & 1/C_{fc} & 0 \\ -1/L_f & -R_f/L_f & 0 \\ -1/L_s & 0 & -R_s/L_s \end{bmatrix},$$

$$B = \begin{bmatrix} 0 & -1/C_{fc} & 0 \\ V_{dc}/L_f & 0 & 0 \\ 0 & 0 & 1/L_s \end{bmatrix},$$

$$x = [v_{fc} \quad i_{fi} \quad i_s]^t, \quad z = [u \quad i_{ft} \quad v_s]^t.$$

Discrete form of the continuous state equation is given as follows [2]:

$$x(k+1) = G\,x(k) + H\,z(k) \tag{2}$$

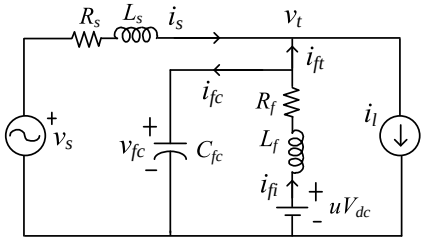

Fig. 2. Single phase equivalent circuit of DSTATCOM in a distribution system.

where G and H are sampled matrices with a sampling time of T_d. For small sampling time, the matrices G and H are calculated as follows:

$$G = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} = e^{AT_d} \approx I + AT_d + \frac{A^2T_d^2}{2}$$

$$= \begin{bmatrix} 1 - \frac{T_d^2}{2L_fC_{fc}} & \frac{T_d}{C_{fc}} - \frac{T_d^2R_f}{2L_fC_{fc}} & 0 \\ -\frac{T_d}{L_f} + \frac{R_fT_d^2}{2L_f^2} & 1 - \frac{R_fT_d}{L_f} - \frac{T_d^2}{2L_f}\left[\frac{1}{C_{fc}} - \frac{R_f^2}{L_f}\right] & 0 \\ -\frac{T_d}{L_s} + \frac{R_sT_d^2}{2L_s^2} & \frac{T_d^2}{2L_sC_{fc}} & 1 - \frac{R_sT_d}{L_s} - \frac{R_s^2T_d^2}{2L_s^2} \end{bmatrix}$$

$$H = \begin{bmatrix} H_{11} & H_{12} & H_{13} \\ H_{21} & H_{22} & H_{23} \\ H_{31} & H_{32} & H_{33} \end{bmatrix} = \int_0^{T_d} e^{A\lambda} B\, d\lambda$$

$$\approx \int_0^{T_d} (I + A\lambda)\, B\, d\lambda$$

$$= \begin{bmatrix} \frac{T_d^2V_{dc}}{2L_fC_{fc}} & -\frac{T_d}{C_{fc}} & 0 \\ \frac{V_{dc}}{L_f}\left(T_d - \frac{R_fT_d^2}{L_f}\right) & \frac{T_d^2}{2L_fC_{fc}} & 0 \\ 0 & \frac{T_d^2}{2L_sC_{fc}} & \frac{1}{L_s}\left(T_d - \frac{R_sT_d^2}{2L_s}\right) \end{bmatrix}.$$

With one switching variable, the VSI can control only one reference at a time. Hence, it is assumed that $u_i(k)$ and $u_v(k)$ are switching variables for CCM and VCM, respectively at the k^{th} sampling. These are calculated as follows:

1) Generation of Current Control Law: The filter current at the $(k+1)^{th}$ sampling instant, from (2), is given as following:

$$i_{fi}(k+1) = G_{21}v_{fc}(k) + G_{22}i_{fi}(k) + H_{21}u_i(k) + H_{22}i_{ft}(k). \tag{3}$$

When (3) is implemented, each switching state gives a different current prediction. In other words, each switching strategy requires a future current through the IGBT which is unknown at the k^{th} sampling. Therefore, a cost function (J) is defined as follows [11]:

$$J = \left[i_{fi}(k+1) - i_{fi}^*(k+1)\right]^2 \tag{4}$$

where $i_{fi}^*(k+1)$ is reference current at $(k+1)^{th}$ sampling. To minimize cost function, it is differentiated with respect to

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$u_i(k)$ and equated to zero. Finally, J is minimum at

$$i_{fi}(k+1) = i^*_{fi}(k+1). \tag{5}$$

Reference current control law is obtained after replacing (5) in (3). However, it can be noticed that the (3) contains future reference current $i^*_{fi}(k+1)$ which is unknown. To know the future value of any signal in discrete domain when sampling time is constant, extrapolation is used which predicts the future value using known values of previous sampling instants. Order of extrapolation depends upon the sampling period. Lesser the sampling period, higher will be extrapolation and vice versa. To know $i^*_{fi}(k+1)$, following Lagrange's extrapolation formula is used [18]:

$$i^*_{fi}(k+1) = \sum_{l=0}^{n} (-1)^{n-1} \binom{n+1}{l} i^*_{fi}(k+l-n). \tag{6}$$

For second order extrapolation, n is replaced by 2 in (6) and a linear prediction is given as

$$i^*_{fi}(k+1) = 3\, i^*_{fi}(k) - 3\, i^*_{fi}(k-1) + i^*_{fi}(k-2). \tag{7}$$

Expression for reference current, $i^*_{fi}(k+1)$, is valid for a wide frequency range, when substituted in (3) yields to one-step-ahead deadbeat current control law. The reference current control law from (3), (5), and (7) is given as

$$u^*_i(k) = \frac{i^*_{fi}(k+1) - G_{21} v_{fc}(k) - G_{22} i_{fi}(k) - H_{21} i_{ft}(k)}{H_{22}}. \tag{8}$$

2) Generation of Voltage Control Law: From (2), the capacitor voltage at the $k+1^{th}$ sampling instant will be

$$\begin{aligned} v_{fc}(k+1) = G_{11} v_{fc}(k) + G_{12} i_{fi}(k) + H_{11} u_v(k) \\ + H_{12} i_{ft}(k). \end{aligned} \tag{9}$$

The procedure for obtaining $u^*_i(k)$ is followed to obtain the reference voltage control law. It is given as follows:

$$u^*_v(k) = \frac{v_{fc}(k+1) - G_{11} v_{fc}(k) - G_{12} i_{fi}(k) - H_{12} i_{ft}(k)}{H_{11}} \tag{10}$$

where

$$v_{fc}(k+1) = v^*_t(k+1)$$

$$v^*_t(k+1) = 3\, v^*_t(k) - 3\, v^*_t(k-1) + v^*_t(k-2). \tag{11}$$

The reference control laws, $u^*_i(k)$ and $u^*_v(k)$, are converted into corresponding VSI switching commands using deadbeat current and voltage controller, respectively [2].

The deadbeat predictive control scheme provides stable and robust operation of the system with excellent dynamic performance [19]–[21]. The stability of the system can be verified by applying the z transform, where the transfer function of system in z domain is given as follows [22]:

$$\frac{x(z)}{u(z)} = (zI - G)^{-1} H. \tag{12}$$

In the above transfer function, all the components of the matrices G and H are known. Also, the term I represents unit matrix. Now, the stability of the deadbeat predictive control scheme is found by analysing the poles of the above transfer function. It is found that all the poles of the transfer function lie within the unit circle. Therefore, the scheme used in this work satisfies the stability criterion.

B. Control of dc Link Voltage

The DSTATCOM remains operational without taking any real power from the source. However, dc link voltage decreases continuously due to the losses in the inverter. Therefore, a control loop is required to maintain the capacitor voltage at a reference value by compensating its losses. It is achieved by taking small real power from the source. The capacitor voltage control in CCM and VCM is achieved as following.

1) Control of dc Link Voltage in CCM: Let the total losses in the VSI be represented by P_{loss}. These losses must be supplied by the source for keeping dc link voltage constant. These are computed using a proportional-integral (PI) controller at positive zero crossing of phase-a voltage. It helps in maintaining the dc link voltage $(v_{dc1} + v_{dc2})$ at a predefined reference value $(2\,V_{dcref})$ by drawing a set of balanced currents from the source and is given as

$$P_{loss} = K_{pc}\, e_{vdc} + K_{ic} \int e_{vdc}\, dt \tag{13}$$

where K_{pc}, K_{ic}, and e_{vdc} = $2\,V_{dcref}$ - $(v_{dc1} + v_{dc2})$ are proportional gain, integral gain, and voltage error of the PI controller, respectively.

2) Control of dc Link Voltage in VCM: Average real power at the PCC (P_{pcc}) is sum of average load power (P_{lavg}) and VSI losses (P_{loss}). The power, P_{pcc}, is taken from the source depending upon the angle between source and load voltages i.e., load angle δ. The VSI losses are compensated by taking small real power, P_{loss}, from the source. If capacitor voltage is regulated to a reference value, then in steady state condition P_{loss} is a constant value and forms a fraction of P_{pcc}. Thus, δ is also a constant value. Once operation mode of DSTATCOM is transferred to VCM, dc link voltage is regulated by generating a suitable value of δ. The total dc link voltage (v_{dc1} + v_{dc2}) is compared with a reference voltage and error is passed through a PI controller. Output of the PI controller, δ, is given as

$$\delta = K_{pv}\, e_{vdc} + K_{iv} \int e_{vdc}\, dt \tag{14}$$

where K_{pv} and K_{iv} are proportional and integral gains of the PI controller, respectively. For stable operation, the value of δ must lie from 0 to 90 degree. Consequently, controller gains are quite small and are chosen carefully.

C. Generation of Reference Quantities

1) Generation of Reference Filter Currents: Performance of a DSTATCOM in CCM mainly depends upon generation of reference filter currents. In this work, reference filter currents (i^*_{fta}, i^*_{ftb}, and i^*_{ftc}) are generated using instantaneous

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symmetrical components theory as following [2]:

$$\begin{aligned} i^*_{fta} &= i_{la} - i^*_{sa} = i_{la} - \frac{v^+_{ta1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \\ i^*_{ftb} &= i_{lb} - i^*_{sb} = i_{lb} - \frac{v^+_{tb1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \\ i^*_{ftc} &= i_{lc} - i^*_{sc} = i_{lc} - \frac{v^+_{tc1}}{\Delta^+_1}(P_{lavg} + P_{loss}) \end{aligned} \tag{15}$$

where $\Delta^+_1 = \sum_{j=a,b,c}(v^+_{tj1})^2$. Losses in the inverter, P_{loss}, are calculated using the PI controller as given in (13). Average load power, P_{lavg}, is calculated using a moving average filter as follows:

$$P_{lavg} = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{ta}i_{la} + v_{tb}i_{lb} + v_{tc}i_{lc})\, dt \tag{16}$$

where terms t_1 and T are arbitrary time instant and time period, respectively.

The voltages v^+_{ta1}, v^+_{tb1}, and v^+_{tc1} are maintained at the PCC and hence, are reference voltages of shunt capacitors. Reference currents through these capacitors lead their respective terminal voltages by 90°. Therefore, reference currents through these capacitors are computed as follows:

$$\begin{bmatrix} i^*_{fca} \\ i^*_{fcb} \\ i^*_{fcc} \end{bmatrix} = j\,\omega\, C_{fc} \begin{bmatrix} v^+_{ta1} \\ v^+_{tb1} \\ v^+_{tc1} \end{bmatrix}. \tag{17}$$

Finally, reference currents of the VSI will be given as

$$\begin{bmatrix} i^*_{fia} \\ i^*_{fib} \\ i^*_{fic} \end{bmatrix} = \begin{bmatrix} i^*_{fta} \\ i^*_{ftb} \\ i^*_{ftc} \end{bmatrix} + \begin{bmatrix} i^*_{fca} \\ i^*_{fcb} \\ i^*_{fcc} \end{bmatrix}. \tag{18}$$

Deadbeat current predictive control as given in (8) is used to realize these currents using the VSI.

2) Generation of Reference Load Voltages: DSTATCOM compensates voltage disturbances by injecting reactive currents. To keep filter current minimum, the load voltages are maintained at 0.9 and 1.1 p.u. during sag and swell, respectively. This improves the voltage regulation capability of DSTATCOM compared to conventional VCM where load voltage magnitude is set at 1.0 p.u.

By knowing the zero crossing of phase-a source voltage, choosing suitable reference load voltage magnitude (V^*_t), and computing load angle from (14), the three-phase reference load voltages are given as follows:

$$\begin{aligned} v^*_{ta} &= \sqrt{2}\, V^*_t \sin(\omega t - \delta) \\ v^*_{tb} &= \sqrt{2}\, V^*_t \sin(\omega t - 2\pi/3 - \delta) \\ v^*_{tc} &= \sqrt{2}\, V^*_t \sin(\omega t + 2\pi/3 - \delta) \end{aligned} \tag{19}$$

where ω is system frequency. These voltages are realized by the VSI using deadbeat voltage predictive control law given in (10).

III. Flexible Mode Transfer Voltage Range for Interactive DSTATCOM

Generally, loads perform satisfactorily within the $\pm 10\%$ range of the nominal voltage (i.e., 0.9 to 1.1 p.u.), also called normal operating conditions. In these conditions, current related PQ problems are of the main concern. Therefore, the DSTATCOM is operated in CCM for load harmonic and reactive current compensation. It results in balanced and sinusoidal source currents with unity power factor at the PCC.

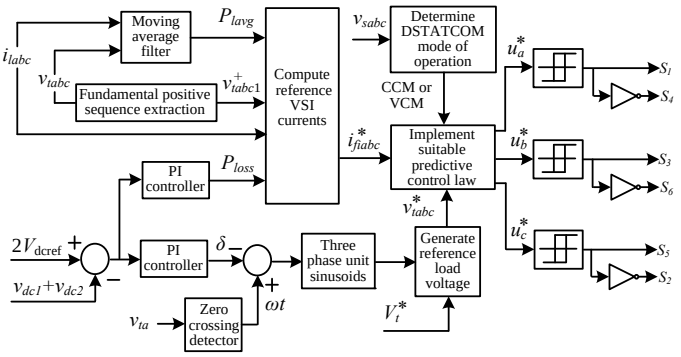

Fig. 3. Control block diagram of proposed interactive DSTATCOM.

However, the load voltage can change at any time due to voltage disturbances. This will result in performance deterioration of the sensitive loads making CCM operation of DSTATCOM redundant. In this case, DSTATCOM must switch to VCM from CCM to protect sensitive loads from these unwanted variations in voltage by maintaining a constant voltage at the load terminal. In this section, a control algorithm for flexible mode transfer between CCM to VCM and vice versa has been presented.

At any time of DSTATCOM operation, relation between the source and load points from Fig. 2 is given as follows:

$$\boldsymbol{V}_s = \boldsymbol{V}_t + \boldsymbol{I}_s \boldsymbol{Z}_s. \tag{20}$$

The DSTATCOM operating in CCM maintains unity power factor at the PCC. Therefore, the source current and the load voltage will be in-phase with the each other. $\boldsymbol{V}_s = V_s\angle\delta$, $\boldsymbol{V}_t = V_t\angle 0^\circ$, $\boldsymbol{I}_s = I_s\angle 0^\circ$, and $\boldsymbol{Z}_s = R_s + jX_s$ are replaced in (20). After simplification, we get

$$V_s\angle\delta = V_t + I_sR_s + jI_sX_s. \tag{21}$$

Equating the magnitude of both sides of (21), following relation is obtained:

$$V_s^2 = (V_t + I_sR_s)^2 + (I_sX_s)^2. \tag{22}$$

Rearranging (22), the load voltage magnitude is given as

$$V_t = \sqrt{V_s^2 - (I_sX_s)^2} - I_sR_s. \tag{23}$$

After further simplification

$$V_t = V_s\left[\sqrt{1 - \left(\frac{I_sX_s}{V_s}\right)^2} - \frac{I_sR_s}{V_s}\right]. \tag{24}$$

With $\frac{I_sR_s}{V_s} = \epsilon_r$ and $\frac{I_sX_s}{V_s} = \epsilon_x$ as p.u. resistance and reactance, respectively, (24) will result into

$$V_t = V_s\left[\sqrt{1 - \epsilon_x^2} - \epsilon_r\right]. \tag{25}$$

It can be observed that the load voltage magnitude will re-

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TABLE I
SYSTEM PARAMETERS FOR SIMULATION STUDIES

System quantities	Values
Source voltage	230 V rms (L-N), 50 Hz
Feeder impedance	Z_s = 0.785 + j3.14 Ω
Linear load	Z_{la} = 60 + j62.8 Ω, Z_{lb} = 40 + j78.5 Ω, Z_{lc} = 50 + j50.24 Ω
Non-linear load	25 + j47.1 Ω
VSI parameters	V_{dc} = 600 V, C_{dc} = 3000 μF, C_{fc} = 10 μF L_f = 5 mH, R_f = 0.01 Ω
PI controller gains	K_{pv} = 7×10^{-6}, K_{iv} = 8×10^{-6}, K_{pc} = 20, K_{ic} = 1

duce with the increase in load power and maximum reduction will be at the base load. Also, both the feeder resistance and inductance contribute in the load voltage drop.

From (25), it is clear that the minimum source voltage at which the load voltage does not become less than 0.9 p.u. must be computed at the base value of the feeder impedance. If load voltage is more than 0.9 p.u. for maximum load then it will certainly be more than 0.9 p.u. for other loads. Also, it is required to find out minimum operating source voltage at which the load voltage will be more than 1.1 p.u. of the nominal voltage, i.e., the load experiences voltage swell. If load voltage is less than 1.1 p.u. for the lowest possible value of the load power, then it is valid for all other loads. Eventhough this scheme does not require knowledge of source impedance throughout the DSTATCOM operation, several schemes for online grid impedance measurement have been available [23]–[27].

Let us consider that subscripts '1' and '2' represent voltage sag and swell, respectively. Therefore, (25) leads into two different equation.

$$V_{t1} = V_{s1}\left[\sqrt{1-\epsilon_{x1}^2} - \epsilon_{r1}\right]. \tag{26}$$

$$V_{t2} = V_{s2}\left[\sqrt{1-\epsilon_{x2}^2} - \epsilon_{r2}\right]. \tag{27}$$

For base load of 10 kVA with the parameters given in Table I, the base value of the source resistance and reactance are 0.05 and 0.2 p.u., respectively. Also, minimum value of source impedance can be zero. After substituting these values in (26) and (27), following two relations are obtained:

$$V_{t1} = 0.9748\, V_{s1}. \tag{28}$$

$$V_{t2} = V_{s2}. \tag{29}$$

Several schemes have been presented to estimate source voltage for different applications like grid connected inverters, rectifier operation, motor drive application, renewable energy applications, power quality control, etc., [28]–[30]. The source voltage measurement schemes used in above applications are equally applicable for DSTATCOM application as well. Therefore, it is assumed that the measurement of source voltage is available.

Based on (28) and (29), a source voltage range is derived for CCM operation of the DSTATCOM. Any voltage deviation from this range is an indication of the voltage disturbance

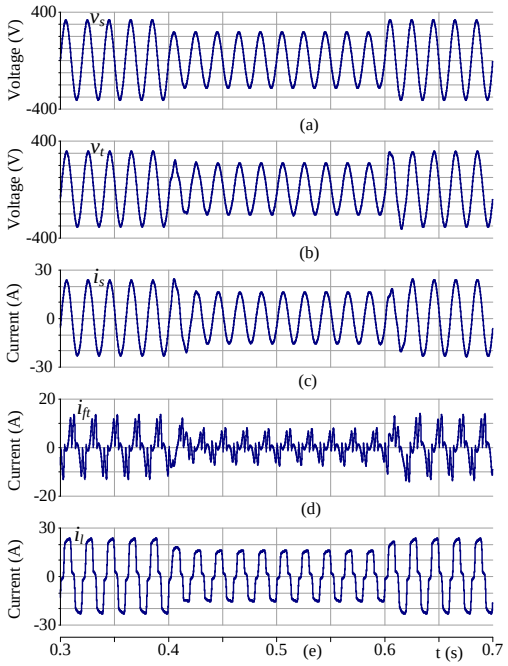

Fig. 4. Simulation results with conventional CCM. (a) Source voltage. (b) Load voltage. (c) Source current. (d) Filter current. (e) Load current.

and the DSTATCOM mode will be transferred to VCM. From (28), load voltage is 0.9748 p.u. for a source voltage of 1.0 p.u. under the worst normal operating conditions. The voltage sag refers to reduction in load voltage from 0.9 to 0.1 p.u. of nominal value for half cycle to one minute [2]. It means that if V_s is 0.9232 p.u. then PCC will experience sag. Thus, it is possible to set limit for sag occurrence as V_s = 0.9232 p.u. and is denoted as lower limit. A swell is defined as increase in terminal voltage from 1.1 to 1.8 p.u. from nominal voltage for half cycle to one minute. From (29), V_s = 1.1 p.u. will produce a swell at PCC at worst normal operating condition and is denoted by upper limit. Thus, it can be concluded that:

(1) If V_s is less than 0.9232 p.u. and greater than 1.1 p.u. then the DSTATCOM can operate in VCM to regulate load voltage.

(2) If source voltage lies between 0.9232 to 1.1 p.u. then the DSTATCOM can operate in CCM.

IV. SIMULATION RESULTS

Before showing results of proposed improved performance interactive DSTATCOM, results providing limitations of the conventional CCM and VCM DSTATCOM operations are presented. PSCAD software is used for the simulation studies. System parameters are given in Table I.

Performance of conventional CCM operation of DSTATCOM is shown in Figs. 4(a)-(e). The figure shows waveforms of source voltage (v_s), load voltage (v_t), source current (i_s), filter current (i_{ft}), and load current (i_l), respectively. Throughout the operation, filter current consists of reactive and harmonic component of load current and makes source current sinusoidal and in-phase with the load voltage. For t = 0.4 to 0.6 s, source voltage is reduced by 30%. In this case,

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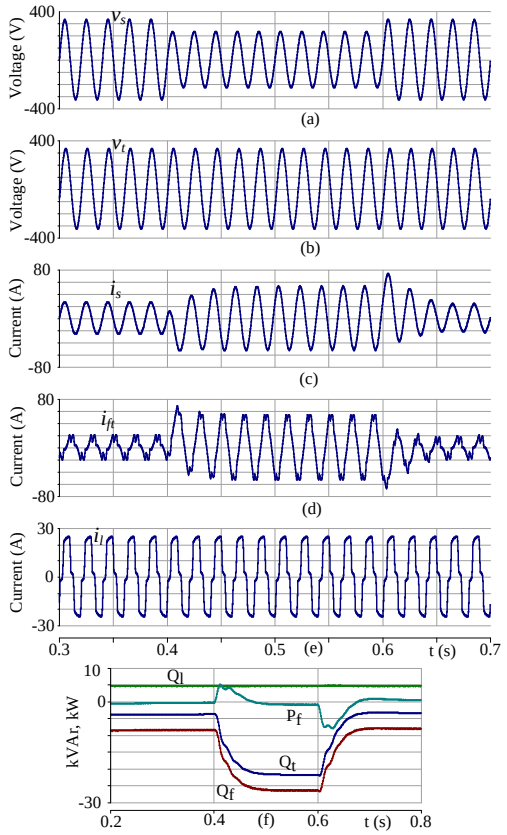

Fig. 5. Simulation results with conventional VCM. (a) Source voltage. (b) Load voltage. (c) Source current. (d) Filter current. (e) Load current. (f) Load reactive (Q_l), filter reactive (Q_f), source reactive (Q_t), and filter real (P_f) powers.

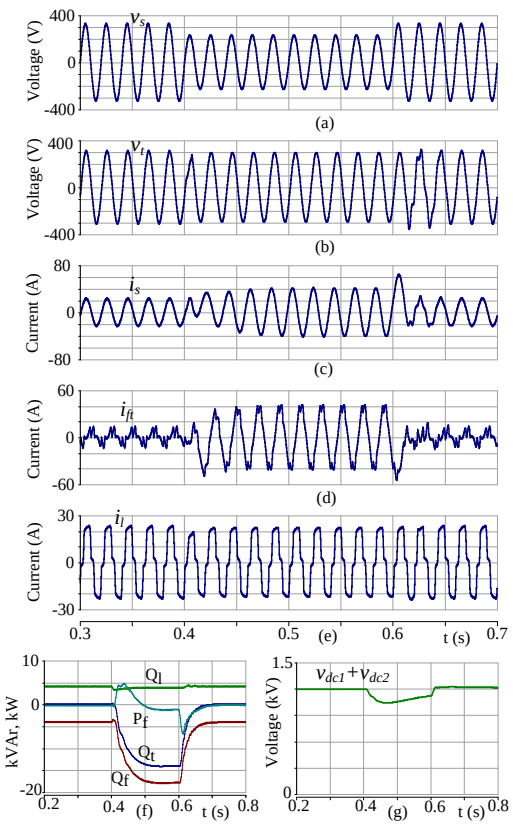

Fig. 6. Simulation results in proposed scheme during normal to sag and vice-versa. (a) Source voltage. (b) Load voltage. (c) Source current. (d) Filter current. (e) Load current. (f) Load reactive (Q_l), filter reactive (Q_f), source reactive (Q_t), and filter real (P_f) powers. (g) Voltage at dc bus.

load voltage also gets reduced. Consequently, performance of the load deteriorates. Therefore, CCM operation is not useful during voltage disturbances, and DSTATCOM needs to be removed from the operation. This is a major limitation of CCM operation.

Fig. 5 shows waveforms of conventional VCM operation of DSTATCOM where reference voltage is set at 1.0 p.u. Here, the DSTATCOM compensates for the drop in the feeder. In this case, filter supplies reactive current into the source, and source current leads the load voltage. Therefore, filter and source currents are increased. As seen from Fig. 5(f) during normal operation, the filter supplies total of 8.5 kVAr out of which 4 kVAr is supplied towards the source. Therefore, source exchanges reactive power in conventional VCM operation even at normal operation. During t = 0.4 to 0.6 s when source voltage is reduced by 30%, load voltage is maintained at 1.0 p.u. To achieve this, the filter injects 27 kVAr, whereas 22.5 kVAr is supplied to the source.

Compensation performance of proposed interactive DSTATCOM operation is shown in Fig. 6. Nominal source voltage is applied for t = 0 to 0.4 s. The DSTATCOM operates in CCM to compensate for load harmonic and reactive current. The load voltage and source current are sinusoidal. The filter current, consisting of harmonic and reactive components of load current, makes the load voltage and source current in-phase with each other. Also, source does not exchange reactive power as opposed to 4 kVAr in conventional VCM operation. Further, a voltage sag of 30% is created for 10 cycles from t = 0.4 to 0.6 s. Once sag is detected, the mode of operation is changed to VCM and a constant voltage of 0.9 p.u. is maintained at the load terminal. The source current increases during this period due to reactive current supplied by the filter for providing voltage support. However, the reactive power supplied by the filter is only 18 kVAr as compared to 27 kVAr in conventional VCM operation. At t = 0.6 s, source voltage is brought back to normal value. Hence, the operational mode of the DSTATCOM is transferred to CCM. The voltage at the dc bus, shown in Fig. 6(g), is maintained at 1200 V during the CCM using the PI controller. During sag, the voltage decreases but PI controller used in VCM slowly brings it back towards the reference value. Once sag vanishes, the CCM PI controller brings the voltage to the reference voltage.

A. Reduction in Power Rating

Since the conventional CCM operation of DSTATCOM is not useful during voltage disturbances, it is not considered here. However, the ratio of reactive power requirement in proposed scheme (S_{pro}) and conventional VCM (S_{con}) during sag is computed as follows:

$$\frac{S_{pro}}{S_{con}} = \frac{18}{27} = 0.67. \tag{30}$$

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TABLE II
COMPARISON PERFORMANCE OF PROPOSED INTERACTIVE DSTATCOM WITH THE CONVENTIONAL SCHEMES

Performance index	**CCM operation**	**Proposed scheme**
Normal operation	Inverter supplies reactive and harmonic component of load current	Inverter supplies reactive and harmonic component of load current
Voltage disturbances	No voltage regulation capability, taken out from service	Maintains a constant voltage at the load terminal
Load operation	Does not guarantee continuous load operation	Guarantees continuous load operation
Utilization	Only for load compensation	Maximized utilization, a single compensator provides several operational features

Performance index	**VCM operation**	**Proposed scheme**
Normal operation	Inverter exchanges reactive power with the source	No reactive power exchange with the source. Hence, reduced current is supplied by the inverter
Voltage disturbances	Maintains constant voltage of 1.0 pu at load terminal	Maintains a constant voltage at 0.9 pu at load terminal which is sufficient for load operation
Power rating	More current is required for voltage compensation, and therefore more power rating VSI is needed	With reduced current requirement for sag mitigation, reduced power rating VSI needed
Loss and efficiency	More current injection means more losses in inverter and feeder. Also, the efficiency will reduce	Reduced losses and improved efficiency

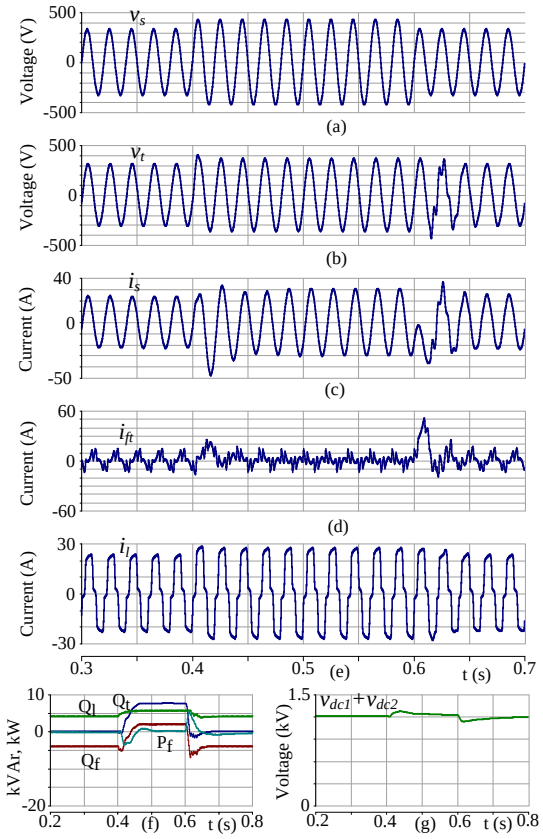

Fig. 7. Simulation results in proposed scheme during normal to swell and vice-versa. (a) Source voltage. (b) Load voltage. (c) Source current. (d) Filter current. (e) Load current. (f) Load reactive (Q_l), filter reactive (Q_f), source reactive (Q_t), and filter real (P_f) powers. (g) Voltage at dc bus.

Therefore, it can be seen that the power rating of the proposed interactive DSTATCOM is only 67% of the conventional VCM operated DSTATCOM. Further, it can be concluded that the sag mitigation capability of the conventional DSTATCOM increases when proposed interactive algorithm is used.

B. Reduction in Losses

Losses in the feeder (P_{lfed}) and interfacing filter (P_{lfil}) are given as follows:

$$P_{lfed} = 3I_s^2 R_s,\ P_{lfil} = 3I_{f1}^2 R_f. \tag{31}$$

It can be seen from Figs 5 and 6 that the source and filter currents are decreased in proposed scheme compared to conventional VCM. Therefore, losses in the feeder as well as interfacing filter are also decreased. The losses can be computed using above equation. Further, reduction in VSI current decreases the power losses in the IGBT switches of the inverter, improves the efficiency, and reduces the electro-magnetic interference.

The compensation performance of proposed scheme during swell is shown in Fig. 7. Before t = 0.4 s, DSTATCOM operates in CCM. The source voltage increases by 30% from t = 0.4 to 0.6 s. To protect load from voltage disturbances, the DSTATCOM changes its mode to VCM and maintains a constant sinusoidal voltage at the load terminal after initial transients. The filter supplies a leading current during this period to support the load voltage. The source voltage recovers at t = 0.6 s and DSTATCOM operating mode is transferred to CCM. Once initial transients are over, load voltage attains its normal value and source current is drawn at a unity power

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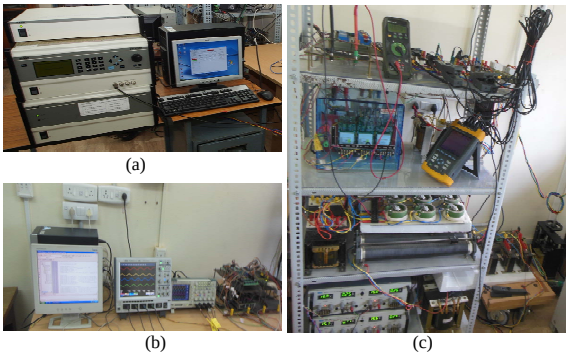

Fig. 8. Experimental setup. (a) Programmable ac power source. (b) Signal conditioning circuit, DSP controller, and host computer. (c) VSI, LC filter, and loads.

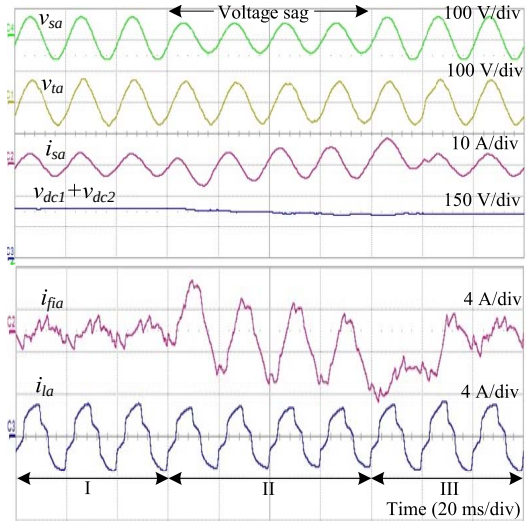

Fig. 9. Experimental waveforms from normal to sag and vice-versa showing source voltage (v_{sa}), load voltage (v_{ta}), source current (i_{sa}), dc bus voltage (v_{dc1} + v_{dc2}), filter current (i_{fia}), and load current (i_{la}).

factor operation with the PCC. Both PI controllers used in CCM and VCM try to maintain dc link voltage at the reference value as seen in Fig. 7(g).

Finally, the advantages of proposed interactive DSTATCOM over conventional CCM and VCM operational modes of DSTATCOM are summarized in Table II.

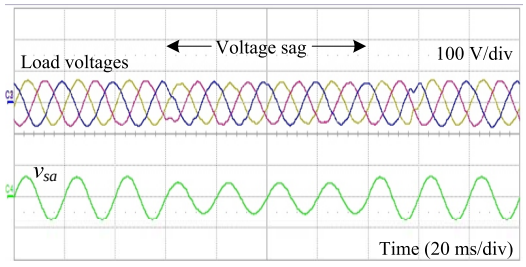

Fig. 10. Experimental waveforms showing three phase load voltages and phase-a source voltage from normal to sag and vice versa.

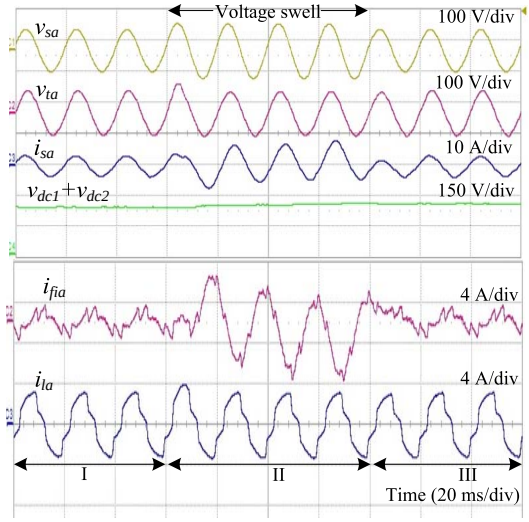

Fig. 11. Experimental waveforms from normal to swell and vice versa showing source voltage (v_{sa}), load voltage (v_{ta}), source current (i_{sa}), dc bus voltage (v_{dc1} + v_{dc2}), filter current (i_{fia}), and load current (i_{la}).

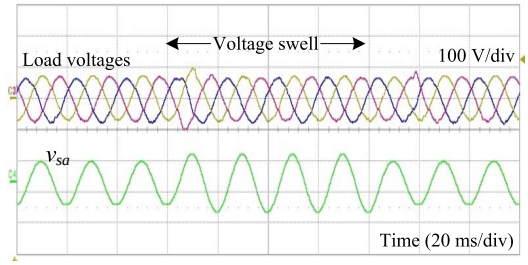

Fig. 12. Experimental waveforms showing three phase load voltages and phase-a source voltage from normal to swell and vice versa.

V. Experimental Results

Reduced scale experimental setup is shown in Fig. 8. The performance of the proposed scheme under various supply conditions are given in this section. System parameters are same as given in Table I with source voltage as 50 V rms per phase.

A. Normal Operation to Sag and Vice Versa

The compensation performance is shown in Fig. 9. It contains three operating regions (I-III) and two mode change overs. Region I shows the steady state waveforms of CCM operation of DSTATCOM. Source current (i_{sa}) and load voltage (v_{ta}) are sinusoidal and in-phase with each other. Filter current (i_{fia}) contains reactive and harmonic component of the distorted load current (i_{la}), whereas dc link voltage (v_{dc1} + v_{dc2}) is maintained at the reference value.

At the end of region I, a voltage sag of 30% is created. Once algorithm detects sag, operational mode of DSTATCOM is transferred from CCM to VCM and a fast regulation is achieved by maintaining load voltage constant. Voltage sag continues for 4 cycles and denoted as region II. In this region, filter supplies additional reactive current towards source to support load voltage which increases the source current. Source current contains some dc component due to

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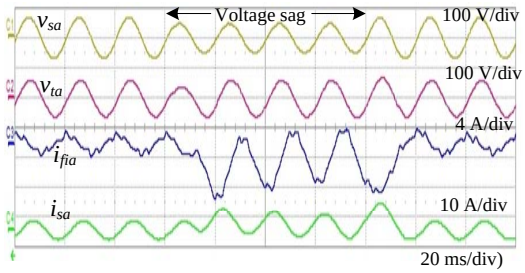

Fig. 13. Experimental waveforms from normal to sag and vice versa where load voltage is maintained at 1.0 p.u. during sag.

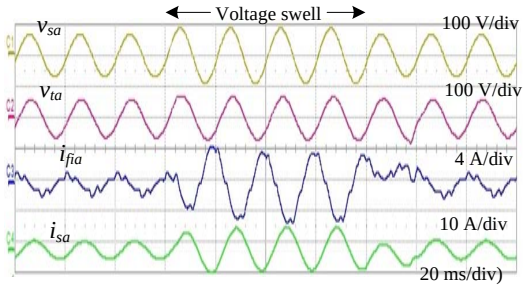

Fig. 14. Experimental waveforms from normal to swell and vice versa where load voltage is maintained at 1.0 p.u. during swell.

the nature of the sag. However, this dc component decays slowly if sag remains for a longer time. When sag is removed, again operation of DSTATCOM is transferred to CCM from VCM and corresponding waveforms are shown in region III of Fig. 9. Source current becomes sinusoidal and unity power factor is achieved within one cycle. The PI controller slowly brings dc link voltage towards the reference voltage. Moreover, load current is drawn as per the requirement. Fig. 10 shows the three phase load voltages, which are balanced and sinusoidal throughout the operation. It can be observed that the DSTATCOM mode transitions are smooth, fast, and provide stable load operation. Further, filter and source currents are reduced in proposed scheme as compared to conventional VCM. Hence, all the benefits as discussed in simulation studies are obtained in experimental studies

B. Normal Operation to Swell and Vice Versa

Fig. 11 shows the performance of DSTATCOM when a voltage swell of 30% is created and removed. Again, it contains three operating regions and two mode change overs. Steady state CCM advantages are achieved in regions I and III, where source current is sinusoidal with a unity power factor. In region II with a swell of 30%, the load voltage is maintained constant at reference value to protect the sensitive loads. Moreover, it can be noticed that the transition of operation modes (from CCM to VCM and vice versa) are nearly smooth and without any transients in load voltage. Three phase load voltages and source voltage in phase-a are shown in Fig. 12. The load voltages waveforms are maintained balanced and sinusoidal, while fast compensation performance is achieved during the mode change over.

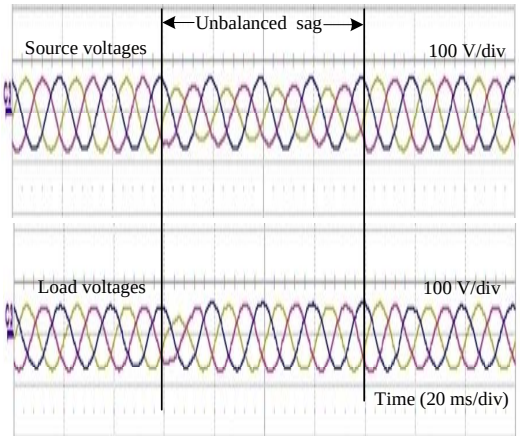

Fig. 15. Experimental waveforms showing three phase source and load voltages during unbalanced voltage sag.

Moreover, the experiments are also conducted under sag and swell conditions where the voltage at the load terminal is maintained at 1.0 p.u. by the DSTATCOM. The experimental waveforms for sag and swell are shown in Figs. 13 and 14, respectively. These results confirm that the proposed interactive DSTATCOM operation can maintain load voltage at the desired reference voltage during voltage disturbances.

Fig. 15 shows the performance of proposed scheme during the unbalanced sag conditions. It can be observed that the scheme allows DSTATCOM to operate in VCM during the unbalanced sag conditions and a balanced sinusoidal voltage is maintained at the load terminal. Moreover, the DSTATCOM operates in CCM during the normal operation.

VI. Conclusions

Operation and control of an improved performance interactive DSTATCOM has been proposed in this paper. The simple control algorithm proposed here, defines a range of supply voltage for which DSTATCOM operates in CCM to mitigate current related PQ problems. During voltage disturbances, operational mode of the DSTATCOM is transferred into VCM from CCM to protect the sensitive loads. The scheme ensures continuous operation of the load. Moreover, losses in feeder and VSI are reduced which improves efficiency of the system. Additionally, these advantages are achieved using a reduced power rating VSI. Therefore, the proposed interactive DSTATCOM has improved performance with reduced loss, cost, and power rating VSI as compared to the conventional CCM and VCM DSTATCOM operation. The simulation and experimental results confirm the effectiveness of the proposed scheme.

References

[1] M. Bollen, *Understanding power quality problems*. IEEE press New York,, 2000, ch. 1, pp. 1-35.

[2] A. Ghosh and G. F. Ledwich, *Power quality enhancement using custom power devices*. Kluwer Publications, 2002.

[3] H. Akagi and K. Isozaki, "A hybrid active filter for a three-phase 12-pulse diode rectifier used as the front end of a medium-voltage motor drive," *IEEE Trans. Power. Electron.*, vol. 27, no. 1, pp. 69–77, Jan. 2012.

[4] B. Singh and S. Arya, "Back-propagation control algorithm for power quality improvement using DSTATCOM," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1204–1212, Mar. 2014.
[5] K. Karanki, G. Geddada, Mahesh K. Mishra, and B. Kumar, "A modified three-phase four-wire UPQC topology with reduced DC-link voltage rating," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3555–3566, Sep. 2013.
[6] A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Parallel-connected shunt hybrid active power filters operating at different switching frequencies for improved performance," *IEEE Trans. Ind. Electron*, vol. 59, no. 11, pp. 4007–4019, Nov. 2012.
[7] S. Rahmani, A. Hamadi, K. Al-Haddad, and L. Dessaint, "A combination of shunt hybrid power filter and thyristor-controlled reactor for power quality," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2152–2164, May 2014.
[8] A. Bhattacharya and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 421–428, Feb. 2011.
[9] B. Singh, C. Jain, and S. Goel, "Ilst control algorithm of single-stage dual purpose grid connected solar pv system," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5347–5357, Oct. 2014.
[10] H. Fujita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," *IEEE Trans. Power. Electron.*, vol. 22, no. 3, pp. 1046–1053, May 2007.
[11] Mahesh K. Mishra, A. Ghosh, and A. Joshi, "Operation of a DSTATCOM in voltage control mode," *IEEE Trans. Power Del.*, vol. 18, no. 1, pp. 258–264, Jan. 2003.
[12] A. Jain, K. Joshi, A. Behal, and N. Mohan, "Voltage regulation with STATCOMs: modeling, control and results," *IEEE Trans. Power. Del.*, vol. 21, no. 2, pp. 726–735, Apr. 2006.
[13] G. Ledwich and A. Ghosh, "A flexible DSTATCOM operating in voltage or current control mode," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 149, no. 2, pp. 215–224, Mar. 2002.
[14] C. Kumar and Mahesh K. Mishra, "A voltage-controlled DSTATCOM for power-quality improvement," *IEEE Trans. Power Del.*, vol. 29, no. 3, pp. 1499–1507, Jun. 2014.
[15] M. Rivera, V. Yaramasu, A. Llor, J. Rodriguez, B. Wu, and M. Fadel, "Digital predictive current control of a three-phase four-leg inverter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4903–4912, Nov. 2013.
[16] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 1323–1325, Feb. 2012.
[17] S. Srikanthan and Mahesh K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.
[18] O. Kukrer, "Discrete-time current control of voltage-fed three-phase PWM inverters," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 260–269, Mar. 1996.
[19] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive control of a three-phase neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2697–2705, Oct. 2007.
[20] P. Cortes, J. Rodriguez, D. Quevedo, and C. Silva, "Predictive current control strategy with imposed load current spectrum," *IEEE Trans. Power. Electron.*, vol. 23, no. 2, pp. 612–618, Mar. 2008.
[21] L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for pwm rectifiers and active filters," *IEEE Trans. Ind. Appl.*, vol. 35, no. 3, pp. 613–620, May 1999.
[22] K. Ogata, *Discrete-time control systems*. Prentice Hall Englewood Cliffs, NJ, 1995, vol. 2.
[23] W. Ghzaiel, M.-B. Ghorbal, I. Slama-Belkhodja, and J. Guerrero, "A novel grid impedance estimation technique based on adaptive virtual resistance control loop applied to distributed generation inverters," in *15th European Conference on Power Electronics and Applications (EPE), 2013*, Sep. 2013, pp. 1–10.
[24] N. Hoffmann and F. Fuchs, "Minimal invasive equivalent grid impedance estimation in inductive-resistive power networks using extended kalman filter," *IEEE Trans. Power. Electron.*, vol. 29, no. 2, pp. 631–641, Feb. 2014.
[25] M. Gasperi, D. Jensen, and D. Rollay, "Method for ac powerline impedance measurement," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1034–1037, Jul. 2008.
[26] A. Timbus, R. Teodorescu, F. Blaabjerg, and U. Borup, "Online grid measurement and ens detection for pv inverter running on highly inductive grid," *IEEE Power Electron. Letters*, vol. 2, no. 3, pp. 77–82, Sep. 2004.
[27] ——, "Online grid impedance measurement suitable for multiple pv inverters running in parallel," in *Twenty-First Annual IEEE, Applied Power Electronics Conference and Exposition, 2006*, Mar. 2006, pp. 5 pp.–.
[28] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an lcl-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep. 2005.
[29] J. Kwon, S. Yoon, and S. Choi, "Indirect current control for seamless transfer of three-phase utility interactive inverters," *IEEE Trans. Power. Electron.*, vol. 27, no. 2, pp. 773–781, Feb. 2012.
[30] Z. Yao, L. Xiao, and Y. Yan, "Seamless transfer of single-phase grid-interactive inverters between grid-connected and stand-alone modes," *IEEE Trans. Power. Electron.*, vol. 25, no. 6, pp. 1597–1603, Jun. 2010.

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