Single-Inductor Dual-Output Buck–Boost Power Factor Correction Converter

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***Abstract*—A single-inductor dual-output (SIDO) buck–boost power factor correction (PFC) converter operating in critical conduction mode is proposed in this paper. By multiplexing a single inductor, each output of the SIDO buck–boost converter can be regulated independently. Compared with a conventional two-stage multiple-output converter, the SIDO buck–boost PFC converter benefits from significant overall cost saving, small size, and light weight. Moreover, the efficiency of the SIDO buck–boost PFC converter can be improved due to single-stage power conversion. The control strategy and characteristics of the proposed converter are analyzed. The efficiency, power factor, total harmonic distortion, and output accuracy are verified using the experimental results.**

***Index Terms*—Critical conduction mode (CRM), power factor correction (PFC), single-inductor dual-output (SIDO), single stage, time multiplexing (TM).**

I. Introduction

MULTIPLE-OUTPUT ac/dc power converter has been becoming popular with fast development of consumer electronics and LED lighting [1]–[3], such as multilevel voltage supply systems, current balancing for multiple LED string driving, RGB LED lighting, etc. IEC 61000-3-2 class C for lighting equipment establishes a strict requirement for the input current harmonic content of power converters [4]. Power factor correction (PFC) is usually used to provide a sinusoidal input current. Hence, research of multiple-output ac/dc power converter with low cost and high power factor (PF) is important.

In order to achieve a high PF and to accurately regulate the output voltages or currents of a multiple-output ac/dc converter, a conventional multiple-output ac/dc power converter consisting of two-stage power conversion is utilized, as shown in Fig. 1, where the PFC preregulator provides the dc bus voltage $v_{\rm bus}$ and parallel-connected dc-to-dc regulators are used to regulate the output voltage or output current from $v_{\rm bus}$ [5]. The circuit configuration of the multiple-output ac/dc converter shown in Fig. 1 is complex and suffers from high cost, with multiple inductors and controllers required [6], [7]. Moreover, the two-stage power conversion with PFC preregulator and dc-to-dc converters suffers from lower efficiency and higher volume and cost. However, the single-stage PFC converter can achieve high PF and output current or voltage regulation at the same time [8], [9]. Hence, it has drawn more and more attention in recent years.

A flyback PFC converter with multiple secondary windings is a typical single-stage multiple-output converter, where only one output can be well regulated. Multiple secondary windings in the transformer lead to cross-regulation due to leakage inductance, forward voltage drop of diodes, and series resistance of the windings [10]. Moreover, only voltage output regulation can be achieved, while multiple current outputs are hard to regulate independently. In order to achieve a highly accurate regulation of multiple-output converters, the magnetic-amplifier postregulator approach is applied in [11] and [12], but it still requires multiple inductors and windings.

A single-inductor multiple-output (SIMO) converter with only one inductor benefits from significant overall cost saving, small size, and light weight, which make it as one of the most suitable and cost-effective solutions for multiple-output power supplies. SIMO dc/dc converters in mobile application have been studied in recent years [13]–[17]. In some offline applications, such as LED lighting, single-stage PFC converters are preferred. A single-stage buck–boost PFC converter has the advantage of low cost and high PF, which make it widely applied in single-output nonisolated general lighting applications [18]. In this paper, a novel single-inductor dual-output (SIDO) buck–boost PFC converter operating in critical conduction mode (CRM) is proposed. Its control strategy and corresponding characteristics are analyzed. Independent regulation of each output can be achieved in this converter by multiplexing a single inductor. Compared with a conventional two-stage multiple-output converter, the proposed converter benefits from significant overall cost saving, small size, light weight, and high power conversion efficiency due to single-stage power conversion. The proposed converter can also be easily extended to realize the SIMO buck–boost PFC converter to fulfill different system requirements.

This paper is organized as follows. In Section II, the SIDO buck–boost PFC converter is proposed and analyzed. The design considerations and analysis are described in Section III. The experimental results including efficiency, PF, total harmonic distortion (THD), and output regulation accuracy are given in Section IV, and Section V summarizes the conclusion drawn from the study.

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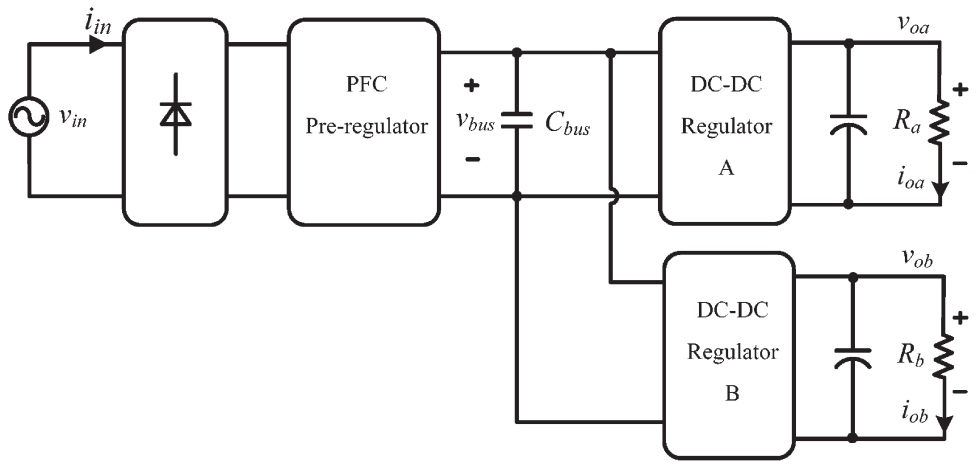

Fig. 1. Block diagram of a conventional multiple-output ac/dc power converter with a high PF.

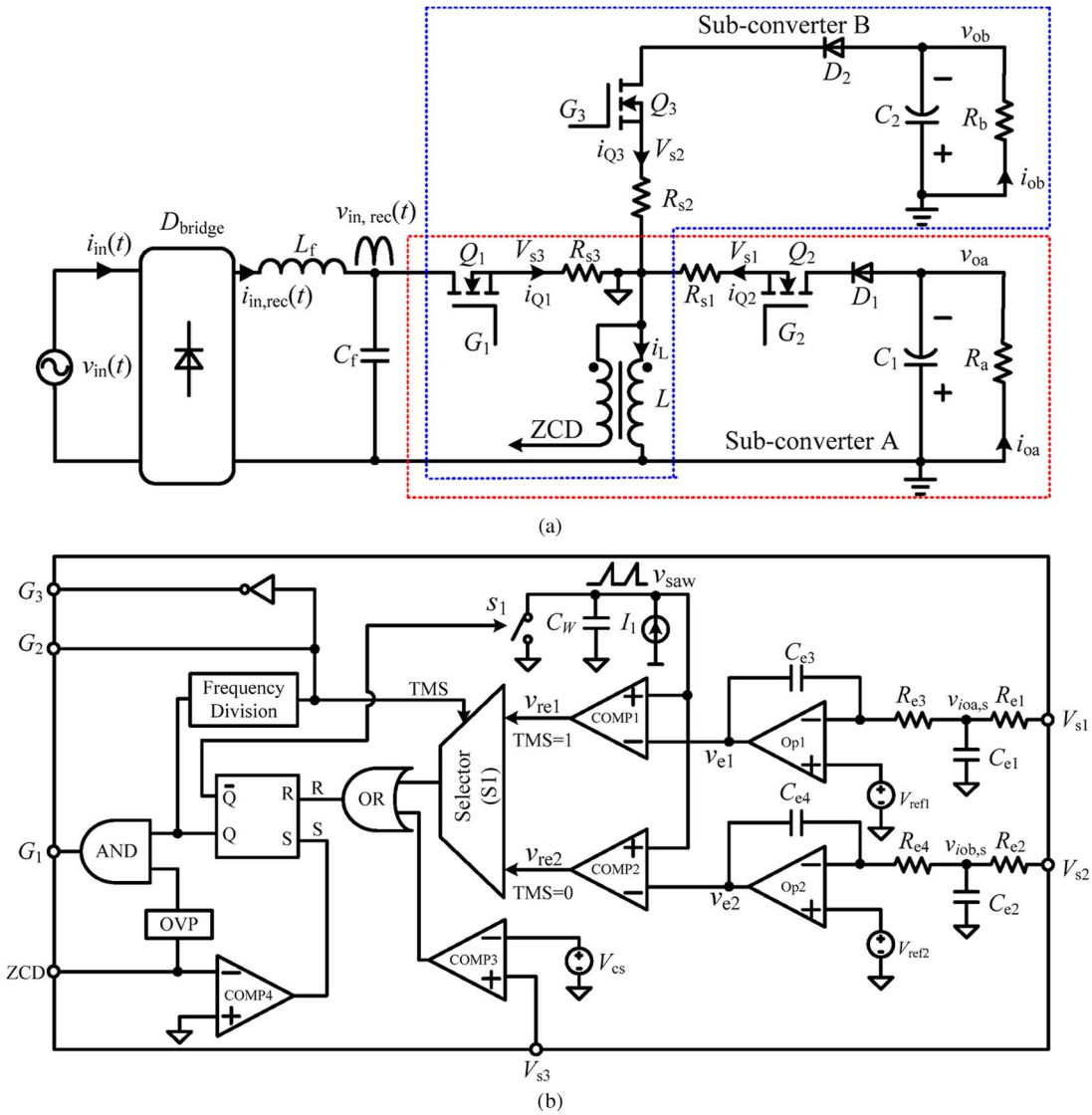

Fig. 2. Proposed SIDO buck–boost PFC converter. (a) Power stage. (b) Controller.

II. Proposed SIDO Buck–Boost PFC Converter

As shown in Fig. 2(a), the power stage of the SIDO buck–boost PFC converter consists of a diode bridge D_{bridge}; an input filter consisting of L_f and C_f; three switch networks consisting of Q_1, Q_2, and Q_3 and their corresponding sense resistors R_{s1}, R_{s2}, and R_{s3}; two freewheeling diodes D_1 and D_2; a

time-multiplexing inductor L; and two output filter capacitors C_1 and C_2. Q_2 and Q_3 are the time-multiplexing control switches of each output. When Q_2 is turned on and Q_3 is turned off, the converter transfers power to output A, and when Q_2 is turned off and Q_3 is turned on, the converter transfers power to output B.

Fig. 2(b) shows the control loop of the SIDO buck–boost PFC converter with two constant output currents. R_{s1}, R_{s2}, and R_{s3} are series connected with Q_1, Q_2, and Q_3, respectively, and their common-connect point is set as signal ground. Thus, Q_1, Q_2, and Q_3 can be driven as "low side" with respect to this signal ground, which benefits from simple driving. As the average of the inductor freewheeling current for each subconverter in a half line cycle is equal to the corresponding output current, it can be detected as the output current for control. V_{s1} and V_{s2} are the sense voltages across sense resistors R_{s1} and R_{s2}, produced by inductor freewheeling currents i_{Q2} and i_{Q3}. The average of V_{s1} and V_{s2} by low-pass filters (R_{e1} and C_{e1}, and R_{e2} and C_{e2}) is used as the output current information for each output. The sense voltage V_{s3} across sense resistor R_{s3}, produced by switch current i_{Q1}, is used as the cycle-by-cycle current limit signal for over current protection. The voltage comparators COMP$[i](i=1,2)$ compare $v_{e[i]}(i=1,2)$ with saw-tooth signal to generate reset signals $v_{\rm re1}$ and $v_{\rm re2}$ for timing-multiplexing (TM) selector S1, respectively, where v_{e1} and v_{e2} are the compensated error voltages between each output and reference current $v_{\rm ref}[i](i=1,2)$. The time-multiplexing signal (TMS), which is the divide-by-2 frequency division signal of the RS flip-flop output, is used to determine which output is controlled. When TMS $=1$, $v_{\rm re1}$ will be selected by S1, and $i_{\rm oa}$ will be regulated to $v_{\rm ref1}/R_{s1}$; similarly, when TMS $=0$, $i_{\rm ob}$ will be regulated to $(v_{\rm ref2}/R_{s2})$. The saw-tooth generator will be reset to zero when Q_1 is turned off and will be set again when the set terminal of the RS flip-flop is high. The input signal of the set terminal of the RS flip-flop is the zero-current-detection (ZCD) signal of the inductor. The ZCD signal, which is coupled by the auxiliary winding from the two outputs, also reflects the output voltage information. When the output voltage is higher than the set value of the controller, over voltage protection (OVP) will be triggered. When the inductor current decreases to zero, the voltage of the auxiliary winding (ZCD) will change to negative. This information can be detected as the zero-current signal for the controller. Therefore, the SIDO buck–boost PFC converter operates in varied-frequency CRM with ZCD.

III. Design Considerations and Analysis

In this section, the SIDO buck–boost PFC converter operating in CRM is analyzed under the following assumptions.

1) All of the components as shown in Fig. 2 are ideal.
2) The switching frequency $f_{\rm sw}$ is much higher than the line frequency $2f_L$, i.e., $f_{\rm sw} \gg 2f_L$; the input voltage can thus be considered as constant in a switching cycle.
3) The input voltage is a full-wave rectified sine wave, i.e., $v_{\rm in,rec}(t)=|v_{\rm in}(t)|=V_p|\sin(\omega_L t)|$, where V_p is the amplitude and $\omega_L=2\pi f_L$ is the angular frequency of the ac input voltage.
4) The output voltages $v_{\rm oa}$ and $v_{\rm ob}$ are constant, i.e., they have a negligible ac ripple in steady state.
5) As the bandwidth of the control loop of the PFC converter is usually much lower than the rectified line frequency $(2f_L)$, the error voltage of each output $v_e[i](i=1,2)$ is constant within each half of a line cycle, i.e., constant on time control can be achieved by the controller.

A. Input Current and Harmonic Current Analysis

Fig. 3 shows the inductor current waveform and its control sequence within a half line cycle. The SIDO buck–boost PFC converter transfers input power to each output alternately by using a varied multiplexing time $(T_A+T_B=T_s)$.

In CRM, the peak inductor current of subconverters A and B in a multiplexing cycle can be obtained as

$$\begin{cases} i_{p,A}(t)=\frac{T_{{\rm on},A}}{L}v_{\rm in,rec}(t)=\frac{v_{\rm oa}}{L}T_{{\rm off},A}(t) \\ i_{p,B}(t)=\frac{T_{{\rm on},B}}{L}v_{\rm in,rec}(t)=\frac{v_{\rm ob}}{L}T_{{\rm off},B}(t) \end{cases} \tag{1}$$

where $T_{{\rm on},A}$, $T_{{\rm on},B}$, $T_{{\rm off},A}$, and $T_{{\rm off},B}$ are the turn-on times and turn-off times of subconverter A and subconverter B, and $v_{\rm oa}$ and $v_{\rm ob}$ are the output voltages of subconverters A and B, respectively.

From (1), the turn-off time of subconverters A and B in a multiplexing cycle can be described by

$$\begin{cases} T_{{\rm off},A}(t)=\frac{T_{{\rm on},A}}{v_{\rm oa}}v_{\rm in,rec}(t) \\ T_{{\rm off},B}(t)=\frac{T_{{\rm on},B}}{v_{\rm ob}}v_{\rm in,rec}(t). \end{cases} \tag{2}$$

From (1) and (2), the multiplexing cycle of the CRM SIDO buck–boost PFC converter can be given as

$$T_s(t)=T_{{\rm on},A}+T_{{\rm on},B}+(k_1T_{{\rm on},A}+k_2T_{{\rm on},B})|\sin\omega t| \tag{3}$$

where $k_1=V_p/v_{\rm oa}$, $k_2=V_p/v_{\rm ob}$, and $T_s(t)=1/f_s(t)$.

From (1) and (3), the average input currents of subconverters A and B in a multiplexing cycle are

$$\begin{cases} i_{{\rm in,rec},A}(t)=\frac{\alpha T_{{\rm on},A}V_p|\sin\omega t|}{2L[1+\alpha+(\alpha k_1+k_2)|\sin\omega t|]} \\ i_{{\rm in,rec},B}(t)=\frac{T_{{\rm on},B}V_p|\sin\omega t|}{2L[1+\alpha+(\alpha k_1+k_2)|\sin\omega t|]} \end{cases} \tag{4}$$

where $\alpha=T_{{\rm on},A}/T_{{\rm on},B}$.

From (4), the input power of subconverters A and B in a half line cycle can be obtained as

$$\begin{cases} P_{{\rm in},A}=P_{o,A}=\frac{\int_0^\pi v_{\rm in,rec}(t)i_{{\rm in,rec},A}(t)d(\omega t)}{\pi}=\frac{\alpha\beta V_p^2T_{{\rm on},A}}{2\pi L} \\ P_{{\rm in},B}=P_{o,B}=\frac{\int_0^\pi v_{\rm in,rec}(t)i_{{\rm in,rec},A}(t)d(\omega t)}{\pi}=\frac{\beta V_p^2T_{{\rm on},B}}{2\pi L} \end{cases} \tag{5}$$

where

$$\begin{cases} \alpha=\frac{T_{{\rm on},A}}{T_{{\rm on},B}}=\sqrt{\frac{P_{o,A}}{P_{o,B}}} \\ \beta=\int_0^\pi\frac{\sin^2\omega t}{1+\alpha+(\alpha k_1+k_2)\sin\omega t}d(\omega t). \end{cases} \tag{6}$$

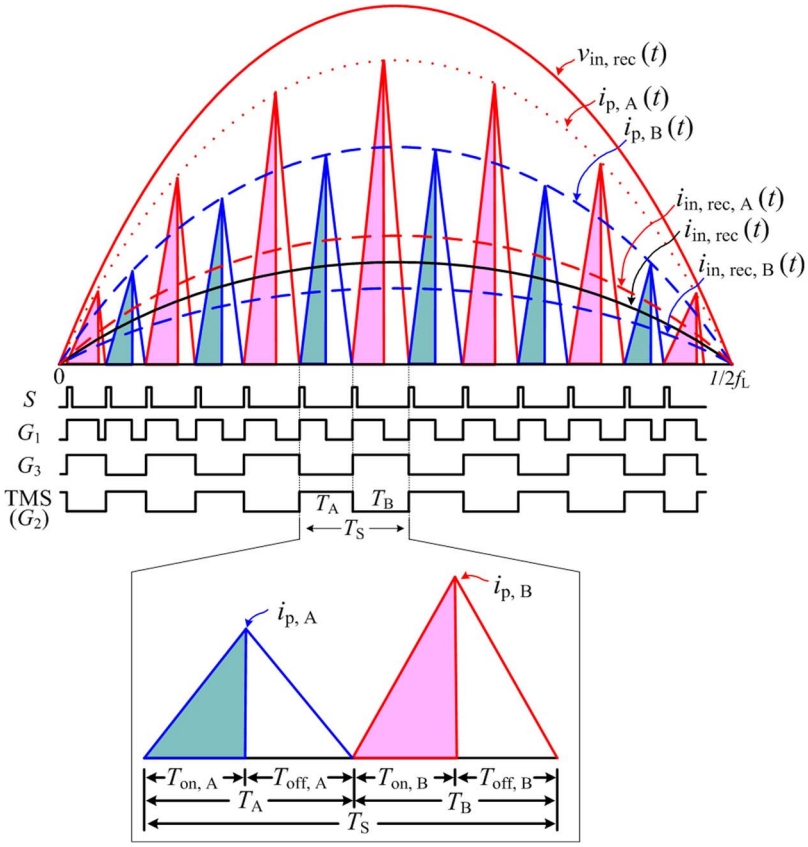

Fig. 3. Inductor current waveform and control sequence of the SIDO buck–boost PFC converter operating in CRM.

From (5), the turn-on time of subconverters A and B can be expressed as

$$\begin{cases} T_{\text{on},A} = \frac{2\pi L\sqrt{P_{o,A}P_{o,B}}}{\beta V_p^2} \\ T_{\text{on},B} = \frac{2\pi L P_{o,B}}{\beta V_p^2}. \end{cases} \tag{7}$$

From (4), the average input current of the CRM SIDO buck–boost PFC converter in a multiplexing cycle is

$$\begin{aligned} i_{\text{in,rec}}(t) &= i_{\text{in,rec},A}(t) + i_{\text{in,rec},B}(t) \\ &= \frac{(\alpha T_{\text{on},A} + T_{\text{on},B})V_p|\sin\omega t|}{2L\left[1+\alpha+(\alpha k_1+k_2)|\sin\omega t|\right]}. \end{aligned} \tag{8}$$

By substituting (7) into (8), the input current of the CRM SIDO buck–boost PFC converter can be expressed as

$$i_{\text{in,rec}}(t) = \frac{\pi(P_{o,A}+P_{o,B})|\sin\omega t|}{V_p\int_0^{\pi}\frac{\sin^2\omega t}{k+\sin\omega t}d(\omega t)\,(k+|\sin\omega t|)} \tag{9}$$

where

$$k = \frac{1+\alpha}{\alpha k_1 + k_2}. \tag{10}$$

According to (9), by using MATLAB, the normalized input currents of the CRM SIDO buck–boost PFC converter in a half line cycle with different k values are shown in Fig. 4. From

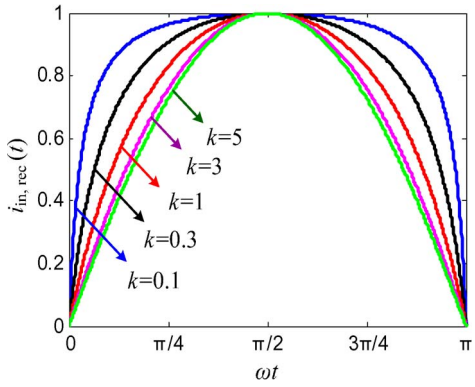

Fig. 4. Input current waveforms of the SIDO buck–boost PFC converter operating in CRM.

Fig. 4, it can be known that the distortion of the input current waveform will decrease with the increase of k.

Fig. 5 shows the harmonic spectrum of the input current. To compare with IEC 61000-3-2 class C limits, the vertical axis of Fig. 5 is the ratio of the harmonic current and the total input current, where $i_{\text{in}}(n)$ is the n-order harmonic content of the input current i_{in} and $\text{IEC}(n)$ represents the n-order harmonic current limit of IEC 61000-3-2 class C. It should be noted that it is easier to meet this standard limit for high-order harmonic currents (11th–19th). Therefore, only third to ninth harmonic currents are analyzed in this paper. It can be seen from Fig. 5 that, when $k > 0.19$, the third to ninth harmonic currents meet the IEC 61000-3-2 class C requirements.

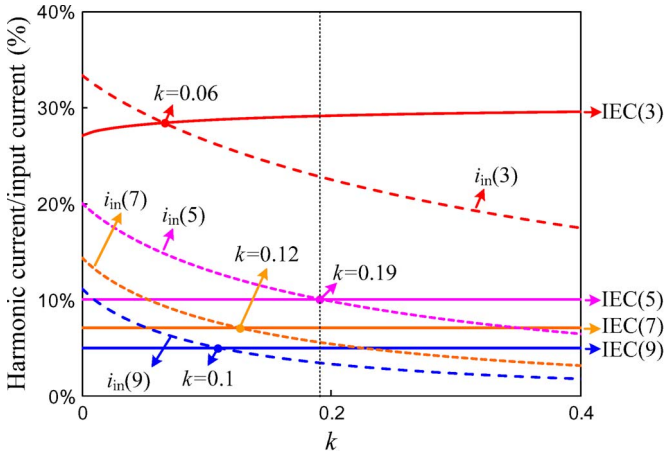

Fig. 5. Harmonic analysis of the input current.

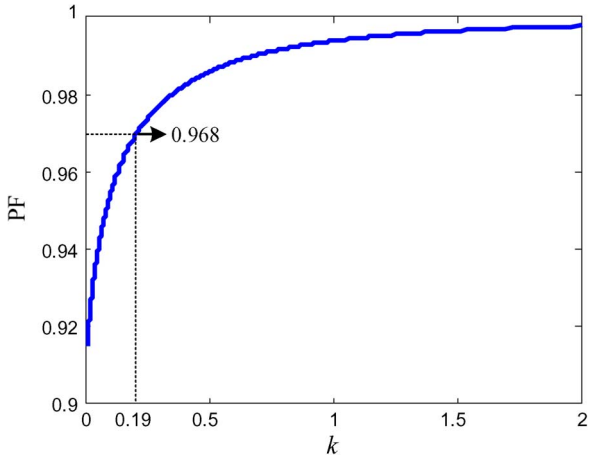

Fig. 6. Relationship between PF and k of the CRM SIDO buck–boost PFC converter.

B. PF Analysis

The PF of the CRM SIDO buck–boost PFC converter can be obtained as

$$\mathrm{PF}=\frac{\sqrt{2}\int_0^{\pi}\frac{\sin^2\omega t}{k+\sin\omega t}d(\omega t)}{\sqrt{\pi}\sqrt{\int_0^{\pi}\frac{\sin^2\omega t}{k^2+2k\sin\omega t+\sin^2\omega t}d(\omega t)}}. \tag{11}$$

By using MATLAB, Fig. 6 shows the PF of the CRM SIDO buck–boost PFC converter, from which it can be known that, with the increase of k, PF will be close to 1.

According to (10), k is determined by k_1, k_2, and α. Let $\lambda=\alpha^2$ be defined as the power ratio of $P_{o,A}$ and $P_{o,B}$; by using MATLAB, the relationships between PF, k_1, k_2, and λ are shown in Fig. 7. From Fig. 7, it can be known that, when k_1 and k_2 are the same, PF is independent of λ, while when k_1 and k_2 are not the same, PF will be affected by λ. As λ increases, PF will be seriously affected by k_1. It means that, if k_1 is equal to k_2, the PF of the CRM SIDO buck–boost PFC converter is similar to the single-output CRM buck–boost PFC converter and is only determined by k_1 or k_2. If k_1 is not equal to k_2, the PF of the CRM SIDO buck–boost PFC converter is

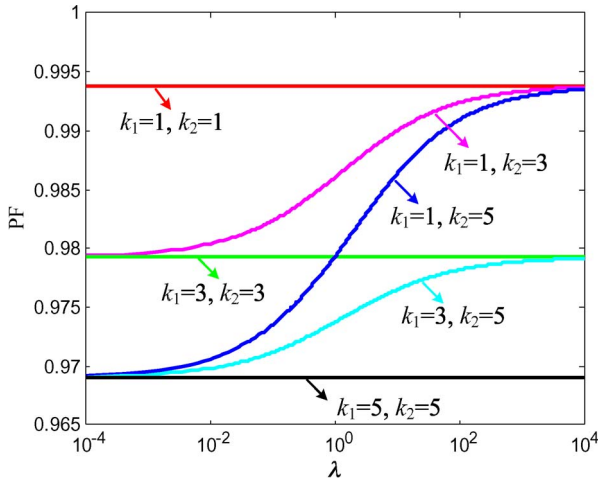

Fig. 7. Relationship between PF, k_1, k_2, and λ of the CRM SIDO buck–boost PFC converter.

not only determined by k_1 and k_2 but is also determined by λ. As λ increases, PF will be seriously affected by subconverter B.

C. Current Stress Analysis

By substituting (6) and (7) into (1), the peak inductor current of subconverters A and B can be described as

$$\begin{cases} i_{p,A}(t)=\frac{2\pi\sqrt{P_{o,A}P_{o,B}}}{\beta V_p^2}v_{\mathrm{in,rec}}(t) \\ i_{p,B}(t)=\frac{2\pi P_{o,B}}{\beta V_p^2}v_{\mathrm{in,rec}}(t). \end{cases} \tag{12}$$

It can be seen from (12) that $i_{p\_A}(t)$ and $ip\_B(t)$ are sinusoidal in a half line cycle. The peak inductor current will increase to its maximum when $|\sin\omega_L t|=1$, i.e.,

$$\begin{cases} i_{p,A,\max}=\frac{2\pi\sqrt{P_{o,A}P_{o,B}}}{\beta V_p} \\ i_{p,B,\max}=\frac{2\pi P_{o\_B}}{\beta V_p}. \end{cases} \tag{13}$$

Equation (13) demonstrates that $i_{p,A,\max}$ or $i_{p,B,\max}$ is a function of the amplitude of the input voltage, output power, and β. In other words, $i_{p,A,\max}$ and $i_{p,B,\max}$ will be fixed if the input and output are fixed.

D. Voltage Stress Analysis

As shown in Figs. 2 and 3, in steady state, the maximum reverse voltage of Q_1 can be described as

$$v_{Q_1,R,\max}=\begin{cases} V_p+|v_{\mathrm{oa}}|, & \mathrm{TMS}=1 \\ V_p+|v_{\mathrm{ob}}|, & \mathrm{TMS}=0. \end{cases} \tag{14}$$

From (14), it can be known that the reverse voltage of Q_1 is determined by TMS. When TMS $=1$, the reverse voltage of Q_1 is $V_p+|v_{\mathrm{oa}}|$, and when TMS $=0$, the reverse voltage of Q_1 is $V_p+|v_{\mathrm{ob}}|$. The reverse voltage of Q_1 is the same as that of the single-output buck–boost PFC if $v_{\mathrm{oa}}=v_{\mathrm{ob}}$.

When TMS $=0$, Q_2 will be turned off, and the maximum reverse voltage of Q_2 can be given as

$$v_{Q_2,R,\max}=\begin{cases} v_{\mathrm{ob}}-v_{\mathrm{oa}}, & |v_{\mathrm{oa}}|>|v_{\mathrm{ob}}| \\ 0, & |v_{\mathrm{oa}}|<|v_{\mathrm{ob}}|. \end{cases} \tag{15}$$

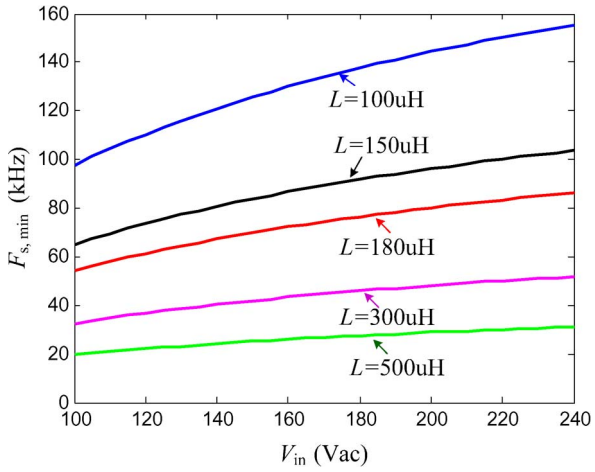

Fig. 8. Relationship of $F_{s\_\min}$ and L in condition of 100–240-Vac input voltage.

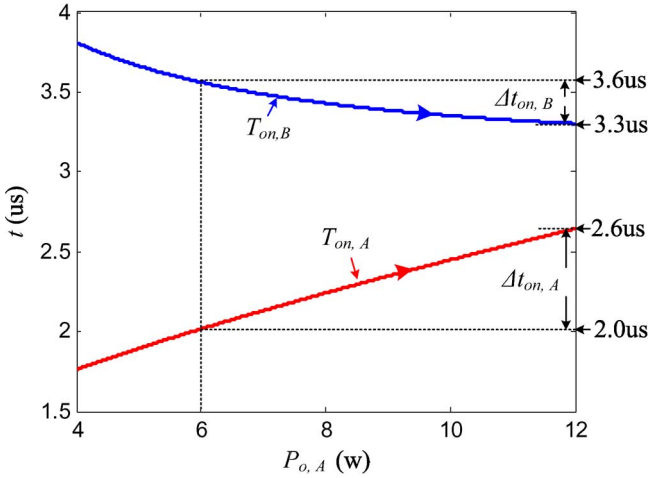

Fig. 9. $T_{\mathrm{on},A}$ and $T_{\mathrm{on},B}$ for different $P_{o,A}$ values at 100-Vac input voltage, with $i_{\mathrm{oa}} = 0.2$ A, $i_{\mathrm{ob}} = 0.25$ A, $R_b = 300\ \Omega$, and $L = 180\ \mu$H.

From (15), the maximum reverse voltage of Q_2 is affected by two outputs. If $|v_{\mathrm{oa}}| > |v_{\mathrm{ob}}|$, the maximum reverse voltage of Q_2 is $v_{\mathrm{ob}} - v_{\mathrm{oa}}$; otherwise, the maximum reverse voltage of Q_2 is zero. Equation (15) shows that the voltage stress of Q_2 is low. If $|v_{\mathrm{oa}}|$ is lower than $|v_{\mathrm{ob}}|$, Q_2 can be removed because the reverse voltage of Q_2 is equal to zero, which improves the efficiency and reduces control complexity. However, for constant current output loads, it cannot guarantee that $|v_{\mathrm{oa}}|$ is always lower than $|v_{\mathrm{ob}}|$. Thus, removing Q_2 will cause more serious cross-regulation when the voltage of each output is very close. Therefore, it is not suggested to remove Q_2. The reverse voltage of Q_3 is similar to that of Q_2.

E. Multiplexing Frequency Analysis

From (3), it can be known that the minimum multiplexing frequency of the CRM buck–boost PFC converter appears at the peak ($|\sin\omega_L t| = 1$) of the minimum input voltage and under full-load condition due to its CRM operating mode, i.e.,

$$F_{s,\min} = \frac{2\pi L(1+k_1)\sqrt{P_{o,A}P_{o,B}} + 2\pi L(1+k_2)P_{o,B}}{\beta V_p^2}. \tag{16}$$

Equation (16) demonstrates that $F_{s,\min}$ is a function of L if the input voltage and output voltage are fixed. Fig. 8 shows $F_{s,\min}$ for different L values under the input voltage range of 100–240 Vac, with $i_{\mathrm{oa}} = 0.2$ A, $R_a = 300\ \Omega$, $i_{\mathrm{ob}} = 0.25$ A, and $R_b = 300\ \Omega$. It can be known that, for the same input voltage, $F_{s,\min}$ will increase when L decreases, and for the same L, $F_{s,\min}$ will increase when the input voltage increases. High $F_{s,\min}$ will cause high switching loss of the power switch. As Q_1 will switch two times in a multiplexing cycle T_s, the input filter of the SIDO PFC converter operating in CRM should deal with more varied switching frequency in contrast with the single-output PFC operating in CRM. If the loads of the CRM SIDO buck–boost PFC are symmetrical, which means T_A and T_B are close, the input filter design is similar to that of the single-output PFC converter.

F. Cross-Regulation

For a multiple-output converter with each output regulated independently, if one output is affected by the variation of other outputs, transient cross-regulation occurs [18]. The CRM SIDO buck–boost PFC converter operates at varied switching frequency determined by $T_{\mathrm{on},A}$, $T_{\mathrm{on},A}$, k_1, and k_2 as described by (3). According to (6) and (7), $T_{\mathrm{on},A}$ and $T_{\mathrm{on},B}$ are interdependent and determined by k_1, k_2, $P_{\mathrm{on},A}$, and $P_{\mathrm{on},B}$ together. Fig. 9 shows $T_{\mathrm{on},A}$ and $T_{\mathrm{on},B}$ for different $P_{o,A}$ values at 100-Vac input voltage, with $i_{\mathrm{oa}} = 0.2$ A, $i_{\mathrm{ob}} = 0.25$ A, $R_b = 300\ \Omega$, and $L = 180\ \mu$H. It can be known that, when the load of subconverter A varies from 6 to 12 W, $T_{\mathrm{on},A}$ will change from 2.0 to 2.6 μs, and $T_{\mathrm{on},B}$ will also change from 3.6 to 3.3 μs, which means that, when the load of output A changes, $T_{\mathrm{on},A}$ and $T_{\mathrm{on},B}$ should be regulated at the same time by the corresponding control loops to ensure constant current regulation. Therefore, transient cross-regulation will occur if one of the output loads varies.

IV. Simulation and Experimental Verification

A 30.75-W prototype of the proposed CRM SIDO buck–boost PFC shown in Fig. 2 is built to verify the theoretical analysis. Each output current of the proposed CRM SIDO buck–boost PFC is constant. The prototype parameters are shown in Table I. From (10), coefficient k is 0.49 to 0.20, with input voltage varying from 100 to 240 Vac, which is higher than 0.19. Therefore, according to Fig. 5, the harmonic current in the prototype can meet the IEC limit. According to the analysis of Fig. 8, L is designed as 180 μH. L_f and C_f, which are used to provide switching noise attenuation and achieve low displacement angle between the input voltage and current [19], are seriously affected by $F_{s\_\min}$ at low input voltage. A low $F_{s\_\min}$ requires a low cutoff frequency of the input filter, which will increase the size of the filter. In this paper, L_f and C_f are designed as 1 mH and 220 nF considering a wide input voltage.

According to Fig. 2, low pass filters (R_{e1} and C_{e1}, and R_{e2} and C_{e2}) are used to filter the inductor freewheeling current sense signal on R_{s1} and R_{s2}. Due to low-frequency ($2f_L$) ripple on R_{s1} and R_{s2}, the time constant of these low-pass

TABLE I
CIRCUIT PARAMETERS OF THE SIDO BUCK–BOOST PFC CONVERTER

Variable	Definition	Value
v_{in}	Input voltage	100~240Vac
R_{a}	Rated load resistor of output A	300Ω
i_{oa}	Current of output A	0.2A
R_{b}	Rated load resistor of output B	300Ω
i_{ob}	Current of output B	0.25A
L	Inductor/Bobbin	180uH/RM8
Q_1	Power MOSFET	7N65
Q_2, Q_3	Multiplexing MOSFET	IRFR13N15D
D_1, D_2	Freewheeling diode	ES2J
L_{f},	Input filter inductor	1mH
C_{f}	Input filter capacitor	220nF
C_1, C_2,	Output filter capacitor	220uF

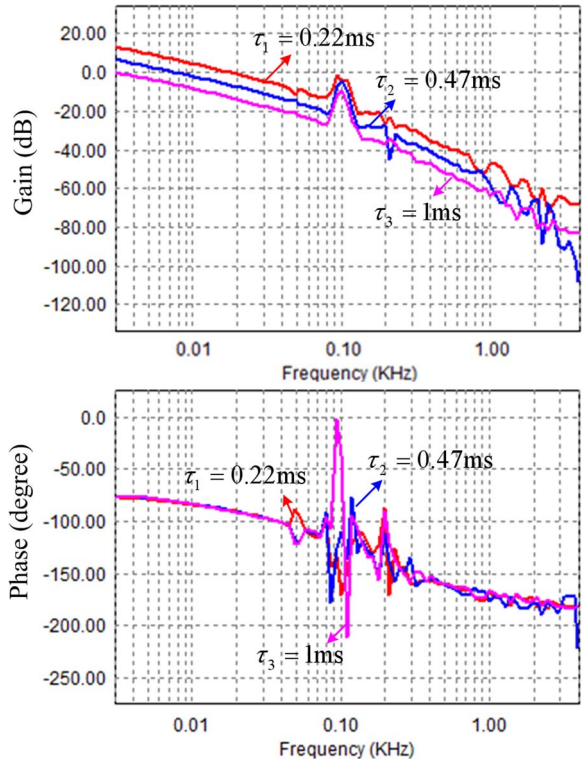

Fig. 10. Loop gain simulation results of subconverter A with $\tau = R_{e3}C_{e3}$.

filters should be lower than $(1/2f_L)$. The capacitance and resistance of these two filters are designed as 100 nF and 120 kΩ in this prototype. Two compensators (Op1, R_{e3} and C_{e3}; and Op2, R_{e4} and C_{e4}) are applied to achieve a sufficient phase margin and a low bandwidth for PFC. Fig. 10 shows the loop gain of the Psim simulation results at 100 Vac for subconverter A with different compensation parameters (τ_1, τ_2, and τ_3) by using the circuit parameters shown in Table I. It can be observed that, when time constant $\tau = R_{e3}C_{e3}$ is lower than 0.22 ms, the phase margin is approximately 90° when the compensator is applied. The bandwidth will be lower than 20-Hz, which can ensure an acceptable PFC requirement, but this low bandwidth severely affects the control loop dynamics [20], [21]. A poor transient performance will also cause a poor transient cross-regulation performance. Therefore, the control loop design is a

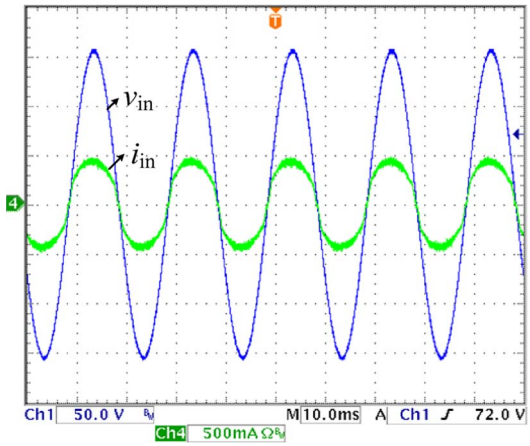

Fig. 11. v_{in} and i_{in} waveforms of the SIDO buck–boost PFC converter at 110-Vac input.

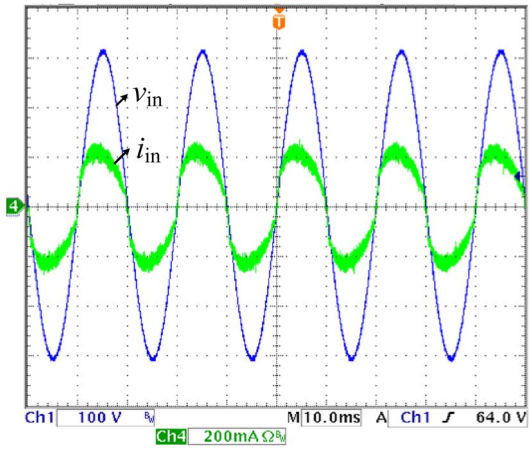

Fig. 12. v_{in} and i_{in} waveforms of the SIDO buck–boost PFC converter at 220-Vac input.

tradeoff between PF and transient performance. The simulation result of the transfer function with 50-Hz ac input shows fluctuations at frequencies around 100-Hz. This fluctuation is due to the combined effects of 100-Hz switching at the bridge rectifier and the 100-Hz ripple in the output voltage. In order to make the design simple, the same compensation parameters are applied in two compensation networks, and the compensation parameters are designed as $R_{e3} = R_{e4} = 10$ kΩ and $C_{e3} = C_{e4} = 47$ nF considering high PF and acceptable transient performance, i.e., $\tau = 0.47$ ms.

The steady-state input current waveforms of the CRM SIDO buck–boost PFC converter at rated output power are shown in Figs. 11 and 12. From Figs. 11 and 12, it can be known that input current i_{in} is in phase with input voltage v_{in}. The PFC function is achieved.

Fig. 13 shows the PF of the prototype. It shows that PF is higher than 0.95 within the wide input voltage range from 100 to 240 Vac.

Harmonic currents (up to 15th) at 110- and 220-Vac input voltage are shown in Fig. 14. It shows that the CRM SIDO buck–boost PFC prototype has lower harmonic input current contents and can meet the IEC 61000-3-2 class C limit with large margins. The THDs of the prototype are 13.88% and 16.41% in 110- and 220-Vac input voltage.

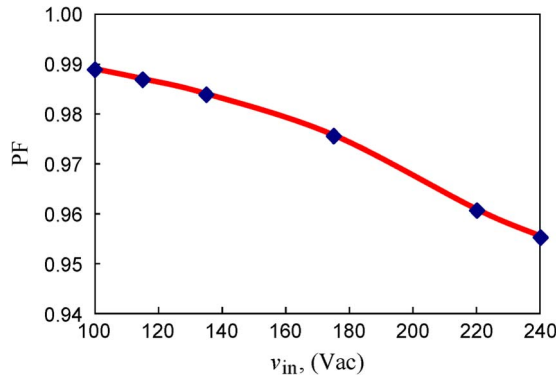

Fig. 13. PF of the SIDO buck–boost PFC converter.

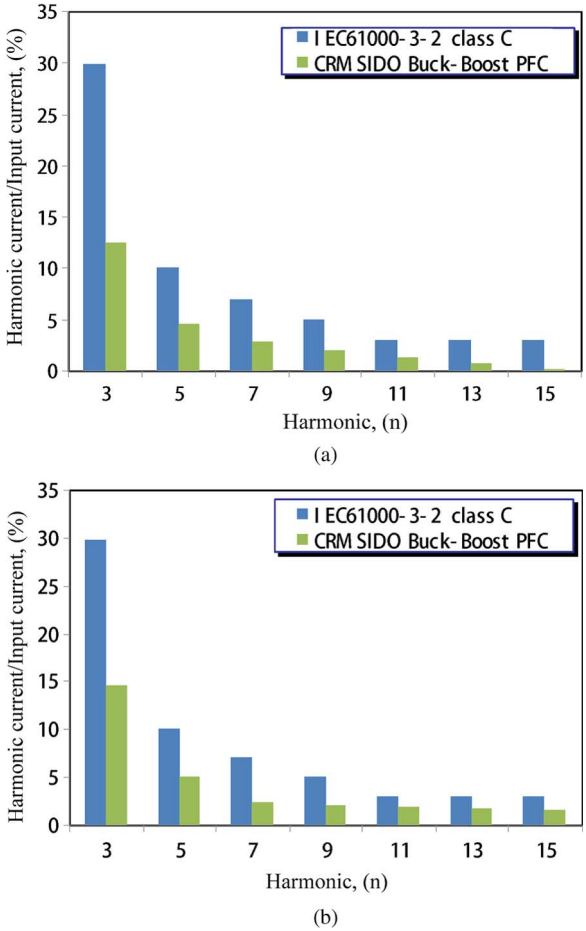

Fig. 14. Harmonic test results of input current $i_{\rm in}$. (a) 110 Vac. (b) 220 Vac.

The inductor current at peak input voltage of a line cycle is shown in Fig. 15. It can be known from Fig. 15 that the multiplexing cycle is varied due to CRM operation. It shows that the multiplexing cycle is 18 μs ($F_{s\_\min} = 55.5$ kHz) at 110-Vac input voltage, and 13 μs ($F_{s\_\min} = 76.9$ kHz) at 220-Vac input voltage, respectively. The $F_{s\_\min}$ values obtained from Fig. 8 are 58 and 83 kHz at 110- and 220-Vac input voltage, respectively. The difference between the experimental results and the theory analysis results is mainly due to the efficiency and ZCD circuit delay.

The transient cross-regulation performance is shown in Fig. 16. From Fig. 16, when the load of subconverter A varies

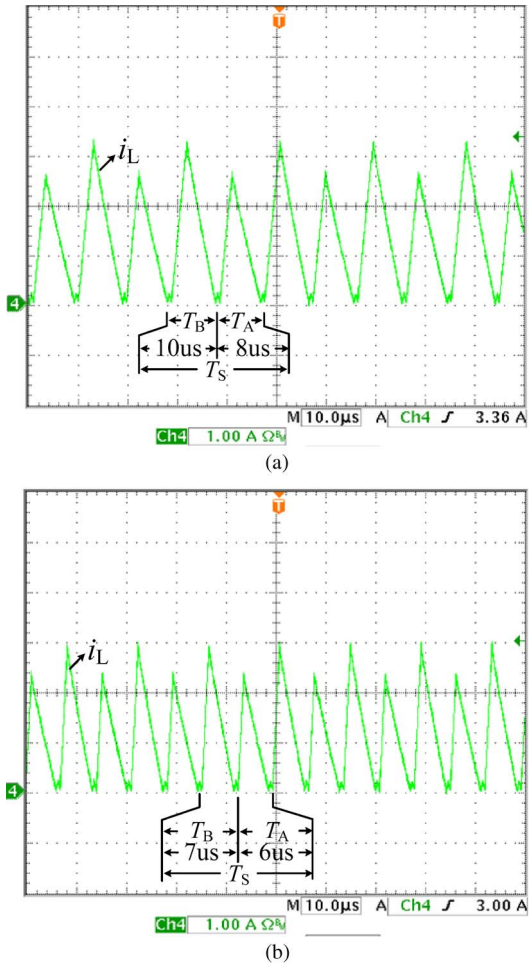

Fig. 15. i_L waveforms of the SIDO buck–boost PFC converter in CRM. (a) 110 Vac. (b) 220 Vac.

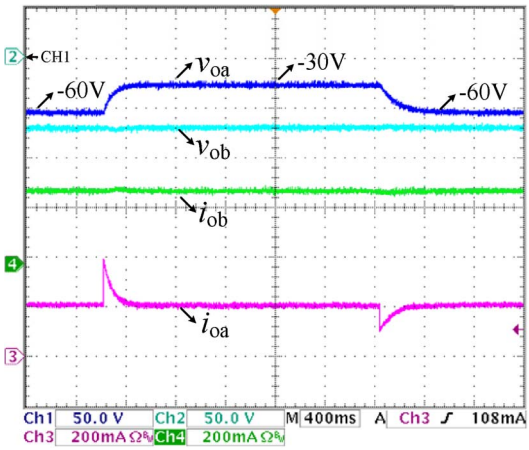

Fig. 16. Output current and output voltage response of the CRM prototype under the load variation of output A load between 12 and 6 W.

between 12 and 6 W, output current overshoot and undershoot of subconverter A appear because of the low bandwidth of the control loop; however, the current overshoot and undershoot of subconverter B under output A load variation are not significant. The transient cross-regulation of the CRM SIDO buck–boost PFC is not significant because of the low bandwidth of the control loop.

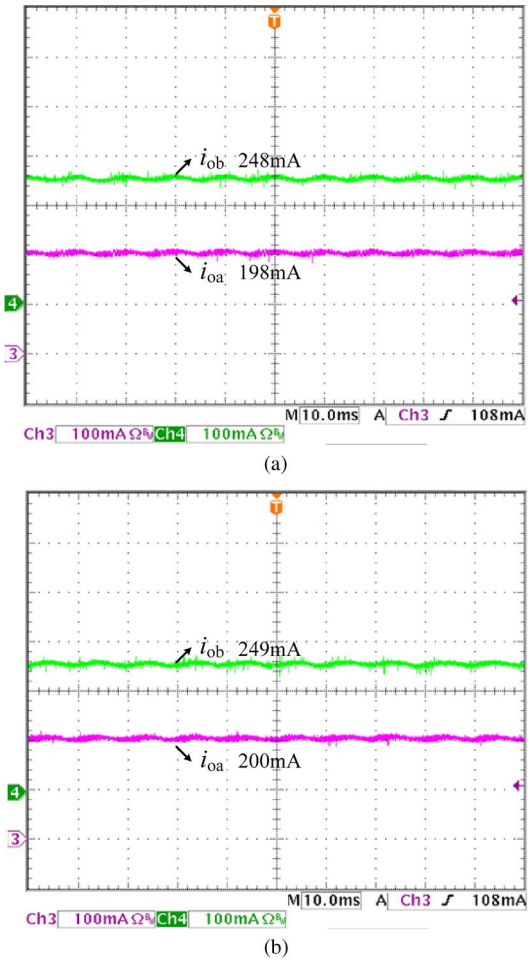

Fig. 17. Output current waveforms of the CRM SIDO buck–boost PFC converter. (a) 110 Vac. (b) 220 Vac.

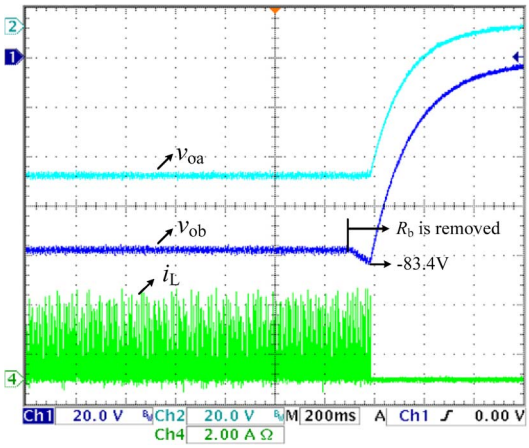

Fig. 18. Output B varies from full load to no load with $i_{oa} = 0.2$ A and $v_{oa} = 60$ V.

Fig. 17 shows the output current waveforms of the CRM SIDO buck–boost PFC converter. From Fig. 17, it can be known that two constant output currents can be well regulated.

Fig. 18 shows the experimental results under severe load unbalance condition that output A is under full load and output B varies from full load to no load. With output B at no load, i.e., when load resistor R_b is removed, the output current sense signal is extremely low, and the error voltage (v_{e2}) of output B will reach its maximum value. Then, the output voltage v_{ob} will increase continuously. This is an unsafe operation if without protection. When v_{ob} increases to 83.4 V, OVP will be triggered. The converter will stop to work unless the ac input voltage resets. This is an extreme load unbalance case. Increasing the load resistance may also trigger this protection.

TABLE II
OUTPUT CURRENT OF THE SIDO BUCK–BOOST PFC CONVERTER

Output (mA)	v_{in} (Vac)					
	100	110	135	175	220	240
i_{oa}	197.7	198.2	199.0	199.3	200.3	200.7
i_{ob}	248.0	248.0	248.3	248.8	249.3	249.6

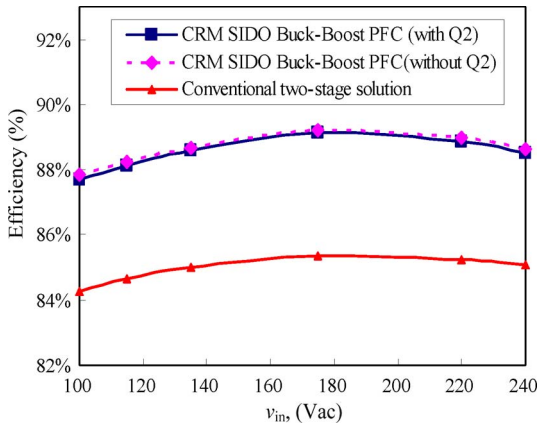

Fig. 19. Efficiency curves of the SIDO buck–boost PFC converter and conventional two-stage converter.

Table II illustrates the test results of the output currents. It shows good performance of output current regulation under wide input voltage from 100 to 240 Vac.

Fig. 19 shows the efficiency curves of the SIDO buck–boost PFC converter and conventional two-stage converter. In the conventional two-stage converter as shown in Fig. 1, the PFC preregulator is a CRM buck–boost PFC topology, and output voltage v_{bus} is set to 80 V. The dc-to-dc regulator is the CCM buck converter. As shown in Table I, the output voltage of subconverter A is 60 V, which is lower than the output voltage of subconverter B (75 V). As shown in Fig. 19, the efficiency values for the cases with Q_2 and without Q_2 are very close, which indicates that the power loss of Q_2 is very small due to low R_{dson} (0.18Ω) and zero-current-switching operation. Low voltage stresses of Q_2 and Q_3 make it easier to choose low-R_{dson} MOS. The maximum efficiency of the CRM buck–boost PFC prototype with Q_2 is 89.04%, and the maximum efficiency of the conventional two-stage converter is 85.35%. Therefore, the proposed SIDO buck–boost PFC converter benefits with high efficiency advantage due to single-stage power conversion.

V. CONCLUSION

A SIDO buck–boost PFC converter operating in CRM has been proposed in this paper. Detailed control strategy analysis and design considerations have been presented. Each output can be regulated independently in this converter by multiplexing a single inductor. Compared with conventional two-stage

multiple-output ac/dc converters, the proposed single-stage multiple-output ac/dc converter benefits from significant overall cost saving, small size, and light weight of the device. Experimental results have been presented to verify the analysis results and to demonstrate the advantage of the proposed converter. Although only the dual-output converter is discussed in detail in this paper, the proposed converter can be easily extended to realize SIMO PFC converters with different topologies to fulfill different system requirements.

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