Front-End Converter With Integrated PFC and DC–DC Functions for a Fuel Cell UPS With DSP-Based Control

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Abstract—This paper presents the development of a boost converter with integrated power factor correction (PFC) and dc–dc functions for a proton exchange membrane fuel cell (PEMFC) uninterruptable power supply (UPS). Through the use of a passive resonant soft-commutation cell, which besides providing improvements in efficiency and reduced electromagnetic interference, produces a naturally controlled supercapacitor charger circuit. Supercapacitors are employed in order to provide a proper startup of the PEMFC and to improve its dynamic response. The control strategy is implemented using a digital signal processor and is based on the average current control method for sinusoidal input current imposition ensuring, therefore, a high input power factor and low harmonic distortion of current. The main features of the proposed solution are the use of a PEMFC as an energy storage system, which replace the battery banks commonly used in UPS systems, eliminating the common drawbacks related to working life and maintenance issues, and the use of a front-end converter with integrated PFC and dc–dc functions eliminating the necessity of using an additional and dedicated dc–dc converter for the PEMFC. During power failure or even in conditions of severe voltage sags on the ac mains, the PEMFC is activated assuring the continuous power supply to the electronic load connected to the dc link. In this paper, the authors present the full study description including experimental results that corroborate with the theory herein presented.

Index Terms—Digital signal processor (DSP), fuel cell, power factor correction, UPS.

NOMENCLATURE

E_o Fuel cell's maximum theoretical voltage at open circuit (V).
E_N Fuel cell's reversible voltage no-load (V).
T Temperature in Kelvin (K).
R Universal gas constant (8314 JK/mol).
F Faraday constant (96487 C).
P_{H_2} Hydrogen pressure (atm).
P_{O_2} Oxygen pressure (atm).
C_{O_2} Oxygen concentration (mol/cm^3).
V_Ω Ohmic losses (A).
R_s Membrane and electrodes resistance (Ω).
L Auxiliary inductance for the model (H).
L_r Resonant inductance (H).
C Cell's equivalent capacitance (F).
C_r Resonant capacitor (F).
i Fuel cell's current (A).
i_L Fuel cell's maximum current (A).
i_{Lb} Boost inductor's current (A).
i_L Resonant inductor's current (A).
V_{activ} Activation losses (V).
V_{conc} Concentration losses (V).
V_{cell} Cell's output voltage (V).
V_{in} Input voltage (V).
V_o Output voltage (V).
V_{Lr} resonant inductor's voltage (V).
V_{Cr} Resonant capacitor's voltage (V).
V_{Csc} Supercapacitor's voltage (V).
n Reagent moles number.
n_c Number of cells in stack.
ξ_n Fuel cell's coefficients.
Δt_n Stages of operation periods.
T_s Switching period.
ω_0 Resonant frequency.
D Duty cycle.
α Normalized current.

I. INTRODUCTION

DUE to the remarkable technological development observed in recent years, several industrial processes have begun to depend entirely on the use of electronic devices. In this context, it has become inadmissible the occurrence of interruptions in power supply regarding various fields of work and services, among which one can cite telecommunications systems, devices employed in hospital emergency rooms, and flight control systems [1]. In this sense, many companies invest in research studies, which focus on the development of solutions that avoid energy supply interruptions to their systems. The devices manufactured for this purpose were denominated as uninterruptible power supply (UPS), which commonly present a high power factor (HPF) front-end converter followed by a dc–ac or dc–dc stage (depending on the application) and uses rechargeable batteries such as sealed lead-acid or nickel cadmium, which
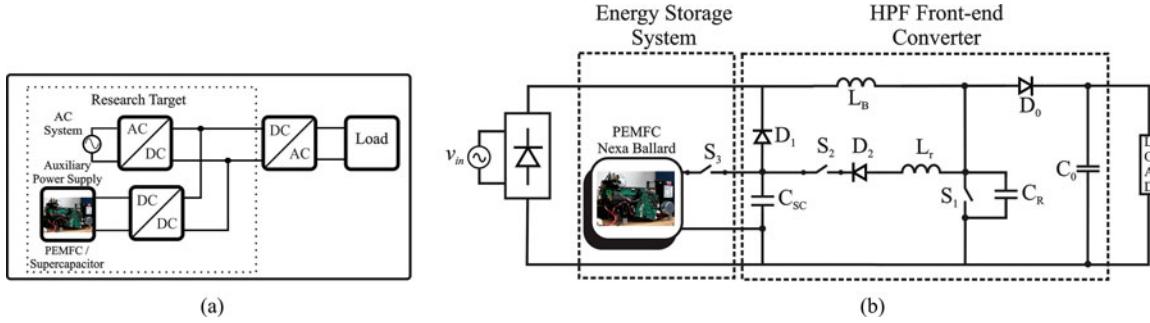
Fig. 1.   (a) Block diagram of an ordinary online UPS system with PEMFC. (b) Proposed integrated online PFC stage for UPS system with PEMFC.

use toxic heavy metals such as cadmium, mercury, and lead. In addition, the unpredictable working life along with limited charge–discharge cycles increase the cost concerning maintenance and replacement. On the other hand, fuel cells (FCs) are emerging as a reliable power source, since it is inherently clean and presents very high overall efficiency (40–60%) [2], [3]. Unlike batteries, performance characteristics of the FCs such as great tolerance to high temperatures (from –40 °C to +50 °C), lower maintenance requirements, scalability, and higher power density, make them a very attractive alternative to UPS systems [4]–[10].

Due to the fact that FCs do not have the capacity to respond immediately to fast load changes or to startup as soon as it is required, supercapacitors can be used in conjunction with the FC [11]. It is important to highlight that they only supply the energy for short periods, which is necessary to allow the FC to achieve steady state. One can also conclude that they are also very attractive for battery storage systems, since the batteries provide energy only during longer interruptions improving, therefore, their working life [12]–[19].

In this context, this paper presents a single-phase HPF front-end converter suitable for an online UPS system using a proton exchange membrane fuel cell (PEMFC) as an energy storage system. Different to ordinary FC UPS as shown in Fig. 1(a) and also observed in [4]–[6], the proposed system, shown in Fig. 1(b), consists of a boost converter with integrated PFC and dc–dc functions, so a dedicated dc–dc converter for the connection of the PEMFC is not needed. A self-resonant zero-current and zero-voltage-switching pulse width modulated cell (SR-ZCS-ZVS-PWM) [20], [21] is used, therefore, besides the soft commutation of switches S_1 (main) and S_2 (auxiliary), the charge circuit for the supercapacitor bank is also ensured.

A supercapacitors bank is able to operate without hindrance at 60% to 100% of rated voltage. Normally, a dedicated control is needed to achieve this condition, such as the smoothing control method presented in [22] or the sliding mode control shown in [23]. In this context, one must emphasize that in the proposed system there is no need for a dedicated energy storage control on the supercapacitors. The power diode D_1, which connects the supercapacitors bank with the boost inductor L_B, provides the path for the transference of the stored energy to the output capacitor when the main switch S_1 is OFF and diode D_0 is forward biased, therefore, controlling the voltage level across the supercapacitors terminals in a natural flowing manner. The

amount of energy processed by the SR-ZCS-ZVS-PWM commutation cell is transferred to the supercapacitors bank every switching cycle. In steady state, the supercapacitor supplies energy to the load only when the input ac voltage is lower than its terminal voltage and, hence, diode D_1 is forward biased. Under a power failure condition on the ac grid, the switch S_3 is turned ON and the supercapacitors provide the necessary condition for the startup of the PEMFC.

The control technique for sinusoidal input line current imposition and for extracting the necessary energy from the PEMFC during power failure at the mains supply, and for controlling the dc-link voltage in both situations, made use of the digital signal processor (DSP) F28335 from Texas Instruments.

In summary, the main features of the proposed solution can be outlined as follows:

1) there is no need to use an external battery bank, which has a short working life and low scalability, as well as an associated charger circuit;
2) there is no need to use a dedicated dc–dc converter for the PEMFC which, thus, reduces cost;
3) the use of nondissipative switching cell improves the overall efficiency and can reduce electromagnetic interference (EMI);
4) the supercapacitors bank is continuously connected to the system, which guarantees zero switching delay between the ac power supply and the startup of the PEMFC;
5) the commutation energy is used for charging the supercapacitors, which presents a higher charge–discharge cycle when compared to batteries [24]–[27];
6) the supercapacitors bank naturally operates under 60% to 100% of rated voltage, so there is no need to implement a dedicated control technique to assure the working life of the supercacitors, making the proposed system simple.

II. PROPOSED SYSTEM

A. Boost Converter With Integrated PFC and DC–DC Functions

The proposed boost converter is used as a preregulator and employs a nondissipative switching cell, which ensures the ZVS turning-on and turning-off of the main switch S_1, and the ZCS turning-on and ZVS-ZCS turning-off of the auxiliary switch S_2. The power diode D_1 connects the supercapacitor bank with the

Fig. 2. On–Off SR-ZCS-ZVS-PWM cell.

Fig. 3. State-space phase of the proposed converter.
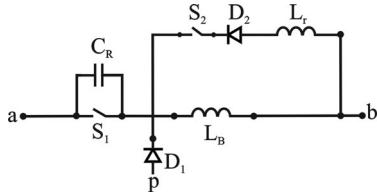
system and it is only forward biased when the input voltage is lower than the supercapacitor voltage or when the ac system is absent. In this situation, the FC supplies the load.

The system employs a DSP-based control, which is responsible for the control of the output voltage and sinusoidal input current imposition through the conventional average current control method, similar to that presented in [28].

B. Soft Switching Cell

In any conventional switched converter, the switches are controlled to turn-on and turn-off with load current. This causes high levels of voltage and/or current transients during switching resulting in elevated commutation losses. It is noteworthy that the commutation losses increase linearly by increasing the switching frequency.

It is necessary to increase the switching frequency of the static converter in order to reduce the size and weight of passive elements, for example, inductors and capacitors, which increase the commutation losses. Consequently, the overall efficiency of the structure is reduced [29]–[31]. Another problem of high frequency switching is the generation of EMI and radio interference due to abrupt variations of voltage and current that follows the turn-on and turn-off of the switches. To avoid these problems and obtain a soft switching, one of the strategies used is the implementation of quasi-resonant converters [30]. In these converters, the turn-on and turn-off of switches occurs under zero voltage (ZVS) and/or under zero current (ZCS).

The proposed soft-commutation cell in Fig. 2 was developed to operate at fixed frequency deploying MOSFETs as active switches and to provide both ZVS and ZCS turn-on and turn-off of the active semiconductors. One observes that one resonant inductor (L_r), one diode (D_2), two switches (S_1 and S_2), and one resonant capacitor (C_R) make up the presented cell. Fig. 3 shows the state-space phase of the proposed converter.

C. Principle of Operation

Considering a single switching period, the proposed PFC converter can be illustrated through seven stages of operation, as shown in Fig. 4(a) to (g).

To simplify the analysis, the output voltage V_0 is considered constant. The switching frequency is much higher than the ac line and the input voltage V_{in} is constant during one switching period.

Mode 1 (t_0–t_1): First, the converter has output voltage greater than input voltage and with its energy being transferred to the load. At the time t_0, the switch S_2 had been turned ON in ZCS, D_1
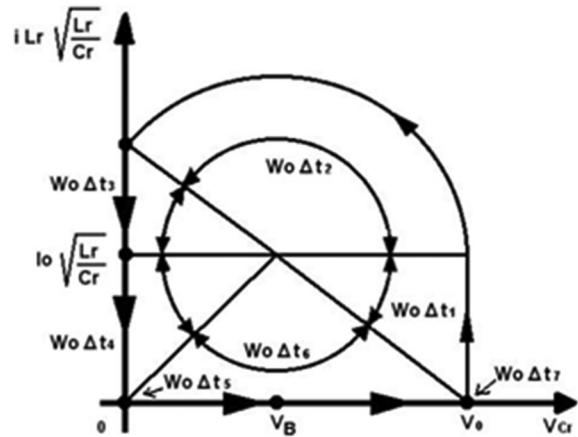
and D_0 are forward biased. With S_2 turned ON, the input current is diverted from the inductor L_B to the resonant inductor L_r; thus, the current I_{Lr} starts to increase and the current on diode D_0 decreases linearly through the action of V_0 in the resonant capacitor C_R. This operation stage ends when I_{Lr} reaches the input inductor current I_0 and the diode D_0 reaches zero. This operation stage is portrayed in Fig. 4(a).

Mode 2 (t_1–t_2): This stage can be described as the resonant stage. At the time t_1, diodes D_1 and D_0 are reversed biased. The I_{Lr} continues to increase and its values comprise of the sum from input inductor current I_0 plus the resonant capacitor current I_{Cr}. As D_1 is reversed biased, the current I_{Lr} flows through the supercapacitor C_{SC}; this stage ends when the resonant capacitor discharges completely. This operation stage is portrayed in Fig. 4(b).

Mode 3 (t_2–t_3): At the time t_2, the current I_{Lr} decreases linearly through the supercapacitor and the intrinsic diode of switch S_1, since the diodes D_1 and D_0 are reversed biased. This stage ends when the current I_{Lr} reaches the value of the input inductor current I_0. This stage of operation is portrayed in Fig. 4(c).

Mode 4 (t_3–t_4): At the time t_3, switch S_1 is turned ON in ZVS. The current I_{Lr} decreases and current I_{S1} increases linearly through the action of C_{SC} and V_{in}. Switch S_2 is still turned ON and the diodes D_1 and D_0 are reversed biased. This stage ends when current I_{Lr} reaches zero and the current I_{S1} reaches I_0. This operation stage is portrayed in Fig. 4(d).

Mode 5 (t_4–t_5): At the time t_4, the current I_{S1} reaches I_0 and the switch S_2 is turned OFF in ZCS. The diodes D_0, D_1, and D_2 are reversed biased and the C_{SC} is not storing energy. This stage ends when the switch S_1 is turned OFF in ZVS. This operation stage is portrayed in Fig. 4(e).

Mode 6 (t_5–t_6): At the time t_5, switch S_1 is turned OFF in ZVS. The C_r voltage increases linearly. The diodes D_0, D_1, and D_2 are reversed biased. This stage ends when the C_r voltage reaches V_0. This operation stage is portrayed in Fig. 4(f).

Mode 7 (t_6–t_7): At the time t_6, the C_r voltage reaches V_0 and the diode D_0 is forward biased. The current I_0 flows through the D_0 and the load receives energy. This stage ends when the
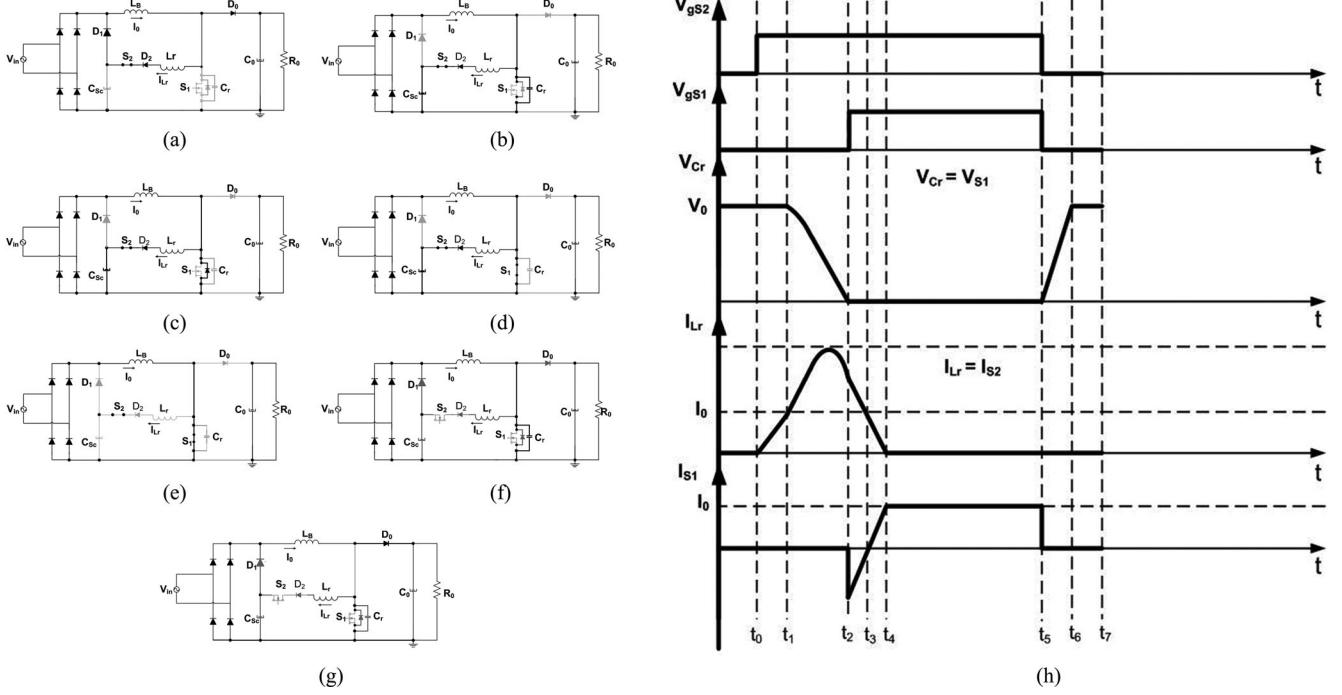
Fig. 4. Equivalent circuits: (a) Stage 1, (b) Stage 2, (c) Stage 3, (d) Stage 4,(e) Stage 5, (f) Stage 6, (g) Stage 7, and (h) theoretical switching waveform.

switch S_2 is turned ON in ZCS, restarting the entire cycle. This operation stage is portrayed in Fig. 4(g).

All operation stages were described in detail in this section. All active switches operate with soft commutation which is assured by the application of the ON–OFF SR-ZCS-ZVS-PWM cell. Fig. 4(h) shows the relevant theoretical waveforms of the proposed converter, which is related to the operating stages described above.

D. Mathematical Analysis

Performing an analysis of the operating stages portrayed in Fig. 4, the following relevant expressions can be obtained. By definition we have

$$\omega_0 = \sqrt{\frac{1}{L_r C_r}} \qquad (1)$$

$$\alpha = \frac{I_{\text{LB}}}{(V_0 - V_{\text{in}})} \sqrt{\frac{L_r}{C_r}} \qquad (2)$$

$$K = \frac{V_{C\text{sc}}}{V_0 - V_{C\text{sc}}} \qquad (3)$$

$$K_1 = \frac{V_{\text{in}}}{V_0 - V_{\text{in}}} \qquad (4)$$

$$K_2 = \frac{V_{C\text{sc}}}{V_{\text{in}}}. \qquad (5)$$

From stage 1, one obtains

$$I_{Lr}(t) = \frac{V_0 - V_{\text{in}}}{L_r}.t \qquad (6)$$

$$\Delta t_1 = \frac{\alpha}{\omega_0}. \qquad (7)$$

From stage 2, one obtains

$$V_{Lr} = V_{C\text{sc}} + V_{Cr} \qquad (8)$$

$$V_{Cr}(t) = (V_0 - V_{C\text{sc}}) \cos \omega_0 t + V_{C\text{sc}} \qquad (9)$$

$$\sqrt{\frac{L_r}{C_r}} I_{Lr}(t) = (V_0 - V_{C\text{sc}}) \sin \omega_0 t + \sqrt{\frac{L_r}{C_r}} I_{\text{LB}}. \qquad (10)$$

When $t = \Delta t_2$, $V_{Cr}(t) = 0$

$$I_{\text{Lr}}(t_2) = \sqrt{\frac{C_r}{L_r}} (V_0 - V_{C\text{sc}}) \sin \omega_0 \Delta t_2 + I_{LB} \qquad (11)$$

$$\Delta t_2 = \frac{1}{\omega_0} \left[\pi - \cos^{-1} K \right]. \qquad (12)$$

From stage 3, one obtains

$$I_{Lr}(t) = -\frac{V_{C\text{sc}}}{L_r} t + I_{Lr}(t_2). \qquad (13)$$

When $t = \Delta t_3$, $I_{Lr}(t) = I_{LB}$

$$\Delta t_3 = \frac{1}{\omega_0} \frac{\sqrt{1 - K}}{K}. \qquad (14)$$

From stage 4, one obtains

$$V_{Lr} = V_{C\text{sc}} \qquad (15)$$

$$I_{Lr}(t) = -\frac{V_{C\text{sc}}}{L_r} t + I_{LB}. \qquad (16)$$

When $t = \Delta t_4$, $I_{Lr}(t) = 0$

$$\Delta t_4 = \frac{L_r I_{LB}}{V_{C\text{sc}}} = \frac{\alpha}{K \omega_0}. \qquad (17)$$
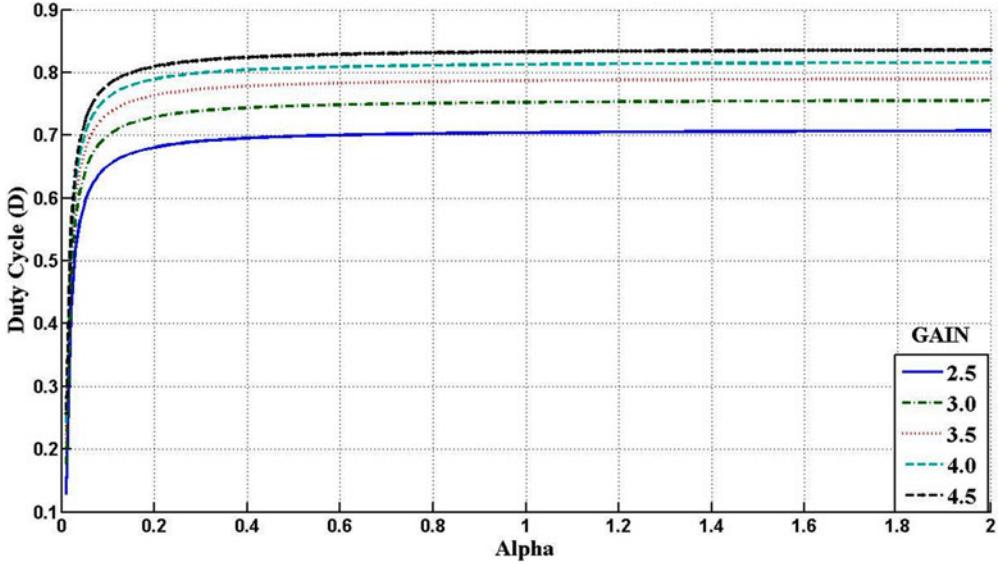
Fig. 5.   Static gain of the proposed converter.

From stage 5, one obtains

$$I_{Lr}(t) = 0 \tag{18}$$

$$V_{Cr}(t) = 0 \tag{19}$$

$$\Delta t_5 = \frac{1}{\omega_0} \left[T_S D \omega_0 - \frac{\sqrt{1-K}}{K} - \frac{\alpha}{K\omega_0} \right]. \tag{20}$$

From stage 6, one obtains

$$I_{Lr}(t) = 0 \tag{21}$$

$$V_{Cr}(t) = \frac{I L_B}{C_r} t. \tag{22}$$

When $t = \Delta t_6$, $V_{Cr}(t) = 0$

$$\Delta t_6 = \frac{V_0 C_r}{I_{LB}} = \frac{1}{\omega_0} \frac{K+1}{\alpha}. \tag{23}$$

From stage 7, one obtains

$$I_{Lr}(t) = 0 \tag{24}$$

$$V_{Cr}(t) = 0 \tag{25}$$

$$\Delta t_7 = T_S - (\Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 + \Delta t_5 + \Delta t_6). \tag{26}$$

The operating stages mathematical analysis of the proposed power converter gives rise to the static gain equation given by

$$G = \frac{V_0}{V_{\text{in}}} = \frac{1 + \frac{K_2}{T_s \omega_0} \left[\frac{\sqrt{1-K}}{K} + \pi - \cos^{-1} K \right]}{1 - \frac{K_1 + 1}{2\omega_0 \alpha T_s} - D}. \tag{27}$$

Solving (1) for different load values (α) and duty ratio values (D), one obtains the set of curves shown in Fig. 5. Thus, it can be seen that the proposed converter is an overlay of a conventional boost converter and the quasi-resonant converter. The proposed structure operates as a quasi-resonant converter for low loads

and as a PWM converter for high loads, without presenting any limitations as observed in the operation of conventional PWM converters and others that use the nondissipative switching technique.

E. Modeling of the PEMFC and Supercapacitor

The PEMFC model is presented in Fig. 6(a) and it represents the chemical reactions that occur in a PEMFC, by means of voltage sources that are dependent on the PEMFC's current and parameters, with the possibility of changing the number of cells for the stack voltage adjustment [32]. The model can be divided into no-load voltage (E_N), ohmic losses (V_Ω), activation losses (V_{activ}), and concentration losses (V_{conc}). The main equations representing each voltage source are presented as follows.

The no-load voltage of a single cell is given by (28) and depends on temperature (T), the maximum theoretical open-circuit voltage of a cell (E_0), the hydrogen pressure (P_{H_2}) and oxygen pressure (P_{O_2}). In (28), R is the universal gas constant (8314 JK/mol) and F is the Faraday constant (96487 C)

$$E_N = E_0 + \frac{RT}{2F} \left[\ln(P_{\text{H}_2}) + \frac{1}{2} \ln(P_{\text{O}_2}) \right]. \tag{28}$$

The ohmic losses that represent the internal FC resistance, is given by (29) and depends on output FC current (i), as well as the membrane and electrodes resistance (R_s)

$$V_\Omega = R_{\text{S}} i. \tag{29}$$

The activation losses are related to the kinetic processes that occur at the electrodes and are given by (30) where ξ_i represents coefficients that are dependent on the FC's modeling, and C_{O2} represents the oxygen concentration

$$V_{\text{activ}} = \xi_1 + \xi_2 T + \xi_3 T \ln(C_{\text{O2}}) + \xi_4 T \ln(i). \tag{30}$$

The concentration losses represent the establishment of a concentration gradient of the reactant that is consumed at
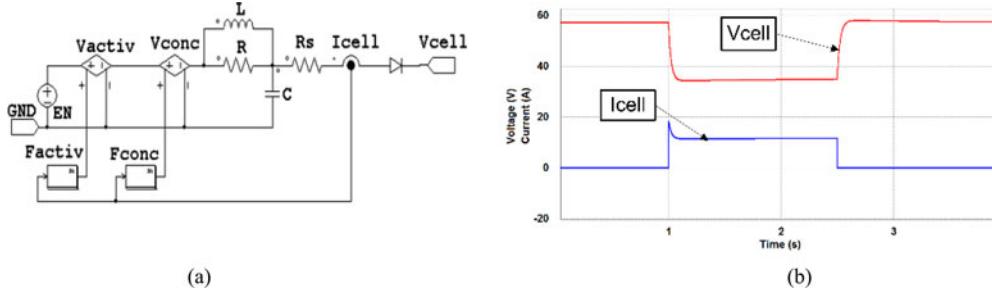
Fig. 6.　(a) Developed PEMFC model for PSIM simulation platform. (b) PEMFC output transient during heavy load step-up.

TABLE I
PEMFC SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
T [K]	333.15	ξ_1	-0.948
P_{O_2} [atm]	0.26	ξ_2	3.1×10^{-3}
P_{H_2} [atm]	1	ξ_3	7.60×10^{-5}
Rs [Ω]	0.35	ξ_4	-1.93×10^{-4}
R [Ω]	0.175	n_c	48
C [F]	0.0072	E_0 [V]	1.229
L [H]	0.175	i_L [A]	45

the electrode through the electrochemical reaction of the FC. Equation (31) represents the concentration losses, where n is the reactant mols number and i_L is the FC limit current (above this value, the cell's voltage abruptly decreases)

$$V_{\text{conc}} = \frac{RT}{nF} \ln\left(1 - \frac{i}{i_L}\right). \tag{31}$$

Equation (32) represents the FC output voltage V_{cell} where n_c is the number of cells in series

$$V_{\text{cell}} = n_c(E_N - V_\Omega - V_{\text{activ}} - V_{\text{conc}}). \tag{32}$$

To verify the effectiveness of the proposed model at this first stage, data taken of a SR-12FC-1000W PEMFC were used, which are presented in Table I. The main result is presented in Fig. 6(b), which shows the output voltage and current transient under severe load step-up. The detailed FC model is presented in [32].

One the significant risks to FCs during transient load conditions is fuel starvation that could cause irreversible damage to the cell. The extent of the risk is dependent on FC temperature and fuel delivery mechanism, such as pumps, valves, hydrogen reformers (when used), and their associated time constants [33]. In order to prevent the damage to the FC, if such a failure should occur on the ac grid, the supercapacitor bank will supply the entire system during the FC startup, which takes up to 20 s, as illustrated in Fig. 7.

The energy stored in the supercapacitor is determined by (33). Since the energy stored in a supercapacitor is directly proportional to the square of the voltage, if a 30% decrease of voltage occurs, there will be a stored energy release of 50% of the rated power. The internal losses due to the series resistance of the capacitor must also be accounted for [34]; therefore, (33)
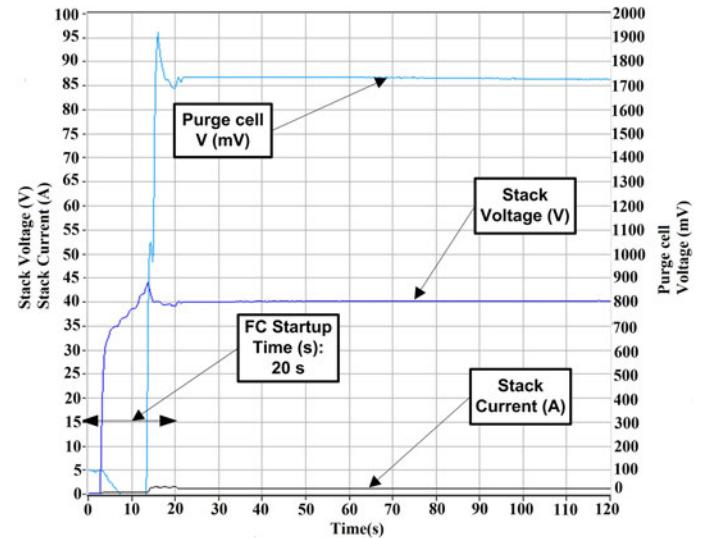
Fig. 7.　Fuel cell startup.

can be written as (34), where C is the capacitance, V is the operating supercapcitor voltage, k is the efficiency that will be less than one due to the series resistance of the capacitor, P_{stored} is the power stored in the capacitor, and t is the time that the capacitor remains charged

$$w_c = \frac{1}{2}CV \tag{33}$$

$$P_{\text{stored}} \cdot t = \frac{1}{2}\left[CV^2 - C(0.7V)\right] \cdot k \tag{34}$$

The value of t should be equal to the time of startup of the FC, which is shown in Fig. 7 (approximately 20 s) ensuring that the supercapacitors are able to power the system until the FC reaches its nominal operation. Thus, substituting the values in (34), we thus have

$$C = \frac{4P_{\text{stored}}t}{kV} = \frac{4 \times 500 \times 20}{0.9 \times 40} = 27.77\text{F}. \tag{35}$$

For obtaining this value, a series configuration with 15 supercapacitors (400 F, 2.7 V) was used. The supercapacitors specifications are presented in Table II.

Capacitance (F)	400
ESR, dc $\leq$(mΩ) [10 ms]	3.2
$P_{\max}$ (kW/kg)	7.9
Current, short circuit (A)	844
Voltage (cont.)	2.7
Continuous current (A)	24
Dimensions (mm)	35×69
Weight (kg)	0.077
Volume (L)	0.065
Temperature-operating and storage (°C)	-40 to $+70$

F. Implemented Control Technique

The control technique is based on the conventional average current control method for sinusoidal input current imposition and dc-link voltage control assuring, therefore, high input power factor, low harmonic distortion of current, and better dc-link voltage regulation for the connection of other electronic loads. During power failures or even in conditions of severe voltage sags on the ac grid, the PEMFC is activated, assuring the continuous energy supply to the load.

This control strategy ensures high fixed switching frequency and operation in continuous conduction mode, with soft commutation in all switches. In order to implement the control logic, the DSPF28335 was used. The choice for the digital control implementation was based on the high processing capacity as well as the operational flexibility provided by this type of microprocessor [35]. The block diagram portrayed in Fig. 8(a) illustrates the control logic used herein. The effort to establish the control code in the DSP follows the principles illustrated in the flowchart shown in Fig. 8(b). The control steps are described as follows:

1) A sample of the output voltage V_0 is compared with the reference voltage signal (V_{REF}), and the obtained error signal is applied to a PI controller (output voltage compensator). The signal obtained at the output of the voltage compensator is multiplied by the reference current signal ($|v_{\sin}|$), which is digitally generated and synchronized with the input ac voltage. A sample of the input voltage signal (v_{in}) is used for this purpose.

2) The result of this multiplication generates the I_{REF} signal. Therefore, a sample of the inductor current I_{LB} is compared with I_{REF} and the current error signal is applied to another PI controller (current compensator). The current compensator output signal (Kb) is used in the PWM block in order to generate the gate drive signals for switches S_1 and S_2.

3) By monitoring the voltage across the resonating capacitor (V_{Cr}) it is possible to identify when the drain-to-source voltage of the main switch (S_1) is null, determining, therefore, the moment when the PWM gate-drive signal of S_1 can be applied. This procedure allows the ZVS operation of S_1.

4) The AC power supply status is determined through the analysis of a sample of the input voltage signal ($v_{\sin}$). If
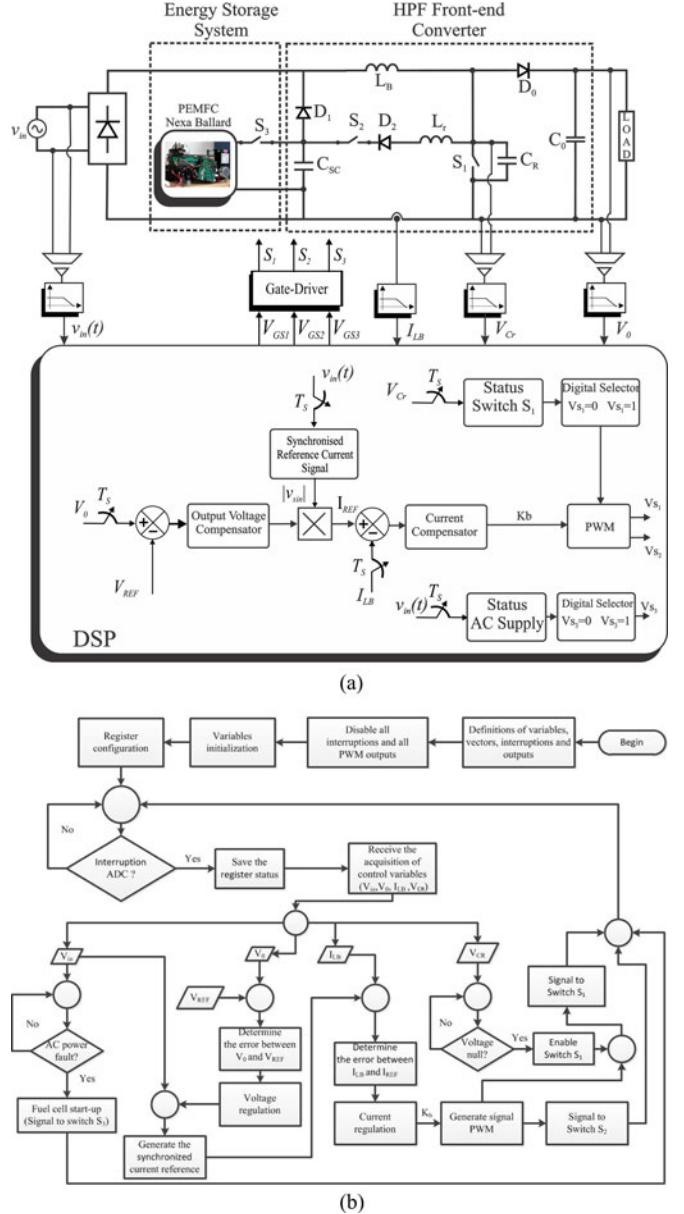
Fig. 8. (a) Block diagram illustrating the DSP-based control technique. (b) Flowchart of the control strategy.

there is a power failure, the switch S_3 is activated providing the start-up and connection of the FC to the system.

G. Average State-Space Model for Determining the Transfer Functions of the Plant and the Voltage and Current Controllers

The transfer function from boost converter can be obtained through an analysis of average state space as presented in [36]–[38]. It is important to emphasize that the operation of the soft-switching cell occurs in a short period of time when compared to a switching period; hence, the influence of the soft-switching cell on the analysis of the proposed converter regarding the system's dynamic response can be ignored.

Based on the project parameters presented in Table III, the transfer function of the plant can be divided between the plant
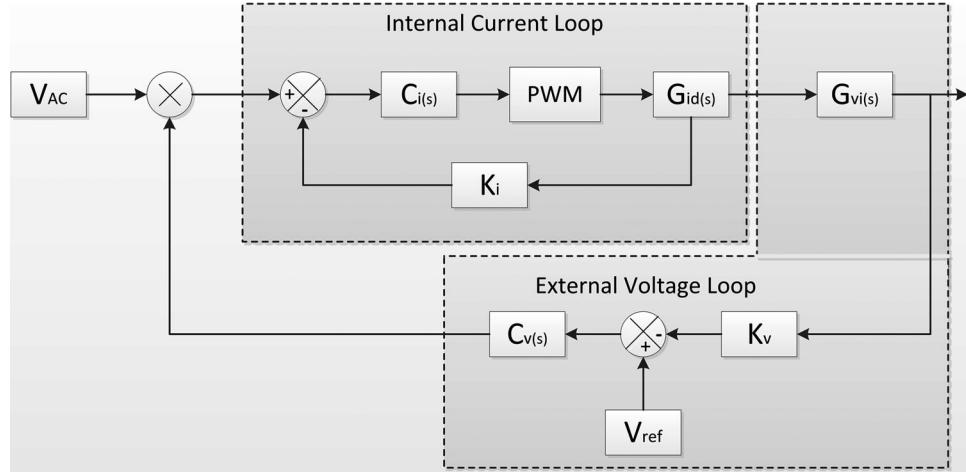
Fig. 9.   Simulation diagram in closed loop.
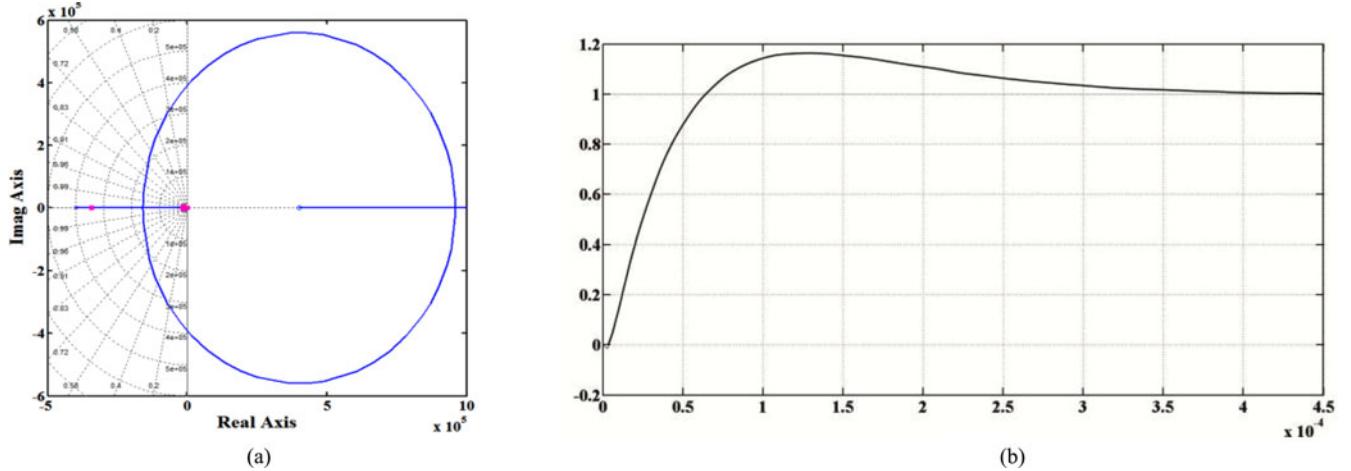
Fig. 10.   (a) Root locus of the internal current loop. (b) Step response of the internal current loop.

TABLE III
SPECIFICATIONS

Project Specifications
Output voltage, $V_{0(avg)} = 250$ V
Output power, $P_0 = 500$ W
Input voltage $V_{in(rms)} = 127$ V
Switching frequency = 100 kHz
Integrated PFC and DC–DC Boost Converter
Rectifier bridge TB-258
Boost inductor $L_B = 450 \ \mu$H
Filter capacitor, $C_0 = 940 \ \mu$F
Resonant capacitor $C_r = 4,7n/400$V
Main switch MOSFET IRFP460
Auxiliary switch MOSFET IRFP460
Diodes HFA15TB60

transfer function of the inductor current by the duty cycle $G_{id}(s)$, which is given by (36), and the plant transfer function of the output voltage by inductor current $G_{vi}(s)$, which is given by

$$G_{id}(s) = \frac{(21.15s + 360)}{(84.41 10^{-6}s^2 + 0.71 10^{-3}s + 46.35)} \quad (36)$$

$$G_{vi}(s) = \frac{89.8}{(117.5 10^{-3}s + 1)}. \quad (37)$$

The voltage controller transfer function $C_v(s)$ given by (38) and the current controller transfer function $C_i(s)$ given by (39) were implemented. Once the plant transfer functions are at hand, the *MATLAB-Sisotool* was used to analyze the performance of the internal current loop and the external voltage loop control as illustrated in Fig. 9. The results obtained are shown in Figs. 10 and 11, where it is possible to observe the system's stability and the step response for each control loop. One notes from the step response that the internal current loop is faster than the external voltage loop as desired

$$C_v(s) = \frac{(0.2017s + 1.636)}{s} \quad (38)$$

$$C_i(s) = \frac{(330.1s + 2.611 10^6)}{s} \quad (39)$$

.

The *Simulink* tool from the software *MATLAB* was used to simulate the complete system in closed loop, as portrayed in Fig. 12(a). The result for the step response is presented in Fig. 12(b), where one notes that despite the oscillations during the transient period, it comes into steady state at about 25 ms, which demonstrates that the voltage controller has a

(a)   (b)
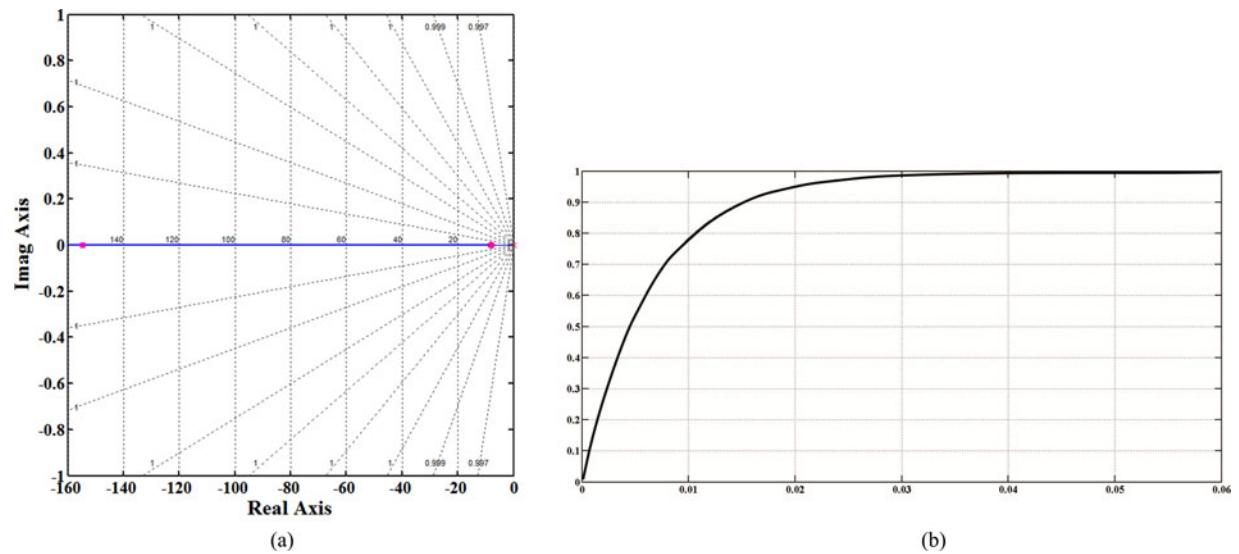
Fig. 11.   (a) Root locus of the external voltage loop. (b) Step response of the external voltage loop.

(a)

(b)
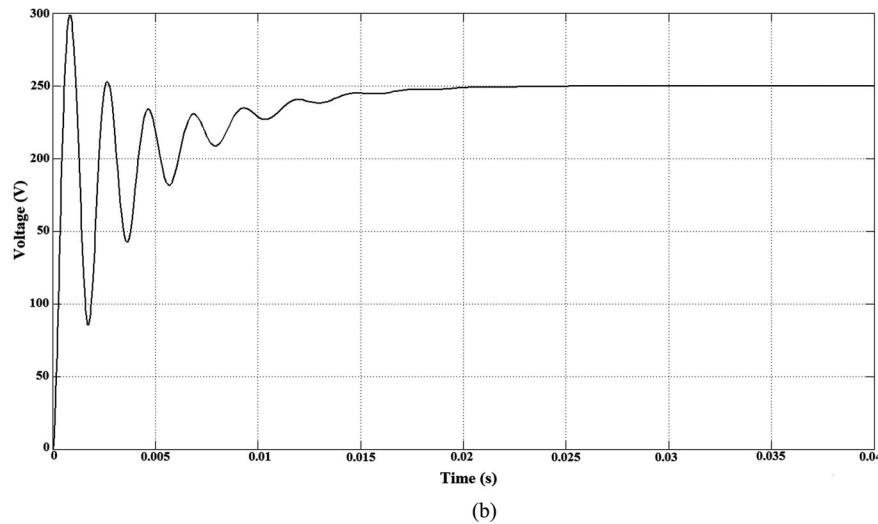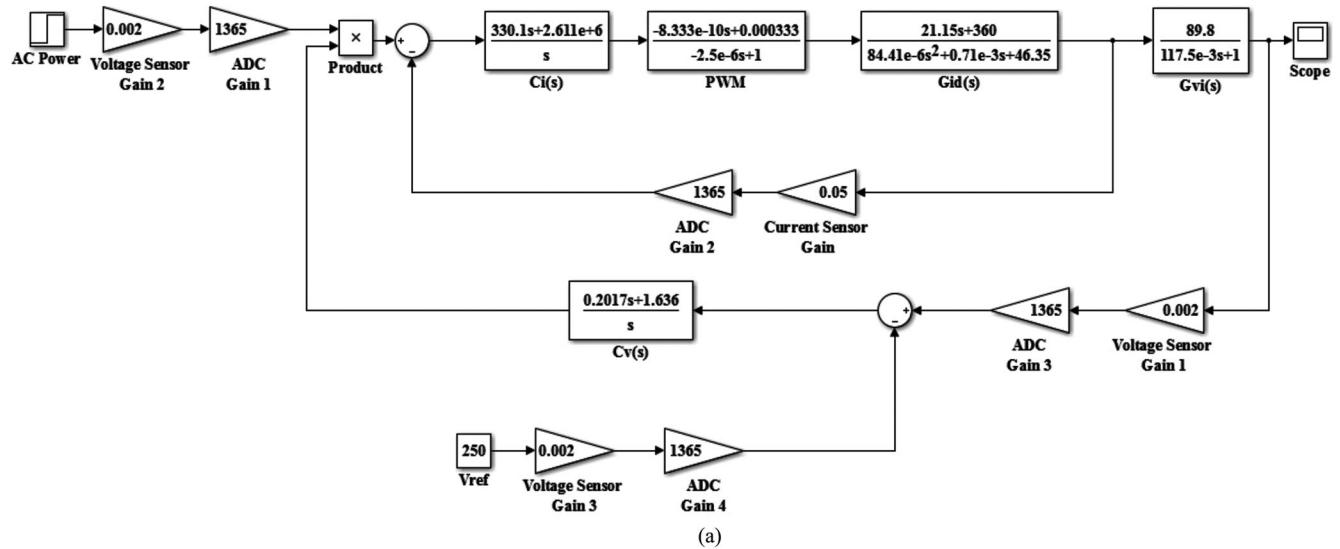
Fig. 12.   (a): Simulation diagram in closed loop. (b) Step response.
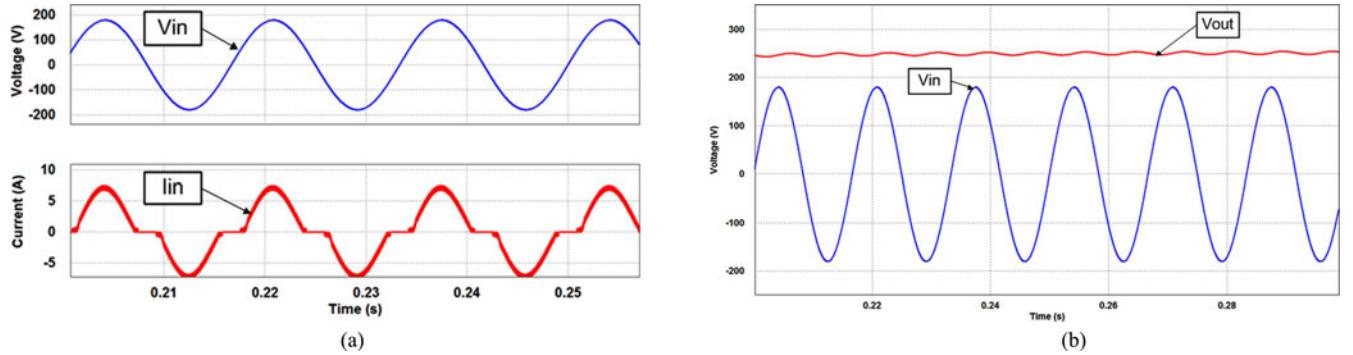
Fig. 13. (a) Simulated input current and input voltage. (b) Simulated input voltage and output current.
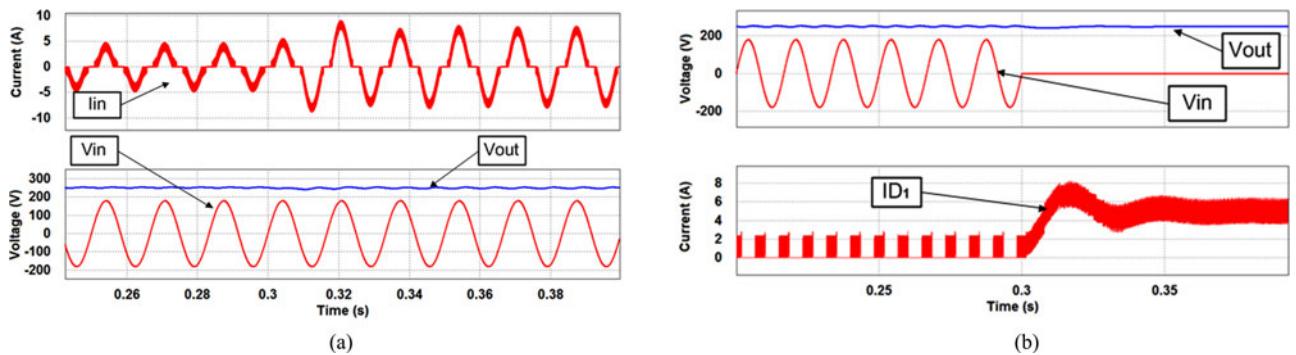
Fig. 14. (a) Simulated analysis for input ac current and voltage waveforms and the dc-link voltage, during a positive load step-up from 50% to 100% of the rated power. (b) Simulated analysis for input ac current and voltage waveforms, dc-link voltage, and the supercapacitor before and after the occurrence of the ac voltage failure at the supply grid.
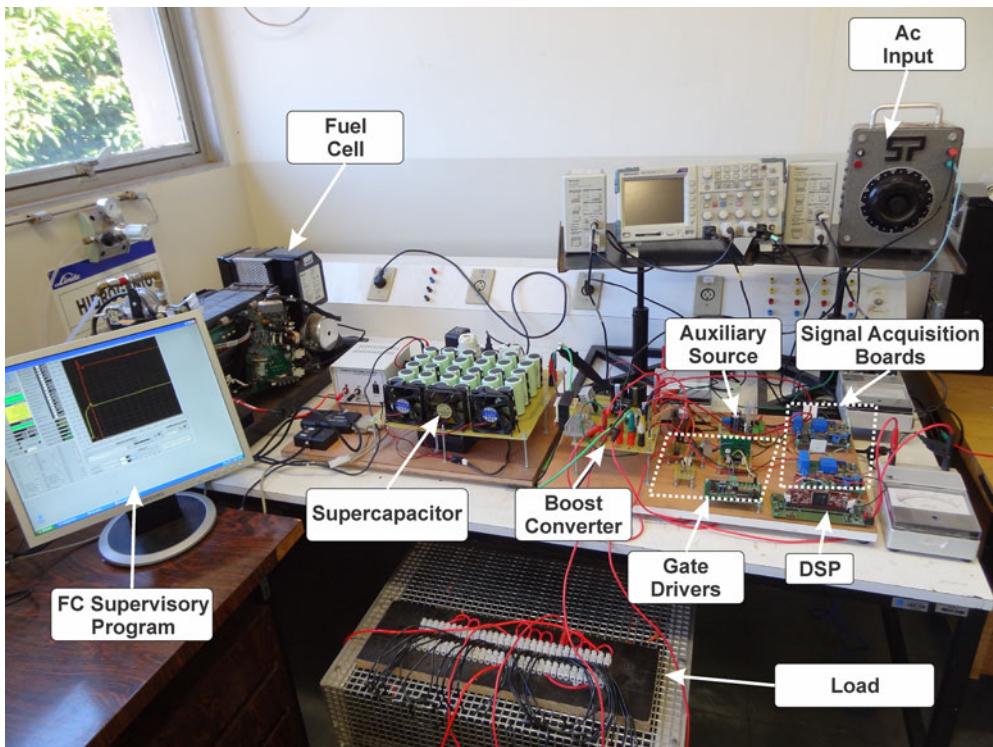
Fig. 15. Experimental setup.
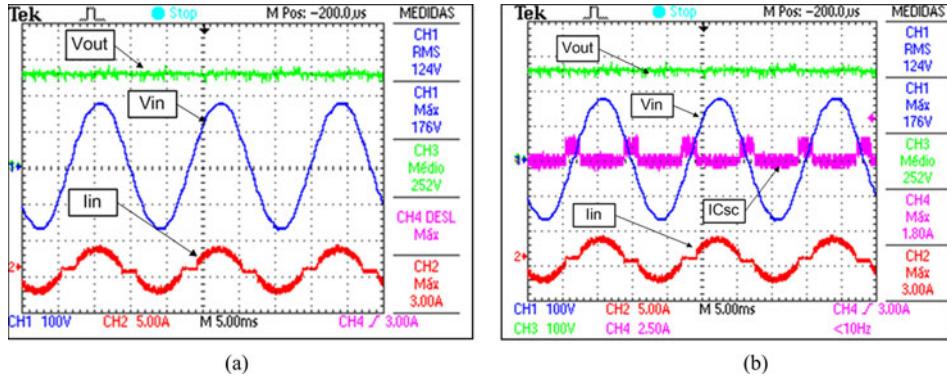
Fig. 16.   (a) Input current, input voltage, and output voltage in steady state. (b) Input voltage, output voltage, input current, and the supercapacitor current.
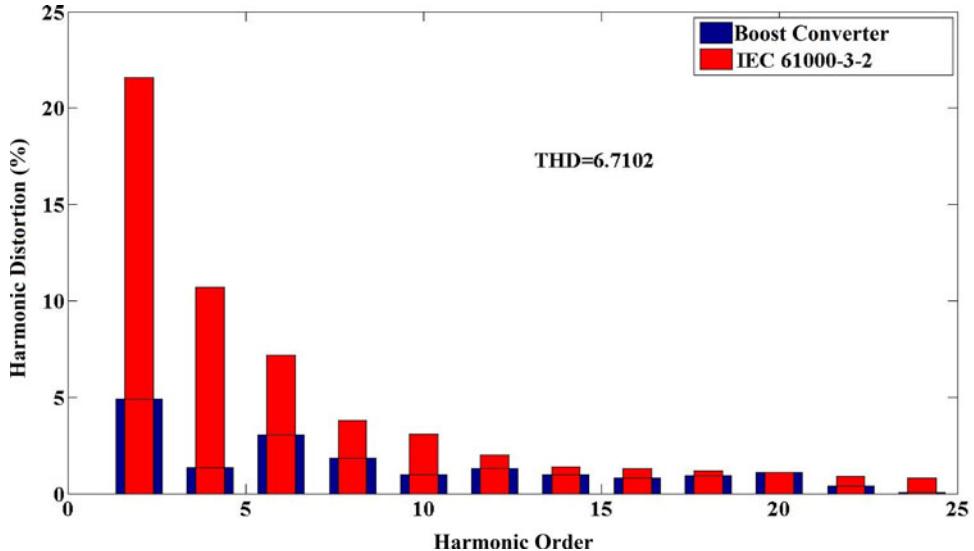
Fig. 17.   Harmonic spectrum of the input current in comparison with the harmonic content restrictions imposed by IEC 61000-3-2.
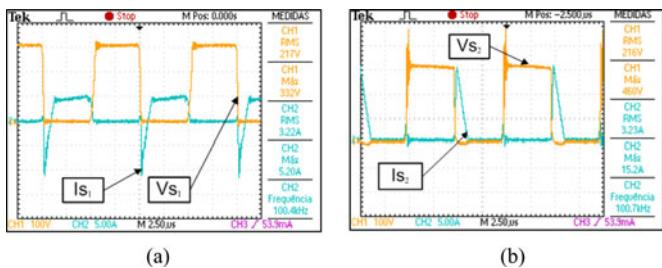
Fig. 18.   (a) Voltage and current of the main switch S_1. (b) Voltage and current of the auxiliary switch S_2.

quick enough response to control the output voltage, as desired. Significant oscillations are observed due to the fact that the initial capacitors voltage and the initial inductors current are zero including the dc-link capacitor.

III. SIMULATION RESULTS

In order to demonstrate the performance of the proposed UPS system, a simulation was implemented in the software PSIM following the project specifications parameters; its respective components are shown in Table III.

In Fig. 13, the signal of the input current, input voltage, and output voltage in steady state are shown. The power factor obtained in simulation was 0.98. The presence of D1, which connects the supercapacitors with the system, results in zero states for the input current. For this reason, it is not feasible to obtain unity power factor.

To conclude the simulation analysis, in Fig. 14(a) the input ac current and voltage waveforms and the dc-link voltage, during a load step-up from 50% to 100% of the rated power, are portrayed. It is possible to observe that the control of the dc-link voltage as well as the sinusoidal input line current imposition is achieved before and after the transient, demonstrating the effectiveness of the proposed solution. In Fig. 14(b), one also observes the behavior of the system during an ac power supply interruption, where there is little voltage drop in the dc link, which is maintained at 250 V as desired. The supercapacitors bank assures, together with the PEMFC, the continuous power supply to the electronic load connected to the dc link.
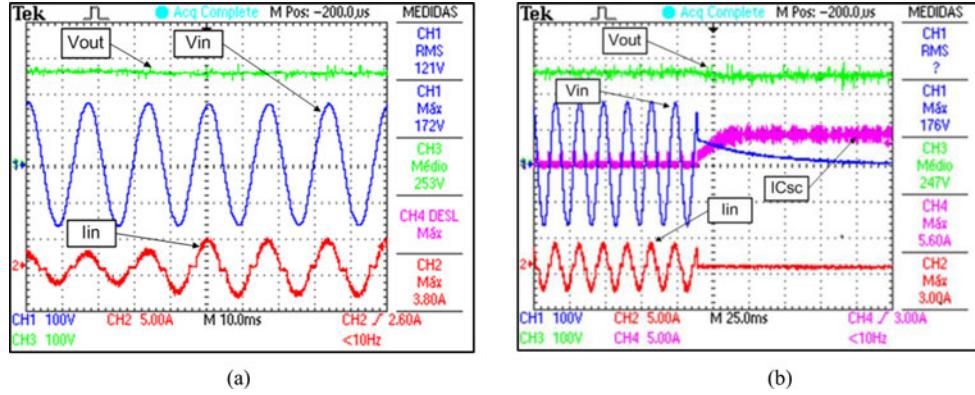
Fig. 19. (a) Input ac current and voltage waveforms and the dc-link voltage during a positive load step-up from 50% to 100% of the rated power. (b) Input ac current and voltage waveforms, dc-link voltage, and the supercapacitor current before and after the occurrence of the voltage failure at the supply grid.
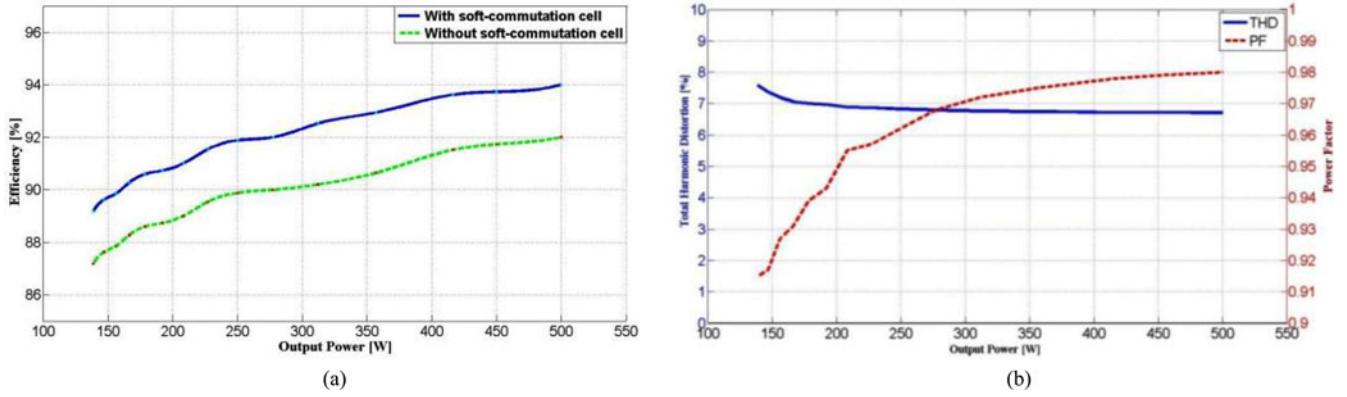

Fig. 20. (a) Efficiency comparison analysis of the proposed boost converter with integrated PFC and dc–dc functions and the conventional hard-switching boost PFC for rated input voltage. (b) THD_I and PF as a function of the output power.

IV. EXPERIMENTAL RESULTS

Aiming at performing an experimental evaluation of the proposed system, a 500 W prototype was employed in the laboratory. The experimental setup is portrayed in Fig. 15, illustrating the PEMFC which was used as an energy storage system in substitution of the battery bank. The supercapacitor bank is also presented, together with the PFC converter and the instrumentation used. The main experimental results obtained and the harmonic distortion analysis of the input current are presented from Figs. 16 to 19.

In Fig. 16, the signal of the input current, input voltage, and output voltage in steady state and the input voltage, input current together with the supercapacitor current are shown. It is possible to observe the current flow through the supercapacitor bank illustrating the moments that the supercapacitors bank is charged by the commutation energy and the time interval that the supercapacitors bank delivers energy to the load. This occurs when the input voltage is lower than the supercapacitors bank voltage and, therefore, the input current is zero, as can be seen by analyzing the input current waveform portrayed in Fig. 16. It is important to emphasize that despite this, the harmonic spectrum of the input line current is in accordance with the harmonic limits imposed by IEC 61000-3-2 as evidenced by Fig. 17.

In Fig. 18, the voltage and current waveforms of the main switch S_1 and of the auxiliary switch S_2 are shown in order to illustrate the soft-commutation condition achieved in both switches.

In Fig. 19, the input ac current and voltage waveforms and the dc-link voltage, during a positive load step-up from 50% to 100% of the rated power and the behavior of the system during an ac power supply interruption, where there is a little voltage drop at the dc link, are portrayed. The response was satisfactory and consistent with the one presented through simulation.

To conclude the experimental analysis, an analysis of efficiency, power factor, and THD_I for different load conditions were performed and the results obtained are portrayed in Fig. 20. Concerning the efficiency analysis, the performance of the proposed converter was evaluated with and without the soft-commutation cell using the same prototype showing that with soft commutation the efficiency is 2% higher. Regarding the power factor and the harmonic content of the input line current, it is shown that for a wide load ratio (from 50% to 100%), power factor higher than 0.96 is achieved, approaching 0.98 at full load and the THD_I is less than 7% and in accordance with the standard IEC61000-3-2, as demonstrated in Fig. 17. When compared to other PFC topologies presented, for example, in [39], [40], it is possible to conclude that the performance achieved

is very similar. It is also important to highlight that if better semiconductors, e.g., with lower series resistance and higher switching frequency capability, were employed, efficiency rates around 97–98% could also be achieved, as presented in [28].

V. Conclusion

This paper presents the development and analysis of a single-phase front-end converter with integrated PFC and dc–dc functions for online FC UPS. The elimination of dedicated dc–dc converters, as well as batteries and associated charging systems, results in significant size and cost reduction and in improving the reliability and working life of the system.

The dynamic performance of the proposed FC UPS system was improved using a decoupling supercapacitors bank which is continuously connected to the system assuring conditions for the prevention of critical operation situations during the startup of the FC along with zero switching delay of the ac power to the PEMFC. The DSP-based control technique is based on the average current control method for sinusoidal input current imposition and dc-link voltage control.

Theoretical analyses were presented and corroborated with experimental results. It was shown that high input power factor, low harmonic distortion of current, and improved dc-link voltage regulation for the connection of other electronics loads can be achieved. Special attention was given to the dynamic performance analyses of the proposed solution under conditions of ac power supply interruptions showing that the FC is activated assuring the continuous energy supply.

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