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Isolated AC/DC Offline High Power Factor Single-switch LED Drivers without Electrolytic Capacitors

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***Abstract*—Energy-efficient residential lighting such as household Light-Emitting Diode (LED) lamps with AC input require an AC/DC converter (or driver) with large output capacitance to minimize the low frequency LED current ripple. The energy storage capacitor used in the conventional AC/DC LED driver is usually an electrolytic capacitor due to its low cost and high energy density. However, the average lifetime of an electrolytic capacitor is at least 2 to 3 times less than that of a LED device. Hence, the potential lifetime of the LED lamp is significantly affected by the presence of the electrolytic capacitor in the driver circuit. In this paper, 2 novel isolated single-switch AC/DC high power factor LED drivers without using any electrolytic capacitors are proposed. In the proposed circuits, the energy storage capacitor is moved to the rectifier side, with a three-winding transformer used to provide isolation; input power factor correction as well as to store and provide the required energy to the output. As a result, the energy storage capacitance is significantly reduced, which allows film capacitor to be used to replace the conventionally used electrolytic capacitors. The circuit's operating principles and its characteristics are described in this paper. Simulation and experimental results are given on a 120Vrms, 12W prototype to confirm that a power factor of at least 0.96 is achieved.**

Keywords: Light-Emitting Diode (LED), Power Factor, Electrolytic Capacitor, Efficiency

I. INTRODUCTION

Lighting plays a significant role in our lives. It accounts for over 20% of the overall worldwide energy consumption. In order to significantly reduce the energy cost consumed by lighting, solid state lighting such as light-emitting diode (LED) lamps is the way of the future, as they are eco-friendly; mercury-free and have much higher energy efficiency and longer lifetime than other lighting technologies. The global market model predicts that LED market share in the residential segment will continue to increase to almost 50% in 2016 and over 70% by 2020 [1]. LEDs are temperature sensitive devices and their performance is determined by the driving current in the LEDs. A current limiting device is therefore required to ensure proper LEDs operation. As commercial or residential LED lamps are now required to achieve high power factor according to the U.S. Energy Star program [2], the LED driver circuit must include a power factor corrector to ensure that the input current harmonics meet the requirement.

The most common power factor correctors used in the conventional LED driver circuits [3] are usually either single-stage switch-mode DC/DC converter (i.e. buck or flyback) or two-stage converter [4]-[6] that consists of a front-end AC/DC converter for power factor correction (PFC) and a step-down voltage conversion circuit. A typical two-stage converter structure used in LED drivers is shown in Fig. 1. For applications used for AC input voltage with an input line frequency of either 50 or 60 Hz, a large energy storage capacitor in the range of several tens to hundreds of microfarads is often required in the LED driver circuit to balance the energy difference between the AC input power and the DC output power; and to reduce the low frequency ripple in the LED current. In order to minimize the LED driver size and overall cost, electrolytic capacitor is the most cost-effective choice due to its high energy density. Hence, it is commonly used as the energy storage component in LED drivers. However, compared to the average lifetime of a LED semiconductor device, which lasts about 50,000 hours, the average lifetime of the electrolytic capacitor is only around 10,000 hours. The lifetime of the overall LED system is then significantly affected by the presence of the electrolytic capacitor.

Different AC/DC driver solutions for LED lighting have been studied extensively and presented in [5]-[21]. In particular, a numerous number of works on eliminating the electrolytic capacitors in AC/DC LED drivers has also been presented in [7]-[9], [11]-[21]. Each of these works has its own merits. For example, in [16][18], multiple stages power conversion with multiple switches and a front-end boost PFC was employed. The energy storage capacitance was reduced due to the large input impedance of the second stage DC/DC converter, but the number of electronic components, overall size and cost of the driver circuit are increased. The efficiency is also much lower than the single-stage approach. A few modified single-stage AC/DC converter topologies such as [12][13][15][18][19][21] were also presented. In [7] and [12], flyback converter with a bi-directional buck-boost converter at the flyback's output was presented to absorb the pulsating component of the LED current, so that the low frequency component of the LED current and the output energy storage capacitor used in the conventional flyback converter are eliminated. In [13], a modified flyback converter with an additional auxiliary winding and three switches was presented to provide almost constant current to the output. In [15][21], a valley-fill circuit was used to replace the series capacitor of a conventional SEPIC converter to provide the required energy path to drive the LEDs. Although the electrolytic capacitors are eliminated in these works, they require either multiple transistors or several high voltage film capacitors in the range of tens of micro-farads in the driver circuit, which either leads to the use of complicated gate drive controller or increases the cost of the overall circuit. Instead of improving the driver circuit topology, the use of applying harmonic injection method [11][20] to the input current has also been presented to reduce the low frequency ripple in the LED current.

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In order to truly eliminate the electrolytic capacitor in the AC/DC LED driver without either increasing the number of transistors; using large size high voltage film capacitors or injecting current harmonics to provide energy balance, this paper proposes two novel isolated single-switch AC/DC high power factor electrolytic capacitor-less LED drivers. Each of the two proposed drivers has an integrated PFC circuit and a step-down voltage conversion circuit to drive the LEDs. The circuit's operating principles and its mathematical analysis will be discussed in this paper. This paper is organized as follows: section II describes the proposed LED driver topology; provides the circuit operating principles and design criterion of the circuit; section III gives an alternative topology of the proposed circuit; section IV gives a design example and discusses the performance of the proposed work through simulation and experimental results based on a 12W LED lamp with a tested input voltage range from 90 ~ 135Vrms; section IV provides a conclusion to summarize the features of the proposed work.

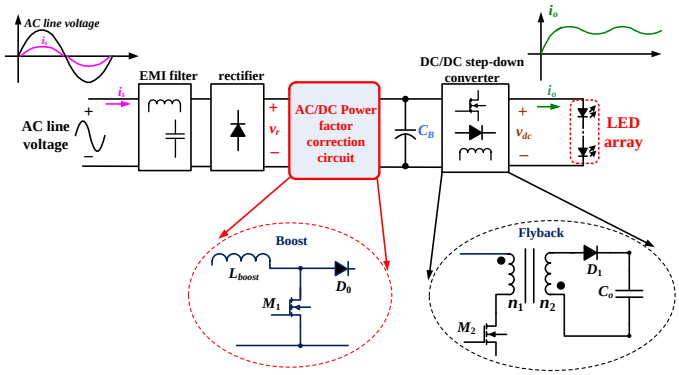

Fig. 1 Two-stage AC/DC Flyback LED driver with a front-end boost PFC

II. Description Of The Proposed Topology

In order to completely eliminate the use of the electrolytic capacitors in the LED driver, the proposed approach is to move the energy storage component from the output to the intermediate stage of the converter, similar to the two-stage approach mentioned in the introduction. But instead of having two separate converters to perform PFC and to provide step-down voltage conversion, the proposed approach utilizes an extra winding to feedback part of the energy to the energy storage capacitor while at the same time, providing a close-to-sinusoidal rectified current at the output of the diode rectifier. In addition, in order to provide isolation in the driver circuit, the proposed LED driver is derived by combining a discontinuous conduction mode (DCM) power factor corrector and a continuous conduction mode (CCM) forward converter into a single-stage single-switch topology. In this topology, the secondary side of a flyback converter is used as the DCM power factor corrector, as illustrated in Fig 2. Fig 3 shows the circuit diagram of the final topology. The integrated PFC circuit consists of D_0, C_B and L_{sec} (secondary winding of L_m), where the voltage across capacitor C_B is boosted from the rectified voltage (v_r). By operating the power factor corrector in DCM, the current flowing through D_0 follows the low frequency voltage envelope provided by the difference between v_r and v_{dc}. The output stage is an isolated forward converter that consists of L_m, L_{tri} (tertiary winding of L_m), M, D_1, D_2 and an output filter (L_o and C_o). L_f and C_f form the input EMI filter. The detailed discussion on the circuit's operating principles and the circuit's characteristics will be given in the following sub-sections.

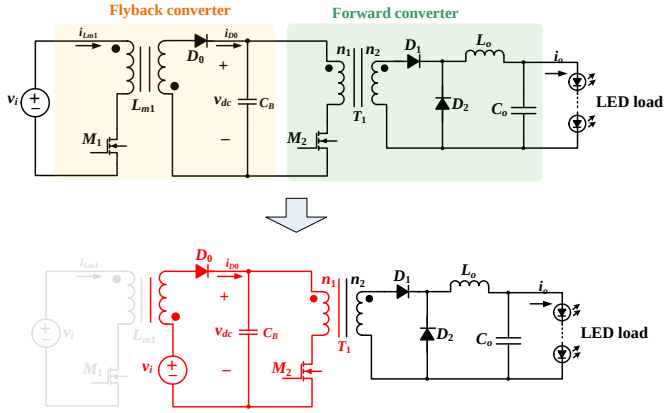

Fig. 2 Derivation of the proposed isolated AC/DC LED driver

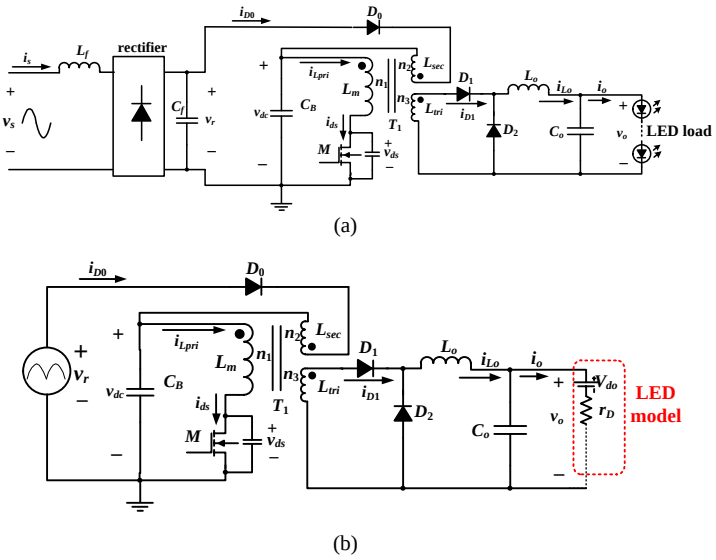

Fig. 3 (a) Proposed isolated AC/DC forward LED driver with integrated PFC, (b) Equivalent circuit with rectified voltage source

A. Circuit operating principles

The operating principles of the proposed LED driver is illustrated by the three different circuit operating stages within a switching period (T_s) as shown in Fig. 4.

[t_0 < t < t_1]: At t_0, the switch (M) turns on, current i_{Lpri} flows through C_B and M. At the same time, the positive voltage across L_{tri} forces D_1 to turn on. i_{Lo} then flows through D_1 and to the load. The MOSFET current (i_{ds}) or i_{Lpri} then consists of the rising charging current of L_m and i_{Lo}. The peak value of i_{ds} occurs at $t = dT_s$ and is given by (1), where d is the duty ratio; L_m is the inductance referred to the primary side; T_s is the switching period; V_{dc} is the average value of v_{dc}; and $i_{Lo,pk}$ is given by (2a), where v_o

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is the output voltage that is given by (2b) with n represents the number of series-connected LEDs, V_{do} is the LED threshold voltage and r_D is the LED resistance. By substituting (2) into (1), $i_{ds,pk}$ can be expressed as a function of d, V_{dc} and the turns ratio between n_3 and n_1 as shown in (3). This stage ends when the gate signal applied to M is removed.

$$i_{ds,pk} = \frac{V_{dc}}{L_m} dT_s + i_{Lo,pk}\left(\frac{n_3}{n_1}\right) \quad (1)$$

$$i_{Lo,pk} = \frac{\left(V_{dc}\frac{n_3}{n_1} - v_o\right)}{2L_o} dT_s + i_o \quad (2a)$$

$$v_o = n\left(r_D i_o + V_{d0}\right) \quad (2b)$$

$$i_{ds,pk}(d, V_{dc}) = dT_s\left(\frac{V_{dc}}{L_m} + \frac{n_3}{n_1}\frac{\left(V_{dc}\frac{n_3}{n_1} - v_o\right)}{2L_o}\right) + i_o\frac{n_3}{n_1} \quad (3)$$

[t_1 < t < t_2] At t_1, the gate signal that was applied to M is now removed and M turns off. The negative voltage across L_{sec} turns on D_0. Due to the voltage difference between v_r and v_{dc}, i_{Do} decreases linearly through L_{sec}. The voltage (v_{ds}) across M is given by (4), in which the maximum voltage stress on M occurs when v_r = 0 and is approximately given by (5), where V_{dc} can be obtained by knowing that the average voltage across L_m must be zero over T_s as given by (6). Re-arranging (6) gives the ratio between v_r and the V_{dc} as shown in (7), where d_1 is the discharge portion of L_{sec} during the time when D_0 is on.

$$v_{ds} = v_{dc} - v_{pri} \quad (4)$$

$$v_{ds,pk} = v_{dc}\left(1 + \frac{n_1}{n_2}\right) \quad (5)$$

$$V_{dc}\frac{n_2}{n_1} dT_s + (v_r - V_{dc}) d_1 T_s = 0 \quad (6)$$

$$\frac{V_{dc}}{v_r} = \frac{\frac{n_1}{n_2} d_1}{\frac{n_1}{n_2} d_1 - d} \quad (7)$$

[t_2 < t < t_2] At t_2, i_{D0} decreases to zero and D_0 turns off. v_{ds} is equal to the voltage (v_{dc}) across C_B. Meanwhile, i_{D2} continues to decrease linearly through the output filter (L_o and C_o) and the LED load until M turns on again. In general, the voltage conversion ratio between v_r and v_o can be defined by (8), where v_o/V_{dc} is given by (9). Hence, by combining (7) and (9), the voltage conversion ratio in the proposed circuit is given by (10).

$$\frac{v_o}{v_r} = \frac{v_o}{V_{dc}}\frac{V_{dc}}{v_r} \quad (8)$$

$$\frac{v_o}{V_{dc}} = \frac{n_3 d}{n_1} \quad (9)$$

$$\frac{v_o}{v_r} = \frac{\frac{n_1}{n_2} d_1}{\frac{n_1}{n_2} d_1 - d}\frac{n_3 d}{n_1} \quad (10)$$

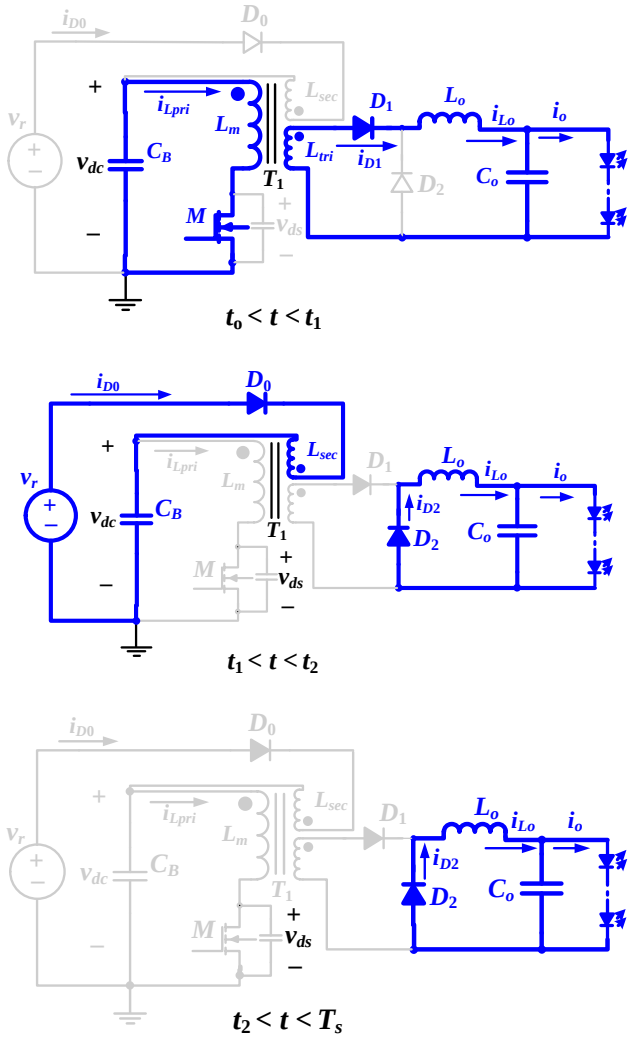

Fig. 4 Circuit operating stages

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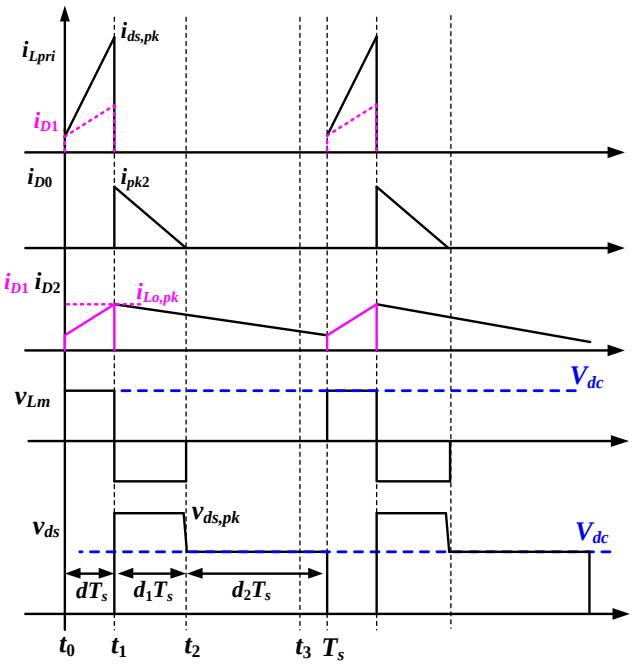

Fig. 5 Steady-state operating waveforms

B. Analysis of the Proposed LED driver

At the input side of the proposed circuit, PFC is achieved by operating L_m, the magnetizing inductance of the transformer in DCM. Essentially, the current (i_{Lsec} or i_{D0}) flowing through diode D_0 follows the voltage envelope generated by the difference between v_r and v_{dc}. Let V_p and f_L represent the peak value and the line frequency of the input voltage (v_s), then the rectified voltage (v_r) is represented by (11). Based on Fig. 5, the discharge portion (d_1) is given by (12). Then the average current through D_0 is given by (13), where i_{pk2} is given by (14), with $i_{Lo,pk}$ and $i_{ds,pk}$ given by (2) and (1) respectively. The average rectified current is average current flowing through diode D_0. Substituting (14) into (13) gives the average input current as shown by (15), where K_o is given by (16). (15) is then normalized and is plotted in Fig. 6 as a function of the ratio between V_p and V_{dc}. It shows that the shape of the input current is strongly affected by the ratio between V_p and V_{dc}. As V_{dc} is close to V_p, the input current becomes more distorted.

$$v_r = V_p\left|\sin\left(2\pi f_L t\right)\right| \tag{11}$$

$$d_1 = \frac{i_{pk,2}L_{\sec}}{\left(V_{dc}-v_r\right)T_s} \tag{12}$$

$$i_{Do,avg} = \frac{i_{pk2}}{2}\frac{d_1T_s}{T_s} = \frac{i_{pk2}}{2T_s}\left(\frac{i_{pk2}L_{\sec}}{V_{dc}-V_p\left|\sin\left(2\pi f_L t\right)\right|}\right) \tag{13}$$

$$i_{pk2} = \frac{V_{dc}dT_s}{L_m} - \frac{n_3}{n_1}i_{Lo} \tag{14}$$

$$i_{s,avg} = i_{Do,avg} = K_o\left(\frac{1}{1-\frac{V_p}{V_{dc}}\left|\sin\left(2\pi f_L t\right)\right|}\right) \tag{15}$$

$$K_o = \frac{\left(\frac{V_{dc}dT_s}{L_m} - \frac{n_3}{n_1}i_{Lo}\right)^2 L_{\sec}}{2T_sV_{dc}} \tag{16}$$

Since the average input power is given by (17), substituting (15) and the input line voltage equation into (17) give (18). The definition of the input RMS current is given by (19). By substituting (15) into (19), the final expression of the input RMS current is obtained as shown in (20). Finally, the power factor expression is obtained by combining (18) and (20) together. Eq. (21) will be used in the design example to select the ratio between V_p and V_{dc} to optimize the input power factor.

$$P_{i,avg} = \frac{1}{\pi}\int_0^{\pi} v_s(\theta)i_s(\theta)d(\theta) \tag{17}$$

$$\begin{aligned} P_{i,avg} &= \frac{V_pK}{\pi}\int_0^{\pi}\left(\frac{\sin(\theta)}{1-\beta\sin(\theta)}\right)d(\theta) \\ &= \frac{V_pK}{\pi}\left(\frac{-\pi}{\beta}+\frac{1}{\beta\sqrt{1-\beta^2}}\left(\pi+2\tan^{-1}\left(\frac{\beta}{\sqrt{1-\beta^2}}\right)\right)\right) \end{aligned} \tag{18}$$

$$i_{s,RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_s^2(\theta)d(\theta)} \tag{19}$$

$$\begin{aligned} i_{s,RMS} &= \sqrt{\frac{K^2}{\pi}\int_0^{\pi}\left(\frac{1}{1-\beta\sin(\theta)}\right)^2 d(\theta)} \\ &= \sqrt{\frac{K^2}{\pi}\left(\frac{2\beta}{1-\beta^2}+\frac{2}{\left(1-\beta^2\right)^{3/2}}\left(\frac{\pi}{2}-\tan^{-1}\left(\frac{-\beta}{\sqrt{1-\beta^2}}\right)\right)\right)} \end{aligned} \tag{20}$$

$$\begin{aligned} PF &= \frac{P_{i,avg}}{v_{s,RMS}i_{s,RMS}} \\ &= \frac{\sqrt{2}P_{i,avg}}{V_pi_{s,RMS}} \end{aligned} \tag{21}$$

The power efficiency of the proposed circuit can be analyzed according to the circuit model shown in Fig. 7. Similar to the input current shaper presented in [22]-[23], a "loss-free resistor" (R_s) is introduced between the output of the rectifier and the energy storage capacitor in the proposed circuit. The "loss-free resistor" used in the proposed circuit consists of diode D_0 and the secondary winding of the high frequency transformer T_1. Unlike [22], where the input current conduction time is affected, according to Fig. 6 and (15), the input current achieved from the proposed circuit is always continuous. From Fig. 7, it can be

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observed that the power transferred to the output load (P_o) can be affected by the series connection of R_s. Assume that the efficiency of the isolated DC/DC portion is η_s and a power share factor [24] of m_s is used in the proposed circuit for the power shared by R_s, P_o is then given by (22), where P_i is the converter input power. Rearranging (22) gives the circuit efficiency as shown by (23), which shows that if m_s is kept small in the circuit, the circuit efficiency will be maximized.

$$P_o = (P_i - m_s P_i)\eta_s \tag{22}$$

$$\frac{P_o}{P_i} = \eta_s(1 - m_s) \tag{23}$$

Recall that the MOSFET voltage is a function of both V_{dc} and the turns ratio (n_2/n_1) according to (5). Knowing that the shape of the input line current is a function of V_{dc}, $v_{ds,pk}$ is then plotted in Fig. 8 as a function of the turns ratio (n_2/n_1) for different ratios of V_{dc} and V_p. It is observed that $v_{ds,pk}$ decreases as n_2/n_1 increases and as V_{dc} is close to $V_{p.}$. Both Fig. 6 and Fig. 8 will be used in the design example to choose the appropriate values of n_2/n_1 and the ratio between V_{dc} and $V_{p.}$

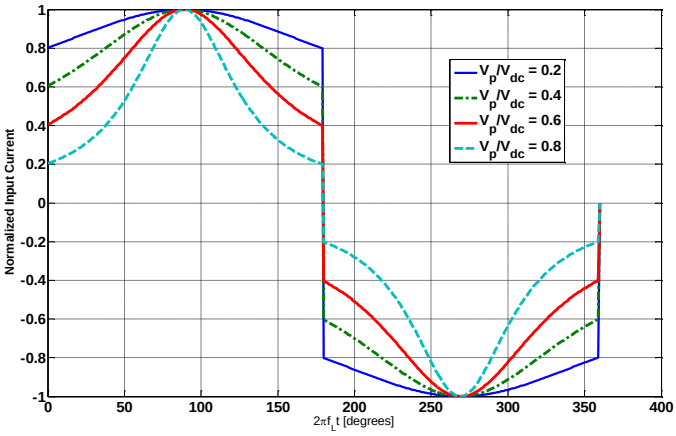

Fig 6 Theoretical i_s waveform for different values of v_{dc} for a line cycle

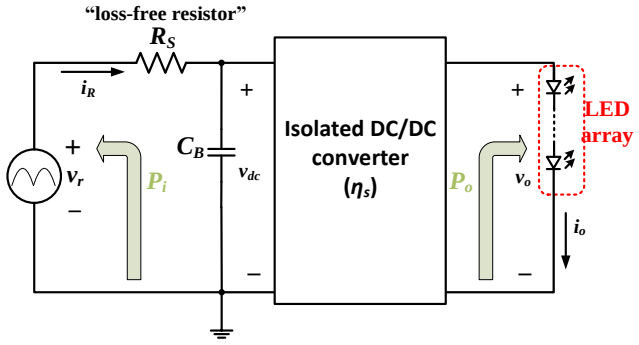

Fig 7 Equivalent circuit of the proposed LED driver with "loss-free resistor"

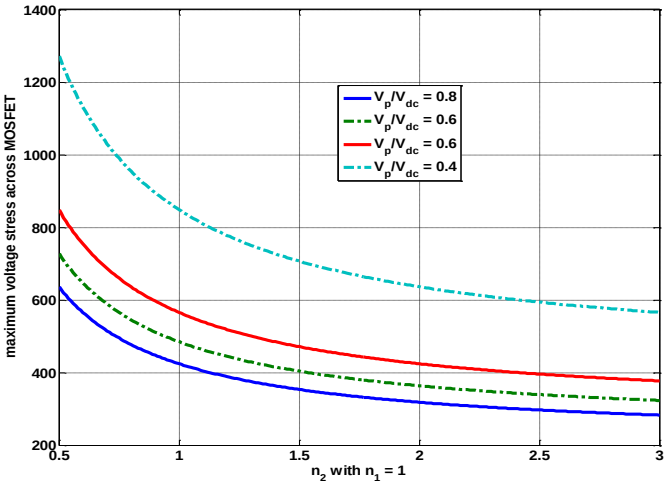

Fig 8 $v_{ds,pk}$ VS turns ratio n_2/n_1

In the proposed circuit, the energy storage capacitor is C_B whereas capacitor C_o is only used for high frequency filtering purpose. As C_B is moved to the high voltage side and hence, due to the high input impedance of the forward converter and the continuous energy exchange between C_B and L_{sec}, the hold-up energy demanded by C_B can be reduced significantly and hence, smaller value of C_B can be used, which allows film capacitor to be used as the energy storage capacitor. Fig. 9 shows the low frequency theoretical waveforms of v_{dc} and i_{D0} for a line cycle. Since the voltage (v_{dc}) across C_B is boosted from the input line voltage, hence, the equivalent load resistance across C_B becomes larger. The change in the energy (ΔE) in C_B is defined by (24), where $V_{dc,max}$ and $V_{dc,min}$ are the maximum and minimum values of V_{dc} as shown in Fig. 9. As ΔE is also defined by (25) according to Fig. 9, by combining (24) and (25) together, (26) is obtained, where η_s is the efficiency of the circuit. It can be observed from (26) that the required C_B can be decreased if V_{dc} is increased for the same input average power. (26) will be used to determine the required capacitance in the design example

$$\Delta E = \frac{1}{2} C_B \left(V_{dc,\max}{}^2 - V_{dc,\min}{}^2 \right) \tag{24}$$

$$\Delta E = \frac{P_{i,avg}}{4\pi f_L} \tag{25}$$

$$C_B = \frac{P_{o,avg}}{\eta_s 4\pi f_L V_{dc} \Delta V_{dc}} \tag{26}$$

In the output stage of the proposed circuit, in order to ensure that CCM is provided in i_{Lo}, the minimum required L_o can be calculated from (27), where $i_{o,avg}$ is the average output current.

$$L_{o,\min} = \frac{dT_s \left(V_{dc} \frac{n_3}{n_1} - v_o \right)}{2 i_{o,avg}} \tag{27}$$

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Based on (9) and (26), it can be observed that when d is controlled to regulate the output current for a wide range of input voltages, V_{dc} will be varied. In the case when the input voltage increases, d will be decreased to regulate the output current and according to (9), V_{dc} will be increased accordingly. Hence, higher voltage rated capacitor (C_B) will be required if the proposed circuit is employed to work with a wide range of input voltages.

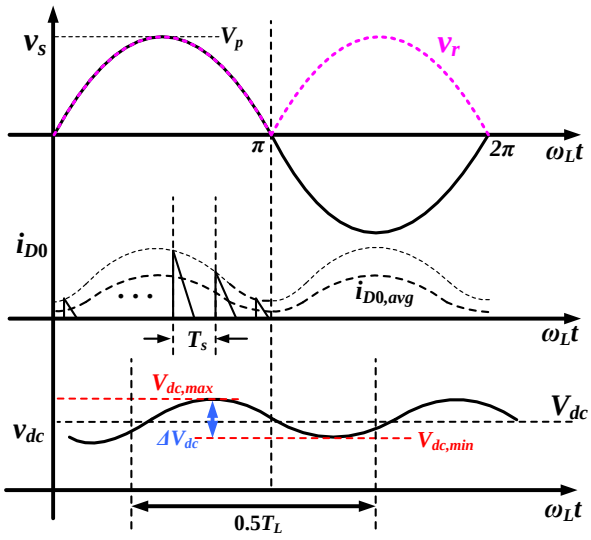

Fig 9 V_{dc} waveform analysis

III. Alternative Electrolytic Capacitor-less AC/DC Isolated Topology

By applying the same integration concept that discussed in the previous section, the DCM power factor corrector can also be combined with a flyback converter with an output LC filter to form an alternative single-stage topology of the isolated LED driver as shown in Fig 10. In this circuit, the windings L_m and L_{tri} form the flyback transformer. Compared to the circuit shown in Fig 3, the proposed converter with a flyback output stage saves one diode. Since the mathematical analysis of the input current of the circuit in Fig 10 is very similar to the one illustrated in the previous section, the input current analysis will not be repeated here. The operating stages and key waveforms of this circuit are then shown in Fig 11 and Fig 12 respectively, where the circuit's operating principles can be analyzed by four different stages again within a switching period. A brief description of each of the operating stages is as follows:

[$t_0 < t < t_1$]: At t_0, the switch (M) turns on, current i_{Lpri} flows through C_B and M. At the same time, the current i_{D1} is discharging its energy through D_1 and C_o. This stage ends when i_{D1} drops to zero.

[$t_1 < t < t_2$]: At t_1, D_1 turns off while the switch (M) is still on, the rising portion of current i_{Lpri} is determined solely by the voltage across capacitor C_B. Since D_1 is off, the output capacitor C_o discharges its energy to the load.

[$t_2 < t < t_3$]: At t_2, the switch (M) turns off, the reverse polarity of the transformer forces D_0 and D_1 to conduct and hence, due to the step-down voltage function of the flyback output stage, i_{D1} rises linearly, and since V_{dc} is boosted from the rectified voltage, i_{D0} decreases linearly. This stage ends when i_{D0} decreases to zero.

[$t_3 < t < T_s$]: At t_3, due to the DCM operation of the input stage, i_{D0} is decreased to zero and D_0 turns off, the output inductor (L_o) continues to provide its energy to the output load.

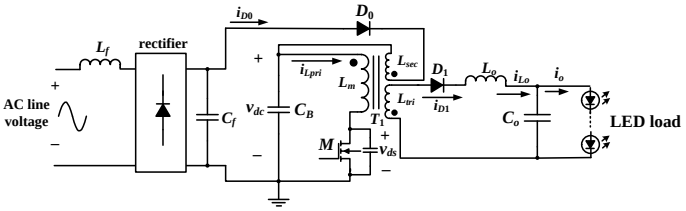

Fig 10 Proposed isolated electrolytic capacitor-less LED driver with flyback converter

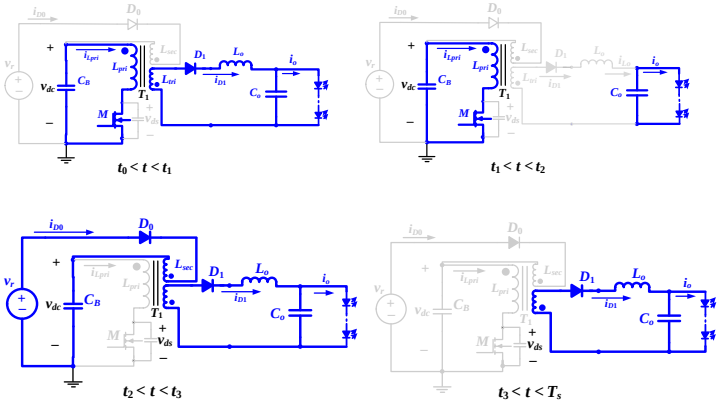

Fig 11 Operating stages of the proposed electrolytic capacitor-less LED driver with a flyback converter

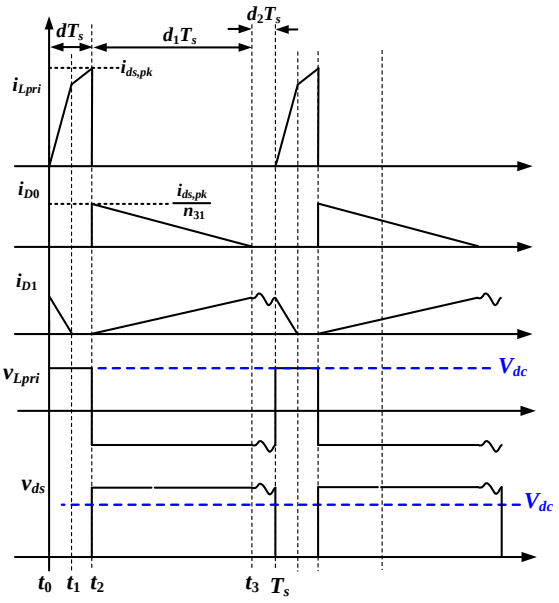

Fig 12 Key waveforms of the proposed LED driver with a flyback output stage

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IV. Design Example, Results and Performance

To validate the theoretical analysis of the proposed LED circuits, a design example of the proposed circuit shown in Fig 3 is given in this section. The tested input voltage range is: 90 ~ 135Vrms, 60Hz. The output load consists of 10 series-connected LEDs of model: MX3AWT-A1-0000-000E50, 3000k, each with an average current of 0.35A which gives a total output power of close to 12W. The switching frequency (f_s) of the LED driver is 62kHz and ΔV_{dc} is specified to be 10%.

A design procedure of the proposed topology is given below for this design example:

1) With V_p = 120*1.414 = 170V, according to Fig. 6 and Fig. 13 (which is obtained according to (21)), the optimized input current shape occurs at a ratio of V_p/V_{dc} between 0.6 and 0.8. In this example, a ratio of V_p/V_{dc} 0.7 is chosen to give V_{dc} equals to 245V.
2) Based on (18), with ΔV_{dc} specified to be 10%, and V_{dc} = 245V, assume that an efficiency of 0.85 is achieved in the circuit, the minimum C_B is then calculated to be 2μF. In this example, 2.7μF is used for C_B in the simulation.
3) L_o is then designed according to (25), with $n_3 = n_1$, $L_{o,min}$ is 0.75mH. The actual L_o used in this example is 1.5mH.
4) The MOSFET maximum voltage ($v_{ds,pk}$) is then determined from (5), with n_1:n_2 chosen to be 2:5 based on Fig. 8 and the pre-determined V_{dc}, $v_{ds,pk}$ is then calculated to be 338V. In order to further reduce the high frequency ripple in the output current, the output filter capacitor (C_o) is chosen to be 2μF.
5) The input EMI filter components: L_f and C_f are designed according to [25][26]. The cut-off frequency is selected to be around 1/5 of f_s [26]. Since the presence of C_f can introduce a phase shift between the line voltage and the line current, and will then affect the input power factor. The capacitance of C_f should not be too large in the actual design. The cut-off frequency is chosen to be 20kHz, and according to the cut-off frequency equation: $f_c = 1/\left(2\pi\sqrt{L_f C_f}\right)$, if C_f is chosen to be 47nF, then L_f is calculated to be 1.3mH.

Fig. 14 shows the circuit diagram used in the simulation with a current feedback control loop, where the PI compensator of the form in (28) is designed according to classical linear control theory [27], with K_c represents the gain and T_c represents the time constant of the PI compensator. The fact that a pole is placed at s = 0 in (28) helps to eliminate any steady-state errors. The values of K_c and T_c are determined with the aid of the "sisotool" toolbox from MATLAB. Fig. 15 – Fig. 16 summarize the Bode plots of the loop transfer function obtained from PSIM for different line voltages with different values of K_c and T_c. Fig. 15 shows the Bode plots for v_s = 90V_{rms} and 135V_{rms} when K_c and T_c are 0.4 and 0.0005 respectively. The phase margin (PM) is measured to be 72.1° at v_s = 90V_{rms} and 62.5° at v_s = 135V_{rms}. The corresponding output current is also shown in the figure, and the low frequency ripple is measured to be 20.4% at v_s = 90V_{rms} and 13.9% at v_s = 135V_{rms}. The performance can be further optimized with a reduction in the output current low frequency ripple by either increasing K_c or decreasing T_c in (28). Fig. 16 shows the Bode plots for v_s = 90V_{rms} and 135V_{rms} when T_c is decreased to 0.00018. The PM is then measured to be 46.6° at v_s = 90V_{rms} and 40.2° at v_s = 135V_{rms}. The corresponding low frequency output current ripple is measured to be 7.5% at v_s = 90V_{rms} and 5.4% at v_s = 135V_{rms}. Although the low frequency output current ripple can be further reduced at low input voltage range by further decreasing T_c, the PM will be further reduced at high input voltages as well. In this case, oscillations or unstable operation will be observed.

In general, given the fact that there are no specific requirements or regulations on the LED current low frequency ripple, the LED current low frequency ripple achieved from this design example will be in the range: 10 – 20%. The final values of K_c and T_c are selected to be 0.4 and 0.0003 respectively.

$$G_c(s) = \frac{K_c(1+sT_c)}{sT_c} \tag{28}$$

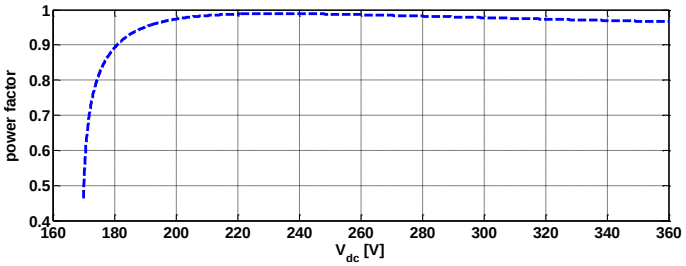


Fig 13 Power factor as a function of V_{dc} for the design example (with V_p = 170V)

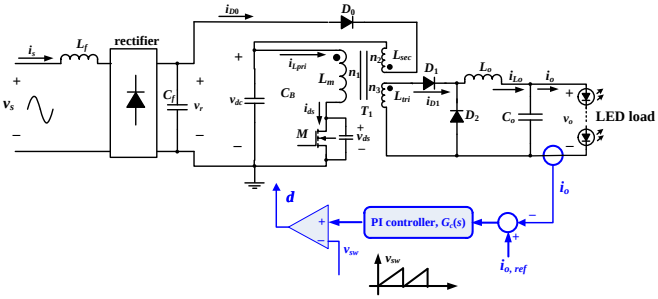
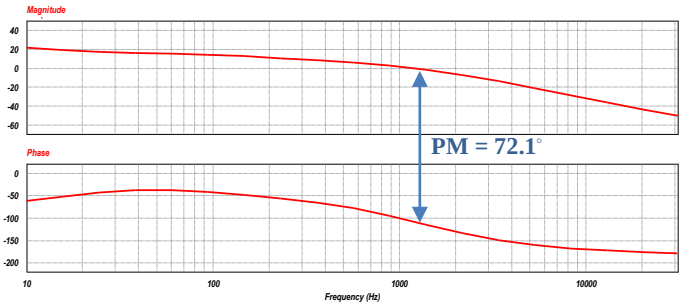


Fig 14 Proposed LED driver with current feedback controller in simulation



i) Bode plot at v_s = 90V_{rms} with K_c = 0.4, T_c = 0.0005

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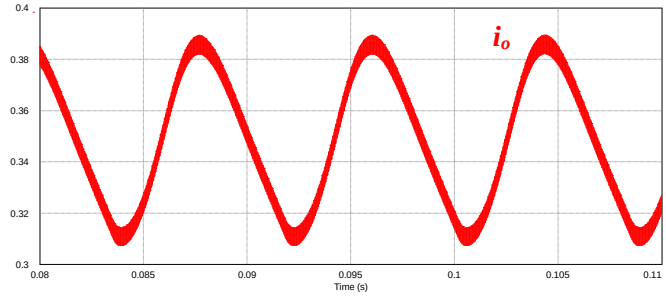
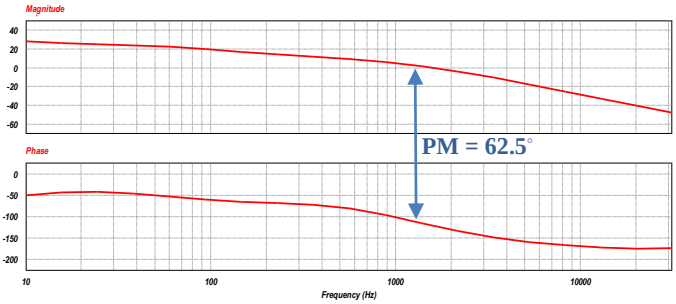
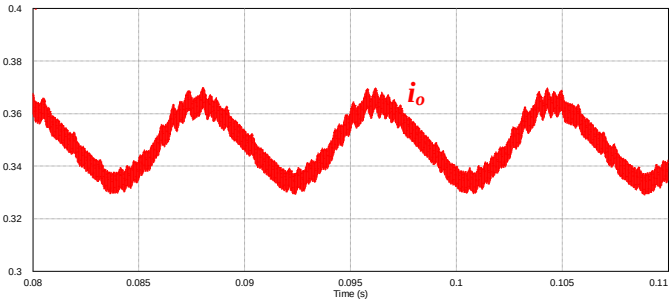


ii) output current at $v_s = 90V_{rms}$ with $K_c = 0.4$, $T_c = 0.0005$

(a) At $v_s = 90V_{rms}$



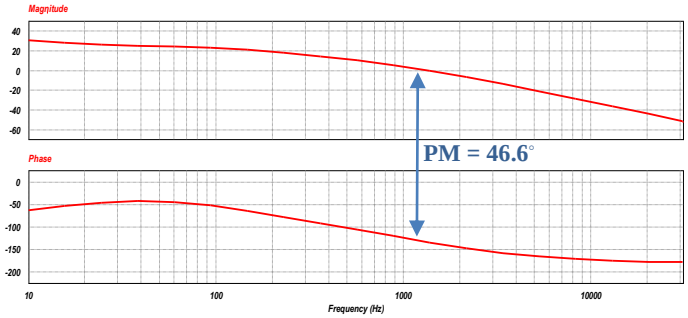
i) Bode plot at $v_s = 135V_{rms}$ with $K_c = 0.4$, $T_c = 0.0005$



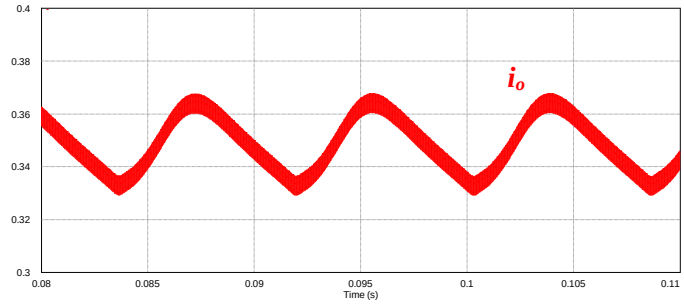
ii) output current at $v_s = 135V_{rms}$ with $K_c = 0.4$, $T_c = 0.0005$

(b) At $v_s = 135V_{rms}$

Fig 15 Performance with $K_c = 0.4$, $T_c = 0.0005$

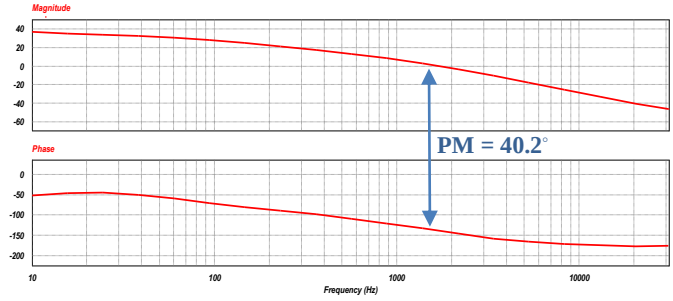


i) Bode plot at $v_s = 90V_{rms}$ with $K_c = 0.4$, $T_c = 0.00018$

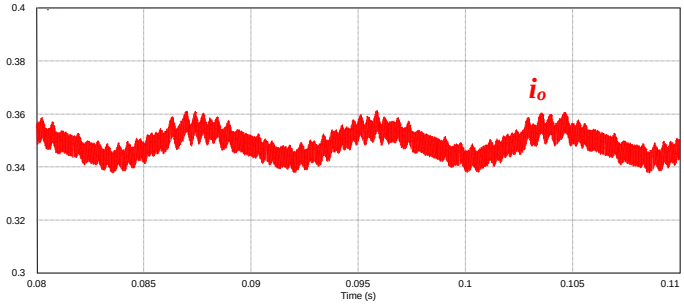


ii) output current at $v_s = 90V_{rms}$ with $K_c = 0.4$, $T_c = 0.00018$

(a) At $v_s = 90V_{rms}$



i) Bode plot at $v_s = 135V_{rms}$ with $K_c = 0.4$, $T_c = 0.00018$



ii) output current at $v_s = 135V_{rms}$ with $K_c = 0.4$, $T_c = 0.0005$

(b) At $v_s = 135V_{rms}$

Fig 16 Performance with $K_c = 0.4$, $T_c = 0.00018$

A. Simulation results

Fig. 17 shows the simulated line current and output current for different values of input line voltage. A power factor of 0.968 with a total harmonic distortion (THD) of less than 16% is achieved at $v_s = 90V_{rms}$, and a power factor of 0.974 with a THD of less than 15% is achieved at $v_s = 135V_{rms}$. The output current ripple is measured to be 19.8% with an average current of 347mA at $v_s = 90V_{rms}$ and 11.6% with an average current of 348mA at $v_s = 120V_{rms}$.

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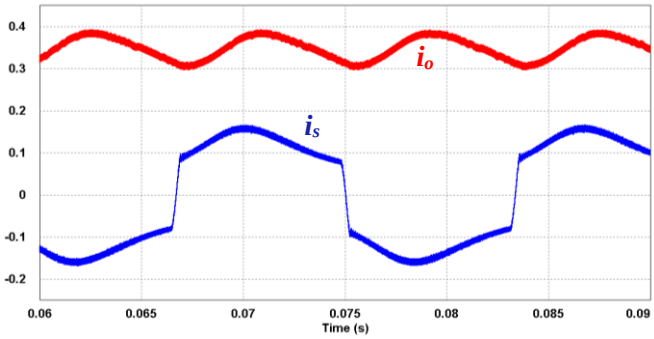
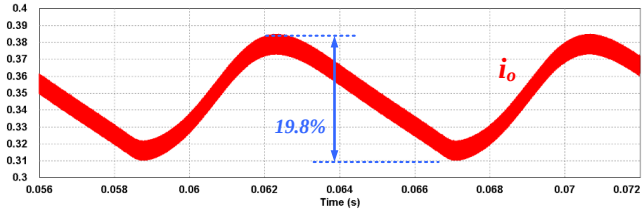
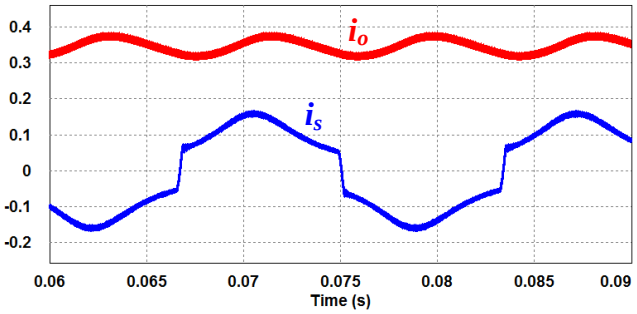
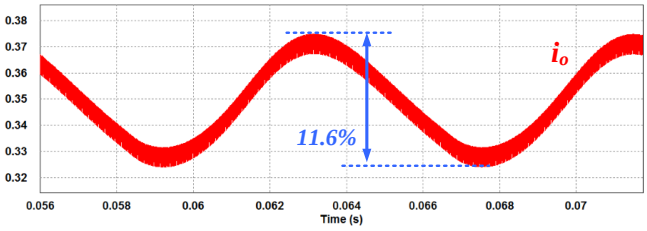


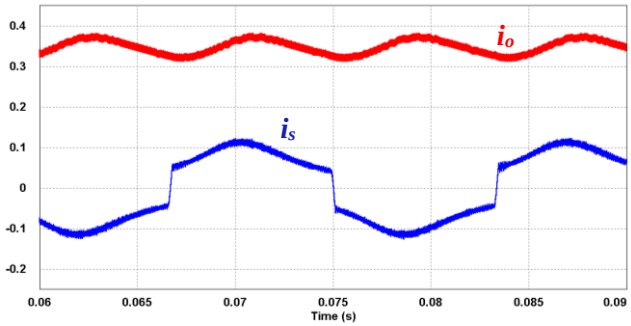


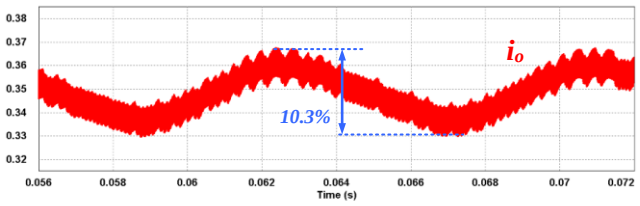
(a) at $v_s = 90V_{rms}$





(b) at $v_s = 120V_{rms}$

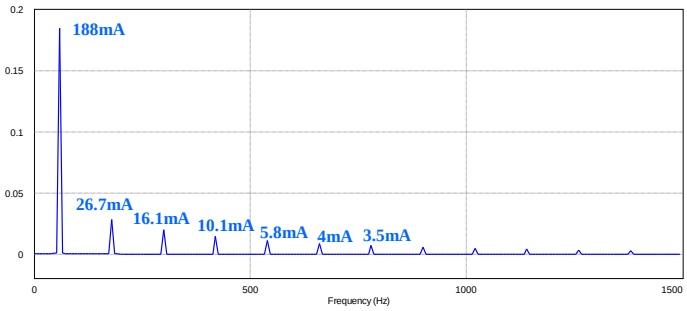




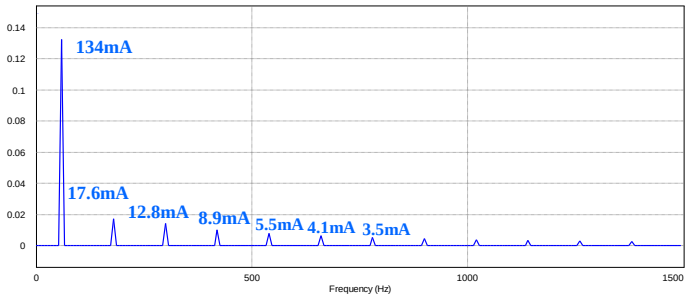
(b) at $v_s = 1350V_{rms}$

Fig 17 Simulated output current (i_o) and line current (i_s) (a): at $v_s = 90V_{rms}$, (b): at $v_s = 120V_{rms}$, (c) at $v_s = 135V_{rms}$

Fig. 18 shows the harmonics of the input current (i_s) at $v_s = 90V_{rms}$ and $v_s = 135V_{rms}$. Since the output power of this example is $\leq 25W$, the harmonic contents of i_s are required to comply with the IEC 61000-3-2 Class D standard [28][29]. TABLE I compares the harmonic contents of i_s at different line voltages with the IEC 61000-3-2 Class D requirements. It shows that the harmonics of i_s meet the requirements specified in the IEC 61000-3-2 Class D standard. Fig. 19 shows the V_{dc} waveform at $v_s = 120V_{rms}$. The average value of V_{dc} is 270V. Fig. 20 and Fig. 21 show the MOSFET voltage and current waveforms. The maximum v_{ds} and i_{ds} are 320V and 1.39A $v_s = 120V_{rms}$. To verify the feasibility of the proposed circuit for high input line voltage, the proposed circuit is simulated in PSIM for $v_s = 220V_{rms}$. Fig. 22 shows the MOSFET voltage at $v_s = 220V_{rms}$ and the maximum voltage stress is measured to be 589V.



(a) $v_s = 90V_{rms}$



(b) $v_s = 135V$

Fig 18 Line current harmonics (a) at $v_s = 90V_{rms}$; (b) at $v_s = 135V_{rms}$

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TABLE 1: Measured line current harmonics with IEC 61000-3-2 Class D limits

Harmonic order (n)	Maximum Permissible Harmonic Current Per watt [mA/W]	Actual Limit [mA]	Measured at v_s = 90V_{rms} [mA]	Measured at v_s = 135V_{rms} [mA]
3	3.4	40.8	26.7	17.6
5	1.9	22.8	16.1	12.8
7	1.0	12	10.2	8.9
9	0.5	6	5.8	5.5
11	0.35	4.2	4	4.1
13 ≤ n ≤ 39	3.85/n	3.6	3.5	3.5

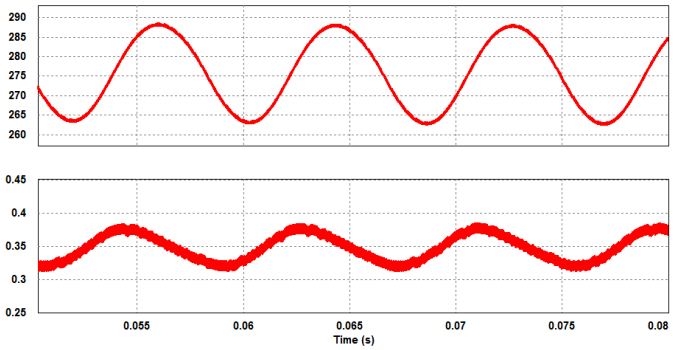

Fig. 19 Simulated voltage across C_B (V_{dc}) at v_s = 120V_{rms}

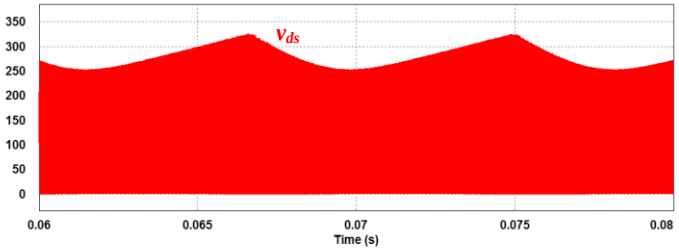

Fig. 20 Simulated switch voltage (v_{ds}) at v_s = 120V_{rms}

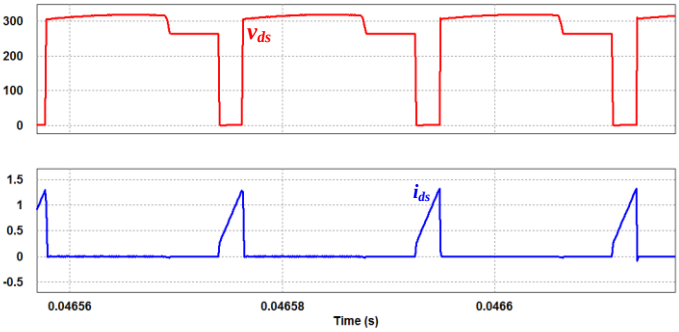

Fig 21 Simulated v_{ds} and i_{ds} at v_s = 120V_{rms}

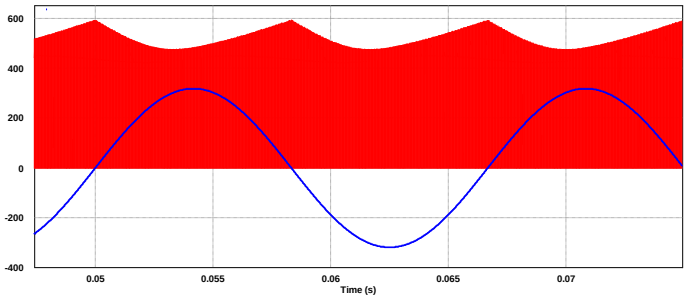

Fig 22 Simulated v_{ds} at v_s = 220V_{rms}

B. *Experimental results*

An experimental prototype of the circuit shown in Fig. 3 was built and tested in the laboratory. Based on the circuit parameters determined from the simulation results, the list of circuit components used in the prototype is given in TABLE II. Fig. 23 shows the picture of the experimental prototype. In the prototype, a film capacitor of 2.7µF was used as highlighted in Fig. 23. Fig. 24 shows the measured input line current and voltage. The power factor is measured to be 0.965. The power factor reading is obtained from the programmable AC voltage source of mode # AC 61603 from Chroma. Fig. 25 shows the measured line voltage and LED current. The average output current is measured to be 349mA and the current ripple is measured to be 62.3mA, which corresponds to 17.85% low frequency current ripple. The MOSFET voltage is shown in Fig. 26, with a maximum v_{ds} of 317V is obtained. The measured MOSFET current is shown in Fig. 27. The overall circuit efficiency is shown in Fig. 28 for various line voltages. The efficiency is 86.1% at 120V_{rms}. It should be emphasized that although the low frequency ripple in the LED current is measured to be 18%, there is no visible flickering observed. In fact, according to [30], the Alliance for Solid-State Illumination System and Technologies (ASSIST) has defined the flicker acceptability criteria based on their testing. Using the ASSIST criteria, at 120 Hz, percent flicker greater than 30% is unacceptable. Therefore, the achieved low frequency current ripple is well below the unacceptable level.

TABLE II. Circuit parameters in the experimental prototype

Circuit Designator	Parameters/Part number
D_0, D_1, D_2	MUR160 (600V)
M	NDF08N50ZG (500V)
C_f	47nF, 250V
C_B	ECW-FD2W275K (2.7µF, 450V) X 1
C_o	ECQ-V1J105JM (1µF, 63V) X 2

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T_1	0.75mH
L_o	2mH
L_f	2.2mH

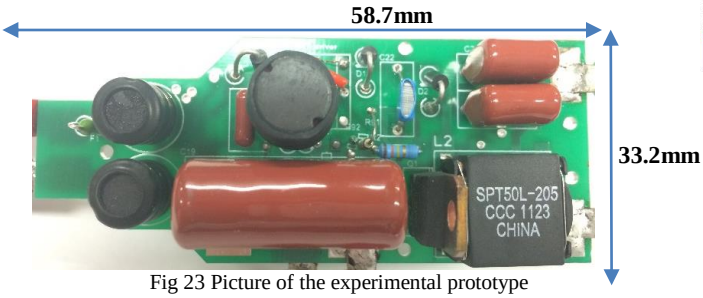


Fig 23 Picture of the experimental prototype

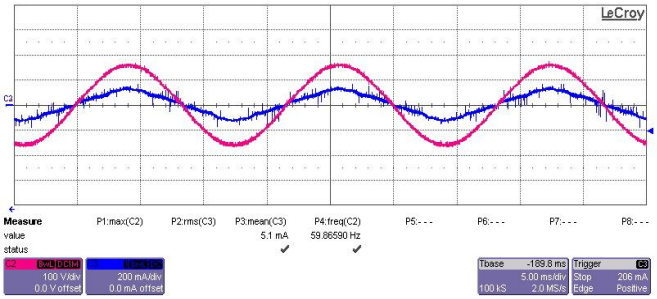


Fig 24 Line current (blue) and voltage (pink) (v_s: 100V/div; i_s: 0.2A/div; time: 5ms/div)

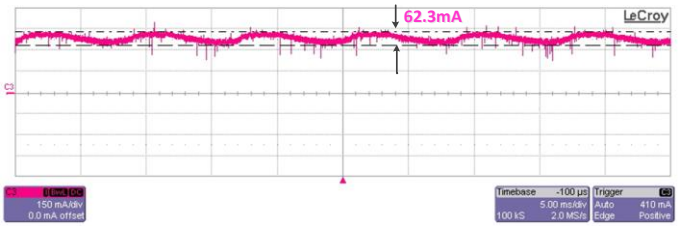
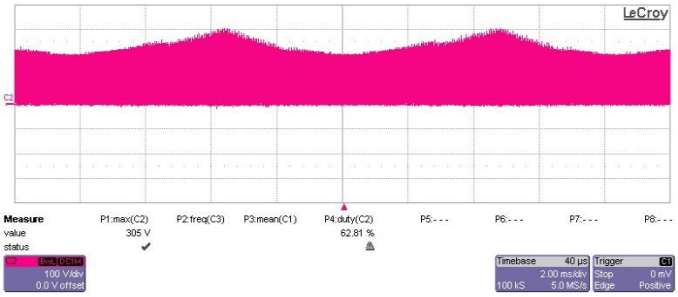
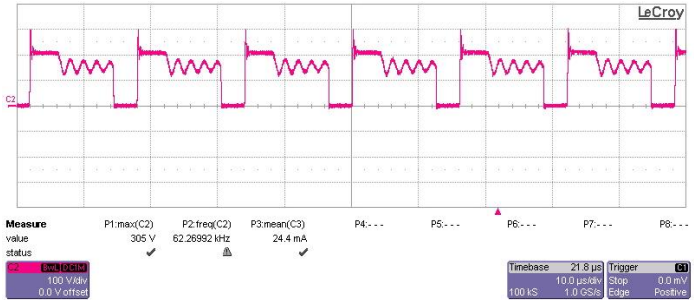


Fig 25 Output current (i_o: 0.15A/div; time: 5ms/div)



(a)



(b)

Fig 26 Switch voltage at v_s = 120V_{rms} (a): (v_{ds}: 100V/div; time: 2ms/div); (b) switch voltage within a few switching cycles (v_{ds}: 100V/div; time: 10µs/div)

Fig 27 Switch current (green) at 120V_{rms} (i_{ds}: 0.3A/div; time: 10µs/div)

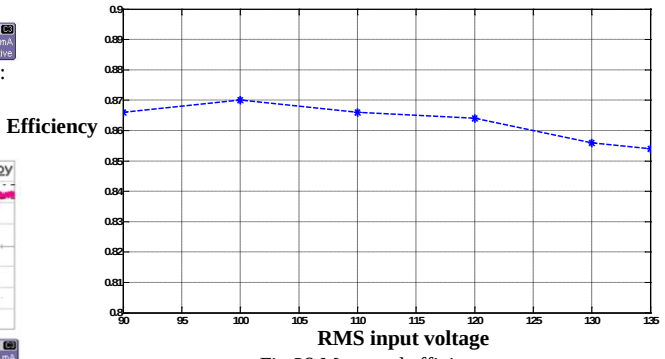


Fig 28 Measured efficiency

C. *Evaluation and discussion*

It is known that the single-stage AC/DC flyback converter is widely used in the existing low power LED drivers [31]-[34]. With respect to the flyback's efficiency, Fig. 28 shows that the proposed solution has comparable efficiency with the flyback LED drivers, in the range of 85 – 86%. In terms of the MOSFET voltage stress, as illustrated by Fig. 21 and Fig. 26, both the flyback converter and the proposed circuit also have very similar performance. Although flyback LED drivers have slightly higher power factor than the one achieved with the proposed circuit, as shown by Fig. 18, the harmonics of the input current achieved by the proposed circuit meet the IEC 61000-3-2 Class D standard. Finally, although the proposed circuit requires one more magnetic component and two more diodes than the flyback converter, those are standard fast-recovery diodes and the overall cost of the circuit will not be much higher than the standard flyback converter. In addition, the proposed circuit has the added advantages of having

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much longer lifetime and higher reliability, and is able to achieve almost the same power factor as the flyback circuit.

Dimming is an attractive feature in energy-efficient lighting. One way to achieve dimming with the conventional LED drivers is to adjust one of the control parameters (i.e. duty cycle, switching frequency, etc.) in the driver circuit. In the proposed circuit, when the duty cycle (*d* is decreased to provide low-level dimming, as mentioned in the previous section, the capacitor voltage (V_{dc}) will be increased. This implies that film capacitor with much higher voltage rating will be required in this scenario.

However, dimming household LED lamps or LED lighting fixtures often employ standard phase-cut dimmers (i.e. TRIAC dimmers) to reduce the input RMS line voltage. Several works that discuss the use of TRIAC dimmers for dimming LED lamps in low power application (i.e. < 20W) have been presented [35][36]. Since the proposed circuit is intended for household LED lamps, TRIAC dimmers can be utilized to work with the proposed topology to provide dimming operation. In this case, *d* in the proposed circuit does not need to be decreased significantly to provide dimming and the issue of using high voltage rated film capacitor will not be present. The analysis and operating principles of the proposed circuit with TRIAC dimmers are beyond the scope of this paper and will therefore be presented in future publications.

V. CONCLUSION

In residential or commercial LED lighting where the AC input line frequency is either 50 or 60 Hz, large output capacitance is often required in the driver circuit to: (1) balance the energy difference between the AC input power and the DC output power. In this paper, two novel AC/DC isolated offline LED drivers that do not require any electrolytic capacitors to achieve low output current ripple have been presented for household LED lighting applications. With the integrated PFC stage in the proposed circuit, high power factor was able to be achieved in both circuits. The detailed descriptions of the circuit operating principles and the circuit characteristics have been discussed in this paper. A 12W LED lamp design example has been given to confirm that a power factor of at least 0.96 and a low frequency output current ripple of less than 15% are achieved in the proposed circuit. Finally, it should be emphasized that although compared to the conventional single-stage LED driver, the proposed topologies require additional fast recovery diodes and an inductor, the lifetime and reliability of the resulting LED lighting system are significantly enhanced with the proposed circuits.

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