

A New Common-Mode Transformerless Photovoltaic Inverter

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Abstract— Transformerless inverters are being widely used in grid-connected photovoltaic (PV) generation systems. Transformer elimination, in grid-connected PV systems, has many advantages. This not only reduces cost, size and weight, but also increases the whole system efficiency. However, once the transformer is removed, there is no galvanic isolation between grid and PV array; as a consequence, leakage current appears due to parasitic capacitance to the ground, resulting in prohibitive electromagnetic interference and security issues.

This paper presents a novel topology in order to reduce this ground leakage current. It is established that the neutral line in the grid is the same as that of the negative terminal in a PV system, eliminating this way, any possibility of leakage current in this terminal. A sliding mode controller that controls the output current has been employed. The principle of operation of the transformerless inverter is analyzed, but also the topology has been simulated and experimentally tested.

Index Terms— Transformerless inverter, photovoltaic (PV) systems, leakage current, common-mode, sliding mode control.

I. INTRODUCTION

Nowadays PV systems are used extensively for the generation of energy in private and commercial circles. The PV inverters convert the energy given by a PV array and it is delivered into the AC mains (on grid). According to the European Photovoltaic Industry Association, at the end of 2009, the world's cumulative installed PV capacity was approaching 24 GW [1]. One year later it was 40.7 GW and at the end of 2011 it was 71.1 GW. In 2012, more than 100 GW of PV are installed globally, which the majority has been installed in Europe 70%, China 8.3%, USA 7.8% and Japan 6.9%. Today, this installation is capable to produce at least 110 TWh of electricity every year [1].

The grid-connected PV systems need to be carefully

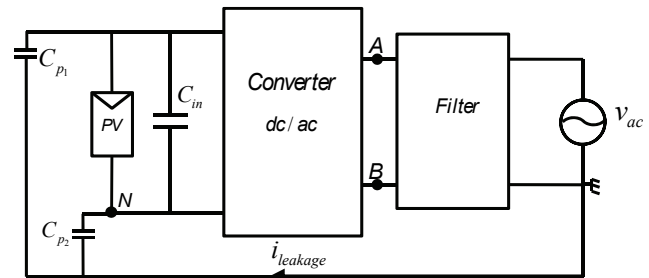


Fig. 1. Block diagram that illustrates the leakage current in transformerless inverter

designed for achieving high efficiency, low cost, small size, and weight. For safety reasons PV systems should employ galvanic isolation, this may be on the grid side by using an AC low frequency transformer, however, this transformer is big and heavy, which makes a bulky PV system. Galvanic isolation may also be on the DC side by using a high-frequency transformer, which is smaller and cost less than an AC transformer. Nevertheless, this kind of transformer requires an additional power stage that makes a more complex PV system, where system efficiency is reduced.

Grid-connected PV systems may also be used without a transformer, which improves their efficiency and makes the whole system lighter, smaller and easier to install [2-25]. However, a transformerless grid-connected PV system creates a common-mode resonant circuit, which includes the filter, the inverter, the grid impedance and the PV parasitic capacitance [11]. This common-mode generates a leakage current ($i_{leakage}$) that circulates through parasitic capacitances C_{p1} and C_{p2} in PV array to the ground, as shown in Fig. 1. The common-mode voltage, the modulation strategy and the value of the parasitic capacitance greatly affect the value of leakage current [3].

The parasitic capacitance value depends on many factors such as [15]:

- PV panel and frame structure.
- Surface of cells.
- Distance between cells.
- Weather conditions.
- Type of EMC filter

Furthermore, leakage current may have consequences on security issues; for instance, it is responsible for higher current harmonic, higher losses and electromagnetic interference issues (EMI) [2-13].

Some works have been deployed to set a maximum allowed leakage current [14-15]. Several topologies have tried to reduce the current leakage and some solutions are [3-10]:

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- Disconnect the AC side and the PV during freewheeling times.
- Connect the midpoint of the DC-link capacitors to the neutral line of the utility grid.
- Connect the PV negative terminal to the neutral line of the utility grid directly.

Following this trend, this paper presents a novel topology that has low leakage current without using complex control techniques. The proposed topology establishes that the neutral line in the grid is the same as that of the negative terminal in a PV system, which keeps common-mode (CM) voltage constant.

Some known transformerless topologies are described in the second section. The proposed topology and its analysis are discussed in the third section, where a controller using sliding modes is considered to control the output current. Numerical and experimental results from a 200W prototype demonstrating the converter performance are illustrated in the fourth section. And finally some conclusions are made.

II. LEAKAGE CURRENT IN TRANSFORMERLESS PV TOPOLOGY

In this section, a brief description of some transformerless topologies is given. At the beginning, traditional topologies are presented, then variations performed to the differential inverter are reported and finally, converters with common connection are discussed.

A. Full and Half Bridge topology [3-9, 25]

H-Bridge inverter, which consists of a full-bridge as shown in Figure 2, is recognized due to its simplicity in design. Different PWM switching may be used: bipolar and unipolar. Normally unipolar PWM switching is preferred because it improves the quality and reduces the losses; however, during its operation, the leakage current is very high, which makes this not only unsafe but also unsuitable for its use in PV generation systems.

In [25] is proposed a buck-boost converter plus a two half-bridge inverter to support split phase; this configuration has the advantage of having reduced low-frequency input current ripple, additionally to the low leakage current.

B. HERIC topology [3, 13]

This topology combines advantages from two alternatives: the three level output voltage of the unipolar PWM, besides the reduced common-mode voltage as in the case of bipolar

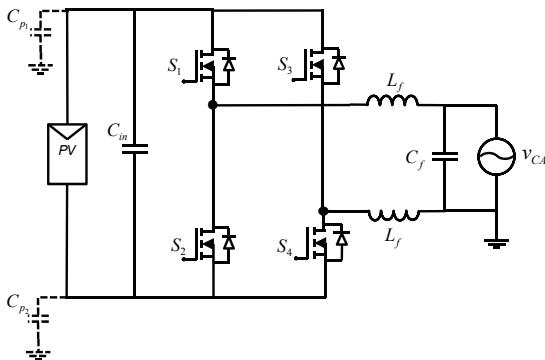


Fig. 2. H-Bridge Inverter

PWM. It consists of a full-bridge inverter plus two additional switches, as illustrated in Figure 3. Each group of diagonal switches of the full bridge operates in high frequency during the half wave of the grid. One of the two additional switches is turned on during the half wave of the grid. S_5 or S_6 is used when the disconnection occurs between the grid and PV array, which reduces the leakage current. The main drawback of this topology is the pair of additional semiconductors.

C. H5 topology [3, 9, 17]

This inverter maintains the traditional topology with a full-bridge, where the upper switches operate at grid frequency and the lower ones work at a high frequency. It has incorporated an extra switch S_5 on the DC side that operates in both semi-cycles at high frequency (Figure 4). The main characteristic of this configuration is that the PV array is decoupled from the grid when this extra switch is turned off.

Normally during active states, the current flows during freewheeling modes through two switches, but in active vectors, the current flows through three switches causing

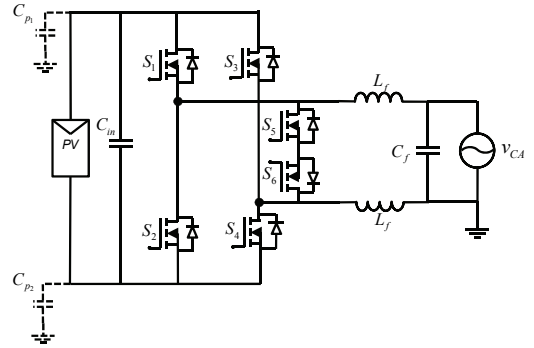


Fig. 3. HERIC topology

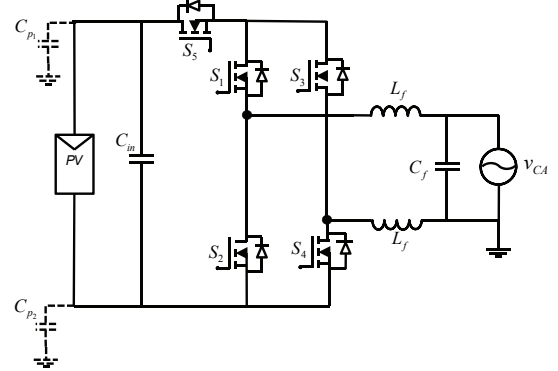


Fig. 4. H5 topology

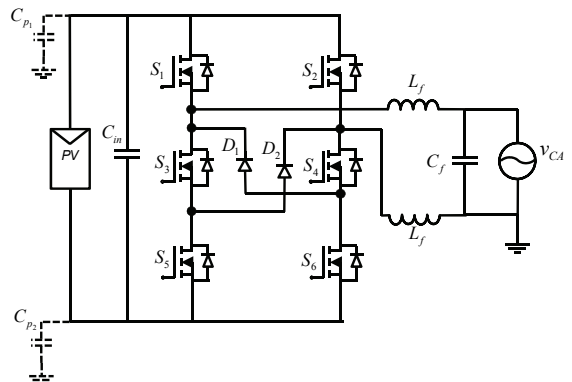


Fig. 5. H6 topology

significant conduction losses, which become a disadvantage.

D. H6 topology [2, 9]

This inverter is composed of six power MOSFETs and two diodes for the freewheeling mode, as shown in Figure 5. While operating in a freewheeling mode for the positive semi-cycle, the current circulates through S_4 and the diode D_1 that allows not only the disconnection between the PV array and the grid, but also avoids the high-frequency voltage in parasitic capacitance, and then the leakage current is reduced. Something similar occurs for the negative half-wave of the grid.

Diodes and two additional switches are used besides the traditional full-bridge; therefore its cost is higher. For this topology, during both positive and negative active vectors, the current flows through three switches, this may turn out to be an inconvenience for implementing the system.

E. Multilevel Topologies [19-21, 26]

The multilevel Neutral Point Clamped (NPC) inverter, shown in Figure 6, is suitable for reducing the leakage current. The midpoint of the DC-Link capacitor should be connected to the neutral line of the utility grid. The output voltage may be unipolar. During operation of this system, the input voltage must be twice higher than the H-Bridge Inverter. Reason, probably enough, to disregard this converter.

In [26] is proposed a new multilevel inverter that should be useful in PV applications, providing a low harmonic distortion, but certainly increasing the number of semiconductors and complexity.

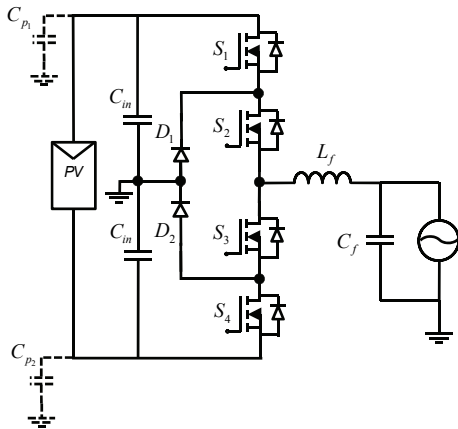


Fig. 6. NPC Multilevel converter

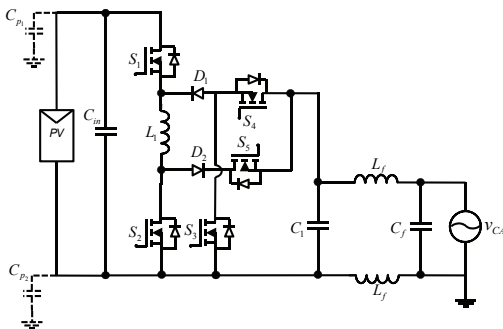


Fig. 7. Flying inductor topology

F. Flying inductor topology [11]

A flying inductor converter is shown in Figure 7. It is also known as the Karschny inverter. This topology has the advantage of having the negative PV array connected directly to the neutral terminal of the grid. However, not only it requires more diodes than the H-Bridge but also most of the switching states have three devices conducting at the same time, which become a serious demerit since reduces efficiency.

G. Common Mode Topology

An unusual topology is reported in [22], which connects the PV negative terminal to the neutral line of the utility grid, shown in Figure 8. It is easily seen that the input voltage may be similar to the traditional H-bridge inverter. However, its operation is not only complex, but also the required number of components is considerably higher than the normally used.

III. PROPOSED TOPOLOGY

The circuit diagram for the proposed inverter is shown in Figure 9. The main idea is like in literature [11] and [22] that has the neutral terminal of the grid also connected straight to the negative PV array. The topology is composed by two power MOSFETs (S_1 and S_2), and just a single device is conducting in each switching state. The converter includes two capacitors and three inductors (C_f , C_{dc} and L_1 , L_2 , L_f).

Since the negative of the PV array is connected straight to the neutral line of the grid, the ground leakage current is very low for our proposed topology, while the applied voltage to the parasitic capacitance is maintained almost constant (only appear low frequency variations).

Waveforms, for the converter, are shown in Figure 10. Control signals, for the switches S_1 and S_2 , are also included. According to this figure the converter operates as follows:

- 1) During $t_0 - t_1$. The positive switching state is used at this time, where S_1 is turned on and S_2 is turned off (Figure 9.b). During this switching state, the input voltage (PV voltage) is applied to the LCL output filter, which provides a positive voltage (V_{AB}). It should be noticed the polarity of the capacitor voltage (C_{dc}), where the inductor L_1 is

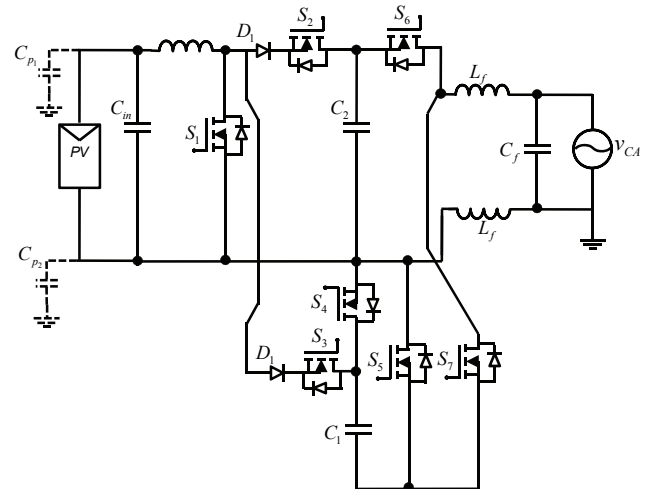


Fig. 8. Common Mode Inverter proposed in [22]

discharged into the capacitor.

- 2) *During $t_1 - t_2$.* The negative switching state is applied at this time, where S_1 is turned off and S_2 is turned on (Figure 9.c). The capacitor voltage, C_{dc} , is applied to the output filter, which provides in this form a negative voltage to the LCL output filter (V_{AB}). At this stage, the inductor L_1 is charged from the PV panel.

The proposed converter is able to provide AC current to the AC mains with an appropriate controller, since the converter may provide a positive or negative voltage depending on the switching state. Typical waveforms for the converter at low frequency are shown in Figure 10.b. These were obtained by numerical simulation.

It should be noticed that the positive voltage is lower than the negative voltage. Due to this a traditional modulator cannot be used because a voltage unbalance may occur. For regulating the injected current to the AC mains, it is suggested to use a closed loop controller.

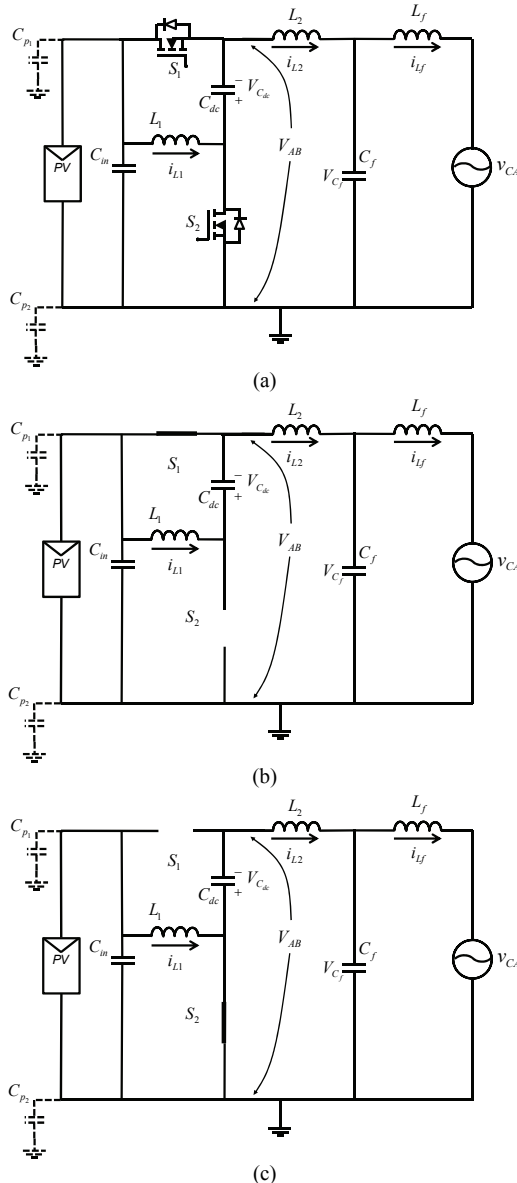


Fig. 9. Proposed topology. a) Converter, b) Subcircuit during $t_0 - t_1$, c) Subcircuit during $t_1 - t_2$

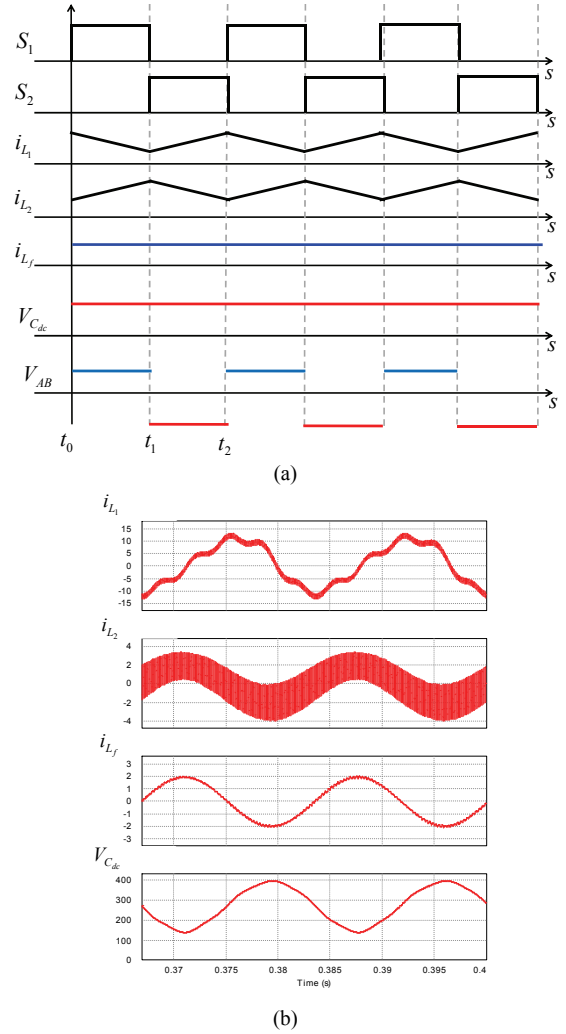


Fig. 10. Waveforms of the converter. a) at high frequency, but positive semicycle, b) at low frequency

The input voltage of the inverter should be higher than the peak of the utility line in order to inject current to the AC mains. The required voltage may be obtained depending on the amount of PV panels connected in series; however, it is also possible to consider a DC/DC boost converter for increasing the voltage, in case of few PV panels are installed.

A. Model of the Converter

The parasitic resistor of each inductor is considered to obtain the model of the proposed converter.

The obtained system of equations for the converter when S_1 is turned on and S_2 is turned off, is written as:

$$\begin{bmatrix} i'_{L1} \\ i'_{L2} \\ i'_{Lf} \\ v'_{Cdc} \\ v'_{Cf} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{R_{Lf}}{L_f} & 0 & -\frac{1}{L_f} \\ \frac{1}{C_{dc}} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{Lf} \\ v_{Cdc} \\ v_{Cf} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i + \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} v_{ac} \quad (1)$$

where: L_1, L_2, L_f are the inductances of the circuit
 C_f is the capacitance of the output filter

C_{dc} is the capacitance of the bulky capacitor
 R_{L1}, R_{L2}, R_{Lf} are the parasitic resistance of the inductors
 v_i, v_{ac} are the input and AC mains voltage respectively

The system of equations, when S_1 is turned off and S_2 is turned on, is:

$$\begin{bmatrix} i'_{L1} \\ i'_{L2} \\ i'_{Lf} \\ v'_{Cdc} \\ v'_{Cf} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & -\frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & -\frac{R_{Lf}}{L_f} & 0 & \frac{1}{L_f} \\ 0 & \frac{1}{C_{dc}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{Lf} \\ v_{Cdc} \\ v_{Cf} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i + \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} v_{ac} \quad (2)$$

The full bilinear model may be obtained as follows:

$$X' = [A_1d + A_2(1-d)]X + [B_1d + B_2(1-d)]v_i + [C_1d + C_2(1-d)]v_{ac} \quad (3)$$

where: d is the duty cycle

Finally, the complete model of the system may be re-written as:

$$\begin{bmatrix} i'_{L1} \\ i'_{L2} \\ i'_{Lf} \\ v'_{Cdc} \\ v'_{Cf} \end{bmatrix} = \begin{bmatrix} -\frac{R_{L1}}{L_1} & 0 & 0 & -\frac{d}{L_1} & 0 \\ 0 & -\frac{R_{L2}}{L_2} & 0 & -\frac{1-d}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & -\frac{R_{Lf}}{L_f} & 0 & \frac{1}{L_f} \\ \frac{d}{C_{dc}} & \frac{1-d}{C_{dc}} & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & -\frac{1}{C_f} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{Lf} \\ v_{Cdc} \\ v_{Cf} \end{bmatrix} + \begin{bmatrix} \frac{1-d}{L_1} \\ \frac{d}{L_2} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i + \begin{bmatrix} 0 \\ 0 \\ -\frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} v_{ac} \quad (4)$$

When 'd' takes a unit value, it physically implies that S_1 is turned on and S_2 is turned off; while 'd' takes a zero value, then S_1 is turned off and S_2 is turned on.

B. Proposed controller

The difference in the voltage between the positive and negative switching state does not allow using a traditional PWM modulator for the proposed inverter. Instead of this, it is proposed to use a controller that employs a different modulation scheme such as sliding mode control (SMC).

SMC offers some advantages such as stability, robustness under input voltage variations, good dynamic response and simple implementation. Therefore, this controller is suitable for our purpose. Certainly the control theory involved is rather complex compared to the traditional control theory.

The system is forced by SMC to maintain itself into the sliding surface; then the system is driven towards the equilibrium point.

Due to the application, it is proposed to use the error current through the inductor L_2 as the sliding surface, this means:

$$\sigma = ex_2 = 0 \quad (5)$$

where: ex_2 is the error between i_{L2} and the reference i_{L2r}

i_{L2} is the current of L_2 ,

$i_{L2r} = k \sin(\omega t)$ is the current reference

The sliding surface must be satisfied by the equation that guarantees the existence of sliding mode [27-28]:

$$\sigma \cdot \sigma' < 0 \quad (6)$$

where: σ' is the tangent vector of σ

Obtaining σ' by using (4) and (5) gives:

$$\sigma' = -\frac{R_{L2}i_{L2}}{L_2} + \frac{(d-1)v_{Cdc}}{L_2} - \frac{v_{Cf}}{L_2} + \frac{dv_i}{L_2} - \omega k \cos(\omega t) \quad (7)$$

The two possible values of the duty cycle are as follows:

$$d = \begin{cases} 1, & \sigma < 0 \\ 0, & \sigma > 0 \end{cases} \quad (8)$$

Expression (7) should be evaluated by using (8) and (9) for the positive and negative possible values of σ . When σ takes a positive value, the σ' variable must be negative to fulfill (7), particularly, in this case, there exist two conditions in regards of the current reference amplitude k :

$$k > \frac{-v_{Cdc} - v_{Cf} - R_{L2}i_{L2}}{L_2\omega} \quad (9)$$

$$k > \frac{v_{Cdc} + v_{Cf} + R_{L2}i_{L2}}{L_2\omega} \quad (10)$$

The other possible case is when σ is negative, then σ' must be positive and the next two similar conditions result again:

$$k < \frac{v_i - v_{Cf} - R_{L2}i_{L2}}{L_2\omega} \quad (11)$$

$$k < \frac{-v_i + v_{Cf} + R_{L2}i_{L2}}{L_2\omega} \quad (12)$$

Considering (9)-(12), one of the conditions is the most restrictive, and it also satisfies the expression (6):

$$k < \frac{v_i - v_{Cf} - R_{L2}i_{L2}}{L_2\omega} \quad (13)$$

The equivalent control technique in SMC may be employed for analyzing the steady state of the system [27]. The equivalent control is obtained by considering that the system is already held into the sliding surface. The equivalent control expression is obtained from the equation (7) which is made equal to zero. It is finally obtained as:

$$d_{eq} = \frac{R_{L2}i_{L2} + v_{Cdc} + v_{Cf} + kL_2\omega \cos(\omega t)}{v_{Cdc} + v_i} \quad (14)$$

The system is decoupled by the proposed controller, once the converter is into the sliding surface, then the inductor L_2 may be substituted by a current source. Therefore, the system of equations for the output becomes:

$$\begin{bmatrix} i'_{Lf} \\ v'_{Cf} \end{bmatrix} = \begin{bmatrix} -\frac{R_{Lf}}{L_f} & \frac{1}{L_f} \\ -\frac{1}{C_2} & 0 \end{bmatrix} \begin{bmatrix} i_{Lf} \\ v_{Cf} \end{bmatrix} + \begin{bmatrix} -\frac{v_{ac}}{L_f} \\ \frac{k \sin(\omega t)}{C_2} \end{bmatrix} \quad (15)$$

Please notice that (15) is stable because eigenvalues have negative real parts.

For implementation purposes, the SMC requires a switching frequency limiter and a maximum power point tracker (MPPT). Figure 11 shows a two stage PV system, which includes the current reference generation for the SMC (phase

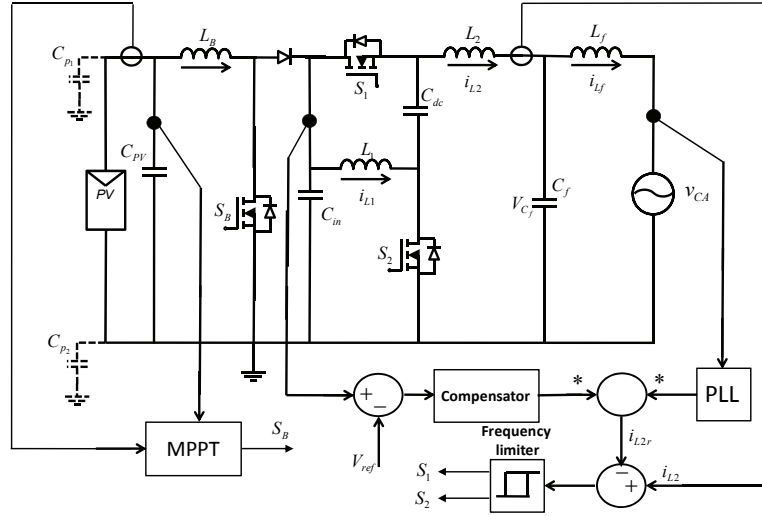


Fig. 11. Block diagram of two stage PV system: controller and power stage

lock loop (PLL), voltage compensator and a multiplier), a DC/DC boost converter, and a maximum power point tracker (MPPT).

C. Steady state operation

Numerical simulation is the best way to establish the steady state behavior of the system, this is given because of the circumstances where the converter operates on AC and the resultant equations are nonlinear; the steady state equations can be obtained by substituting (14) in (4). The waveform for the state variables, shown in Figure 10.b, neglects the parasitic resistances of the inductors.

These graphs may be used for obtaining the voltage and current stress of the passive elements, as a result of this, the semiconductor stress may be determined too. The voltage stress of the semiconductor is established by the switching states, so that, the voltage stress of the semiconductors is $V_i + V_{dc}$.

D. Design procedure

The proposed converter operates at high frequency; however, some elements should be designed not only at this high frequency, but also some others at low frequency.

The output current filter may easily be designed by choosing both a desired filter corner frequency and a small capacitor value. Once this is established, the inductor may be estimated by:

$$L_f = \frac{1}{C_f(2\pi f_c)^2} \quad (16)$$

where: f_c is the corner frequency of the filter.

Considering $f_c = 4$ kHz and $C_f = 2.2$ μ F, L_f is obtained as 720 μ H; however, in practice it is approximated to 1mH. Due to the symmetry of the filter, L_2 is selected by the same value of L_f . It should be noticed that the design procedure for this filter should be different, like the proposed in literature [29].

The following equation is considered for obtaining L_1 :

$$L_1 = \frac{V_i(1-D)}{\Delta I_L f_s} \quad (17)$$

where: ΔI_L is desired ripple at the inductor

Considering $f_s = 40$ kHz, $D = 0.5$, $V_i = 250$ V and $\Delta I_L = 1.5$ A is calculated $L_1 = 2$ mH. At the zero crossing of the AC mains voltage, the converter has a duty cycle of 0.5, this time was selected for the design.

The capacitor C_{dc} was calculated by considering its stored energy to alleviate the low frequency of the AC mains, then it may be calculated by:

$$C_{dc} = \frac{2\xi}{V_{dc}^2} \quad (18)$$

where: ξ is the energy stored in the capacitor

V_{dc} is the capacitor voltage

Considering $V_{dc} = 250$ V and $\xi = 3.32$ J (which corresponds approximately to the energy handled during a cycle in the experimental prototype). C_{dc} is obtained as 106 μ F, but it is approximated to 110 μ F; for practical purposes, an electrolytic type was selected.

E. Bonding the switching frequency

An ideal sliding mode controller implies an infinite switching frequency, and then in a practical implementation this switching frequency must be bounded.

Different techniques may be used to limit the switching frequency [30-31]. This paper considers the hysteresis method, because its simplicity for practical realization.

F. Comparison with other schemes

The proposed topology is compared in this section with other schemes that connect the PV negative terminal with the neutral of the grid, where also the NPC topology was included. All these schemes certainly offer a very low leakage current.

For comparative purposes, the amount of semiconductors, the passive elements and the stress of the semiconductors are considered. The proposed converter, not only has fewer semiconductors than other topologies, but also, it has fewer or almost the same amount of passive elements than the other

schemes, as it may be easily seen in Table I. The input voltage in all the converters must be higher than the peak of the AC mains voltage; however, the NPC topology requires the double of the voltage. It should be noticed that the voltage stress at the semiconductor is similar to the NPC and [25] scheme.

It is important to notice that [25] is intended for split phase applications and additionally solve the low frequency current issues at the PV panel. But the topology does not consider an LCL output filter, just a simple inductor filter.

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

A. Simulation results

The converter was numerically simulated for evaluating the performance of this proposed inverter.

The parameters used for these simulations are:

$C_{in}=250\mu F$, $C_{dc}=110\mu F$, $C_f=2.2\mu F$, $L_1=2mH$, $L_2=1mH$, $L_f=1mH$, $f_{sw}=40kHz$, $P_o=200W$.

The converter performance at steady state is shown in Figures 12 and 13. Figure 12 shows the output current, which has a small ripple. The output voltage of the inverter before output filter is also illustrated. It has two levels and its frequency is equal to the switching frequency, where a zoomed view at the zero crossing of the AC mains is also included.

The leakage current through the parasitic capacitance of the proposed converter is shown in Figure 13.d. This leakage current is very small. There exist current just in a single capacitance due to the connection between the neutral of the grid and the negative of the PV array.

B. Comparison with other topologies by simulation

Different simulations were carried out to compare the obtained results of the proposed converter with some other schemes. The comparison is made with converters that do not connect the negative terminal of the PV with the neutral.

A comparison of the leakage current of different PV inverter topologies with the proposed one is shown in Figure 13, where each one is operating under the same conditions. The considered converters were the H-bridge unipolar [11], H5 and H6. The same current scale was used in order to

appreciate clearly differences among them.

The H-bridge unipolar topology has the biggest leakage current, as shown in Figure 13.a (actually the current is over the selected scale), compared with the H5 and H6 topologies that exhibit a smaller leakage current, as illustrated in Figure 13.b and 13.c. Remarkably the proposed topology offers smaller leakage current, as easily seen in Figure 13.d.

C. Experimental Results

An experimental prototype was designed and built in order to verify the performance of the proposed converter. The parameters are:

$C_{in}=250\mu F$, $C_{dc}=110\mu F$, $C_f=2.2\mu F$, $L_1=2mH$, $L_2=1mH$, $L_f=1mH$, $f_{sw}=40kHz$, $P_o=200W$. The MOSFETs used during the tests were: C2M0080120D, Silicon Carbide Power MOSFET. The parasitic capacitance of the PV panel to the ground is 5nF.

The experimental setup was designed for applications

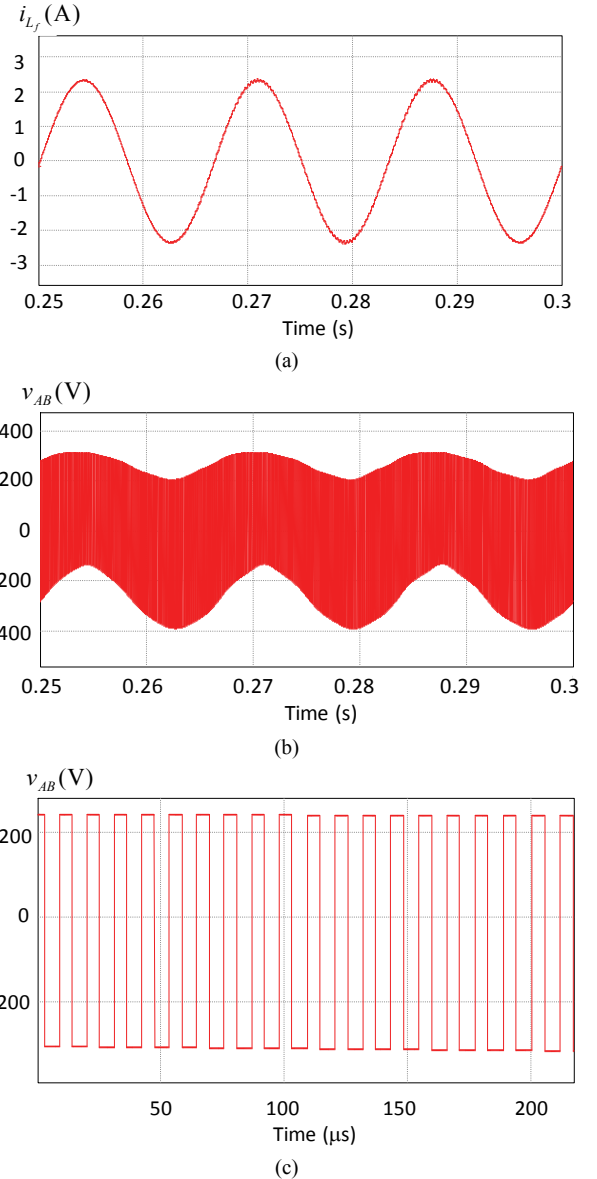


Fig. 12. Performance at steady state: (a) output current, (b) output inverter voltage before filter, (c) zoom of output voltage

TABLE I
COMPARISON OF THE PROPOSED CONVERTER

Converter	Semiconductors			Passive components	
	Voltage stress	Switches	Diodes	Ls	Cs
NPC Converter	$>2V_{pk}$	4	2	2	3
Flying Inductor	$>V_{pk}$	4	2	3	3
Common mode Ref. [21]*	$>V_{pk}$	6	1	2	3
Common mode Ref. [25]	$>2V_{pk}$	6	0	3	2
Proposed	$>2V_{pk}$	2	0	2	3

V_{pk} is the voltage peak of the AC mains

*Is not considered the dc/dc boost converter of the topology

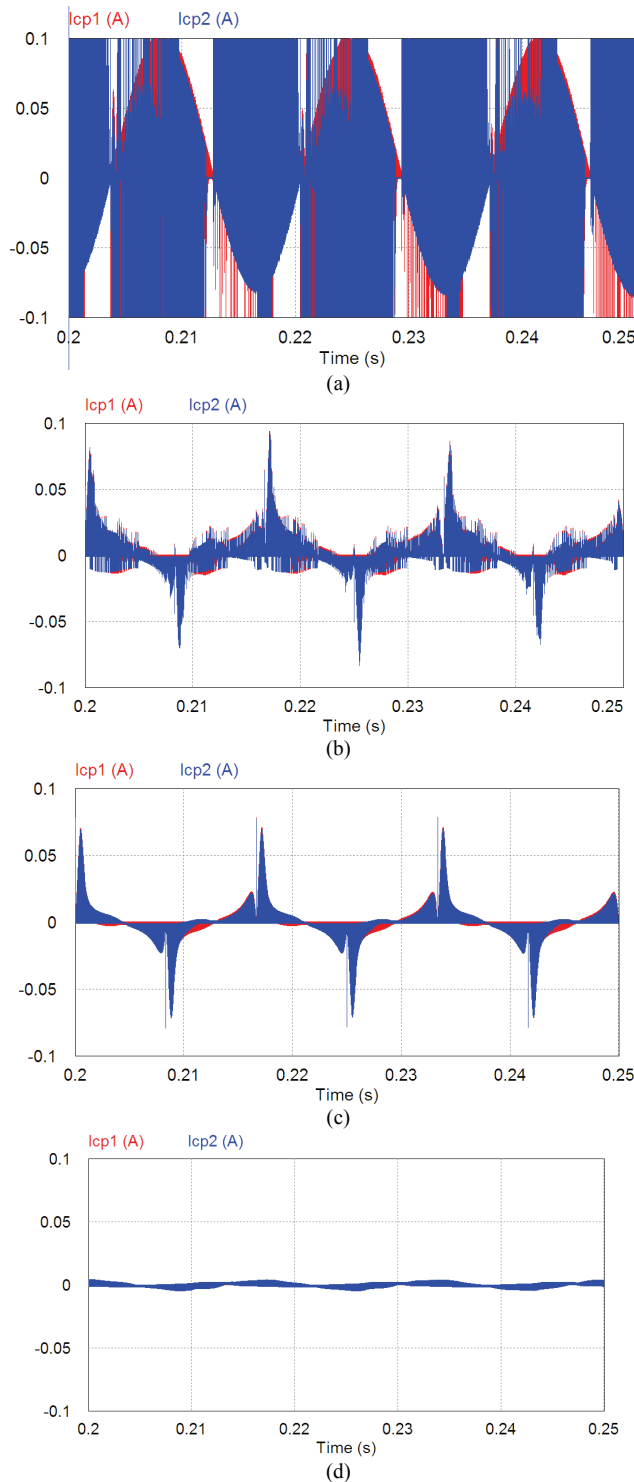


Fig. 13. Leakage current in some PV inverters topologies: (a) H-bridge unipolar, (b) H5, (c) H6, and (d) Proposed topology

which consider a DC/DC boost converter in order to connect the PV panel and the inverter input, as shown in Figure 11. This arrangement is able to prevent PV panels from the 120 Hz input ripple current. This proposal is capable of operating from PV panels connected in series, without the DC/DC boost converter; and this is carried out with a bulky capacitive filter which that reduces the low frequency issues.

Converter performance is illustrated in Figures 14 through 18. The AC mains voltage and the output current injected into

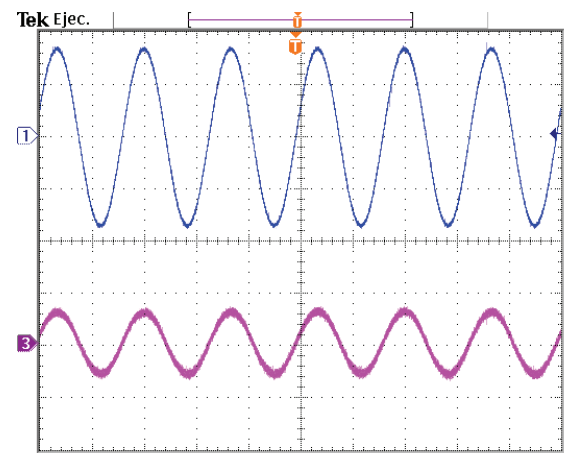


Fig. 14. Waveforms at the output. Top to bottom: AC mains voltage (100V/div), Output current (5A/div), Time 10ms/div

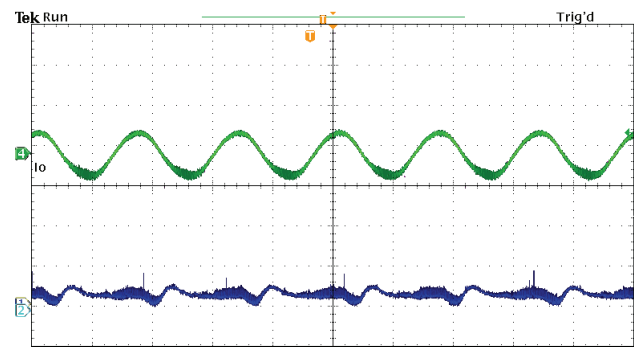


Fig. 15. Leakage current and output current. Top to bottom: Output current (5A/div), leakage current (5mA/div), Time 10ms/div

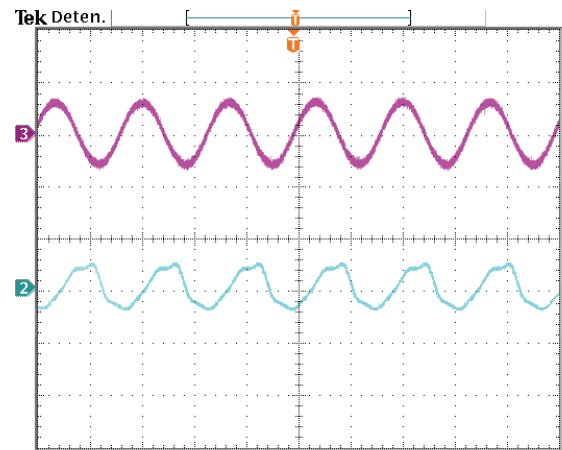


Fig. 16. Current waveforms of the converter. Top to bottom: Output current (5A/div), Inductor L_1 current (20A/div), Time 10ms/div

the grid are shown in Figure 14. It may easily be seen that these are in phase and the distortion is low.

The low leakage current through the parasitic capacitance that was obtained by simulations may be observed in Figure 15. The leakage current is shown at the bottom of the figure, with a scale of 5 mA per division. It also shows the injected current (top).

The current waveforms of the converter at steady state are illustrated in Figure 16. The inductor current L_1 and the output current are also shown. The voltage waveforms of the converter at steady state are shown in Figure 17, where the

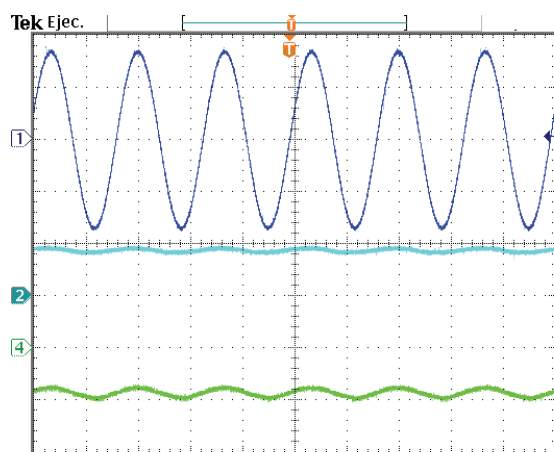


Fig. 17. Voltage waveforms of the converter. Top to bottom: AC mains voltage (100V/div), Input voltage (250V/div), Capacitor C_{dc} voltage (250V/div). Time 10ms/div

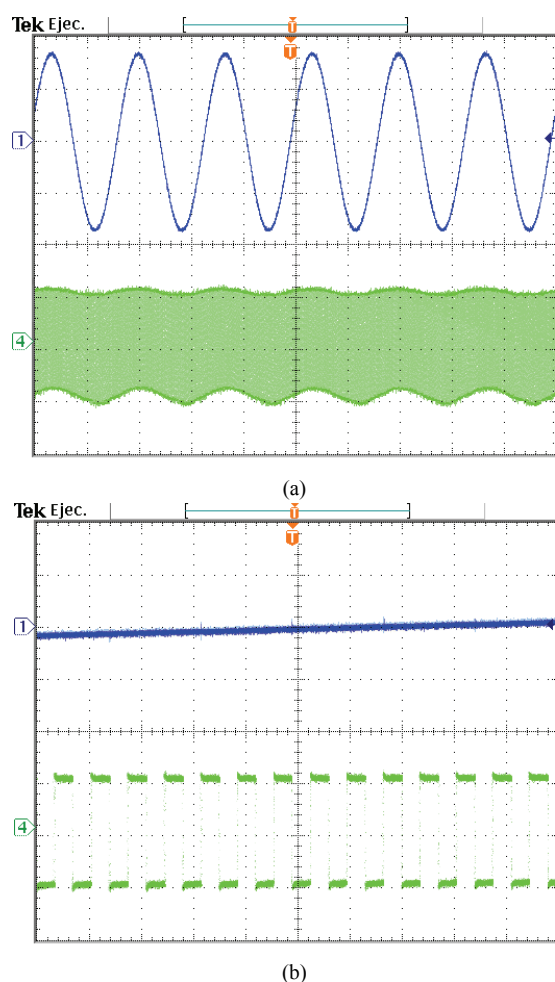


Fig. 18 Inverter output voltage. Top to bottom: ac mains voltage (250V/div), inverter output ((250V/div). Time 40μs/div. a) At low frequency, b) At high frequency

input voltage, the AC mains voltage and the bulky capacitor C_{dc} voltage are included.

The output inverter waveform is shown in Figure 18. Figure 18.a illustrates the operation at the AC mains time scale. But, it has also been included in Figure 18.b a zoomed view at the zero crossing of the AC mains.

The proposed inverter efficiency is 96%, not includes the DC/DC boost converter. This value considers the California Energy Commission (CEC) efficiency that consists of a weighted efficiency.

V. CONCLUSION

Transformerless PV inverter has many advantages, for instance: cost, size, and weight reduction. In addition, it increases the whole system efficiency, certainly depending on the topology a leakage current should appear.

Recently, many topologies of transformerless PV inverters have been proposed, trying to reduce the leakage current at the ground connection. Following this trend, this paper proposes a new transformerless inverter for PV generation systems.

The main features of this proposed topology are: in the first place, the negative of the PV array is connected directly to the neutral of the grid greatly reducing the ground leakage current through the parasitic capacitance; and in second place, the topology only uses two MOSFETs reducing cost of the whole system.

The results of this paper indicate that this proposal offers a good choice for smaller values of leakage current. The experimental prototype has been designed and tested for ensuring the inverter operation. The obtained results show clear evidence that the proposal is suitable for PV inverters connected to the AC mains. In addition, several alternatives for PV inverter have been compared with the proposed inverter.

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