High-Frequency-Fed Unity Power-Factor AC–DC Power Converter With One Switching Per Cycle

Chi-Kwan Lee, *Senior Member, IEEE*, Sitthisak Kiratipongvoot, and Siew-Chong Tan, *Senior Member, IEEE*

***Abstract*—This paper presents a power converter and its control circuit for high-frequency-fed ac to dc conversion. Based on the resonant technique, the input current is shaped to be sinusoidal and is forced to follow the high-frequency sinusoidal input voltage so as to achieve unity power factor. With the proper selection of the characteristic impedance of the resonant tank, the converter is able to perform the function of a buck, boost, or buck–boost converter. The initial condition of the resonant tank is used to control the output voltage gain of the converter. Since all the switches are operated at the fundamental frequency of the input ac source, the switching loss of the converter is small. A control scheme is also proposed for the converter. A proof-of-concept prototype operating at 400 kHz is constructed and its performance is experimentally measured. Results show that the proposed converter operates as theoretically anticipated.**

***Index Terms*—AC to DC conversion, high-frequency rectifier, power factor (PF) correction, resonant technique, wireless power transfer (WPT).**

I. Introduction

EMERGING technologies such as wireless power transfer (WPT) often adopt a high operating frequency in the range from a few hundred of kHz to over 10 MHz [1]–[4]. Recently, much research effort has been devoted to improving the performance of WPT systems in terms of transfer distance and system's energy efficiency [5]–[9]. There is a lack of research targeting the optimal design of the power converter at the receiver side. Traditionally, the simplest approach is to use a diode rectifier circuit with an output storage capacitor, as shown in Fig. 1(a) [10]. However, this capacitor is charged to a value close to the peak of the ac input voltage [see Fig. 1(b)]. As a result, pulsating input current of large magnitude occurs near the peak of the ac input voltage. Discontinuous current implies that wireless power does not flow continuously from the primary side of the WPT system to the output of the system. Such diode rectifiers draw highly distorted current from the ac power source and result in a poor input power factor (PF). The energy efficiency and power transfer capability of a poor PF system are relatively low because of the high conduction loss in the power converters and transmission wires. Additionally, the distorted current has a rich high-order harmonic content which may cause the emission of electromagnetic interference (EMI) that affects the operation of neighbor electronic equipment.

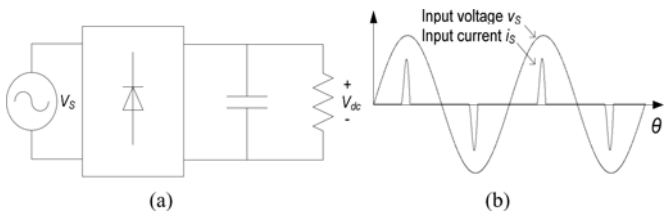


Fig. 1. (a) Diode rectifier with a capacitor connected at the dc output side. (b) Input voltage and current waveforms.

A power electronic converter such as a boost converter can be used to shape the input ac current drawn by the rectifier to be sinusoidal and in phase with the ac voltage [11]. Fig. 2(a) shows a classical boost converter connected after a diode bridge rectifier to form a PF correction (PFC) circuit. The output dc voltage is sensed and fed to an error amplifier. The difference between the actual and reference voltage is derived and applied to a compensator circuit such as a proportional-integral (PI) compensator. The output of the compensator is multiplied with the signal proportional to the ac voltage waveform $v_{\rm S}$ to produce the reference current signal $i_{L,\rm ref}$. Afterward, a current-mode controller is used to generate the ON and OFF signal to the switch shaping the current waveform of the inductor. Therefore, the average waveshape of the ac current is forced to follow the waveform of the ac voltage. Fig. 2(b) depicts the input ac current waveform of the converter. It can be observed that the switching frequency of the PFC converter must be several times higher than the frequency of the ac system. Using a 400-kHz ac transmission system as an example, applying this current-shaping technology implies that the power switch has to operate in the tens of MHz. As a result, the switching loss becomes significant and the efficiency of the converter sharply reduces.

Furthermore, MHz switching converter is also exposed to a number of problems arising from the passive and active components. For instance, the loss associated with the charging and discharging of the parasitic capacitance of power MOSFETs becomes significant [12], [13]. The high-frequency behavior of the devices is very different from that of the low-frequency behavior [14], [15]. In terms of using passive components in design, it is important to enhance their temperature stability and to minimize the unwanted stray and parasitic elements [15]. For the design of printed circuit board, it is crucial to eliminate undesired coupling between neighboring components and the rest of the circuit [16]. Without addressing these issues, the converter cannot be operated at a high frequency and achieved a high

Manuscript received February 20, 2014; revised May 2, 2014; accepted April 7, 2014. Date of publication June 12, 2014; date of current version November 3, 2014. This work was supported in part by the Hong Kong Innovation and Technology Fund under Project ITS/286/12. Recommended for publication by Associate Editor T.-J. (Peter) Liang.

The authors are with the Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong (e-mail: cklee@eee.hku.hk; ksitthis@eee.hku.hk; sctan@eee.hku.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2330631

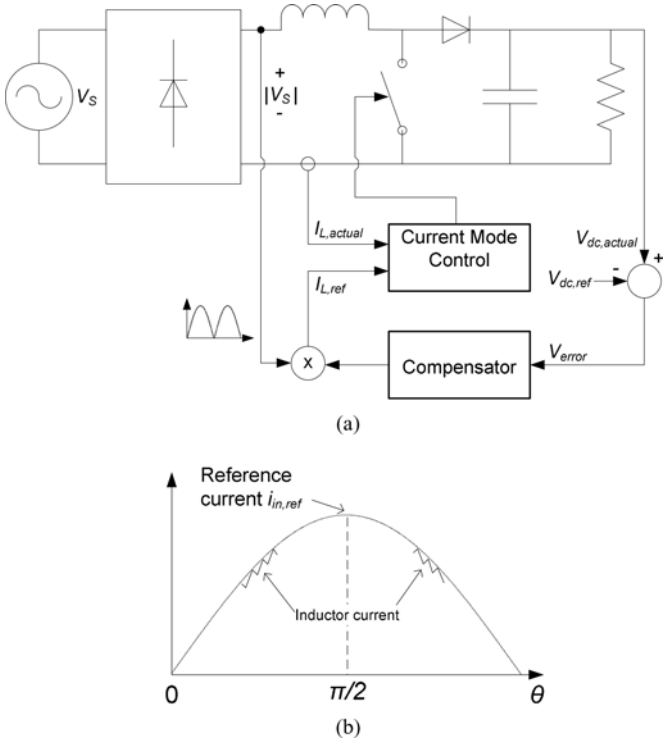


Fig. 2. (a) PF correction circuit. (b) Input voltage and current waveforms.

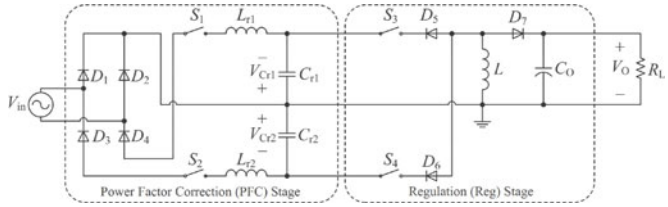


Fig. 3. Proposed high-frequency-fed ac–dc power converter.

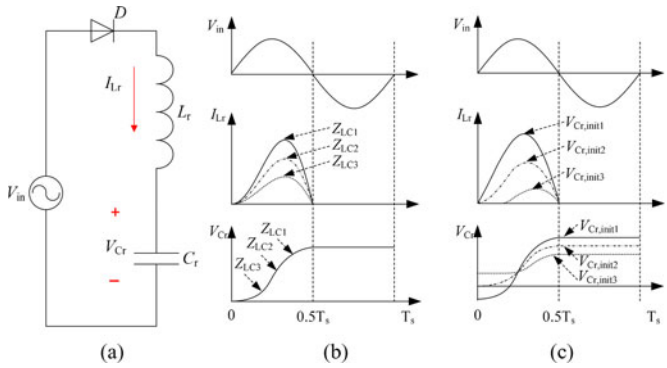


Fig. 4. (a) *LC* series resonant circuit diagram, and the input voltage, input current and resonant capacitor voltage waveforms: (b) with different equivalent impedance ($Z_{\rm LC}$); $Z_{\rm LC1} < Z_{\rm LC2} < Z_{\rm LC3}$, and (c) with different initial voltage of resonant capacitor $V_{\rm Cr,init1} < (V_{\rm Cr,init2} = 0) < V_{\rm Cr,init3}$.

efficiency [17]. In [18] and [19], device-level packaging and circuit interconnection technologies are proposed to substantially reduce the structural parasitics and to improve the thermal management. However, the thermal performance and EMI are still big challenges which are difficult to solve individually as they are closely related to the circuit layout and packaging [20].

The paper is organized as follows. In Section II, the concept of using inductor–capacitor (*LC*) series resonant circuit to perform PF correction will be introduced. The operating principle of the proposed high-frequency-fed ac–dc power converter will be explicitly described using the corresponding timing diagrams and equivalent circuit diagrams. Then, the voltage conversion ratio and efficiency of the converter will be analytically investigated and presented in Section III. Afterwards, the construction of a proof-of-concept prototype and its experimental measurement results will be discussed. Section V gives the conclusions of the paper.

II. Topology and Operating Principle

In this section, a high-frequency-fed ac–dc power converter is presented as given in Fig. 3 and its operating and control principles are explained [21]. The advantageous features of this converter include near-unity input PF and only one switching action per cycle for all the power switches.

A. LC Series Resonant Circuit

The PF conditioning property is performed using the *LC* series resonant circuit at the input stage. The operation of the positive half cycle is used to describe how the *LC* resonant circuit can perform PF control in the high-frequency ac–dc power converter. A simplified circuit diagram is shown in Fig. 4(a).

Assume that the source frequency is the same as the resonant frequency of the *LC* circuit $\omega = \omega_r = 1/[2\pi(L_r C_r)^{1/2}]$ and the initial current of the resonant inductor is zero. There are two parameters that will affect the amplitude and waveform of the inductor current. The first parameter is the equivalent impedance of the *LC* circuit which is designed by the resonant inductor and capacitor such that $Z_{LC} = (L_r/C_r)^{1/2}$, and the second parameter is the initial voltage of the resonant capacitor.

Fig. 4(b) shows the current and voltage waveforms of the *LC* resonant circuit with different equivalent impedances in the positive half cycle of the input voltage. The initial voltage of the resonant capacitor and the current of the resonant inductor are zero ($V_{\rm Cr,init} = 0$ and $I_{\rm Lr,init} = 0$). It can be observed that the source current is affected by the equivalent impedance of the *LC* circuit while the voltage waveform of the resonant capacitor remains the same. The total energy stored in the resonant capacitor over the positive half cycle is proportional to the size of the capacitance.

Fig. 4(c) shows the positive half cycle of the input voltage, the current of the resonant inductor, and the voltage of the resonant capacitor of the same circuit but with different initial conditions. It can be seen that the initial voltage value of the resonant capacitor can affect the magnitude of the resonant current of the inductor, of which the lower the initial resonant capacitor voltage, the higher the resonant inductor current becomes, and the lower the initial resonant capacitor voltage, the higher the capacitor voltage becomes at the end of the half cycle.

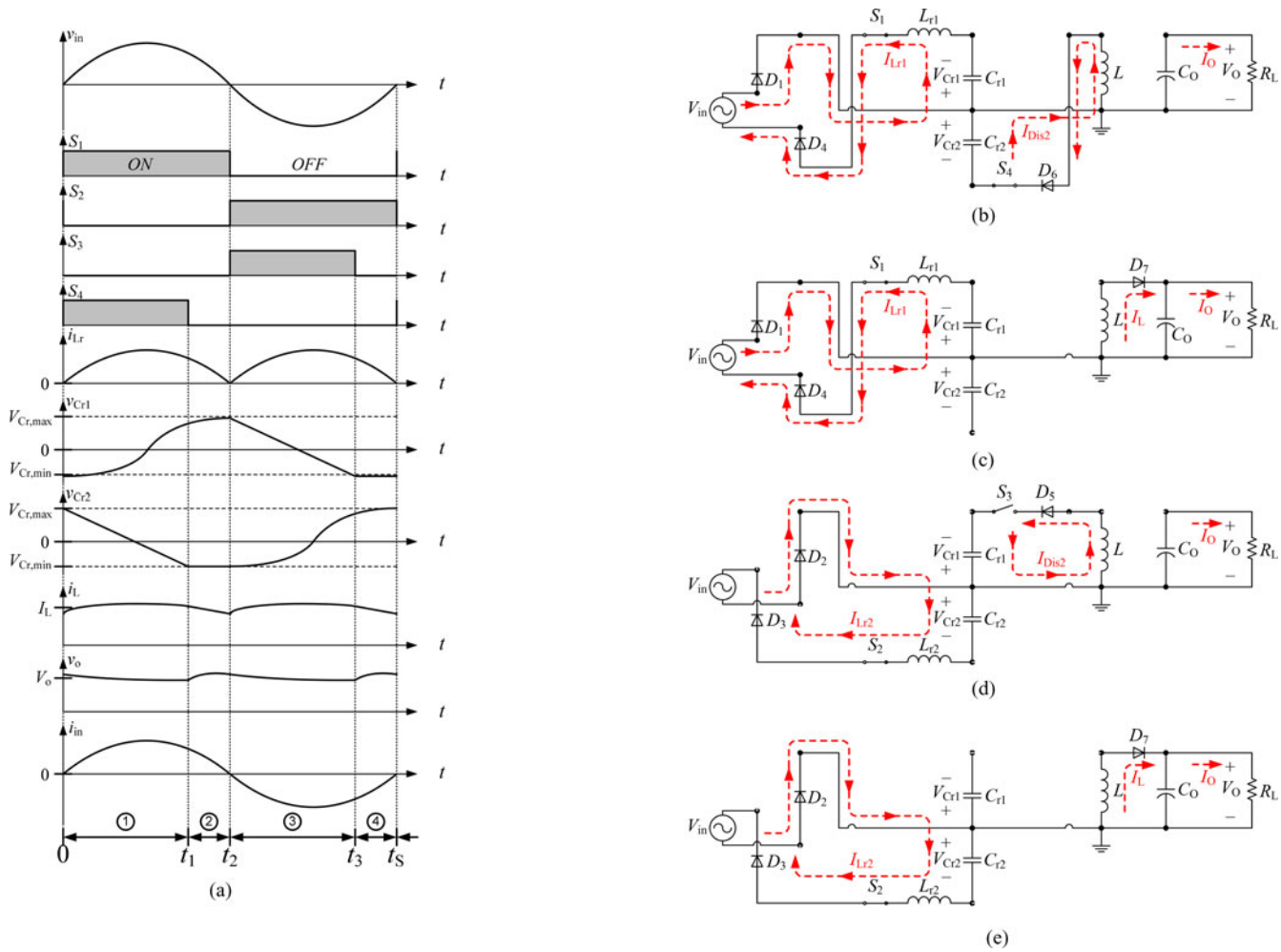


Fig. 5. (a) Timing diagrams of the converter. Equivalent circuit diagrams in each operating mode: (b) Mode 1, (c) Mode 2, (d) Mode 3, and (e) Mode 4.

B. Proposed Topology

The proposed two-stage circuit topology is shown in Fig. 3. The first stage (PFC stage) consists of two switches, four diodes, two resonant inductors, and two resonant capacitors. The second stage (regulation stage) consists of two switches, three diodes, one inductor, and one capacitor. In the PFC stage, the capacitor C_{r1} and C_{r2} are alternately charged by the input ac voltage source through the alternate switching actions of power switches S_1 and S_2. C_{r1} is charged in the positive half cycle and C_{r2} is charged in the negative half cycle. In the regulation stage, the capacitors C_{r1} and C_{r2}, which have been charged by the first-stage converter, is commutated alternately as energy sources for the second-stage converter. Note that the second stage can be implemented by several types of power converters. In this paper, the buck–boost converter was selected for illustrating the proposed idea. The proposed topology can achieve high PF by using the property of the series resonant circuit as discussed in Section II-A.

C. Timing Diagram and Operating Modes

The timing diagrams of the proposed high-frequency-fed ac–dc power converter are shown in Fig. 5(a). It can be seen that there are four operating modes as shown in Fig. 5(b) to 5(e). In the PFC stage, switches S_1 and S_2 are used to select the resonant tanks $L_{r1}-C_{r1}$ and $L_{r2}-C_{r2}$ for the positive and negative half-cycles, respectively. In the regulation stage, S_4 and S_3 are the switches for controlling the buck–boost converter for the positive and negative half-cycles, respectively. Here, it is assumed that $C_{r1} = C_{r2}$ and $L_{r1} = L_{r2}$.

Mode 1 $(0 < t < t_1)$*:* Prior to turning the switches S_1 and S_4 ON, the capacitor C_{r1} and C_{r2} are assumed to be charged to $V_{\mathrm{Cr,min}}$ and $V_{\mathrm{Cr,max}}$, respectively. The positive half-cycle begins at $t = 0$. In the PFC stage, switch S_1 is turned ON and switch S_2 is turned OFF. Diodes D_1 and D_4 are in the conducting state but diodes D_2 and D_3 are not conducting [see Fig. 5(b)]. L_{r1} and C_{r1} are connected in series forming a series resonant circuit. The first half of the resonance takes place and the inductor current starts from an initial value (zero), follows the first half of a sinusoidal waveform and then decreases to zero as D_1 and D_4 block the reverse current flow. Meanwhile, the voltage of capacitor C_{r1} is charged from its initial value $V_{\mathrm{Cr,min}}$ to a certain level at $t = t_1$.

In the regulation stage, switch S_4 is turned ON and diode D_6 is in its conducting state. Switch S_3 is turned OFF and diodes D_5 and D_7 are reverse biased. The inductor L is sufficiently large

such that the current i_L can be assumed to be a constant magnitude. Capacitor C_{r2} and inductor *L* form a closed circuit. C_{r2} is discharged in one direction due to the polarity of diode D_6 until the voltage of capacitor C_{r2} is equal to the minimum voltage of capacitor $C_{r2}(V_{\mathrm{Cr,min}})$. The minimum voltage of capacitor C_{r2} is either a positive voltage ($V_{\mathrm{Cr,min}} > 0$), zero voltage ($V_{\mathrm{Cr,min}} = 0$), or negative voltage ($V_{\mathrm{Cr,min}} < 0$) depending on the output power. Energy is transferred from the PFC stage to the regulation stage and is stored in the inductor *L*. In this time period, the output capacitor C_O delivers energy to the output load resistor R_L.

Mode 2 ($t_1 < t < t_2$)*:* In the PFC stage, the functions of the switches (S_1 and S_2) and diodes (D_1, D_2, D_3, and D_4) are the same as that in Mode 1. Thus, the capacitor C_{r1} is kept charging by the power source to the level $V_{\mathrm{Cr,max}}$ at $t = t_2$, at which the positive cycle ends. Now, I_{Lr1} becomes zero and the switch S_1 is commutated OFF naturally. The diodes D_1 and D_4 become nonconducting. In the regulation stage, S_3 and D_5 remain in the OFF state. S_4 is turned OFF at $t = t_1$ and D_6 is reverse biased when the voltage of C_{r2} is equal to $V_{\mathrm{Cr,min}}$. Now, capacitor C_{r2} is not connected to the PFC or the regulation stage. The current of inductor *L* cannot be changed instantaneously, resulting in the forward-biased conduction of diode D_7. Therefore, the energy stored in inductor *L* is delivered to theoutput capacitor C_O and the load resistor R_L.

Mode 3 ($t_2 < t < t_3$)*:* In the negative half-cycle of v_{in}, the negative part of the waveforms are similar to that of the positive half-cycle. In the PFC stage, switch S_2 is turned ON and switch S_1 is turned OFF. Diodes D_2 and D_3 are in the conducting state while diodes D_2 and D_3 are reverse biased [see Fig. 5(d)]. Resonant tank $L_{r2} - C_{r2}$ is connected in series with the input source V_{in}. The input current i_{in} is shaped as a sinusoidal waveform. The voltage on capacitor C_{r2} is charged from the initial value $V_{\mathrm{Cr,min}}$ to $V_{\mathrm{Cr,max}}$. Energy is transferred from the input source V_{in} to capacitor C_{r2}. In the regulation stage, switch S_4 and diode D_6 remain in the OFF state. Switch S_3 is turned ON. Diode D_5 is in the conducting state while D_7 is reverse biased. The energy stored in resonant capacitor C_{r1} is transferred to inductor L.C_{r1} is discharged to *L* until the voltage of capacitor C_{r1} is equal to $V_{\mathrm{Cr,min}}$. Similarly to Mode 1, the load resistor R_L is supplied by the output capacitor C_O.

Mode 4 ($t_3 < t < t_S$)*:* In the PFC stage, the switching state of the switches (S_1 and S_2) and diodes (D_1, D_2, D_3, and D_4) are the same as that in Mode 3. In the regulation stage, switch S_3 is turned OFF at $t = t_3$ when the voltage of C_{r1} is equal to $V_{\mathrm{Cr,min}}$. Energy stored in inductor *L* is transferred to output capacitor C_O and load resistor R_L through diode D_7. Its equivalent circuit diagram is shown in Fig. 5(e). Switch S_2 is commutated OFF naturally when input source V_{in} becomes positive at $t = t_S$. Afterward, switches S_1 and S_4 are turned ON and the positive part of the operation is repeated.

D. Control Methodology

Fig. 6 shows the control block diagram of the proposed high-frequency-fed ac–dc power converter. In the PFC stage, the ac source voltage V_{in} is sensed and fed to a phase detector circuit as shown in Fig. 6(b). The outputs of the phase detector circuit are connected to the driver circuit to control the ON/OFF time of switches S_1 and S_2 following the ac source frequency. The signals Crt_S_1 and Crt_S_2 are the control signals of switches S_1 and S_2, respectively.

The outputs of the phase detector are also applied to the pulse-width modulation generator to derive the control signals Crt_S_3 and Crt_S_4 for switches S_3 and S_4, respectively. The instantaneous output voltage V_O is sensed and subtracted from the reference output voltage V_{Ref}, of which the error is applied to a compensator to generate the threshold voltage $V_{\mathrm{Cr,min}}$ for the resonant capacitors C_{r1} and C_{r2}. Fig. 6(c) shows the control circuit of the regulation stage where the instantaneous voltage of the resonant capacitors V_{Cr1} and V_{Cr2} are being sensed and compared with $V_{\mathrm{Cr,min}}$ to generate the pulse width of the switches S_3 and S_4. It is important to note that the proposed control circuit can be realized using simple operational amplifiers and digital logic gates. Consequently, they can be easily fabricated as an integrated circuit (IC) for mass production.

III. Circuit Analysis

A. Voltage Conversion Ratio

The derivation of the voltage conversion ratio of the proposed converter is presented in this section. For simplicity, all diodes and switches are considered ideal. In the PFC stage, an *LC* series resonant circuit is connected in series with the high-frequency ac source. The instantaneous current and voltage of the resonant inductor L_r and capacitor C_r in the half-cycle of the ac source can be described by (1) and (2). The detailed derivation of (1) and (2) are presented in Appendix A:

$$i_{\mathrm{Lr}}(s) = \begin{cases} 0 & \text{for } t \le t_\alpha \\ \left(\dfrac{\hat{V}_{\mathrm{in}}\sin(\alpha) - 2V_{\mathrm{Cr,min}}}{2Z_{LC}}\right)\sin(\omega t - \alpha) & \text{for } t_\alpha < t \le \dfrac{\pi}{\omega} \\ \quad + \dfrac{\hat{V}_{\mathrm{in}}\omega}{2Z_{LC}} t\sin(\omega t) & \end{cases} \tag{1}$$

$$v_{\mathrm{Cr}}(s) = \begin{cases} V_{\mathrm{Cr,min}} & \text{for } t \le t_\alpha \\ \dfrac{\hat{V}_{\mathrm{in}}}{2}\cos(\alpha)\sin(\omega t - \alpha) & \text{for } t_\alpha < t \le \frac{\pi}{\omega} \\ \quad -\dfrac{\hat{V}_{\mathrm{in}}}{2}(\omega t - \alpha)\cos(\omega t) & \\ \quad + V_{\mathrm{Cr,min}}\cos(\omega t - \alpha)) & \end{cases} \tag{2}$$

$$\alpha = \arcsin\left(\frac{V_{\mathrm{Cr,min}}}{\hat{V}_{\mathrm{in}}}\right). \tag{3}$$

In (1) and (2), $\hat{V}_{\mathrm{in}}$ and ω are, respectively, the peak voltage and angular frequency of the ac source. $V_{\mathrm{Cr,min}}$ is the minimum voltage or the initial voltage of the resonant capacitor. Z_{LC} is the characteristic impedance of the *LC* resonant circuit. α is

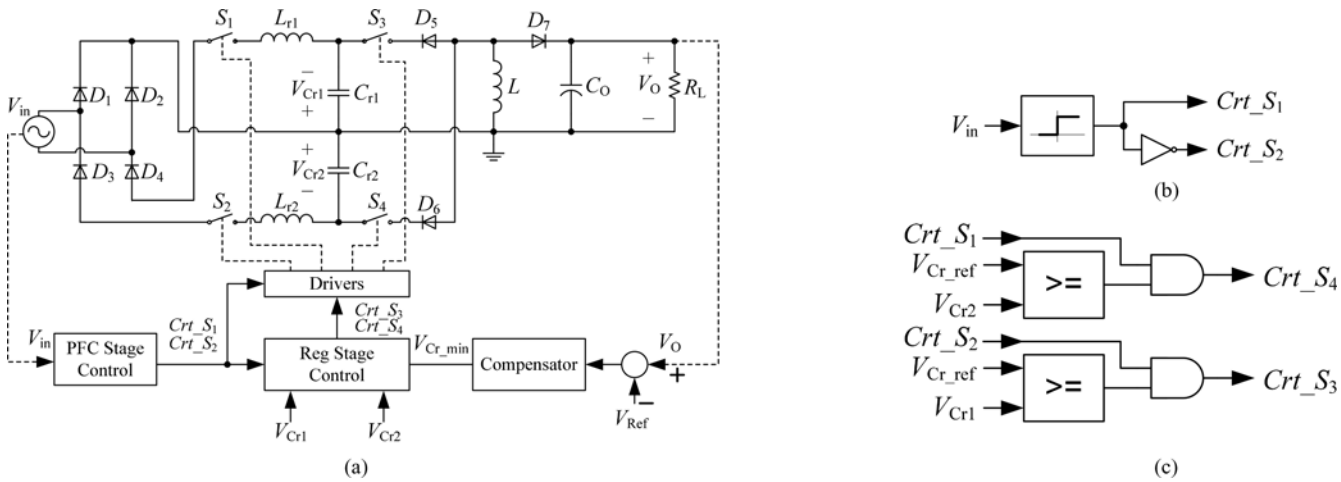


Fig. 6. (a) Overall control block diagram, (b) control circuit of the PFC stage, and (c) control circuit of the regulation stage.

the delay angle when the diode becomes forward-biased (i.e., $v_{\rm in} > V_{\rm Cr,min}$), which can be determined using (3). Thus, the corresponding delay time t_α is equal to α/ω. Substituting $t = \frac{\pi}{\omega}$ into (1) and (2), the current of the resonant inductor and the voltage of the resonant capacitor at the end of the half cycle of the ac source can be obtained. The current of the resonant inductor is zero and the maximum voltage of the resonant capacitor, i.e., $V_{\rm cr,max}$ is

$$V_{\rm Cr,max} = \frac{\hat{V}_{\rm in}}{4}\left[\sin(2\alpha) + 2(\pi - \alpha)\right] - V_{\rm Cr,min}\cos(\alpha). \quad (4)$$

Thus, the input energy $E_{\rm Cr}$ stored in the resonant capacitor can be obtained as

$$E_{Cr} = \frac{1}{2}Cr\left(V^2_{\rm Cr,\,max} - V^2_{\rm Cr,\,min}\right) \quad (5)$$

where C_r is the capacitance of the resonant capacitor.

In the regulation stage, the output energy E_O delivered to the resistive load in the half cycle of the ac source can be expressed as

$$E_O = \frac{V_O^2}{R_L} \times \frac{\pi}{\omega} \quad (6)$$

where V_O is the average output voltage of the converter.

Neglecting the power losses associated with all the circuit elements, the input energy $E_{\rm Cr}$ is equal to the output energy E_O, such that $E_{\rm O} = E_{\rm Cr}$ and $\frac{1}{2}Cr\left(V^2_{\rm Cr,max} - V^2_{\rm Cr,min}\right) = \frac{V_O^2\,\pi}{R_L\,\omega}$.

Substituting $\omega = \frac{1}{\sqrt{L_r C_r}}$ into equation, and solving for V_O gives

$$V_O = \sqrt{\frac{R_L\left(V^2_{\rm Cr,max} - V^2_{\rm Cr,min}\right)}{2\pi Z_{\rm LC}}} \quad (7)$$

and the voltage conversion ratio of the converter is equal to

$$\frac{V_O}{\hat{V}_{\rm in}} = \sqrt{\frac{R_L\left(V^2_{\rm Cr,max} - V^2_{\rm Cr,min}\right)}{2\pi Z_{\rm LC}\hat{V}^2_{\rm in}}}. \quad (8)$$

.

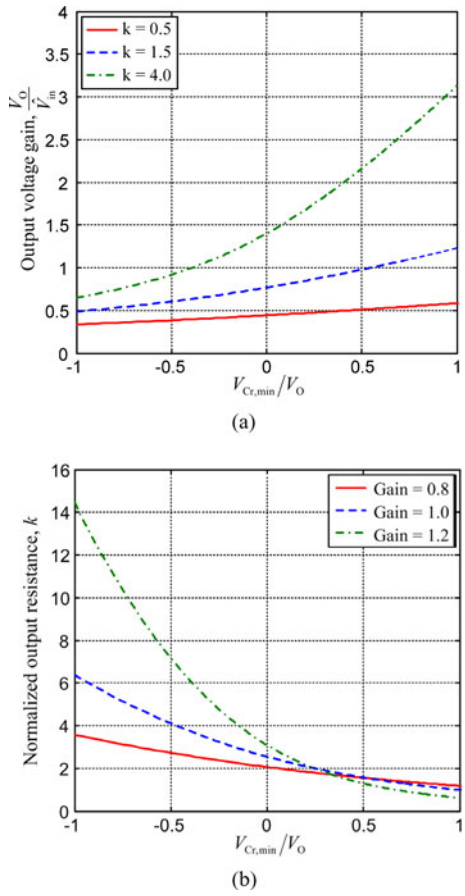


Fig. 7. Plots of (a) output voltage gain and (b) output load variation versus normalized threshold voltage $V_{\rm Cr,min}/V_{Cr}$, where $k = R_L/{\rm Z_{LC}}$.

The voltage conversion ratio against the normalized threshold voltage $V_{\rm Cr,min}/V_O$ is plotted in Fig. 7(a). It can be observed that the output voltage of the converter is dependent on the characteristic impedance Z_{LC} (input impedance) of the converter and the output load resistance R_L. With the proper selection of the characteristic impedance of the resonant tank, the converter is able

to perform the function of a buck and boost conversion. Fig. 7(b) shows the relationship of the output load variation against the normalized threshold voltage $V_{\mathrm{Cr,min}}/V_O$ of the converter. It can be observed that the output power can be controlled using $V_{\mathrm{Cr,min}}$ of which $V_{\mathrm{Cr,min}}$ is the initial voltage value of the resonant capacitor controlling the amount of input energy to the converter. As a result, the output voltage can be regulated.

B. Efficiency of the Converter

The estimation of the individual efficiency of the PFC and the regulation stage is presented in this section on the assumption that the converter operates ideally with unity PF. From first principle, the energy consumption of the converter is found by integrating the instantaneous input power and it can be expressed as

$$E_{\mathrm{in}} = \int_0^{T/2} [v_{\mathrm{in}}(t) \times i_{\mathrm{in}}(t)]\, dt. \tag{9}$$

.

Since $v_{\mathrm{in}}(t) = \hat{V}_{\mathrm{in}} \sin(\omega t)$ and $i_{\mathrm{in}}(t) = i_{\mathrm{Lr}}(t)$, (9) can be rewritten as

$$E_{\mathrm{in}} = \int_{t_\alpha}^{T/2} \left[\begin{array}{l} \hat{V}_{\mathrm{in}} \sin(\omega t) \left(\frac{\hat{V}_{\mathrm{in}} \sin(\alpha) - 2V_{\mathrm{Cr,min}}}{2Z_{\mathrm{LC}}} \right) \sin(\omega(t - t_\alpha)) \\ + \frac{\hat{V}_{\mathrm{in}}\omega}{2Z_{\mathrm{LC}}} t \sin(\omega(t - t_\alpha) + \alpha) \end{array} \right] dt. \tag{10}$$

Substituting (4) into (5), the energy stored in the resonant capacitors can be derived as

$$E_{\mathrm{Cr}} = \frac{1}{2} Cr \left[\left(\frac{\hat{V}_{\mathrm{in}}}{4} [\sin(2\alpha) + 2\omega(\pi - \alpha)] - V_{\mathrm{Cr,min}} \cos(\alpha) \right)^2 - V_{\mathrm{Cr,min}}^2 \right]. \tag{11}$$

Thus, the efficiency of the PFC stage and the regulation stage can be obtained from (12) and (13), respectively. The total efficiency of the converter can be expressed as

$$\eta_{\mathrm{PFC}} = \frac{E_{\mathrm{Cr}}}{E_{\mathrm{in}}} \times 100\% \tag{12}$$

$$\eta_{\mathrm{Reg}} = \frac{E_O}{E_{\mathrm{Cr}}} \times 100\% \tag{13}$$

$$\eta_{\mathrm{Total}} = \eta_{\mathrm{PFC}} \times \eta_{\mathrm{Reg}}. \tag{14}$$

IV. Experimental Results

A. Voltage Conversion Ratio

A proof-of-concept prototype of the proposed high-frequency-fed ac–dc power converter is constructed. The control scheme is implemented using discrete components and the circuit is shown in Fig. 8. The converter is designed to convert a 400-kHz ac voltage source into a dc source. The input voltage and the expected output power of the converter are 50 V_{rms} and 30 W, respectively. The output load resistance of the converter

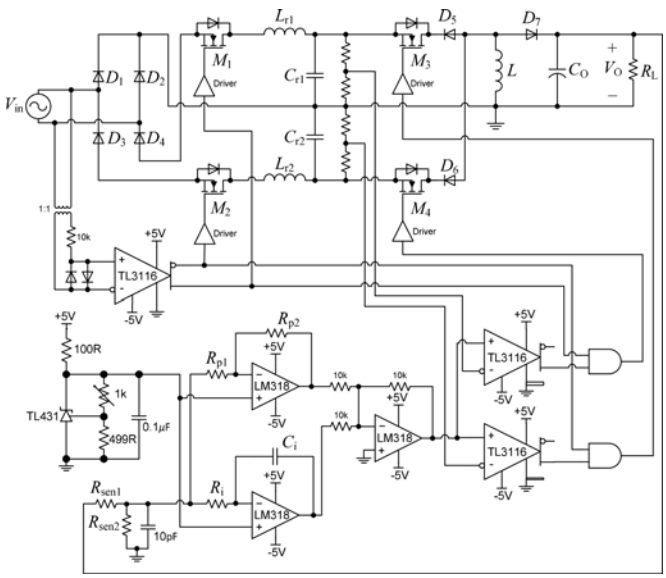


Fig. 8. Schematic of the proposed high-frequency-fed ac–dc power converter.

is 100 Ω. Given the input ac voltage and the threshold voltage $V_{\mathrm{Cr,min}}$, the potential difference across the resonant capacitor can be calculated following (4). Neglecting the power loss of the circuit elements, the input energy over half an ac cycle is equal to the output energy delivered to the load over the same half cycle. The size of the resonant capacitor can be determined using (5) and (6). As shown in (7), the size of the resonant inductor is calculated according to the requirement of the output voltage of the converter. The switching devices used in the prototype are CoolMOS transistors, which have a lower switching and conduction losses than traditional power MOSFET in the high-frequency range. Silicon-carbide Schottky (Sic) diodes are selected because of their very-low junction capacitance, resulting in a low reverse recovery current and power loss. The inductors and capacitors are commercial off-the-shelf products. The detailed specifications of the components are summarized in Table I. Note that the specifications and test conditions of the converter are arbitrary selected to examine the operation of the converter. The test of the converter is carried out at three different output power levels at 11, 18, and 30 W. The converter operating waveforms are captured to verify the theoretical circuit analysis. The associated input current harmonics and efficiency of the converter are measured.

B. Experimental Results and Discussion

Fig. 9 shows the captured waveforms of the input voltage, input current, and resonant capacitors' voltages of the converter at different output power levels. The output power of the converter is increased from 11 to 30 W when the threshold voltage is reduced from 25 to −50 V. The converter is connected to a constant resistive load. Therefore, the output voltage changed from 29 to 54 V accordingly. The experimental waveforms are in good agreement with the theoretical analysis given in Section II. In Fig. 9(a), it can be observed that the input current is

TABLE I
COMPONENTS SPECIFICATIONS OF THE CONVERTER

Components	Symbols	Specifications
Resonant inductors	L_{r1} and L_{r2}	Coiltronics, UP3B-330-R33 μH, 3Ω @400 kHz
Resonant capacitors	C_{r1} and C_{r2}	5 nF 500 V, ESR = 0.15Ω @400 kHz
Boost inductor	L	TDK-SLF12575T-221M1R3-PF,220 μH, 0.3Ω @DC, 15Ω @400 kHz
Output Capacitor	$C_{\rm O}$	220 nF 630 V, x 8
Transistors	M_1, M_2, M_3 and M_4	N-Ch CoolMos, IPD60R950C6, 650 V, 4.4 A, $R_{\rm DS(ON)} = 0.95\,\Omega$
Diodes	D_1, D_2, D_3, D_4, D_5, D_6 and D_7	SiC Diode, C3D04060A,600 V, 7 A, $V_F = 1.5$ V

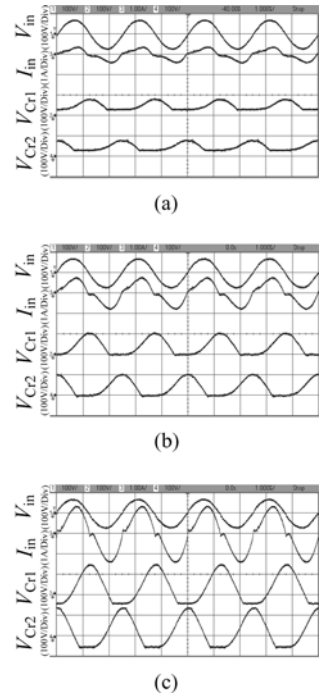


Fig. 9. Waveforms of the input voltage, input current, and voltage of the resonant capacitors at different output power levels; (a) $V_{\rm Cr,min} = 25$ V, $P_{\rm out} = 11$ W, (b) $V_{\rm Cr,min} = 0$ V, $P_{\rm out} = 18$ W, and (c) $V_{\rm Cr,min} = 50$ V, $P_{\rm out} = 30$ W.

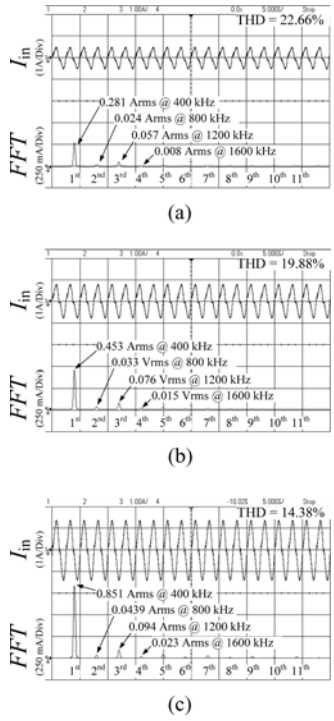


Fig. 10. Waveform of the input current and its FFT at different output power levels; (a) $V_{\rm Cr,min} = 25$ V, $P_{\rm out} = 11$ W, (b) $V_{\rm Cr,min} = 0$ V, $P_{\rm out} = 18$ W, and (c) $V_{\rm Cr,min} = 50$ V, $P_{\rm out} = 30$ W.

distorted when the output power of the converter is low. In the other words, the delay angle α is not zero. The diodes in the PFC stage become reverse biased when the input voltage is lower than the initial voltage of the resonant capacitors. Nevertheless, a zero or negative initial voltage on the resonant capacitors causes the diodes to conduct at the beginning of each half cycle. As a result, the quality of the input current improves substantially as shown in Fig. 9(b) and (c). Fig. 10 shows the captured input current waveforms and their harmonic spectra using fast Fourier transform (FFT).

The total harmonic distortion (THD) of the input current at 11, 18, and 30 W output power are found to be 22.66%, 19.88%, and 14.38%, respectively. Fig. 11 shows the captured output voltage waveform and its harmonic spectrum using FFT. Since all the switches are operated in a synchronized manner with the input ac source, the output voltage contains a double-line frequency ripple.

The ac input voltage and current are recorded by a digital oscilloscope. Thus, the ac input power of the converter can be

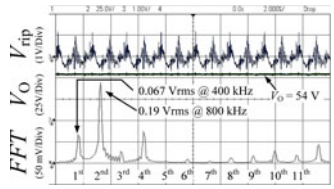


Fig. 11. Waveforms of the output voltage, output voltage ripple and its FFT at $V_{\rm Cr,min} = 50$ V, $P_{\rm out} = 30$ W.

obtained by integrating the product of the instantaneous input voltage and current. The dc output power is measured by a digital multimeter. Thus, the PF and overall efficiency of the converter are calculated. Major key performance indices of the converter at different output power levels are summarized in Table II. It can be observed that the PF of the converter at all the output power levels can be maintained above 0.9. The efficiency of the PFC and regulation stages are estimated using (9) to (14)

TABLE II
PERFORMANCE OF THE CONVERTER AT DIFFERENT OUTPUT POWER LEVELS

Parameters	Symbols	Conditions I	II	III
Output power	P_O	11.63 W	17.99 W	30.39 W
Output voltage	V_O	34.11 V	42.41 V	55.31 V
Output voltage ripple	$V_{\rm rip}$	0.56 V	0.71 V	0.74 V
Input power	Pin	14.70 W	23.36 W	42.76 W
Input power factor	PF	0.95	0.94	0.93
Input current	$i_{\rm in}$	0.308 A	0.496 A	0.918 A
Input current (THD)	THD-$i_{\rm in}$	22.66%	19.88%	14.38%
Threshold voltage	$V_{\rm Cr,min}$	25 V	0 V	−50 V
Efficiency				
PFC stage	$\eta_{\rm PFC}$	92.68%	91.05%	86.64%
Regulation stage	$\eta_{\rm Reg}$	85.37%	84.56%	82.03%
Overall	η	79.13%	76.99%	71.08%

as shown in Table II. They are all within reasonable range from 80% to 90%. The drop of efficiency in the PFC stage is resulted from the high conduction loss of diodes and ac resistance of resonant inductors. The efficiency of the converter can be further improved by proper selection of components according to the desired applications. The detailed studies on the converter design procedure, the passive and active components' selection together with the optimization of the voltage conversion ratio and efficiency for practical high-frequency ac–dc applications are left for further work.

V. CONCLUSION

A 400-kHz high-frequency-fed ac–dc PFC converter with one switching action per cycle is demonstrated. With a single converter topology, the converter is able to perform the function of a buck and boost conversion depending on the characteristic impedance of the resonant tank. The voltage conversion ratio of the converter can be further controlled by the initial voltage of the resonant capacitors. Experimental results prove that the converter is able to achieve a high PF (PF $>$ 0.9) and a low input current distortion (THD $<$ 20%). A control scheme is also proposed for the converter. It can be realized by simple operational amplifiers and digital logic gates, and thereby can be easily fabricated as an IC for mass production. The distinctive features of this converter are favorable for future high-frequency ac power transfer system operating in the range from a few hundred kHz to the MHz range.

APPENDIX

Fig. 12 shows a half wave rectifier with an inductive–capacitive load. The Laplace equations of the circuit can be expressed as

$$V_{\rm in}(s) = V_{\rm Lr}(s) + V_{\rm Cr}(s) \tag{A1}$$

$$V_{\rm Lr}(s) = sL_{\rm r}I_{\rm Lr}(s) - L_{\rm r}I_{\rm Lr}(0) \tag{A2}$$

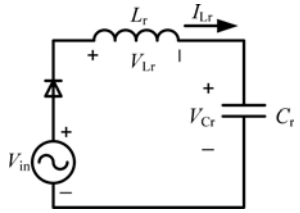


Fig. 12. Half wave rectifier with inductive–capacitive load.

$$V_{\rm Cr}(s) = \frac{I_{\rm Lr}(s)}{sC_{\rm r}} + \frac{V_{\rm Cr,min}}{s}. \tag{A3}$$

Combining (A1) to (A3), (A1) can be rewritten as

$$V_{\rm in}(s) = sL_{\rm r}I_{\rm Lr}(s) - L_{\rm r}I_{\rm Lr}(0) + \frac{I_{\rm Lr}(s)}{sC_{\rm r}} + \frac{V_{\rm Cr,min}}{s}. \tag{A4}$$

The substitution of $V_{\rm in}(t) = \hat{V}_{\rm in}\sin(\omega t + \alpha)$ into (A4), and the application of Laplace transform gives

$$\hat{V}_{\rm in}\left[\frac{s\sin(\alpha) + \omega\cos(\alpha)}{s^2+\omega^2}\right] = \left[\frac{s^2+\omega^2}{s}\right]L_{\rm r}I_{\rm Lr}(s) + \frac{V_{\rm Cr,min}}{s}. \tag{A5}$$

The substitution of $L_{\rm r} = {\rm Z_{LC}}/\omega$ into (A5), where ${\rm Z_{LC}} = \sqrt{L_{\rm r}/C_r}$ and $\omega = \omega_S = 1/(L_rC_r)$, gives the solution of inductor current $I_{\rm Lr}(s)$ as

$$I_{\rm Lr}(s) = \frac{s^2\hat{V}_{\rm in}\omega\sin(\alpha)}{{\rm Z_{LC}}(s^2+\omega^2)^2} + \frac{s\hat{V}_{\rm in}\omega^2\cos(\alpha)}{{\rm Z_{LC}}(s^2+\omega^2)^2} - \left[\frac{\omega}{(s^2+\omega^2)}\right] \times \frac{V_{\rm Cr,min}}{{\rm Z_{LC}}}. \tag{A6}$$

On the other hand, the Laplace transform equation of the capacitor voltage is

$$V_{\rm Cr}(s) = \frac{I_{\rm Lr}(s)}{sC_{\rm r}} + \frac{V_{\rm Cr,min}}{s}. \tag{A7}$$

Substituting (A6) into (A7), it can be rewritten as

$$V_{\rm Cr}(s) = \left[\frac{s^2\omega\sin(\alpha) + s\omega^2\cos(\alpha)}{sC_{\rm r}{\rm Z_{LC}}(s^2+\omega^2)^2}\right]\hat{V}_{\rm in} - \left[\frac{\omega}{sC_{\rm r}{\rm Z_{LC}}(s^2+\omega^2)}\right]V_{\rm Cr,min} + \frac{V_{\rm Cr,min}}{s}. \tag{A8}$$

Substitution for $C_r = 1/(\omega{\rm Z_{LC}})$, the solution of the capacitor voltage can be found by

$$V_{\rm Cr}(s) = \left[\frac{s\omega^2\sin(\alpha) + s\omega^3\cos(\alpha)}{(s^2+\omega^2)^2}\right]\hat{V}_{\rm in} + \left[\frac{s}{s^2+\omega^2}\right] \times V_{\rm Cr,min}. \tag{A9}$$

We can get the time domain equations of the inductor current and capacitor voltage by taking inversed Laplace transform of

(A6) and (A9), respectively. The solutions are expressed as

$$i_{\mathrm{Lr}}(t) = \left(\frac{\hat{V}_{\mathrm{in}}\sin(\alpha) - 2V_{\mathrm{Cr,min}}}{2\mathrm{Z_{LC}}}\right)\sin(\omega t - \alpha) + \frac{\hat{V}_{\mathrm{in}}\omega}{2\mathrm{Z_{LC}}}t\sin(\omega t) \tag{A10}$$

and

$$v_{\mathrm{Cr}}(t) = \frac{\hat{V}_{\mathrm{in}}}{2}\cos(\alpha)\sin(\omega t - \alpha) - \frac{\hat{V}_{\mathrm{in}}}{2}(\omega t - \alpha)\cos(\omega t) + V_{\mathrm{Cr,min}}\cos(\omega t - \alpha) \tag{A11}$$

REFERENCES

[1] N. Tesla, "Apparatus for transmitting electrical energy," U.S. Patent 1 119 732, Dec. 1, 1914.

[2] J. Schuder, H. Stephenson, and J. Townsend, "High-level electromagnetic energy transfer through a closed chest wall," *Inst. Radio Engrs. Int. Conv. Rec.*, vol. 9, pp. 119–126, 1961.

[3] J. C. Schuder, J. H. Gold, and H. E. Stephenson, "An inductively coupled RF system for the transmission of 1 kW of power through the skin," *IEEE Trans. Biomed. Eng.*, vol. BME-18, no. 4, pp. 265–273, Jul. 1971.

[4] W. Ko, S. Liang, and C. F. Fung, "Design of radio-frequency powered coils for implant instruments," *Med. Biol. Eng. Comput.*, vol. 15, pp. 634–640, 1977.

[5] M. Kiani and M. Ghovanloo, "The circuit theory behind coupled-mode magnetic resonance-based wireless power transmission," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1–10, Sep. 2012.

[6] S. Cheon, Y. H. Kim, S. Y. Kang, M. L. Lee, J. M. Lee, and T. Zyung, "Circuit-model-based analysis of a wireless energy-transfer system via coupled magnetic resonances," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2906–2914, Jul. 2011.

[7] Y. H. Kim, S. Y. Kang, S. Cheon, M. L. Lee, J. M Lee, and T. Zyung, "Optimization of wireless power transmission through resonant coupling," in *Proc. Compat. Power Electron.*, 2009, pp. 426–431.

[8] N. Y. Kim, K. Y. Kim, J. Choi, and C. W. Kim, "Adaptive frequency with power-level tracking system for efficient magentic resonance wireless power transfer," *Electron. Lett.*, vol. 48, no. 8, pp. 452–454, Apr. 2012.

[9] S. Y. R. Hui, D. Lin, C. K. Lee, and J. Yin, " Methods for parameters identification, load monitoring and output power control for wireless power transfer," U.S. Patent Application, US 61/862,627, Aug. 6, 2013.

[10] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed., New York, NY, USA: Wiley, 2000, pp. 483–494.

[11] C. K. Tse, "Circuit theory and design of power factor correction power supplies," IEEE Distinguished Lecture 2005, Circuit and Systems. [Online]. Available: http://cktse.eie.polyu.edu.hk/Tse-IEEElecture2.pdf

[12] K. Gauen, "The effect of MOSFET output capacitance in high frequency applications," in *Proc. Ind. Appl. Soc. Annu. Meet.*, 1989, vol. 2, pp. 1227–1234.

[13] M. Hartmann, H. Ertl, and J. W. Kolar, "On the tradeoff between input current quality and efficiency of high switching frequency PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3137–3140, Jul. 2012.

[14] Z. Chen, D. Boroyevich, and J. Li, "Behavioral comparison of Si and SiC power MOSFETs for high-frequency applications," in *Proc. Appl. Power Electron. Conf. Expo.*, 2013, pp. 2453–2460.

[15] Q. Li, M. Lim, J. Sun, A. Ball, Y. Ying, F. C. Lee, and K. D. T. Ngo, "Technology roadmap for high frequency integrated dc–dc converter," in *Proc. Power Electron. Motion Control Conf.*, 2009, pp. 1–8.

[16] W. Liang, J. Glaser, and J. Rivas,"13.56 MHz high density DC–DC converter with PCB inductors," in *Proc. Appl. Power Electron. Conf. Expo.*, 2013, pp. 633–640.

[17] J. M. Burkhart, R. Korsunsky, and D. J. Perreault, "Design methodology for a very high frequency resonant boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1929–1937, Apr. 2013.

[18] S. Ji, D. Reusch, and F. C. Lee, "High-frequency high power density 3-D integrated gallium-nitride-based point of load module design," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4216–4226, Sep. 2013.

[19] F. C. Lee and J. D. van Wyk, " IPEM-based power electronics system," in *Proc. Integr. Power Syst.*, 2006, pp. 1–14.

[20] W. Zhang, F. C. Lee, and D. Y. Chen, "Integrated EMI/Thermal design for switching power supplies," in *Proc. IEEE 31st Annu. Power Electron. Spec. Conf.*, Jun. 18–23, 2000, vol. 1, pp. 47–52.

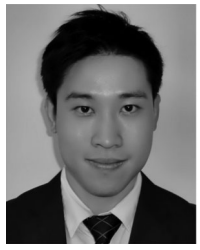
[21] C. K. Lee and K. Sitthisak, "Electronic apparatus and control method for high frequency AC to DC conversion," U.S. Patent Application, US 14/160,830, Jan. 22, 2014.

Chi-Kwan Lee (M'08–SM'14) received the B.Eng. and Ph.D. degrees in electronic engineering from the City University of Hong Kong, Kowloon, in 1999 and 2004, respectively.

He was a Postdoctoral Research Fellow in the Power and Energy Research Centre, National University of Ireland, Galway, from 2004 to 2005. In 2006, he joined the Centre of Power Electronics in City University of Hong Kong as a Research Fellow. From 2008 to 2011, he was a Lecturer of electrical engineering at the Hong Kong Polytechnic University. He was a Visiting Academic at Imperial College London from 2010 to 2013. Since January 2012, he has been an Assistant Professor at the Department of Electrical and Electronic Engineering, The University of Hong Kong. His current research interests include applications of power electronics to power systems, advanced inverters for renewable energy and smart grid applications, reactive power control for load management in renewable energy systems, wireless power transfer, energy harvesting, and planar electromagnetics for high-frequency power converters.

Sitthisak Kiratipongvoot received the B.Eng. and M.Eng. degrees in electrical engineering from King Mongkut's University of Technology North Bangkok, Thailand, in 2001 and 2008, respectively.

From October 2008 to July 2012, he worked as a Research Assistant in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University. Since August 2012, he is a Research Assistant in the Department of Electrical and Electronic Engineering, The University of Hong Kong. His research interests include dc–dc converters, power factor correction ac–dc converters, resonant inverters, soft-switching techniques, renewable energy systems, electric vehicle, and wireless energy transfer.



Siew-Chong Tan (S'00–M'06–SM'11) received the B.Eng. (Hons.) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, in 2000 and 2002, respectively, and the Ph.D. degree in electronic and information engineering from the Hong Kong Polytechnic University, in 2005.

From October 2005 to May 2012, he worked as a Research Associate, Postdoctoral Fellow, Lecturer, and Assistant Professor in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University. From January to October 2011, he was a Senior Scientist in Agency for Science, Technology and Research (A*Star), Singapore. He is currently an Associate Professor in the Department of Electrical and Electronic Engineering, The University of Hong Kong. He was a Visiting Scholar at Grainger Center for Electric Machinery and Electromechanics, University of Illinois at Urbana-Champaign, from September to October 2009, and an Invited Academic Visitor of Huazhong University of Science and Technology, Wuhan, China, in December 2011. His research interests include the areas of power electronics and control, LED lightings, smart grids, and clean energy technologies. He serves extensively as a reviewer for various IEEE/IET transactions and journals on power, electronics, circuits, and control engineering. He is a coauthor of the book *Sliding Mode Control of Switching Power Converters: Techniques and Implementation* (Boca Raton: CRC, 2011).