Improved-Power-Quality Bridgeless-Converter-Based Multiple-Output SMPS

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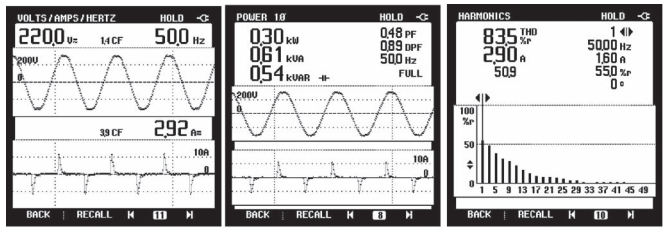
***Abstract*—This paper deals with the design, analysis, simulation, and development of a power-factor-correction (PFC) multiple-output switched-mode power supply (SMPS) using a bridgeless buck–boost converter at the front end. Single-phase ac supply is fed to a pair of back-to-back-connected buck–boost converters to eliminate the diode bridge rectifier, which results in reduction of conduction losses and power quality improvement at the front end. The operation of the bridgeless buck–boost converter in discontinuous conduction mode ensures inherent PFC operation and reduces complexity in control. The performance of the proposed multiple-output SMPS is evaluated under varying input voltages and loads by simulating this circuit in MATLAB/Simulink environment, and the results obtained through simulation are validated experimentally on a developed prototype. Both simulation and experimental results demonstrate the improved performance of the proposed SMPS.**

***Index Terms*—Bridgeless buck–boost converter, discontinuous conduction mode (DCM), improved power quality, multiple-output switched-mode power supply (SMPS), power factor (PF) correction (PFC).**

I. Introduction

SWITCHED-MODE power supplies (SMPSs) are used for powering up different parts in a personal computer (PC) by developing multiple dc voltages from a single-phase ac voltage from the power grid. Normally, a diode bridge rectifier (DBR) followed by a filter capacitor is used at the front end of these SMPSs. DBR causes significant deterioration in the power quality [1], [2], leading to very low power factor (PF) and high harmonic distortion at the ac mains with a high crest factor of the input current [3]. Fig. 1 shows the input voltage and input current of a typical SMPS that is currently employed in most of the PCs. The current waveform is very peaky, nonsinusoidal, and highly distorted; the PF is around 0.48. At full load, the total harmonic distortion (THD) of input ac mains current is 83.5%. The performance of the power supply is violating the limits set by various international standards such as the International Electrotechnical Commission (IEC) 61000-3-2 [4]. Due to these issues, improved-power-quality SMPSs are extensively being researched, which are expected to draw a sinusoidal input current at a high PF. Improvement in power quality also results in better reliability and enhanced efficiency. To achieve a perceivable improvement in power quality, PF-correction (PFC) circuits are employed in these SMPSs at the utility interface point [5]–[7]. PFC circuits are able to achieve high PF and low THD in the input current even at fluctuating input voltages and varying loads. Apart from this, they are also capable of yielding stiffly regulated output dc voltages.



(a) (b) (c)

Fig. 1. (a) Conventional SMPS input voltage and input current, (b) input power and PF, and (c) input current harmonic spectrum.

The use of nonisolated PFC converters at the front end of these power supplies is a commonly accepted solution to achieve a good power quality at varying input voltages and loads [8]. Discontinuous conduction mode (DCM) operation of these converters results in inherent PFC and reduction in sensor requirements. Furthermore, DCM can also be implemented with simple control strategy. Recent advancements in the field of power electronics have enabled the elimination of DBR at the front end of the power supplies, thereby improving the power quality at the ac mains. Various bridgeless single-ended primary-inductance converter and Cuk converters are proposed in the literature, which result in low voltage stress, improved thermal management, and low conduction losses [9]–[11]. However, the component count is increased in these converters, which is not suitable for low-power SMPS applications, although the output voltage range is fairly large. A bridgeless buck PFC converter is proposed in [12], which acts as a voltage doubler. A bridgeless boost converter is reported in [13], which eliminates one diode drop in the current path. However, in both converter topologies, the output voltage range is limited. A buck–boost converter configuration is best suited for computer SMPSs among various bridgeless converter topologies

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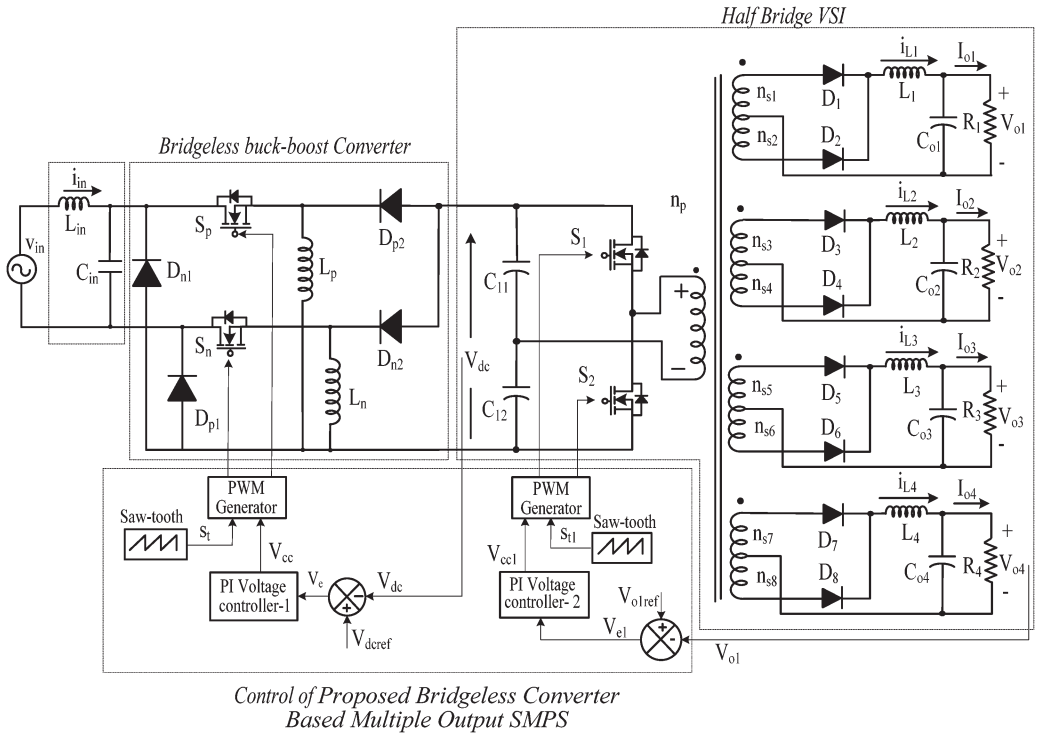


Fig. 2. Proposed bridgeless-converter-based multiple-output SMPS.

particularly because it can handle a larger voltage range and yet deliver stiffly regulated output voltages. Such a bridgeless buck–boost converter is proposed in [14] for universal input PFC applications, which offers low switch stress, reduced magnetic size, and low inductor conduction losses. However, one of the switching devices is always on in the conduction path. Wei *et al.* [15] have proposed a bridgeless buck–boost converter that uses three switches in the conduction path, which increases the conduction losses. Normally, a half-bridge voltage source inverter (VSI) is used at the output for high-frequency isolation and multiple dc output voltages in computer power supplies because it provides better core utilization than any other unipolar converter and it is cost effective compared to push–pull and full-bridge converters [16]–[19].

It is observed from the available literature that the bridgeless-converter-based multiple-output SMPS has not been attempted so far, particularly targeting SMPSs for PCs. Therefore, an attempt is made here to reduce the current harmonics and to achieve high PF at the utility interface in a multiple-output SMPS by using a bridgeless buck–boost converter at the front end. The diode bridge at the front end is eliminated, and two buck–boost converters are connected back-to-back so that each takes care of one half cycle of the ac supply. The bridgeless buck–boost converter is designed in DCM for single control loop and for inherent PFC. This regulated dc voltage is given to half-bridge VSI for obtaining multiple-output dc voltages. The half-bridge VSI is designed in continuous conduction mode to reduce the component stress. Moreover, only one control loop is required to regulate multiple dc voltages. The proposed system is designed, analyzed, and simulated in MATLAB/Simulink software [20], and the performance is studied during varying input voltages and loads to demonstrate the improved performance in terms of low THD and high PF. The hardware of the proposed SMPS system is developed as an experimental prototype, and the simulated results are validated with the help of test results on the prototype to confirm the improved power quality at the ac mains.

II. Configuration of Bridgeless-Converter-Based Multiple-Output SMPS

The system configuration of the proposed multiple-output SMPS is shown in Fig. 2. Single-phase ac supply is fed to two buck–boost converters through an inductor–capacitor ($L_{\rm in}$–$C_{\rm in}$) filter to eliminate the high-frequency ripples. The upper buck–boost converter that conducts during the positive half cycle of the ac supply consists of one high-frequency switch S_p, inductor L_p, and two diodes D_{p1} and D_{p2}. Similarly, the lower buck–boost converter that operates during the negative half cycle consists of one high-frequency switch S_n, inductor L_n, and two diodes D_{n1} and D_{n2}. Both inductors L_p and L_n of buck–boost converters are designed in DCM to obtain inherent PFC at the input ac mains. The input capacitor of the half-bridge VSI acts as the filter at the output of the buck–boost converter. The voltage and current stresses on the switches of the buck–boost converters are evaluated to estimate the switch rating and heat sink design. The output dc voltage of the buck–boost converter is regulated by using closed-loop control. The regulated dc output voltage of the buck–boost converter is fed to the half-bridge VSI for obtaining multiple dc voltages. The half-bridge VSI consists of two input capacitors C_{11} and C_{12}, two high-frequency switches S_1 and S_2, and one multiple-output high-frequency transformer (HFT). The HFT is having one primary winding and four secondary windings which are connected in center-tapped configuration to reduce the losses. At the secondary side of the HFT, filter inductors L_1, L_2, L_3,

and L_4 and capacitors C_{o1}, C_{o2}, C_{o3}, and C_{o4} are connected to each winding to reduce the current and voltage ripples, respectively. The output voltages are regulated by using closed-loop control of one of the output voltages. The highest rated dc voltage is sensed for this purpose. The other three outputs are controlled through duty ratio control of the half-bridge VSI because a common core is used for all other secondary windings of the HFT with proper winding arrangements. The effect of varying input voltages and loads is studied to reveal the improved performance of the proposed bridgeless-converter-based multiple-output SMPS. The hardware of the SMPS is implemented in a laboratory prototype to verify the simulated results.

III. Operating Principle of Bridgeless-Converter-Based Multiple-Output SMPS

The proposed bridgeless-converter-based multiple-output SMPS consists of a single-phase ac supply feeding two back-to-back-connected buck–boost converters with a half-bridge VSI and multiple-output HFT at the load end. The buck–boost converters are controlled suitably to obtain a high PF and low input current THD. The half-bridge VSI at the output takes care of high-frequency isolation with multiple dc output voltages being regulated. The operation of both converters in one switching cycle is described in the following subsections.

A. Operation of Buck–Boost Converter

The switches in the upper and lower buck–boost converters are switched on and off alternately in the positive and negative half cycles of the ac voltage, respectively. The operation of the upper buck–boost converter in DCM during the positive half cycle of the ac input voltage is shown in Fig. 3. The lower one operates in the same way but during the negative half cycle. Three states are observed in DCM operation in each switching cycle. In the first state, when the upper switch S_p is on, inductor L_p starts storing energy from the input, and the inductor current increases to the maximum value, as shown in Fig. 3(a). Diode D_{p1} completes the current flow path in the input side. In the second state, S_p is turned off, and the energy in inductor L_p is transferred to the output, thus reducing its current from maximum value to zero, as shown in Fig. 3(b). In the last state of one switching cycle, neither the switch and nor the diode conducts, and the inductor current remains zero, ensuring DCM operation [Fig. 3(c)]. Fig. 3(d) shows the waveforms for one complete pulse width modulation (PWM) switching cycle. In the next switching cycle, the same sequence of operation repeats itself. Similarly for negative half cycle of the input voltage, the lower buck–boost converter operates, and the same sequence of operation continues.

B. Operation of Half-Bridge VSI

The controlled output dc voltage of the dual buck–boost converter is fed to the half-bridge VSI for high-frequency isolation, for voltage scaling, and for obtaining multiple dc output voltages. The operation of the half-bridge VSI in one switching cycle is described in four states. The second and

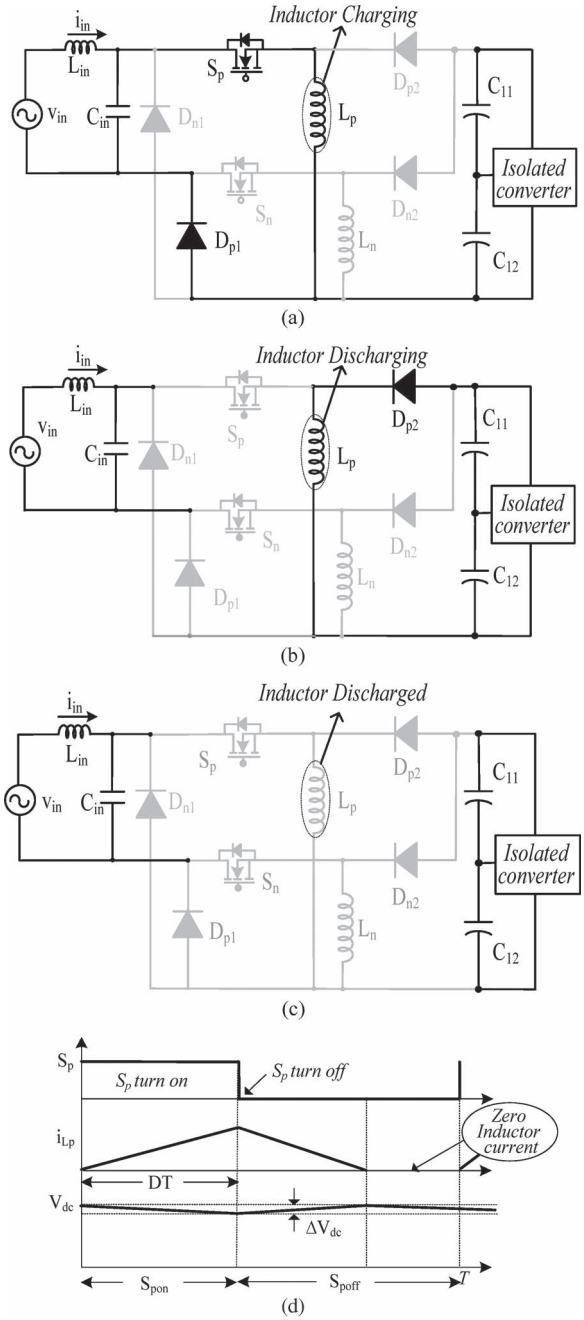


Fig. 3. Operating modes for under (a) upper switch S_p is on, (b) upper switch S_p is off, (c) both switch and diode are off, and (d) waveforms in one switching cycle.

fourth states are similar and occur twice in each switching cycle, as shown in Fig. 4(b). In the first state, the upper switch S_1 is turned on; the input current circulates through the primary winding of the HFT to the lower input capacitor C_{12}. Diodes D_1, D_3, D_5, and D_7 start conducting, and the inductors associated with the windings start storing energy, as shown in Fig. 4(a). Therefore, inductor currents i_{L1}, i_{L2}, i_{L3}, and i_{L4} increase, and output filter capacitors C_{o1}, C_{o2}, C_{o3}, and C_{o4} discharge through the loads. In the second state [Fig. 4(b)], both switches are turned off, and all secondary diodes D_1–D_8 freewheel the stored energy until the voltage across the HFT becomes zero. Therefore, inductor currents i_{L1}, i_{L2}, i_{L3}, and i_{L4} start decreasing. In the third state of the switching cycle,

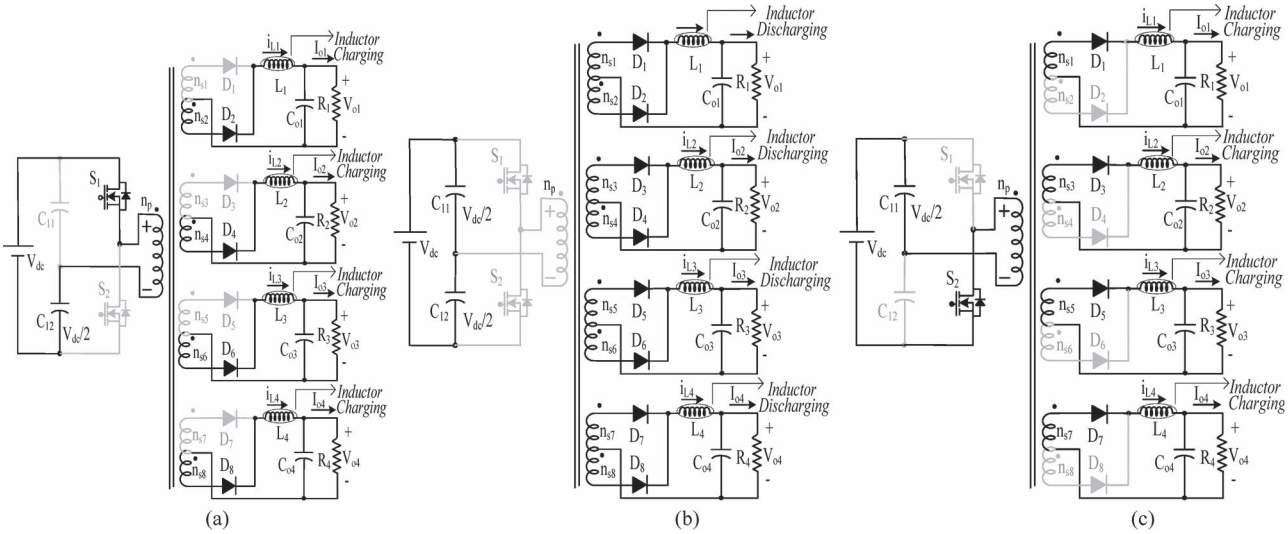


Fig. 4. (a) When the first switch S_1 is on, (b) when both switches are off, (c) and when the second switch S_2 is on.

the second switch S_2 is turned on, and the input current flows through upper capacitor C_{11} and the primary winding, as shown in Fig. 4(c). Associated diodes D_2, D_4, D_6, and D_8 in the secondary windings conduct, and inductors L_1, L_2, L_3, and L_4 start storing energy. When the energy stored in the inductors reaches maximum values, the switch is turned off. In the last state, all secondary diodes start conducting, which is similar to the second state. The same operating states repeat in each switching cycle.

IV. Design of the Proposed Bridgeless-Converter-Based Multiple-Output SMPS

To simulate the proposed bridgeless-converter-based multiple-output SMPS, it is essential to estimate the component values. To derive the necessary design equations, the switches and diodes are considered to be ideal, and the switching frequency is considered very high compared to the line frequency (50 Hz). This enables considering the average quantity in one switching cycle for analysis purposes. The specifications of the proposed bridgeless-converter-based multiple-output SMPS are given in the Appendix.

A. Design of Buck–Boost Converter

The design of the inductors in the buck–boost converters is very important to ensure DCM operation. The values of upper and lower inductors are the same, and they are chosen based on the change in input current in one switching cycle during on condition of the switch. The inductor value for a specified current ripple is expressed as [2]

$$L_p = \frac{DTV_{\text{avg}}}{\Delta i_{Lp\text{on}}} \tag{1}$$

where D is the duty cycle, i.e., t_{ON}/T, where t_{ON} is the "on" time of the switch and T is the total period in one switching cycle, and V_{avg} is the average of single-phase ac input voltage across the input of the buck–boost converter.

In DCM condition, the inductor current ripple is considered maximum, and it must be equal to twice the input current

$$\Delta i_{L\text{on}} = 2 * I_{\text{in}}. \tag{2}$$

Substituting (2) in (1) yields the value of $L_{p\min}$ as

$$L_{p\min} = \frac{DTV_{\text{avg}}}{2i_{\text{in}}} = \frac{0.2 * 50\ \mu\text{S} * 198\ \text{V}}{2 * 1.63\ \text{A}} = 607\ \mu\text{H}. \tag{3}$$

For a deep DCM condition, the inductor value should be less than one-tenth of the minimum inductor value [21]. Thus, it is selected as

$$L_p < \frac{L_{p\min}}{10}. \tag{4}$$

The inductor value is calculated as 60 μH for a D value of 0.2, with switching time T being 50 μS and V_{avg} being 198 V. A 60-μH inductance value is selected here for ensuring DCM under all operating conditions.

B. Input Filter Design

To filter the higher order harmonics in the proposed SMPS, it is essential to use an $L-C$ filter. This filter also reduces the harmonic distortion at the ac supply. The maximum capacitance value is expressed as [22]

$$C_{\text{inmax}} = \frac{I_m \tan\theta}{\omega V_m} = \frac{2.30\ \text{A} * .0174}{314 * 311\ \text{V}} = 409\ \text{nF} \tag{5}$$

where I_m and V_m are the peak input ac current and ac voltage, respectively. The maximum capacitance is estimated as 409 nF for a θ value of 1° (for ensuring high PF). The capacitance value C_{in} for the prototype is selected to be 330 nF.

The filter inductor for obtaining low harmonic distortion at input ac mains is calculated as

$$L_{\text{in}} = \frac{1}{4 * \pi^2 * f_c^2 * C_{\text{in}}} = \frac{1}{4 * (3.14)^2 * (5000\ \text{kHz})^2 * 330\ \text{nF}} = 3.07\ \text{mH} \tag{6}$$

where f_c is the cutoff frequency. The filter inductor $L_{\rm in}$ is calculated as 3.07 mH. A 2.5-mH filter inductor is selected for the hardware development.

C. Design of Half-Bridge VSI

The input capacitors of the half-bridge VSI act as a low-pass filter to eliminate the harmonics, which is reflected due to the single-phase ac mains.

1) Design of Input Capacitor: The input capacitor is designed to eliminate the harmonics introduced due to the single-phase ac mains. Thus, it is governed by the amount of the 100-Hz (lowest harmonic) current flowing in the capacitor. For maintaining PFC operation, the input current and voltage should be in phase. Therefore, the input power $P_{\rm in}$ [2] is

$$P_{\rm in} = \sqrt{2}V_{\rm in}{\rm Sin}\omega t * \sqrt{2}I_{\rm in}{\rm Sin}\omega {\rm t} = V_{\rm in}I_{\rm in}(1 - {\rm Cos}2\omega t) \quad (7)$$

where the latter term corresponds to the 100-Hz ripple which is reflected on the input capacitors of the half-bridge VSI. It is expressed as

$$i_C(t) = -\frac{V_{\rm in}I_{\rm in}}{V_{\rm dc}}{\rm Cos}2\omega t \quad (8)$$

where $i_c(t)$ is the total current flowing in the capacitors C_{11} and C_{12}.

The output voltage ripple corresponding to these capacitors' current is given by [2]

$$\Delta V_{\rm dc} = \frac{1}{C}\int i_C(t){\rm d}t = -\frac{I_{\rm dc}}{2\omega C}{\rm Sin}2\omega t. \quad (9)$$

${\rm Sin}(\omega t)$ is taken as one for the maximum value of voltage ripple at the capacitor. Hence, (9) is rewritten as

$$C = \frac{I_{\rm dc}}{2\omega\Delta V_{\rm dc}}. \quad (10)$$

Therefore, the capacitors C_{11} and C_{12} are estimated as

$$\frac{C_{11}}{2} = \frac{C_{12}}{2} = \frac{I_{\rm dc}}{2\omega\Delta V_{\rm dc}} = \frac{1.2\ {\rm A}}{2 * 314 * 6\ {\rm V}} = 0.63\ {\rm mF}. \quad (11)$$

Two equal valued input capacitors C_{11} and C_{12} are calculated as 0.63 mF for an ω of 314 rad/s, with ΔV_o being 6 V (2% of V_o) and output current of the buck–boost converter being 1.2 A.

The permissible current ripple is assumed to be 2%.

2) Design of Turns Ratio: In steady-state condition, the change in output inductor current i_{L1} during switch on and off conditions is equal to zero, and it is expressed as

$$\frac{T_h(0.5nV_{\rm dc} - V_{o1})D_h}{L_1} + \frac{T_hV_{o1}(0.5 - D_h)}{L_1} = 0 \quad (12)$$

where V_{o1} is the sensed dc output voltage, D_h is the duty cycle of half-bridge VSI, and T_h is one switching time.

Solving (8) for calculating turns ratio

$$n = \frac{V_{o1}}{D_dV_{\rm dc}} = \frac{12\ {\rm V}}{0.4 * 300\ {\rm V}} = 0.1. \quad (13)$$

The turns ratio from (13) is calculated as 0.1 for an output dc voltage of +12 V and for a duty cycle D_h of 0.4.

TABLE I
PARAMETERS OF BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

Component	Calculated	Selected	Experiment
Input inductors L_p and L_n	60 µH	60 µH	60 µH
Filter capacitor C_{in}	390 nF	330nF	330nF
Filter inductor L_{in}	3.07mH	2.5mH	2.5mH
Capacitor C_{11} and C_{12}	630µF	660µF	660µF

These component values are used in the modeling of the proposed multiple-output computer SMPS. These values and the ones used in the experimental prototype are tabulated in Table I.

V. CONTROL OF PROPOSED BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The control of the SMPS is carried out using two independent controllers. The front-end bridgeless buck–boost converter utilizes the voltage follower approach, while the half-bridge VSI utilizes the average current control.

A. Control of Front-End Converter

The control of the PFC bridgeless converter generates the PWM pulses for both switches (S_p and S_n) according to the polarity of input ac mains voltage. In this technique, voltage error V_e, i.e., the difference between the reference voltage $V_{\rm dcref}$ and the sensed dc output voltage V_{o1}, is fed to a proportional–integral (PI) voltage controller, as shown in Fig. 2. The voltage error signal (V_e) is expressed as

$$V_e(n) = V_{\rm dcref}(n) - V_{\rm dc}(n) \quad (14)$$

where n represents the nth sampling instant.

This error voltage signal (V_e) is fed to the voltage PI controller 1 to generate a controlled output voltage $(V_{\rm cc})$. It is expressed as

$$V_{\rm cc}(n) = V_{\rm cc}(n-1) + k_p\{V_e(n) - V_e(n-1)\} + k_iV_e(n) \quad (15)$$

where k_p and k_i are the proportional and integral gains of the voltage PI controller 1.

Finally, the output of the voltage controller 1 is compared with a high-frequency sawtooth signal (S_t) to generate the PWM pulses

$$\begin{aligned} &\text{For } v_{\rm in} > 0; \quad \left\{\begin{array}{ll} \text{if } s_t < V_{\rm cc}, & \text{then } S_p = \text{on} \\ \text{if } s_t \geq V_{\rm cc}, & \text{then } S_p = \text{off} \end{array}\right\} \\ &\text{For } v_{\rm in} < 0; \quad \left\{\begin{array}{ll} \text{if } s_t < V_{\rm cc}, & \text{then } S_n = \text{on} \\ \text{if } s_t \geq V_{\rm cc}, & \text{then } S_n = \text{off} \end{array}\right\} \end{aligned} \quad (16)$$

where S_p and S_n represent the switching signals of PFC bridgeless buck–boost converter.

B. Control of Half-Bridge VSI

For controlling the output voltage of the half-bridge VSI, an average current control scheme is used. The highest rated

winding output voltage V_{o1} is sensed and compared with a constant reference value $V_{o1\mathrm{ref}}$. The voltage error signal (V_{e1}) is fed to PI controller 2, and its output is compared with the sawtooth signal to generate PWM switching signals to maintain the output voltage constant. Thus, the control is able to take care of the impact of any individual output on the overall variation in the duty ratio and also the contribution of the present load condition of any of the outputs to the variations in V_{o1}, V_{o2}, V_{o3}, and V_{o4}. If the load on any of the other windings is varied, the duty cycle undergoes a change according to the impact felt on the highest rated output, and hence, voltage regulation is taken care of. However, the response of the other windings is slightly slower as compared to the winding whose output is sensed. Switches S_1 and S_2 are switched on and off alternately in each half cycle of one PWM period with sufficient dead time to avoid shoot-through.

VI. Simulated Performance of the Proposed Bridgeless-Converter-Based Multiple-Output SMPS

Performance of the proposed multiple-output SMPS is simulated in MATLAB/Simulink environment using Sim-Power-System toolbox and discrete time sampling. A sampling time of 0.8 μs is considered during simulation. The waveforms, such as input voltage v_{in}, input current i_{in}, buck–boost converter output voltage V_{dc}, inductor currents i_{Lp} and i_{Ln}, switch voltages V_{Sp} and V_{Sn}, currents I_{Sp} and I_{Sn}, multiple-output voltages V_{o1}, V_{o2}, V_{o3}, and V_{o4}, and respective output currents I_{o1}, I_{o2}, I_{o3}, and I_{o4} are depicted to demonstrate its performance. Various power quality indices such as displacement PF, distortion factor, PF, and input current THD are analyzed for assessing the power quality at single-phase ac mains. Performance evaluation of the proposed bridgeless-converter-based multiple-output SMPS is categorized in terms of its performance during the following: 1) steady-state condition; 2) varying input voltages; and 3) load variations.

A. Performance Under Steady-State Condition

The performance of the proposed bridgeless-converter-based multiple-output SMPS at 220-V ac rms voltage and at full load is described in this section. Fig. 5(a) shows the input voltage v_{in}, input current i_{in}, buck–boost converter output voltage V_{dc}, and half-bridge VSI output voltages V_{o1}, V_{o2}, V_{o3}, and V_{o4} and currents I_{o1}, I_{o2}, I_{o3}, and I_{o4}. The input current is sinusoidal and in phase with the ac input voltage, ensuring high PF operation with very low harmonic distortion [Fig. 5(b)]. The output voltage of the buck–boost converter and output dc voltages of VSI are maintained constant. The harmonic distortion of the input current is on the order of 4.48%. The current stresses of the upper inductor and lower inductors, and the peak voltage and current stresses of switches S_p and S_n are shown in Fig. 5(c). The peak voltage of the switch is around 550 V, which is quite close to the calculated value, which is $V_{\mathrm{dc}} + v_{\mathrm{in}}$, i.e., 520 V. The inductor current waveform shows the DCM operation as it touches zero in every switching cycle. The enlarged view of upper inductor current and lower inductor

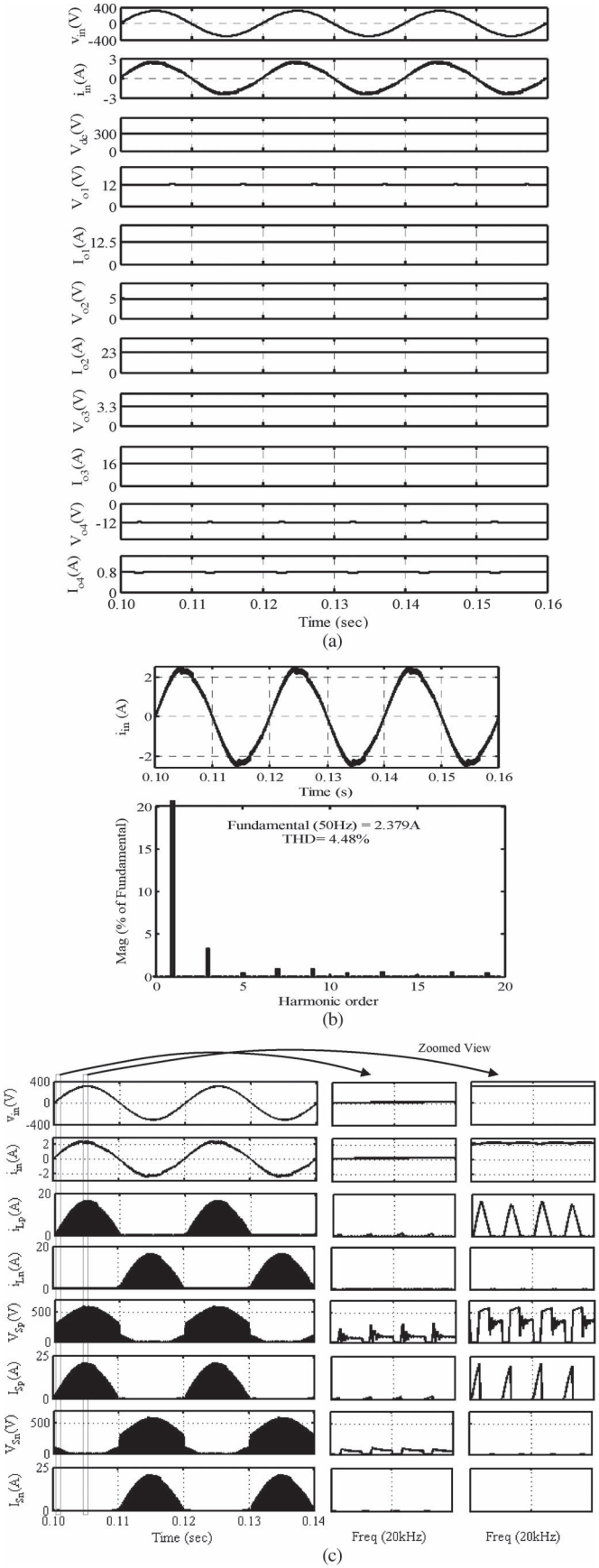


Fig. 5. (a) Input voltage, current, buck–boost converter output voltage, half-bridge VSI output voltages, and currents at 220 V and full load. (b) Waveform of input current and its harmonic spectrum at 220 V and full load. (c) Waveforms of v_{in}, i_{in}, i_{Lp}, i_{Ln}, V_{Sp}, I_{Sp}, V_{Sn}, and I_{Sn} at 220 V and full load.

TABLE II
POWER QUALITY INDICES OF BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

Input voltage(rms)	DPF	DF	PF	i_{in}(A)	i_{inTHD}(%)
170 V	1	0.9994	0.9994	2.17	3.30
220V	1	0.9989	0.9989	1.68	4.48
270V	1	0.9986	0.9986	1.38	5.29

current, and the peak voltage and current stresses of switches S_p and S_n at very low and peak input voltages are also shown in Fig. 5(c). It clearly shows the DCM of inductor current under all operating conditions. The upper inductor L_p and the lower inductor L_n operate in the positive and negative half cycles of the input voltage, respectively. This shows the satisfactory operation of the bridgeless converter of the proposed power supply.

B. Performance Under Varying Input Voltages

To demonstrate the performance of the proposed SMPS at varying input voltages, the input voltage is varied in the range of 170–270 V, and the performance is studied in detail. Table II shows the power quality indices of the proposed power supply at varying input voltages. At lower voltage, the THD of the input current is improved due to its increased value; this is required to maintain power balance. Thus, a high PF operation with improved input power quality is observed, which is within the limits set by IEC 61000-3-2.

C. Performance Under Varying Loads

To study the dynamic performance of the SMPS, a step change in loads is applied simultaneously on +12- and +5-V outputs. The load on +12-V output is varied from 100% to 20% at 0.15 s, and simultaneously in +5 V, it is varied from 100% to 70% at 0.25 s, as shown in Fig. 6(a). The output voltage of the buck–boost converter is maintained constant with a small overshoot. Multiple-output dc voltages remain constant. THD of the input ac mains current is observed as 5.14%, which is within the limit set by IEC 61000-3-2 [4], as shown in Fig. 6(b).

The simulated performance of bridgeless-converter-based multiple-output SMPS under the following conditions is found satisfactory: 1) steady-state condition; 2) at varying input voltages; and 3) varying loads. The input current harmonic content is within the international standard limits with unity PF at the utility interface [4].

VII. HARDWARE IMPLEMENTATION OF THE PROPOSED BRIDGELESS-CONVERTER-BASED SMPS

To validate the design and simulation, an experimental prototype of the bridgeless-converter-based multiple-output SMPS is developed, and the obtained test results are compared with the simulated results. A digital signal processor (DSP; TI-TMS320F2812) is used for providing PWM pulses to the bridgeless buck–boost converter devices through the PWM channels of the DSP. A Hall-effect voltage sensor is used to sense the output voltage of the buck–boost converter. The isolation between power circuit and the DSP is provided by an optocoupler 6N136. The performance of the proposed power supply is categorized in the three following subsections.

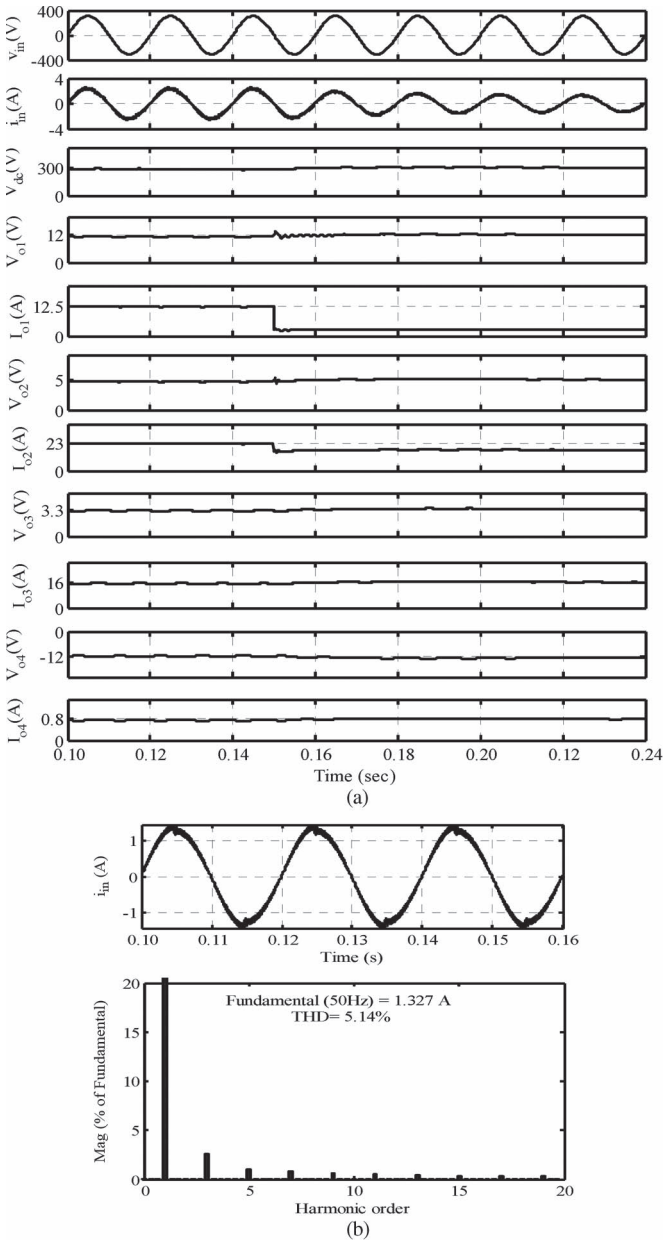


Fig. 6. (a) Input voltage, current, bridgeless buck–boost converter output voltage, half-bridge VSI output voltages, and currents at load variation in +12- and +5-V outputs at 0.25 s. (b) Waveform of input current and its harmonic spectrum at light load.

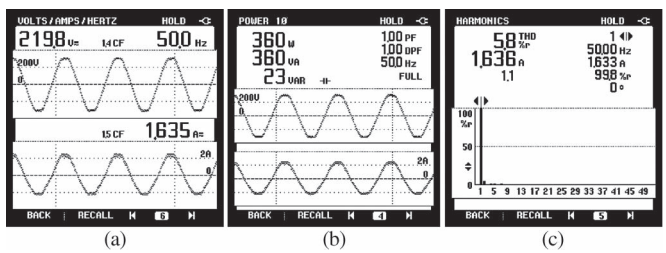


Fig. 7. (a) Input voltage and current at full load. (b) Input power and PF at full load. (c) Input current harmonic spectrum at full load.

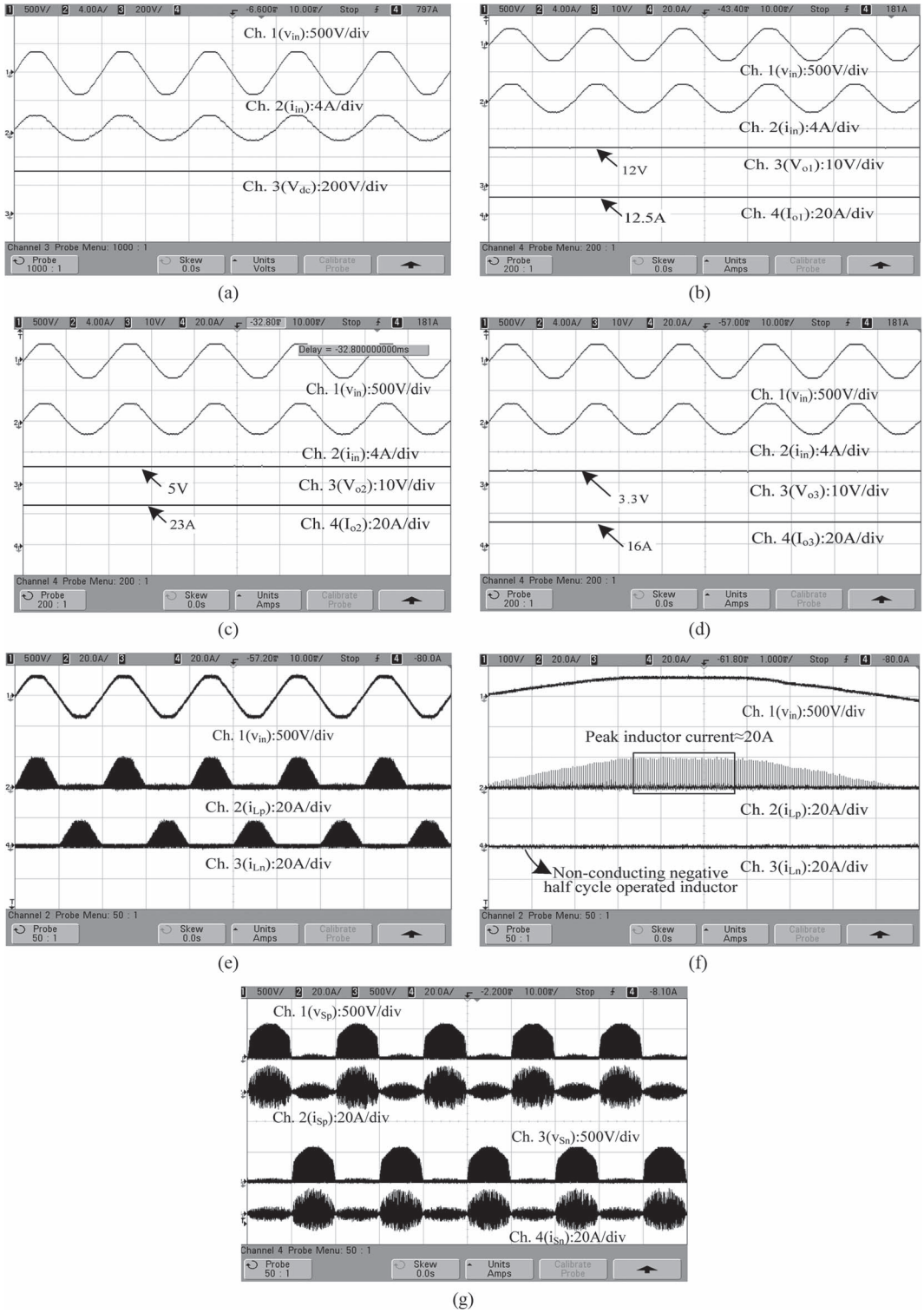
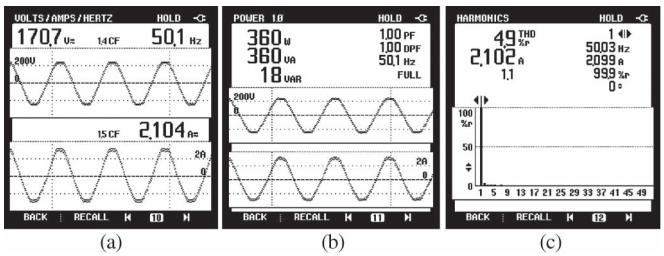


Fig. 8 (a) Waveforms of $v_{\rm in}$, $i_{\rm in}$, and $V_{\rm dc}$. (b) Waveforms of $v_{\rm in}$, $i_{\rm in}$, V_{o1}, and I_{o1}. (c) Waveforms of $v_{\rm in}$, $i_{\rm in}$, V_{o2}, and I_{o2}. (d) Waveforms of $v_{\rm in}$, $i_{\rm in}$, V_{o3}, and I_{o3}. (e) Waveforms of $v_{\rm in}$, $i_{\rm Lp}$, and $i_{\rm Ln}$ in DCM. (f) Enlarged view of $i_{\rm Lp}$ in DCM. (h) Waveforms of upper switch peak voltage and current, and lower switch peak voltage and current at rated load.

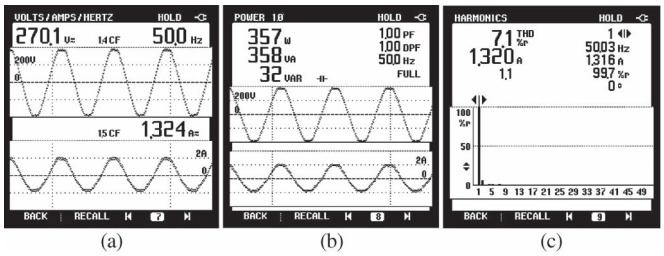
A. Steady-State Performance

The steady-state performance of the proposed multiple-output computer SMPS at rated load and an ac mains voltage of 220 V is shown in Fig. 7. The PF of the proposed power supply is unity at full load, as shown in Fig. 7(b). Fig. 7(c) shows the input current harmonic spectrum at 220 V and rated load. The THD of the input current is on the order of 5.8% at full load, which is within the limits of international power quality standards [4]. Fig. 8 shows the waveforms of buck–boost converter output voltage, half-bridge VSI output dc voltages, inductor currents, and peak voltage and peak current stresses of switches at rated voltage and full load. The output



(a) (b) (c)

Fig. 9. (a) Input voltage and input current at 170 V. (b) Input power and PF at 170 V. (c) Input current harmonic spectrum at 170 V.



(a) (b) (c)

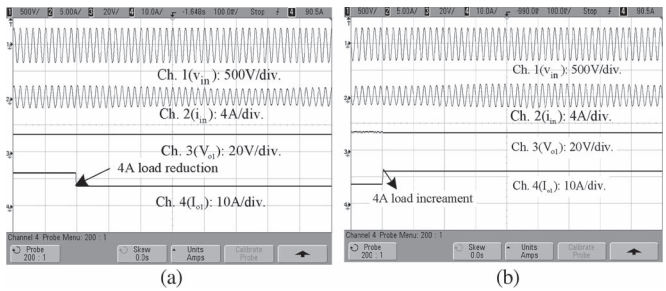
Fig. 10. (a) Input voltage and input current at 270 V. (b) Input power and PF at 270 V. (c) Input current harmonic spectrum at 270 V.

voltage of the buck–boost converter is maintained constant at 300 V, which is shown in Fig. 8(a). Fig. 8(b)–(d) shows the dc output voltages of +12, +5, and 3.3 V, respectively, with their respective output current waveforms. The output voltages of half-bridge VSI remain constant. The input voltage and the upper and lower inductor currents i_{Lp} and i_{Ln} are shown in Fig. 8(e). Both inductor currents touch zero in each switching cycle, demonstrating the buck–boost converter DCM operation. The enlarged view of the upper inductor current has been shown in Fig. 8(f). It is observed that the upper inductor L_p operates in the positive half, and the lower inductor L_n operates in the negative half cycle of the ac input voltage, ensuring satisfactory operation of the bridgeless converter. The voltage and current stresses of the upper and lower switches of the buck–boost converter at rated voltage and full load are shown in Fig. 8(h). The switch voltage is around 550 V, which is quite acceptable and in accordance with the simulated performance.

B. Performance Under Varying Input Voltages

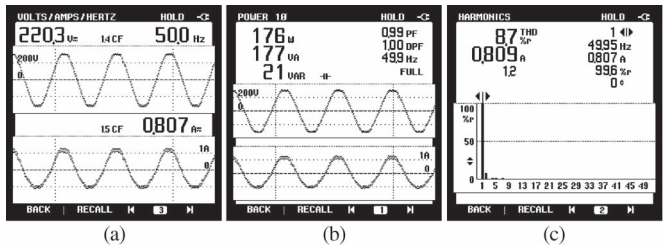
Under practical conditions, the SMPS continuously faces input voltage variation. To demonstrate the performance of the power supply at varying input voltages, the input voltage is varied in the range of 170–270 V, as shown in Figs. 9 and 10. At reduced voltage of 170 V, the THD of input ac current is on the order of 4.9%, as shown in Fig. 9(c). The voltage is increased to 270 V, and the corresponding test results are shown in Fig. 10. The THD of ac mains current at 270-V condition is 7.1%, as shown in Fig. 10(c). The PFs at under- and over-voltage conditions are unity, as shown in Figs. 9(b) and 10(b), respectively.

These test results show the high level performance of the power supply during input voltage variations.



(a) (b)

Fig. 11. (a) Load reduction in +12-V output. (b) Load increment in +12-V output.



(a) (b) (c)

Fig. 12. (a) Input voltage and current at light load. (b) Input power and PF at light load. (c) Input current harmonic spectrum at light load.

C. Performance Under Varying Loads

The dynamic behavior of the proposed bridgeless-converter-based multiple-output SMPS is demonstrated by varying the load on +12-V output. A step change in load is applied at +12-V output voltage, and the output current is reduced from 12.5 to 8.5 A. Test results at reduced load at +12-V output are shown in Fig. 11(a). The input current reduces and remains sinusoidal during the load reduction. The load is increased from 8.5 to 12.5 A, and the input current increases correspondingly. These test results for the load increment at +12-V output are shown in Fig. 11(b). The waveforms of the proposed SMPS at light-load condition (176 W) are shown in Fig. 12. The input current waveform remains sinusoidal and in phase with the input voltage, ensuring high PF at the ac mains. The input current THD at light-load condition is observed on the order of 8.7%, which is well below the IEC standard limit [4].

The losses in the proposed SMPS are the sum of losses in the PFC bridgeless converter and losses in the isolated converter. The losses in three different configurations of SMPS are shown in Fig. 13(a). The losses are low in the conventional SMPS in comparison to the two other configurations. However, the conventional SMPS is not recommendable due to high input current distortion, high crest factor, and low PF. The SMPS based on buck–boost converter PFC with diode bridge has lesser efficiency due to losses in the DBR, while the proposed SMPS has an improved efficiency due to the bridgeless configuration. The efficiency of the proposed SMPS at various loading conditions is shown in Fig. 13(b). At light load, the efficiency of the SMPS is marginally decreased due to the increased losses.

Fig. 14(a) shows the THD of input current at varying ac mains voltages for the conventional SMPS and the proposed SMPS. As discussed earlier, the harmonic distortion in a conventional SMPS is very high (75%–85%), which is not

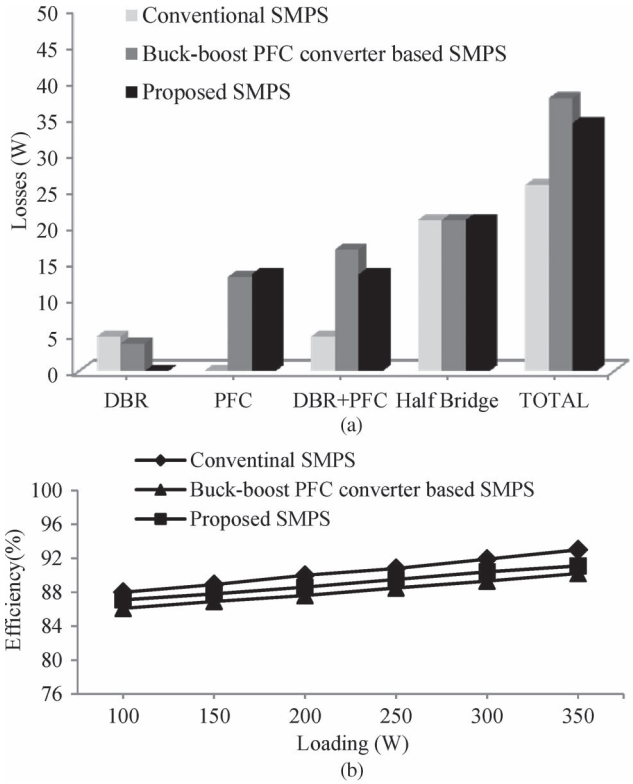


Fig. 13. (a) Comparison of losses of conventional SMPS, PFC-converter-based SMPS, and the proposed SMPS. (b) Comparison of efficiencies of conventional SMPS, PFC-converter-based SMPS, and the proposed SMPS at various loading conditions.

a recommended configuration as per the guidelines of IEC 61000-3-2 [4]. However, the input current THD of the proposed SMPS is well under the limits of IEC 61000-3-2 at varying input voltages. Fig. 14(b) shows the variation of PF of conventional SMPS and the proposed SMPS under varying input voltages. The PF of the proposed SMPS is close to unity, while the conventional SMPS suffers from poor PF. Therefore, the proposed SMPS can be recommended as a viable solution for the computer power supply application.

D. Comparison With Other Existing Bridgeless Topologies

Table III shows the comparison of the proposed SMPS with other bridgeless buck–boost-converter-based SMPS systems. The comparison is carried out on the basis of the following: 1) total number of components in the circuit, i.e., high-frequency switch, diodes, inductors, and capacitors, and 2) total number of components conducting during each half cycle of the ac input voltage. Only bridgeless buck–boost converter is preferred because it can handle larger voltage range in comparison to other buck and boost converters. The proposed configuration has minimum number of components and the least number of conducting devices during each half cycle of the input voltage, which make the proposed converter a preferred choice for PC applications.

An excellent performance of the proposed bridgeless-converter-based multiple-output SMPS is observed during steady-state condition, varying input voltages and loads in both

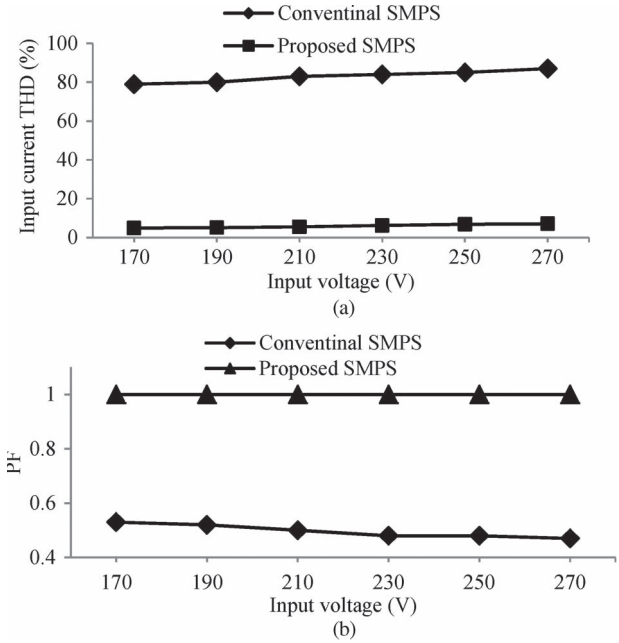


Fig. 14. (a) Comparison of input current THDs of the conventional SMPS and the proposed SMPS. (b) Comparison of PFs of the conventional SMPS and the proposed SMPS.

TABLE III
COMPARISON OF THE PROPOSED PFC CONVERTER WITH OTHER PFC CONVERTERS

Configuration	Components				Half cycle conduction
	Diode	Capacitor	Inductor	Switch	
Bridgeless SEPIC* [9]	2	4	3	2	10
Bridgeless Cuk converter [10]	2	3	3	2	7
Bridgeless Cuk converter[11]	3	2	3	2	8
Bridgeless Buck-boost converter [15]	4	3	1	3	8
Proposed*	4	2	2	2	6

*Two output capacitors are considered.

simulation and test results. Hence, it can be unequivocally stated that the proposed converter can be adopted for SMPS applications for PCs.

VIII. CONCLUSION

A bridgeless-converter-based multiple-output SMPS has been designed, modeled, simulated, and implemented in hardware to demonstrate its capability to improve the power quality at the utility interface. The output dc voltage of the first-stage buck–boost converter has been maintained constant, independent of the changes in the input voltage and the load, and it is operated in DCM to achieve inherent PFC at the single-phase ac mains. A satisfactory performance has been achieved during varying input voltages and loads with power quality indices remaining within the acceptable limits set by IEC 61000-3-2. Finally, a prototype of the proposed bridgeless-converter-based multiple-output SMPS has been developed to validate its performance experimentally. The proposed SMPS has shown satisfactory performance, and hence, it can be recommended as a tangible solution for computers and other similar appliances.

APPENDIX

Nominal input ac mains voltage	220 V, 50 Hz;
half-bridge VSI input voltage	300 V;
gains	K_p : 0.34, K_i : 0.45 (for bridgeless PFC); K_p : 0.6, K_i : 0.83 (for half-bridge VSI);
multiple dc output voltages/currents	12 V/12.5 A, 5 V/23 A, 3.3 V/16 A, and −12 V/ 0.8 A.

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