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An Integrated High-Power-Factor Converter with ZVS Transition

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***Abstract*—This paper proposes a single-phase high-power-factor ac/dc converter with soft-switching characteristic. The circuit topology is derived by integrating a boost converter and a buck converter. The boost converter performs the function of power-factor correction (PFC) to obtain high power factor and low current harmonics at the input line. The buck converter further regulates the dc-link voltage to provide a stable dc output voltage. Without using any active-clamp circuit or snubber circuit, the active switches of the proposed converter can achieve zero-voltage switching-on (ZVS) transition together with high power factor that satisfies the IEC 61000-3-2 standards over a wide load range from 30% to 100% rated power. The steady-state analysis is developed and a design example is provided. A prototype circuit of 60 W was built and tested. Experimental results verify the feasibility of the proposed circuit with satisfactory performance.**

***Keywords*—Boost converter, buck converter, power-factor correction (PFC), zero-voltage switching-on (ZVS).**

I. Introduction

Nowadays, switching-mode ac/dc converters have been widely used in many off-line appliances, such as dc uninterruptible power supply, telecommunications power supply, LED driver etc. [1-2]. The increasing amount urges researchers to develop more efficient, smaller size, and low cost ac/dc converters. In order to meet the standards of harmonic regulation such as IEC 61000-3-2 Class D and IEEE 519, a power-factor corrector is usually required.

Owing to the advantages of simple circuit topology and easy control, boost or buck-boost converters have been widely served as power-factor correctors [3-6]. In order to achieve unity power factor, it requires the output voltage of both converter be higher than the amplitude of the ac line voltage. Therefore, high-power-factor ac/dc converters usually consist of two stages. The first one is an ac-to-dc stage which performs the function of PFC and the second one is a dc-to-dc stage used to supply stable dc voltage to the load [7-10]. In spite of their good performance, the circuit efficiency of two-stage approaches is impaired since it takes two energy-conversion processes which inevitably introduce some losses including switching loss, conduction loss and magnetic core loss. Besides the two-stage approaches, the Cuk and the Sepic converters can also achieve high power factor and regulate the output voltage [11-14]. The Cuk converter is a combination of boost and buck converter and the Sepic converter is a combination of boost and buck-boost converter. Both converters have the advantage of simple circuit topology since they only use one active switch and one diode. High power factor can be achieved by operating the boost converter either at DCM or continuous conduction mode (CCM). The buck or buck-boost converter can further regulate the output voltage of the boost converter to obtain a smooth dc voltage. However, the output voltage of the boost converter is usually higher than the amplitude of the AC line voltage. Before turning on the active switch, the output voltage is across its parasitic capacitor. The energy stored in the parasitic capacitor is discharged at turning on the active switch, resulting in high switching losses and a high spike current. The boost, Cuk and Sepic converters can also be operated at critical conduction mode (CRM) to obtain high power factor. Synchronous rectification (SR) technique is popularly applied while operating these converters at CRM [15-17]. A MOSFET is used to replace the freewheel diode, and hence the conduction loss is effectively reduced. Furthermore, by extending the turn-on time of the synchronous switch, the inductor current would decline to negative. This negative inductor current can discharge the parasitic capacitance of the main switch to provide ZVS. However, SR technique requires additional control circuitry to adjust the timing of the switches. Moreover, the switching frequency is not constant, but varies a wide range within an AC line period while operating these converters at CRM.

In pursuit of high efficiency and high power factor, researchers have presented many single-stage ac/dc converters based on the integration of a PFC stage and a dc-to-dc stage [18-29]. By sharing one or two active switches, the single-stage approaches have the advantages of less component count, simply circuit topology and cost effective. As compared with two-stage approaches, the circuit efficiency is improved since only one power-conversion process is required. Among them, some single-stage approaches integrate a PFC converter with a full-bridge or half-bridge resonant converters. These resonant converters can operate with ZVS if the resonant circuits present inductive, i.e. the switching frequency is above the resonant frequency. Moreover, ZVS can be achieved within a wide load range by variable-frequency control or asymmetrical pulse-width modulation (APWM). Although, these

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topologies can effectively eliminate switching losses by switching the active switches near the resonance frequency to achieve ZVS, operating active switches near the resonance frequency companies with high resonant current and results in more conduction losses. The single-stage approaches that integrate two PWM converters also have some drawbacks that restrict further improving the circuit efficiency. The major problem is that the active switches usually operate in hard switching. An active switch that operates at hard switching not only generates high switching losses but also introduces high voltage and current stresses on circuit components, resulting in poor efficiency and low circuit stability.

The switching loss is theoretically proportional to the switching frequency. Now that hard-switching operation has serious switching losses in the active switches, it prevents converters from using small magnetic components and capacitors by increasing the switching frequency. In order to solve the problem of hard switching, some soft-switching techniques which adopt active-clamp circuit or snubber circuit have been proposed [30-36]. These soft-switching techniques have substantially eliminated the switching loss. However, these techniques need to use additional auxiliary switch, diode and reactive components to make the active switches turn on at zero-voltage. It adds the circuit complexity and overall cost. Besides, another conduction losses resulting from the circulating current in the active-clamp circuit would happen.

In this paper, a new ac/dc converter featuring ZVS with simple control is presented and analyzed. This paper is organized as follows. Section II presents the derivation of the circuit configuration and the circuit operation for the different operation modes. Detail circuit analysis and design equations are provided in Section III. In Section IV, a 60-W prototype circuit is built, and tested to verify the feasibility of the proposed converter. Finally, some conclusions are given in Section V.

II. Circuit Configuration and Operation Modes

Fig. 1 is an example of a high-power-factor ac/dc converter with a two-stage circuit topology. It consists of a boost converter and a buck converter. This two-stage converter can realize high-power factor with a wide load range. Nevertheless, both active switches of the converter operate at hard-switching condition, resulting in high switching losses and high current and voltage stresses.

In order to solve the problem resulting from hard switching, a new ac/dc converter is proposed, as shown in Fig. 2. The circuit topology is derived by relocating the positions of the semiconductor devices in Fig. 1. Here, MOSFETs S_1 and S_2 play the roles of active switches and the antiparallel diodes D_{S1} and D_{S2} are their intrinsic body diodes, respectively. The proposed circuit mainly consists of a low-pass filter (L_m and C_m), a diode-bridge rectifier (D_1-D_4), a boost converter and a buck converter. The boost converter is composed of L_p, D_{S1}, S_2 and C_{dc} and the buck

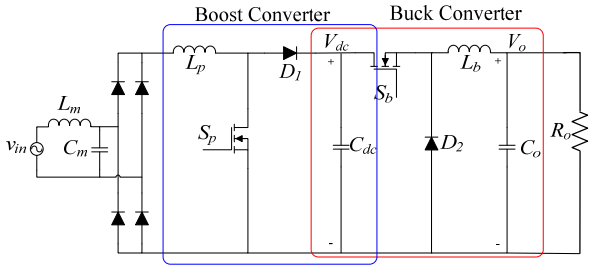

Fig. 1. Two-stage ac/dc converter.

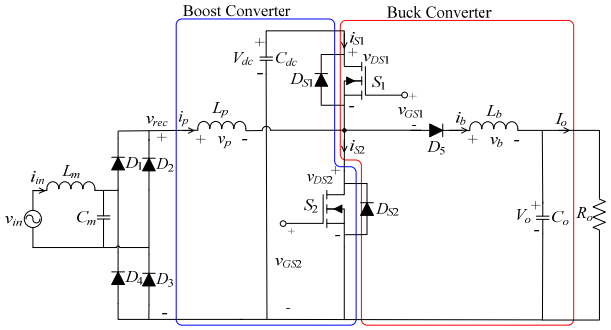

Fig. 2. Circuit topology of the proposed ac/dc converter.

converter is composed of L_b, D_5, D_{S2}, S_1 and C_o. Both converters operate at a high-switching frequency, f_s. The boost converter performs the function of PFC. When it operates at discontinuous-conduction mode (DCM), the average value of its inductor current in every high-switching cycle is approximately a sinusoidal function [5]. The low-pass filter is used to remove the high frequency current of the inductor current. By this way, the boost converter can waveshape the input line current to be sinusoidal and in phase with the input line voltage. In other word, high power factor and low total current harmonic distortion (THDi) can be achieved. The buck converter further regulates the output voltage of the boost converter to supply stable dc voltage to the load. It is also deigned to operate at DCM for achieving ZVS based on the reason that will be discussed in the final of this section.

Two gate voltages, v_{GS1} and v_{GS2} from a half-bridge gate driver integrated circuit (IC) are used to alternately turn S_1 and S_2 on and off. These voltages are complementary rectangular-wave voltages. In order to prevent both active switches from cross conducting, there is a short non-overlap time defined as "dead time". In the dead time, v_{GS1} and v_{GS2} are at a low level. Neglecting the short dead time, the duty cycle of v_{GS1} and v_{GS2} is 0.5.

For simplifying the circuit analysis, the following assumptions are made:

1) The semiconductor devices are ideal except for the parasitic output capacitance of the MOSFETs.
2) The capacitances of C_{dc} and C_o are large enough that the dc-link voltage V_{dc} and the output voltage V_o can be regarded as constant.

At steady state, the circuit operation can be divided into eight modes in every high-frequency cycle. Fig. 3 shows the

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equivalent circuits for each of the operation modes. In these equivalent circuits, the low-pass filter and the diode rectifier are represented by the rectified voltage v_{rec}. Fig. 4 illustrates the theoretical waveforms in each mode for the case of operating the buck converter at DCM. The circuit operation is described as follows.

A. Mode I ($t_0 < t < t_1$)

Prior to Mode I, S_1 is at "ON" state. The boost-inductor current i_p is zero and the dc-link capacitor supplies the buck-inductor current i_b which flows through S_1, D_5, L_b and C_o.

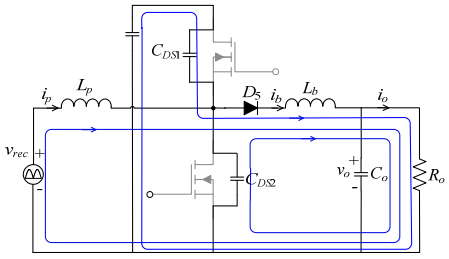
This mode starts when S_1 is turned off by the gate voltage, v_{GS1}. The time interval of this mode is the turn-off transition. At the beginning of this mode, i_b is diverted from S_1 to flow through the output capacitors C_{DS1} and C_{DS2}. C_{DS1} and C_{DS2} are charged and discharged, respectively. As the voltage across C_{DS2} (v_{DS2}) decreases to be lower than the rectified input voltage v_{rec}, the boost-inductor current i_p starts to increase. When v_{DS2} reaches -0.7 V, D_{S2} turns on and Mode I ends.

B. Mode II ($t_1 < t < t_2$)

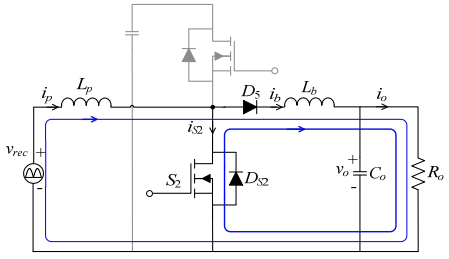
At the beginning of Mode II, voltage v_{DS2} is maintained at about -0.7 V by the antiparallel diode D_{S2}. After the short dead time, S_2 is turned on by the gate voltage, v_{GS2}. If the on-resistance of S_2 is small enough, most of i_b will flow through S_2 in the direction from its source to drain. Neglecting this small value of v_{DS2}, the voltage across L_b and L_p are equal to

$$v_b(t) = -V_o \tag{1}$$

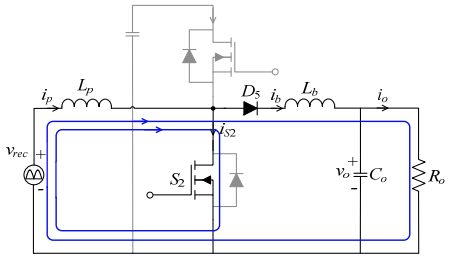
$$v_p(t) = v_{rec}(t) = V_m \left| \sin(2\pi f_L t) \right| \tag{2}$$



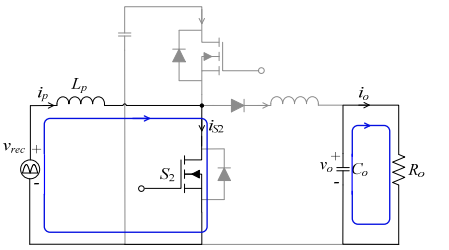
(a) Mode I



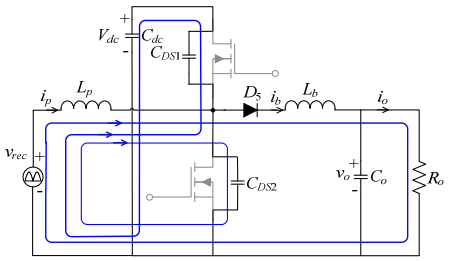
(b) Mode II



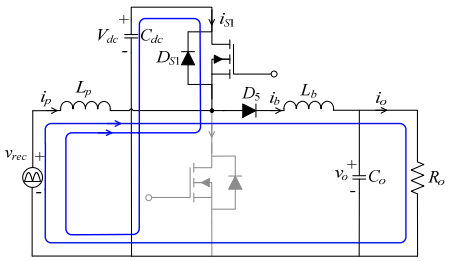
(c) Mode III



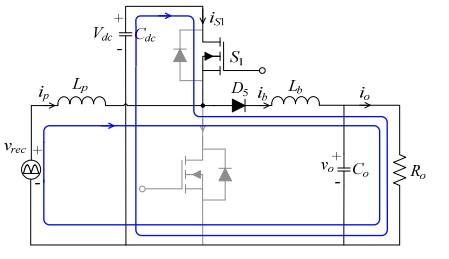
(d) Mode IV



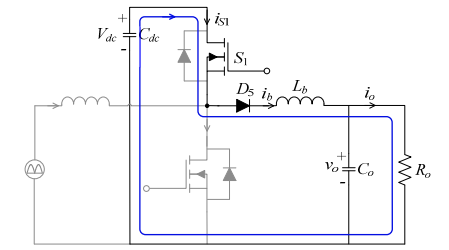
(e) Mode V



(f) Mode VI



(g) Mode VII



(h) Mode VIII

Fig. 3. Operation modes.

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where f_L and V_m are the frequency and the amplitude of the input line voltage, respectively. Since the time interval of Mode I is very short, i_b can be expressed as:

$$i_b(t) = i_b(t_0) - \frac{V_o}{L_b}(t - t_0) \tag{3}$$

From (3), i_b decreases from a peak value. The boost converter is designed to operate at DCM, therefore i_p increases linearly from zero with a rising slope that is proportional to v_{rec}.

$$i_p(t) = \frac{v_{rec}}{L_p}(t - t_0) = \frac{V_m \left|\sin(2\pi f_L t)\right|}{L_p}(t - t_0) \tag{4}$$

In Mode II, i_b is higher than i_p. Current i_b has two loops. Parts of i_b flow through S_2 and the rest are equal to i_p and flow through the line-voltage source, diode rectifier and L_p. This mode ends when i_p rises to become higher than i_b.

C. Mode III ($t_2 < t < t_3$)

In Mode III, i_p is higher than i_b. Current i_p has two loops. Parts of i_p are equal to i_b and flow into the buck converter, while the rest flow through S_2. The current direction in S_2 is naturally changed, i.e. from drain to source. The voltage and current equations for v_b, v_p, i_b and i_p are the same as (1) – (4). Current i_b decreases continuously. On the contrary, i_p keeps increasing. Since the buck converter is designed to operate at DCM, i_b will decrease to zero at the end of this mode.

D. Mode IV ($t_3 < t < t_4$)

In this mode, S_2 remains on to carry i_p. Beacuse i_b is zero, the buck converter is at "OFF" state and the output capacitor C_o supplies current to load. When S_2 is turned off by the gate voltage v_{GS2}, Mode IV ends.

E. Mode V ($t_4 < t < t_5$)

Current i_p reaches a peak value at the time instant of turning off S_2. For maintaining flux balance in L_p, i_p will be diverted from S_2 to flow through C_{DS1} and C_{DS2} when S_2 is turned off. C_{DS1} and C_{DS2} are discharged and charged, respectively. Current i_b is zero at the beginning of this mode, and will start to increase when the voltage across C_{DS1} (v_{DS1}) decreases to be lower than V_{dc}-V_o, that is the voltage across L_b becomes positive. As v_{DS1} reaches -0.7 V, D_{S1} turns on and Mode V ends.

F. Mode VI ($t_5 < t < t_6$)

At the beginning of Mode VI, v_{DS1} is maintained at about -0.7 V by the antiparallel diode D_{S1}. After the short dead time, S_1 is turned on by v_{GS1}. If the on-resistance of S_1 is small enough, most of i_p will flow through S_1 in the direction from its source to drain. Neglecting this small value of v_{DS1}, the voltage imposed on L_p and L_b can be respectively expressed as

$$v_p(t) = v_{rec}(t) - V_{dc} = V_m\left|\sin(2\pi f_L t)\right| - V_{dc} \tag{5}$$

$$v_b(t) = V_{dc} - V_o. \tag{6}$$

For a boost converter, the dc-link voltage V_{dc} is higher than the rectified voltage v_{rec}. Neglecting the short turning off transition of S_2, i_p can be expressed as:

$$i_p(t) = i_p(t_4) - \frac{V_m\left|\sin(2\pi f_L t)\right| - V_{dc}}{L_p}(t - t_4) \tag{7}$$

On the contrary, the voltage across L_b is positive to make i_b rise from zero.

$$i_b(t) = \frac{V_{dc} - V_o}{L_b}(t - t_4) \tag{8}$$

In Mode VI, i_p is higher than i_b. There are two loops for i_p. Parts of i_p flow through S_1 to charge the dc-link capacitor C_{dc} and the rest are equal to i_b and flow into the buck converter. This mode ends when i_b rises to become higher than i_p.

G. Mode VII ($t_6 < t < t_7$)

In Mode VII, i_b is higher than i_p. There are two loops for i_b. Parts of i_b are equal to i_p and flow into the boost converter, while the rest flow through S_1. The current direction in S_1 is naturally changed, i.e. from drain to source. The voltage and current equations for v_p, v_b, i_p and i_b are the same as (5) – (8). Current i_b increases continuously while i_p keeps decreasing. The circuit operation enters next mode as soon as i_p decreases to zero.

H. Mode VIII ($t_7 < t < t_8$)

S_1 remains on and i_b keeps increasing. This mode ends at the time when v_{GS1} becomes a low level to turn off S_1 and, the circuit operation returns to Mode I of the next high-frequency cycle.

Based on the circiuit operation, prior to turning on one active switch, the output capactance is discharged to about 0.7 V by the inductor current. Then, the intrinsic body diode of the active switch turns on to clamp the active voltage at nearly zero voltage. By this way, each active switch achieves ZVS operation.

The reason for operating the buck converter at DCM is explained below. In operation Mode II, i_p rises and i_b decreases. It should be noted that i_p rises in proportional to the input voltage and has a small peak in the vicinity of zero-cross point of the input voltage. If the buck converter is operated at continuous-conduction mode (CCM), i_b could keep higher than i_p. On this condition, the circuit operation would not enter into Mode III and Mode IV, and v_{DS1} is maintain at about V_{dc}. When S_1 is turned on, i_b is diverter from S_2 to S_1. C_{DS1} is discharged at a high voltage of V_{dc}, resulting a spike current and high switching losses.

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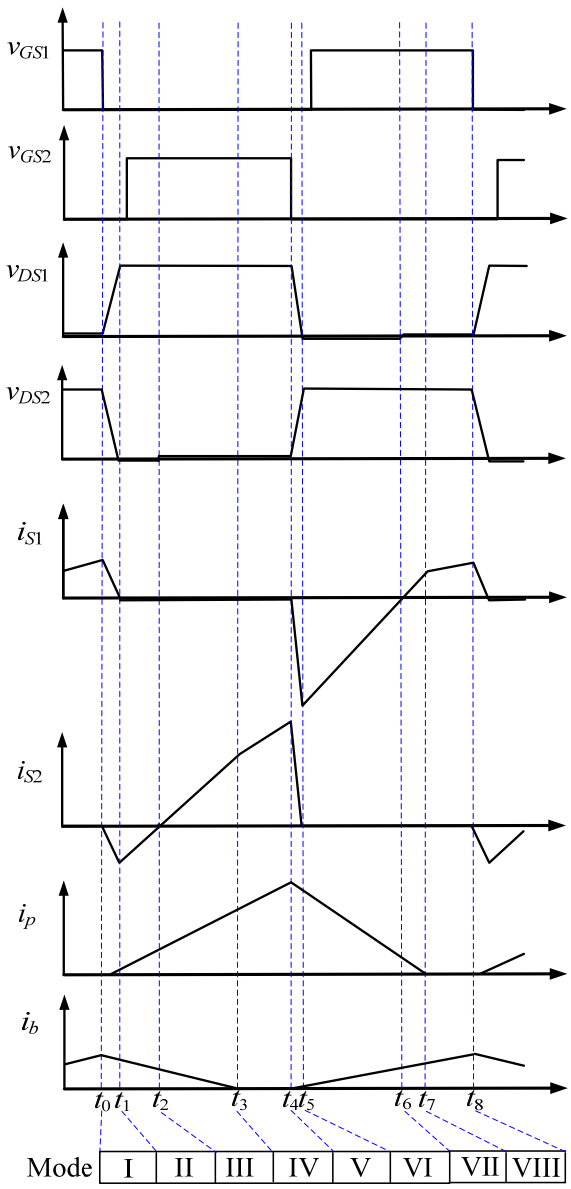

Fig. 4. Theoretical waveforms of the proposed converter.

III. Circuit Analysis

According to the circuit operation in the previous section, it can be seen that the antiparallel diode of the active switch of one converter serves as the freewheeling diode of the other converter. In spite of it, the feathers of the boost and the buck converter can be retained. Therefore, the two converters can be analyzed separately.

A. Boost-Converter-Type Power-Factor Corrector

The boost-inductor current i_p increases from zero and reaches a peak value at the end of Mode IV. In practical, the frequency of the input line voltage, f_L, is much lower than that of the converters. It is reasonable to consider the rectified input voltage v_{rec} as a constant over a high-frequency cycle. From (4), the peak values of i_p can be expressed as

$$i_{p,peak}(t)=\frac{V_m\left|\sin(2\pi f_L t)\right|}{L_p}(t_4-t_0)=\frac{V_m\left|\sin(2\pi f_L t)\right|T_s}{2L_p} \quad (9)$$

where T_s is the high-frequency switching period. At the beginning of Mode V, i_p start to decrease. Eq. (7) can be rewritten as

$$i_p(t)=\frac{V_m\left|\sin(2\pi f_L t)\right|T_s}{2L_p}-\frac{V_m\left|\sin(2\pi f_L t)\right|-V_{dc}}{L_p}(t-0.5T_s). \quad (10)$$

From (10), the duration of the interval during which i_p decreases from the peak value to zero is described by

$$t_{p,off}(t)=\frac{0.5T_sV_m\left|\sin(2\pi f_L t)\right|}{V_{dc}-V_m\left|\sin(2\pi f_L t)\right|}. \quad (11)$$

In order to operate the boost converter at DCM, $t_{p,off}(t)$ must always be less than half of the switching period.

$$t_{p,off}(t)\le 0.5T_s. \quad (12)$$

Combining (11) and (12), V_{dc} should be high enough to ensure DCM operation over an entire input line-frequency cycle, as follows:

$$V_{dc}\ge 2V_m. \quad (13)$$

The conceptual waveform of i_p is shown in Fig. 5. It is noted that the peak values of i_p follow a sinusoidal envelope. The average value of i_p over a high-frequency cycle is given by

$$\overline{i_p}(t)=\frac{\left(0.5T_s+t_{p,off}(t)\right)\cdot i_{p,peak}(t)}{2T_s}. \quad (14)$$

It results in (15) by substituting (9) and (11) into (14).

$$\overline{i_p}(t)=\frac{V_m\left|\sin(2\pi f_L t)\right|}{8\cdot L_p\cdot f_s}\cdot\frac{1}{1-\frac{1}{k}\cdot\left|\sin(2\pi f_L t)\right|} \quad (15)$$

where the index k is defined as

$$k\equiv\frac{V_{dc}}{V_m}. \quad (16)$$

Considering the effect of diode-bridge rectification and the low-pass filter that can remove the high-frequency contents of i_p, the input current i_{in} is equal to the average value of i_p, as follows:

$$i_{in}(t)=\frac{V_m\sin(2\pi f_L t)}{8\cdot L_p\cdot f_s}\cdot\frac{1}{1-\frac{1}{k}\cdot\left|\sin(2\pi f_L t)\right|}. \quad (17)$$

It can be seen that i_{in} will be close to a sinusoidal waveform at a large value of k. In other words, V_{dc} should be

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high enough to have a sinusoidal input current. Using (16) and (17), the input power can be obtained by taking average of the instantaneous product of the input voltage and current over one line-frequency cycle.

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} V_m \sin(2\pi f_L t)\cdot i_{in}(t)\, d(2\pi f_L t) = \frac{V_m^{\,2}}{8\cdot L_p \cdot f_s}\cdot y \tag{18}$$

where y is expressed in (19), as follows: [4]

$$y = \int_0^{\pi} \frac{\sin^2\theta}{1-\frac{1}{k}\sin\theta} d\theta = \frac{k^3}{\sqrt{k^2-1}}\left(1+\frac{2}{\pi}\sin^{-1}\frac{1}{k}\right) - k^2 - \frac{2}{\pi}\cdot k \tag{19}$$

Assuming a circuit efficiency of η, the output power can be expressed as

$$P_o = \frac{\eta V_m^{\,2}}{8\cdot L_p \cdot f_s}\cdot y \tag{20}$$

The root-mean-squared value of the input current is calculated by using (17).

$$I_{in,rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_{in}^2(t)\cdot d(2\pi ft)} = \frac{V_m}{8\sqrt{\pi}\cdot L_p \cdot f_s}\cdot\sqrt{z} \tag{21}$$

where z is expressed in (22), as follows: [5]

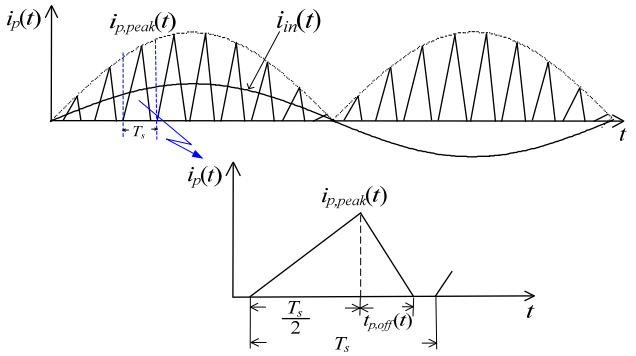

Fig. 5. Conceptual waveform of the boost-inductor current.

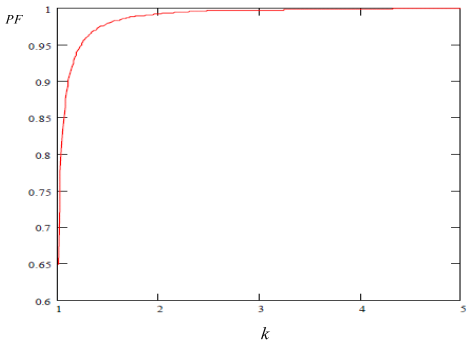

Fig. 6. Power factor versus k. ($k = V_{dc}/V_m$).

$$z = \int_0^{\pi}\left(\frac{\sin\theta}{1-\frac{1}{k}\sin\theta}\right)^2 d\theta \tag{22}$$

$$= \frac{2k^4}{k^2-1} + \pi k^2 + \frac{2k^3\left(2-k^2\right)}{\left(k^2-1\right)^{3/2}}\cdot\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{\sqrt{k^2-1}}\right)\right] \tag{18}$$

Since the input voltage is purely sinusoidal, the power factor defined as the ratio of input power to the product of the root-mean-squared values of input voltage and current can be obtained by using (18) and (21).

$$PF = \frac{P_{in}}{\frac{V_m}{\sqrt{2}} I_{in,rms}} = \frac{\sqrt{2\pi}\, y}{\sqrt{z}}. \tag{23}$$

The power factor as a function of k is calculated and plotted in Fig. 6 by using (19), (22) and (23). As shown, high power factor can be achieved at a high-valued k. From (13), the index k should be higher than 2. In this situation, power factor is better than 0.99.

B. Buck Converter

For DCM operation, i_b rises from zero. Neglecting the short transition of turning off S_2, the rising time of i_b is equal to $0.5T_s$. From (8), i_b has a peak value that is equal to

$$i_{b,peak} = \frac{(V_{dc} - V_o)T_S}{2L_b} \tag{24}$$

The current i_b starts to decrease when S_1 is turned off. By using (3), the time duration for i_b decreasing from the peak value to zero is given by

$$t_{b,off} = \frac{(V_{dc} - V_o)T_S}{2V_o} \tag{25}$$

For fulfilling DCM operation, $t_{b,off}$ should be less than $0.5T_s$. This leads to

$$V_{dc} \le 2V_o \tag{26}$$

AS shown in Fig. 4, i_b is with a triangular waveform and its average value can be derived by using (24) and (25).

$$\overline{i_b} = \frac{(0.5T_s + t_{b,off})i_{b,peak}}{2T_s} = \frac{(V_{dc} - V_o)V_{dc}T_s}{8L_bV_o} \tag{27}$$

At steady-state operation, the average value of i_b will be equal to the output current.

$$\overline{i_b} = I_o = \frac{V_o}{R_o} \tag{28}$$

Combining (27) and (28), the formula of L_b for DCM operation is derived, as follows:

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$$L_b = \frac{(V_{dc} - V_o)V_{dc}T_s}{8V_oI_o} = \frac{(V_{dc} - V_o)V_{dc}}{8P_of_s} \quad (29)$$

IV. Design Example and Experimental Results

An illustrative example for driving sixty 1-W high-brightness LEDs is provided. These LEDs are connected in series. The rated voltage and current of each LED are 3.6 V and 0.28 A, respectively. Table I lists the circuit specifications. The input voltage is 110 V_{rms} ± 10%. The switching frequency is 50 kHz at rated power operation. In this design example, both converters are designed to operate at DCM. The circuit parameters are designed as follows.

A. Parameters Design

From (13) and (26), V_{dc} should be limited between $2V_m$ to $2V_o$. Taking the consideration of 10% input voltage fluctuation, V_{dc} is chosen to be

$$V_{dc} = 360 \text{ V}.$$

In this case, k is calculated to be 2.3. From Fig. 6, the power factor higher than 0.99 can be expected.

Assuming 95% circuit efficiency, L_p and L_b can be calculated by using (18) and (29) respectively.

$$L_p = \frac{0.95\times155^2}{8\times50\times10^3\times60}\cdot\left[\frac{k^3}{\sqrt{k^2-1}}\left(1+\frac{2}{\pi}\sin^{-1}\frac{1}{k}\right)-k^2-\frac{2}{\pi}k\right]$$

$$=0.76 \text{ mH} \quad (k = 2.3)$$

$$L_b = \frac{(360-216)\times360}{8\times216\times0.28\times50\times10^3} = 2.14 \text{ mH}.$$

L_m and C_m are designed to perform as a low-pass filter to filter out the high-frequency components of the boost-inductor i_p. By rule of thumb, the natural frequency of a low-pass filter is about 1 decade below the switching frequency. Here, the natural frequency is designed to be 5 kHz, and L_m and C_m are determined to be

$$L_m = 2.16 \text{ mH}, C_m = 0.47 \text{ μF}.$$

B. Dimming operation

The LED had been tested at different power. Fig. 7 shows its *V-I* curve. Based on these experimental results, the LED voltage as a function of output power can be expressed as

$$V_o = 0.0003P_0^3 - 0.0407P_0^2 + 2.4742P_0 + 150 \quad (30)$$

For dimming operation, the output voltage is adjusted to regulate the LED current. As shown in (20), P_o is functions of y and f_s. From (19), the parameter y would vary slightly when k is in the neighbor of 2.3. Hence, it is reasonable to assume that P_o is inversely proportional to the switching frequency. By using (29), V_{dc} can be expressed as

$$V_{dc} = \frac{V_o + \sqrt{V_o^2 + 32L_bP_of_s}}{2} \quad (31)$$

Fig. 8 shows the theoretical curves of V_{dc} and f_s versus P_o. Using (30) and (31), if the LED is dimmed from 100% to 30% rated power, the switching frequency would vary form 50 kHz to 167 kHz. The dc-link voltage and the output voltage vary form 360 V to 336 V and 216 V to 183.1 V. During the dimming operation, (13) and (26) are satisfied to ensure both converters operate at DCM. In other words, the inductor current of one converter will decline to zero before turning off the active switch of the other converter. It ensures the intrinsic body diode of one active switch will be turned on to flow the inductor current when the other active switch is turned off. By this way, ZVS operation can be achieved within the dimming range.

A prototype circuit is built and tested. Table II lists the circuit parameters. Since the *I–V* characteristic of an LED is similar to that of a diode, a small variation in the LED voltage will result in a significant change in its current. Generally, constant current control with low-frequency pulse-width modulation is usually used to realize LED

TABLE I. Circuit Specifications.

Input Line Voltage, v_{in}	110 V_{rms}±10%, 60 Hz
High Switching Frequency, f_{S1} f_{S2}	50 kHz
Output Power, P_o	60 W
Output Voltage, V_o	216 V (= 3.6 V× 60)
Output Current, I_o	0.28 A

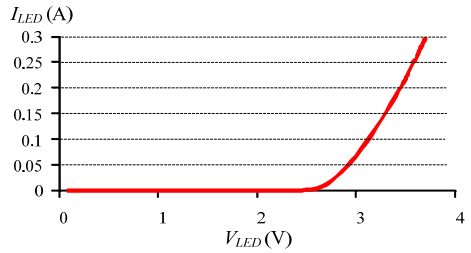

Fig. 7. *V-I* curve of tested LED.

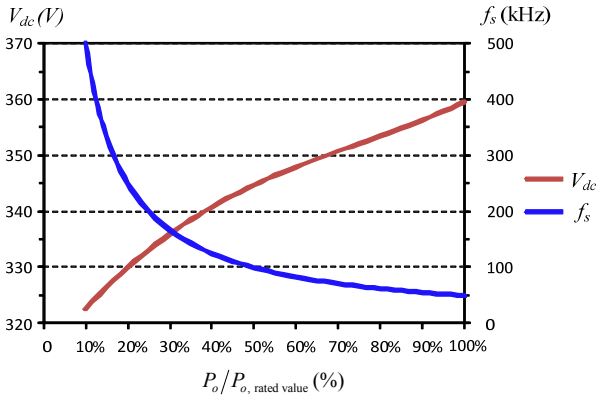

Fig. 8. V_{dc} and f_s versus P_o.

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dimming. However, it requires complicated circuit to precisely detect the peak value of the pulsed LED current. In this prototype circuit, sixty LEDs are connected in series and then, more voltage change is needed to dim the LED. It makes the series-connected LEDs can be easily dimmed by voltage control. Fig. 9 shows the closed-loop control circuit that mainly consists of a double-ended controller (L6599) for half-bridge topology and a photocoupler (PC817). The L6599 provides a pair of gate voltages with fixed dead time (0.3μs) to drive both active switches. Output voltage regulation is obtained by modulating the switching frequency. The feedback signal of the output voltage is transferred to pin 4 of the L6599 via the phototransistor of the optocoupler to modulate the switching frequency. The output voltage is varied by adjusting the variable resistor VR1 for dimming LED.

Fig. 10 to Fig. 13 shows voltage and current waveforms that are measured at rated output power. Fig. 10 shows the waveforms of the input voltage, the input current and the boost-converter current. It is seen that the boost converter operates at DCM over an entire cycle of the line voltage. The input current is close to a sinusoidal waveform. Besides, the input current and the input voltage are in phase with each other. High power factor and low THDi can be achieved. The measured power factor and THDi are 0.995 and 9.25%, respectively. It complies with the standards of IEC 61000-3-2 class D. Fig. 11 shows the waveforms of the output voltage and output current. The measured values well satisfy the theoretical prediction. The inductor-current waveforms of both converters are shown in Fig. 12. Both converters operate at DCM. Fig. 13 shows the voltage and current waveforms of the active switches which are measured at the peak point and the zero-crossing point of the input-line voltage, respectively. As shown, both active switches are switched on at nearly zero voltage. With ZVS operation at both active switches, the circuit efficiency is as high as 94.8%. It is noted that i_p is almost zero at the zero-crossing point of the AC voltage and cannot fully discharge the output capacitance of S_1 within the deadtime. When S_1 is turned on at the end of deadtime, the remaining charges in the output capacitance rapidly flow through S_1, resulting in a spike current, as shown in Fig. 13 (b). Since the non-ZVS operation only happens at the zero-crossing point of the AC input, it insignificantly impairs the circuit efficiency. In order to know how much efficiency can be improved with proposed circuit, a two-stage boost+buck prototyped circuit is built and tested with the same circuit specification as the proposed circuit. At 50 kHz switching frequency, the measure efficiency of the two-stage circuit is 90.7%.

The measured curves of power factor, THDi and circuit efficiency over a load range from 30% to 100% rated power are shown in Fig. 14. Power factor is close to unity over the wide load range, while THDi increases dramatically when the output power is less than 50% rated power. Since the output power is inversely proportional to the switching frequency, more circuit losses would happen at light load. The circuit efficiency drops to 0.84 at 30 % rated power.

TABLE II. CIRCUIT PARAMETERS.

Filter Inductor L_m	2.16 mH
Filter Capacitor C_m	0.47 μF
Boost Inductor L_p	0.76 mH
DC-Link Capacitors C_{dc}	100 μF
Buck Inductor L_b	2.14 mH
Buck Capacitor C_o	100 μF
Active Switches S_1, S_2	IRF840
Diodes D_5	MUR460

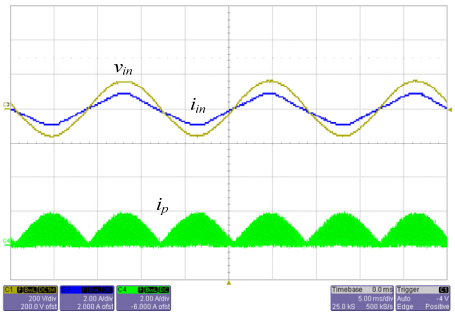
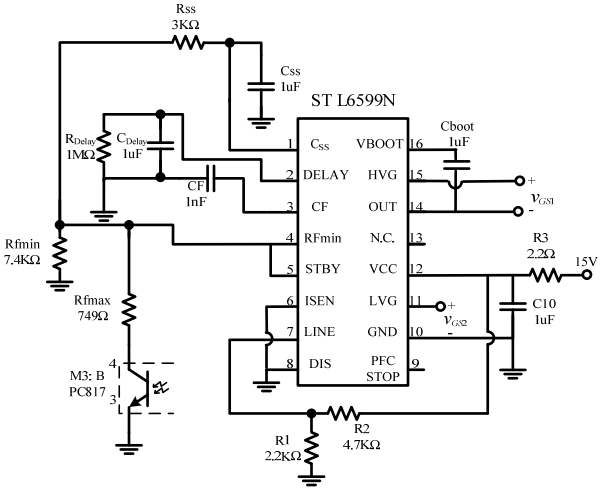


Fig. 10. Waveforms of v_{in}, i_{in} and i_p (v_{in}: 200 V/div, i_{in}, i_p: 2 A/div, time: 5 ms/div).



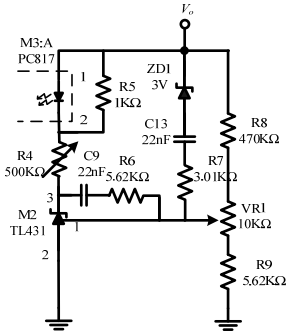


Fig. 9. Control circuit.

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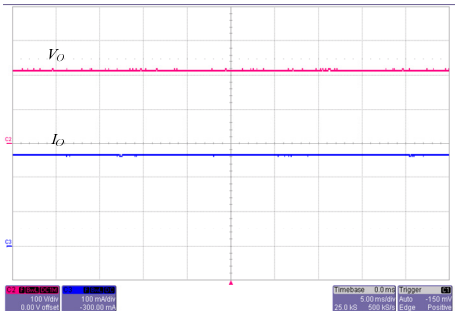


Fig. 11. Waveforms of V_o and I_o (V_o: 100 V/div, I_o: 0.1 A/div, time: 5 ms/div).

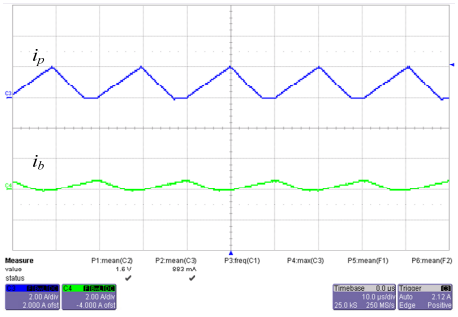
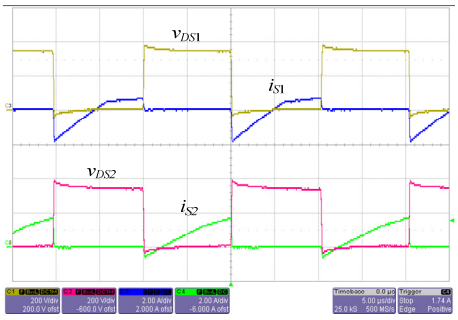
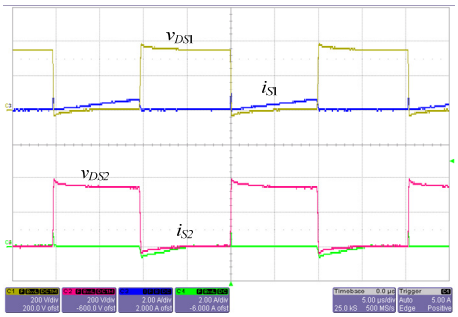


Fig. 12. Waveforms of i_p, and i_b (i_p, i_b: 2 A/div, time: 10 us/div).



(a)



(b)

Fig. 13. Waveforms of v_{DS1}, i_{S1}, v_{DS2}, and i_{S2} at (a) the peak point and (b) the zero-crossing point of the input-line voltage (v_{DS1}, v_{DS2}: 200 V/div, i_{S1}, i_{S2}: 2 A/div, time: 5 us/div).

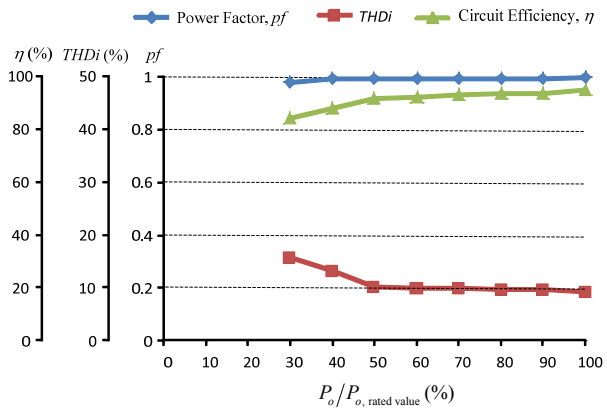


Fig. 14. Measured power factor, THDi and circuit efficiency for different output power.

V. Conclusions

A high efficiency ZVS ac/dc converter that integrates a boost converter and a buck converter is proposed. By freewheeling the inductor currents of the converters to flow through each of the intrinsic diodes of the MOSFETs, both active switches are turned on at ZVS. It assures high circuit efficiency. The boost converter is designed to operate at DCM to perform the function of PFC. It requires that dc-link voltage should be higher than two times of the amplitude of input voltage. The buck converter further regulates the dc-link voltage to obtain a stable dc voltage with low ripple. Experimental results based on the 60-W prototype circuit show that high circuit efficiency, high power factor and low THDi can be achieved over a wide load range. A circuit efficiency of 94.8%, power factor of 0.995 and a THDi of 9.25% are measured at rated output power.

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