Zero-Crossing Disturbance Elimination and Spectrum Analysis of Single-Carrier Seven-Level SPWM

Fengjiang Wu, Fan Feng, Jiandong Duan, and Bo Sun

***Abstract*—In this paper, a seven-level single-carrier and multi-modulation-wave sinusoidal pulsewidth modulation (SCMM-SPWM) strategy is proposed. In the negative half cycle of the modulation waves (MWs), dc offsets related to the amplitude of the carrier are set on the three MWs, respectively, to apply the same comparison logics of the MWs and carrier during positive and negative half cycles of the MWs. Thus, it is implemented with only one digital signal processor chip without any other attached logical circuit or controller. The reason for generating the zero-crossing voltage pulse disturbance (ZCVPD) in this strategy is analyzed, and the elimination of the ZCVPD is proposed and verified by experimental results. The spectral characters of the conventional multi-MW-based SPWM and the proposed one are originally derived and compared with each other by simulation in detail. The theoretical analysis, simulation, and experimental results indicate that the output characters of the proposed strategy are identical to those of the conventional one; it means that the proposed strategy can replace the conventional one while with the benefit of significantly reducing the cost and bulk of the implemental platform.**

***Index Terms*—Multi-modulation-wave (MW) sinusoidal pulsewidth modulation (SPWM), seven-level, spectral character, zero-crossing disturbance.**

I. Introduction

NOWADAYS, multilevel inverters become more and more attractive and have obtained expansive foreground not only in the field of the high-voltage and huge-power system but also in the low-voltage and small-power system, such as the photovoltaic generation system [1]–[3].

Various multilevel topologies have been proposed over the recent years [4]–[9]. Common ones are cascaded H-bridge [4], flying capacitor [5], and diode-clamped [6]. Furthermore, asymmetrical topologies consisted of two kinds of half-bridge legs with different level numbers are presented [7]–[9].

Compared with the symmetrical topologies, the asymmetrical ones significantly reduce the number of the power switches on the premise of obtaining the same level number of the output voltages. The reduction of the amount of power switches means that the overall loss, cost, and bulk can be further reduced.

However, multilevel pulsewidth modulation (PWM) strategies such as the multicarrier-based multilevel sinusoidal PWM (SPWM), the selective harmonic elimination PWM, and the voltage space-vector PWM [10]–[14] are difficult to be implemented only with a digital signal processor (DSP). In [15] and [16], the multilevel SPWMs are implemented with the DSP + complex programmable logic device or DSP + field-programmable gate array (FPGA) platforms. The attached controller increases the cost and decreases the reliability as well. A single-carrier and multi-modulation-wave (MW)-based multilevel SPWM (SCMM-SPWM) strategy is proposed in [17] and [18]. However, this kind of SPWM uses the same waveforms in the positive and negative half cycles of the MWs; in the negative half cycle, the compare logics between the MWs and the carrier need to be inversed against the positive ones to implement overall multilevel output PWM waveforms. The DSP can only implement the same compare logic in the positive half cycle and the negative one; thus, the attached digital logic circuits and dead-time generation circuit or controllers are still needed to switch the control signals of various power switches.

In the low-voltage and small-power system, e.g., in the photovoltaic grid-connected generation system, some control algorithms, including the grid current close-loop control, the maximum power point tracking control of the photovoltaic cells, and the dc link voltage close-loop control, are all needed to be performed. If some kind of multilevel PWM strategy suitable for being implemented with a DSP is developed, all of the former control algorithms and the multilevel PWM strategies can be performed with only one DSP chip; thus, the FPGA or the logic circuit is no longer indispensable. Unfortunately, none of the presented multilevel PWM strategies can be implemented only with a DSP if without any modification.

This paper proposed a seven-level SCMM-SPWM strategy based on MW reversed during negative half cycle. Furthermore, the reason for generating the zero-crossing voltage pulse disturbance (ZCVPD) in SCMM-SPWM is analyzed, and the elimination is proposed. Finally, the spectral characters of the single-carrier and multi-MW-based multilevel SPWM, including the conventional and proposed ones, are originally derived and are compared with each other by simulation. The proposed SCMM-SPWM has the following advantages. The cancelation of the attached logic circuit or controller makes the implementation platform more concise and cheaper and also indirectly improves reliability. As a result, the competitiveness of the

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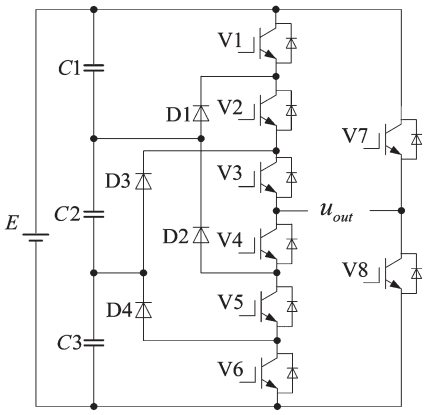

Fig. 1. Schematic of the eight-switch seven-level inverter.

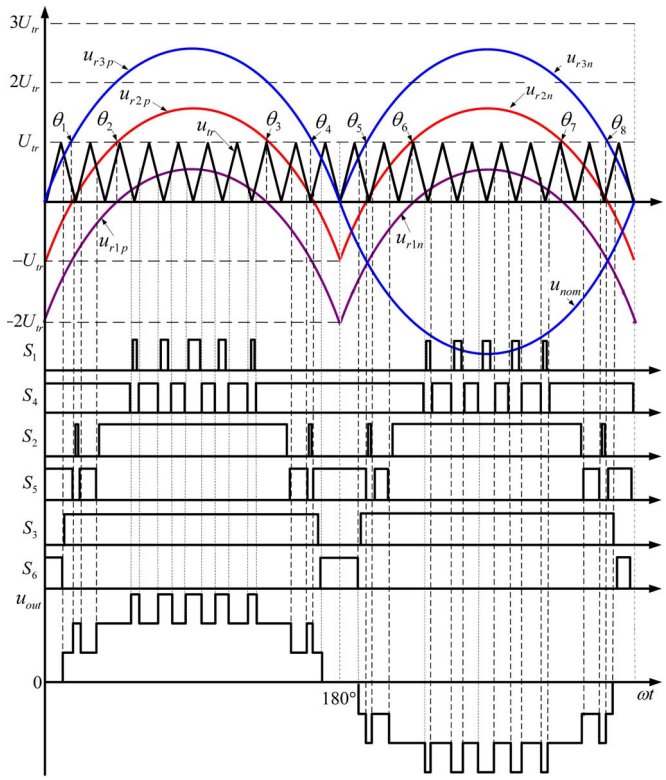

Fig. 2. Schematic of the conventional seven-level SPWM.

multilevel inverters against the two-level ones applied in the field of the low-voltage and small-power system is further enhanced.

II. Principle of the Proposed SCMM-SPWM

The schematic of the single-phase seven-level asymmetrical diode-clamped inverter is shown in Fig. 1. The left bridge arm is a four-level diode-clamped half bridge, and the right bridge arm is a two-level half bridge. The dead zone is set between the pairs of the complementary switches, i.e., V1 and V4, V2 and V5, V3 and V6, and V7 and V8.

The multilevel SPWM strategy in [18], which is called the "conventional seven-level SPWM" in this paper, is analyzed first. The sketch of the conventional seven-level SPWM is shown in Fig. 2. Three MWs are compared with the same carrier to generate seven-level output voltage waveform. In the

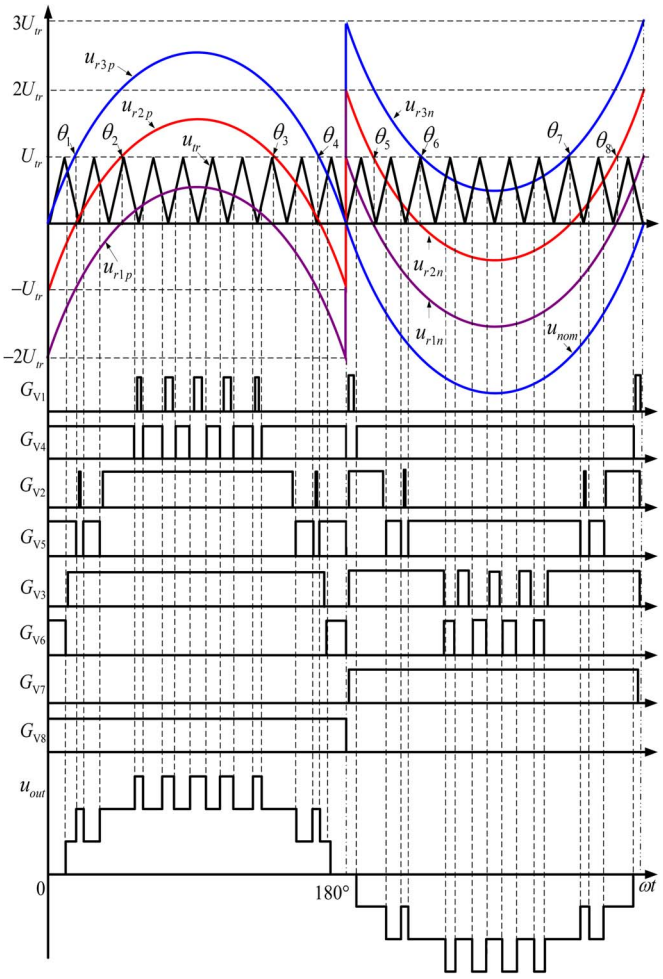

Fig. 3. Schematic of the proposed seven-level SCMM-SPWM.

positive half cycle of the MWs, the comparison results of the MWs and the carrier are directly used as the control signals of various power switches. However, in the negative half cycle of the MWs, the comparison results cannot be directly used to control the various power switches; the comparison results must be reconfigured. The logics between the actual control signals $(G_{V1}-G_{V6})$ and the comparison results (S_1-S_6) are

$$\begin{cases} G_{V1}=S_1\,\&\,S_4+\overline{S_3}\,\&\,\overline{S_4}, G_{V2}=S_2\,\&\,S_4+\overline{S_2}\,\&\,\overline{S_4} \\ G_{V3}=S_3\,\&\,S_4+\overline{S_1}\,\&\,\overline{S_4}, G_{V4}=\overline{S_1}\,\&\,S_4+S_3\,\&\,\overline{S_4} \\ G_{V5}=\overline{S_2}\,\&\,S_4+S_2\,\&\,\overline{S_4}, G_{V6}=\overline{S_3}\,\&\,S_4+S_1\,\&\,\overline{S_4}. \end{cases} \quad (1)$$

Because the logic operation depicted in (1) cannot be performed with a DSP, the attached logic circuit and dead-time generation circuit or FPGA chip should be added to implement this PWM strategy.

To solve the former problems, a novel SCMM-SPWM strategy is proposed and the principle is shown in Fig. 3. To obtain seven-level SPWM waveform without inverting the compare logic, three MWs in their negative half cycles are all inverted and biased with different dc values (related to the amplitude of the carrier). The functions of the three MWs are derived as follows. Define the amplitude of the carrier as $U_{\rm tr}$ and the normal sine MW as

$$u_{\rm nom} = U_{\rm nom}\sin(\omega_s t) \quad (2)$$

where $U_{\rm nom}$ and ω_s are the amplitude and the angular frequency of the normal MW, respectively. The function of the positive half cycle (denoted as u_{r3p}) of u_{r3} has the same format with the normal one. The function of the positive half cycle of u_{r1} is

$$u_{r1p} = U_{\rm nom}\sin(\omega_s t) - 2U_{\rm tr}. \tag{3}$$

The function of the negative half cycle of u_{r1} is

$$u_{r1n} = U_{\rm tr} + U_{\rm nom}\sin(\omega_s t). \tag{4}$$

The function of the positive half cycle of u_{r2} is

$$u_{r2p} = U_{\rm nom}\sin(\omega_s t) - U_{\rm tr}. \tag{5}$$

The function of the negative half cycle of u_{r2} is

$$u_{r2n} = 2U_{\rm tr} + U_{\rm nom}\sin(\omega_s t). \tag{6}$$

The function of the negative half cycle of u_{r3} is

$$u_{r3n} = 3U_{\rm tr} + U_{\rm nom}\sin(\omega_s t). \tag{7}$$

The amplitude modulation ratio of the proposed SCMM-SPWM strategy is

$$M = \frac{U_{\rm nom}}{3U_{\rm tr}}. \tag{8}$$

It can be known in Fig. 3 that, within the overall period of the MW, the exchange of the comparison logic of the carrier and MWs is not needed at all. The PWM signals of various power switches are obtained directly according to the comparison results of the carrier and MWs. It means that the proposed strategy can be implemented only with a DSP, and any other attached logic circuit or FPGA essential for the conventional one is not needed at all.

The laboratory experimental prototype of a seven-level inverter shown in Fig. 1 with a resistance–capacitor low-pass filter and DSP chip TMS30F2812 is designed. DC voltage E is 45 V, the frequency of the carrier is 10 kHz, and the frequency of the MWs is 50 Hz. Timer **T1** in DSP is used to generate the carrier. To obtain eight PWM signals, all the three compare registers (CMPR1–3) in DSP are used, and the IO ports, GPIOA6 and GPIOA7, are used to output the control signals of V7 and V8.

The experimental results with $M = 0.8$ are shown in Fig. 4. The actual three MWs have the same shapes with the waves shown in Fig. 3; the output voltage waveform $u_{\rm out}$ is seven level. However, the voltage pulse disturbances with the amplitude equal to E arise at the two zero-crossing points, which will increase the harmonics, loss and acoustic noise.

III. Elimination of ZCVPD in SCMM-SPWM

In this section, the reason for generating the ZCVPD is analyzed, and the corresponding elimination is proposed. As known from Fig. 3 that, when the phase angle is close to zero, before 0° angle, V1, V2, V3, and V7 are on and the other switches are off, i.e., $u_{\rm out} = 0$. If the states of the left and right arms are switched synchronously, i.e., after the 0° angle, V1,

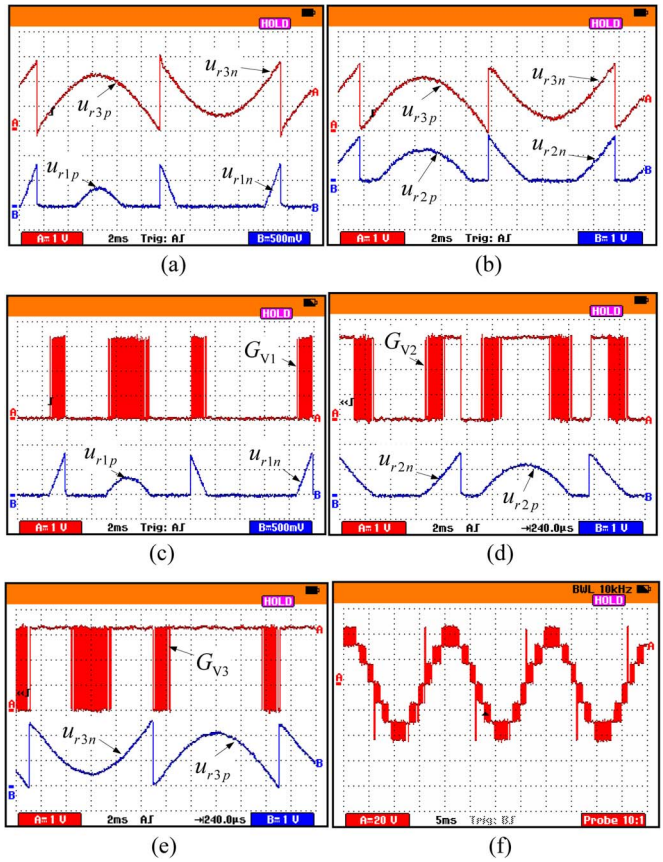

Fig. 4. Experimental waveforms of the proposed seven-level SPWM strategy. (a) u_{r1} and u_{r3}. (b) u_{r2} and u_{r3}. (c) G_{V1} and u_{r1}. (d) G_{V2} and u_{r2}. (e) G_{V3} and u_{r3}. (f) $u_{\rm out}$.

V2, V3, and V7 are turned off and V4, V5, V6, and V8 are turned on; $u_{\rm out}$ is still equal to zero. The voltage pulse disturbance will not occur. However, the control signals of the left arm are generated by the PWM generation module in the DSP; the control signals of the right arm are generated by the software program. The essential nonsynchronous phenomenon inevitably occurs between the former two control signals. Assuming that the right arm changes its output voltage in advance, i.e., V7 is turned off and V8 is turned on first. Before the control signals of the left arm are refreshed, V1, V2, V3, and V8 are on, and the output voltage $u_{\rm out} = +E$. After the control signals of the left arm are refreshed, V4, V5, V6, and V8 are on, the output voltage $u_{\rm out} = 0$, and the output voltage is back to normal. The action of $u_{\rm out} = +E$ is regarded as the voltage pulse disturbance. The duration of $u_{\rm out} = +E$ is equal to the delay time for refreshing the switching states between the left and right arms.

Furthermore, the dead zones between the complementary switch pairs will deteriorate the nonsynchronous phenomenon. Assume that the inverter drives a resistive–inductive load and the flowing direction of the output current is from $\boldsymbol{B}$ to $\boldsymbol{A}$ (as signed in Fig. 5). At 0°, during the exchanging process of the switching state of V7 and V8, the dead zone is set; during the dead time, V7 and V8 are both off. Because the output current holds its direction during the dead zone of V7 and V8, at the same time, V1, V2, and V3 are on, and the output current will flow through the antiparallel diodes of V1, V2, V3, and V8 to

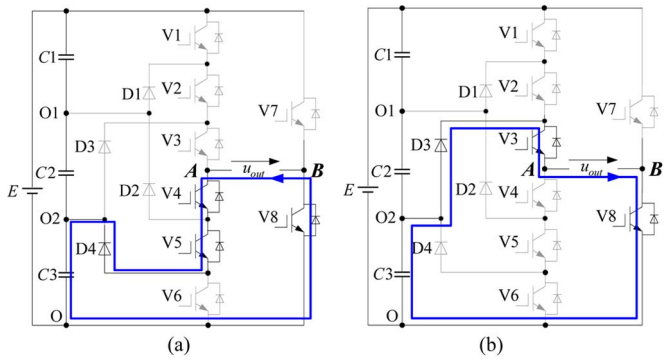

Fig. 5. Current routes with V3, V4, V5, and V8 on at 0°. (a) Current is not equal to zero. (b) Current is equal to zero.

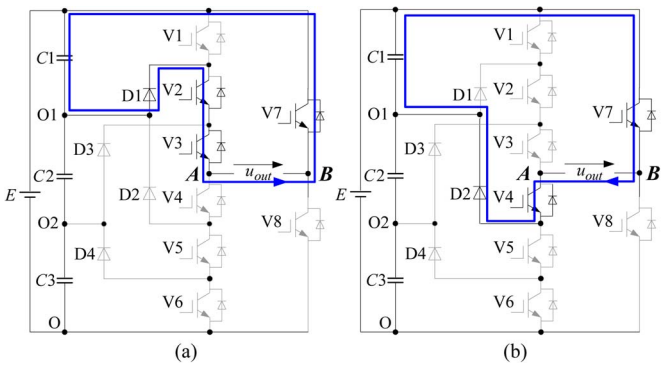

Fig. 6. Current routes with V2, V3, V4, and V7 on at 180°. (a) Current is not equal to zero. (b) Current is equal to zero.

the dc source; the output voltage $u_{\text{out}} = +E$ also appears as the voltage pulse disturbance. When the duration of the dead zone of V7 and V8 is over, V4, V5, V6, and V8 are on, $u_{\text{out}} = 0$, and the voltage pulse disturbance disappears. In the case of 180° angle, the reason is similar to the one of 0° angle; the amplitude of the output voltage pulse disturbance is equal to $-E$.

The corresponding solution is proposed and depicted as follows. Through forcibly changing the switching states of various power switches around the two zero-crossing points, the output voltage can be clamped at some one special level; thus, the voltage pulse disturbance can be eliminated.

At 0°, before V7 and V8 are both turned off, set V3, V4, and V5 to turn on first. Followed by this operation, all the other power switches are turned off. The corresponding current flowing route is shown in Fig. 5(a). In this case, $u_{\text{out}} = E/3$. Then, turning V8 on after the delay of dead time, if the output current is not equal to zero at the moment of V8 turning on, the flowing direction of the output current will not change, then the current flowing route remains unchanged until the current decays to zero. If the output current has been equal to zero, after V8 is turned on, the flowing route of the output current is switched to the case shown in Fig. 5(b); in this case, $u_{\text{out}} = E/3$. At this moment, if setting V4, V5, and V6 to turn on, the output voltage is equal to zero, and the voltage pulse shown in Fig. 5 is eliminated.

In the case of 180°, V2, V3, and V4 are turned on first, and all the other switches are turned off; the corresponding current flowing route is shown in Fig. 6(a), and in this case, $u_{\text{out}} = -E/3$. After the duration of the dead zone, setting V7 to turn on, the current flowing route in the case of the output current equal to zero is shown in Fig. 6(b); in this case, $u_{\text{out}} = -E/3$. The voltage pulse disturbance is eliminated at 180° in the similar manner.

The experimental results after eliminating the ZCVPD are shown in Fig. 7 with the amplitude modulation ratio $M = 0.3, 0.5, 0.8,$ and 1.1, which are corresponding to the cases of three-level, five-level, seven-level, and overmodulated output voltage waveforms, respectively. It is shown in these figures that the output voltages within the overall range of the amplitude modulation ratios are all implemented correctly. The waveforms of the low-pass filtered output voltage u_{LPF} are sinusoidal. The ZCVPDs are eliminated under various amplitude modulation ratios. Thus, the single-phase seven-level

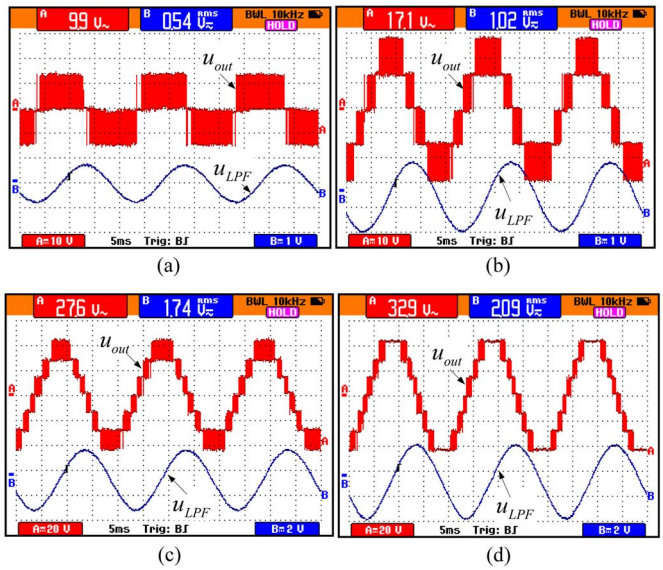

Fig. 7. Experimental waveforms of the output voltage and its low-pass filtered voltage under different amplitude modulation ratios. (a) $M = 0.3$. (b) $M = 0.5$. (c) $M = 0.8$. (d) $M = 1.1$.

asymmetrical diode-clamped inverter is correctly driven with a simple multilevel SPWM.

It must be pointed out that, since the voltage pulse disturbances are caused by the nonsynchronous update of the control signals, this kind of disturbance is not the inherent character of the proposed PWM strategy. From this point of view, the proposed elimination of the disturbance can be also used in other PWM strategies for asymmetrical inverters.

IV. Spectral Characters and Comparison

In this section, the detailed theoretical derivation of the spectral characters of the conventional SPWM strategy presented in [18] and the proposed one are performed. Since the voltage disturbance has been eliminated in the former section, in the following analysis, it is not considered. The phase angles of the carrier and the modulation functions are defined as

$$x = \omega_c t \quad y = \omega_s t \tag{9}$$

where ω_c is the angular frequency of the carrier.

Since the MWs and carrier are all periodic, the output voltage u_{out} can be defined as double Fourier series [19]

$$u_{\text{out}} = \frac{1}{2}A_{00} + \sum_{m=1}^{\infty}[A_{m0}\cos(mx) + B_{m0}\sin(mx)] + \sum_{m=1}^{\infty} \times \sum_{n=-\infty}^{\infty}[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)] \quad (10)$$

where

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_0^{2\pi}\int_{-\pi}^{\pi} u_{\text{out}} e^{j(mx+ny)}\,dx\,dy. \quad (11)$$

The key point of calculating C_{mn} is to determine the integral limits of x and y. The integral limits of y are determined first. During each cycle of the MW, there exist eight "critical angles". At each critical angle, some MW is equal to the envelope of the carrier, and the level number of the output voltage changes. Because within different regions (distinguished by the various critical angles), only one MW is compared with the carrier; by calculating these critical angles, the corresponding functions of the MWs compared with the carrier in various regions can be determined. The critical angles are calculated with $0.67 < M \le 1$ first. For the conventional one, at every critical point, according to (2), (5), and Fig. 2, it yields

$$\begin{cases} U_{\text{tr}} = U_{\text{nom}}\sin(\theta_1),\ U_{\text{tr}} = U_{\text{nom}}\sin(\theta_2) - U_{\text{tr}} \\ \theta_3 = \pi - \theta_2,\ \theta_4 = \pi - \theta_1 \\ U_{\text{tr}} = U_{\text{nom}}\sin(\theta_5 - \pi),\ U_{\text{tr}} = U_{\text{nom}}\sin(\theta_6 - \pi) - U_{\text{tr}} \\ \theta_7 = 3\pi - \theta_6,\ \theta_8 = 3\pi - \theta_5. \end{cases} \quad (12)$$

Then, the critical angles are calculated as

$$\begin{cases} \theta_1 = \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right),\ \theta_2 = \sin^{-1}\left(\frac{2U_{\text{tr}}}{U_{\text{nom}}}\right) \\ \theta_3 = \pi - \sin^{-1}\left(\frac{2U_{\text{tr}}}{U_{\text{nom}}}\right),\ \theta_4 = \pi - \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right) \\ \theta_5 = \pi + \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right),\ \theta_6 = \pi + \sin^{-1}\left(\frac{2U_{\text{tr}}}{U_{\text{nom}}}\right) \\ \theta_7 = 2\pi - \sin^{-1}\left(\frac{2U_{\text{tr}}}{U_{\text{nom}}}\right),\ \theta_8 = 2\pi - \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right). \end{cases} \quad (13)$$

As for the proposed one, because it has the uniform MWs with the conventional one in the positive half cycle, only the case of the negative half cycle needs to be derived. According to (4), (6), and Fig. 3, it yields

$$\begin{cases} 0 = U_{\text{tr}} + U_{\text{nom}}\sin(\theta_{15}),\ 0 = 2U_{\text{tr}} + U_{\text{nom}}\sin(\theta_{16}) \\ \theta_{17} = 3\pi - \theta_{16},\ \theta_{18} = 3\pi - \theta_{15}. \end{cases} \quad (14)$$

Then, the critical angles in the negative half cycle are

$$\begin{cases} \theta_{15} = \pi + \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right) = \theta_5,\ \theta_{16} = \pi + \sin^{-1}\left(\frac{2U_{\text{tr}}}{U_{\text{nom}}}\right) = \theta_6 \\ \theta_{17} = 2\pi - \sin^{-1}\left(\frac{2U_{\text{tr}}}{U_{\text{nom}}}\right) = \theta_7,\ \theta_{18} = 2\pi - \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right) = \theta_8. \end{cases} \quad (15)$$

When $0.33 < M \le 0.67$, u_{r1p} is always smaller than zero and u_{r3n} is larger than U_{tr}; the critical angles are

$$\theta_1 = \sin^{-1}\left(\frac{U_{\text{tr}}}{U_{\text{nom}}}\right),\ \theta_2 = \theta_3 = \frac{\pi}{2},\ \theta_6 = \theta_7 = \frac{3\pi}{2},\ \theta_8 = 2\pi - \theta_1. \quad (16)$$

TABLE I
INTEGRAL LIMITS OF x AND y OF THE CONVENTIONAL STRATEGY

u_{out}(pu)	y	x
1	$0 \le y < \theta_1$	$-3\pi M\sin y \le x \le 3\pi M\sin y$
2	$\theta_1 \le y < \theta_2$	$\pi - 3\pi M\sin y \le x \le -\pi + 3\pi M\sin y$
3	$\theta_2 \le y < \theta_3$	$2\pi - 3\pi M\sin y \le x \le -2\pi + 3\pi M\sin y$
2	$\theta_3 \le y < \theta_4$	$\pi - 3\pi M\sin y \le x \le -\pi + 3\pi M\sin y$
1	$\theta_4 \le y < \pi$	$-3\pi M\sin y \le x \le 3\pi M\sin y$
-1	$\pi \le y < \theta_5$	$3\pi M\sin y \le x \le -3\pi M\sin y$
-2	$\theta_5 \le y < \theta_6$	$\pi + 3\pi M\sin y \le x \le -\pi - 3\pi M\sin y$
-3	$\theta_6 \le y < \theta_7$	$2\pi + 3\pi M\sin y \le x \le -2\pi - 3\pi M\sin y$
-2	$\theta_7 \le y < \theta_8$	$\pi + 3\pi M\sin y \le x \le -\pi - 3\pi M\sin y$
-1	$\theta_8 \le y < 2\pi$	$3\pi M\sin y \le x \le -3\pi M\sin y$

TABLE II
INTEGRAL LIMITS OF x AND y OF THE PROPOSED STRATEGY

u_{out}(pu)	y	x
1	$0 \le y < \theta_1$	$-3\pi M\sin y \le x \le 3\pi M\sin y$
2	$\theta_1 \le y < \theta_2$	$\pi - 3\pi M\sin y \le x \le -\pi + 3\pi M\sin y$
3	$\theta_2 \le y < \theta_3$	$2\pi - 3\pi M\sin y \le x \le -2\pi + 3\pi M\sin y$
2	$\theta_3 \le y < \theta_4$	$\pi - 3\pi M\sin y \le x \le -\pi + 3\pi M\sin y$
1	$\theta_4 \le y < \pi$	$-3\pi M\sin y \le x \le 3\pi M\sin y$
-1	$\pi \le y < \theta_5$	$\pi + 3\pi M\sin y \le x \le \pi - 3\pi M\sin y$
-2	$\theta_5 \le y < \theta_6$	$2\pi + 3\pi M\sin y \le x \le -3\pi M\sin y$
-3	$\theta_6 \le y < \theta_7$	$3\pi + 3\pi M\sin y \le x \le -\pi - 3\pi M\sin y$
-2	$\theta_7 \le y < \theta_8$	$2\pi + 3\pi M\sin y \le x \le -3\pi M\sin y$
-1	$\theta_8 \le y < 2\pi$	$\pi + 3\pi M\sin y \le x \le \pi - 3\pi M\sin y$

When $M \le 0.33$, only u_{r3p} and u_{r1n} are compared with the carrier; the critical angles are determined as

$$\theta_1 = \theta_2 = \theta_3 = \theta_4 = \frac{\pi}{2},\ \theta_5 = \theta_6 = \theta_7 = \theta_8 = \frac{3\pi}{2}. \quad (17)$$

In the following, the integral limits of x with respect to different level numbers of the output voltages are analyzed. According to the amplitude relationships of the various MWs and the carrier, the ranges of the phase angle within one carrier cycle corresponding to different level numbers of the output voltages are derived; the results of the two PWM strategies are presented in Tables I and II.

The contour curves are plotted in Fig. 8. Each curve defines a transition in voltage. It is shown that the contour curves of the two strategies are different, which means different Fourier integral results.

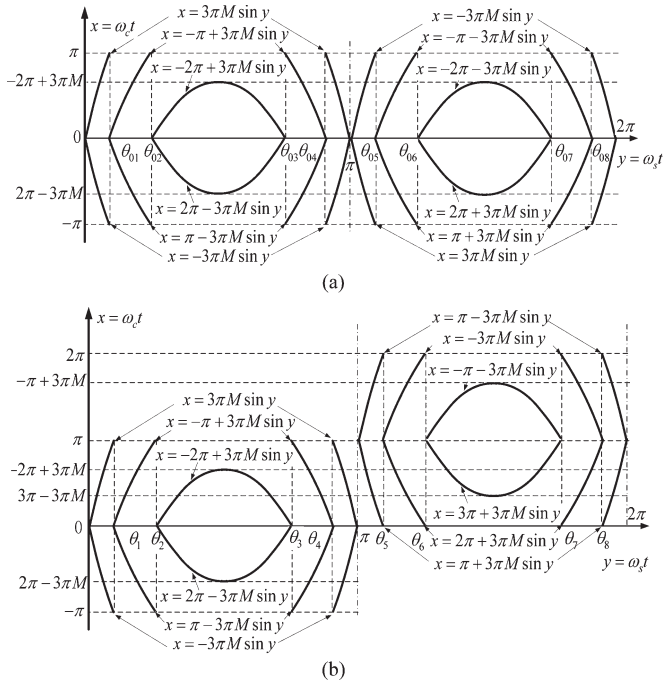

Fig. 8. Contour curves within 2π phase wraparound. (a) Conventional. (b) Proposed.

Utilizing the superposition principle, the Fourier integrals of the conventional one yield from Table I as

$$C_{mn} = \frac{1}{2\pi^2}\left[\int_0^{\theta_1}\int_{-3\pi M\sin y}^{3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_1}^{\theta_2} \times \int_{\pi-3\pi M\sin y}^{-\pi+3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_2}^{\theta_3} \times \int_{2\pi-3\pi M\sin y}^{-2\pi+3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_3}^{\theta_4} \times \int_{\pi-3\pi M\sin y}^{-\pi+3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_4}^{\pi} \times \int_{-3\pi M\sin y}^{3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\pi}^{\theta_5} \times \int_{3\pi M\sin y}^{-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_5}^{\theta_6} \times \int_{\pi+3\pi M\sin y}^{-\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_6}^{\theta_7} \times \int_{2\pi+3\pi M\sin y}^{-2\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_7}^{\theta_8} \times \int_{3\pi+3\pi M\sin y}^{-\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_8}^{2\pi} \times \int_{2\pi+3\pi M\sin y}^{-2\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_7}^{\theta_8} \times \int_{\pi+3\pi M\sin y}^{-\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_8}^{2\pi} \times \int_{3\pi M\sin y}^{-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy\right]. \tag{18}$$

The Fourier integrals of the proposed one yield from Table II as

$$C_{mn1} = \frac{1}{2\pi^2}\left[\int_0^{\theta_1}\int_{-3\pi M\sin y}^{3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_1}^{\theta_2} \times \int_{\pi-3\pi M\sin y}^{-\pi+3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_2}^{\theta_3} \times \int_{2\pi-3\pi M\sin y}^{-2\pi+3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_3}^{\theta_4} \times \int_{\pi-3\pi M\sin y}^{-\pi+3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy + \int_{\theta_4}^{\pi} \times \int_{-3\pi M\sin y}^{3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\pi}^{\theta_5} \times \int_{\pi+3\pi M\sin y}^{\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_5}^{\theta_6} \times \int_{2\pi+3\pi M\sin y}^{-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_6}^{\theta_7} \times \int_{3\pi+3\pi M\sin y}^{-\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_7}^{\theta_8} \times \int_{2\pi+3\pi M\sin y}^{-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy - \int_{\theta_8}^{2\pi} \times \int_{\pi+3\pi M\sin y}^{\pi-3\pi M\sin y} e^{j(mx+ny)}\,dx\,dy\right]. \tag{19}$$

The expansion formula of the Jacobi angle series is [19]

$$\sin(\xi\sin y) = 2\sum_{k=1,\text{odd}}^{\infty}\left[J_k(\xi)\sin(ky)\right]. \tag{20}$$

Setting $\xi = 3mM\pi$, the Fourier series of the output voltage of the conventional strategy yields

$$u_{\text{out}} = M\sin(\omega_s t) + \frac{2}{3\pi^2}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty}^{\infty} \times [B_{mn}\sin(m\omega_c t + n\omega_s t)] \tag{21}$$

$$\begin{aligned} B_{mn} =& J_n(3mM\pi)\left[1-(-1)^n\right] \\ &\times\left\{\sum_{k=1}^{3}\left\{\cos\left[m(k-1)\pi\right](\theta_{k+1}-\theta_k)\right\}\right\} \\ &-\sum_{h\neq -n,\text{odd}}^{\infty}\left\{J_h(3mM\pi)\frac{\left[1+(-1)^{n+h}\right]}{n+h}\right. \\ &\times\sum_{k=1}^{3}\left\{\cos\left[m(k-1)\pi\right]\right. \\ &\times\left\{\sin\left[(n+h)\theta_{k+1}\right]\right. \\ &\left.\left.\left.-\sin\left[(n+h)\theta_k\right]\right\}\right\}\right\}. \end{aligned} \tag{22}$$

The Fourier series of the output voltage of the proposed strategy is

$$\begin{aligned} u_{\text{out}} =& M\sin(\omega_s t) + \frac{2}{3\pi^2}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty}^{\infty} \\ &\times[A_{mn1}\cos(m\omega_c t+n\omega_s t)+B_{mn1}\sin(m\omega_c t+n\omega_s t)] \end{aligned} \tag{23}$$

$$\begin{aligned} A_{mn1} =& \left[1-(-1)^m\right]\left[1+(-1)^n\right] \\ &\times\sum_{h\neq -n,\text{odd}}^{\infty}\left\{J_h(3mM\pi)\frac{1}{n+h}\right. \\ &\times\sum_{k=1}^{3}\left\{\cos\left[m(k-1)\pi\right]\right. \\ &\times\left\{\cos\left[(n+h)\theta_{k+1}\right]\right. \\ &\left.\left.\left.-\cos\left[(n+h)\theta_k\right]\right\}\right\}\right\} \end{aligned} \tag{24}$$

$$\begin{aligned} B_{mn1} =& \left[1+(-1)^m\right]\left[1-(-1)^n\right] \\ &\times\left\{J_n(3mM\pi)\sum_{k=1}^{3}\left\{\cos\left[m(k-1)\pi\right](\theta_{k+1}-\theta_k)\right\}\right. \\ &-\sum_{h\neq -n,\text{odd}}^{\infty}\left\{J_h(3mM\pi)\frac{1}{n+h}\right. \\ &\times\sum_{k=1}^{3}\left\{\cos\left[m(k-1)\pi\right]\right. \\ &\times\left\{\sin\left[(n+h)\theta_{k+1}\right]\right. \\ &\left.\left.\left.\left.-\sin\left[(n+h)\theta_k\right]\right\}\right\}\right\}\right\}. \end{aligned} \tag{25}$$

It can be known from (21)–(25) that the spectral characters of the two strategies are different. There exist no harmonics at the carrier frequency and its multiples in the conventional one. No sideband harmonics exist when m and n are both odd or are both even synchronously in the proposed one.

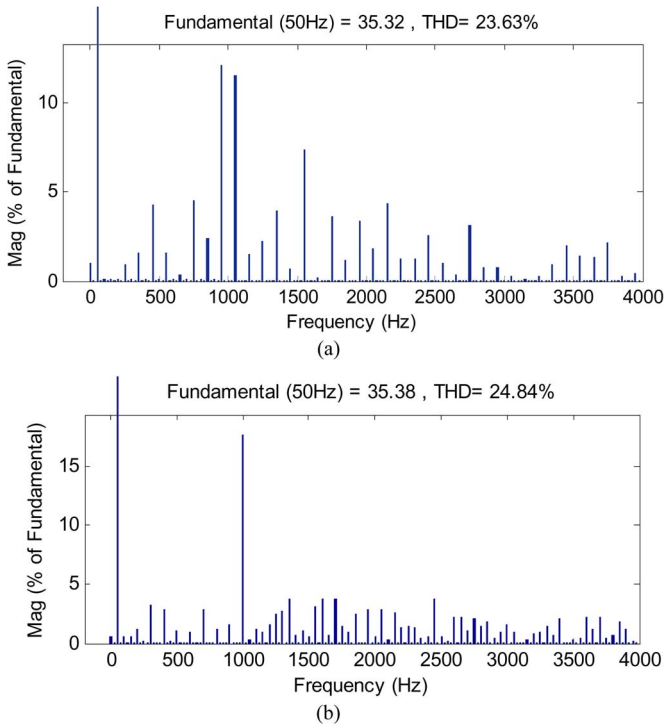

Fig. 9. Fast Fourier transforms of output voltages with $M = 0.8$ and $p = 20$. (a) Conventional. (b) Proposed.

Since the differences of the spectral characters of the two strategies are not distinct from the theoretical results, the total harmonic distortions (THDs) of the two strategies are compared in the simulation. First, the spectrum with lower frequency ratio ($p = 20$) and $M = 0.8$ is simulated, and the results are shown in Fig. 9. The distributions of the spectrum of the two strategies are different, but the THDs are almost the same.

Furthermore, the THDs, the fundamental amplitudes of the output voltage U_{out}, and their differences with different amplitude modulation ratios and frequency ratios (even ratio and odd ratio) of the two strategies are simulated and shown in Fig. 10. ΔU_{out} denotes the differences of the fundamental amplitudes of the output voltages, and ΔTHD denotes the differences of the THDs of the output voltages.

Fig. 10(a) shows the curves with different Ms and the odd frequency ratio $p=199$. It is shown that, when the frequency ratio is odd, the distribution curves of the THD and the foundational amplitude of the output voltage are alike. The difference of the THDs of the two strategies reaches its maximum (0.05%) when $M=0.5$. The difference of the amplitudes of the two strategies is very small during the overall range of M. Fig. 10(b) shows the curves corresponding to M with even frequency ratio ($p=200$). It is shown that, when the frequency ratio is even, the distribution curves of the THD and the foundational amplitude of the output voltage are also alike. The difference of the THDs of the two strategies reaches its maximum (0.1%) when $M=0.3$.

The difference of the amplitudes of the two strategies is very small during the overall range of M. Fig. 10(c) shows the curves with different odd frequency ratios and $M = 0.8$. It is shown that, when the frequency ratio is very small (less than 29), there is a bit difference in the changing trend of the

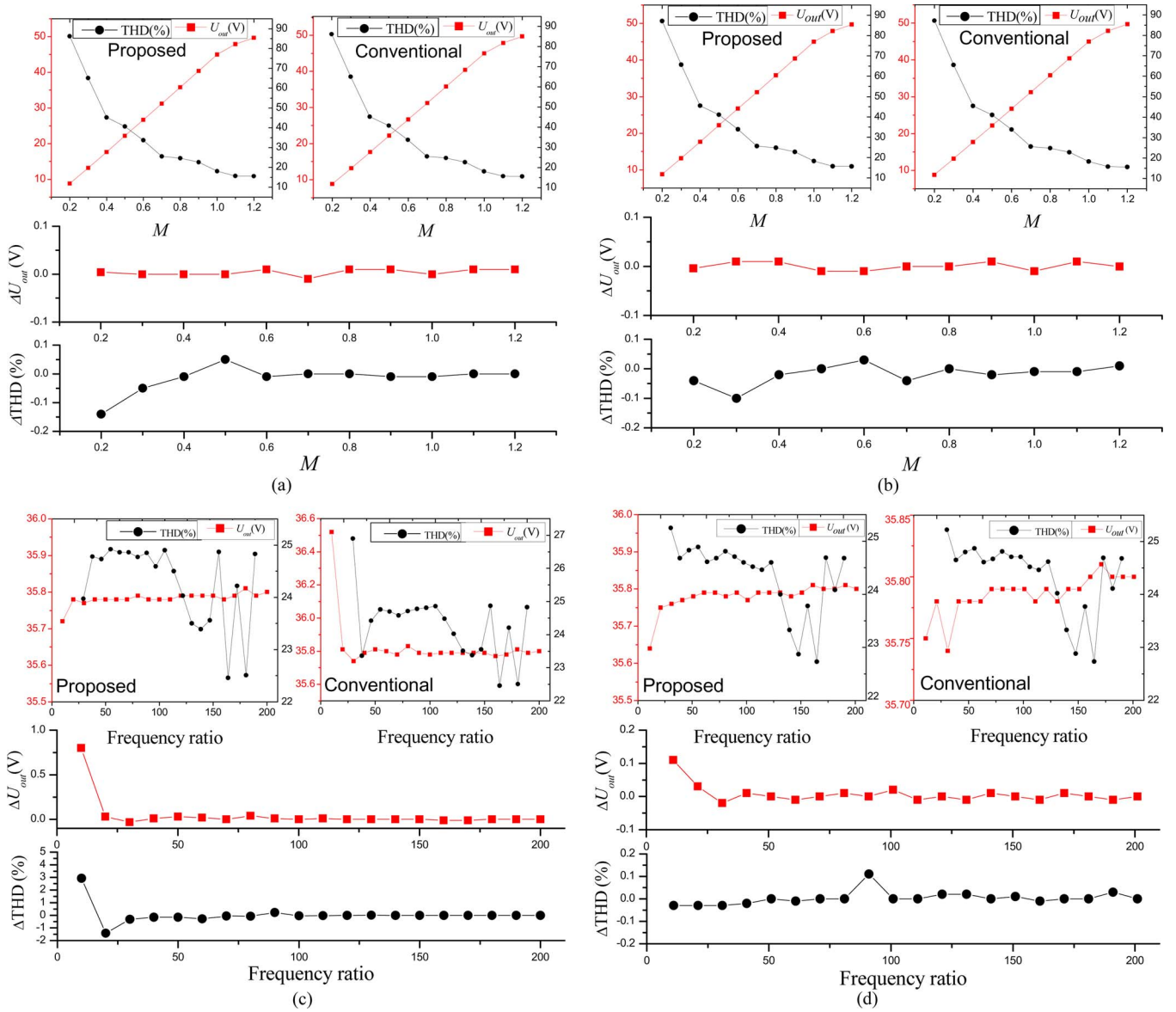

Fig. 10. Distribution curves of the conventional and proposed strategies. (a) Different Ms with $p = 199$. (b) Different Ms with $p = 200$. (c) Different odd frequency ratios with $M = 0.8$. (d) Different even frequency ratios with $M = 0.8$.

curves, and the maximums are 3% and 0.8, respectively. When the frequency ratio gradually increases, the difference of the two curves becomes smaller and smaller.

Fig. 10(d) shows the curves with different even frequency ratios and $M = 0.8$. It is shown that, within the overall range of the frequency ratio, the two THD curves are very close. Just at the point of $p = 90$, the difference reaches its maximum (0.15%). The shapes of the two amplitude curves are somewhat different. The maximum arises at the point of $p = 10$, which is equal to 0.1.

When the frequency ratio is higher, the differences of THDs of the two strategies have been already very tiny and almost can be ignored. Therefore, in the actual system, the performance of the proposed strategy is as good as the conventional one; it means that the proposed strategy can entirely replace the conventional one. The complexity of the system is reduced, and the reliability, as well as the capacity, of resisting disturbance is enhanced.

V. Conclusion

The proposed SCMM-SPWM strategy suitable for controlling the single-phase seven-level asymmetrical diode-clamped inverter has been implemented with only one DSP chip without any other attached logical circuit or controller. The elimination of zero-crossing disturbance in the former asymmetrical inverter is proposed as well. The experimental results verify its accuracy and feasibility. The theoretical and simulated comparison results of the spectral characters between the proposed and the conventional one indicate that the SCMM-SPWM has the similar performance with the conventional one. The proposed strategy can entirely replace the conventional one to drive multilevel inverter. Just because the attached logical circuit or controller is not necessary in the proposed strategy, the implementation platform is simplified, the cost and bulk is reduced, and the reliability is enhanced.

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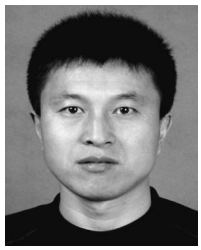

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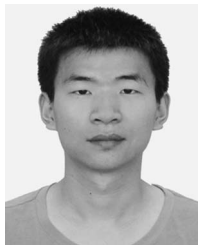

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