Optimum Structures of Proposed New Cascaded Multilevel Inverter with Reduced Number of Components

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***Abstract*— In this paper, a new cascaded multilevel inverter is proposed. For the proposed inverter, two different algorithms to determine the magnitude of dc voltage sources are proposed. Then, in order to generate maximum numbers of output voltage levels by using constant number of power switches and or dc voltage sources, several optimum structures of the proposed inverter are obtained. In comparison with the conventional cascaded multilevel inverters, the proposed inverter is able to generate high number of output voltage levels by using lower number of power electronic devices such as power switches, driver circuits, power diodes and dc voltage sources. In addition, the low amount of blocked voltage by switches is another advantage of the proposed inverter. The accuracy performance of the proposed inverter in generation the positive and negative voltage levels is verified through the experimental results on a 61- level inverter.**

***Keywords*— Cascaded multilevel inverter; H-bridge cascaded inverter; power electronic devices; optimum topologies.**

I. INTRODUCTION

There are different problems in using power semiconductor devices independently in high voltage and high power applications such as limitation in current generation, impossibility of connection to grid directly etc. [1]. Therefore, multilevel inverters have been presented as a suitable selection in these kinds of applications. Recently, in order to generate higher quality output waveforms, reduce the number of required power electronic devices, cost and installation space of the inverter many researches on new control methods and topologies of the multilevel inverters have been done [2]. From different types multilevel inverters, the cascaded multilevel inverter has been received more attentions and are concentrated in this paper. The modularization feature of this inverter is remarkable while the magnitudes of its dc voltage sources in different basic units are equal. This inverter is called symmetric cascaded multilevel inverter and consists of redundant switching states in generation output voltage levels. In [3-7], several symmetric cascaded multilevel inverters have been presented. One of the main disadvantages of these inverters is the high number of required power semiconductor devices such as dc voltage sources, power diodes and insulated gate bipolar transistors (IGBTs) to increase the number of output levels. This feature leads to decrease reliability and increase complexity of control, installation space and total cost of the inverter. By using dc voltage sources with different magnitudes, the asymmetric cascaded multilevel inverter is obtained that increase the number of output voltage levels [8]. Different asymmetric cascaded multilevel inverters have been presented in [9-13]. The used power switches in these topologies are either bidirectional switches or unidirectional ones from voltage points of view. The unidirectional switches conduct current in both directions while block voltage in one polarity. However, the bidirectional ones conduct current in both directions and block voltage with positive and negative polarities. Each bidirectional power switch consists of two numbers of power diodes and IGBTs and a driver circuit if the common emitter structure is used. The main aim of presenting different asymmetric cascaded inverters is increasing the number of output voltage levels by using low number of required semiconductor devices. The main disadvantage of the asymmetric cascaded multilevel inverter is its different value of dc voltage sources.

In this paper, a new cascaded multilevel inverter is proposed. Two different algorithms to generate the positive and negative voltage levels at the output are proposed. In the proposed inverter, by using its algorithms, the number of required power electronic devices such as power switches, power diodes, dc voltage sources and the amount of blocked voltage by power switches are lower than conventional topologies. These advantages are obtained by comparing the proposed cascaded topology with conventional cascaded multilevel inverters from the number of required components points of view. Then, several optimum structures of the proposed inverter based on different aims are obtained. Finally, the experimental results on a 61-level inverter verify all of the theoretically obtained results.

II. PROPOSED TOPOLOGY

Fig. 1 shows the presented basic unit. As shown in this figure, the basic unit consists of $2m$ dc voltage sources and several unidirectional power switches from voltage point of view. Each unidirectional power switch consists of an IGBT with an anti-parallel power diode and a driver circuit. Therefore, in the basic unit, the number of switches (N_{switch}) is equal to the number of power diodes (N_{diode}), IGBTs (N_{IGBT}) and driver circuits (N_{drive}) and is obtained as follows:

$$N_{switch} = N_{diode} = N_{IGBT} = N_{drive} = 4m + 2 \quad (1)$$

where m is the number of the dc voltage sources on each leg. In the basic unit, the power switches of ($S_{L,1}$, $S_{L,2}$), ($S_{L,3}$, $S_{L,4}$), ($S_{R,1}$, $S_{R,2}$), ($S_{R,3}$, $S_{R,4}$), …, ($S_{L,2m-1}$, $S_{L,2m}$) and ($S_{R,2m-1}$, $S_{R,2m}$) should not be turned on simultaneously because of avoiding a short circuit across the dc voltage sources of $V_{L,1}$, $V_{L,2}$, $V_{R,1}$, $V_{R,2}$, …, $V_{L,m}$ and $V_{R,m}$,

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respectively. In addition, S_a and S_b should not be turned on, simultaneously. Table I shows the output voltage of the basic unit for different switching states. As it is obvious from Table I, this unit is able to generate all positive and negative levels at the output.

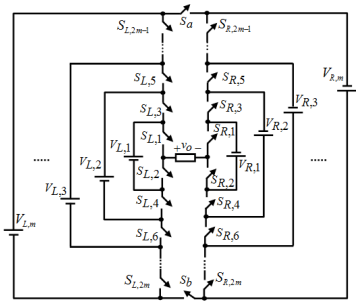


Fig. 1. The topology of basic unit.

TABLE I.
OUTPUT VOLTAGES OF THE BASIC UNIT

v_o	Turned on Switches
$V_{L,1}$	$S_{L,1}$, $S_{L,4}-S_{L,2m}$, $S_{R,2}-S_{R,2m}$, S_b
$V_{R,1}$	$S_{L,2}-S_{L,2m}$, $S_{R,4}-S_{R,2m}$, $S_{R,1}$, S_b
$V_{L,1}+V_{R,1}$	$S_{L,1}$, $S_{R,1}$, $S_{L,4}-S_{L,2m}$, $S_{R,4}-S_{R,2m}$, S_b
$V_{L,2}+V_{R,2}-V_{L,1}$	$S_{L,2}$, $S_{L,3}$, $S_{L,6}-S_{L,2m}$, $S_{R,1}$, $S_{R,3}$, $S_{R,6}-S_{R,2m}$, S_b
⋮	⋮
$V_{L,m}+V_{R,m}$	$S_{L,1}-S_{L,2m-1}$, $S_{R,1}-S_{R,2m-1}$, S_b
0	$S_{L,1}-S_{L,2m-1}$, $S_{R,1}-S_{R,2m-1}$, S_a
$-(V_{L,m}+V_{R,m})$	$S_{L,2}-S_{L,2m}$, $S_{R,2}-S_{R,2m}$, S_a
⋮	⋮
$-(V_{L,1}+V_{R,1})$	$S_{L,2}$, $S_{R,2}$, $S_{L,3}-S_{L,2m-1}$, $S_{R,3}-S_{R,2m-1}$, S_a
$-(V_{R,1})$	$S_{L,1}-S_{L,2m-1}$, $S_{R,2}$, $S_{R,3}-S_{R,2m-1}$, S_a
$-(V_{L,1})$	$S_{L,2}$, $S_{L,3}-S_{L,2m-1}$, $S_{R,1}-S_{R,2m-1}$, S_a

One of the most important parameters to determine the cost of a multilevel inverter is the value of blocked voltage by the switches [14]. By increasing the value of blocked voltage, the cost of the inverter increases. Therefore, it is necessary to calculate the amount of blocked voltage by switches in the basic unit. This parameter is calculated as follows:

$$V_{S_{R,1}} = V_{S_{R,2}} = V_{R,1} \tag{2}$$

$$V_{S_{R,3}} = V_{S_{R,4}} = V_{R,2} - V_{R,1} \tag{3}$$

$$V_{S_{L,1}} = V_{S_{L,2}} = V_{L,1} \tag{4}$$

$$V_{S_{L,3}} = V_{S_{L,4}} = V_{L,2} - V_{L,1} \tag{5}$$

$$\vdots$$

$$V_{S_{R,2m-1}} = V_{S_{R,2m}} = V_{R,m} - V_{R,m-1} \tag{6}$$

$$V_{S_{L,2m-1}} = V_{S_{L,2m}} = V_{L,m} - V_{L,m-1} \tag{7}$$

$$V_{S_a} = V_{S_b} = V_{R,m} + V_{L,m} \tag{8}$$

where, $V_{SL,1}$, $V_{SL,2}$, $V_{SR,1}$, $V_{SR,2}$, …, $V_{SL,2m}$ and $V_{SR,2m}$ are the maximum amount of blocked voltage by switches $S_{L,1}$, $S_{L,2}$, $S_{R,1}$, $S_{R,2}$, …, $S_{L,2m}$ and $S_{R,2m}$, respectively. The maximum amount of blocked voltage by all switches of the basic unit (V_{block}) is equal to:

$$V_{block} = (\sum_{j=1}^{m} V_{S_{R,j}} + V_{S_{L,j}}) + V_{S_a} + V_{S_b} = 4(V_{R,m} + V_{L,m}) \tag{9}$$

In order to increase the number of output voltage levels, it is possible to connect n number of the proposed basic units to generate a new cascaded multilevel inverter. Fig. 2 shows the proposed cascaded multilevel inverter. In the proposed cascaded multilevel inverter, the number of used dc voltage sources in the first, second, … and n^{th} basic unit is generally equal to $2m_1$, $2m_2$, … and $2m_n$, respectively. In other word, $2m_1$ dc voltage sources are used in the first unit, $2m_2$ dc voltage sources are used in second unit and …, $2m_n$ dc voltage sources are used in n^{th} unit. In order to increase the number of output voltage levels by using a constant number of power electronic devices, the number of dc voltage sources in each unit have to be considered equally. It means that $m_1 = m_2 = m_3 = \cdots = m_n = m$.

In the proposed cascaded topology, the number of power switches, IGBTs, driver circuits and dc voltage sources (N_{source}) are calculated as follows, respectively:

$$N_{switch} = N_{IGBT} = N_{drive} = n(4m+2) \tag{10}$$

$$N_{source} = 2nm \tag{11}$$

It is important to note that the number of generated output voltage levels in the proposed cascaded multilevel inverter is directly depends on the magnitudes of used dc voltage sources. Therefore, two different algorithms to determine the magnitudes of dc voltage sources are proposed.

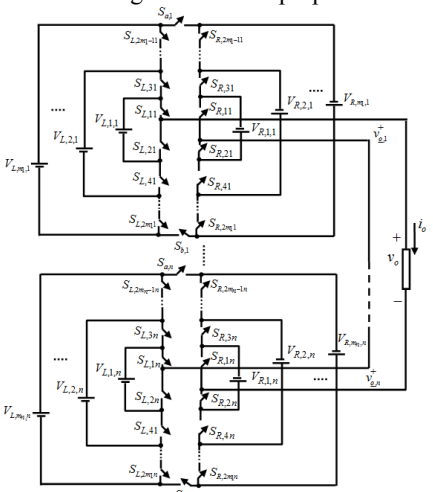


Fig. 2. The proposed cascaded multilevel inverter.

A. First Proposed Algorithm

In the first proposed algorithm, the magnitudes of dc voltage sources of the shown inverter in Fig. 2 are selected as follows:

$$V_{L,j,i} = 5^{j-1}V_{dc} \quad for\ j = 1,2,3,\cdots,m \ \ and \ \ i = 1,2,3,\cdots,n \tag{12}$$

$$V_{R,j,i} = 2\times 5^{j-1}V_{dc} \ for\ j = 1,2,3,\cdots,m \ and \ i = 1,2,3,\cdots,n \tag{13}$$

Considering this proposed algorithm, the number of output voltage levels (N_{level}), maximum magnitude of the output voltage ($V_{o,\max}$) and the amounts of blocked voltage by switches are calculated as follows, respectively:

$$N_{level} = n2^{2m+1} - 2n + 1 \tag{14}$$

$$V_{o,\max} = 3n(5^{m-1})V_{dc} \tag{15}$$

$$V_{block} = 12n(5^{m-1})V_{dc} \tag{16}$$

B. Second Proposed Algorithm

In this sub-section, the magnitudes of the used dc voltage sources in the proposed cascaded multilevel inverter are considered as follows:

First unit:

$$V_{L,j,1} = 5^{j-1} V_{dc} \qquad for \quad j = 1,2,3,\cdots,m \tag{19}$$

$$V_{R,j,1} = 2\times 5^{j-1} V_{dc} \qquad for \quad j = 1,2,3,\cdots,m \tag{20}$$

Second unit:

$$\begin{aligned} V_{L,j,2} &= 5^{j-1}(V_{dc} + V_{L,m,1} + V_{R,m,1}) \\ &= 5^{j-1}(3\times 5^{m-1}+1)\, V_{dc} \qquad for \quad j = 1,2,3,\cdots,m \end{aligned} \tag{21}$$

$$V_{R,j,2} = (2\times 5^{j-1}) V_{L,j,2} \qquad for \quad j = 1,2,3,\cdots,m \tag{22}$$

$\vdots$

n^{th} unit:

$$\begin{aligned} V_{L,j,n} &= 5^{j-1}\left(V_{dc} + \sum_{i=1}^{n-1}(V_{L,m,i} + V_{R,m,i})\right) \\ &= 5^{j-1}(3\times 5^{m-1}+1)^{n-1} V_{dc} \qquad for \quad j = 1,2,3,\cdots,m \end{aligned} \tag{23}$$

$$V_{R,j,n} = (2\times 5^{j-1}) V_{L,j,n} \qquad for \quad j = 1,2,3,\cdots,m \tag{24}$$

In this condition, the number and maximum magnitude of output voltage levels and the amount of blocked voltage by switches are written as follows:

$$N_{level} = 2\times(3\times 5^{m-1}+1)^n - 1 \tag{25}$$

$$V_{o,\max} = \left[(3\times 5^{m-1}+1)^n - 1\right] V_{dc} \tag{26}$$

$$V_{block} = 4\times\left[(3\times 5^{m-1}+1)^n - 1\right] V_{dc} \tag{27}$$

III. COMPARING THE PROPOSED TOPOLOGY WITH THE CONVENTIONAL CASCADED MULTILEVEL INVERTERS

The main aim of presentation the proposed cascaded multilevel inverter is increasing the number of output voltage levels by using lower number of power electronic devices. In order to investigate the feature the proposed cascaded multilevel inverter is compared with the conventional cascaded inverters from the amount of blocked voltage by switches, the number of required power switches, IGBTs and dc voltage sources points of view. In these comparisons, the proposed topology based on its two algorithms is considered. These algorithms are shown by P_1 and P_2 for the first and second proposed algorithms, respectively. The H-bridge cascaded multilevel inverter with five different algorithms as symmetric and asymmetric cascaded inverters are considered. These inverters have been presented in [3] and [9-11]. This topology with its presented algorithms are considered by R_1 to R_5, respectively. These algorithms are equal to:

$$R_1 \text{ for } V_1 = V_2 = \cdots = V_n = V_{dc} \tag{28}$$

$$R_2 \text{ for } V_1 = 2^{j-1} V_{dc} \qquad for \quad j = 1,2,\cdots,n \tag{29}$$

$$R_3 \text{ for } V_1 = 3^{j-1} V_{dc} \qquad for \quad j = 1,2,\cdots,n \tag{30}$$

$$R_4 \text{ for } V_1 = 0.5V_2 = 0.5V_3 = \cdots = 0.5V_n = V_{dc} \tag{31}$$

$$R_5 \text{ for } V_1 = V_2/3 = V_3/3 = \cdots = V_n/3 = V_{dc} \tag{32}$$

In [4-7], four other symmetric cascaded multilevel inverters have been presented. These are shown by R_6 to R_9, respectively. The related algorithms to these topologies are equal to:

$$R_6 \text{ to } R_9 \text{ for } V_1 = V_2 = \cdots = V_n = V_{dc} \tag{33}$$

In [12], two other asymmetric cascaded topologies have been presented which are considered by R_{10} to R_{11} in this comparison, respectively. The algorithms of these topologies are written as follows:

R_{10} for:

$$V_{1,n} = V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m_i} V_{j,i} = \prod_{i=1}^{n-1}(2^{m_i+1}-1)\, V_{dc} \tag{34}$$

$$V_{j,n} = 2^{j-1} V_{1,n} \qquad for \quad j = 2,3,\cdots,m \tag{35}$$

$$R_{11} \text{ for } V_n = (2m+1)^{n-1} V_{dc} \tag{36}$$

In addition, another asymmetric cascaded multilevel inverter with three different algorithms has been presented in [13]. In this comparison, these are indicated by R_{12} to R_{14}, respectively. These algorithms are equal to:

$$R_{12} \text{ for } V_{n,j} = V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m} V_{i,j} = (2m+1)^{n-1} \tag{37}$$

R_{13} for:

$$V_{n,1} = V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m} V_{i,j} = (4m-1)^{n-1}\, V_{dc} \tag{38}$$

$$V_{n,2} = 2\, V_{n,1} = 2\times(4m-1)^{n-1}\, V_{dc} \tag{39}$$

R_{14} for:

$$V_{n,j} = \left(V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m} V_{j,i}\right)^{n-1} \times 2^{j-1} = \left[2^{m+1}-1\right]^{n-1} \times 2^{j-1} \tag{40}$$

Fig. 3(a) shows the comparison of the proposed cascaded multilevel inverter based on its proposed algorithms with above-mentioned inverters from the number of required switches point of view. As it is obvious from this figure, the proposed topology requires less number of power switches than other topologies. This feature is remarkable when its first proposed algorithm is used. Fig. 3(a) also indicates the comparison of the number of used driver circuits. It is also clear that the proposed topology needs lower number of driver circuit than other presented topologies.

As mentioned before, the bidirectional and unidirectional switches are used in the cascaded multilevel inverters. Therefore, it is necessary to compare the number of used IGBTs in the proposed cascaded inverter with other presented inverters in literature. Fig. 3(b) indicates this comparison. As it is obvious from this figure, the number of used IGBTs in the proposed topology is lower than other presented topology especially while its first proposed algorithm is used. As mentioned before, the number of IGBTs is as same as the number of power diodes. Therefore, this figure also shows the comparison of the used power diodes in the proposed inverter and other above-mentioned cascaded inverters. Therefore, the number of required power diodes in the proposed inverter is lower than other conventional cascaded inverters. This feature is another advantage of the proposed cascaded inverter.

Fig. 3(c) compares the number of required dc voltage sources. As it can be seen, the proposed cascaded multilevel inverter based on its first proposed algorithm needs lower number of dc voltage sources than other presented inverters.

Fig. 3(d) compares the value of the blocked voltage by switches. As Fig. 3(d) shows, the proposed inverter generates lower amount of blocked voltage by switches especially when the second proposed algorithms is used. It is pointed out that all values are considered in per unit.

Therefore, it is clear that the proposed cascaded multilevel inverter generates higher number of output levels by using

lower number of power electronic devices than other considered cascaded inverter in this comparison. These features will be remarkable when the first proposed algorithm is used.

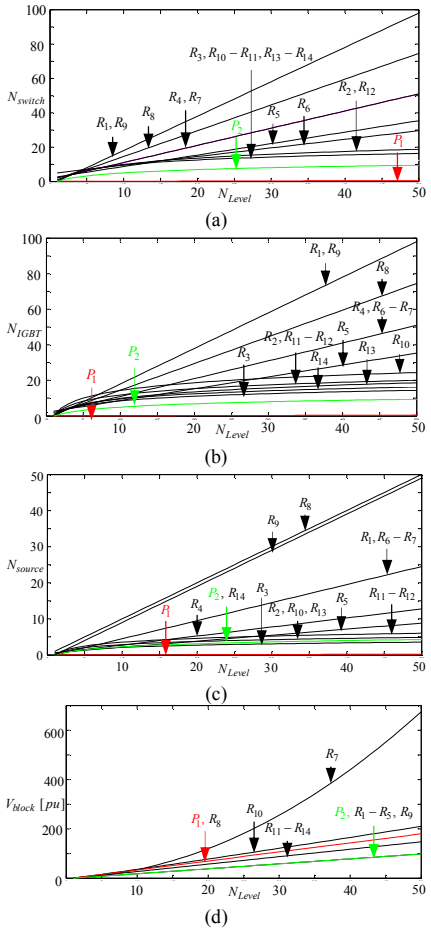


Fig. 3. Comparison of the proposed cascaded multilevel inverter with conventional cascaded inverters; (a) Variation of N_{switch} versus N_{level}; (b) Variation of N_{IGBT} versus N_{level}; (c) Variation of N_{Source} versus N_{level}; (d) Variation of V_{block} versus N_{level}.

IV. OPTIMUM STRUCTURES

It is important to note that the proposed cascaded multilevel inverter can be arranged by different arrays of power switches and dc voltage source to generate different output voltage levels as shown in Fig. 2. Therefore, it is possible to determine the number of series connected basic units and required power electronic devices in each unit to obtain an optimum topology for the specific aims. The obtained optimum topologies lead to reduce the total cost, weight and installation space of the inverter. In the following, the optimum topologies of the proposed inverter will be investigated. In addition, it is assumed that the shown proposed cascaded inverter in Fig. 2 is comprised of n numbers of series connected basic units with m numbers of dc voltage sources in each leg of per basic unit.

A. Optimum Topology for Maximum Number of output Levels Based on Constant Number of Switches

The main aim of the proposed cascaded multilevel inverter is generating maximum numbers of output voltage levels by using constant number of power switches. In this sub-section, the number of power switches is considered constant. The question is that for the shown cascaded multilevel inverter in Fig. 2, which topology can generate maximum number of output voltage levels?

The equation (10) shows the relation between the number of power switches with the number of used proposed basic units and dc voltage sources in each unit. Based on (10), the number of required basic units (n) is obtained as follows:

$$n=\frac{N_{switch}}{(4m+2)} \tag{41}$$

As mentioned before, the maximum output voltage levels for the first and second proposed algorithms are given by (14) and (25), respectively. Therefore, by replacing (41) into (14) and (25) these equations will be rewritten as follows:

$$N_{level,1}=N_{switch}\left(\frac{2^{2m}-1}{2m+1}\right)+1 \tag{42}$$

$$N_{level,2}=2\times\left[(3\times5^{m-1}+1)^{\frac{1}{4m+2}}\right]^{N_{switch}}-1 \tag{43}$$

In (42) and (43), it is necessary to determine the value of m. As the number of switches are considered constant, in order to maximize the equations of (42) and (43), it is enough to be maximum the equations of $\frac{2^{2m}-1}{2m+1}$ and $(3\times5^{m-1}+1)^{\frac{1}{4m+2}}$, respectively. Figs. 4(a) and 4(b) show the variation of $\frac{2^{2m}-1}{2m+1}$ and $(3\times5^{m-1}+1)^{\frac{1}{4m+2}}$ versus m. It is necessary to point out that the number of used elements in each unit is an integer number, so if the calculated number is not an integer number, the nearest integer number is certainly proposed answer. As it is obvious, the maximum number of output levels is obtained by $m=\infty$ for the first and second proposed algorithms. This means that to receive the maximum number of output levels, a basic unit ($n=1$) with its power switches is desired (Fig. 1). In this condition, the number of power switches, IGBTs, driver circuits and dc voltage sources are calculated by equations of (10) and (11). In addition, the number and the maximum magnitude of output voltage levels and the amount of blocked voltage by switches based on the first and second proposed algorithms are considered by (14) to (16) and (25) to (27), respectively.

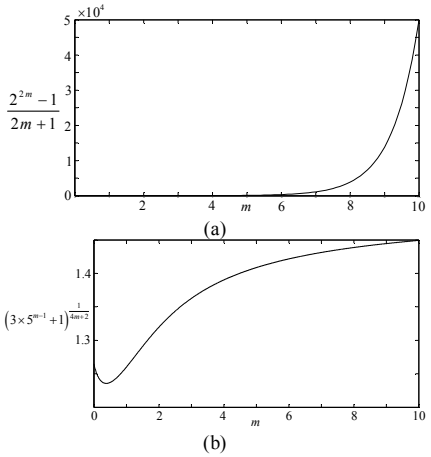


Fig. 4. (a) Variation of $\frac{2^{2m}-1}{2m+1}$ versus m; (b) Variation of $(3\times5^{m-1}+1)^{\frac{1}{4m+2}}$ versus m.

B. Optimum Topology for Maximum Number of output Levels with Constant Number of dc Voltage sources

It is assumed that the number of dc voltage sources is constant. The question is that in this condition, which topology generates maximum number of output voltage levels?

The relation between the number of dc voltage sources with the number of used basic unit and dc voltage sources in each unit are given by (11). Based on (11) it is resulted that:

$$n = \frac{N_{source}}{2m} \tag{44}$$

In addition, the maximum number of output voltage levels for the first and second proposed algorithms are also given by (14) and (25), respectively. Therefore, by applying (44) into (14) and (25) we have:

$$N_{level,1} = N_{source}\left[\frac{2^{2m}-1}{m}\right]+1 \tag{45}$$

$$N_{level,2} = 2\times\left[(3\times 5^{m-1}+1)^{\frac{1}{2m}}\right]^{N_{source}} - 1 \tag{46}$$

In (45) and (46), it is necessary to determine the value of m. Figs. 5(a) and 5(b) show only the variation of $\frac{2^{2m}-1}{m}$ and $(3\times 5^{m-1}+1)^{\frac{1}{2m}}$ versus m because the number of dc voltage sources is constant. As it is obvious, the maximum number of output levels is obtained by $m=\infty$ for the first and second proposed algorithms. This means that to receive the maximum number of output levels, a basic unit ($n=1$) with m ($m=\infty$) dc voltage sources is desired (Fig. 1). In this condition, the number of power switches, IGBTs, driver circuits and dc voltage sources are calculated by equations of (10) and (11). In addition, the number of output voltage levels, the maximum magnitude of the output voltage and the amount of blocked voltage by switches for the first and second proposed algorithm are considered by (14) to (16) and (25) to (27), respectively.

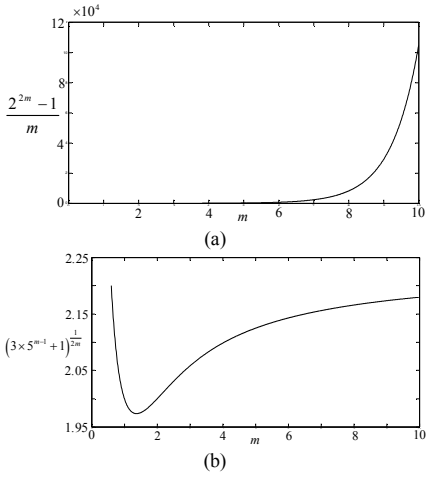


Fig. 5. (a) Variation of $\frac{2^{2m}-1}{m}$ versus m; (b) Variation of $(3\times 5^{m-1}+1)^{\frac{1}{2m}}$ versus m.

C. Optimum Topology for Minimum Number of dc Voltage Sources with Constant Number of Output Voltage Levels

In this sub-section, it is required to know that which topology of the proposed inverter generates specific output voltage levels while the minimum dc voltage sources is used. The numbers of output voltage levels for n numbers of series connected basic units based on the first and second proposed algorithms are obtained by using (14) and (25), respectively. Therefore:

$$n = \frac{N_{level,1}-1}{2^{2m+1}-2} \tag{47}$$

$$n = \frac{\ln\left(\frac{N_{level,2}+1}{2}\right)}{\ln(3\times 5^{m-1}+1)} \tag{48}$$

In (47) and (48), it is necessary to determine the value of m. The relation between the number of dc voltage sources with the number of used basic unit and dc voltage sources in each unit are given by (11). Therefore, by applying (47) and (48) into (11) for the first and second algorithms, respectively, we have:

$$N_{source} = m\times\frac{N_{level,1}-1}{2^{2m}-1} \tag{49}$$

$$N_{source} = 2m\times\frac{\ln\left(\frac{N_{level,2}+1}{2}\right)}{\ln(3\times 5^{m-1}+1)} \tag{50}$$

According to (49) and (50), by reducing the value of $\frac{m}{2^{2m}-1}$ in the first proposed algorithm and $\frac{2m}{\ln(3\times 5^{m-1}+1)}$ in the second proposed algorithm, the number of dc voltage sources will reduce while the number of output levels is constant. Figs. 6(a) and 6(b) show the variation of $\frac{m}{2^{2m}-1}$ and $\frac{2m}{\ln(3\times 5^{m-1}+1)}$ versus m. As it is obvious from these figures, the minimum number of dc voltage source is obtained by $m=5$ for the first proposed algorithm and by $m=\infty$ for the second algorithm.

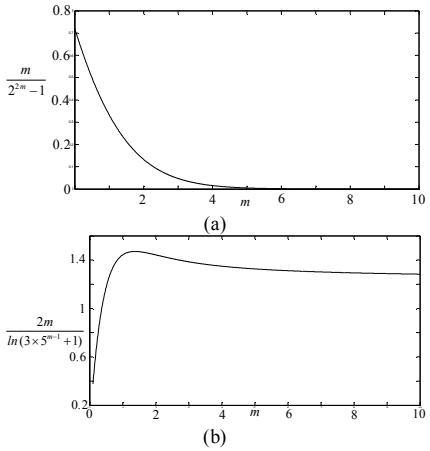


Fig. 6. (a) Variation of $\frac{m}{2^{2m}-1}$ versus m; (b) Variation of $\frac{2m}{\ln(3\times 5^{m-1}+1)}$ versus m.

Therefore, the number of power switches, IGBTs, driver circuits, dc voltage sources and output voltage levels, the maximum producible output voltage and the amount of blocked voltage by power switches for the optimized topology

based on the first proposed algorithm are written as follows, respectively:

$$N_{switch} = N_{IGBT} = N_{drive} = 22n \quad (51)$$

$$N_{source} = 10n \quad (52)$$

$$N_{level} = 2046n + 1 \quad (53)$$

$$V_{o,\max} = 1875nV_{dc} \quad (54)$$

$$V_{block} = 7500nV_{dc} \quad (55)$$

The number of power switches, IGBTs, driver circuits, dc voltage sources and output voltage levels, the maximum producible output voltage and the amount of blocked voltage by power switches for the optimized topology based on the second proposed algorithm are written by equations (10) and (25) to (27), respectively:

D. Optimum Topology for Minimum Number of Power Switches with Constant Number of Output Voltage Levels

In this sub-section, the main question is that if the numbers of output voltage levels be constant, which topology of the proposed inverter requires minimum number of power switches? The relation between the number of output voltage levels and the number of series connected basic units for the first and second proposed algorithms are calculated as (47) and (48), respectively. As mentioned before, the equation (10) shows the relation between the number of power switches with the number of used proposed basic units and dc voltage sources in each unit. By replacing (47) and (48) into (10), the numbers of required power switches in the first and second proposed algorithm are recalculated as follows, respectively:

$$N_{switch} = (N_{level,1} - 1)\left(\frac{2m+1}{2^{2m}-1}\right) \quad (56)$$

$$N_{switch} = \ln\left(\frac{N_{Level,2}+1}{2}\right) \times \left[\frac{4m+2}{\ln(3\times 5^{m-1}+1)}\right] \quad (57)$$

Figs. 7(a) and 7(b) show only the variation of $\frac{2m+1}{2^{2m}-1}$ and $\frac{4m+2}{\ln(3\times 5^{m-1}+1)}$ versus m by considering constant value of output levels. As it is obvious from these figures, the minimum number of dc voltage source is obtained by $m=4$ for the first proposed algorithm and $m=\infty$ (Fig. 1) for the second algorithm.

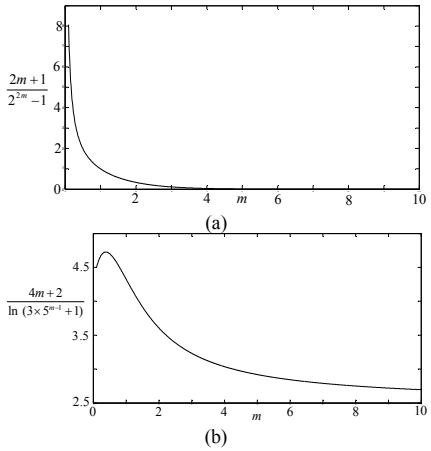


Fig. 7. (a) Variation of $\frac{2m+1}{2^{2m}-1}$ versus m ; (b) Variation of $\frac{4m+2}{\ln(3\times 5^{m-1}+1)}$ versus m.

In this condition, the number of power switches, IGBTs, driver circuits, dc voltage sources and output voltage levels, the maximum output voltage and the amount of blocked voltage by power switches for the optimized topology based on the first proposed algorithm are calculated as follows, respectively:

$$N_{switch} = N_{IGBT} = N_{drive} = 18n \quad (58)$$

$$N_{source} = 8n \quad (59)$$

$$N_{level} = 510n + 1 \quad (60)$$

$$V_{o,\max} = 375nV_{dc} \quad (61)$$

$$V_{block} = 1500nV_{dc} \quad (62)$$

Moreover, for the proposed optimum topology based on the second algorithm a basic unit ($n=1$) is desired and the numbers of power switches, IGBTs, driver circuits and dc voltage sources have been calculated by equations (10) and (11). In addition, the number of output voltage levels, the maximum magnitude of the output voltage and the amounts of blocking voltage are considered by (14) to (16).

E. Optimum Topology for Minimum Value of Blocked Voltage by Switches with Constant Number of Output Voltage Levels

The current and voltage ratings of the switches have most significant role to determine the cost of the multilevel inverters. In different topologies of the proposed inverter, the current of all switches are as same as the load current because of series connected of basic units. This feature is incorrect from voltage point of view. In other word, the voltages of different units are not equal to each other. So, the total amount of blocked voltage by switches could be considered as a significant index in comparison of different topologies. The minimum amount of blocked voltage by switches is considered as one of the most important advantages of the multilevel inverter. If the number of output voltage levels is constant, which topology generates the minimum amount of blocked voltage? As mentioned before, the relation between the number of output voltage levels and the number of series connected basic units for the first and second proposed algorithms are calculated as (47) and (48), respectively. In addition, the relation between the amount of blocked voltage with the number of used proposed basic unit and dc voltage sources for these algorithms are calculated by equations (16) and (27), respectively. By replacing (47) and (48) into (16) and (27), the amount of blocked voltages by switches in the first and second algorithms is recalculated as follows:

$$V_{block} = 4\times(N_{level,1} - 1)\left(\frac{5^{m-1}}{2^{2m}-1}\right)V_{dc} \quad (63)$$

$$V_{block} = 4\times\left[\left[(3\times 5^{m-1})+1\right]^{\left(\frac{1}{\ln(3\times 5^{m-1}+1)}\right)}\right]^{\ln\left(\frac{N_{level,2}+1}{2}\right)} - 1\Bigg]V_{dc} \quad (64)$$

According to (64), Fig. 8 shows only the variation of $\frac{5^{m-1}}{2^{2m}-1}$ versus m by considering the constant value of output levels. As it is obvious from this figure, the minimum amount of blocked voltage by power switches is obtained by $m=1$ for the first proposed algorithm. Considering (64) and based on the constant number of output levels, by decreasing the amount of $\left[(3\times 5^{m-1})+1\right]^{\left(\frac{1}{\ln(3\times 5^{m-1}+1)}\right)}$, the value of blocked voltage will be reduced. According to mathematical roles, the

equation of $\left[(3\times5^{m-1})+1\right]^{\left(\frac{1}{\ln(3\times5^{m-1}+1)}\right)}$ has a constant value. This means that, for a constant number of output voltage levels the amount of blocked voltage is independent to the number of dc voltage sources (m) in each unit. The number of power switches, IGBTs, driver circuits, dc voltage sources and output voltage levels, the maximum producible output voltage and the amount of blocked voltage by power switches for the optimized topology based on the first proposed algorithm are calculated as follows, respectively:

$$N_{switch}=N_{IGBT}=N_{drive}=6n \quad (65)$$

$$N_{source}=2n \quad (66)$$

$$N_{Level,2}=2^{2n+1}-1 \quad (67)$$

$$V_{o,\max}=(4^n-1)V_{dc} \quad (68)$$

$$V_{block}=(4^{n+1}-4)V_{dc} \quad (69)$$

The values of these parameters for the optimized topology based on second proposed algorithm are considered by equations of (10), (11) and (16) to (18), respectively.

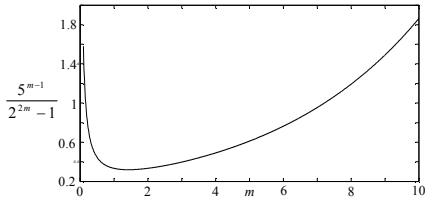
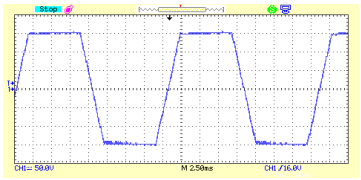


Fig. 8. Variation of $\frac{5^{m-1}}{2^{2m}-1}$ versus m.

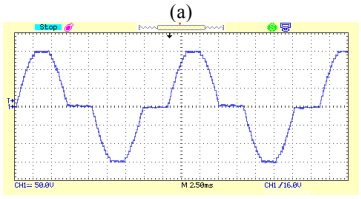
V. EXPERIMENTAL RESULTS

In this section, the ability of the proposed cascaded multilevel inverter in generation a desired output voltage waveform is verified by experimental results on a 61-level cascaded inverter. The 61-level proposed inverter consists of two basic units with two dc voltage sources in each leg of per basic unit. The magnitude of dc voltage sources are selected by using the first proposed algorithm. However, the obtained results for the second proposed algorithms will be as same as the first proposed algorithm. Therefore, the value of the used dc voltage sources in the each unit are considered $V_{L1,1}=V_{L1,2}=10V$, $V_{R1,1}=V_{R1,2}=20V$, $V_{L2,1}=V_{L2,2}=50V$ and $V_{R2,1}=V_{R2,2}=100V$, respectively, if the value of V_{dc} is selected 10V. Based on (14) and (15), this inverter has to be able to generate 61 levels with the maximum amplitude of $300V$ at the output. The required switches in the proposed cascaded multilevel inverter are unidirectional ones. It is important to note that the used IGBTs on the prototype are HGTP10N40C1D (with an internal anti-parallel diode). In addition, the 89C52 microcontroller by ATMEL Company has been used to generate all switching pattern. In all process of the experimental performance, the load is assumed a $R-L$ with $R=100\Omega$ and $L=55mH$. In all experimental results the time/div of the oscilloscope is considered $2.5ms$.

The experimental output voltage waveforms of the first and second basic units are shown in Fig. 9, respectively. As shown in this figure, the first and second units are able to generate all positive and negative levels with the magnitudes of 0, $\pm10V$, $\pm20V$, $\pm30V$, …, $\pm140V$ and $\pm150V$ at the output.



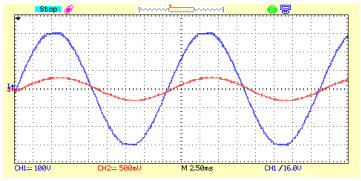
(a)



(b)

Fig. 9. The output voltage waveforms; (a) first unit; (b) second unit.

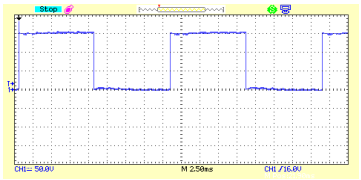
The experimental output voltage and current waveforms are shown in Fig. 10. As it is obvious from Fig. 11, this inverter is able to produce 61 levels with the maximum amplitude of 300V and 3mA at the output. Comparing the voltage waveform with current waveform shows that the current waveform is closer to ideal sinusoidal one. In addition, the current waveform consists of a phase shift in relation to voltage waveform. This is due to resistive-inductive feature of the load, which behaves as a low-pass filter.



(b)

Fig. 10. The output voltage and current waveforms.

As mentioned before, the unidirectional power switches from voltage points of view are used in the proposed cascaded multilevel inverter. In order to investigate this fact the experimental voltage waveforms on switches $S_{a,1}$ and $S_{L,11}$ of the first basic unit and $S_{b,2}$ and $S_{R,22}$ of the second unit are indicated in Fig. 11. As shown in Fig. 11, the magnitude of the blocked voltage on switches $S_{a,1}$, $S_{L,11}$, $S_{b,2}$ and $S_{R,22}$ are either positive or zero and there is not any negative amount on them. This fact reconfirms the existing of unidirectional power switches in this topology. In addition, the maximum blocked voltage by switches $S_{a,1}$, $S_{L,11}$, $S_{b,2}$ and $S_{R,22}$ are equal to $150V$, $10V$, $150V$ and $20V$, respectively. Considering the obtained value of blocked voltage by switches, the related equations to the maximum amount of blocked voltage by the switches are well confirmed.



(a)

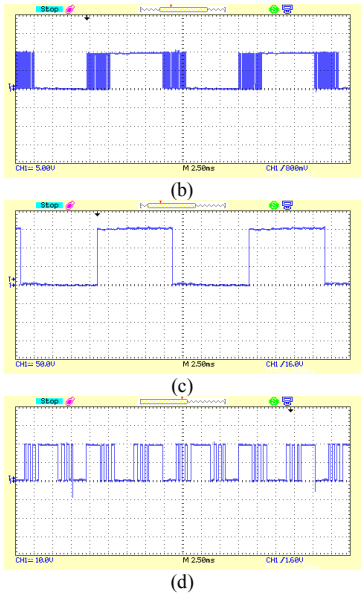


Fig. 11. Experimental voltage waveform on switches; (a) $S_{a,1}$; (b) $S_{L,11}$; (c) $S_{b,2}$; (d) $S_{R,22}$.

VI. CONCLUSION

In this paper, a new cascaded multilevel inverter is proposed. To generate both positive and negative voltage levels at the output, two different algorithms are proposed. Based on these algorithms, this inverter requires lower number of power electronic devices and minimum amount of blocked voltage by switches than the presented topologies in literature that lead to reduce the installation space and cost of the inverter. For instance, to generate minimum 511 levels at the output, the required number of power electronic devices and the amount of the blocked voltage by switches for the proposed topology based on the second algorithm by considering $m=2$ and $n=2$ are equal to $N_{switch}=N_{IGBT}=N_{drive}=20$, $N_{source}=8$ and $V_{block}=1044V_{dc}$. However, these values for the H-bridge cascaded multilevel inverter that has been presented in [9] and known by R_3 in this paper are equal to $N_{switch}=N_{IGBT}=N_{drive}=24$, $N_{source}=6$ and $V_{block}=1456V_{dc}$. However, the presented inverter by R_3 has the best performance between all of the other presented cascaded topologies. Then, the optimum topology for maximum number of output voltage levels based on constant number of switches and dc voltage sources are obtained. In addition, the other optimum structures for the proposed topology are also obtained. These optimizations are based on generation a constant number of output levels based on the minimum number of required switches, or dc voltage sources and or the amount of blocked voltage by power switches. Finally, the obtained experimental results on a 61-level inverter verify the accuracy performance of the proposed inverter.

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