A High Step-Up DC to DC Converter Under Alternating Phase Shift Control for Fuel Cell Power System

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***Abstract*—This paper investigates a novel pulse width modulation (PWM) scheme for two-phase interleaved boost converter with voltage multiplier for fuel cell power system by combining alternating phase shift (APS) control and traditional interleaving PWM control. The APS control is used to reduce the voltage stress on switches in light load while the traditional interleaving control is used to keep better performance in heavy load. The boundary condition for swapping between APS and traditional interleaving PWM control is derived. Based on the aforementioned analysis, a full power range control combining APS and traditional interleaving control is proposed. Loss breakdown analysis is also given to explore the efficiency of the converter. Finally, it is verified by experimental results.**

***Index Terms*—Boost converter, fuel cell, interleaved, loss breakdown, voltage multiplier.**

I. Introduction

WITH increasing concern about energy and environment, it is necessary to explore the renewable energy including wind power, solar, fuel cell, etc. Fuel cell is one of promising choices due to its advantages of zero emission, low noise, higher power density, and being easily modularized for portable power sources, electric vehicles, distributed generation systems, etc [1].

The grid-connected power system based on fuel cell is shown in Fig. 1. For a typical 10-kW proton exchange membrane fuel cell, the output voltage is from 65 to 107 V. However, the input voltage of the three phase dc/ac converter needs to be around 700 V, the voltage gain of the dc/dc converter between fuel cell and the dc/ac converter will be from 6 to 11 V. A high step-up dc/dc converter is needed for the system as shown in Fig. 1. The dc/dc converter will generate a high frequency input current ripple, which will reduce the life time of the fuel cell stack [2]–[4]. In addition, the hydrogen energy utilization decreases with increasing the current ripple of the fuel cell stack output [5]. Therefore, the dc/dc converter for the system as shown in Fig. 1 should have high step-up ratio with minimum input current ripple.

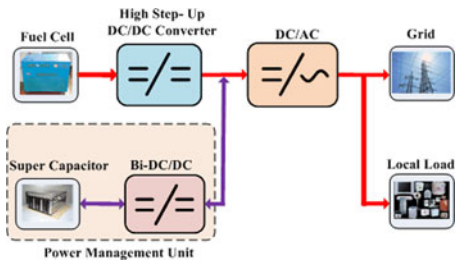

Fig. 1. Grid-connected power system based on fuel cell.

High step-up ratio can be achieved by combining classical boost converter with switched inductors [6], coupled inductors [7]–[9], high-frequency transformer [10], or switched capacitor [11]–[14], [19]. They can obtain high step-up ratio with high efficiency, low-voltage stress, and low electromagnetic interference. In order to reduce output fuel cell stack output current ripple or the dc/dc converter input current ripple, either a passive filter [15] or active filter [5] can be used, however, this will increase the complexity of the system. In fact, interleaving the dc/dc converter can reduce the input current ripple of the dc/dc converter [16]. An interleaved boost converter with voltage multiplier was proposed in [13], [14]. Its voltage gain was increased up to $(M+1)$ times (M is the number of the voltage multiplier) of the classical boost converter with the same duty-cycle D and lower voltage stress. Besides, it has lower input current ripples and output voltage ripples in comparison to the classical boost converter. The interleaving boost converter with voltage multipliers is shown in Fig. 2.

The converter shown in Fig. 2 can achieve low-voltage stress in the power devices, which increases the conversion efficiency. However, this is only true in heavy load when the voltage stress of the power devices might increase when it works in discontinuous conduction mode (DCM) [17], which occurs when fuel cell only supplies a light local load as shown in Fig. 1. In this case, higher voltage power devices need to be used, and therefore its cost and power loss will be increased. These authors proposed

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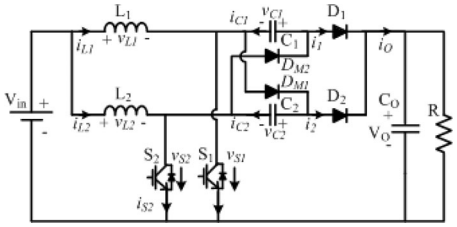

Fig. 2. Structure of two-phase interleaved boost converter with voltage multiplier [13], [14].

a new pulse width modulation (PWM) control method, named as alternating phase shift (APS), to overcome the problem when the converter operates in light load [17], [18].

This paper investigates a novel PWM scheme for two-phase interleaved boost converter with voltage multiplier for fuel cell power system by combining APS and traditional interleaving PWM control. The APS control is used to reduce the voltage stress on switches in light load while the traditional interleaving control is used to keep better performance in heavy load. The boundary condition for swapping between APS and traditional interleaving PWM control is derived. Based on the aforementioned analysis, a full power range control combining APS and traditional interleaving control is proposed. Loss breakdown analysis is also given to explore the efficiency of the converter. Finally, it is verified by experimental results.

II. Boundary Condition Analysis With Traditional Interleaving Control for Low Power Operation

It is assumed that all components in the converter are ideal, both capacitor C_1 and C_2 are large enough, and duty cycle is less than 0.5. The operation of a switching cycle of the converter can be divided into six stages at boundary condition which the voltage stress on switch will be larger than half of the output voltage with traditional interleaving control, as shown in Fig. 3. Typical theoretical waveforms at boundary condition are shown in Fig. 4.

1) *First Stage*(t_0, t_1): At the moment of t_0, both switch S_1 and S_2 are off, the energy stored in the inductor L_2 and capacitor C_2 in previous stage are transferred to the output capacitor C_O through D_2 as shown in Fig. 3(a). The voltage stress on switch S_1 is the input voltage $V_{\rm in}$, and the voltage stress on switch S_2 is $(V_O - V_{C2})$, where V_O is the output voltage and V_{C2} is the voltage of capacitor C_2.
2) *Second Stage*(t_1, t_2): At the moment of t_1, the switch S_1 is turned ON, the inductor L_1 starts to store energy from zero as shown in Fig. 3(b). In the meantime, if $(V_{C1} + V_{C2}) < V_O$, where V_{C1} is the capacitor C_1 voltage, the diode D_2 will be turned OFF and the diode D_{M2} will be turned ON; therefore, the energy in the inductor L_2 will be transferred to the capacitor C_1. If there is enough energy in the inductor L_2, V_{C1} will be charged to the following state: $V_{C1} + V_{C2} \geq V_O$. Then, the diode D_2 will be turned ON again, which is shown in Fig. 5. If there is not enough energy to charge V_{C1} to $(V_O - V_{C2})$, then it will come to the *Third Stage* as shown in Fig. 3(c). If the energy in the inductor L_2 is just discharged to zero and $V_{C1} + V_{C2} = V_O$ at the end of the stage, then we say that the circuit operates in the boundary condition state. During the stage, the voltage stress-on switch S_2 is V_{C1}.

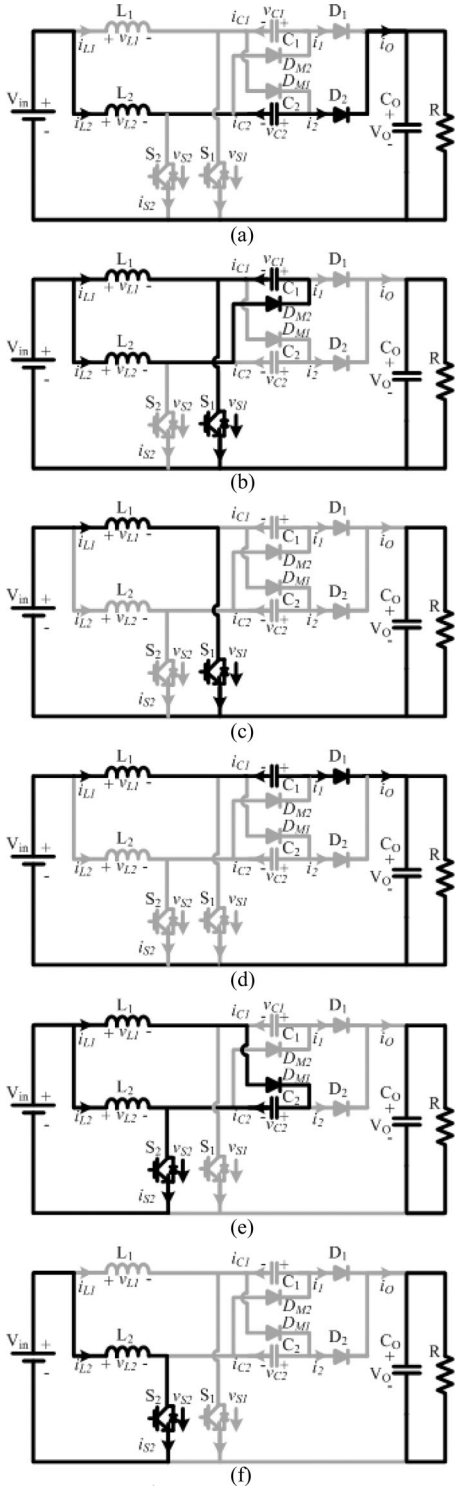

Fig. 3. Stages at boundary condition. (a) First stage (t_0, t_1), (b) second stage (t_1, t_2), (c) third stage (t_2, t_3), (d) fourth stage (t_3, t_4), (e) fifth stage (t_4, t_5), (f) sixth stage (t_5, t_6).

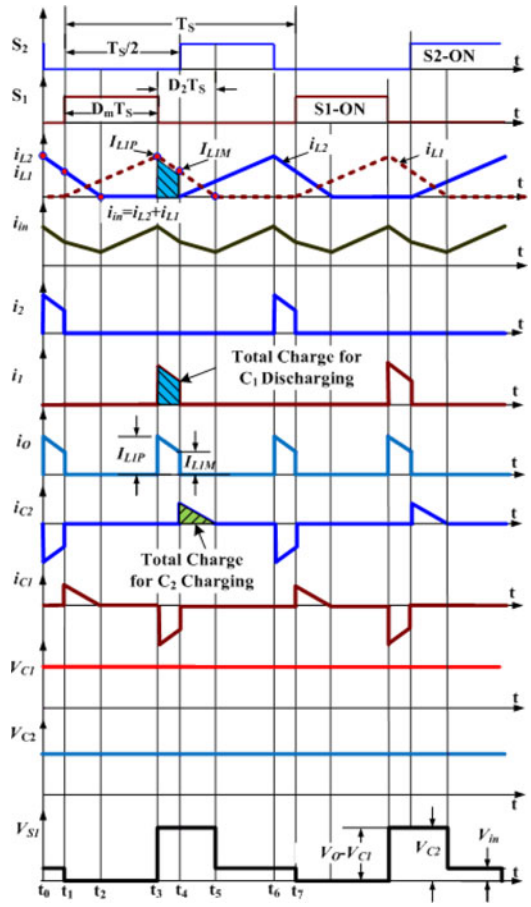

Fig. 4. Main theoretical waveforms at boundary condition.

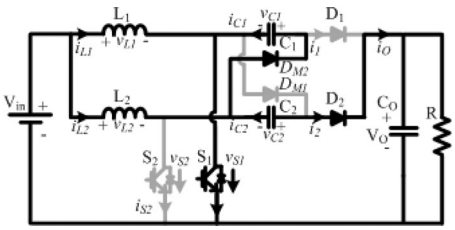

Fig. 5. One stage above boundary condition.

3) *Third Stage*(t_2, t_3): At the moment of t_2, the current in the inductor L_2 just falls to zero, all the diodes are in off state and the inductor L_1 is in charging state until the switch S_1 is turned OFF at the moment of t_3. The voltage stress on switch S_2 is V_{in}. At the end of this stage, the current in the inductor L_1 comes to the peak value I_{L1P}, and

$$I_{L1P} = \frac{V_{\text{in}} D_m T_S}{L} \tag{1}$$

where V_{in} is the input voltage, L is the inductance of L_1 and L_2, D_m is the duty cycle at boundary condition, and T_S is the switching period.

4) *Fourth Stage* (t_3, t_4): At the moment of t_3, switch S_1 and S_2 are in off state, the energy in the inductor L_1 and the capacitor C_1 will be transferred to the output capacitor C_O through the diode D_1, which is similar to *First Stage*. In this stage, the voltage stress on switch S_1 is $(V_O - V_{C1})$, and the voltage stress on switch S_2 is V_{in}. At the end of this stage, the current in the inductor L_1 decreases to be I_{L1M}

$$I_{L1M} = I_{L1P} - \frac{V_O - V_{C1} - V_{\text{in}}}{L}(0.5 - D_m)T_S. \tag{2}$$

5) *Fifth Stage* (t_4, t_5): At the moment of t_4, the switch S_2 is turned ON and the inductor L_2 starts to store energy. This stage is similar to the *Second Stage*. In this stage, the voltage stress on switch S_1 is V_{C2}. At the end of this stage, the current in the inductor L_1 decreases to zero from I_{L1M}. And thus

$$I_{L1M} - \frac{V_{C2} - V_{\text{in}}}{L}(D_2 - 0.5 + D_m)T_S = 0 \tag{3}$$

where D_2 is the duty cycle as shown in Fig. 4.

6) *Sixth Stage* (t_5, t_6): At the moment of t_5, the current in the inductor L_1 decreases to zero. All the diodes are in off state and the inductor L_2 is in charging state until the stage comes to the end at the moment t_6. A new switching period will begin with the next *First Stage*.

From the aforementioned analysis, the voltage sum of capacitor C_1 and C_2 will be V_O at boundary condition. If it is less than V_O, the voltage stress on switch S_1 and S_2 will be larger than $V_O/2$, because the voltage stress on switch S_1 is $(V_O - V_{C1})$ during the *Fourth Stage* and the voltage stress on switch S_2 is $(V_O - V_{C2})$ during the *First Stage*.

The average value of the output current i_O is equal to the dc component of the load current V_O/R, then

$$\begin{aligned}\frac{V_O}{R} &= \frac{1}{T_S}\int_0^{T_S} i_O\,dt = \frac{1}{T_S}\int_0^{T_S}(i_1 + i_2)dt \\ &= \frac{1}{T_S}\int_0^{T_S} i_1\,dt + \frac{1}{T_S}\int_0^{T_S} i_2\,dt.\end{aligned} \tag{4}$$

Considering the same parameters of the circuit in two phases as shown in Fig. 2, therefore

$$\frac{1}{T_S}\int_0^{T_S} i_1\,dt = \frac{1}{T_S}\int_0^{T_S} i_2\,dt. \tag{5}$$

By combining (4) and (5), it is derived

$$\begin{aligned}\frac{V_O}{R} &= \frac{2}{T_S}\int_0^{T_S} i_1\,dt = \frac{2}{T_S}\int_{t3}^{t4} i_1\,dt \\ &= \frac{2}{T_S}\cdot\left[\frac{1}{2}(I_{L1P} + I_{L1M})(0.5 - D_m)T_S\right] \\ &= (I_{L1P} + I_{L1M})(0.5 - D_m)\end{aligned} \tag{6}$$

where R is the load.

At the boundary condition, the diode D_2 (D_1) approaches the conduction state during the *Second Stage* (*Fifth Stage*), which is shown in Fig. 5.

The following equation can be obtained

$$V_{C1} + V_{C2} = V_O. \tag{7}$$

Considering both capacitors C_1 and C_2 are large enough, average voltage of the capacitor will keep equal. Otherwise, the

converter will not operate at boundary condition, therefore

$$V_{C1} = V_{C2} = \frac{1}{2}V_O. \tag{8}$$

By substituting (1) and (8) into (2), the current I_{L1M} can be derived

$$I_{L1M} = \frac{V_{\text{in}} - V_O/2 + V_O \cdot D_m}{2L} T_S. \tag{9}$$

As shown in Fig. 4, the total discharge of capacitor C_1 between t_3 and t_4 is

$$Q_{C1} = \int_{t_3}^{t_4} i_{L1}dt = \frac{1}{2}(I_{L1P} + I_{L1M})(0.5 - D_m)T_S. \tag{10}$$

The total charge of capacitor C_2 between t_4 and t_5 is

$$Q_{C2} = \int_{t_4}^{t_5} i_{L1}dt = \frac{1}{2}I_{L1M}(D_2 - 0.5 + D_m)T_S. \tag{11}$$

According to the previous analysis, the total discharge of C_1 is equal to the total charge of capacitor C_2 at boundary condition. Therefore, there will be

$$Q_{C1} = Q_{C2}. \tag{12}$$

By combining (10), (11), and (12), the following can be derived

$$D_2 = (0.5 - D_m)\left(\frac{I_{L1P}}{I_{L1M}} + 2\right). \tag{13}$$

By combining (3) and (6) and then substituting (1), (9), and (13) into them, the boundary condition can be derived as

$$\begin{cases} K = K\text{crit} = \dfrac{n-2}{2n(n-\sqrt{2})^2} & (a) \\ D_m = \dfrac{n-2}{2(n-\sqrt{2})} & (b) \end{cases} \tag{14}$$

where n is the voltage gain of the converter ($n = V_O/V_{\text{in}}$), and K is the parameters of the circuit and $K = 2L/(R \times T_S)$.

The boundary constraint with traditional interleaving control decided by (14) is shown in Fig. 6. The constraint includes two parts: duty cycle D and the circuit parameters $K = 2L/(R \times T_S)$.

As the switching period T_S and the input inductor L are designed at nominal operation in continuous conduction mode (CCM), the constraint is determined by duty cycle D and the load R. The reason why there are two parts in the boundary constraint is that the duty cycle D varies with the load when the converter operates in DCM. For a given application, the voltage gain of the dc/dc converter is determined. And then, the minimum duty cycle that can maintain low-voltage stress in main power devices with traditional interleaving control will be given by (14)-(b) and as shown in Fig. 6(a). At the same minimum duty cycle, the converter operates at boundary condition when the circuit parameters $K = 2L/(R \times T_S)$ satisfy (14)-(a) and as shown in Fig. 6(b).

When the converter operates above the boundary condition, the circuit parameters are in Zone A of Fig. 6(b), i.e., $K > K_{\text{crit}}$, the converter could achieve halved voltage stress on switches with traditional interleaving control with the duty cycle above

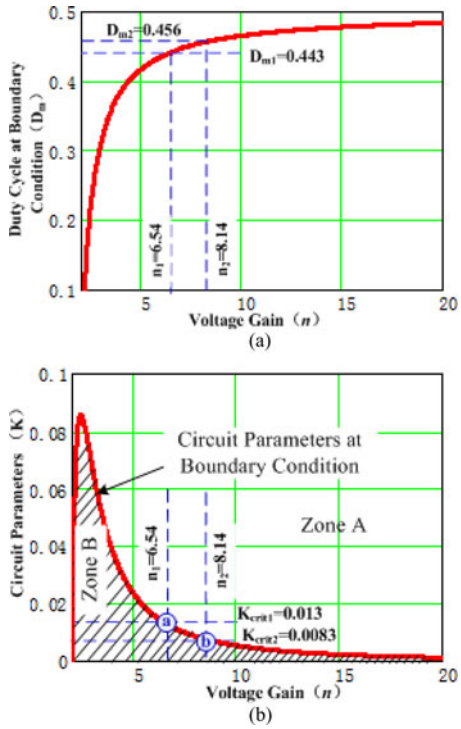

Fig. 6. Boundary constraint varies with voltage gain. (a) Duty cycle at boundary condition varies with voltage gain, (b) circuit parameters at boundary condition varies with voltage gain.

the solid red line as shown in Fig. 6(a). When decreasing the load to the solid red line at boundary condition in Fig. 6(b), i.e., $K = K_{\text{crit}}$, the duty cycle of the converter will be decreased to the solid red line in Fig. 6(a). When decreasing the load further in Zone B in Fig. 6(b), i.e., $K < K_{\text{crit}}$, the duty cycle will be decreased further to be smaller than the minimum duty cycle that maintains low-voltage stress on switches with traditional interleaving control. Then, the APS control should be used to achieve halved voltage stress on switches in Zone B [17], [18].

In our 1-kW prototype design, the input voltage of the converter is 86–107 V, and the output voltage of the converter is 700 V. The voltage gain will vary from $n_1 = 6.54$ to $n_2 = 8.14$, and then the circuit parameters at boundary conditions K_{crit} will vary from $K_{\text{crit1}} = 0.013$ to $K_{\text{crit2}} = 0.0083$ as shown in Fig. 6(b), the duty cycle will vary from $D_{m1} = 0.443$ to $D_{m2} = 0.456$ in order to maintain the stable output voltage. When the circuit parameters $K = 2L/(R \times T_S)$ are below the solid red line from point ⓐ to point ⓑ at different voltage gain as shown in Fig. 6(b), the duty cycle will be decreased further to be less than the solid red line from $D_{m1} = 0.443$ to $D_{m2} = 0.456$ as shown in Fig. 6(a), and then the voltage stress on switches will be increased at this load. In order to achieve the halved voltage stress on switches at this load, APS control is needed.

III. Control Scheme of All Power Range With APS and Traditional Interleaving Control

According to the principle of APS [17], APS control is proposed to solve the light load problem with duty cycle less than 0.5 as shown in Fig. 7(a). With the load increasing, the duty

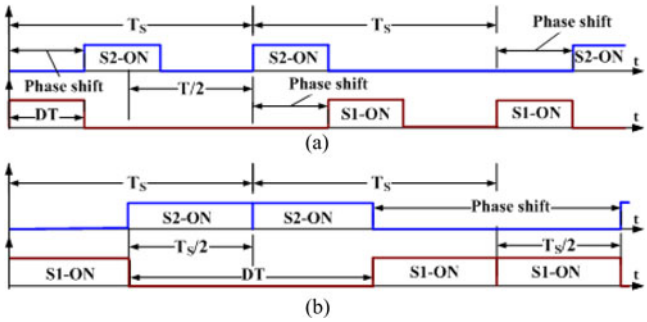

Fig. 7. PWM waveform of APS with D < 0.5 and D = 0.5. (a) D < 0.5, (b) D = 0.5.

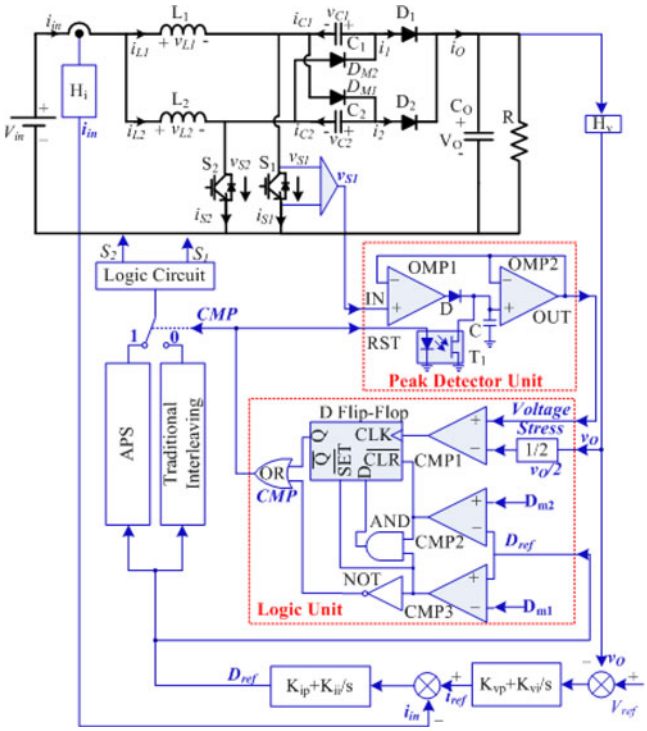

Fig. 8. Block diagram of the converter with the control scheme of all power range.

cycle will be increased as well. When the duty cycle is increased to 0.5, the APS control will be altered to be traditional interleaving control with halved switching frequency as shown in Fig. 7(b). According to previous analysis as shown in Fig. 6, the minimum duty cycle to achieve low-voltage stress on switches with traditional interleaving control is less than 0.5. Therefore, it is possible to combine both APS control and traditional interleaving control to control the converter for full power range operation.

Considering the variation of the input voltage from 86 to 107 V for 1-kW fuel cell operation and the output voltage of the converter 700 V, the minimum duty cycle of traditional interleaving control varies from $D_{m1} = 0.443$ to $D_{m2} = 0.456$. The control scheme is shown in Fig. 8. The duty cycle is divided into three areas: $D < D_{m1}, D > D_{m2}$, and $D_{m1} \le D \le D_{m2}$. In the first area, i.e., $D < D_{m1}$, APS control will be used because traditional interleaving control cannot be effective to maintain low-voltage stress on switches. In the second area, i.e., $D > D_{m2}$, traditional interleaving control will be used. In the third area, i.e., $D_{m1} \le D \le D_{m2}$, either APS control or traditional interleaving control may be used.

TABLE I
OPERATIONAL PRINCIPLE OF THE LOGIC UNIT IN FIG. 8

v_{S1}>0.5v_O	D_{ref}>D_{m1}	D_{ref}<D_{m2}	Control Method
X	1	0	Traditional interleaving control
X	0	1	APS control
0	1	1	Keep the previous control mode
1	1	1	Swap from traditional interleaving control to APS control and stay in APS control until D_{ref}>D_{m2}

In the first area $(D < D_{m1})$ with APS control and the second area $(D > D_{m2})$ with traditional interleaving control, the capacitor voltage is half of the output voltage. Therefore, the switches voltage stress is clamped to half of the output voltage [17], [18].

The swapping between the APS control and traditional interleaving control in the area $D_{m1} \le D \le D_{m2}$ is achieved by detecting the voltage stress of the switch S_1 as shown in Fig. 8. When the voltage stress of the switch S_1 is higher than half of the output voltage, the control is changed from interleaving control to APS control. If the traditional interleaving control is initially used in the second area $(D_{m1} \le D \le D_{m2})$ and once the switch S_1 voltage stress is larger than half of the output voltage, the logic unit output *CMP* in Fig. 8 will be changed to $CMP = 1$ and APS control will be enabled. The aforementioned function for swapping between the APS and traditional interleaving control is achieved by the Logic Unit as shown in Fig. 8, and the operational principle of the Logic Unit is shown in Table I.

If APS control mode is used (i.e., $CMP = 1$), the optocoupler transistor T_1 is turned ON, the voltage of capacitor C in the peak detector unit is resetted and the peak detector unit is disenabled. If the traditional interleaving control mode is used (i.e., $CMP = 0$), the optocoupler transistor T_1 will be turned OFF, and the peak detector unit is enabled and used to detect the voltage stress of switch S_1.

In order to achieve better dynamic performance operation, dual loop control is adopted as shown in Fig. 8, in which the inner current loop is to control the input inductor current while the outer voltage loop is to control the output voltage. K_{ip} and K_{ii} are the PI controller parameters of the inner current loop, while K_{vp} and K_{vi} are the PI controller parameters of the outer voltage loop.

In our 1-kW prototype design, the circuit parameters are as follows, $V_{\text{in}} = 100$ V, $V_O = 700$ V, $C_1 = C_2 = 40\ \mu$F, $C_O = 195\ \mu$F, $L_1 = L_2 = 1158\ \mu$H, $T_S = 100\ \mu$s, $H_v = 20.56$, $H_i = 698.298$, where H_v is the output voltage feedback coefficient and H_i is the input current feedback coefficient. The bandwidth of the inner current loop is 1 kHz with PI parameters as follows: $K_{ip} = 0.061, K_{ii} = 63.67$.

TABLE II
MAIN CHOICES OF POWER DEVICES

Symbol	Voltage Stress	Product Type
S_1,S_2	350V	IKW20N60H3
D_1,D_2	350V	DSEP15-06A IDW16G65C5
D_{M1},D_{M2}	700V	DSEP15-12CR IDH15S120

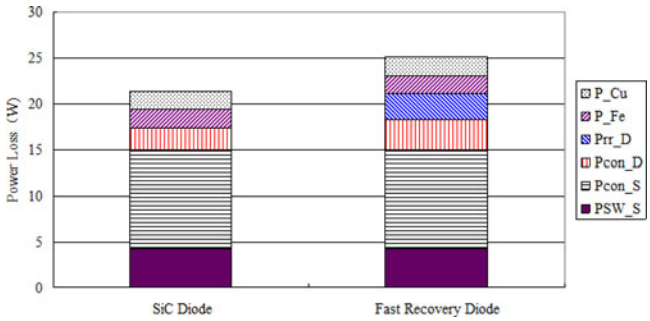

Fig. 9. Loss distribution of the converter with IGBT (IKW20N60H3) in CCM (r = 0.37) at 1 kW. (SiC Diode: IDH15S120 and IDW16G65C5, Fast Recovery Diode: DSEP15-12CR and DSEP15-06A).

The bandwidth of the outer voltage loop is 100 Hz with PI parameters as follows: $K_{vp} = 32.103,\ K_{vi} = 2017$.

IV. LOSS BREAKDOWN ANALYSIS

As the cost of fuel cell is still very high, it is important to maximize the efficiency of the power converter for fuel-cell-based power system in order to reduce its operation cost and increase the utilization of fuels. Therefore, loss breakdown analysis is needed.

The nominal power of the converter is 1 kW for loss breakdown analysis and prototype setup, and the input voltage is 100 V while the output voltage is 700 V with switching frequency $f_S = 10$ kHz. The power devices used are shown in Table II.

The converter could operate in CCM at nominal load with input current ripple ratio $r = 0.37$ and the inductor L_1 and L_2 is 1158 μH. The inductor is built with the amorphous core. As shown in Fig. 9, the main parts of the loss are the conduction loss $(\mathrm{P_{con\_S}})$ and switching loss $(\mathrm{P_{SW\_S}})$ of the IGBT. With the fast recovery diodes (DSEP15-12CR and DSEP15-06A) and IGBT (IKW20N60H3), the efficiency of the converter at nominal load can be 97.49%. As there is no reverse recovery loss $(\mathrm{P_{rr\_D}})$ in silicon carbide (SiC) diode, the efficiency can be increased to be 97.86% with SiC diode (IDH15S120 and IDW16C65C5) and IGBT (IKW20N60H3).

The converter could also operate in boundary conduction mode (BCM) at nominal load with input current ripple ratio ($r = 0.6$) and the inductor L_1 and L_2 is 714.3 μH. The inductor is built with the amorphous core. As shown in Fig. 10, the main parts of the loss also include the conduction loss $(\mathrm{P_{con\_S}})$ of the IGBT. Compared with CCM as shown in Fig. 9, there is no fast recovery loss even with fast recovery diodes in BCM. However, the inductor loss including the core loss $(\mathrm{P_{\_Fe}})$ and the wire loss

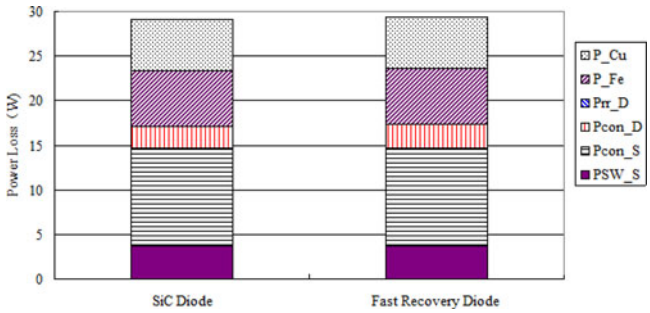

Fig. 10. Loss distribution of the converter with IGBT(IKW20N60H3) in BCM (r = 0.6) at 1 kW. (SiC Diode: IDH15S120 and IDW16G65C5, Fast Recovery Diode: DSEP15-12CR and DSEP15-06A).

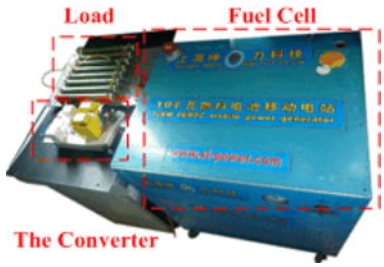

Fig. 11. Prototype of the 1-kW Converter with fuel cell and load.

$(\mathrm{P_{\_Cu}})$ is increased in BCM as the current ripple is increased from 0.37 to 0.6. In BCM, the efficiency of the converter can be 97.09% with SiC diode and 97.06% with fast recovery diode.

Comparing Fig. 9 and Fig. 10, the efficiency of the converter with IGBT and fast recovery diode in CCM is a bit higher than that in BCM. In CCM, the efficiency of the converter with fast recovery diode is only 0.37% less than that with SiC diode. Therefore, we use IGBT and fast recovery diode in CCM for experiments.

V. EXPERIMENTAL RESULTS

A. Static Experiments

In order to verify the previous analysis, prototype is built as shown in Fig. 11. The circuit parameters are as follows, $V_{\mathrm{in}} = 100$ V, $V_O = 700$ V, $C_1 = C_2 = 40\ \mu$F, $C_O = 195\ \mu$F, $L_1 = L_2 = 1158\ \mu$H, $T_S = 100\ \mu$s. The load at boundary condition is $R_{BC} = 2023\ \Omega$ and $K_{\mathrm{crit}} = 0.011$ at boundary condition according to (14), the duty cycle D_m at boundary condition is 0.448.

The experimental results at boundary condition are shown in Fig. 12, which are in accordance with the theoretical waveform in Fig. 4.

The experimental results are given to verify the previous analysis. With $R = 478\ \Omega$, the output power is a bit greater than 1 kW, and $K = 0.048 > K_{\mathrm{crit}} = 0.011$, the converter is designed to operate in Zone A of Fig. 6(b), and the traditional interleaving control can maintain the voltage stress on switches with half of the output voltage (i.e., 350 V) as shown in Fig. 13. With $R = 1658\ \Omega$, i.e., $K = 0.014 > K_{\mathrm{crit}} = 0.011$, the converter will continue operating in Zone A of Fig. 6(b), and the voltage stress

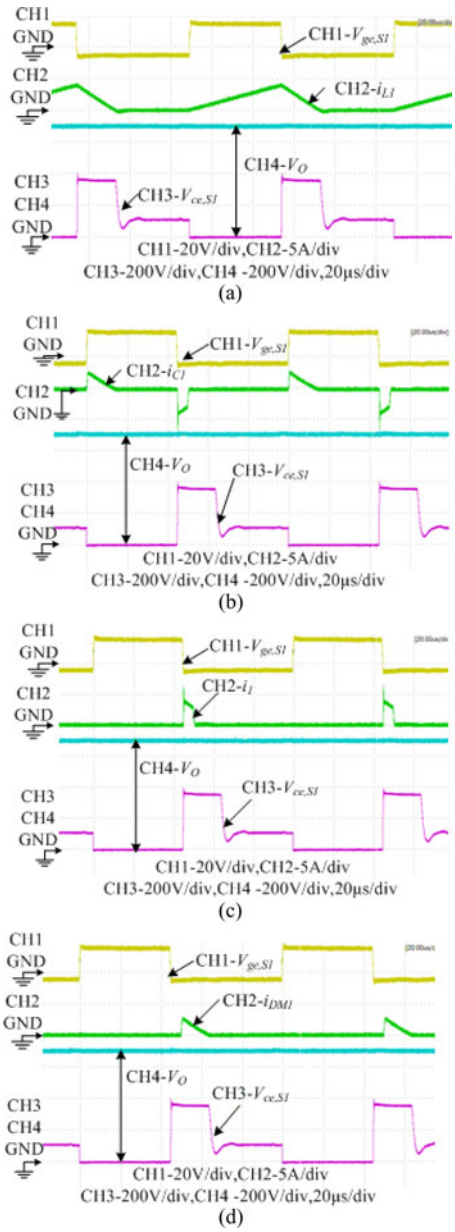

Fig. 12. Experimental results at boundary condition with traditional interleaving control ($L = 1158$ μH, $R = 2023$ Ω, and $D = 0.448$). (a) CH1-S_1 Driver Voltage, $\mathrm{CH2} - L_1$ Current, CH3-S_1 Voltage Stress, CH4-Output Voltage, (b) CH1-S_1 Driver Voltage, $\mathrm{CH2} - C_1$ Current, CH3-S_1 Voltage Stress, CH4-Output Voltage, (c) CH1-S_1 Driver Voltage, $\mathrm{CH2} - D_1$ Current, CH3-S_1 Voltage Stress, CH4-Output Voltage, (d) CH1-S_1 Driver Voltage, $\mathrm{CH2} - DM_1$ Current, CH3-S_1 Voltage Stress, CH4-Output Voltage.

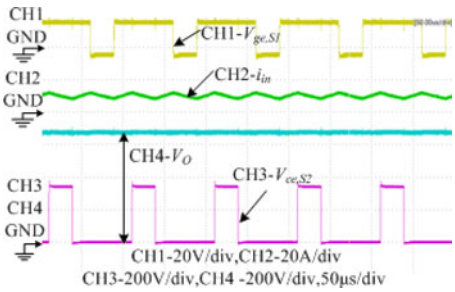

Fig. 13. Traditional interleaving control at nominal load ($L = 1158$ μH and $R = 478$ Ω).

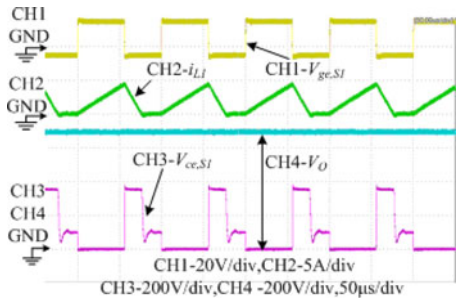

Fig. 14. Traditional interleaving control in Zone A ($L = 1158$ μH and $R = 1658$ Ω).

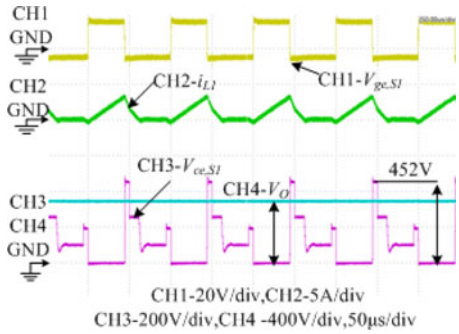

Fig. 15. Traditional interleaving control in Zone B ($L = 1158$ μH and $R = 3460$ Ω).

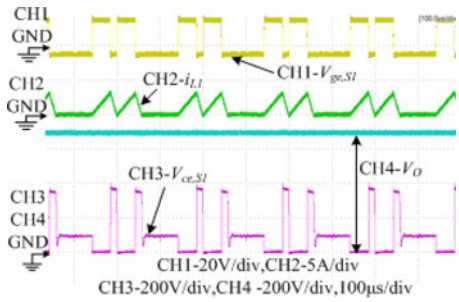

Fig. 16. APS control in Zone B ($L = 1158$ μH and $R = 3460$ Ω).

on switches is still 350 V, which is about the half of the output voltage as shown in Fig. 14. However, when decreasing the load to be 3460 Ω, i.e., $K = 0.0067 < K_{\mathrm{crit}} = 0.011$, the converter will operate in Zone B of Fig. 6(b). Here for comparison, two control methods are used and the results are shown in Fig. 15 and Fig. 16, respectively. In Fig. 15, traditional interleaving control is used, and we can see the voltage stress on the switch is 452 V which is higher than half of the output voltage. In Fig. 16, APS control is used, and we can see the voltage stress on the switch is 350 V which is about half of the output voltage. Therefore, it is effective to use APS control when the converter operates in Zone B.

With the control scheme as shown in Fig. 8, more experiments are conducted to measure the voltage stress on power switches in all power range of the load. As shown in Fig. 17, the voltage stress follows the variation of the output voltage, and almost keeps half of the output voltage in all power range. The reason

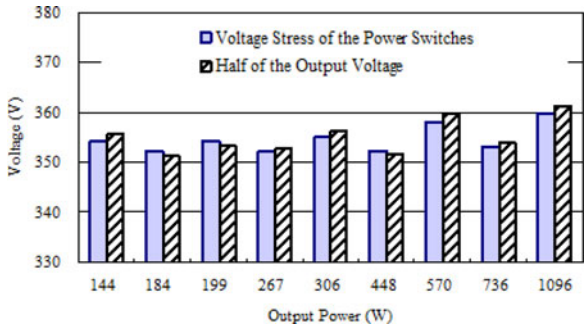

Fig. 17. Voltage stress on power switches in all power range of the load.

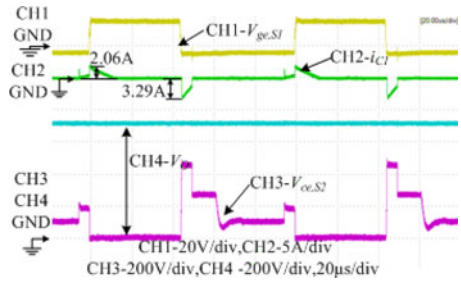

Fig. 18. Experimental results of current peak of capacitor C_1 with traditional interleaving control under $R = 3460\ \Omega$.

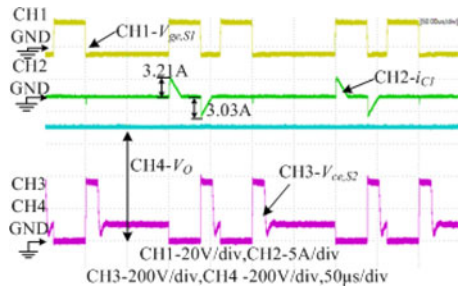

Fig. 19. Experimental results of current peak of capacitor C_1 with APS control under $R = 3460\ \Omega$.

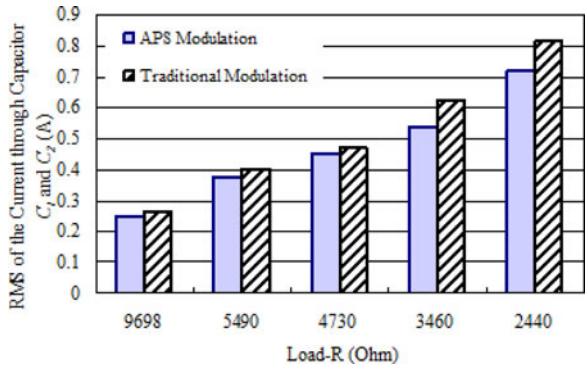

Fig. 20. Comparison on RMS of the current through capacitor (C_1 and C_2) with different control method below boundary condition ($R > 2023\ \Omega$).

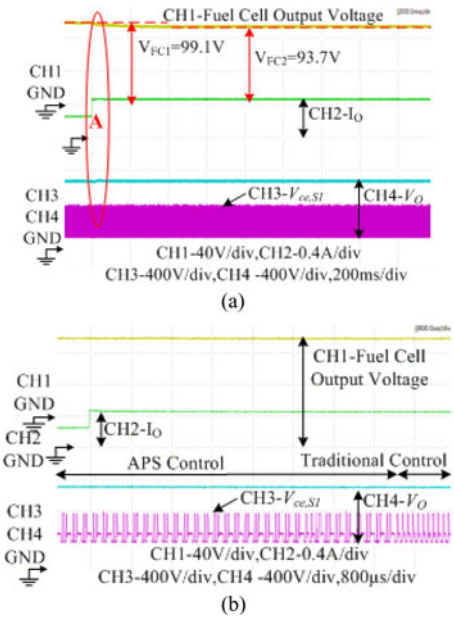

Fig. 21. Waveforms when load varies from 3478 Ω to 1658 Ω with fuel cell as input. (a) Waveforms when the load varies from 3478 Ω to 1658 Ω. (b) zoomed waveforms in Area A.

why the output voltage is not stable comes from the voltage ripple of 20 V in the output voltage.

As the current ripple through capacitors C_1 and C_2 has bad effect on their lifetime and reliability, it is important to test whether the maximum current ripple is increased when utilizing APS control. Considering the symmetry of the converter, we only test the current through C_1. As shown in Fig. 18, the peak current through capacitor C_1 is 3.29 A with traditional interleaving control under the load $R = 3460\ \Omega$, and the RMS of the current through capacitor C_1 is 0.623 A. With APS control, the current ripple is not increased but reduced to be 3.21 A under the same load as shown in Fig. 19, and the RMS of the current through capacitor C_1 is reduced to be 0.538 A. More experiments are conducted under different load as shown in Fig. 20, the current ripple with APS control is less than that with traditional interleaving control. Therefore, the proposed APS control can increase the lifetime and reliability of capacitors C_1 and C_2.

The C_1 and C_2 are designed with film capacitor with the part number is SHB-500–40–4 from EACO Capacitor, Inc., and its maximum RMS current is 19 A, which is much greater than the aforementioned current ripple.

B. Dynamic Experiments

In order to test the dynamic performance of the converter with fuel cell as input, the converter is connected to the output of the PEMFC shown in Fig. 11.

When the load varies from 3478 Ω to 1658 Ω as shown in Fig. 21, the output voltage of the fuel cell will varies from 99.1 to 93.7 V, the control scheme will swap from APS control to traditional interleaving control, the voltage stress of power switches keeps half of the output voltage during the period of load variation, and the output voltage of the converter keeps 700 V in stable operation under the two load. When the load varies from 1658 Ω to 3478 Ω as shown in Fig. 22, the output voltage of the fuel cell will varies from 93.7 to 99.1 V accordingly, the

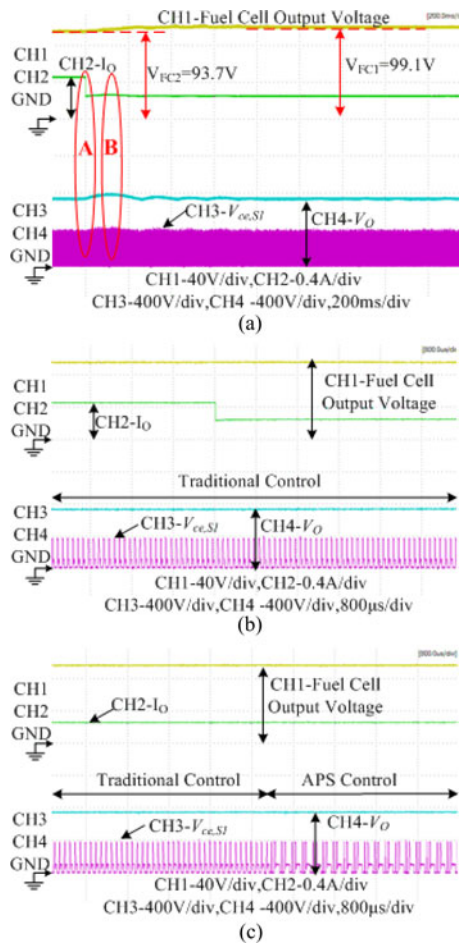

Fig. 22. Waveforms when load varies from 1658 Ω to 3478 Ω. Waveforms when load varies from 1658 Ω to 3478 Ω with fuel cell as input. (a) Waveforms when load varies from 1658 Ω to 3478 Ω, (b). (a) Waveforms when load varies from 1658 Ω to 3478 Ω with fuel cell as input, (b) Zoomed waveforms in Area A, (c) Zoomed waveforms in Area B.

control scheme will swap from traditional interleaving control to APS control, and the voltage stress of power switches keeps half of the output voltage as well. Therefore, the control scheme proposed in this paper could achieve halved voltage stress on switches when swapping between traditional interleaving control and APS control.

The prototype is built with the fast recovery diodes (DSEP15–12CR and DSEP15–06A) and IGBT (IKW20N60H3) and operates in CCM at 1 kW with input current ripple ratio $r = 0.37$. The inductor $L_1 = L_2 = 1158$ H is built with the amorphous core, and the number of the turns is N = 55, and the air gap is lg = 0.26 cm. The efficiency of the converter is shown in Fig. 23. The maximum point of test efficiency on the converter is 97.4%, and the efficiency at nominal power 1 kW is 97.2%. For comparison on the efficiency, traditional control method is also tested. As the voltage stress on devices will be increased to be greater than 600 V, only 1200-V devices (DSEP15–12CR and IKW25N120H3) are chosen. As shown in Fig. 23, the efficiency of the proposed control is better than that of traditional interleaving control.

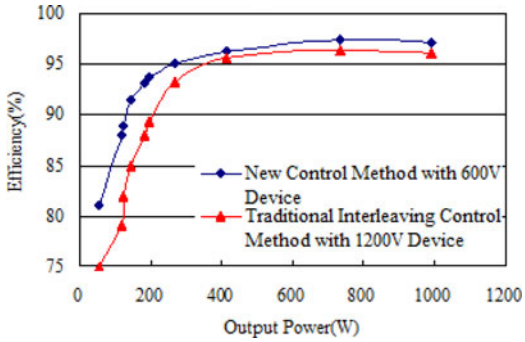

Fig. 23. Efficiency comparison of the converter with two control method. (Power device with new control method: DSEP15–12CR, DSEP15–06A and IKW20N60H3. Power device with traditional interleaving control method: DSEP15–12CR and IKW25N120H3).

VI. Conclusion

The boundary condition is derived after stage analysis in this paper. The boundary condition classifies the operating states into two zones, i.e., Zone A and Zone B. The traditional interleaving control is used in Zone A while APS control is used in Zone B. And the swapping function is achieved by a logic unit. With the proposed control scheme, the converter can achieve low-voltage stress on switches in all power range of the load, which is verified by experimental results.

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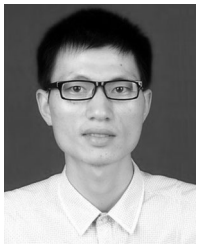

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