High-Power-Factor Rectifier Using the Modified SEPIC Converter Operating in Discontinuous Conduction Mode

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***Abstract*—The theoretical and experimental analysis of a modified version of the SEPIC dc–dc converter used as preregulator operating in discontinuous conduction mode (DCM) is presented in this paper. The proposed converter presents a low input current ripple operating in DCM, and the switch voltage is lower than the output voltage. The switch voltage reduction increases the converter reliability and a low drain-to-source on-resistance ($\mathrm{RDS_{on}}$) MOSFET can be used depending on the converter specification. Moreover, a digital control technique is applied to the proposed converter in order to reduce the third-harmonic input current distortion resultant of the operation in DCM. Finally, a 100-W prototype was developed operating with efficiency equal to 95.6%.**

***Index Terms*—AC–DC power conversion, digital control, rectifiers.**

I. Introduction

THE usual solution for the implementation of a high power factor (HPF) preregulator for a low-output power application ($P_o < 200\,\mathrm{W}$) is to use a boost converter operating in discontinuous conduction mode (DCM) [1], [2]. This is a simple and cost-effective solution because the design of the rectifier in DCM allows the converter to operate as a voltage follower, where the input current naturally follows the input voltage profile without the use of a current-control loop. The operation in DCM reduces the commutation losses since the switch turn-on occurs with zero-current switching (ZCS), and the output diode does not present reverse recovery current. This solution is limited for low-power applications due to an increased converter conduction losses operating in DCM.

Since the input inductor of the boost converter operates in DCM, a high-frequency filter composed by an inductor L_f and capacitor C_f must be used in the preregulator input in order to reduce the input current ripple, as presented in Fig. 1.

However, a problem presented by the boost preregulator operating in DCM is the input current distortion, presenting a third-harmonic component.

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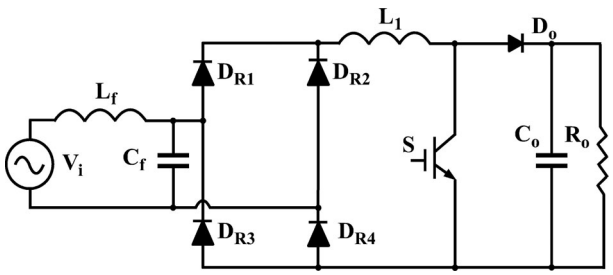

Fig. 1. Classical boost preregulator operating in DCM.

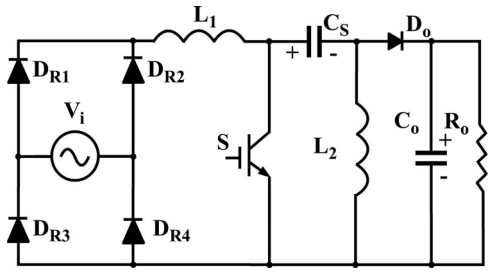

Fig. 2. Classical SEPIC preregulator operating in DCM.

The voltage applied across the input inductor during its demagnetization is equal to the output voltage minus the input voltage; hence, the current distortion increases when the difference between the output voltage and the peak input voltage is reduced. Therefore, the output voltage can be increased, reducing the third-harmonic input current distortion and improving the power factor. Also a variable duty-cycle control can be used in order to reduce the input current distortion as presented in Section V. The boost converter can operate with unitary power factor independently of the difference between the output and input voltage operating at the boundary of the DCM and continuous conduction mode (CCM) with a variable switching frequency modulation.

The classical SEPIC converter, shown in Fig. 2, presents a step-up/step-down static gain and usually is used as an HPF preregulator in applications where the output voltage must be lower than the peak of the ac input voltage [3], [4]. The implementation of the preregulator using the classical SEPIC converter in DCM presents two additional operation characteristics. Firstly, the converter operates as a voltage follower when designed in DCM with a low value for the inductor L_2 and using a high

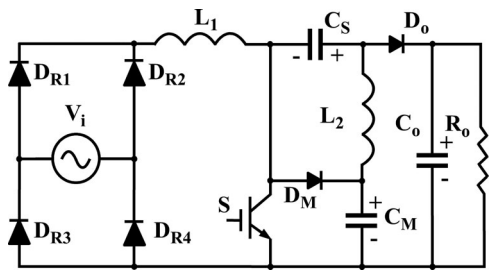

Fig. 3. Modified SEPIC preregulator operating in DCM.

value for the inductor L_1, but the input current presents a low current ripple just as a boost rectifier operating in CCM with current-control loop. Consequently, the L_f–C_f filter used in the boost converter input operating in DCM is not necessary using the SEPIC converter operating in DCM. Therefore, the number of components for both converters operating in DCM is equal. However, in a practical application, an electromagnetic interference (EMI) filter is necessary as in any rectifier topology.

The second important characteristic using the SEPIC converter in DCM is that the input current follows the input voltage waveform without input current distortion. The third-harmonic distortion is not presented because the inductor L_2 is demagnetized with the output voltage.

Nevertheless, the boost converter is the preferred topology used for the preregulator application where the output voltage must be higher than the peak of the input voltage, given that the switch voltage of the SEPIC converter is equal to the sum of the input and output voltages. The SEPIC converter can be successfully used in applications where the output voltage is lower than the input voltage. Several high-efficiency bridgeless configurations using the SEPIC and CUK converters are presented in [5]–[10].

The modified SEPIC converter used as preregulator operating in DCM is shown in Fig. 3. A modified SEPIC dc–dc converter was proposed in [11] with the inclusion of an additional diode (D_M) and capacitor (C_M) at the classical SEPIC converter, changing several characteristics such as the operation with a switch voltage lower than the output voltage. However, only the operation as dc–dc converter in CCM was analyzed in [11]. This converter was also used in [12] as a preregulator operating in CCM presenting some advantages when compared with the classical boost preregulator operating in CCM for universal line input application ($90\,V_{\rm rms} - 260\,V_{\rm rms}$).

Notwithstanding, the theoretical and experimental analyses of the modified SEPIC converter operating in DCM as a dc–dc converter and preregulator were not presented yet, which is focus of this paper.

The proposed topology presents the same limitations of the classical boost converter when compared with the classical SEPIC converter because its operation is solely possible as a nonisolated converter with step-up static gain. Differently from the classical SEPIC converter, an auxiliary inrush limitation circuit must be included for the rectifier start-up. Also, the power factor is lower than the classical SEPIC converter due to the third-harmonic component in the input current. However, the power factor and the input current distortion of the modified SEPIC converter can be significantly improved applying a simple open-loop action using the input and output voltage information.

The use of the boost and modified SEPIC rectifiers are only possible in applications with an output voltage higher than the peak of the input voltage, and these rectifiers are more appropriated than the SEPIC converter with the same specification, since the SEPIC converter presents a high switch voltage.

The lowest switch voltage level is presented by the modified SEPIC topology.

The modified SEPIC converter operates as a voltage follower and the input current presents low current ripple such as a classical SEPIC converter, designing the converter in DCM and using a low value for the inductor L_2 and a high value for the inductor L_1. The main converter characteristics and analyses are presented in the following, with the theoretical operation development of the proposed converter.

II. Theoretical Analysis

The circuit of the preregulator using the modified SEPIC converter operating in DCM is presented in Fig. 3. The main difference from the preregulator presented in [12] is the operation mode and the control system that is composed by only a voltage control loop due to the DCM operation. Also, the nondissipative current snubber used in [12] is not necessary because the reverse recovery current of the diodes and the turn-on switching losses operating in CCM are reduced with the DCM operation.

The modified SEPIC dc–dc converter operating in DCM presents three operation stages. The theoretical analysis is initially developed considering the operation as a dc–dc converter at steady state and all circuit components are considered ideal. The voltages across all capacitors are considered constant during a switching period, as an ideal voltage source. The DCM operation occurs when there is the third operation stage, where the power switch is turned off and the currents in all diodes of the circuit are null. Therefore, the DCM operation occurs when D_o and D_M diodes are blocked before the switch turn-on.

The analysis and design procedure is also developed for the operation as a preregulator with a diode bridge at input and an ac input voltage, based on the study as dc–dc converter.

The circuit presents two inductors, thus, different inductor values combination can be adopted for the DCM operation. In order to reduce the input current ripple of the preregulator, a relative high value for the inductor L_1 is considered. A relative low value of the inductor L_2 is used for the converter operation in DCM as a voltage follower, where the input current follows the input voltage waveform. As a result, the preregulator input current follows the input voltage waveform with low current ripple, without input filter and without current-control loop.

An important equation for the operation analysis of the converter is presented in (1).

Considering the operation at steady state, the average voltage across the inductors L_1 and L_2 are null and the sum of the input voltage V_i and capacitor C_S voltage is equal to the capacitor C_M voltage.

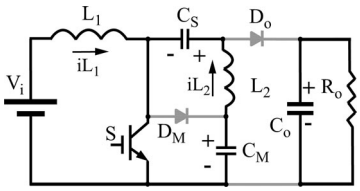

Fig. 4. First operation stage.

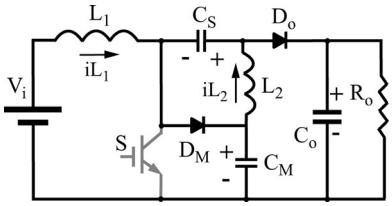

Fig. 5. Second operation stage.

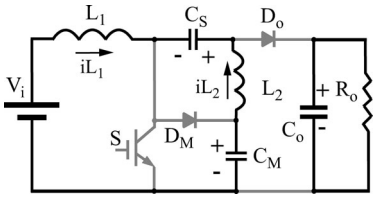

Fig. 6. Third operation stage.

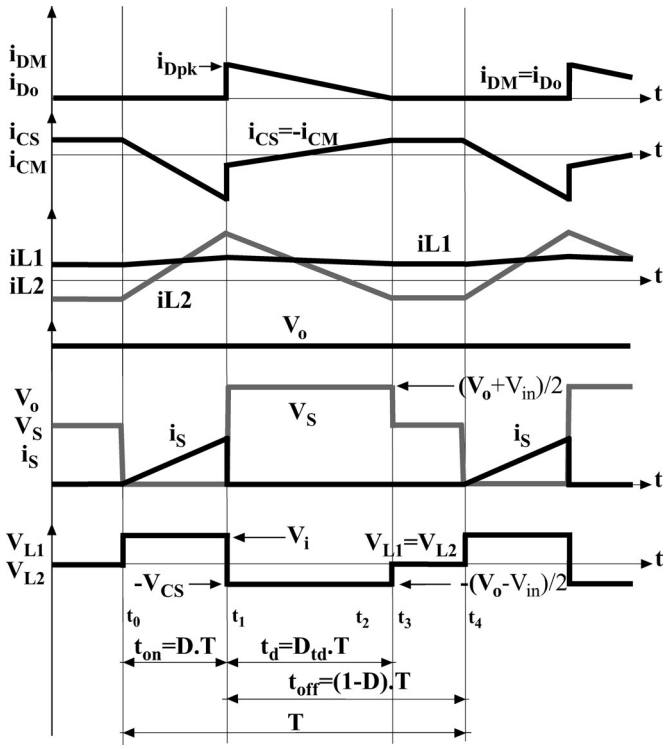

Fig. 7. Main theoretical waveforms.

The operation stages in DCM are presented as follows:

$$V_{C_M} = V_i + V_{C_S}. \tag{1}$$

1) First Stage [$t_0 - t_1$] (see Fig. 4): During the conduction of the power switch *S*, the input inductor stores energy with the input voltage applied across L_1 (V_{L_1}). The voltage applied across L_2 (V_{L_2}) is equal to the voltage of capacitor C_M minus the voltage of capacitor C_S. As presented in (1), this voltage difference is equal to the input voltage. Therefore, inductors L_1 and L_2 store energy in this operation stage and the same voltage is applied across these inductors. The currents through inductors L_1 and L_2 increase following (3) and (4), respectively, but since L_2 is lower than L_1, the current variation in L_2 is higher than in L_1, as presented in the theoretical waveforms shown in Fig. 7. The diodes D_M and D_o are blocked during this operation stage

$$V_{L_1} = V_{L_2} = V_i \tag{2}$$

$$\Delta i_{L_1} = \frac{V_i \cdot D}{L_1 \cdot f} \tag{3}$$

$$\Delta i_{L_2} = \frac{V_i \cdot D}{L_2 \cdot f} \tag{4}$$

where *f* is the switching frequency and *D* is the converter duty cycle.

2) Second Stage [$t_1 - t_2$] (see Fig. 5): At the instant t_1, switch *S* is turned off and the energy stored in the input inductor L_1 is transferred to the output through the C_S capacitor and output diode D_o. There is also energy transference to C_M capacitor through diode D_M and the maximum switch voltage is equal to the C_M capacitor voltage. The energy stored in inductor L_2 is also transferred to the output and capacitor C_S through diodes D_o and D_M. The voltage applied across L_1 is equal to C_M capacitor voltage minus the input voltage and this difference is equal to the C_S capacitor voltage as calculated by (1). The voltage across the inductor L_2 is equal to the negative capacitor C_S voltage. Thus, the voltage applied across the inductor L_1 and L_2 are equal to the negative capacitor C_S voltage during this operation stage and the inductor current variation is calculated by (6) and (7), respectively.

As presented in Fig. 7, the time interval (t_2–t_1) of the second operation stage is defined as t_d and is equal to the transference period of the energy stored in inductors L_1 and L_2 through diodes D_o and D_M. When L_2 current value becomes equal to L_1 current value with the same direction, the currents at diodes D_o and D_M becomes null, finishing this operation stage. Therefore, t_d is the conduction time of diodes D_M and D_o, when the energy stored in the inductors L_1 and L_2 is transferred

$$V_{L_1} = V_{L_2} = -V_{C_S} \tag{5}$$

$$-\Delta i_{L_1} = \frac{-V_{C_S} \cdot D_{t_d}}{L_1 \cdot f} \tag{6}$$

$$-\Delta i_{L_2} = \frac{-V_{C_S} \cdot D_{t_d}}{L_2 \cdot f} \tag{7}$$

where

$$D_{t_d} = \frac{t_d}{T} = t_d \cdot f. \tag{8}$$

3) Third Stage [$t_3 - t_4$] (see Fig. 6): When diodes D_o and D_M are blocked at the instant t_3, the voltage applied across the inductors L_1 and L_2 are null, maintaining the inductors currents constant as presented in (9) and (10). The currents through the inductors L_1 and L_2 present the same value, operating as a freewheeling stage. This operation stage is finished when the power switch is turned on at the instant t_4, returning to the first operation stage

$$V_{L_1} = V_{L_2} = 0 \tag{9}$$

$$\Delta i_{L_1} = \Delta i_{L_2} = 0. \tag{10}$$

The main theoretical waveforms are presented in Fig. 7. The switch turn-on occurs with ZCS such as a classical dc–dc converter operating in DCM and the diodes do not present reverse recovery current. The maximum switch voltage is equal to the capacitor C_M voltage, and this voltage is lower than the output voltage. The L_1 inductor average current is equal to the input current and the L_2 inductor average current is equal to the output current. The average current in the capacitors C_S and C_M are null at steady state; thus, the average current of diodes D_M and D_o are equal to the output current.

III. Mathematical Analysis Operating as a DC–DC Converter

The main equations of the modified SEPIC converter, operating in DCM as a dc–dc converter with constant input voltage V_i are presented. Subsequently, a design procedure operating as preregulator with ac input voltage is presented based on the established equations.

A. Converter Static Gain and the Capacitors C_S and C_M Voltages

The output voltage is equal to the sum of the C_S and C_M capacitors voltages, as observed at the second operation stage presented in Fig. 5 and the C_M voltage is calculated as follows:

$$V_{C_M} = V_o - V_{C_S}. \tag{11}$$

Replacing (1) in (11), the voltage across the capacitor C_S is obtained and presented as follows:

$$V_{C_S} = \frac{V_o - V_i}{2}. \tag{12}$$

Replacing (1) in (12), the voltage across the capacitor C_M is obtained and presented as follows:

$$V_{CM} = \frac{V_o + V_i}{2}. \tag{13}$$

The maximum switch voltage for the classical SEPIC converter is equal to the sum of the input and output voltages, while the switch voltage is equal to the output voltage for the boost converter. The maximum switch voltage of the modified SEPIC converter is equal to the voltage across the C_M capacitor calculated by (13). The voltage obtained from (13) for the modified SEPIC converter is always lower than the switch voltage of the classical boost and SEPIC converters because the input voltage is always lower than the output voltage in the modified SEPIC converter.

Considering the operation at steady state and the average voltage across the inductors as equal to zero, the theoretical waveforms presented in Fig. 7 shows that the positive area of the inductor voltage must be equal to the negative area as presented in (14) for the inductor L_1. The converter duty cycle is equal to *D* and D_{t_d} is the ratio between the diodes D_M and D_o conduction period t_d and the switching period *T*, as presented in (8)

$$V_i \cdot D \cdot T = (V_{C_M} - V_i) \cdot D_{t_d} \cdot T. \tag{14}$$

The voltage across the C_M capacitor is obtained from (14)

$$\frac{V_{C_M}}{V_i} = 1 + \frac{D}{D_{t_d}}. \tag{15}$$

Replacing (13) in (15), the converter static gain is obtained

$$\frac{V_o}{V_i} = 1 + \frac{2 \cdot D}{D_{t_d}}. \tag{16}$$

The C_S capacitor voltage is obtained from (12) and (16)

$$\frac{V_{C_S}}{V_i} = \frac{D}{D_{t_d}}. \tag{17}$$

The conduction period of the diodes t_d and the parameter D_{t_d} must be calculated for the static gain determination. As presented in Fig. 7, the currents at the diodes D_M and D_o are equal and the average value is equal to the output current I_o. The current I_o can be calculated by (18), where I_{Dpk} is the peak value of the current conducted by the diodes D_M and D_o

$$I_o = \frac{I_{\mathrm{Dpk} \cdot D_{t_d}}}{2}. \tag{18}$$

The peak current at the output diode is equal to half of the sum of the inductors L_1 and L_2 current ripple, calculated as follows:

$$I_{\mathrm{Dpk}} = \frac{\Delta_{L_1} + \Delta_{L_2}}{2}. \tag{19}$$

Replacing (3) and (4) in (19), the output diode peak current is equal to

$$I_{\mathrm{Dpk}} = \frac{1}{2} \cdot \left(\frac{V_i \cdot D}{L_1 \cdot f} + \frac{V_i \cdot D}{L_2 \cdot f} \right). \tag{20}$$

Therefore

$$I_{\mathrm{Dpk}} = \frac{V_i \cdot D}{2 \cdot L_{\mathrm{eq}} \cdot f} \tag{21}$$

where

$$L_{\mathrm{eq}} = \frac{L_1 \cdot L_2}{L_1 + L_2}. \tag{22}$$

Replacing (21) in (18), the conduction period of the output diode is obtained, presented as follows:

$$D_{t_d} = \frac{4 \cdot I_o \cdot L_{\mathrm{eq}} \cdot f}{V_i \cdot D}. \tag{23}$$

Considering

$$K = \frac{4 \cdot I_o \cdot L_{\mathrm{eq}} \cdot f}{V_i}. \tag{24}$$

The conduction period of the output diode is equal to

$$D_{t_d} = \frac{K}{D}. \tag{25}$$

Hence, the static gain and the voltage across the capacitors C_M and C_S are calculated by (26), (27), and (28)

$$\frac{V_o}{V_i} = 1 + \frac{2 \cdot D^2}{K} \tag{26}$$

$$\frac{V_{C_M}}{V_i} = 1 + \frac{D^2}{K} \tag{27}$$

$$\frac{V_{C_S}}{V_i} = \frac{D^2}{K}. \tag{28}$$

B. Limit for the DCM operation

The design procedure of the converter must ensure the operation only in DCM for any line voltage angle and in all operation conditions in order to maintain the HPF operation. The operation in CCM without current-control loop results in input current distortion increasing the total harmonic distortion (THD).

The conduction period of the power switch is represented by the interval $(t_1 - t_0)$ in Fig. 7 and also by the converter duty cycle ($D{\cdot}T$). The conduction period of the output diode is defined by the interval $(t_2 - t_1)$ and by the parameter ($D_{t_d}T$). The limit for the DCM operation occurs when the sum of the switch conduction period and the diode conduction period is equal to the switching period (T), presented as follows:

$$D + D_{t_d} \leq 1. \tag{29}$$

Replacing the parameter D_{t_d} from (17) in (29), the maximum duty cycle for the DCM operation is obtained and presented as follows:

$$D \leq \frac{V_{C_S}}{V_{C_S} + V_i}. \tag{30}$$

Also, considering the voltage across the capacitor C_S calculated by (12) and replacing in (30), the maximum switch duty cycle as a function of the input and output voltage is obtained

$$D \leq \frac{V_o - V_i}{V_o + V_i}. \tag{31}$$

As presented in [11], the static gain of the modified SEPIC converter operating in CCM (q_{CCM}) is calculated by

$$q_{\mathrm{CCM}} = \frac{V_o}{V_i} = \frac{1 + D}{1 - D}. \tag{32}$$

The duty cycle obtained from (32) is equal to the value calculated by (31) because at the boundary of the conduction modes, the static gain obtained with the converter operating in DCM presents the same value obtained with the CCM equation.

The value of the equivalent inductance (L_{eqcrit}) for the boundary of CCM and DCM operation is obtained replacing (23) in (29) and is presented in (33) using the duty cycle calculated by (31). This inductance can also be calculated by (34) as a function of the input and output voltage, replacing (31) in (33)

$$L_{\mathrm{eqcrit}} = \frac{(1 - D) \cdot D \cdot V_i}{4 \cdot f \cdot I_o} \tag{33}$$

$$L_{\mathrm{eqcrit}} = \frac{(V_o - V_i) \cdot V_i^2}{(V_o + V_i)^2 \cdot 2 \cdot f \cdot I_o}. \tag{34}$$

TABLE I
DESIGN SPECIFICATIONS

Parameter	Preregulator with Modified SEPIC Converter
Nominal input voltage ($V_{i\mathrm{rms}}$)	$V_{i\mathrm{rms}} = 127\,\mathrm{V}$
Peak value of input voltage (V_{pk})	$V_{\mathrm{pk}} = 180\,\mathrm{V}$
Output voltage (V_o)	$V_o = 400\,\mathrm{V}$
Output power (P_o)	$P_o = 100\,\mathrm{W}$
Switching frequency (f)	30 kHz
Line frequency (f_L)	$f_L = 60\,\mathrm{Hz}$
Maximum input current ripple	$\Delta i_L = 26\%$ of the input peak current

IV. DESIGN PROCEDURE OF THE PREREGULATOR

Considering the mathematical analysis developed, a design example of the preregulator proposed is presented considering the specification in Table I.

The preregulator input voltage is presented in (35). Since the third-harmonic distortion at the preregulator input is relatively low with an rms input voltage equal to 127 V and an output voltage equal to 400 V, some results are also presented with an rms input voltage equal to 220 V

$$V_i(\omega t) = V_{\mathrm{pk}} \cdot \sin(\omega t). \tag{35}$$

A. Limit of the DCM Operation and the Nominal Duty Cycle

The maximum duty cycle for the DCM operation is calculated by (31). The peak value of the ac input voltage must be considered in the equation of the maximum duty cycle

$$D \leq \frac{V_o - V_{\mathrm{pk}}}{V_o + V_{\mathrm{pk}}} \leq \frac{400 - 180}{400 + 180} = 0.379. \tag{36}$$

Therefore, a duty cycle equal to $D = 0.337$ is used for the converter operation at the nominal input voltage.

B. Inductors L_1 and L_2

The input inductance L_1 is calculated by (3) with the specification of the maximum input current ripple (Δi_L). The peak of the input current (I_{inpk}) is calculated by (37) and considering the input current ripple Δi_L presented in Table I and a theoretical efficiency equal to 96%, the input inductor can be calculated by (39)

$$I_{\mathrm{inpk}} = \frac{P_o}{\eta \cdot V_{\mathrm{irms}}} \cdot \sqrt{2} = \frac{100}{0.96 \cdot 127} \cdot \sqrt{2} = 1.157\,\mathrm{A} \tag{37}$$

$$\Delta i_L = I_{\mathrm{inpk}} \cdot 0.26 = 0.3\,\mathrm{A}. \tag{38}$$

Therefore, the input inductance L_1 obtained from (3) is equal to

$$L_1 = \frac{V_{pk} \cdot D}{\Delta i_L \cdot f} = \frac{180 \times 0.337}{0.3 \times 30 \times 10^3} = 6.72 \text{ mH}. \quad (39)$$

An input inductance equal to $L_1 = 6.8\,\text{mH}$ was used in the prototype.

Considering the operation as a rectifier, the average value of the output diode current ($I_o(\omega t)$) calculated in each switching period, changes with the ac input voltage and is calculated by (40), obtained from (23)

$$I_o(\omega t) = \frac{V_{\text{pk}} \cdot \sin(\omega t) \cdot D \cdot D_{t_d}(\omega t)}{4 \cdot L_{\text{eq}} \cdot f}. \quad (40)$$

Replacing the parameter $D_{t_d}(\omega t)$ by (17) and (12), the average value of the output diode current is calculated as follows:

$$I_o(\omega t) = \frac{(V_{\text{pk}} \cdot \sin(\omega t) \cdot D)^2}{2 \cdot L_{\text{eq}} \cdot f \cdot (V_o - V_{\text{pk}} \cdot \sin(\omega t))}. \quad (41)$$

The dc load current (I_o), after the output filter capacitor, is equal the average value of $I_o(\omega t)$ presented as follows:

$$I_o = \frac{1}{\pi} \int_0^{\pi} I_o(\omega t) \cdot d\omega t = \frac{V_{\text{pk}} \cdot D^2}{2 \cdot \pi \cdot L_{\text{eq}} \cdot f} \times \int_0^{\pi} \frac{\alpha \cdot \sin(\omega t)^2}{1 - \alpha \cdot \sin(\omega t)} \cdot d\omega t \quad (42)$$

where

$$\alpha = \frac{V_{\text{pk}}}{V_o} = \frac{180}{400} = 0.45. \quad (43)$$

Solving the integral presented in (42), the dc-load current is equal to

$$I_o = \frac{V_{\text{pk}} \cdot D^2}{2 \cdot \pi \cdot L_{\text{eq}} \cdot f} \cdot K_i \quad (44)$$

where

$$K_i = \left[-2 - \frac{\pi}{\alpha} + \frac{2}{\alpha \cdot \sqrt{1-\alpha^2}} \cdot \left[\frac{\pi}{2} + \tan^{-1}\left(\frac{\alpha}{\sqrt{1-\alpha^2}}\right)\right]\right] = 1.159. \quad (45)$$

Therefore, the equivalent inductance L_{eq} is calculated by (46) and the inductor L_2 is calculated by (47)

$$L_{\text{eq}} = \frac{V_{\text{pk}} \cdot D^2}{2 \cdot \pi \cdot f \cdot (P_o/V_o)} \cdot K_i = \frac{180 \times 0.337^2}{2\pi \times 30 \times 10^3 \times (100/400)} \times 1.159 = 500.28\,\mu\text{H} \quad (46)$$

$$L_2 = \frac{L_1 \cdot L_{\text{eq}}}{L_1 - L_{\text{eq}}} = \frac{6.8 \times 10^{-3} \times 500 \times 28 \times 10^{-6}}{6.8 \times 10^{-3} - 500 \times 28 \times 10^{-6}} = 543.4\,\mu\text{H}. \quad (47)$$

An L_2 inductance equal to 540 μH was used in the prototype.

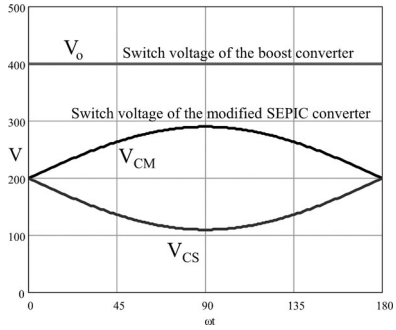

Fig. 8. Capacitors C_S and C_M voltages operating as preregulator.

C. Capacitors C_S and C_M

The voltages across the capacitors C_S and C_M calculated by (12) and (13) change with the ac input voltage and are presented in Fig. 8, considering the voltage ripple across the capacitors null. The voltage across the C_S and C_M capacitors are equal to 110 and 290 V, respectively, at the peak of the input voltage. The switch voltage is equal to the C_M capacitor voltage and lower than the output voltage.

In the classical SEPIC and in the modified SEPIC converters, the theoretical capacitors voltage are considered constant in a switching period. However, as presented in Fig. 8, the capacitors voltages follow the line voltage variation in the operation as preregulator. Therefore, the values of the capacitors must be high enough to be considered a voltage source during a switching period but not too large in order to follow the line input voltage variation without distortion in the preregulator input current. In order to comply with these requirements, a design methodology considering the converter resonance frequency is presented in [3].

The converter resonant frequency must be considerably greater than the line frequency to avoid input current oscillations at every line half cycle. Also, the converter resonant frequency must be lower than the switching frequency to assure almost constant voltage in a switching period.

Considering a converter resonance frequency equal to $f_R = 5.5$ kHz and the same value for the capacitors C_S and C_M, the capacitor value is calculated by

$$C_S = C_M = \frac{2}{(2 \cdot \pi \cdot f_R)^2 \cdot (L_1 + L_2)} = \frac{2}{(2 \cdot \pi \cdot 5.5 \times 10^3)^2 \cdot (6.8 \times 10^{-3} + 0.54 \times 10^{-3})} = 228.2\,\text{nF}. \quad (48)$$

A capacitance equal to $C_S = C_M = 220$ nF was used in the prototype.

The rms current through C_M and C_S capacitors are calculated considering that the minimum current during each switching period at the L_1 inductance $I_{i\min}(\omega t)$ (49). The parameter $D_{t_d}(\omega t)$ and the output diode maximum current $I_{\text{Dpk}}(\omega t)$ (50) are modulated by the sinusoidal input voltage $V_i(\omega t)$. The number of commutations during one semicycle of line voltage can

be calculated by

$$I_{i\min}(\omega t) = \frac{\sqrt{2}}{0.9}\cdot\left(\frac{P_o}{V_i}-\frac{V_i\cdot D}{2\cdot L_1}\right)\cdot\sin(\omega t) \tag{49}$$

$$I_{\mathrm{Dpk}}(\omega t) = \frac{\sqrt{2}}{0.9}\cdot\frac{2\cdot I_o}{D_{t_d}(\omega t)}\cdot\sin(\omega t) \tag{50}$$

$$n = \frac{1}{2\cdot f_L\cdot T} \tag{51}$$

where f_L is the line frequency and T is the high-frequency switching period.

The rms capacitor current value at each switching cycle can be calculated by (52), shown at the bottom of the page, considering the parameter (i) changing from 1 to n as (52), where

$$A = I_{i\min}\left(\frac{\pi\cdot i}{n}\right)-\frac{V_i(\pi\cdot i/n)}{L_2}\cdot t \tag{53}$$

$$B = I_{i\min}(\pi\cdot i/n)-\frac{V_i(\pi\cdot i/n)\cdot D}{L_2\cdot f}\cdot t + I_{\mathrm{Dpk}}(\pi\cdot i/n) + \left[\left(\frac{V_i(\pi\cdot i/n)}{L_2\cdot f}-I_{\mathrm{Dpk}}\left(\frac{\pi\cdot i}{n}\right)\right)\cdot\frac{(t-D\cdot T)}{D_{t_d}(\pi\cdot i/n)\cdot T}\right] \tag{54}$$

$$C = I_{i\min}\left(\frac{\pi\cdot i}{n}\right). \tag{55}$$

Thus, the total rms currents through capacitor C_M and C_S are calculated by

$$I_{C_{M\mathrm{rms}}} = I_{C_{S\mathrm{rms}}} = \sqrt{\frac{1}{n}\cdot\sum_{i=1}^{n}\left[I_{C_{M\mathrm{rms}}}(i)\right]^2} = 0.824\,\mathrm{A}. \tag{56}$$

D. Semiconductors Stress

The maximum voltage in all semiconductors is equal to the C_M capacitor voltage and the average current of the diodes D_M and D_o is equal to the average output current I_o.

The average and rms switch current are calculated by (57) and (58), respectively

$$Is_{\mathrm{avg}} = \frac{V_{\mathrm{pk}}\cdot D^2}{f\cdot\pi\cdot L_{\mathrm{eq}}} = \frac{180\times 0.337^2}{30\times 10^3\times\pi\times 500\times 10^{-6}} = 0.431\,\mathrm{A} \tag{57}$$

$$Is_{\mathrm{rms}} = \frac{V_{\mathrm{pk}}}{f\cdot L_{\mathrm{eq}}}\cdot\sqrt{\frac{D^3}{6}} = \frac{180}{30\times 10^3\times 500\times 10^{-6}}\sqrt{\frac{0.337^3}{6}} = 0.953\,\mathrm{A}. \tag{58}$$

TABLE II
PREREGULATOR PARAMETERS DESIGNED AT THE BOUNDARY OF CCM AND DCM

Boost	SEPIC	Modified SEPIC
Duty cycle D		
$D=\frac{V_o-V_{\mathrm{pk}}}{V_o}$	$D=\frac{V_o}{V_o+V_{\mathrm{pk}}}$	$D=\frac{V_o-V_{\mathrm{pk}}}{V_o+V_{\mathrm{pk}}}$
$D=0.55$	$D=0.689$	$D=0.379$
Inductance for the boundary operation		
$L_{\mathrm{crit}}=\frac{(1-D)\cdot D\cdot V_{\mathrm{pk}}}{2\cdot f\cdot I_o(90^\circ)}$	$L_{\mathrm{eqcrit}}=\frac{(1-D)\cdot D\cdot V_{\mathrm{pk}}}{2\cdot f\cdot I_o(90^\circ)}$	$L_{\mathrm{eqcrit}}=\frac{(1-D)\cdot D\cdot V_{\mathrm{pk}}}{2\cdot f\cdot I_o(90^\circ)}$
$L_{\mathrm{crit}}=1485\,\mu\mathrm{H}$	$L_{\mathrm{eqcrit}}=1286\,\mu\mathrm{H}$	$L_{\mathrm{eqcrit}}=706\,\mu\mathrm{H}$
Switch voltage		
$Vs_{\max}=V_o$	$Vs_{\max}=V_o+V_{\mathrm{pk}}$	$Vs_{\max}=\frac{V_o+V_{\mathrm{pk}}}{2}$
$Vs_{\max}=400\mathrm{V}$	$Vs_{\max}=580\,\mathrm{V}$	$Vs_{\max}=290\,\mathrm{V}$
Switch peak current at the peak of the input voltage		
$\mathrm{is_{pk}}(90^\circ)=\frac{V_{\mathrm{pk}}\cdot D}{L_{\mathrm{crit}}\cdot f}$	$\mathrm{is_{pk}}(90^\circ)=\frac{V_{\mathrm{pk}}\cdot D}{L_{\mathrm{eqcrit}}\cdot f}$	$\mathrm{is_{pk}}(90^\circ)=\frac{V_{\mathrm{pk}}\cdot D}{L_{\mathrm{eqcrit}}\cdot f}$
$\mathrm{is_{pk}}(90^\circ)=2.2\,\mathrm{A}$	$\mathrm{is_{pk}}(90^\circ)=3.21\,\mathrm{A}$	$\mathrm{is_{pk}}(90^\circ)=3.21\,\mathrm{A}$

E. Comparison at the Boundary of the CCM and DCM Operation

Table II presents some parameters calculated considering the operation at the boundary of the CCM and DCM at the peak of the input voltage and considering the nominal specifications presented in Table I, in order to compare the three topologies.

The modified SEPIC converter presents the lowest duty cycle due to the highest static gain. The input current ripple equation for the SEPIC and modified SEPIC converter are the same (39), so the input inductor of the modified SEPIC converter is lower than the input inductor of the SEPIC converter because the duty cycle of the modified SEPIC converter is close to half of the duty cycle of the SEPIC converter. Also, the equivalent inductance of the modified SEPIC converter for the boundary operation and for the same operation point in DCM is lower than in the others topologies.

The modified SEPIC converter presents the lowest switch voltage. The boost converter presents the lowest switch peak current, and the SEPIC and modified SEPIC converters present the same peak current but with a lowest switch conduction time for the modified SEPIC converter.

V. THIRD-HARMONIC REDUCTION TECHNIQUE

The classical boost rectifier operating in DCM and the modified SEPIC rectifier present a third-harmonic distortion in the input current. This current distortion is a function of the voltage difference between the input and output voltage. Normally, the output voltage is increased in order to reduce the third-harmonic distortion and to maintain HPF, but the semiconductors losses are increased.

$$I_{C_{M\mathrm{rms}}}(i) = \sqrt{\frac{1}{T}\cdot\left[\int_0^{D\cdot T}A^2\cdot dt + \int_{D\cdot T}^{\left[D+D_{t_d}\left(\frac{\pi\cdot i}{n}\right)\right]\cdot T}B^2\cdot dt + \int_{\left[D+D_{t_d}\left(\frac{\pi\cdot i}{n}\right)\right]\cdot T}^{T}C\cdot dt\right]} \tag{52}$$

In order to reduce the third-harmonic distortion without increasing the output voltage, an open-loop control action for the classical boost converter with analog implementation was presented in [13]. Only the information of the input and output voltage are necessary to define a duty-cycle variation in a line voltage half period, reducing the third-harmonic distortion even for a relatively low output voltage.

The same open-loop technique is developed in this paper for the modified SEPIC converter using a digital implementation, obtaining HPF.

Considering by simplification that the converter operates without losses, the input power is equal to the output power

$$\begin{aligned} P_i(\omega t) &= P_o(\omega t) = V_{\rm pk} \cdot \sin(\omega t) \cdot I_{i\rm pk} \cdot \sin(\omega t) \\ &= V_o \cdot I_o(\omega t). \end{aligned} \tag{59}$$

Replacing (16) and (41) in (59), the instantaneous input power is calculated by

$$\begin{aligned} &V_{\rm pk} \cdot \sin(\omega t) \cdot I_{i\rm pk} \cdot \sin(\omega t) \\ &= \left[V_{\rm pk} \cdot \sin(\omega t) + \frac{V_{\rm pk} \cdot \sin(\omega t) \cdot 2 \cdot D}{D_{t_d}(\omega t)} \right] \\ &\times \left[\frac{V_{\rm pk} \cdot \sin(\omega t) \cdot D \cdot D_{t_d}(\omega t)}{4 \cdot L_{\rm eq} \cdot f} \right]. \end{aligned} \tag{60}$$

The preregulator input current is calculated by (61) obtained from (60)

$$I_{i\rm pk} \cdot \sin(\omega t) = \frac{V_{\rm pk} \cdot \sin(\omega t)}{4 \cdot L_{\rm eq} \cdot f} \cdot (D_{t_d}(\omega t) + 2 \cdot D) \cdot D. \tag{61}$$

Therefore, the preregulator input current will be sinusoidal if the term $K_{\rm c}$ presented in (62) is constant

$$K_c = (D_{t_d}(\omega t) + 2 \cdot D) \cdot D. \tag{62}$$

The converter duty cycle must be changed in a half cycle of the ac input voltage in order to maintain (62) constant, since the parameter $D_{t_d}(\omega t)$ changes with the input voltage.

Replacing the parameter D_{t_d} calculated by (17) and the V_{C_S} voltage calculated by (12) in (62), the duty-cycle variation is obtained and presented in (63), in order to maintain (62) constant

$$D(\omega t) = \sqrt{\frac{K_c}{2}} \cdot \sqrt{1 - \frac{V_{\rm pk} \cdot \sin(\omega t)}{V_o}}. \tag{63}$$

Therefore, the third-harmonic distortion can be reduced solving (63) requiring solely the measurement of the input and output voltages. The output voltage can be replaced by the output voltage reference in (63), considering the operation at steady state.

The peak of the preregulator input current $I_{i_{\rm pk}}$ is presented as follows:

$$I_{i\rm pk} = \frac{2 \cdot P_o}{V_{\rm pk}} = \frac{V_{\rm pk}}{4 \cdot L_{\rm eq} \cdot f} \cdot K_c = 1.111\ \text{A}. \tag{64}$$

The parameter K_c can be calculated by

$$K_c = \frac{8 \cdot P_o \cdot L_{\rm eq} \cdot f}{V_{\rm pk}^2}$$

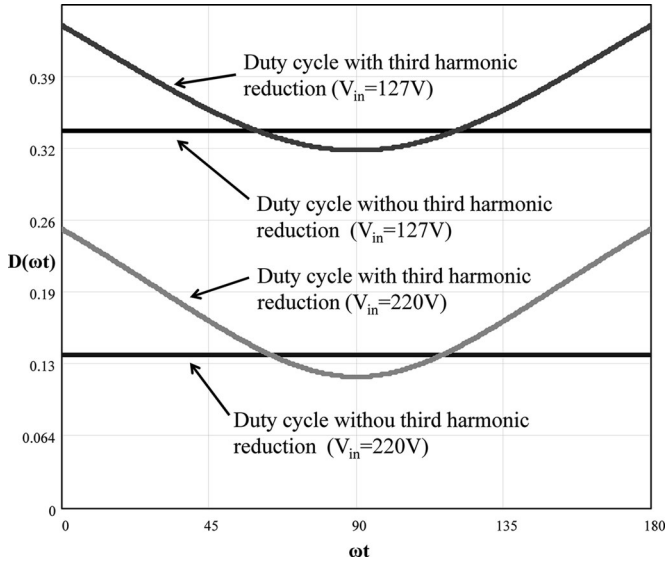

Fig. 9. Duty-cycle variation in a half line period with and without the reduction of the third-harmonic distortion.

$$K_c = \frac{8 \times 100 \times 500 \times 28 \times 10^{-6} \times 30 \times 10^3}{180^2} = 0.372. \tag{65}$$

The parameter K_c should be calculated at each half cycle of the ac input voltage because this parameter is a function of the peak of the input voltage $V_{\rm pk}$ and also changes with the output current. However, a constant value for the parameter K_c can be used considering the nominal specifications and the duty-cycle variation calculated by (63) can be multiplied by the output voltage control loop. The preregulator duty cycle obtained by multiplying the output voltage control loop and the value calculated by (63) with constant value for the parameter K_c, regulates the output voltage and allows the reduction of the third-harmonic distortion with the correct gain.

The variation of the main rectifier parameters with the input voltage as the duty cycle, conduction period of the output diode, input current, and the average value of the output diode current are presented for the operation with and without the third-harmonic reduction technique.

The duty-cycle variation calculated by (63), considering the nominal values presented in Table I and the components calculated at the design procedure, is shown in Fig. 9.

The output diode conduction period D_{t_d}, considering the operation with a constant duty cycle and with the variable duty cycle calculated by (63), are presented in Fig. 10.

Changing the preregulator duty cycle D as calculated by (63), the output diode conduction period D_{t_d} calculated by (17) also changes. Replacing these two parameters in the input current equation [see (61)], the theoretical input current waveform is obtained, considering the inductor current ripple null. Fig. 11 presents the preregulator theoretical input current waveform operating with and without the third-harmonic reduction technique. The theoretical input current waveform is improved mainly for preregulator operation with the highest value of the

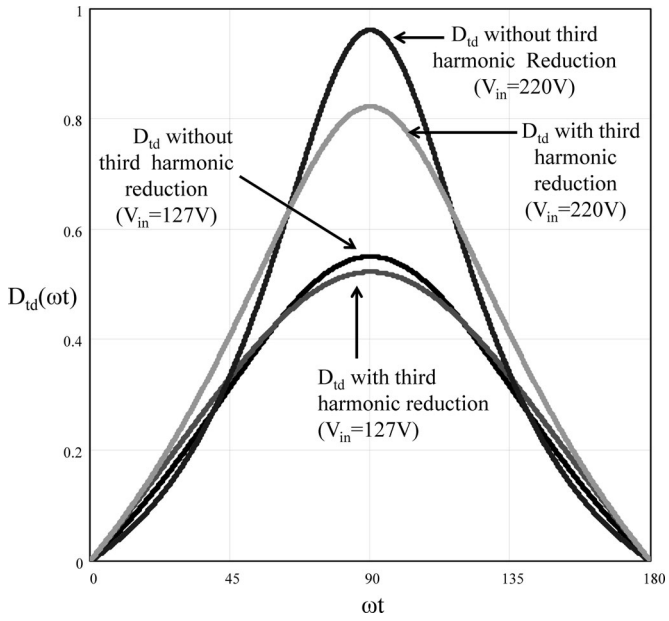

Fig. 10. Output diode conduction period D_{t_d} operating with constant duty cycle and with a variable duty cycle with third-harmonic reduction.

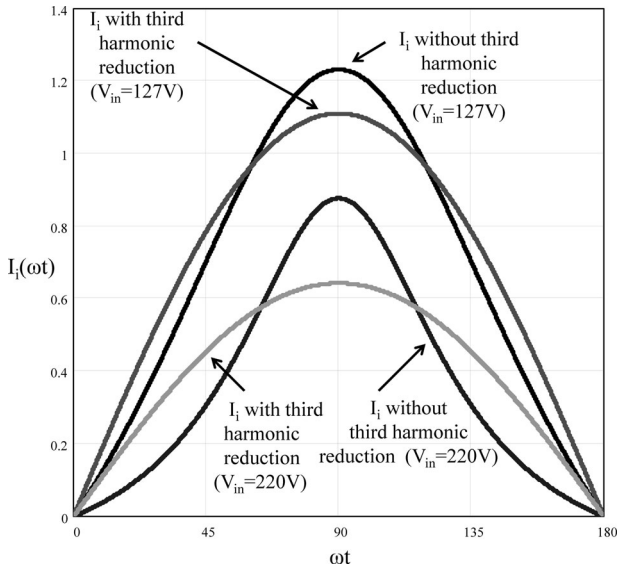

Fig. 11. Preregulator theoretical input current waveform with and without the third-harmonic reduction.

input voltage (220 V), where the third-harmonic distortion is more expressive.

The average value of the output diode current is presented in Fig. 12.

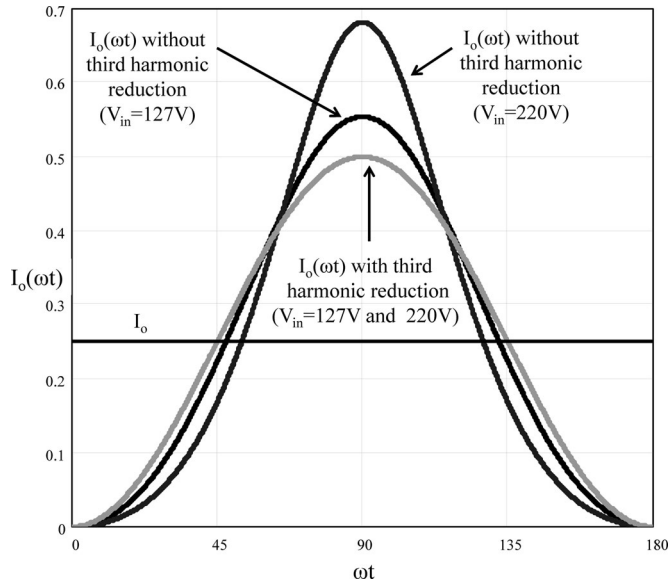

Fig. 12. Output diode average current $I_o(\omega t)$ and the dc output current (I_o) waveforms with and without the third-harmonic reduction.

TABLE III
THEORETICAL POWER FACTOR AND TOTAL HARMONIC CURRENT DISTORTION

Input voltage	127 V		220 V	
Control	With third-harmonic reduction	Without third-harmonic reduction	With third-harmonic reduction	Without third-harmonic reduction
$I_{i\mathrm{rms}}$	0.786 A	0.79 A	0.455 A	0.474 A
PF	1	0.996	1	0.959
THD_i	0%	8.845%	0%	29.65%

The theoretical waveform of the output diode average current is equal for the operation with input voltage equal to 127 and 220 V with the third-harmonic reduction technique.

The theoretical rectifier power factor (PF) and the input current total harmonic distortion (THD_i) can be calculated by (67) and (68), respectively, from the theoretical input current waveform presented in Fig. 11, considering the input current rms value (66), shown at the bottom of the page. Results with the input voltage equal to 127 and 220 V are summarized in Table III

$$\mathrm{PF} = \frac{P_o}{V_{i\mathrm{rms}} \cdot I_{i\mathrm{rms}}} \tag{67}$$

$$\mathrm{THD}_i(\%) = 100 \times \sqrt{\frac{1}{\mathrm{PF}^2} - 1}. \tag{68}$$

$$I_{i\mathrm{rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\frac{V_{\mathrm{pk}} \cdot \sin(\omega t)}{4 \cdot L_{\mathrm{eq}} \cdot f} \cdot \left(D_{t_d}(\omega t) + 2 \cdot D(\omega t)\right) \cdot D(\omega t)\right)^2 \cdot d\omega t} \tag{66}$$

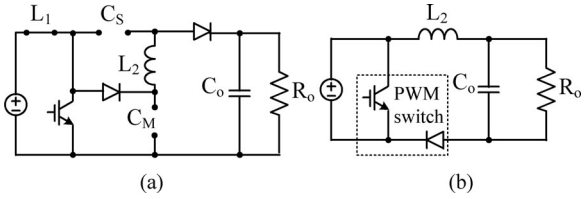

Fig. 13. Simplified circuit model of modified SEPIC dc–dc: (a) with neglected components and (b) equivalent circuit.

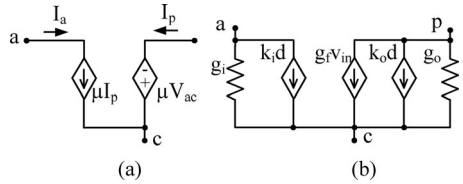

Fig. 14. Model of PWM switch in DCM: (a) average model and (b) small-signal model.

VI. Output Voltage Control System

A. Control-to-Output Transfer Function [$v_o(s)/d(s)$]

A dynamic model of switching converter is required for feedback control loop. However, the power converters are described by a set of the nonlinear differential equations. Usually, it is easier to analyze a small signals model that is linearized related to the quiescent operation point in order to obtain a linear model, as presented in [15].

The small signal equivalent circuit of buck, boost, and buck–boost converters presents a capacitor and an inductor, operating in DCM. The transfer functions have two poles. One pole is due to the output capacitor, at low frequency, and other pole, in much higher frequency due to the inductor. For this reason, an approximate way to determine the low-frequency small-signal transfer function of the basics converters is to let the inductance tend to zero [15].

Also, the capacitor C_M and C_S are very small in the modified SEPIC converter, where $C_o >> C_M$ and $C_o >> C_S$. Therefore, they can be neglected to obtain control-to-output transfer function for low frequency. In this case, the high-frequency capacitors dynamics can be ignored. The modified SEPIC without C_M, C_S, and L_1 is shown in Fig. 13(a) and the equivalent circuit is shown in Fig. 13(b). The remaining model is solved for the low-frequency converter dynamics.

To perform this analysis, the model of the pulsewidth-modulated (PWM) switch in DCM proposed in [16] is used considering the equivalent circuit presented in Fig. 13(b). The equivalent circuit of an average model and small-signal model of PWM switch in DCM is shown in Fig. 14.

Transfer function is obtained considering a resistive load. The model of the PWM switch in DCM is replaced in the modified SEPIC converter and the input voltage is shortened. Fig. 15 shows the equivalents circuits. Here

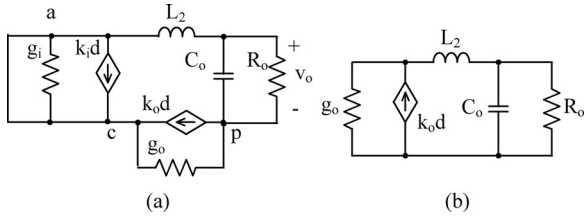

Fig. 15. Small-signal equivalent circuit for control-to-output transfer function of modified SEPIC: (a) complete circuit and (b) simplified circuit.

$$g_i = \frac{I_a}{V_{\rm ac}} \tag{69}$$

$$k_i = \frac{2 \cdot I_a}{D} \tag{70}$$

$$k_o = \frac{2 \cdot I_p}{D} \tag{71}$$

$$g_o = \frac{I_p}{V_{\rm cp}} \tag{72}$$

$$g_f = \frac{2 \cdot I_p}{V_{\rm ac}}. \tag{73}$$

The control-to-output transfer functions of the converter can be obtained applying circuit analysis in circuit of Fig. 15(a), and the transfer function is presented in (74) shown at the bottom of the page.

The small-signal parameters are evaluated at the operating point, where $I_p = I_o$ and $V_{\rm cp} = V_o$, as follows:

$$k_o = \frac{2 \cdot I_o}{D} \tag{75}$$

$$g_o = \frac{I_o}{V_o}. \tag{76}$$

Fig. 16 shows the dynamic behavior of the output voltage waveform under duty-cycle disturbances considering the operation as a dc–dc converter. At 0.5 s, a 1% step is applied in the duty cycle. At 1.1 s, the duty cycle returns to its nominal value. The results show good resemblance between the proposed model and the simulation of the converter power circuit. The dynamic response of the proposed converter operating in DCM is an overdamped second-order system with a step response similar to a first-order system.

The modified SEPIC rectifier presents an oscillating input voltage with double-line frequency. On the other hand, a large output capacitor is used to minimize the output voltage ripple. Thus, output voltage does not change significantly in a half-line period and a simplified model can be considered without the input ripple.

$$\frac{V_o(S)}{d(S)} = \frac{R_o \cdot K_o}{(1 + R_o \cdot g_o) + (C_o \cdot R_o + L_2 \cdot g_o) \cdot S + (C_o \cdot R_o \cdot L_2 \cdot g_o) \cdot S^2} \tag{74}$$

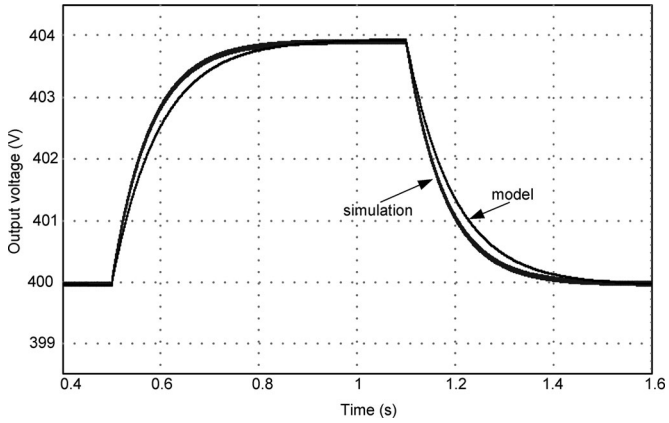

Fig. 16. Comparison of the transient responses of output voltage for a 1% disturbance in the duty cycle for the modified SEPIC operating as a dc–dc converter in DCM.

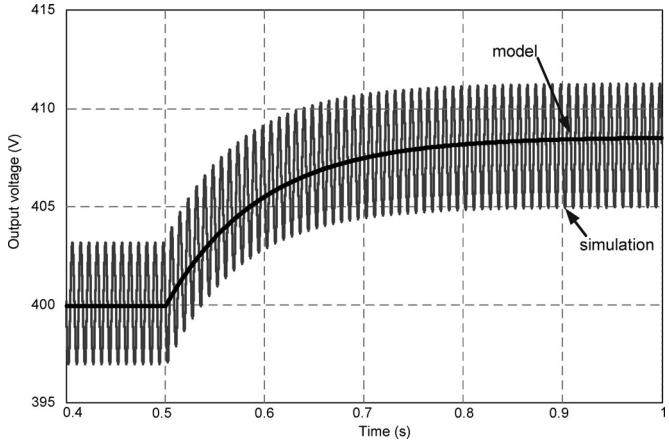

Fig. 17. Comparison of the transient responses of output voltage for a 2% disturbance in the duty cycle for the modified SEPIC operating as a rectifier in DCM.

The simulation result of the modified SEPIC operating as a rectifier and the prediction of the small signal model for a step change in the duty cycle are shown in Fig. 17.

It can be observed that this model gives good results at low frequencies. It cannot accurately predict high-frequency dynamics because C_M, C_S, and L_1 are neglected. However, the output voltage feedback loop in the conventional rectifier control system must have a low bandwidth in order to avoid distortions in the input current waveform. The controller should have sufficiently small loop gain at the even harmonics of the ac line frequency. Therefore, low-frequency small-signal transfer function is appropriate for the control of the modified SEPIC rectifier.

B. Control System

The preregulator operation in DCM allows obtaining HPF without a current-control loop and only a voltage control loop is necessary [14]. The output voltage control algorithm used in the proposed converter is based on the classical PI controller. The design procedure can be simplified using a design procedure

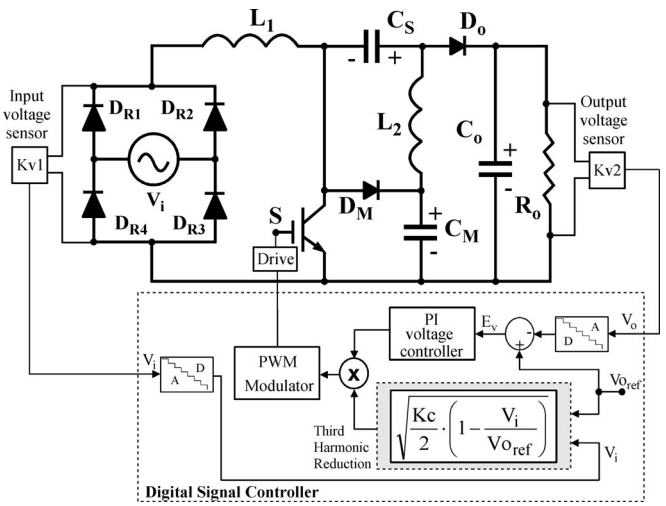

Fig. 18. Block diagram of the preregulator control system.

TABLE IV
PREREGULATOR COMPONENTS

Parameter	Preregulator with modified SEPIC converter
Inductor L_1	$L_1 = 6.8$ mH, ESR $= 692$ mΩ
Inductor L_2	$L_2 = 540$ μH, ESR $= 98$ mΩ
Capacitor C_S	$C_S = 220$ nF, ESR $= 10$ mΩ
Capacitor C_M	$C_M = 220$ nF, ESR $= 10$ mΩ
Output capacitor C_o	$C_o = 120$ μF, ESR $= 390$ mΩ
Diodes $D_M - D_o$	$D_M = D_o =$ UF5408 $V_f = 1.7$V
Power switch S	$S =$ FQA28N50 $V_{DSS} = 500$ V $R_{DSon} = 0.16\Omega$ (25 °C)

similar to the classical boost converter. Also, the 120 Hz ripple of the preregulator output voltage must be rejected by the voltage control loop in order to maintain the HPF operation. Therefore, the voltage control loop presents a very slow dynamic response such as any classical preregulators.

The block diagram of the digital control implementation is presented in Fig. 18, including the third-harmonic reduction technique. Only the output and input voltages are necessary to control the preregulator. The control algorithm was developed using a digital signal processor TMS320F2812, operating with sampling rate equal to 30 kHz. The sampled output voltage signal is compared to an output voltage reference and the error is applied to a PI voltage controller. Simultaneously, the sampled rectified input voltage and the output voltage reference are applied to (63) in order to calculate the duty-cycle variation for the third-harmonic reduction. The result of the PI output voltage controller and the result of the third-harmonic reduction are multiplied obtaining the preregulator duty cycle and generating the PWM signal that controls the switch *S*.

VII. EXPERIMENTAL RESULTS

The proposed preregulator was implemented as presented in Fig. 18 using the specifications presented in Table I, and the components used are shown in Table IV. The preregulator performance is compared with and without the implementation

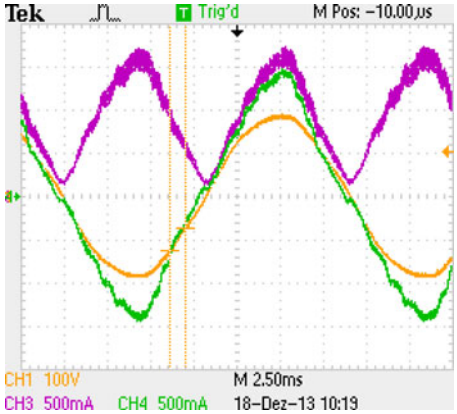

Fig. 19. Input voltage and current operating with $V_i = 127\,V_{\rm rms}$ and without the third-harmonic reduction technique (CH1: input voltage—100 V/div; CH3: L_1 current—0.5 A/div; CH4: input current—0.5 A/div).

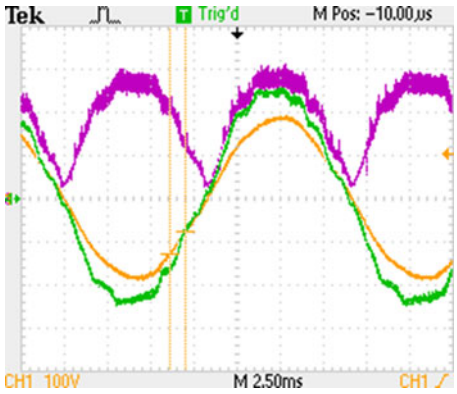

Fig. 20. Input voltage and current operating with $V_i = 127\,V_{\rm rms}$ and with the third-harmonic reduction technique (CH1: input voltage—100 V/div; CH3: L_1 current—0.5 A/div; CH4: input current—0.5 A/div).

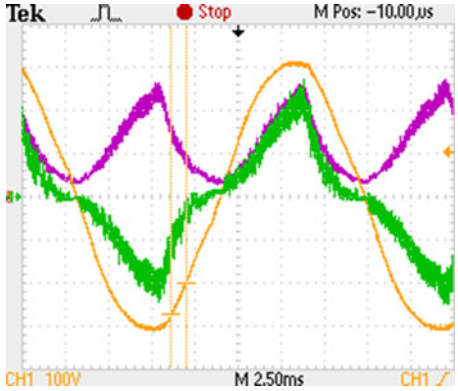

Fig. 21. Input voltage and current operating with $V_i = 220\,V_{\rm rms}$ and without the third-harmonic reduction technique (CH1: input voltage—100 V/div; CH3: L_1 current—0.5 A/div; CH4: input current—0.5 A/div).

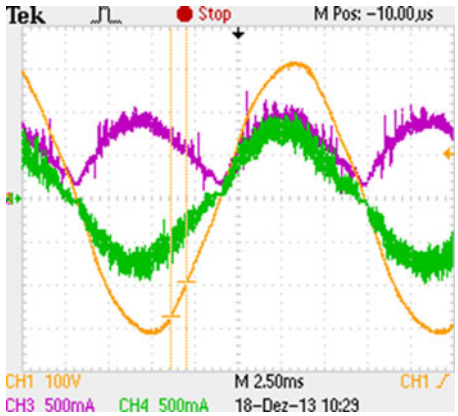

Fig. 22. Input voltage and current operating with $V_i = 220\,V_{\rm rms}$ and with the third-harmonic reduction technique (CH1: input voltage—100 V/div; CH3: L_1 current—0.5 A/div; CH4: input current—0.5 A/div).

of the third-harmonic reduction technique. The waveforms were obtained with nominal output power and input voltage equal to 127 and 220 $V_{\rm rms}$.

The preregulator input current and voltage waveforms, operating with $V_i = 127\,V_{\rm rms}$ and without the third-harmonic distortion reduction technique are presented in Fig. 19.

The total input current harmonic distortion is equal to 13% without the application of the third-harmonic reduction technique and the preregulator power factor is equal to 0.993. The total input voltage harmonic distortion is equal to 3.1%.

The preregulator input current and voltage waveforms, operating with $V_i = 127\,V_{\rm rms}$ and with the third-harmonic distortion reduction technique are presented in Fig. 20. The total input current harmonic distortion is reduced to 5.3% with the application of the third-harmonic reduction technique and the preregulator power factor is increased to 0.999. Considering that the total voltage harmonic distortion is equal to 3.1%, the total input current distortion is 2.2% higher than the total input voltage distortion.

The preregulator input current and voltage waveforms, operating with $V_i = 220\,V_{\rm rms}$ and without the third-harmonic distortion reduction technique are presented in Fig. 21. Reducing the voltage difference between the peak of the input voltage and the output voltage, the third-harmonic distortion increases, operating with constant duty cycle.

The total input current harmonic distortion is equal to 35.9% without the application of the third-harmonic reduction technique and the preregulator power factor is reduced to 0.951.

The preregulator input current and voltage waveforms, operating with $V_i = 220\,V_{\rm rms}$ and with the third-harmonic distortion reduction technique are presented in Fig. 22.

The total input current harmonic distortion is reduced from 35.9% to 8.84% with the application of the third-harmonic reduction technique and the preregulator power factor is increased from 0.951 to 0.988. The total input current distortion is 5.74% higher than the total input voltage distortion.

The preregulator operation with nominal output power and input voltage equal to $V_i = 127\,V_{\rm rms}$ are presented from Figs. 23 to 30, considering the operation with the third-harmonic reduction technique.

The L_1 and L_2 currents are presented in Fig. 23 and its current ripple is close to the theoretical values 0.3 and 3.56 A, respectively.

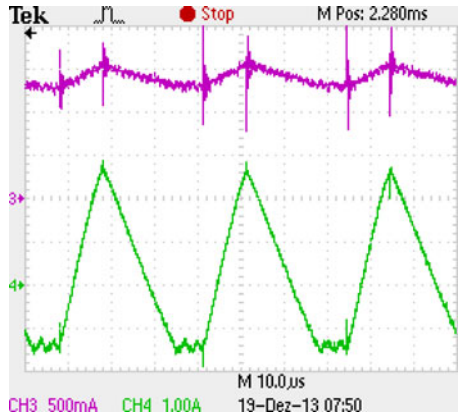

Fig. 23. L_1 and L_2 currents (CH3: L_1 current—0.5 A/div; CH4: L_2 current—1 A/div).

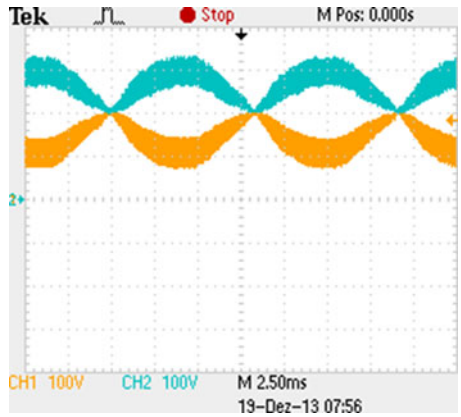

Fig. 24. C_S and C_M capacitor voltages (CH1: C_S voltage—100 V/div; CH2: C_M voltage—100 V/div).

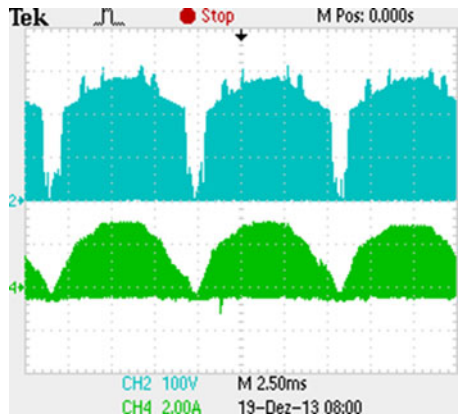

Fig. 25. Switch voltage and current (CH2: switch voltage—100 V/div; CH4: switch current—2 A/div, 2.5 ms/div).

The C_S and C_M capacitor voltages are presented in Fig. 24. The theoretical value of the C_S and C_M capacitor voltages at the peak of the input voltage, considering the capacitor voltage ripple null, is equal to 110 and 290 V, respectively.

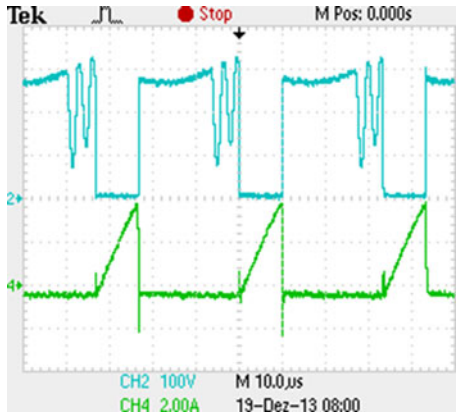

Fig. 26. Switch voltage and current (CH2: switch voltage—100 V/div; CH4: switch current—2 A/div, 10 μs/div).

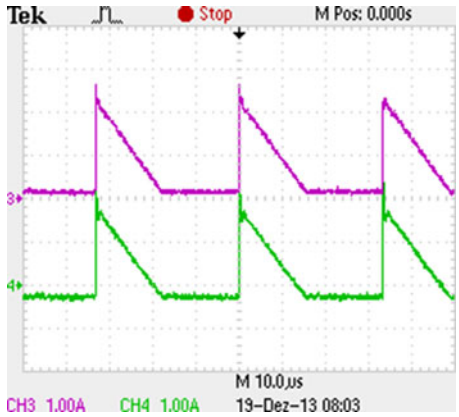

Fig. 27. Currents in the diodes D_M and D_o (CH3: D_M current—1 A/div; CH4: D_o current—1 A/div).

The switch voltage and current are presented in Figs. 25 and 26. The maximum switch voltage is close to 300 V for an input voltage equal 127 $V_{\rm rms}$ and output voltage equal to 400 V.

The currents in the diodes D_M and D_o are presented in Fig. 27. The theoretical diode peak current is equal to 2 A, and the theoretical value of the diode conduction period is equal to $t_d = 17.45$ μs at the peak of the input voltage.

The PWM modulation signal obtained from the product of the voltage control loop and the third-harmonic reduction technique, as presented in Fig. 18, was applied to a digital to analog converter of the digital controller and is presented in Fig. 28 operating with $V_i = 127\,V_{\rm rms}$ and $V_i = 220\,V_{\rm rms}$. The voltage variation from 0 to 1 V corresponds to the duty-cycle variation from 0 to 1. The modulation signal obtained from the prototype is similar to the theoretical result presented in Fig. 9.

The dynamic response of the preregulator is presented in Figs. 29 and 30 for $V_i = 127\,V_{\rm rms}$. Fig. 29 shows the dynamic response of the converter during the load change from 100% to 30%, and Fig. 30 presents the load transient from 30% to 100%.

The theoretical efficiency of the proposed converter operating with a rms input voltage equal 127 V has been estimated

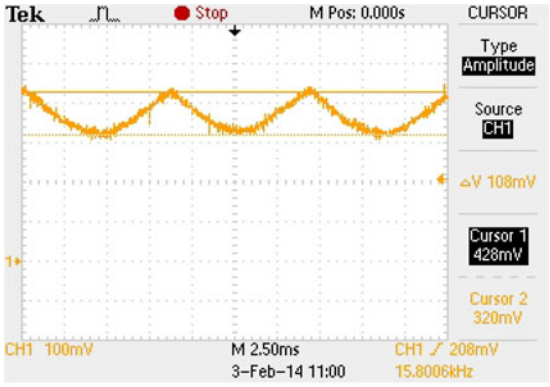

Fig. 28. PWM modulation signal (a) $V_i = 127$ V and (b) $V_i = 220$ V.

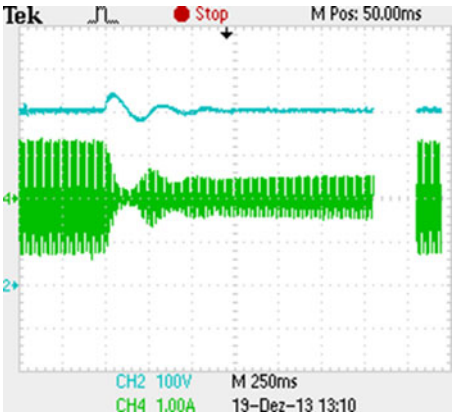

Fig. 29. Load change from 100% to 30% (CH2: output voltage—100 V/div; CH4: input current—1 A/div, 250 ms/div).

considering the component parameters used in the prototype shown in Table IV.

Considering the rms switch current calculated by (58) and the $\mathrm{RDS_{on}}$ MOSFET with resistance equal 240 mΩ (at 80 °C), the switch conduction loss is equal to 0.22 W.

The average current in the D_M and D_o diodes are equal to the output current and considering the diode UF5408 (3A-800 V)

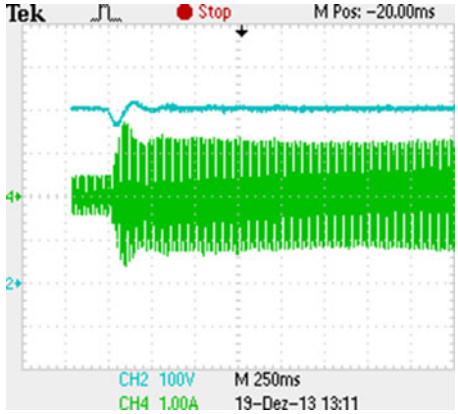

Fig. 30. Load change from 30% to 100% (CH2: output voltage—100 V/div; CH4: input current—1 A/div, 250 ms/div).

used in the prototype with a diode forward voltage equal to 1.7 V, the D_M and D_o diodes total conduction losses is equal to 0.85 W.

The average current in the input bridge diodes is equal to 0.37 A, and the total conduction losses of input diode bridge is equal to 2.52 W. Therefore, the estimated theoretical efficiency of the proposed converter is equal to 95.6% considering the total losses of the inductors equal to 1 W. The classical boost converter presents similar losses in all components. However, there is only one diode in the converter output, reducing the diode conduction losses in 0.42 W for the boost prototype in comparison to the proposed converter prototype, resulting in a theoretical efficiency equal to 96%.

The same diode (UF5408) was used in the experimental prototypes of the boost and the modified SEPIC converters. However, since the maximum voltage in the diodes D_M and D_o is always lower than the output voltage ($V_o = 400$ V), the diode UF5404 (3 A–400 V) with a diode forward voltage equal to 1.0 V, as presented in the diode manufacturer catalog (Vishay), could be used in the proposed converter prototype.

Consequently, using the diode 1N5408 in the classical boost converter, the output diode conduction losses is equal to 0.425 W and using the diode 1N5404 in the proposed converter as the diodes D_M and D_o, the total diode conduction losses will be reduced from 0.85 to 0.5 W. Also, a lower $\mathrm{RDS_{on}}$ MOSFET could be used in the proposed converter due to the lower switch voltage.

The experimental efficiency of the proposed converter operating with $V_i = 127\,V_{\mathrm{rms}}$ and $V_i = 220\,V_{\mathrm{rms}}$ are shown in Figs. 31 and 32, respectively, measured with the digital power meter Yokogawa WT230. The prototype configuration was also changed to the classical boost rectifier presented in Fig. 1 using the same semiconductors of the proposed converter. The efficiency curve of the boost converter is presented considering an operation point similar to the proposed converter using an inductance equal to 1.1 mH.

The efficiency of the proposed converter operating with output power equal to 108 W and $V_i = 127\,V_{\mathrm{rms}}$ is equal to 95.6%, while for the boost converter is equal to 95.2%.

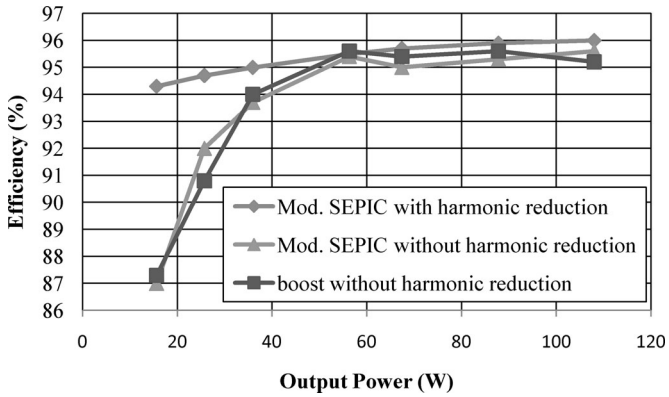

Fig. 31. Preregulator efficiency for $V_i = 127\,V_{\rm rms}$.

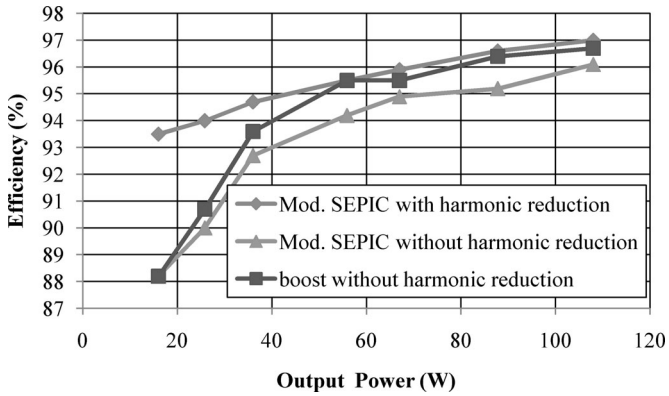

Fig. 32. Preregulator efficiency for $V_i = 220\,V_{\rm rms}$.

The efficiency of the proposed converter was measured also operating with the third-harmonic reduction technique. The experimental results show that not only a reduction of the third-harmonic input current distortion and the improvement of the rectifier power factor occur, but there is also an increment in the converter efficiency. The efficiency increment using the third-harmonic reduction modulation operating with the nominal output is close to 0.5% for the input voltage $V_i = 127\,V_{\rm rms}$ and equal to 1% for the input voltage $V_i = 220\,V_{\rm rms}$.

However, a significant efficiency increment occurs in both input voltages for the light load operation, maintaining the converter efficiency higher than 93% for all load range. This operation characteristic is interesting for applications where the rectifier operates during a long period with low output power.

VIII. Conclusion

The theoretical and experimental analysis of the modified SEPIC converter used as preregulator operating in DCM is presented in this paper. The proposed converter presents low input current ripple operating in DCM and the switch and diodes voltages are lower than the output voltage. The switch voltage reduction increases the converter reliability and a lower $\rm RDS_{on}$ MOSFET can be used depending on the converter specification.

The experimental results presented operating with the third-harmonic reduction technique shows that the total input current harmonic distortion is reduced from 13% to 5.3% operating with an input voltage equal 127 $V_{\rm rms}$ and is reduced from 35.9% to 8.84% operating with an input voltage equal to 220 $V_{\rm rms}$, considering a total input voltage harmonic distortion equal to 3.1%. The power factor is higher than 0.988 with the third-harmonic reduction in all input voltage range.

The efficiency operating with input voltage equal to 127 $V_{\rm rms}$ and output power equal to 108 W is equal to 95.6%. The experimental results show that there is also an increment in the converter efficiency operating with the third-harmonic reduction modulation that mainly occurs at light load operation in 127 and 220 $V_{\rm rms}$.

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