This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2015.2433351, IEEE Transactions on Circuits and Systems II: Express Briefs

# High Gain Zero Voltage Switching Bidirectional converter with reduced number of switches

Muhammad Aamir, Saad Mekhilef *Member IEEE* and Hee-Jun Kim *Senior Member IEEE*

***Abstract*—A non-isolated bidirectional DC-DC Converter has been proposed in this paper for charging and discharging the battery bank through single circuit in applications of Uninterruptible Power Supplies (UPS) and the hybrid electric vehicles. The proposed bidirectional converter operates under zero voltage switching (ZVS) condition and provides large voltage diversity in both the modes of operation. This enables the circuit to step up the low battery bank voltage to high DC link voltage and vice versa. The bidirectional operation of the converter is achieved by employing only three active switches, a coupled inductor and an additional voltage clamped circuit. Complete description of the operation principle of the circuit is explained and design procedure of the converter has been discussed. The experimental results of a 300W prototype of the proposed converter confirmed the validity of the circuit. The maximum efficiency of 96% is obtained at half load for boost operation mode, and 92% for buck mode of operation.**

***Index Terms*—Bidirectional DC-DC Converter, Zero voltage switching (ZVS), Coupled inductor**

## I. Introduction

Bidirectional DC-DC Converters are widely used in many industrial applications such as hybrid vehicles, auxiliary supplies, and in battery charging/discharging DC converters in UPS system. Usually battery bank are the backup energy source which provides very low voltage at the input of the bidirectional converter. Although, a string of batteries connected in series can provide a high input voltage, but still it has some disadvantages. A larger battery bank increases the size and cost of the system. Also if there is a slight mismatch in the batteries voltage or difference in the batteries temperature with in the string, it will cause charge imbalance in the battery bank [1]. This study therefore focuses on the analysis and design of a high efficiency bidirectional converter with high voltage conversion ratio, which helps in reducing the number of batteries in order to elude a larger battery bank.

The bidirectional converter may be transformer isolated [2] or non-isolated [3-10]. Isolated bridge-type bidirectional converters are probably the most popular topology in high power applications. However, the major concerns of this topology are high switching losses, excessive voltage and current stresses, and significant conduction losses because of the increased in the number of switches [6]. Hence, their practical implementation is quite complex.

With incorporation of coupled inductor and zero voltage switching (ZVS), Non-isolated bidirectional converters has attracted special interest due to high conversion ratio, reduced switching losses, and simplicity in design. These types of topologies are highly cost effective and acceptable due to high efficiency improvement, and considerable reduction in the weight and volume of the system. Several topologies of the non-isolated converters have been proposed so far [3-6]. A ZVS bidirectional converter with single auxiliary switch has been proposed in [3]. Although the main switches operate under ZVS which increase the efficiency of the system, but the auxiliary switch still performs hard switching and the converter offers very limited voltage diversity [7].

Other high voltage gain bidirectional converters have been proposed in [8-11]. These converters provide high voltage gain in both the boost and buck mode of operation but at the cost of high number of active switches and extra auxiliary circuit components used in the circuit. This adds more complexity in the control circuitry, with high size and cost.

According to the analysis of the drawbacks related to the aforementioned topologies, this paper proposes a new non-isolated bidirectional DC-DC converter with coupled inductor. The proposed converter has following advantages.

1. High Voltage Gain in both the buck and boost mode
2. Only three active switches are used to perform bidirectional operation.
3. Less number of passive components are used in the circuit
4. Zero voltage switching (ZVS), synchronous rectification, and voltage clamping circuit are used which reduces the switching and conduction losses.

This paper is organized as follows: the operation of proposed topology is explained in section II. Design considerations are presented in section III, followed by experimental results in section IV and conclusion in Section V.

## II. Converter Operation

The circuit configuration of the proposed circuit is shown in the Fig. 1. The Low Voltage Side (LVS) of the bidirectional converter is connected with the battery bank or fuel cells and the high voltage side (HVS) is connected to the high voltage DC bus. Coupled inductor has been used with $L_P$ as primary inductance and $L_S$ as the secondary inductance tightly coupled on the same ferrite core. The coupled inductor increases the voltage diversity of the circuit in both the buck and boost mode of operation. The polarities of the primary and secondary windings keep changing, depending on the switches



This work was supported by the High Impact Research - Ministry of Higher Education under Project. UM.C/HIR/MOHE/ENG/17 and Bright Spark Unit

Muhammad Aamir and Saad Mekhilef are with Power Electronics And Renewable Energy Research Laboratory (PEARL), University of Malaya, 50603 Kuala Lampur, Malaysia (email: m_aamir801@hotmail.com; saad@um.edu.my)

H.-J. Kim is with the School of Electrical Engineering and Computer Science, Hanyang University, Ansan 426-791, Korea (email: hjkim@hanyang.ac.kr)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2015.2433351, IEEE Transactions on Circuits and Systems II: Express Briefs



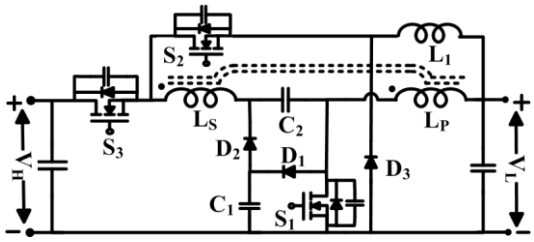



Fig.1 Proposed ZVS non-isolated bidirectional converter

PWM. The inductor is custom based designed depending on the turn ratio and the voltages of LVS and HVS. Capacitor $C_2$ inserted in the main power across the primary and secondary windings of the transformer gives high voltage diversity and reduces the peak current stress allowing current in the primary continuous. Also the voltage stress of the capacitor $C_2$ will be minimum at this position. The circuit can operate both in the buck mode to recharge the battery and boost mode to provide the regulated high DC output voltage.

*A. Buck Mode of Operation:*

The characteristic waveforms of the converter during buck mode of operation are shown in Fig. 2. $D_1$ is the duty ratio of $S_1$ and $S_2$, where $D_3$ is the duty ratio of switch $S_3$. Both $D_1$ and $D_3$ are related to each other by a relationship $D_1$ (= 1− $D_3$). The coupled inductor can be modeled as an ideal transformer with the magnetizing inductor Lm and turns ratio N = $N_2/N_1$, where $N_1$ and $N_2$ are the winding numbers in the primary and secondary side of the coupled inductor respectively. Fig. 3 describes the circuit of each mode during buck operation.

**Mode 1 ($t_0$ ~ $t_1$):** The Switch $S_3$ remains ON while the switches $S_1$ & $S_2$ are OFF during mode 1. The current $i_{LS}$ flows from High voltage side (HVS) to the Low Voltage Side (LVS) of the circuit through the capacitor $C_2$ and both the windings of the coupled inductor. Applying KVL we get (1).

$$V_H = V_{LS} + V_{C2} + V_{LP} + V_L \quad (1)$$

$$V_H = V_{LP}(1 + N) + V_{C2} + V_L \quad (2)$$

The diode $D_3$ is also conducting with continuous inductor current $i_{L1}$ into the low voltage side LVS of the circuit. Hence, $V_L$ is the voltage across inductor $L_1$.

**Mode 2 ($t_1$ ~ $t_2$):** At the start, the switch $S_3$ turns OFF. Due to the storage energy in the leakage inductor, the polarities are reversed across the primary and secondary windings ($L_S$ & $L_P$) of the coupled inductor. Switch $S_3$ is OFF in this mode, but the secondary current $i_{LS}$ is still conducting, so the switch $S_2$ body diode turns ON in order to keep the current $i_{LS}$ flowing. The diode $D_3$ keeps conducting in this mode. The switch $S_1$ body diode also turns ON because though the secondary current $i_{LS}$ decreases, but the primary current $i_{LP}$ remains the same.

**Mode 3 ($t_2$ ~ $t_3$):** Both the Switches $S_1$ and $S_2$ turns ON following zero voltage switching (ZVS) condition. The capacitor $C_2$ starts discharging across LVS of the circuit through the switch $S_2$ and inductor $L_1$. Thus the secondary current is induced in reverse by discharging capacitor $C_2$. Clamp capacitor $C_1$ also discharge through the diode $D_2$ by adding small current $i_3$ into the secondary current flowing into the Low voltage side of the circuit.

Using the voltage second balance, $V_{C2}$ will be,

$$V_{C2} = V_{L1} + V_L + V_{LS} \quad (3)$$

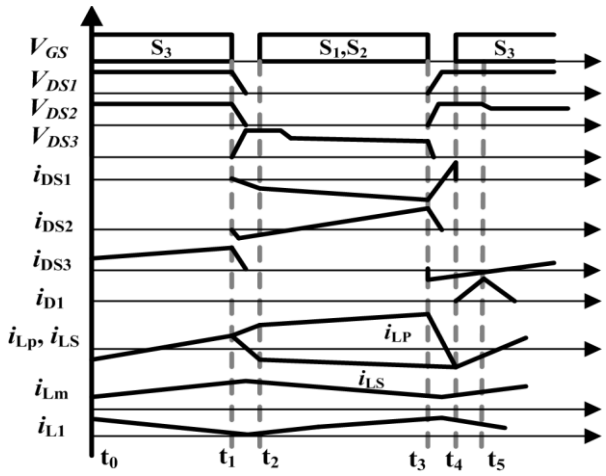



Fig. 2 Characteristic waveforms of the buck mode of operation

The stored energy in the coupled inductor is released by primary current through the switch $S_1$ into LVS.

Using the voltage-second balance, the $V_{L1}$ is given by,

$$D_1 V_{L1} = D_3 V_L \quad (4)$$

Primary winding voltage $V_{LP}$ can be obtained as,

$$D_3 V_{LP} = D_1 V_L \quad (5)$$

Putting (4) and the values of $V_{L1}$, and $V_{LP}$ in (2), the voltage gain during buck mode of operation is given by equation,

$$G_{buck} = V_L/V_H = [D_3(1 - D_3)]/[2N(1 - D_3)^2 + 1] \quad (6)$$

**Mode 4 ($t_3$ ~ $t_4$):** Both the switches $S_1$ and $S_2$ turn OFF at the start of this mode. The primary and secondary winding currents $i_{LP}$ & $i_{LS}$ will continue conduction due to the leakage inductance of the coupled inductor. The secondary current will charge the parasitic capacitance of the switches $S_1$ & $S_2$, and discharge the parasitic capacitance of the switch $S_3$. When the voltage across the switch $S_2$ equals to $V_H$, the body diode of the switch $S_3$ turns ON. The primary current $i_{LP}$ starts decreasing unless it equals to the secondary current $i_{LS}$, then this mode finishes.

**Mode 5 ($t_4$ ~ $t_5$):** The switch $S_3$ turns ON under zero voltage switching (ZVS) condition. The capacitor $C_1$ is charges through the clamped Diode $D_1$. The primary and secondary current starts increasing. At the end of this mode, the circuit starts repeating mode 1of the next cycle.

*B. Boost Mode of Operation:*

The characteristic waveform of the proposed circuit during boost mode of operation is shown in Fig. 4. During boost mode, the proposed converter steps up the low battery bank voltage to high DC link voltage. The switch $S_2$ remains OFF during boost mode of operation. The operation of the circuit during boost mode is shown in the Fig. 5.

**Mode 1 ($t_0$ ~ $t_1$):** During mode 1, the Switch $S_1$ was ON, while the switch $S_3$ was OFF. Low battery bank voltage is applied at the Low voltage side LVS of the circuit. Capacitor $C_2$ remains charged before mode 1 and the magnetizing current $i_{LM}$ of the coupled inductor increase linearly as shown in the Fig. 4. Applying KVL, we get,

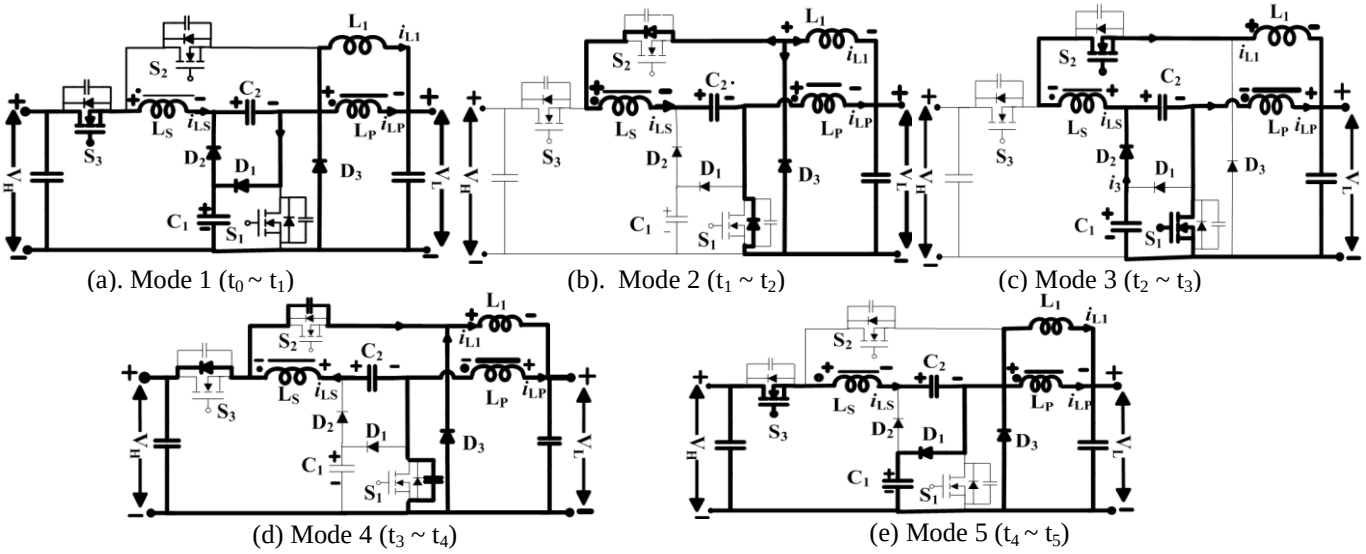
$$V_L = V_{Lp} = V_{LS}/N \quad (7)$$

The voltage across the primary winding can be derives using voltage second balance

$$V_{LP} D_3 = V_L D_1 \quad (8)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2015.2433351, IEEE Transactions on Circuits and Systems II: Express Briefs






(a). Mode 1 ($t_0 \sim t_1$) (b). Mode 2 ($t_1 \sim t_2$) (c) Mode 3 ($t_2 \sim t_3$)

(d) Mode 4 ($t_3 \sim t_4$) (e) Mode 5 ($t_4 \sim t_5$)

Fig. 3 Topological stages in Buck mode: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5

**Mode 2 ($t_1 \sim t_2$):** The switch $S_1$ turns OFF in mode 2. The primary current $i_{LP}$ charges the parasitic capacitance across the switch $S_1$ and the secondary current $i_{LS}$ discharges the parasitic capacitance across switch $S_3$. When the voltage across switch $S_1$ equals to the capacitor voltage $V_{C1}$, this mode finishes.

**Mode 3 ($t_2 \sim t_3$):** Since the switch $S_1$ is OFF, leakage inductance cause the primary current $i_{LP}$ to decrease while the secondary current $i_{LS}$ increases. As a result the body diode of switch $S_3$ turns ON. Capacitor $C_1$ starts charging through diode $D_1$ because the voltage across the switch $S_1$ gets higher than capacitor $C_1$. This limits the voltage stress across the switch $S_1$. The voltage across the capacitor is given by,

$$V_{C1} = V_L + V_{LP} \quad (9)$$

Using (7), $$V_{C1} = V_L/D_3 \quad (10)$$

**Mode 4 ($t_3 \sim t_4$):** Switch $S_3$ turns ON under the condition of zero voltage switching (ZVS). The primary and secondary windings of the coupled inductor and the capacitor $C_2$ are all now connected in series to transfer the energy to the High voltage side HVS of the circuit. The $i_{LS}$ starts increasing until it reaches the $i_{LP}$, then it follows the $i_{LP}$ till the end of the mode 4. Thus the energy stored in the primary and secondary discharges across the HVS of the circuit. Both the diodes $D_1$ and $D_2$ remain OFF during this mode as shown in Fig. 5(d). Using voltage second balance, we get (11)

$$V_H = V_L + V_{LS} + V_{C2} + V_{Lp} \quad (11)$$

$$V_H = V_L + V_{C2} + (N+1)V_{LP} \quad (12)$$

**Mode 5 ($t_4 \sim t_5$)**: During this mode, the switch $S_3$ turns OFF. The current $i_{LS}$ charges the parasitic capacitance of the switch $S_3$. The capacitor $C_1$ starts discharging across the capacitor $C_2$, through the diode $D_2$.

$$V_{C2} = V_{C1} = V_L/D_3 \quad (13)$$

By putting (8) and (13) in (12), Voltage gain of the circuit is.

$$V_H = V_L + V_L/D_3 + (N+1)\, D_1/D_3\, V_L \quad (14)$$

$$\mathbf{G_{boost} = V_H/V_L = (2 + ND_1)/(1 - D_1)} \quad (15)$$

The body diode of the switch $S_1$ turns ON because of the polarities of capacitor $C_2$ and inductor $L_P$.

**Mode 6 ($t_5 \sim t_6$):** During Mode 6, switch $S_1$ turns ON under the condition of zero voltage switching. Since $S_1$ is not deriving any current from the clamped circuit, thus the switching losses remains low due to ZVC and the efficiency of the circuit increases. When both the $V_{C1}$ and $V_{C2}$ get equal, than the next switching cycle starts and repeats the operation in mode 1

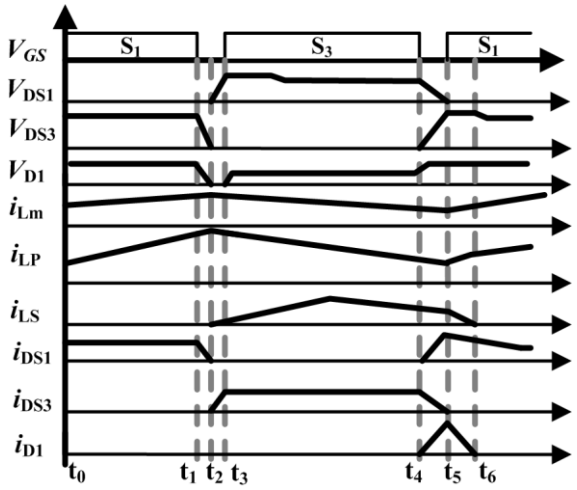



Fig. 4 Characteristic waveforms of the Boost mode

## III. Design Considerations

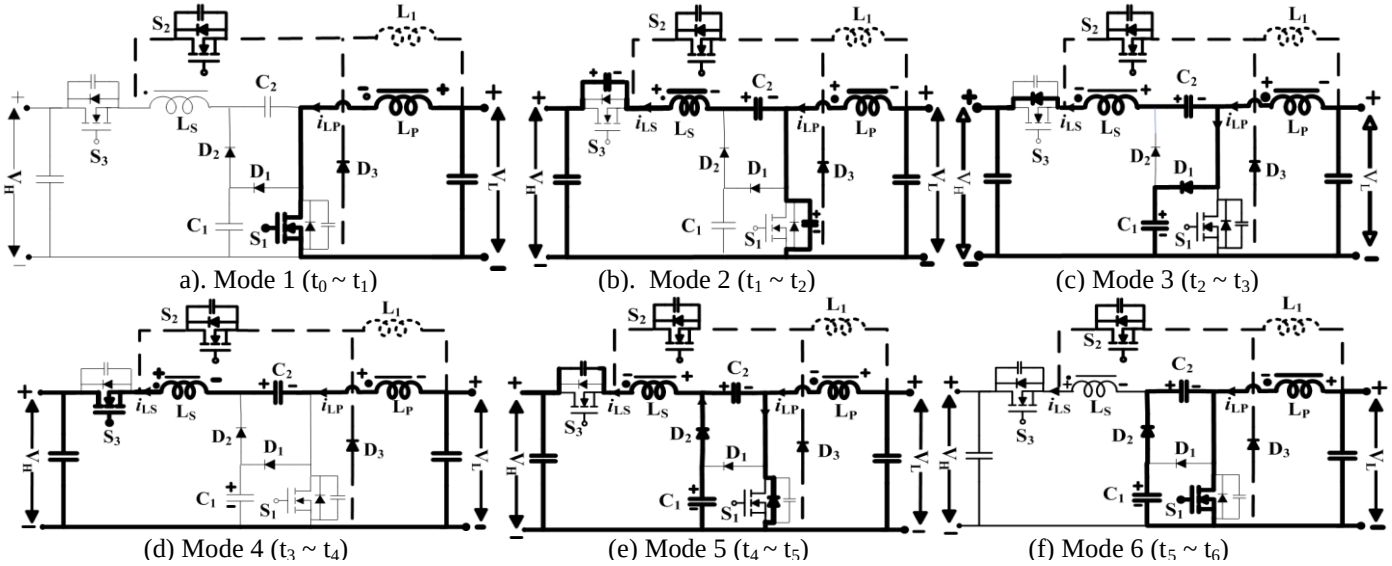
Analyzing (6) and (15) shows that turn ration N should be selected as such to satisfy the voltage gain during both buck and boost mode of operation. Fig. 6 shows the voltage gain at both the buck and Boost mode with respect to duty cycle D3 at different values of turn ratio N. Analysis of the graphs in Fig. 6 shows that the turns ratio N should be selected as N=2.5 which gives the operation condition of $V_H$ =200V, and $V_L$ =24V. The duty ratio ($D_3$ and $D_1$) during above conditions is about 0.6 in their respective modes.

### *A. Coupled Inductor Design:*

The inductor needs to be high enough to minimize the ripple and associated losses. In order to design a coupled inductor, analyze the circuit in either buck or boost mode of operation and calculate the magnetizing inductor Lm, and the number of turns $N_1$ & $N_2$ of the coupled inductor [12]. Consider boost mode of operation, the magnetizing current $i_{Lm}$ when the switch S1 turns ON is given by,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2015.2433351, IEEE Transactions on Circuits and Systems II: Express Briefs






a). Mode 1 ($t_0 \sim t_1$) (b). Mode 2 ($t_1 \sim t_2$) (c) Mode 3 ($t_2 \sim t_3$)

(d) Mode 4 ($t_3 \sim t_4$) (e) Mode 5 ($t_4 \sim t_5$) (f) Mode 6 ($t_5 \sim t_6$)

Fig. 5 Topological stages in Boost mode: (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6

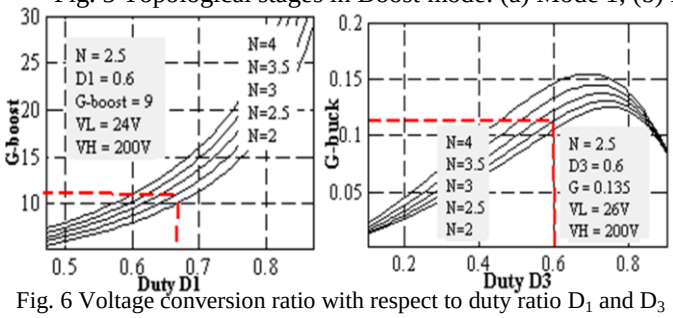



Fig. 6 Voltage conversion ratio with respect to duty ratio $D_1$ and $D_3$

$$i_{Lm} = \frac{1}{L_m} V_{in} t + I_L(0) \qquad 0 \le t < DT \tag{16}$$

where $I_L(0)$ is the initial current at t = 0. The $i_{LM}$, when switch $S_1$ turns OFF and $S_3$ ON is given by,

$$i_{Lm} = \frac{1}{Lm}\left(\frac{V_o - 2V_{in}}{2+N}\right)(t - D_1 T) + I_L(D_1 T) \quad DT \le t < T \tag{17}$$

Putting $t = D_1 T$ in (16) and $t = T$ in (17), we get

$$I_L(D_1 T) - I_L(0) = \frac{1}{Lm} V_{in}(D_1 T) \tag{18}$$

$$I_L(D_1 T) - I_L(0) = -\frac{1}{Lm}\left(\frac{2V_{in} - V_o}{2+N}\right)(1 - D_1 T)T \tag{19}$$

$$\frac{V_o}{V_{in}} = \frac{2+ND_1}{1-D_1} \tag{20}$$

The inductor ripple current is given by,

$$\Delta I = \frac{1}{Lm} \frac{Vo(1-D_1)D_1 T}{2+ND_1} \tag{21}$$

Average input current is given by,

$$I_{in} = \frac{I_{Lm(max)} + I_{Lm(min)}}{2} \tag{22}$$

Average Output Inductor Current is given by,

$$I_o = \left(\frac{I_{Lm(max)} + I_{Lm(min)}}{2}\right)(1 - D_1) = \frac{V_o}{R} \tag{23}$$

$$I_{Lm(max)} = \left(\frac{2+ND_1}{(1-D_1)^2 R} + \frac{D_1 T}{2Lm}\right) \tag{24}$$

To solve for the minimum critical magnetizing inductance value, that keeps the converter into Continuous conduction mode (CCM), we set the $I_{Lm(min)} = 0$,

$$L_{m(crit)} = \frac{D_1(1-D_1)^2 RT}{2(2+ND_1)} \tag{25}$$

Using (25), the number of turns can be calculated as [13],

$$\frac{N_2}{N} = N_1 = \frac{L_m I_m}{B_{max} A_c} 10^4 \tag{26}$$

$B_{max}$ is max flux density; $A_C$ is the core cross sectional area.

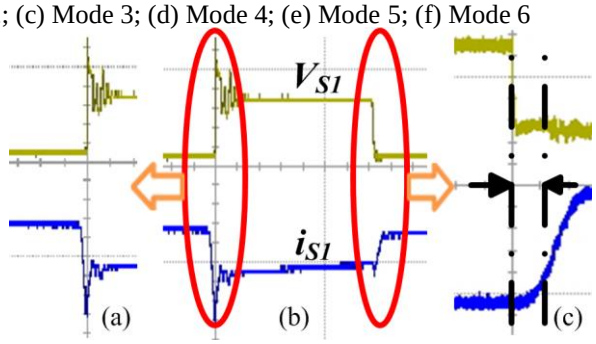


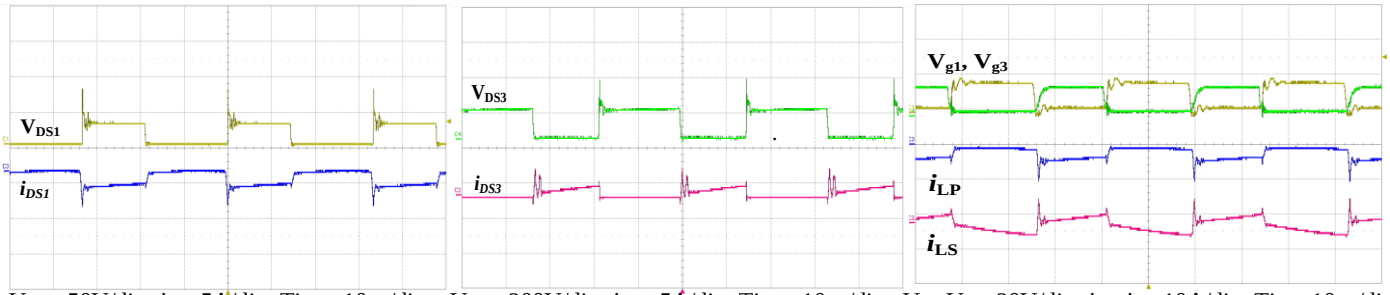

Fig. 7 ZVS of the switch $S_1$ during buck mode

## IV. Experimental Results

A 300W protype has been built to confirm the feasibility of the proposed circuit. The circuit operated between LVS voltage $V_L$ = 24V, and HVS voltage $V_H$ =200V. The switching frequency is 20 KHz. The Switches $S_1$-$S_3$ used in the circuit are IPW60R045CP MOSFETs. Coupled inductor is designed using PQ40-40 with magnitising inductance of 24uH, and turns ratio N = 2.5. An inductor $L_1$ has 80uH inductance, so the size is very small. Besides $C_1$ and $C_2$ consist of 4.4uF ceramic capacitors. The diodes $D_1$~$D_3$ used are ultrafast recovery diodes UF5408. Thus all the axilary components are not adding considerable in the size of the circuit. A low cost PWM controller TL494 is employed for controlling the switches of the bidirectional converter. The dead time between the switching PWM is 5us which helps in ZVS of the circuit. An experimental prototype was built to confirm its feasibility. Fig 8 and Fig. 9 shows the experimental waveform during buck and boost mode of the proposed circuit respectively.The voltage stress across both the switches $S_1$ and $S_2$ is about 50V which is quite small as compare to HVS (200V). The voltage across the Switch $S_2$ is quite low, and conduction current in the coupled inductor is smoothened as shown in the Fig.8. Fig.7 shows the Zero voltage switching in switch $S_1$ during buck mode of operation. Fig. 10 gives the experimental results which shows maximum efficiency of about 96% during boost mode and 92% during buck mode of operation Thus utilizing synchronous rectification and soft switching reduces the switch losses and increases the efficiency of the system. The

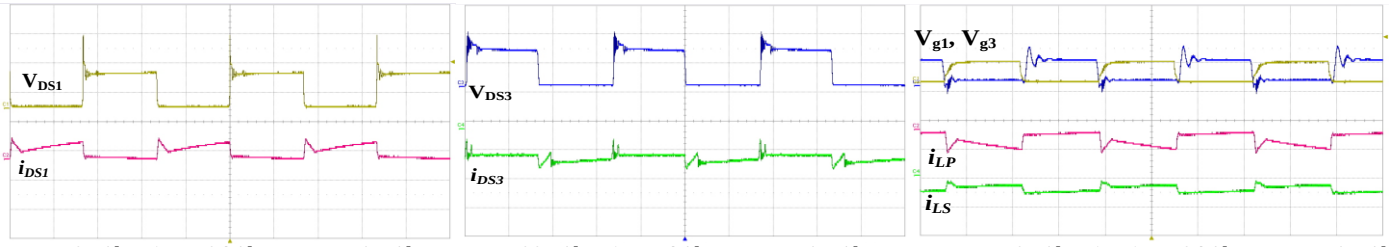
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2015.2433351, IEEE Transactions on Circuits and Systems II: Express Briefs






$V_{DS1}$: 50V/div; $i_{DS1}$:5A/div; Time: 10us/div $V_{DS3}$: 200V/div; $i_{DS3}$: 5A/div; Time: 10us/div $Vg_1$,$Vg_3$: 20V/div; $i_{LP}$, $i_{LS}$: 10A/div; Time:10us/div

Fig. 8 Experimental Waveform of Drain to Source Switch voltages and Inductor current during Buck Mode




$V_{DS1}$:50V/div; $i_{DS1}$:10A/div; Time: 10us/div $V_{DS3}$:200V/div; $i_{DS3}$:5A/div; Time: 10us/div; $Vg_1$, $Vg_3$: 20V/div; $i_{LP}$, $i_{LS}$: 10A/div; Time: 10us/div

Fig. 9 Experimental Waveform of Drain to source voltages and Inductor current during Boost mode

efficiency during buck mode is less than boost mode due to utilization of an additional switch $S_2$ which is not used in the boost mode. Table. I shows the comparison of different bidirectional converters recently published. The voltage conversion ratio of the proposed converter shows more diversity as compared to [9] and [10], with less no of switches. [11] shows high gain ratio but with five switches which increases the size and cost of the circuit. The size of the proposed circuit is considerable small with small heat sink for the given power rating, and only few passive auxillary components help in operation under ZVS.

## V. Conclusion

This paper presents a non-isolated ZVS bidirectional DC-DC converter. The most promising features of the converter are high voltage conversion ratio in both modes of operation, with less number of active switches, and low voltage & current stresses on the switches. The operation principle of each mode has been explained and the design steps of the converter are discussed. The experimental results of the proposed converter shows exemplary results with high efficiency of about 96% and 92% in boost and buck modes of operation respectively.

TABLE I. Comparison of different Topologies

| Topology Features | Conv. | [11] | [9] | [10] | Proposed Topology |
|---|---|---|---|---|---|
| Switches | 2 | 5 | 4 | 4 | 3 |
| $M_{BOOST}$ | $1/(1-D)$ | $\frac{1+N}{(1-D)}+N$ | $\frac{2+N}{D}$ | $\frac{2}{1-D}$ | $\frac{2+ND}{1-D}$ |
| $M_{BUCK}$ | $D$ | $\frac{D}{1+N+DN}$ | $\frac{D}{N+2}$ | $\frac{D}{2}$ | $\frac{D(1-D)}{2N(1-D)^2+1}$ |
| Efficiency (%) | 90 | 96 | 95 | 94 | 96 |
| Size | Small | Large | Medium | Medium | Small |
| Estimated Cost(US $) | - | ~172 | ~118 | ~136 | ~116 |

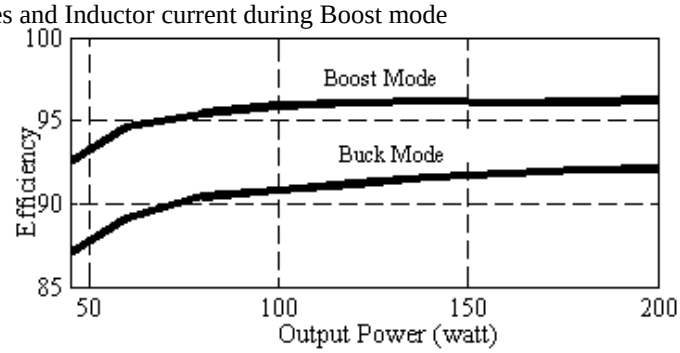



Fig.10 Experimental Efficiency Graphs

## References


[1] M. Uno and K. Tanaka, "Single-switch cell voltage equalizer using multistacked buck-boost converters operating in discontinuous conduction mode for series-connected energy storage cells," *IEEE Transactions on Vehicular Technology*, vol. 60, pp. 3635-3645, Oct. 2011

[2] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications," *IEEE Transactions on Power Electronics*, vol. 21, pp. 422-429, Mar. 2006.

[3] P. Das, B. Laan, S. A. Mousavi, and G. Moschopoulos, "A nonisolated bidirectional ZVS-PWM active clamped DC–DC converter," *IEEE Transactions on Power Electronics*, vol. 24, pp. 553-558, Jan. 2009.

[4] J. Zhang, J.-S. Lai, R.-Y. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 22, pp. 1145-1153, Jul. 2007.

[5] J.-W. Yang, and H.-L. Do, "Soft-Switching Bidirectional DC-DC Converter Using a Lossless Active Snubber," *IEEE Transactions on Circuits and Systems I*, vol. 61, no. 5, pp. 1588-1596, May. 2014.

[6] H. Shiji, K. Harada, Y. Ishihara, T. Todaka, and G. ALZAMORA, "A zero-voltage-switching bidirectional converter for PV systems," *IEICE transactions on communications*, vol. 87, pp. 3554-3560, Oct. 2004.

[7] S.-H. Park, S.-R. Park, J.-S. Yu, Y.-C. Jung, and C.-Y. Won, "Analysis and design of a soft-switching boost converter with an HI-Bridge auxiliary resonant circuit," *IEEE Transactions on Power Electronics*, vol. 25, pp. 2142-2149, Aug. 2010.

[8] M. Kwon, S. Oh, and S. Choi, "High Gain Soft-Switching Bidirectional DC–DC Converter for Eco-Friendly Vehicles," *IEEE Transactions on Power Electronics*, vol. 29, pp. 1659-1666, April. 2014.

[9] R.-Y. Duan and J.-D. Lee, "High-efficiency bidirectional DC-DC converter with coupled inductor," *IET Power Electronics*, vol. 5, pp. 115-123, Jan. 2012.

[10] C.-C. Lin, L.-S. Yang, and G. Wu, "Study of a non-isolated bidirectional DC–DC converter," *IET Power Electronics*, vol. 6, pp. 30-37, Jan. 2013.

[11] Y.-P. Hsieh, J.-F. Chen, L.-S. Yang, C.-Y. Wu, and W.-S. Liu, "High-conversion-ratio bidirectional dc–dc converter with coupled inductor," *IEEE Transactions on Industrial Electronics*, pp. 210-222, Jan. 2014.

[12] I. Batarseh, *Power electronic circuits*: John Wiley, 2004.

[13] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*: Springer, 2001.