ECE 593 FUNDAMENTALS OF PRE-SILICON VALIDATION
PROJECT PROPOSAL
VERIFICATION OF AMBA AXI4-Lite PROTOCOL

TEAM MEMBERS:

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OBJECTIVE:

Implementing AXI4-lite BFM (slave and master) to study AXI4 transaction protocol by developing interfaces, coverage, checkers and monitors to verify AXI4-lite protocol.

AXI4-Lite Protocol:

Advanced eXtensible Interface 4 (AXI4) is a family of buses defined by ARM Advanced Microcontroller Bus Architecture (AMBA) standard. AX4-Lite lacks burst access capability. It has a simpler interface than the full AXI4 interface.

AXI4-Lite consists of five channels

- Read Address
- Read Data
- Write Address
- Write Data
- Write Response

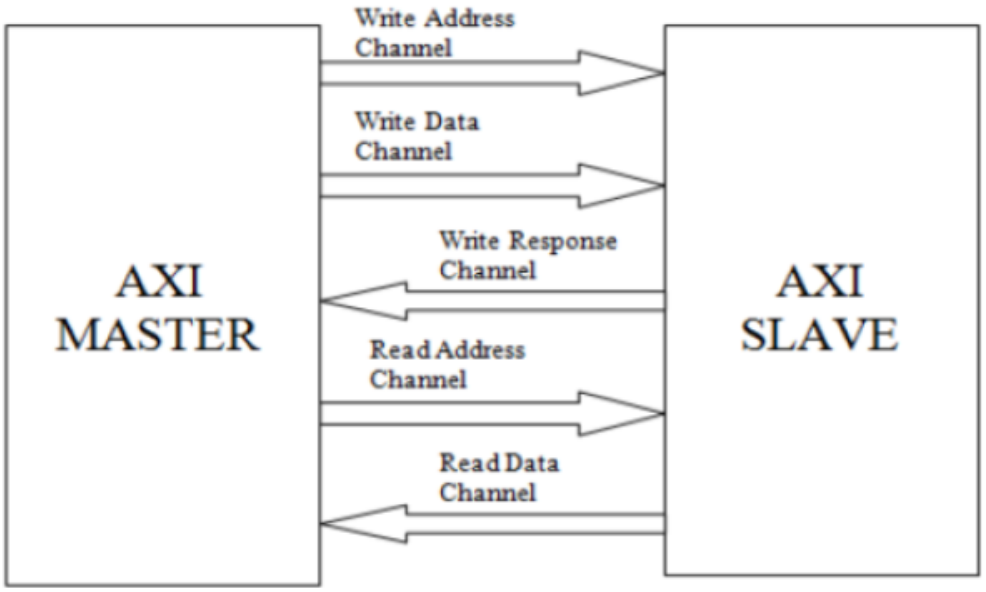

Figure1: AXI4-Lite Channels

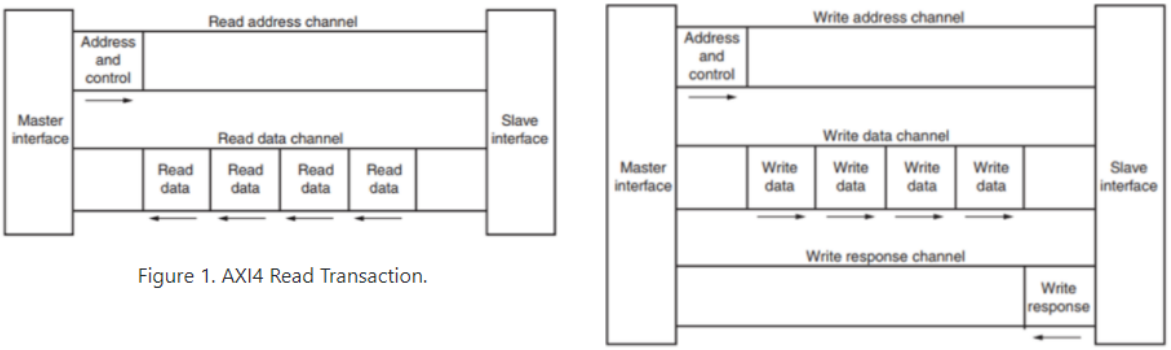

Figure 1. AXI4 Read Transaction.

Figure2: AXI4 Read and Write transactions

Testbench components:

1. Interface:
    a. Slave and master AXI4-Lite interface
    b. Tasks to generate read and write on the master interface.
2. Monitor
    a. To keep track of all the transactions issued by the master interface and generate transaction log file.
3. Checker
    a. To verify the master receives the correct response for all of it's requests.
4. Coverage
    a. Various coverpoints for read & write transactions of data & address, master and slave FSM components with the combination of reset.
5. SV Class
    a. To define different AXI4-Lite transaction packets.
    b. Various tasks with directed testcases and random stimulus.

Existing design source codes:

https://github.com/durganila/Verification-of-AMBA-AXI4-Lite-Protocol

Reference:

- https://developer.arm.com/documentation/ihi0022/e/AMBA-AXI4-Lite-Interface-Specification?lang=en