FIRST HALT 2017 1-6-17

T1624 / T1080 S.E.(INFORMATION TECHNOLOGY)(SEM IV) (CBSGS) COMPUTER ORGANIZATION AND ARCHITECTURE

Q.P. Code : 09892

[Time: Three Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B: 1. Question.No.1 is compulsory.
2. Attempt any THREE out of the remaining questions.
3. Assume suitable data if necessary.

Q.1 Solve any **Four** sub questions

a) Draw and explain Memory hierarchy. 05
b) Represent $(12.25)_{10}$ in double precision IEEE 754 binary floating point representation format. 05
c) Draw and explain basic instruction execution cycle. 05
d) What are the types of pipeline hazards? 05
e) What are the major functions of an I/O module? 05

Q.2 a) Explain the functioning of Wilke's Microprogrammed control unit with its advantages. 10
b) Draw the flowchart of Booths algorithm and multiply (4)*(-3) using Booths algorithm. 10

Q.3 a) Differentiate between RISC and CISC in detail with example. 10
b) Draw flowchart of binary Restoring division and use it to divide 16/4. 10

Q.4 a) Calculate the number of page hits and faults using FIFO, LRU and OPTIMAL page replacement algorithms for the following page frame sequence : 2, 3, 1, 2, 4, 3, 2, 5, 3, 6, 7, 9, 3, 7. (FRAME SIZE = 3). 10
b) What is instruction pipelining? Explain with suitable diagram. 10

Q.5 a) What are the elements of a cache design? 10
b) Explain DMA in detail. 10

Q.6 Write detailed notes on **(any two)** 20

a) Microinstruction formats
b) Programmed I/O
c) Interleaved and Associative memory
d) Evolution of Computers
