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EE610 ANALOG VLSI CIRCUIT- PROJECT

The single stage differential amplifier is to be designed with the following specifications at room temperature (27℃).
gpdk 180nm library is used for transistors.

- VDD = 1.8 V
- CL = 10 pF
- Minimum loop gain at DC: 25 dB
- Minimum CMRR at DC: 80 dB
- NMOS input differential pair
- One ideal 1 μA current source with one terminal (sink) connected to ground.

Schematic of Final circuit

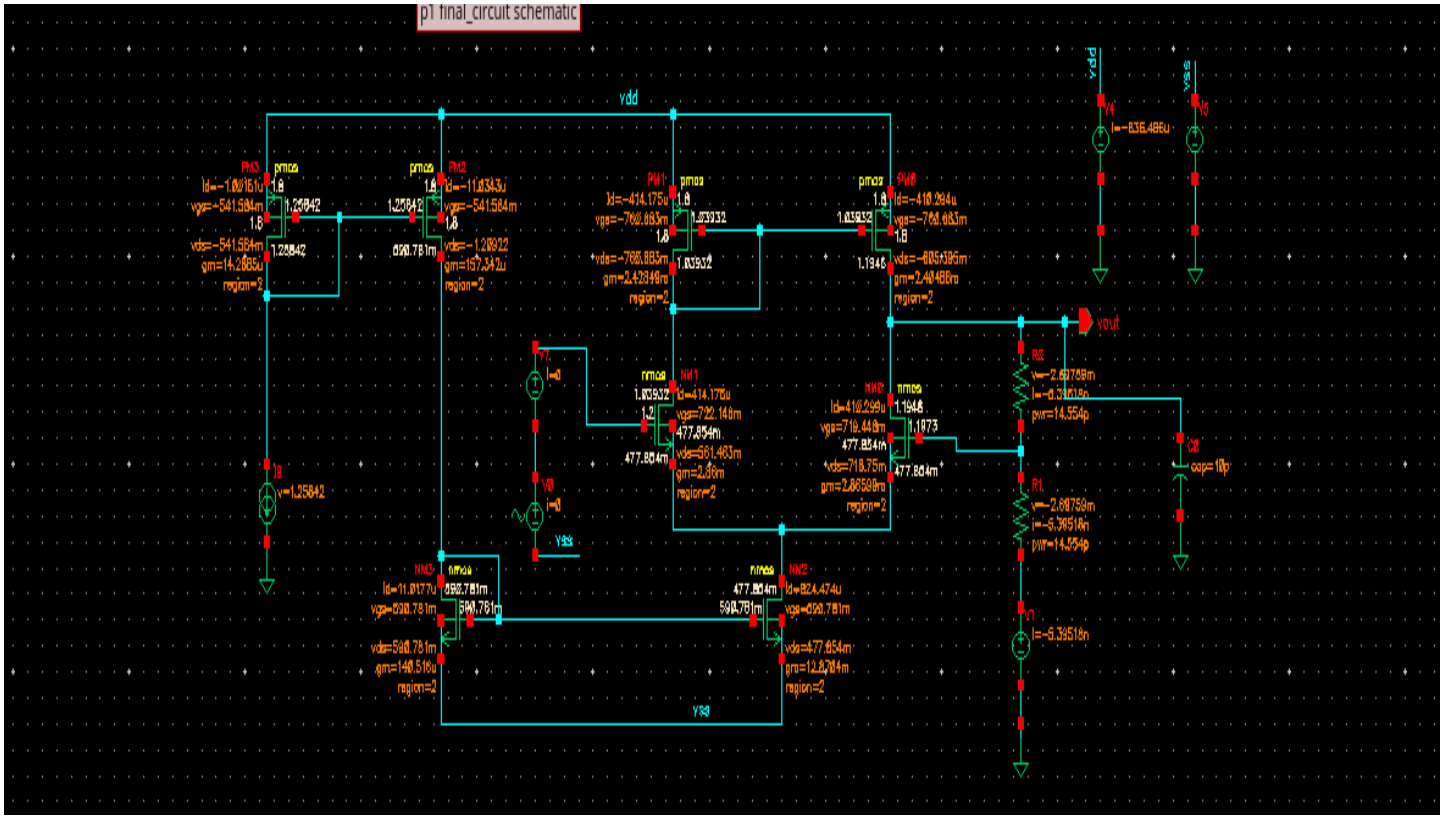

Fig1: Schematic of Final circuit

Schematic (Loop Gain)

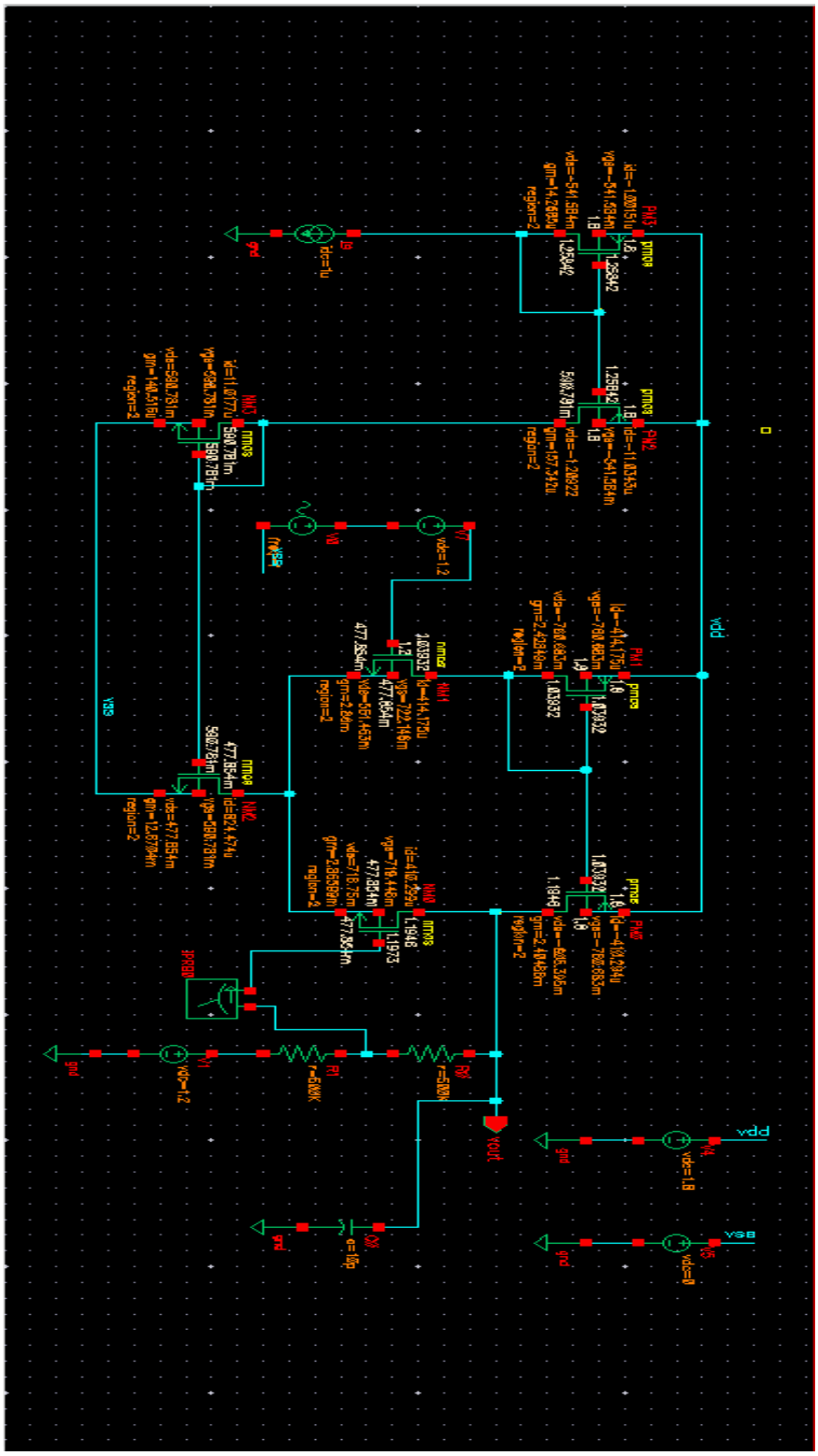

Fig2: Schematic for analysis of loop gain

CMRR Schematic (Ad and Acm schematic)

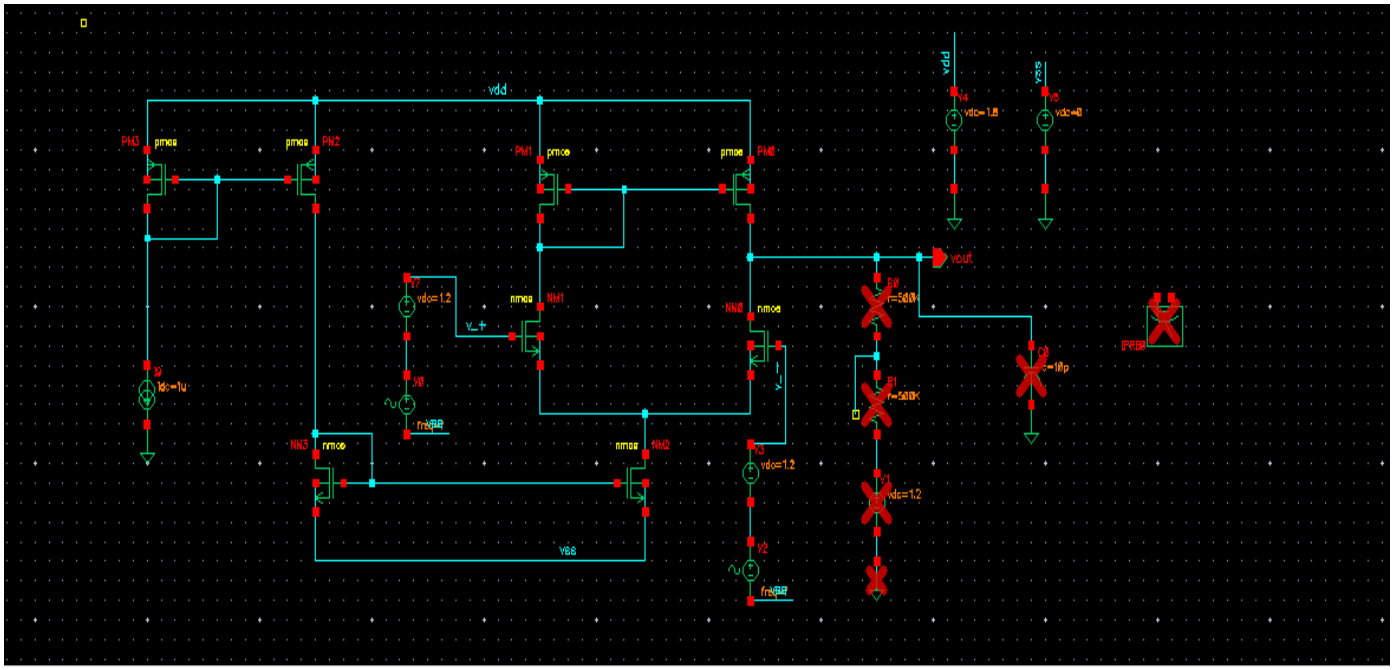

Fig3: Schematic for (Differential gain schematic)

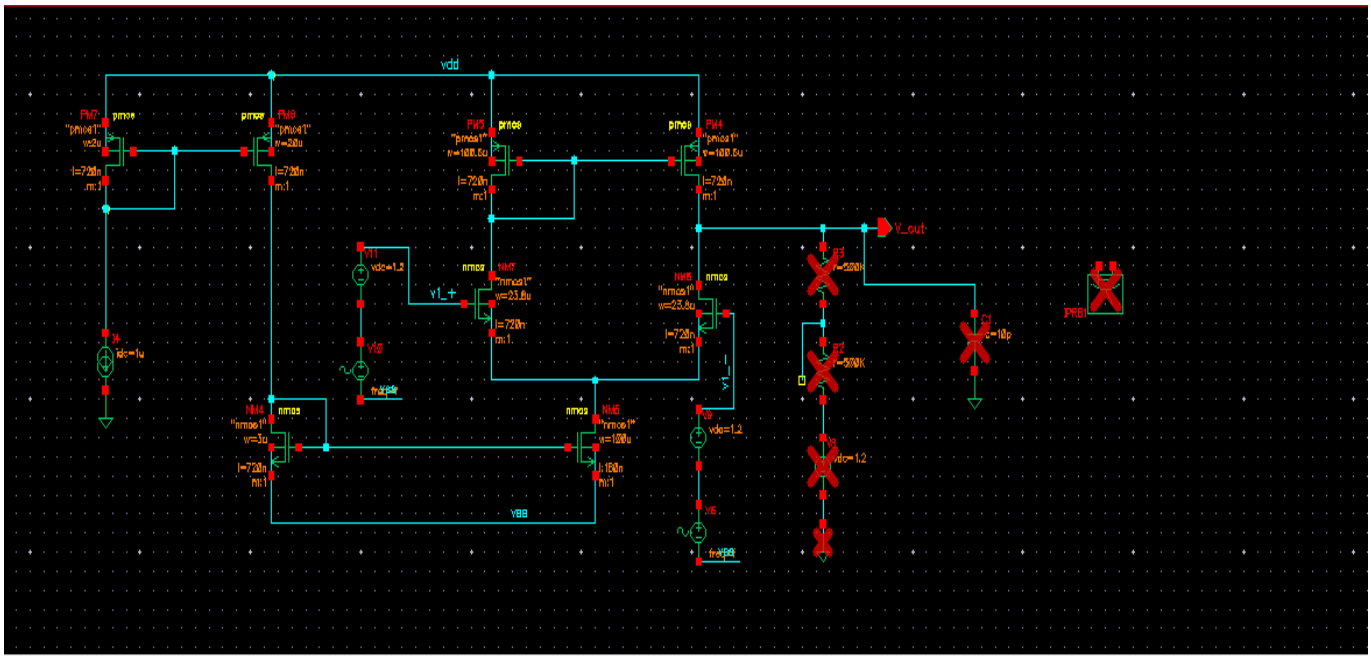

Fig4: Schematic for (Common mode gain)

Table 1: Loop gain and CMRR at different Temperatures

	0℃	27℃	70℃
Loop gain	29.8984 dB	29.0629 dB	27.8174 dB
CMRR	58.6187 dB	57.6038 dB	56.1679 dB

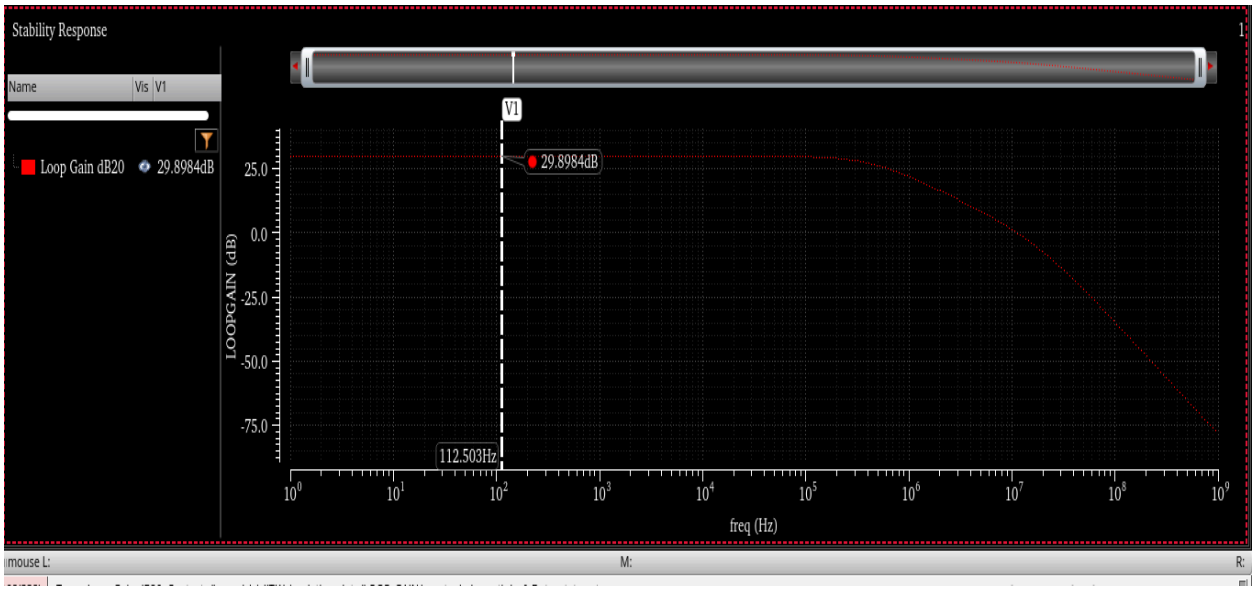

Fig5: Loop Gain at 0℃

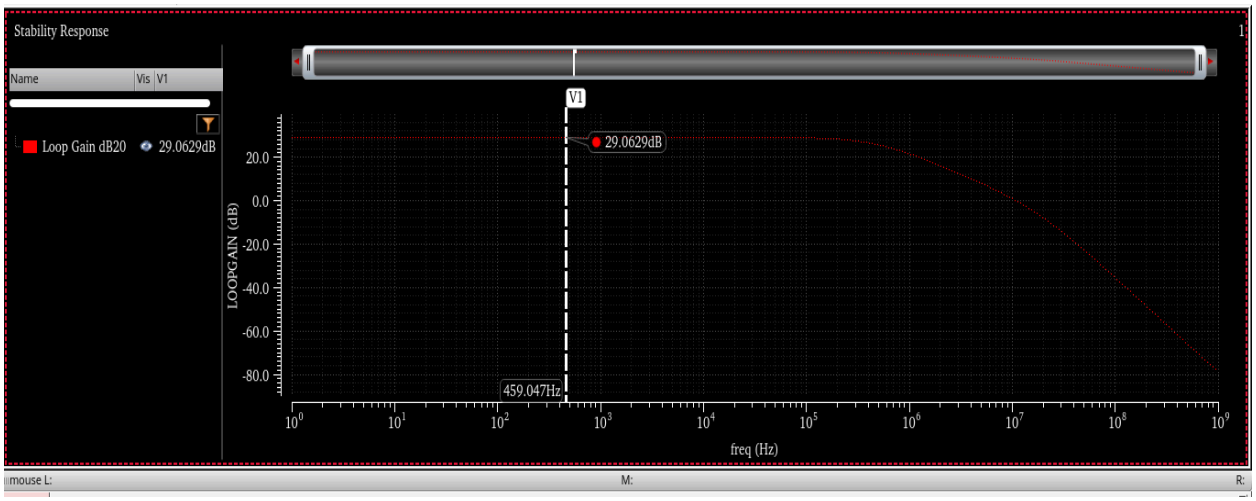

Fig6: Loop Gain at 27℃

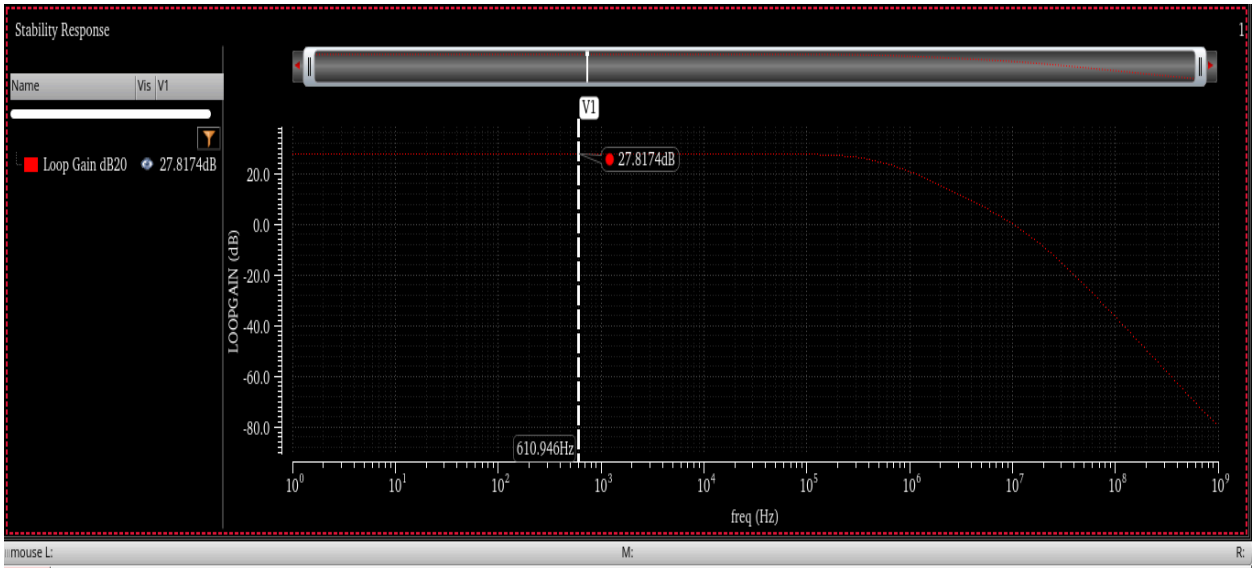

Fig7: Loop Gain at 70℃

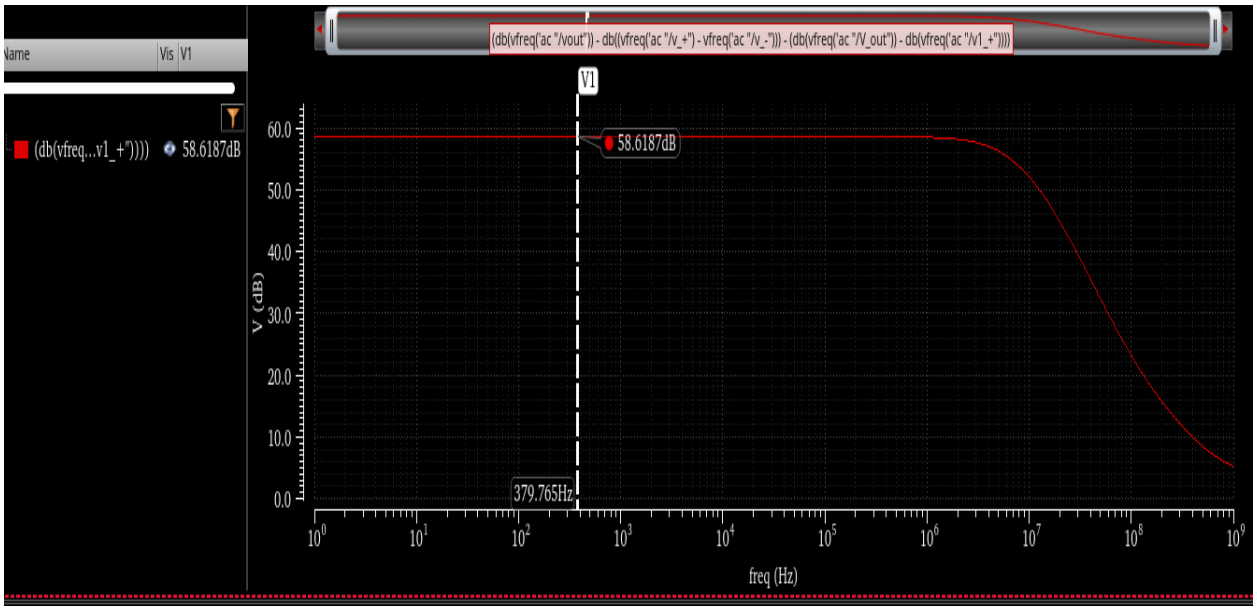

Fig8: CMRR at 0℃

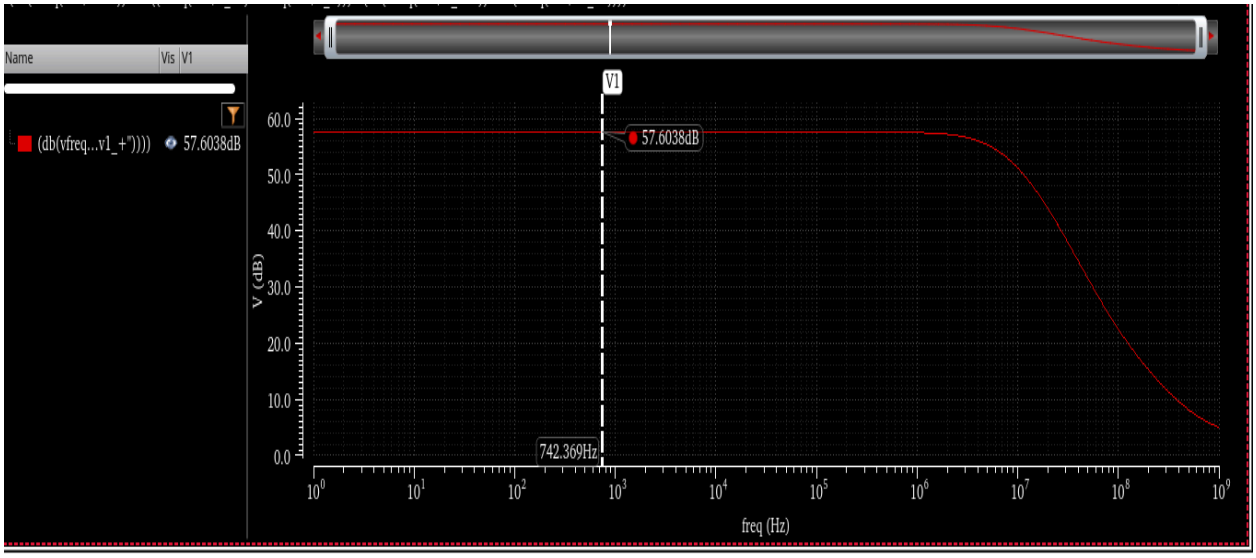

Fig9: CMRR at 27℃

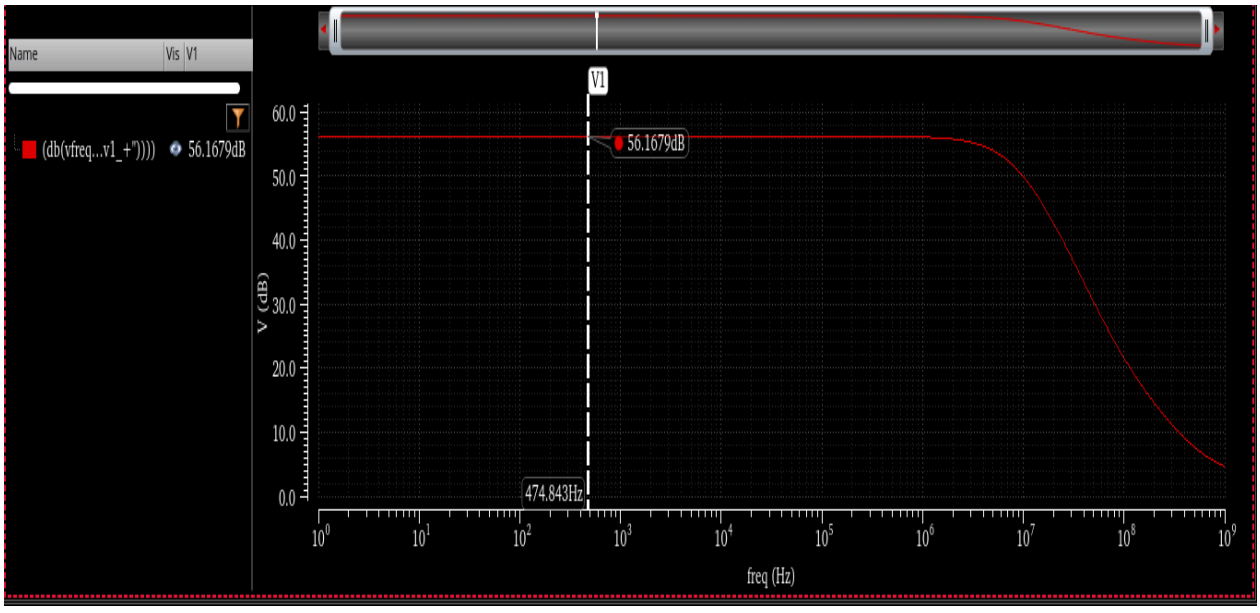

Fig10: CMRR at 70℃

Power Calculation

From dc analysis, Current across vdd= -836.48uA

Power= 1.8X(836.48)=1.505664 mW

3 dB Bandwidth at (27°C)

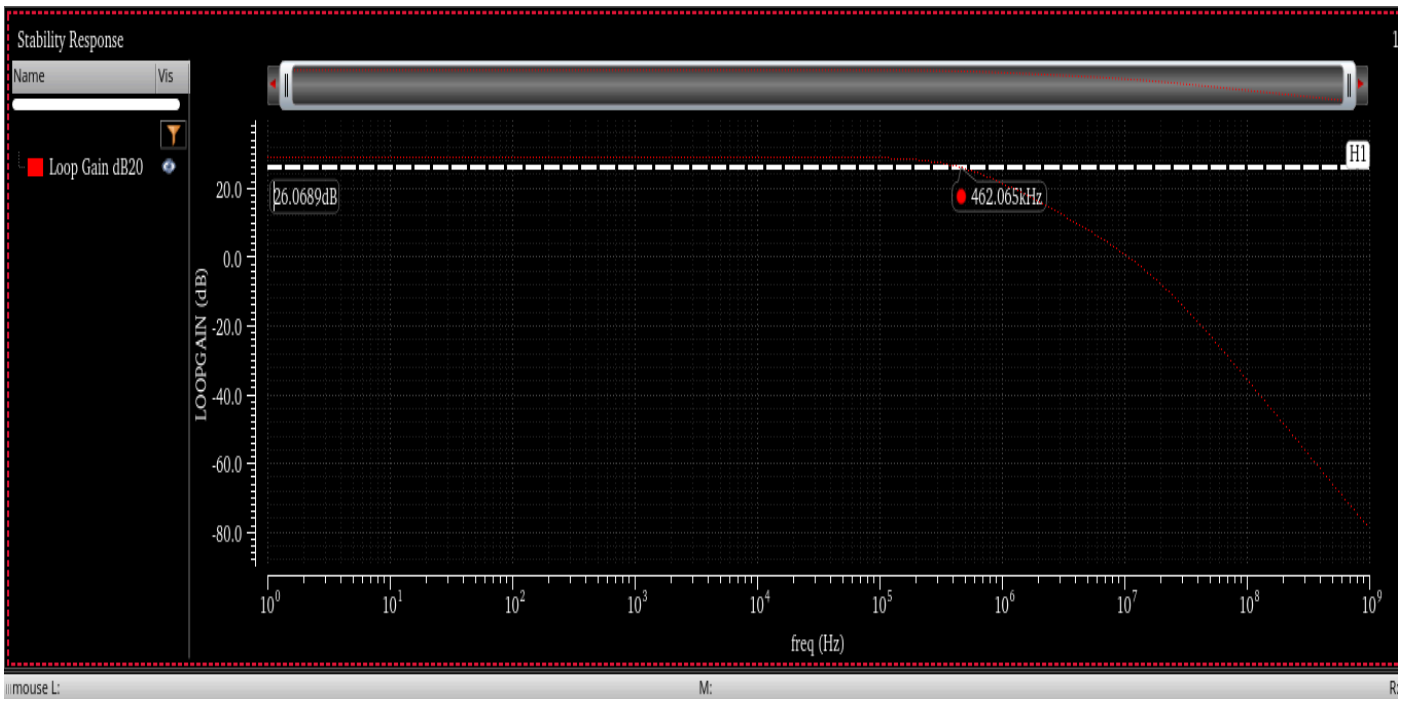

Fig11: 3dB Bandwidth at **27**°C is 462.05 KHz

Design Methodology

First I have done nmos analysis and figuring out the length of transistors to be used in differential pairs.
Since 25dB of gain was required to achieve so in order to achieve this,
For this I assumed Aβ=32 dB to achieve gain greater than 25dB then from this I got, gm /gds value approximately =159.24. And found out the corresponding length. Then I made a nmos circuit schematic for nmos characterisation.

1) Nmos analysis

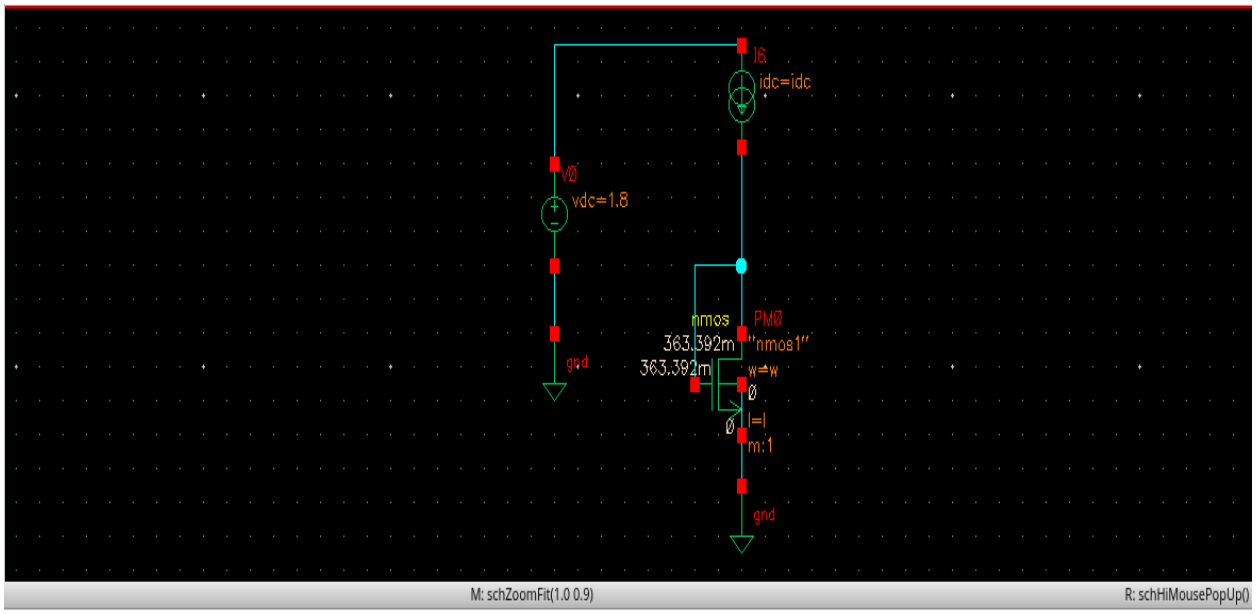

Fig12: Nmos schematic

- Now after this I sweep the length from L= 180 nm to L=900 nm and plot the gm/gds vs Id graph for different lengths as in figure 13 . Then check the length at which the gm/gds value line is cutting it. So from the graph I checked it length coming out to be 720nm.
- So from this I got length for the transistors of differential pairs =720nm

- The plot for gm/gds at different lengths (180nm,360 nm,540 nm,720nm and 900nm is obtained.

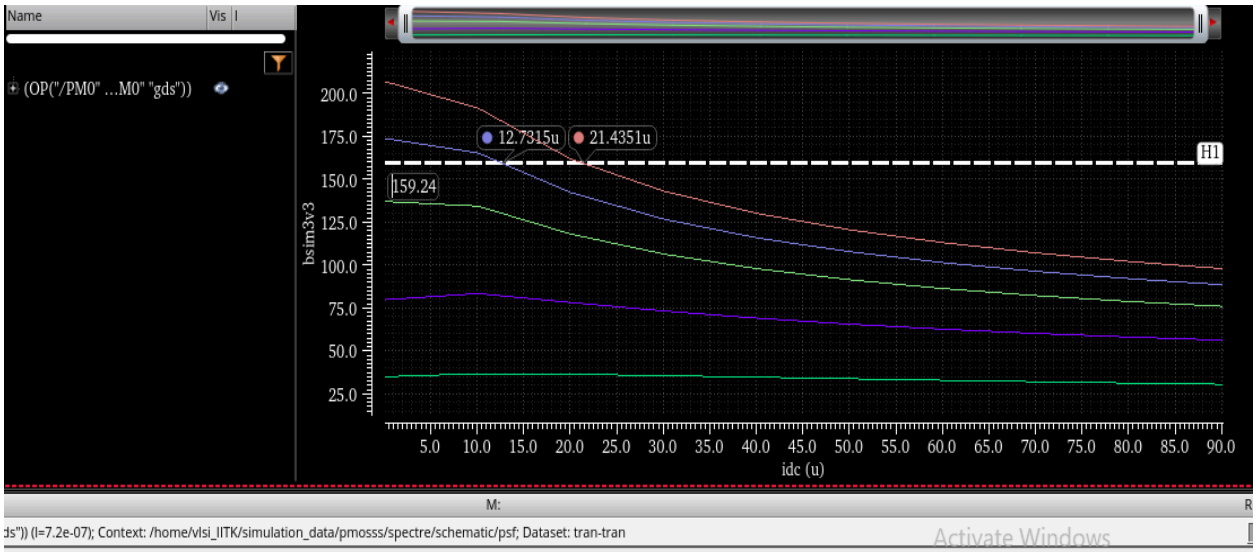

Fig13: gm/gds vs Id for different lengths

- The gm/gds line is cutting at L=720 nm and 900nm , I took 720nm.(fig 13)

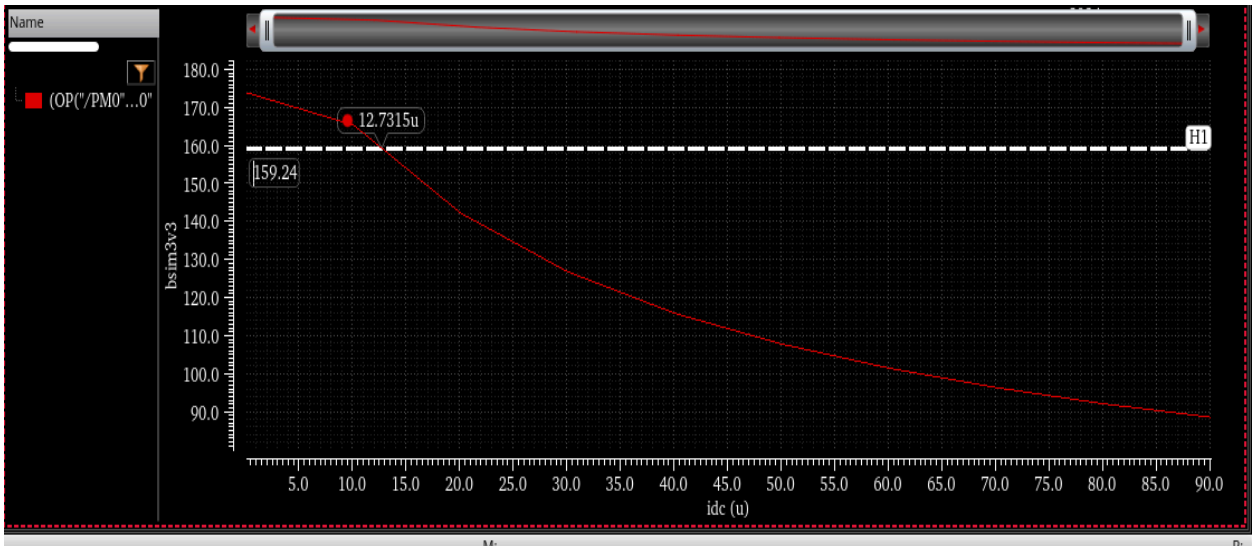

Fig14: gm/gds vs Id for L=720nm

- gm/gds vs Id for L=720nm , Id=12.7315u

- Plot for gm/gds vs id/w at L=720 nm and from this Id/w=6.3658

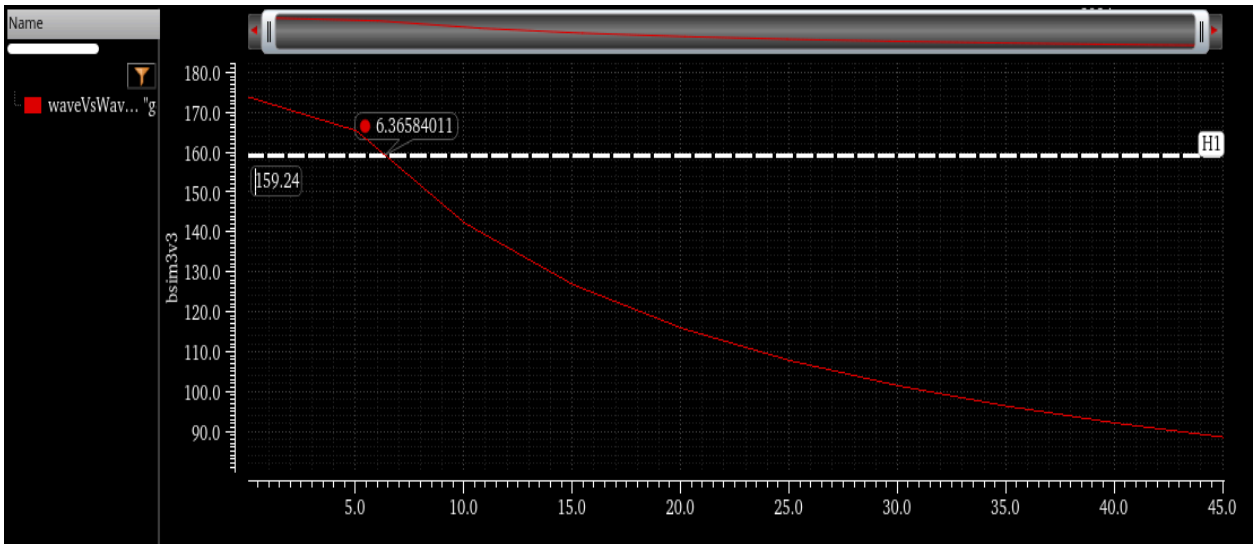

Fig15: gm/gds vs id/w

- gm/Id coming out to be 10.53931/V (fig 16)

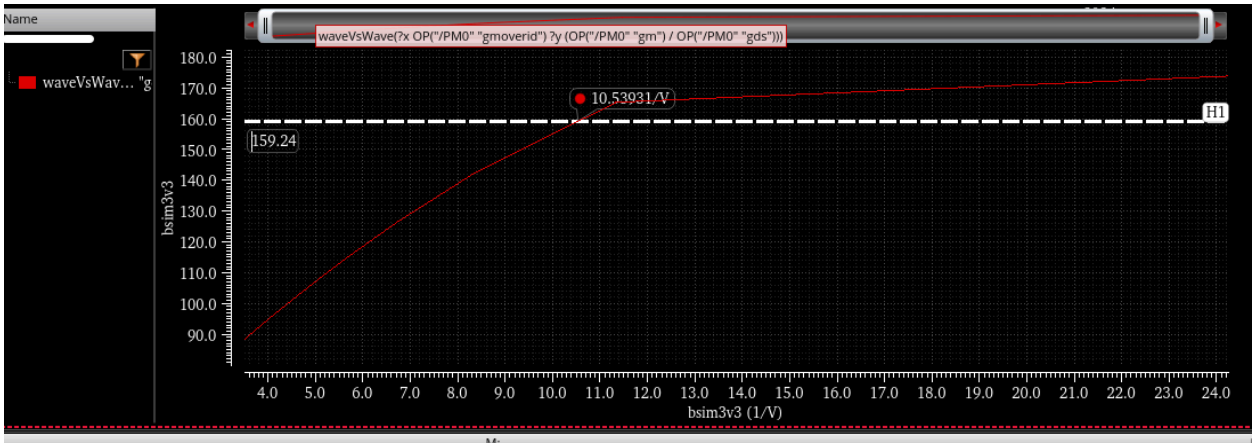

Fig16: gm/gds vs gm/Id

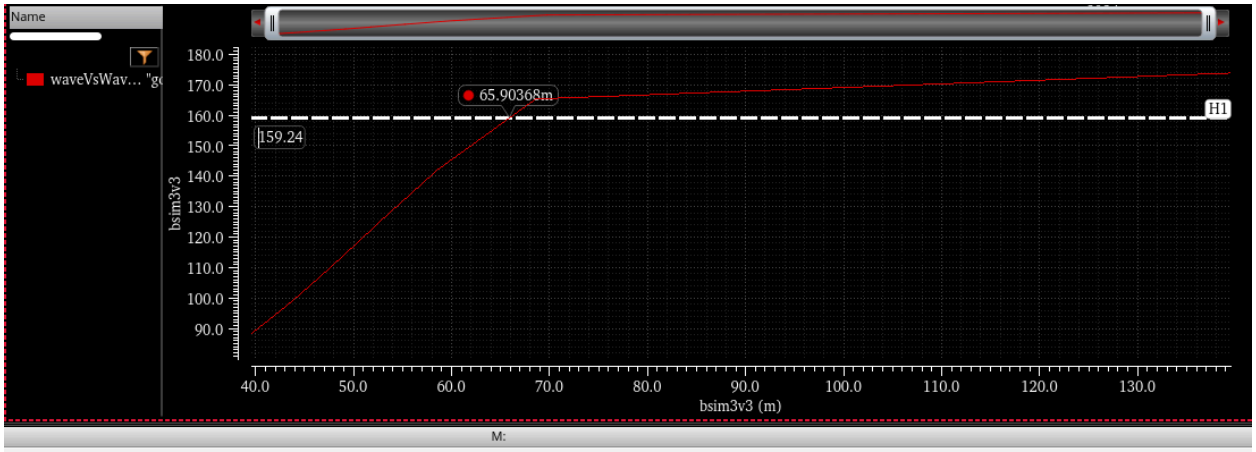

Fig17: gm/gds vs gds/id

Calculations for length and width of nmos transistor

- gm/gds vs Id for L=720nm , Id=12.7315
- From the plot for gm/gds vs id/w at L=720 nm and from this Id/w=6.3658
- gm/Id coming out to be 10.53931/V (fig 16)
- gds/Id comes out to be 65.90368m
  Now by assuming value of gd=10u,
  and gds/Id=65.90368m,
  and using the ratio (Id/W)

I got the width of nmos transistor to be 23.8 um and length= 720nm

2. Pmos Analysis

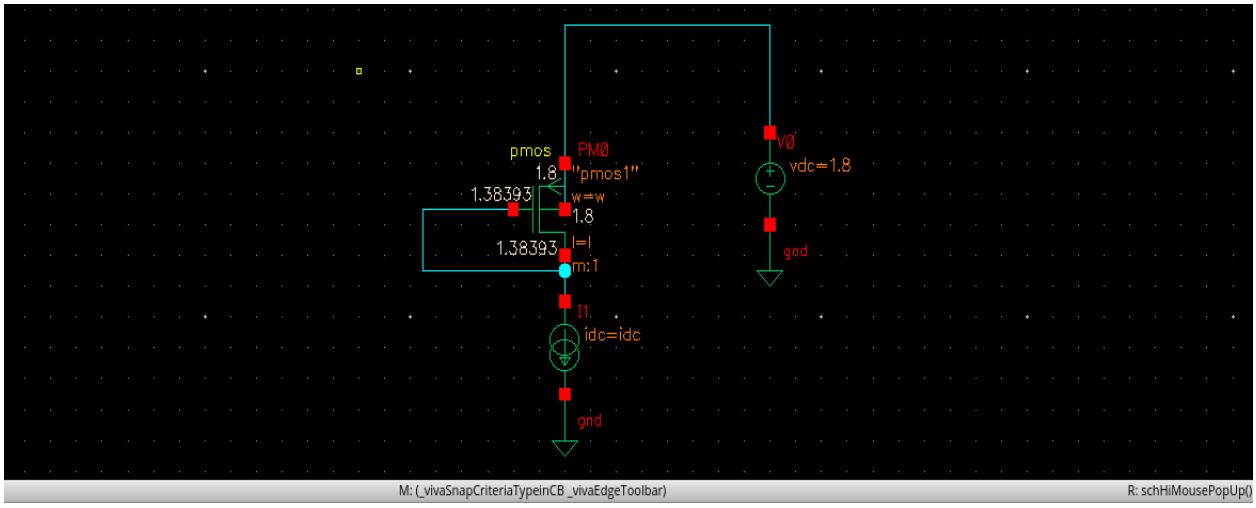

Fig18: Schematic for pmos analysis

Plot for gm/gds vs gds/Is for a pmos, from this i got gm/gds=141.0308 (fig19)

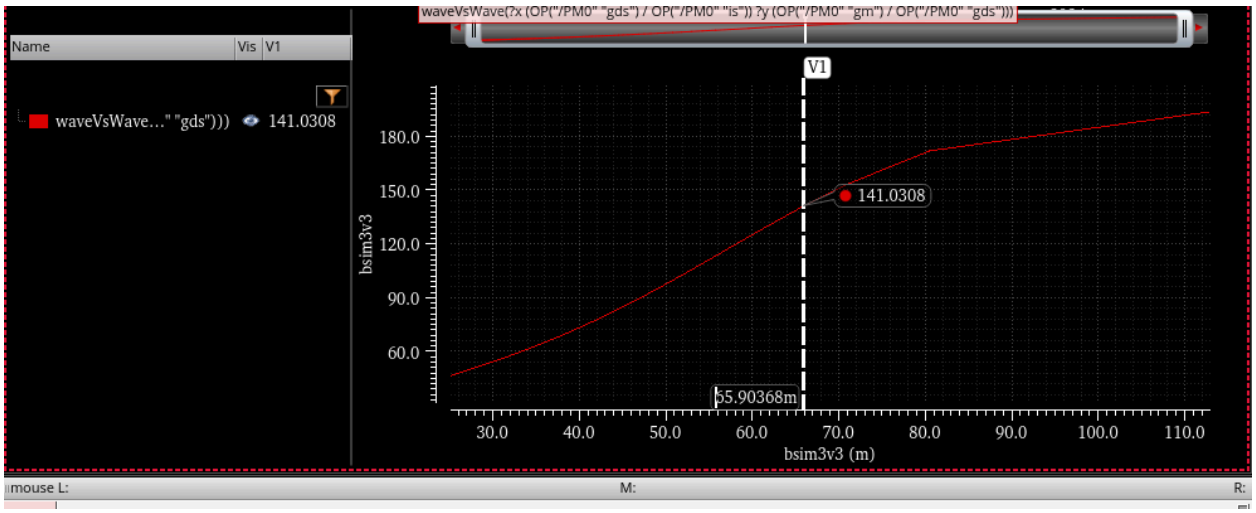

Fig19: gm/gds vs gds/Is

Now from the fig(20) gds/is vs is/w i got is/w=1.50761

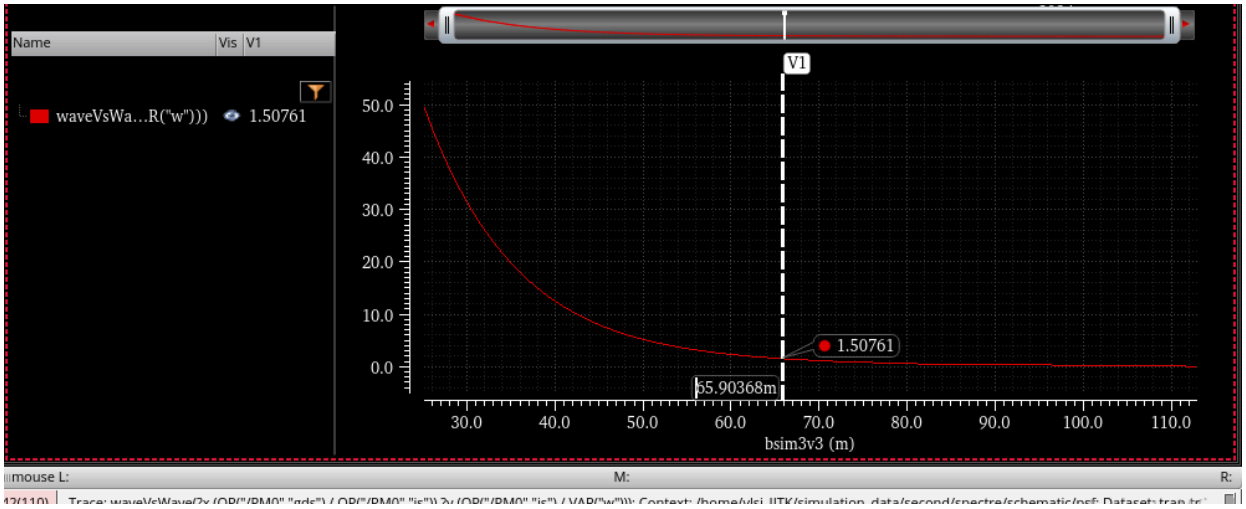

Fig20: gds/Is vs Is/w

Now from this plot (fig21) gm/gds vs gmoverId , i got gmoverid=9.30041/V

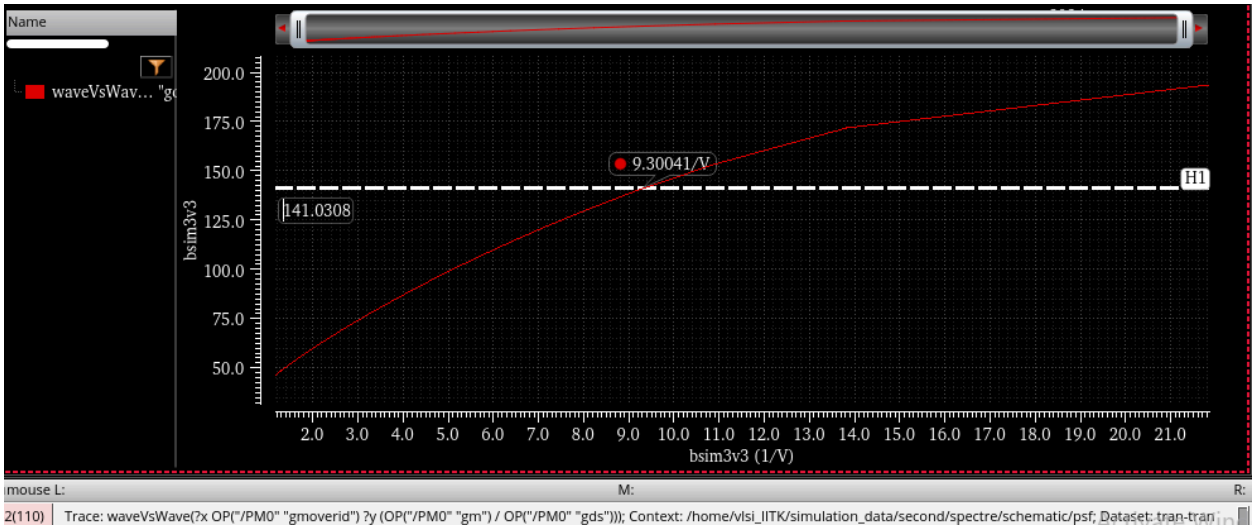

Fig21: gm/gds vs gmoverId

Calculations for length and width of pmos transistor

From plot for gm/gds vs gds/Is for a pmos, from this i got gm/gds=141.0308 (fig19).
Now from the fig(20) gds/is vs is/w i got is/w=1.50761
gmoverid=9.30041/V

Using the above relations I got width for pmos=100.622um and length is kept at 720nm.
Since we cannot enter a width of greater than 50 um directly , I adjusted fingers and finger width accordingly.

Current Mirror Implementation
Now I have been given the current source of 1uA, now I have to use this current source to get the current value required in the tail of the circuit which I have observed from my schematic after dc analysis. Initially the nmos below the circuit was not coming in the saturation region so I tweaked the width and length of nmos and pmos used in the current mirror so that all my mosfets are in region 2 (saturation). After I achieved all the mosfets in region 2, then connected the given R and C and then I calculated loop gain and cmrr at different temperatures as required.
The results I got are written in above table 1.