PWM Controller Register Configuration

- **PWM Controller Registers Information :**

Sr.No	Name	Address (Hex)	Width (bits)	Access (R/W)	Description
1	pwm_clock_divide	0x00	32	R/W	Clock Divider
2	pwm_duty_cycle	0x01	32	R/W	Duty Cycle
3	pwm_enable	0x02	32	R/W	Enable

- **Detailed Explanation :**

1. Clock Divider :

- **Address** : 0x00

- **Description** : This register is used to set frequency for the pwm operation by using following formula.

- **clk_divide** = $\dfrac{\text{Oscillator Frequency} - \text{Desired Frequency}}{\text{Desired Frequency}}$

- **Example** :
  - Oscillator Frequency = 100 MHz
  - Desired Frequency = 100 KHz,
  - clk_divider = $\dfrac{100 \text{ MHz} - 100 \text{ KHz}}{100 \text{ KHz}}$ = 999

- **Conclusion** : To get 100 KHz from 100 MHz frequency, "999" value should be loaded in the clock divide register.

2. Duty Cycle :

- **Address** : 0x01

- **Description** : This register is used to set the duty cycle (on-off times for the motor) by using following formulae.

- **ON-Time of desired frequency :**
  - ➢ ON-Time = (clk_divider - duty_cycle + 1) x (Osc_clk_period)

- **OFF-Time of desired frequency :**
  - ➢ OFF-Time = (duty_cycle) x (Osc_clk_period)

- **Example** :
  - Osc_clk_period = 10 ns (i.e. for 100 MHz clock)
  - clk_divider   = 999
  - duty_cycle   = 12
  - ON-Time   = (999 – 12 +1) x (10) ns = 9880 ns
  - OFF- Time   = (12) x (10) ns = 120 ns
- **Conclusion** : To rotate motor at fast speed, ON time should be more and OFF time should be less and vice-versa.

3. **Enable** :
- **Address**   : 0x02

- **Description** : This is called "pwm enable register". If this " 0 " then pwm output is "zero" and if it is " 1 " then pwm output is according to the values set in clock divider and duty cycle registers.