Cursul 4_2
Citeste Instructiunea & Intrerupere (IF)

Locatia	Eticheta	Destinatia	UAL	Sursa 1	Sursa 2	Constanta	Diverse	Conditia	Eticheta Salt	Observatii
0	ifetch:							intr?	intr:	Verificare cerere intr.
1	iloop:						cit.instr:	Mready?	iloop:	RI ←M[CP]
2		СР	ADD	СР	const.	4	TS1 ← RG[rs]	DCD1?		Decodifica
							TS2← RG[rt]			
3	intr:	RAI	PASS S1	CP						Intrerupere
4		СР	PASS S2		const.	0		necond	ifetch:	
Incarca	& Memo	reaza & T	ransfera	(RD)						
Locatia	Eticheta	Destinatia	UAL	Sursa 1	Sursa 2	Constanta	Diverse	Conditia	Eticheta Salt	Observatii
5	mem:	RA	ADD	TS1	imed16			incarca?	load:	Instructiune de memorare
6	store:	RD	PASS S1	TS2						Memoreaza
7	dloop:						scrie date	Mready?	Dloop:	

Cursul 4_2

Locatia	Eticheta	Destinatia	UAL	Sursa 1	Sursa 2	Constanta	Diverse	Conditia	Eticheta Salt	Observatii
8								necond	ifetch:	Salt la citeste instructiunea
9	load:						cit. date:	Mready?	load:	$RD \leftarrow M[RA]$
10								DCD1?		Decodifica
11 12	LB:	TEMP T D	SLL SRA	RD TEMP	const const.	24 24		necond	write1:	Incarca octet cu semn extins Deplasare aritmetica dreapta
13	LBU:	TEMP	SLL	RD	const.	24				Incarca octet fara semn
14	store:	TD	SRL	TEMP	const.	24		necond	write1:	Deplasare dreapta logica
15	LH:	TEMP	SLL	RD	const.	16				Incarca semicuvant
16		TD	SRA	TEMP	const.	16		necond	write1:	Deplasare dreapta aritmetica
17	LHU:	TEMP	SLL	RD	const.	16				Incarca semicuvant fara semn
18		TD	SRL	TEMP	const.	16		necond.	write1	Deplasare dreapta logica
19	LW:	TD	PASS S1	RD				necond.	write1	Incarca cuvant
20	MOVI2S:	RAI	PASS S1	TS1				necond.	ifetch:	Incarca registrul special
21	MOVS2I:	TD	PASS S1	RAI						Incarca de la registrul special
22	write1:						$ $ RG[rd] \leftarrow TD	necond.	ifetch:	Memoreaza rezultatul in RG

Operatii UAL

Locatia	Eticheta	Destinatia	UAL	Sursa 1	Sursa 2	Constanta	Diverse	Conditia	Eticheta Salt	Observatii
23		TEMP	PASS S2		TS2			DCD2:		TEMP ← Registru
24		TEMP	PASS S2		imed16			DCD3:		TEMP← imed16
25	ADD/I:	TD	ADD	TS1	TEMP			necond	write2:	Adunare
26	SUB/I:	TD	SUB	TS1	TEMP			necond	write2:	Scadere
27	AND/I:	TD	AND	TS1	TEMP			necond	write2:	Produs logic
28	ORI/I:	TD	OR	TS1	TEMP			necond	write2:	Suma logica
29	XOR/I:	TD	XOR	TS1	TEMP			necond	write2:	SAU Exclusiv
30	SLL/I:	TD	SLL	TS1	TEMP			necond	write2:	Deplasare logica stanga
31	SRL/I:	TD	SRL	TS1	TEMP			necond	write2:	Deplasare logica dreapta
32	SRA/I:	TD	SRA	TS1	ТЕМР			necond	write2:	Deplasare aritmetica dreapta
33	LHI:	TD	SLL	TEMP	const.	16		necond	write2:	Incarca jumatatea superioara
34	write2:						RG[rd] ←TD	necond	ifetch:	

Executia instructiunilor SET

Locatia	Eticheta	Destinatia	UAL	Sursa 1	Sursa 2	Constanta	Diverse	Conditia	Eticheta Salt	Observatii
35	SEQ/I:		SUB	TS1	TEMP			zero?	set1:	Set la egal
36		TD	PASS S2		const	0		necond	write3:	Set fals
37	SNE/I:		SUB	TS1	TEMP			zero?	set0:	Set la diferit
38		TD	PASS S2		const	1		necond	write3:	Set fals
39	SLT/I:		SUB	TS1	TEMP			negativ?	set1:	Set la mai mic
40		TD	PASS S2		const	0		necond	write3:	Set fals
41	SGE/I:		SUB	TS1	TEMP			negativ?	set0:	Set la mai mare sau egal
42		TD	PASS S2		const	1		necond	write3:	Set fals
43	SGT/I:		SUB	TEMP	TS1			negativ?	set1:	Set la mai mare
44		TD	PASS S2		const	0		necond	write3:	Set fals
45	SLE/I:		SUB	TEMP	TS1			negativ?	set0:	Set la mai mic sau egal
46		TD	PASS S2		const	1		necond	write3:	Set adevarat
47	set0:	TD	PASS S2		const	. 0		necond	write3:	Set fals
48	set1:	TD	PASS S2		const	1		necond	write3:	Set adevarat
49	write3:						$RG[rd] \leftarrow TD$	necond.	ifetch:	Memoreaza rezultatul in RG

Executia Instructiunilor de Ramificare si Salt

Locatia	Eticheta	Destinatia	UAL	Sursa 1	Sursa 2	Constanta	Diverse	Conditia	Eticheta Salt	Observatii
50	beq:		SUB	TS1	const	0		zero?	branch:	Ramificare la egal
51								necond	ifetch:	Ramificare neexecutata
52	bne:		SUB	TS1	const	0		zero?	branch:	Ramificare la diferit
53	branch:		ADD	СР	imed16			necond	ifetch:	Ramificare executata
54	jmp:	СР	ADD	СР	imed26			necond	ifetch:	Ramificare executata
55	jreg:	СР	PASS S1	TS1				necond	ifetch:	Ramificare executata
56	jal:	TD	PASS S1	СР						Salt cu legatura
57		СР	ADD	СР	imed26		$RG[31] \leftarrow TD$	necond	ifetch:	Ramificare executata
58	jalr:	TD	PASS S1	CP						Salt cu legatura registru
59		СР	ADD	TS1			RG[31] ← TD	necond	ifetch:	Ramificare executata
60	trap:	RAI	PASS S1	СР						Capcana - Trap
61		СР	PASS S2		const	16		necond	ifetch:	

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