# MT2625 Datasheet

Version: 1.5

Release date: 1 June 2018

# Document Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 18 January 2018 | Initial release |
| 1.1 | 29 January 2018 | Update Features, Figure1.2-1, Figure5.5-2, Table6.1-2, Table6.2-1, Ch7.2 |
| 1.2 | 31 January 2018 | Update Table2.5-2, Table4.3-1 |
| 1.3 | 7 February 2018 | Update Table 5.4-2, Ch.6.2.2 |
| 1.4 | 23 March 2018 | Update Features (I2S interface), Figure 2.5-1 |
| 1.5 | 1 June 2018 | Update Ch.2.3.6 |

# Features

**NB-IoT transceiver**

- Compliant with 3GPP R13/R14 NB-IoT standard
- Supports DL 200kHz bandwidth/UL single tone and multi-tone
- Supported RF bands: B1/B2/B3/B5/B8/B11/B12/B13/B17/B18/B19/B20/B21/B25/B26/B28/B31/B66/B70/B71
- Supports PSM and eDRX mode

**Microcontroller subsystem**

- ARM® Cortex®-M4 with FPU and MPU
- 14 DMA channels
- One RTC timer, one 64-bit and five 32-bit general purpose timers
- Development support: SWD, JTAG
- Crypto engine
  - AES 128, 192, 256 bits
  - DES, 3DES
  - MD5, SHA-1, 224, 256, 384, 512
- True random number generator
- JTAG password protection

**Memory**

- Up to 32KB SYSRAM, with zero-wait state
- Up to 32KB L1 cache, with high hit rate and zero-wait state
- Embedded 32Mbits flash
  - Sleep current 200nA
- Embedded 32Mbits pseudo SRAM
  - Sleep current 10µA

**Communication interfaces**

- Two SDIO 2.0 masters and one SDIO 2.0 slave
- Three I2C (3.4Mbps) interfaces
- Four UART interfaces (3Mbps, UART1/2 with hardware flow control)
- Two SPI masters and one SPI slave
- Two I2S interfaces
  - Both support 16/24-bit, master/slave mode
  - Both support 16, 24, 48, 96, 192kHz and 11.025kHz, 22.05kHz, 44.1kHz, TX/RX, 2 channels
- Four PWM channels
- 37 GPIOs (5V-tolerant)
- Seven IOs for BPI and MIPI interfaces
- Three IOs for SIM
- 5 channel 10-bit AUXADC (PinMux with GPIO), maximum input voltage 1.4V
- Embedded thermal sensor

**Power management**

- Three integrated high efficiency buck converters with low quiescent current
- Four integrated LDO regulators for RTC, SIM, RF frontend and GPIOs
- Operating temperature from -40°C to 85°C

**Clock source**

- 26MHz crystal oscillator
- 32kHz crystal oscillator or internal 32kHz oscillator for RTC

**Package**

- 5.6-mm x 5.6-mm x 1.05-mm TFBGA with 0.5-mm ball pitch

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# 1. System Overview

MediaTek MT2625 is a highly integrated chipset featuring an application processor, a low power multiband narrowband Internet of Things transceiver and a power management unit (PMU).

MT2625 is based on ARM® Cortex®-M4 with floating point microcontroller unit (MCU) integrated with 4MB PSRAM and 4MB flash memory. MT2625 also supports interfaces including UART, I2C, SPI, I2S, PWM, SDIO, ADC, USB, keypad and USIM.

The NB-IoT transceiver contains the 3GPP R13/R14 radio, baseband and MAC that are designed to meet low power and extended battery life application requirements.

## 1.1. MT2625X product family

***Table 1.1-1. Difference between all product series chipsets***

| Item | MT2625D series | | MT2625A series | |
|---|---|---|---|---|
| Product Number | MT2625DA | MT2625DPA | MT2625AA | MT2625APA |
| Package size | 5.6-mm x 5.6-mm x 1.05-mm | | 5.6-mm x 5.6-mm x 1.05-mm | |
| Package ball, pitch | 121-ball, 0.5mm pitch | | 121-ball, 0.5mm pitch | |
| SiP flash size | 32Mbits | | N/A | |
| SiP PSRAM size | 32Mbits | | 32Mbits | |
| ARM® Cortex®-M4 operation frequency | 78 MHz | 156 MHz | 78 MHz | 156 MHz |
| PSRAM operation frequency | 39 MHz | 78 MHz | 39 MHz | 78 MHz |
| Flash operation frequency | 78MHz | | 78MHz | |

## 1.2. System architecture

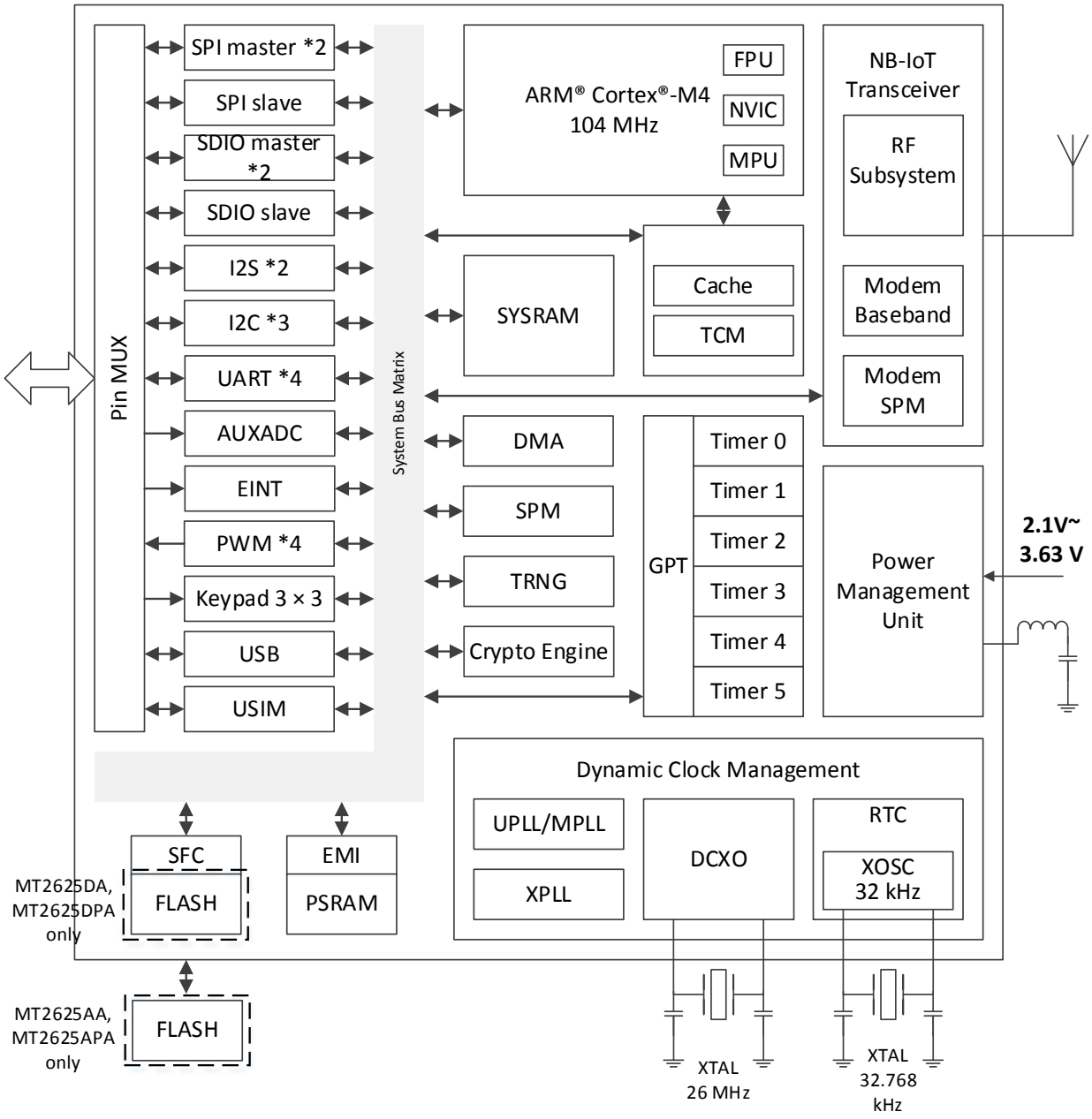



***Figure 1.2-1. MT2625 chipset architecture***

## 1.3. Platform features overview

### 1.3.1. Host processor subsystem

- ARM® Cortex®-M4 with FPU application processor
- 32kB L1 cache with high hit rate and zero wait state
- eXecute In Place (XIP) on flash memory

### 1.3.2. Memory

- SiP 32Mb low power flash memory with 0.2µA deep-down current (typical condition)
- SiP 32Mb low power PSRAM with 10µA half-sleep mode current
  (current condition: PASR 1/8 at 25°C 1x refresh)
- 32kB SYSRAM with zero wait state

### 1.3.3. Peripheral interfaces

The following interfaces are multiplexed with GPIO.

- Two SPI master interface, 1, 2, 4-bit mode, up to 52MHz
- One SPI slave interface, 1, 2, 4-bit mode, up to 52MHz
- Two SDIO host interface (v2.0)
- One SDIO device interface (v2.0)
- One USB interface (v1.1)
- 3x3 keypad
- Two I2S interface supporting 16 or 24-bit, master or slave mode
  (supports 16, 24, 48, 96, 192, 11.025, 22.05 and 44.1kHz sample rates, transmit and receive, two channels)
- Up to four UART interfaces, UART1/2 with hardware flow control (~3Mbps)
- Up to three I2C master interfaces (3.4Mbps)
- Up to five channels of 10-bit ADC
- Up to four PWM channels

***Table 1.3-1. MT2625 series peripherals***

| Peripheral | Counts | Description |
|---|---|---|
| **Keypad** | 3x3 keypad scanner | with double key detection |
| **PWM** | 4 | - |
| **UART** | 4 | up to 3Mbps, UART1/2 support RTS/CTS |
| **USB** | 1 | v1.1, require external LDO for USB |
| **I2C** | 3 | master mode, 400kbps, Up to 3.4Mbp |
| **I2S** | 2 master/slave | - |
| **MSDC** | 2 master | v2.0, up to 52MHz, 1-bit/4-bit mode<br>eMMC4.41 , no booting and not support DDR mode |
| **SDIO** | 1 slave | v2.0, up to 52MHz, external host booting via SDIO |
| **SPI** | 2 master | clock up to 52MHz, 1-bit/2-bit/4-bit |
| **SPI** | 1 slave | clock up to 52MHz, 1-bit/2-bit/4-bit, external host booting via SPI |
| **SIM** | 1 | no support 3V SIM if non-chargeable battery |
| **AUXADC** | 5-channel | 10-bit ADC, pin mux by AGPIO |
| **GPIO** | 37 | all pins with interrupt except GPIO0 |

### 1.3.4. Security

- Crypto engine that supports AES, DES/3DES, MD5, SHA1/SHA2
- True random number generator

### 1.3.5. Others

- Up to 37 GPIO interfaces with 5V-tolerant fast IOs, each IO can be configured as an external interrupt source
- 27 DMA channels
- Single RTC timer, one 64-bit and five 32-bit general purpose timers (GPTs)

## 1.4. Modem features overview

- Compliant to 3GPP 36.101 R13/R14 category NB1/NB2
- Supported bands include EUTRA 1, 2, 3, 5, 8, 12, 13, 17, 18, 19, 20, 25, 26, 28, 66 and 70.
- Optional bands are EUTRA 11, 21, 31, and 71.
- Low power 1.3-V single-ended Saw-Less RX and Polar TX.
- Built-in low dropout linear regulators that are powered by switching regulator

## 1.5. Power management unit (PMU) features overview

- Wider input voltage range 2.1V to 3.63V
- Four Low Drop-out Regulators (LDOs) and three high efficiency buck converters
- Contains Under-Voltage Lockout (UVLO) circuit and a reference band-gap circuit

## 1.6. Package

- For MT2625, a TFBGA of 5.6mm*5.6mm, 121-ball, 0.5mm pitch package is offered.

# 2. Functional Description

## 2.1. Host processor subsystem

### 2.1.1. ARM® Cortex®-M4 with FPU

The Cortex-M4 with FPU is a low-power processor with 3-stage pipeline Harvard architecture. It has reduced pin count and low power consumption and delivers very high performance efficiency and low interrupt latency, making it ideal for embedded microcontroller products.

The processor incorporates:

- IEEE754-compliant single-precision floating-point computation unit (FPU).
- A Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing.
- Enhanced system debugging with extensive breakpoint.
- An optional Memory Protection Unit (MPU) to ensure platform security robustness.

The Cortex-M4 executes the Thumb®-2 instruction set with 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers. The instruction set is fully backward compatible with Cortex-M3/M0+.

MT2625 has further enhanced the Cortex-M4 with FPU to reduce the power by another 11% (in Dhrystone) compared to the original Cortex-M4. Low power consumption is a significant feature for IoT and Wearables application development.

### 2.1.2. Cache controller

A configurable 32kB cache is implemented to improve the code fetch performance when CPU accesses a non-zero wait-state memory such as EMI, external flash or boot ROM through the on-chip bus.

The core cache is a small block of memory containing a copy of a small portion of cacheable data in the external memory. If CPU reads a cacheable datum, the datum will be copied to the core cache. Once CPU requests the same datum again, it can be obtained directly from the core cache (called cache hit) instead of fetching it again from the external memory to achieve zero wait-state latency.

The cache can be disabled and this block of memory can be turned into tightly coupled memory (TCM), a high-speed memory for normal data storage. The sizes of TCM and cache can be set to one of the following four configurations:

- 32kB cache, 64kB TCM
- 16kB cache, 80kB TCM
- 8kB cache, 88kB TCM
- 0kB cache, 96kB TCM

### 2.1.3. Memory management

Three types of memories are implemented for use:

- On-die memories (SRAMs) with up to 32kB at CPU clock speed with zero wait state.
- Embedded flash of 32Mbits to store programs and data
- Embedded pseudo SRAM (PSRAM) of 32Mbits for application storage

The SRAMs are composed of TCMs and L1 caches. The L1 cache (up to 32kB) is implemented to improve processor access performance of the long latency memories (flash and PSRAM).

TCMs are designed for applications requiring high speed, low latency and low power consumption. Each TCM has its own power state; active, retention or power-down. TCM must be in active state for normal read and write access. Retention state saves the SRAM content and consumes the minimum leakage current with no access. Power-down state loses the content and consumes almost zero power.

The TCMs can also be accessed by other internal AHB masters like DMA or multimedia subsystem for low power applications. These applications can run on TCM without powering on PSRAM or flash to save more power.

Boot ROM is also implemented for processor boot–up and its content is unchangeable.

### 2.1.4. Memory protection unit (MPU)

The MPU is an optional component to manage the CPU access to memory. The MPU provides full support for:

- Protection regions (up to 8 regions and can be further divided up into 8 sub-regions).
- Overlapping protection regions, with region priority.
- Access permissions.
- Exporting memory attributes to the system.

The MPU is useful for applications where a critical code has to be protected against misbehavior of other tasks. It can be used to define access rules, enforce privilege rules and separate processes.

### 2.1.5. Nested vectored interrupt controller (NVIC)

The NVIC supports up to 76 maskable interrupts and 16 interrupt lines of Cortex-M4 with 128 priority levels. The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable tail-chaining of interrupts. The processor supports both level and pulse interrupts with programmable active-high or low control.

### 2.1.6. External interrupt controller

The external interrupt controller consists of up to 32 edge/level detectors for generating event/interrupt requests. Each input line can be independently configured to select the type (interrupt or event) and the corresponding trigger event (rising edge or falling edge or both or level). Each line can also be masked independently. A pending register maintains the status line of the interrupt requests. Up to 37 GPIOs can be connected to 23 external interrupt lines.

## 2.2. Platform description

### 2.2.1. Boot mode

- Internal or external booting device, flow control

There are three boot source options:

- Serial flash
- SPI slave (to load binary from host)
- SDIO slave (to load binary from host)

The host may transmit a binary through SPI slave or SDIO slave to internal SRAM. The MCU (Cortex-M4) can execute on internal SRAM after transmission is complete.

The boot source in boot ROM is determined according to the flowchart shown in Figure 2.2-1. HIF_EN and HIF_SEL can be configured at power up using BPI_2 and BPI_3, respectively.

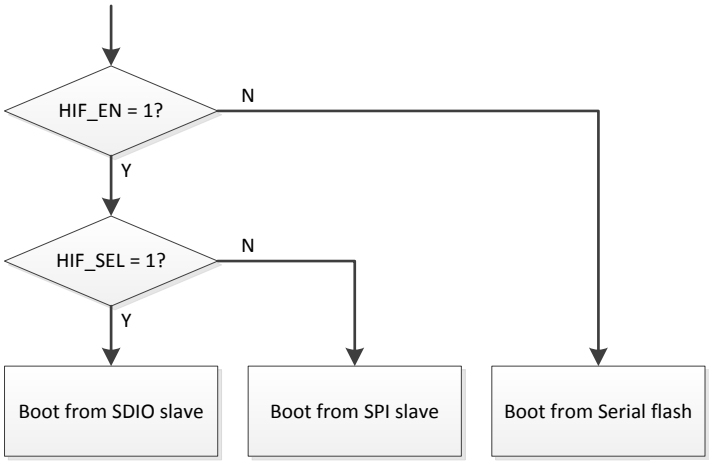



***Figure 2.2-1. Boot source flow***

## 2.2.2. Trapping and mode selection

| Mode selection | Pin name | Description | Trapping condition |
|---|---|---|---|
| 32kHz clock source select | BPI1 | GND : 32kHz source is from external (default)<br>DVDD_IO_1 : 32kHz source is from internal (divided from 26MHz clock) | Power-on reset |
| Boot with host interface (HIF_EN) | BPI2 | GND : Boot with host interface disabled (default)<br>DVDD_IO_1 : Boot with host interface enabled | Power-on reset |
| Host interface select (HIF_SEL) (active if HIF_EN is enabled) | BPI3 | GND : Host interface via SPI slave (**default, HIF_SEL must keep GND level, if HIF_EN is "GND"**)<br>DVDD_IO_1 : Host interface via SDIO slave | Power-on reset |
| System Level Test (SLT) mode | BPI4 | GND : Normal mode (default)<br>DVDD_IO_1 : SLT mode | Power-on reset |
| USB download | GPIO0 | GND : Enter USB download mode in Boot ROM<br>DVDD_IO_2 : No USB download in Boot ROM (default) | Power-on reset or system reset |

Note 1: Strapping resistors for default option are implemented as internal pull-down or internal pull-up 47kΩ.

Note 2: If non-default option is used, it is recommended to use pull-down or pull-up 10kΩ as external strapping resistors.

Note 3: **HIF_SEL must keep GND level, if HIF_EN is "GND".**

### 2.2.3. General purpose timer (GPT)

The GPT includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes; ONE-SHOT, REPEAT, freerun with interrupt (FREERUN_I), and FREERUN, and can operate on one of the two clock sources; RTC clock (32.768kHz) and system clock (13MHz).

### 2.2.4. Interrupt controller

The NVIC supports up to 76 maskable interrupts and 16 interrupt lines of Cortex-M4 with 128 priority levels. The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable tail-chaining of interrupts. The processor supports both level and pulse interrupts with programmable active-high or low control.

### 2.2.5. Real-time clock (RTC)

The RTC module provides time and data information, as well as 32.768kHz clock source. The clock is selected between three clock sources — one from an external (XOSC32) and two from an internal (XO, EOSC32). The RTC block has an independent power supply switch. In addition to providing timing data, an alarm interrupt will be generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches the maximum value. The year span is supported up until 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

## 2.3. Peripheral description

### 2.3.1. USB1.1 full-speed device controller

The USB11 device controller supports only full-speed (12Mbps) operation. The USB11 device controller provides six endpoints in the USB device controller besides the mandatory control endpoint, where among them, four endpoints are for IN transactions and two endpoints are for OUT transactions.

Word, half-word and byte access are all allowed for loading and unloading the FIFO. The controller features 4 DMA channels for data transfer.

| Feature | Description |
|---|---|
| Speed | Full speed (12MHz) |
| Enhanced feature | Generic device |
| Endpoint | 4TX/2RX |
| DMA channel | 4 |
| Embedded RAM | 2816 |

### 2.3.2. MSDC

The MSDC supports

- SD memory card specification 2.0
- SDIO card specification 2.0
- eMMC4.41, no booting and not support DDR mode

There are two ports MSDC which are MSDC0, MSDC1.

Both of them can be used as the host controller of SD/SDIO/eMMC

The details feature list of MSDCx is as follow:

- 32 bit access for control registers
- Built-in CRC circuit
- Support PIO mode, Basic DMA mode, Descriptor DMA mode
- Interrupt capabilities
- Support SD/SDIO speed mode:
  - Default Speed mode (DS)
  - High Speed mode (HS)
- Support eMMC speed mode:
  - Backwards Compatibility with legacy MMC card (DS)
  - High Speed SDR mode (HS)
- Support 1-bit/4-bit SD/SDIO/eMMC bus width. The module is targeted at 52MHz operating clock at 1.1V and 1.3V, and 26MHz at 0.9V. Data rates up to 52Mbps in 1-bit mode, 52 x 4 Mbps in 4-bit mode
- Programmable serial clock rate on SD/SDIO/eMMC bus (256 gears)
- Card detection capabilities (This SOC uses the EINT controller for card detection)
- Do not support SPI mode for SD memory card
- Do not support suspend/resume for SDIO card
- Do not support eMMC boot feature

### 2.3.3. SDIO2.0 slave

MT2625 HIF module provides one SDIO2.0 card interface connected to the host and can support multiple speed modes, which include default speed, high speed. SDIO provides high-speed data I/O with low power consumption for mobile devices. During normal initialization and interrogation by the SDIO host, the SDIO client identifies itself as an SDIO card. The host software obtains the card information in a tuple (linked list) format and determines if the I/O functions of the card are acceptable to activate.

Main feature list:

- Support SDver2.0 spec. Bus speed  support DS or HS mode (all pins are 3.3v)
- SD_CLK up to 52MHZ
- Support 1-bit and 4-bits SD modes
- Suppport CMD52 and CMD53
- Support programmable drive strength
- Support one user function
- Support common interrupt (data[1])
- One set DMAC is built in SDOIO Device Controller

### 2.3.4. Serial peripheral interface (SPI)

MT2625 chipset features two SPI master controller and one SPI slave controller to receive and transmit device data using single, dual and quad SPI protocol. The SPI controllers can communicate at up to 52 Mbps.

The chip select signal and SPI clock of SPI master controllers are configurable. The SPI controllers also support DMA mode for large amount of data transmission.

### 2.3.5. Universal asynchronous receiver transmitter (UART)

MT2625 chipset houses four UART interfaces that provide full duplex serial communication between the baseband chipset and external devices. UART has both M16C450 and M16550A modes of operation compatible with a range of standard software drivers.

UARTs support baud rates from 110bps up to 3Mbps and baud rate auto-detection function. Both UART1 and UART2 provide hardware and software flow control of the RTS/CTS signals.

UARTs can configure data transfer lengths from 5 to 8 bits, with an optional parity bit and one or two stop bits by software. They can be served by the DMA controller.

### 2.3.6. Inter-integrated circuit interface (I2C)

MT2625 chipset provides three I2C master controllers. There are three types of speed modes in the I2C controllers: standard mode (100kbit/s), fast mode (400kbit/s) and high-speed mode (3.4Mbit/s), supporting 7-bit/10-bit addressing and can be served by the DMA controller.

The I2C package size supports up to 1,024 bytes per transfer and 1,024 transfers per transaction in DMA mode and 8 bytes per transfer in non-DMA mode. START, STOP, REPEATED START conditions can be increased to support single or multiple transfer. These features can be configured by software based on customer requirements.

### 2.3.7. Pulse-width modulation (PWM)

There are four PWM controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals can be programmed. The PWM controllers can be configured to use 48MHz, 13MHz or 32kHz clock source to support a wide range of output pulse frequencies.

### 2.3.8. Keypad scanner

MT2625 platform provides a keypad hardware module. The keypad supports two types of keypads: 3 x 3 single keys and 3 x 3 configurable double keys.

The 3 x 3 keypad supports a matrix with 3*3*2 = 18 keys. The 18 keys are divided into 9 subgroups and each group consists of two keys and a 20Ω resistor. The keypad de-bounce time is software configurable.

### 2.3.9. DMA

MT2625 chipset features two DMA controllers, containing 27 channels in power down domain. They manage data transfer between peripheral devices and memory.

There are three types of DMA channels in the DMA controller – full-size DMA channel, half-size DMA channel and virtual FIFO DMA for different peripheral devices. DMA controllers support ring-buffer and double-buffer memory data transactions.

To improve the bus efficiency, the DMA controllers provide an unaligned-word access function. When this function is enabled, it can automatically convert the address format from the unaligned type to aligned type, ensuring compliance with the AHB/APB protocol.

Each peripheral device is connected to a dedicated DMA channel that can configure transfer data sizes, source address and destination address by software. The DMA controllers can be used with the following peripherals:

- Three I2C interfaces
- Two I2S interfaces
- Four UART interfaces
- An USB interface
- An USIM interface

### 2.3.10. Universal subscriber identity module (USIM)

ISO/IEC 7816 is a series of standards specifying integrated circuit cards and the use of such cards for interchange. These cards are identification cards intended for information exchange negotiated between the outside world and the integrated circuit in the card. Because of an information exchange, the card delivers information (computation result, stored data), and/or modifies its content (data storage, event memorization). The USIM is a device which providing transaction between SIM card and chip.

| Feature | Description |
|---|---|
| Speed | SIMCLK can be configured to 4.33MHz/3.25MHz<br>1ETU >= 8 CLKs |
| Enhanced feature | T=0, T=1; DMA with 16 bytes FIFO; Support CLK stop mode |
| Voltage | 1.8V/3.0V |
| Support standard/class | Compliance to ISO/IEC 7816-3 |

## 2.4. Modem system

### 2.4.1. Overview

MT2625 baseband supports 3GPP technical specification release 13 features and key features from release 14, as listed below:

- Release 13 features:
  - PSM
  - eDRX
  - Control Plane EPS CIoT optimization
  - Attach without PDN
  - Multi-tone Uplink
  - NAS Security
  - RoHC (Control Plane)
  - Idle-mode Mobility
  - User Plane EPS CIoT optimization (RRC connection suspension/resumption)

- RoHC (User Plane)
- AS Security
- S1-U data transfer
- RRC connection re-establishment
- RRC connection reconfiguration
- Multi-carrier (non-anchor) operation

- Release 14 features:
  - OTDOA
  - Two HARQ process in UL/DL
  - Support for maximum UL/DL TBS of 2536 bits (Cat-NB2).
  - RRC Re-establishment for CP data (Mobility enhancement)

### 2.4.2. Block diagram

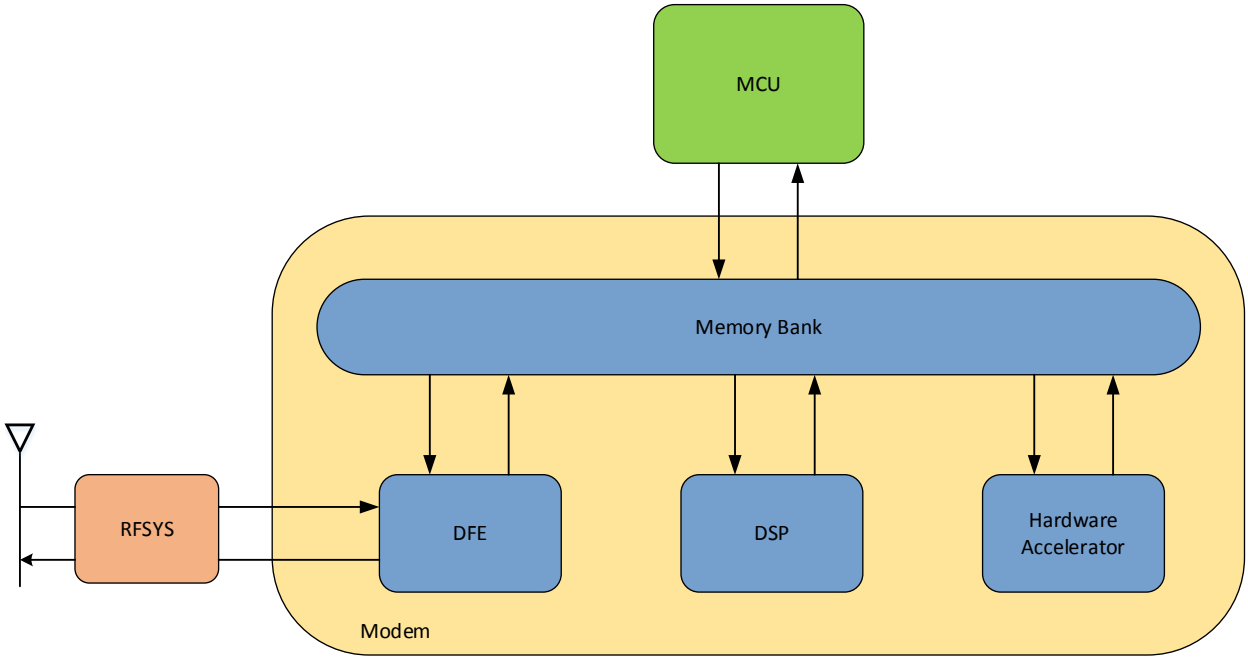



***Figure 2.4-1. Block diagram***

### 2.4.3. Functional block description

The dataflow picture contains parts of the design.

- Memory bank: The memory bank is used for data exchange between MCU, DSP, DFE and hardware accelerators.
- Hardware accelerators: Hardware accelerators contain engines for signal processing.
- Digital front–end (DFE): DFE sends and receives data to/from ADC. It covers a filter chain (CICs/FIR), IRR and interpolators for uplink and downlink.

- Digital Signal Processing (DSP): The DSP is responsible for inner algorithms, including channel estimation and synchronization.

#### 2.4.3.1. Downlink reception

DFE samples the data sent from the ADC. DFE receives data with a source synchronous clock. The DFE will also be the only part of the design that is aware of system time (provided from NB-IoT Timer). The system is data driven after passing through DFE. DFE covers a filter chain (CICs/FIR), IRR and interpolators. The interpolators write data into a time domain buffer through a port opened/closed by software, depending on system conditions.

The DSP is responsible for inner algorithms, including channel estimation and synchronization. The output is the demodulated symbol (LLRs) to decoding engine.

#### 2.4.3.2. Uplink reception

MCU sends data to memory bank. The hardware accelerator is executed offline to prepare the transmitted block and handle the symbol rate processing. Then DFE provides data to the ADC.

## 2.5. Analog baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the data transfer to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete analog baseband signal processing:

1) Auxiliary ADC. Provides an ADC for battery and other auxiliary analog function monitoring.
2) Clock generation. Includes PLLs to provide clock signals to MCU, I2S and USB.
3) XOSC32. A 32kHz crystal oscillator circuit for RTC applications on analog blocks.

### 2.5.1. Auxiliary ADC

#### 2.5.1.1. Block description

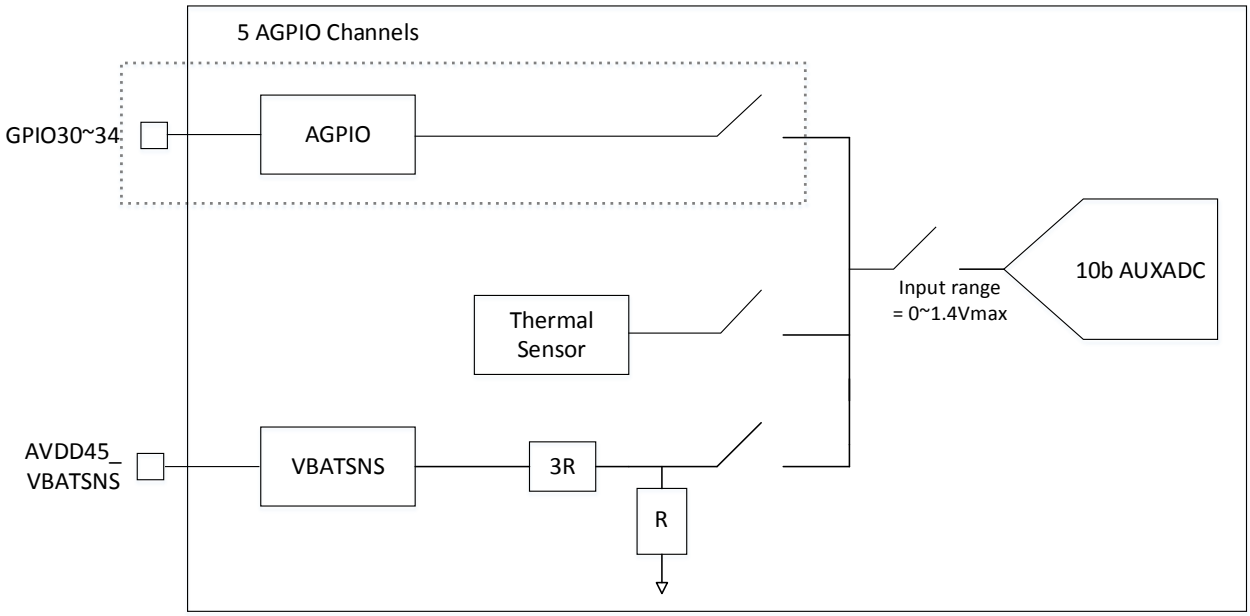



***Figure 2.5-1. Block diagram***

The auxiliary ADC includes the following functional blocks:

1) Analog multiplexer. Selects signal from one of the seven auxiliary input pins. Real-world messages, such as temperature, are monitored and translated to the voltage domain.
2) 10-bit A/D converter: Converts the multiplexed input signal to 10-bit digital data.

***Table 2.5-1. Auxiliary ADC input channels***

| Channel | Application | Input range [V] |
|---|---|---|
| 1~5 | GPIO30~34 | 0V to 1.4V |

| Channel | Application | Input range [V] |
|---|---|---|
| 6 | Thermal Sensor | -40°C to 125°C |
| 7 | VBATSNS | 0V to 5.2V |

#### 2.5.1.2. Functional specifications

The functional specifications of the auxiliary ADC are listed in Table 2.5-2.

***Table 2.5-2. Auxiliary ADC Specifications***

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **N** | Resolution | - | 10 | - | Bit |
| **FC** | Clock rate | - | 3.25 | 4 | MHz |
| **FS** | Sampling rate at N-Bit | - | FC/(N+4) | - | MSPS |
| **VIN** | Input swing | 0 | - | 1.4 | V |
| **CIN** | Input capacitance<br>Unselected channel<br>Selected channel | <br>-<br>- | <br>100<br>4.56 | <br>-<br>- | <br>fF<br>pF |
| **RIN** | Input resistance<br>Unselected channel<br>Selected channel | <br>33<br>- | <br>-<br>- | <br>-<br>1 | <br>MΩ<br>MΩ |
| **RS** | Source Impedance | | | 7 | kΩ |
| | Clock latency | - | N+4 | - | 1/FC |
| **DNL** | Differential nonlinearity | - | ± 1 | - | LSB |
| **INL** | Integral nonlinearity | - | ± 2 | - | LSB |
| **OE** | Offset error | - | ± 10 | - | mV |
| **FSE** | Full swing error | - | ± 10 | - | mV |
| **SINAD** | Signal to noise and distortion ratio (10-kHz full swing input & 3.25-MHz clock rate) | 50 | TBD | - | dB |
| **DVDD** | Digital power supply | 0.81 | 1.1 | 1.43 | V |
| **AVDD** | Analog power supply | 1.62 | 1.8 | 1.98 | V |
| **Temp** | Operating temperature | -40 | - | 85 | °C |
| | Current consumption<br>Power-up<br>Power-down | <br>-<br>- | <br>500<br>1 | <br>-<br>- | <br>µA<br>µA |

Absolute Maximum Ratings:

- The input voltage of AGPIO0~4, i.e. GPIO30 ~ GPIO34, must be under **1.4V**, when GPIO pins are configured as analog IO.

## 2.5.2. Phase locked loop and oscillators

### 2.5.2.1. Block description

There are three phase-locked loops (PLL) in PLLGP: UPLL, MPLL and XPLL.

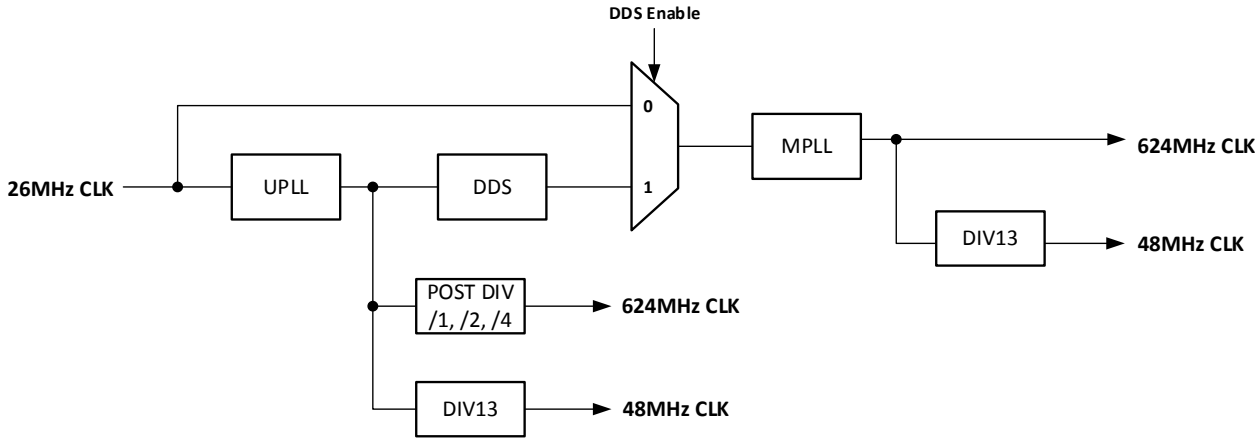



*Figure 2.5-2. Block diagram of UPLL and MPLL clock sources*

Figure 2.5-2 shows the block diagram of the UPLL and MPLL clock sources. The UPLL and MPLL are composed of typical PLL components such as phase-frequency detector, charge pump, low pass filter, voltage-controlled oscillator and frequency dividers.

The UPLL generates 624MHz clock output, and a frequency divider derives the fixed 48MHz clock.

The DDS-based MPLL provides a maximum frequency of 624MHz. With a frequency hopping range from -8% to 0%, it can give a clock output ranging from 574MHz to 624MHz. A divider scales down this frequency to generate a corresponding clock with a maximum frequency of 48MHz.

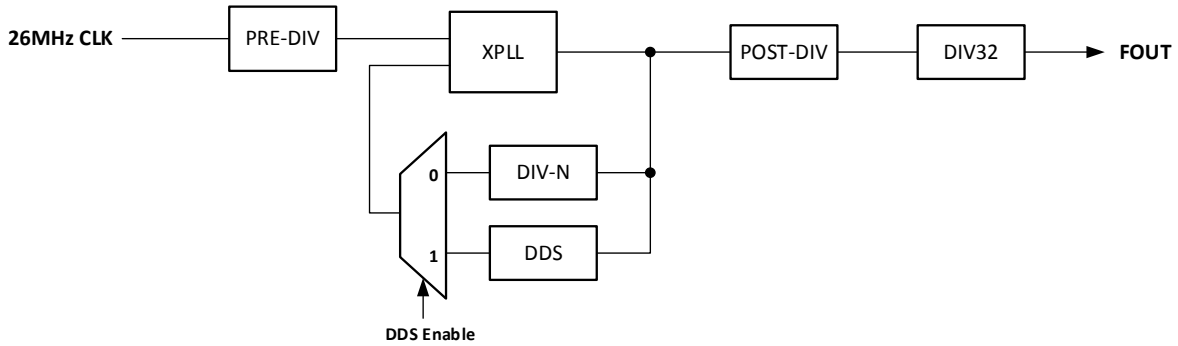



*Figure 2.5-3. Block diagram of XPLL clock sources*

A fractional-N XPLL with an 8-bit integer and 24-bit fractional divisor is programmable to generate clocks ranging from 0.5GHz to 1.5GHz.

Figure 2.5-3 shows the block diagram of the XPLL clock source composed of typical PLL components, such as phase-frequency detector, charge pump, low pass filter, voltage-controlled oscillator and frequency dividers. The feedback divider of PLL is implemented by an 8-bit multi-modulus divider (MMD) which can operate at very high

speed with wide divisor range. The divisor of MMD is controlled by the DDS to implement fractional-N frequency multiplication. The period-controlled word (PCW) of the DDS is a 32-bit binary number with an 8-bit integer part and a 24-bit fractional part. The pre-divider and the post-divider are both simple binary dividers added to facilitate the frequency configuration of the PLL.

These three PLLs do not require off-chip components to operate, and can be turned off to save power. Figure 2.5-2 and Figure 2.5-3show the block diagram of clock sources.

After powering up, the PLLs are all off by default control register setting. The source clock signal for the UPLL/MPLL is selected through multiplexers from 26MHz XTAL. The software maintains the PLL lock time while the clock selection is changing.

For power management, the MCU software configuration may stop MCU Clock by setting up the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode and return the MCU to the running mode.

#### 2.5.2.2. Functional specifications

The functional specifications of PLLs and oscillators are shown in the tables below.

***Table 2.5-3. MPLL specifications***

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Fin** | Input clock frequency | - | 26 | - | MHz |
| **Fout** | Output clock frequency | -<br>- | 624<br>48 | -<br>- | MHz<br>MHz |
| | Settling time | - | 20 | - | us |
| | Output clock duty cycle | 44 | 50 | 56 | % |
| | Output clock jitter (RMS period jitter) | - | 20 | - | ps |
| | Frequency Hopping | -8 | - | 0 | % |
| **DVDD** | Digital power supply | 0.99 | 1.1 | 1.43 | V |
| **AVDD** | Analog power supply | 1.62 | 1.8 | 1.98 | V |
| **T** | Operating temperature | -40 | - | 85 | °C |
| | Current consumption (with DDS) | - | 1.1 | - | mA |
| | Power-down current consumption | - | 0.1 | - | µA |

***Table 2.5-4. UPLL specifications***

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Fin** | Input clock frequency | - | 26 | - | MHz |
| **Fout** | Output clock frequency | -<br>- | 624<br>48 | -<br>- | MHz |
| | Settling time | - | 20 | - | us |
| | Output clock duty cycle | 44 | 50 | 56 | % |
| | Output clock jitter (rms period jitter) | - | 20 | - | ps |
| **DVDD** | Digital power supply | 0.99 | 1.1 | 1.43 | V |
| **AVDD** | Analog power supply | 1.62 | 1.8 | 1.98 | V |
| **T** | Operating temperature | -40 | - | 85 | °C |
| | Current consumption | - | 1.5 | - | mA |

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| | Power-down current consumption | - | 0.1 | - | µA |

***Table 2.5-5. XPLL specifications***

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Fin** | Input clock frequency | - | 26 | - | MHz |
| **Fout** | Output clock frequency | - | 2626 (VCO: 832)<br>24.576 (VCO: 786.432)<br>22.5792 (VCO: 722.5344) | - | MHz |
| | Settling time | - | 50 | - | µs |
| | Output clock duty cycle | 44 | 50 | 56 | % |
| | Output clock jitter (rms period jitter) | - | 20 | - | ps |
| | Frequency Tuning | -1 | - | 0 | % |
| **DVDD** | Digital power supply | 0.99 | 1.1 | 1.43 | V |
| **AVDD** | Analog power supply | 1.62 | 1.8 | 1.98 | V |
| **T** | Operating temperature | -40 | - | 85 | °C |
| | Current consumption | - | 2 | - | mA |
| | Power-down current consumption | - | 0.1 | - | µA |

# 3. RF Subsystem

## 3.1. Radio characteristics

The RF subsystem (RFSYS) is the built-in NB-IoT transceiver in the chip. It downconverts RF signals from antenna switch to RX DFE, and upconverts baseband signal from TX DFE to Power Amplifier. The digitally controlled crystal oscillator (DCXO) is also integrated in RFSYS to generate 26-MHz system clock. It also provides 32kHz clock in non-RTC mode.

### 3.1.1. Features

- Compliant to 3GPP 36.101 release 13 and 14 category NB1/NB2
- Supported bands include EUTRA 1, 2, 3, 5, 8, 12, 13, 17, 18, 19, 20, 25, 26, 28, 66 and 70
- Optional bands are EUTRA 11, 21, 31, and 71
- Low power 1.3-V single-ended Saw-Less Rx and Polar TX
- Built-in low dropout linear regulators are capable to power on by switching regulator.

### 3.1.2. Block diagram

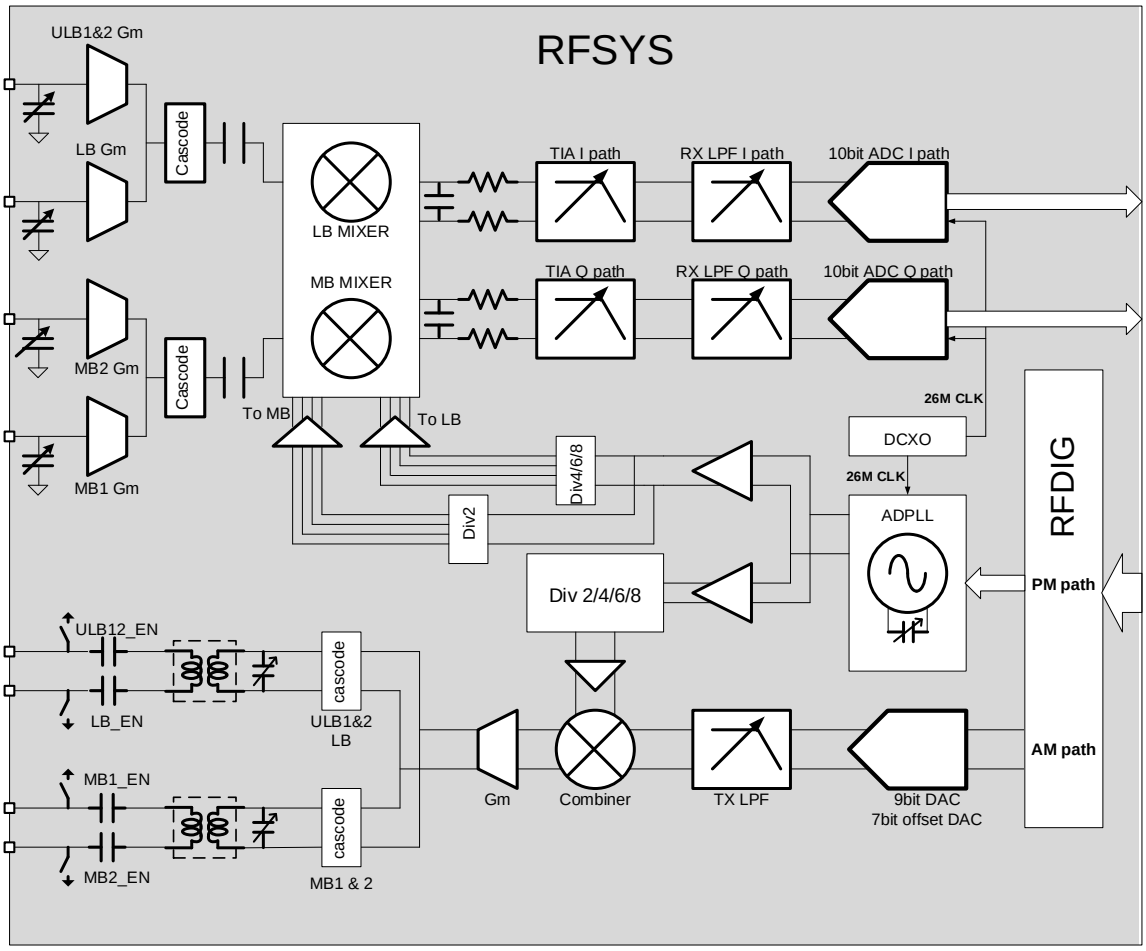



***Figure 3.1-1. RF block diagram***

# 4. Power Management Unit and Low Power Control System

## 4.1. Overview

The power management unit (PMU) controls the power supply of the chip, including the baseband, processor, memory, PA, SIM and more. There are two power input source for MT2625:

- For RTC timer control and PMU control (AVDD33_LDO, AVDD33_CORE, and AVDD33_VRF):

It's operated by wider input voltage range (2.1V to 3.63V), to support real time clock control and alarm logic, and to provide AP low power system control. The PMU contains Under-Voltage Lockout (UVLO) circuit, several low drop-out regulators (LDOs), efficiency buck converters and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection and low output noise.

- For PA and SIM control (AVDD33_VPA, AVDD33_VSIM):

A single regulated 3.3V power supply is required for the MT2625. It could be from external DC-DC converter to convert higher voltage supply to 3.3V or boost from a lower voltage supply to 3.3V. The low drop-out voltage output LDOs support 1.8V and 2.9V two types of SIM applications. The efficiency PA buck converters with efficient line/load regulation, high ripple rejection support wider range (0.5 to 2.8V) of power amplifiers.

Due to ultra-low input voltage and low current consumption, the battery lifetime is enhanced by using portable batteries.

## 4.2. Low-power operating mode

The MT2625 power state diagram is illustrated in Figure 4.2-1. In **ACTIVE** mode, the frequency of Cortex®-M4 can be configured as 104 MHz or 26 MHz. When the system is in the idle condition, it can enter **IDLE** or **LIGHTSLEEP** mode. In **IDLE** mode, the PMU keeps current voltage and all Cortex®-M4 and peripherals are in the idle state, which can be returned to **ACTIVE** state by any interrupt event. But if the system goes to **LIGHTSLEEP** mode, the PMU can be changed to the low power mode to further lower the current consumption with 32K clock only. The **DEEPSLEEP** mode provides a lower current consumption than **LIGHTSLEEP** mode with the ability for 8K SRAM retention. It is suitable for the applications which could be idle in a long period but also need to keep data in SRAM. It is controlled by SW to enter the **DEEPSLEEP** mode and exited by RTC or PWRKEY event. The **OFF** mode is similar with **DEEPSLEEP** mode but no data keep in SRAM. This mode is used when device is under **Power Save Mode** (**PSM**). In **SHIPPING** mode, there are only some logics to detect the power on condition and lowest power consumption in this mode.

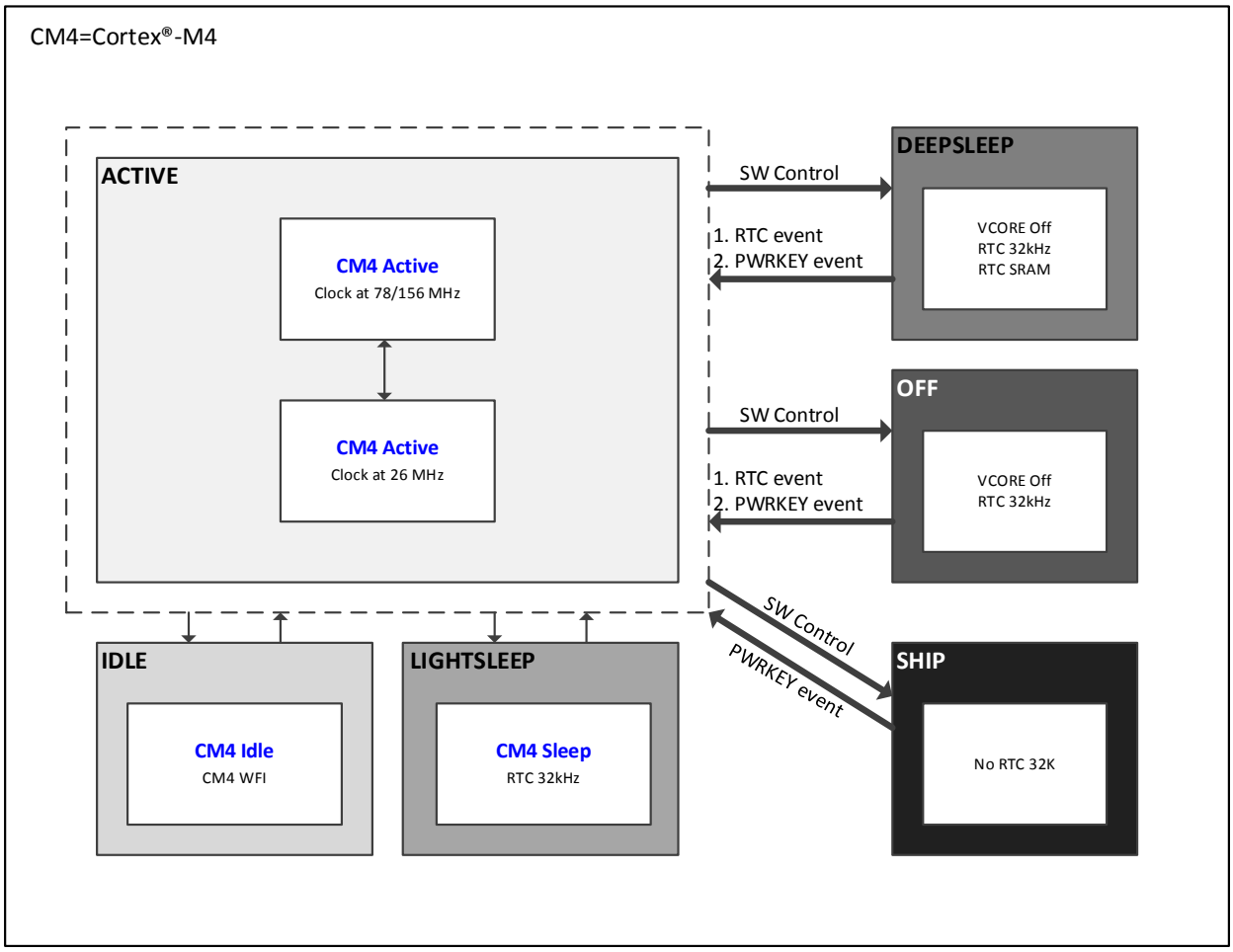



***Figure 4.2-1. MT2625 power states***

## 4.3. Power performance summary

Table 4.3-1 list the current consumption of some basic scenarios at battery domain. Note that the current measurement condition is under the typical condition of process, voltage, and temperature.

***Table 4.3-1. Current consumption in different power modes***

| Operation Mode | | Test Conditions[1] | Current Consumptions [2] | Unit |
|---|---|---|---|---|
| Power Mode | Scenario | | | |
| SHIP | SHIP | • Shipping mode | < 0.3 | uA |
| OFF | OFF | • RTC Timer<br>• XTAL 32kHz | 2.6 | uA |
| DEEPSLEEP | DEEPSLEEP | • RTC Timer<br>• 8KB SRAM data retention | 3.4 | uA |

[1] No SYSRAM data is retained in these scenarios.

[2] Conditions: battery voltage@3.3V, DVDD_IO_0/1/2@3.3V, 25°C, Typical corner IC, XTAL@26Mhz.

| Operation Mode | | Test Conditions[1] | Current Consumptions[2] | Unit |
|---|---|---|---|---|
| Power Mode | Scenario | | | |
| | | • XTAL 32kHz | | |
| LIGHTSLEEP | LIGHTSLEEP | • Cortex®-M4 in sleep state<br>• TCM 96KByte SRAM is retained<br>• XTAL 32kHz | 50uA[3] | uA |
| ACTIVE[4] | RX | • RX | 15 | mA |
| | TX | • MB Band1<br>• TX 23dBm | 291 | mA |
| | | • MB Band1<br>• TX 10dBm | 64 | mA |
| | | • MB Band1<br>• TX 0dBm | 31 | mA |
| | | • LB Band8<br>• TX 23dBm | 333 | mA |
| | | • LB Band8<br>• TX 10dBm | 60 | mA |
| | | • LB Band8<br>• TX 0dBm | 34 | mA |

## 4.4. PMU architecture for low power system

The 3.3V power source is directly supplied to the switching regulator, digital IOs and RF-related circuit. It is converted from 3.3V by the PMU for low voltage circuits. The built-in CORE and RF buck convert to 1.1V and 1.3V for digital core, RF circuits. The four LDOs are VIO18, VSIM, VSRAM_RTC and VFEM. VCORE buck converter and VSRAM stands for digital core 1.3V to 0.7V low power mode control. VRF, VPA buck converter and VFEM stands for RF, PA and front-end module control, and VIO18 stands for IOs, PLL, and internal/external memory LDO.

In **ACTIVE/ IDLE** mode, the buck converter converts 1.1V output in MT2625. It can operate in PFM mode for optimize the power consumption. With an external on-board LC filter (2.2uH inductor and 10uF cap), it outputs a low ripple 1.1V to core system. In **ACTIVE/ IDLE** mode, VIO18 outputs 1.8V for whole chip digital IOs, memory, PLL used.

In **LIGHTSLEEP** mode back to **ACTIVE** mode, VCORE buck output voltage will converts to 1.1V from 0.7V to core system by DVFS (Dynamic Voltage Frequency Scale) control. While MT2625 is in **LIGHTSLEEP** mode, VSRAM will reduce its output level from 1.1V to 0.775V for internal retention SRAM power. VIO18 keeps outputs 1.8V for whole chip digital IOs, memory, PLL used.

In **DEEPSLEEP** mode (Deep Sleep Mode), VCORE, VRF, VPA, VFEM and VIO18 will be shut down. During this mode, only some PMU logics, RTC timer controller and retention LDO VSRAM_RTC are alive 0.775V to keep lower current

[3] The current includes SIM card current 25uA.

[4] The current includes PA SKY68018-11.

consumption. During this mode, only some PMU logics, RTC timer controller and retention SRAM are alive to keep lower current consumption.

In **OFF** mode, it's similar with **DEEPSLEEP** mode but turn off the VSRAM_RTC regulator and SRAM application.

In **SHIPPING** mode, all regulator and VSRAM_RTC will be shut down to efficiently enhance the battery life.

The MT2625 PMU power grid is illustrated in Figure 4.4-1.

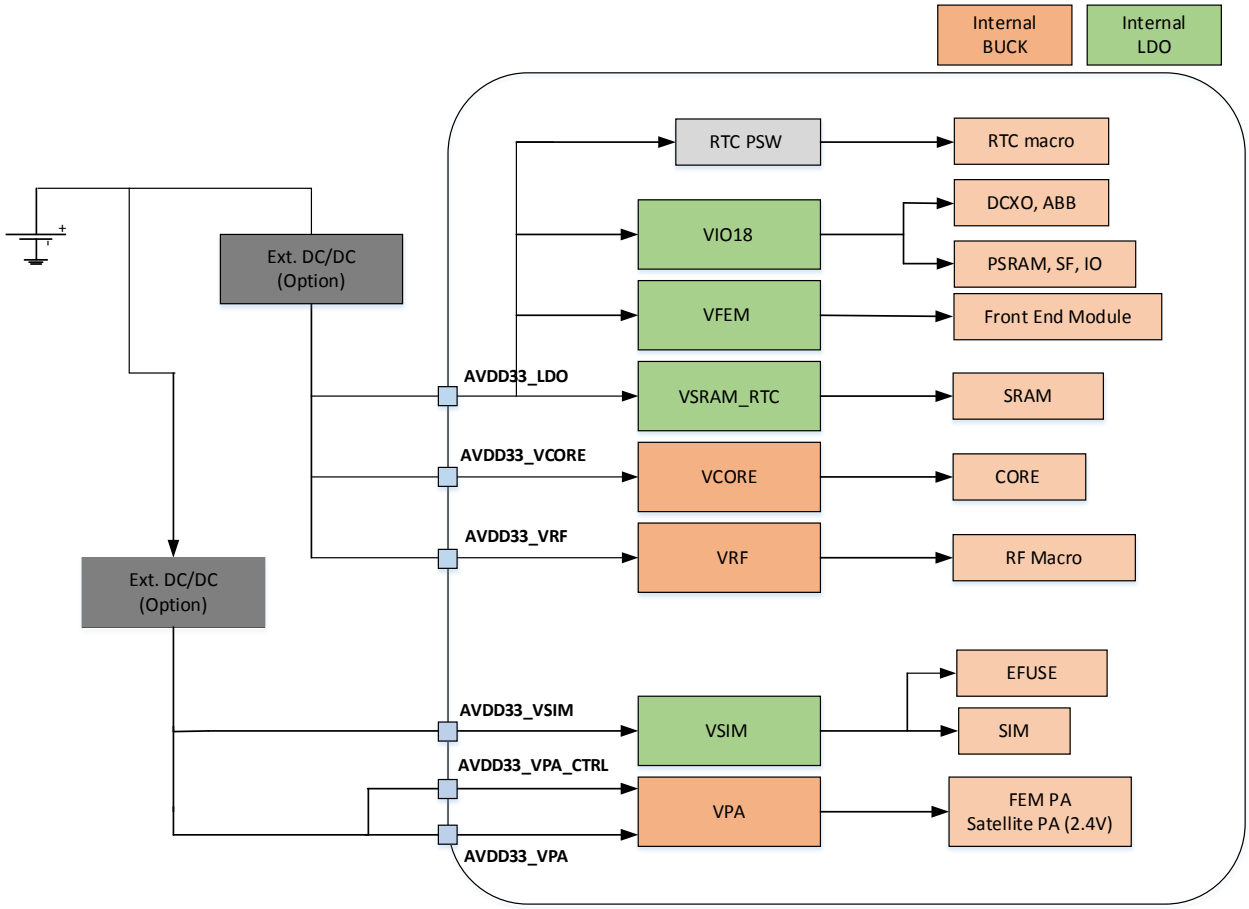



***Figure 4.4-1. MT2625 PMU power grid***

Table 4.4-1 lists the internal BUCK/ LDO output range, default voltage setting and the output current capabilities.

***Table 4.4-1. BUCK / LDO characteristic***

| Regulator Type | Name | Output Voltage Range(V) | Default ON Voltage(V) | IOUT (mA) |
|---|---|---|---|---|
| **BUCK** | VCORE | 0.7 ~ 1.3 | 1.2 | 150 |
| | VRF | 1.3 | Default off | 35 |
| | VPA | 0.5 ~ 2.8 | Default off | 500 |
| **LDO** | VIO18 | 1.8 | 1.8 | 180 |
| | VFEM | 1.8 | Default off | 35 |

| Regulator Type | Name | Output Voltage Range(V) | Default ON Voltage(V) | IOUT (mA) |
|---|---|---|---|---|
| | VSRAM_RTC | 0.775 / 1.1 | Default off | 5 |
| | VSIM | 1.8 / 2.8 / 2.9 | Default off | 60 / 100/ 60 |

## 4.5. PMU functional description

### 4.5.1. UVLO

#### 4.5.1.1. Under-voltage lockout (UVLO)

The UVLO state in PMU prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by AVDD33_LDO. It ensures that the device is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator that ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMU will be turned off by itself, except for RTC macro and PMU always on domain, it will draw low quiescent current. In order to optimize the low power performance, there is no UVLO in DEEPSLEEP and LIGHTSLEEP mode.

| Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|
| Under voltage falling threshold | 1.80 | 1.85 | 1.90 | V |
| Under voltage rising threshold (UVLO_VTH) | 2.05 | 2.10 | 2.15 | V |

### 4.5.2. PWRKEY

Pulling PWRKEY low is a typical method to turn on the device. The system reset ends when all default-on regulators are sequentially turned on. After that, the SOC will send the power ready signal back to PMU for acknowledgement. To successfully power on the device, PWRKEY should be kept low until PMU receives power ready from the AP.

| Parameter | Conditions | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| **PWRKEY** | | | | | |
| High voltage | | 0.7*AVDD33_LDO | | | V |
| Low voltage | | | | 0.3* AVDD33_LDO | V |
| De-bounce time | OFF/DEEPSLEEP to ACTIVE | 16 | 32 | 48 | msec |
| | SHIPPING to ACTIVE | 1 | 2 | 3 | sec |

### 4.5.3. Long press shutdown

Long press shutdown is default feature to provide a reliable hardware reset to force shutdown PMU without removing the battery, which detects negative pulse width on PWRKEY.

#### 4.5.3.1. Long-press shutdown timer:

When negative pulse width is greater than the timer setting, the PMU will force shutdown to OFF mode.

There are four types of Long-press shutdown key-pressed timing select timer options:

- 5s
- 8s **(DEFAULT)**
- 11s
- 25s

Note: The timing variation is +/-50% for this feature.

#### 4.5.3.2. Long-press shutdown function type:

For default setting, after long press shutdown, if PWRKEY not released, enters re-power on by sequence and long-press shutdown periodically.

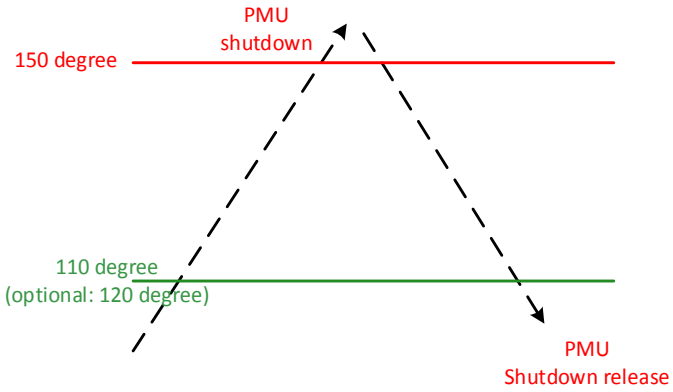
There are three options for PWRKEY Long Press Function for users:

- Disabled. No long press shutdown function.
- Enabled. The power on sequence will start after the PWRKEY is released and then pressed again.
- Enabled. The power on sequence will start after the PWRKEY de-bounce time, if PWRKEY is kept low. **(DEFAULT)**

### 4.5.4. Thermal shutdown

This is the hardware thermal protection function and PMU will shut down immediately when the function is triggered.

If the chip reaches 150°C (±15°C), the PMU enters OFF mode by immediate power-off sequence. It will auto recover by power-on sequence, if the chip temperature is cooled down below 110 °C. (Register option for 120 °C recovery).




### 4.5.5. Shipping mode

User can enter SHIPPING mode by setting register, and PMU will power-off. When in SHIPPPING mode, please note that if PWRKEY is pressed over 2 seconds, the PMU will re-power-on to normal mode by normal power-on sequence.

### 4.5.6. SYSRSTB cold-reset application

SYSRSTB is used to reset the PMU when system hangs. This function is default ON by hardware.

Cold reset function can be triggered by pressing SYSRSTB for over 32ms de-bounce time. When cold reset is triggered, the system is shut down immediately with immediate-off sequence. The shutdown time is 20ms to make sure analog circuits discharge completely. Then the PMU will do the normal power on. Note that the cold reset cannot be triggered in SHIPPING mode.

# 5. Pin Description

## 5.1. MT2625D series ball diagram

For MT2625D series, a TFBGA 5.6mm*5.6mm, 121-ball, 0.5mm pitch package is offered. Pin-outs and the top view for this package are shown in Figure 5.1-1.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GPIO12 | GPIO10 | GPIO9 | GPIO6 | GPIO7 | GPIO0 | RESETB_OUT | TXO_MB1 | TXO_LB | LNA_LB | AVSS_RF | A |
| B | GPIO14 | GND | GPIO11 | GND | GPIO2 | GPIO1 | FSOURCE_P | TXO_MB2 | TXO_ULB | LNA_OPIS | LNA_ULB | B |
| C | DVDD_IO_0 | GPIO17 | GPIO15 | GPIO16 | DVDD_IO_2 | GPIO4 | GPIO3 | AVSS_RF | AVSS_RF | LNA_MB2 | LNA_MB1 | C |
| D | GPIO23 | GPIO22 | GPIO19 | GPIO18 | GPIO13 | GPIO5 | GPIO8 | BPI0 | AVSS_RF | EXT_CLK_SEL | AVDD_RF | D |
| E | VDDK | GND | GPIO25 | GPIO20 | GND | GND | GND | BPI2 | AVDD18_RF | XTAL2 | XTAL1 | E |
| F | DVDD18_MLDO | GPIO27 | GPIO29 | GPIO24 | GPIO21 | GND | GND | BPI1 | BPI4 | AVSS_DCXO | AVSS_DCXO | F |
| G | LX_VRF | PMU_TESTMODE | GPIO28 | GPIO26 | GND | GND | GND | GPIO36 | SRCLKENAI | BPI3 | FREF | G |
| H | AVDD33_VRF | AVSS33_VRF | FB_VRF | FB_VPA | AVSS33_LDO | GPIO32 | GPIO34 | GPIO33 | VDDK | MIPI_SCLK | MIPI_SDATA | H |
| J | LX_VPA | AVSS33_VPA | PMU_SYSRSTB | FB_VCORE | VSRAM_RTC | RTC_EINT | RTC_GPIO0 | GND | GPIO31 | GPIO35 | DVDD_IO_1 | J |
| K | AVDD33_VPA | AVSS33_VCORE | AVDD33_VPA_CTRL | AVDD45_VBATSNS | PMU_PWRKEY | VFEM | XIN | GPIO30 | USB11_DM | SIM0_SIO | SIM0_SRST | K |
| L | LX_VCORE | AVDD33_VCORE | AVDD33_LDO | VIO18 | GND_VREF | AVDD33_VSIM | XOUT | AVDD33_VUSB | USB11_DP | VSIM | SIM0_SCLK | L |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |

***Figure 5.1-1. MT2625D series ball diagram and top view***

### 5.1.1. MT2625D series pin coordination

***Table 5.1-1. MT2625D series pin coordinates***

| Pin# | NETNAME | Pin# | NETNAME | Pin# | NETNAME |
|---|---|---|---|---|---|
| A1 | GPIO12 | H4 | FB_VPA | D8 | BPI0 |
| B1 | GPIO14 | J4 | FB_VCORE | E8 | BPI2 |
| C1 | DVDD_IO_0 | K4 | AVDD45_VBATSNS | F8 | BPI1 |
| D1 | GPIO23 | L4 | VIO18 | G8 | GPIO36 |
| E1 | VDDK | A5 | GPIO7 | H8 | GPIO33 |

| Pin# | NETNAME | Pin# | NETNAME | Pin# | NETNAME |
|---|---|---|---|---|---|
| F1 | DVDD18_MLDO | B5 | GPIO2 | J8 | GND |
| G1 | LX_VRF | C5 | DVDD_IO_2 | K8 | GPIO30 |
| H1 | AVDD33_VRF | D5 | GPIO13 | L8 | AVDD33_VUSB |
| J1 | LX_VPA | E5 | GND | A9 | TXO_LB |
| K1 | AVDD33_VPA | F5 | GPIO21 | B9 | TXO_ULB |
| L1 | LX_VCORE | G5 | GND | C9 | AVSS_RF |
| A2 | GPIO10 | H5 | AVSS33_LDO | D9 | AVSS_RF |
| B2 | GND | J5 | VSRAM_RTC | E9 | AVDD18_RF |
| C2 | GPIO17 | K5 | PMU_PWRKEY | F9 | BPI4 |
| D2 | GPIO22 | L5 | GND_VREF | G9 | SRCLKENAI |
| E2 | GND | A6 | GPIO0 | H9 | VDDK |
| F2 | GPIO27 | B6 | GPIO1 | J9 | GPIO31 |
| G2 | PMU_TESTMODE | C6 | GPIO4 | K9 | USB11_DM |
| H2 | AVSS33_VRF | D6 | GPIO5 | L9 | USB11_DP |
| J2 | AVSS33_VPA | E6 | GND | A10 | LNA_LB |
| K2 | AVSS33_VCORE | F6 | GND | B10 | LNA_OPIS |
| L2 | AVDD33_VCORE | G6 | GND | C10 | LNA_MB2 |
| A3 | GPIO9 | H6 | GPIO32 | D10 | EXT_CLK_SEL |
| B3 | GPIO11 | J6 | RTC_EINT | E10 | XTAL2 |
| C3 | GPIO15 | K6 | VFEM | F10 | AVSS_DCXO |
| D3 | GPIO19 | L6 | AVDD33_VSIM | G10 | BPI3 |
| E3 | GPIO25 | A7 | RESETB_OUT | H10 | MIPI_SCLK |
| F3 | GPIO29 | B7 | FSOURCE_P | J10 | GPIO35 |
| G3 | GPIO28 | C7 | GPIO3 | K10 | SIM0_SIO |
| H3 | FB_VRF | D7 | GPIO8 | L10 | VSIM |
| J3 | PMU_SYSRSTB | E7 | GND | A11 | AVSS_RF |
| K3 | AVDD33_VPA_CTRL | F7 | GND | B11 | LNA_ULB |
| L3 | AVDD33_LDO | G7 | GND | C11 | LNA_MB1 |
| A4 | GPIO6 | H7 | GPIO34 | D11 | AVDD_RF |
| B4 | GND | J7 | RTC_GPIO0 | E11 | XTAL1 |
| C4 | GPIO16 | K7 | XIN | F11 | AVSS_DCXO |
| D4 | GPIO18 | L7 | XOUT | G11 | FREF |
| E4 | GPIO20 | A8 | TXO_MB1 | H11 | MIPI_SDATA |
| F4 | GPIO24 | B8 | TXO_MB2 | J11 | DVDD_IO_1 |
| G4 | GPIO26 | C8 | AVSS_RF | K11 | SIM0_SRST |
| | | | | L11 | SIM0_SCLK |

## 5.2. MT2625A series ball diagram

For MT2625A series, a TFBGA 5.6mm*5.6mm, 121-ball, 0.5mm pitch package is offered. Pin-outs and the top view for this package are shown in Figure 5.1-1.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GPIO12 | GPIO10 | GPIO9 | GPIO6 | GPIO7 | GPIO0 | RESETB_OUT | TXO_MB1 | TXO_LB | LNA_LB | AVSS_RF | A |
| B | GPIO14 | GND | GPIO11 | GND | GPIO2 | GPIO1 | FSOURCE_P | TXO_MB2 | TXO_ULB | LNA_OPIS | LNA_ULB | B |
| C | DVDD_IO_0 | GPIO17 | GPIO15 | GPIO16 | DVDD_IO_2 | GPIO4 | GPIO3 | AVSS_RF | AVSS_RF | LNA_MB2 | LNA_MB1 | C |
| D | GPIO23 | GPIO22 | GPIO19 | GPIO18 | GPIO13 | GPIO5 | GPIO8 | BPI0 | AVSS_RF | EXT_CLK_SEL | AVDD_RF | D |
| E | VDDK | GND | SFSHOLD | GPIO20 | GND | GND | GND | BPI2 | AVDD18_RF | XTAL2 | XTAL1 | E |
| F | DVDD18_MLDO | SFSCK | SFSOUT | SFSCS0 | GPIO21 | GND | GND | BPI1 | BPI4 | AVSS_DCXO | AVSS_DCXO | F |
| G | LX_VRF | PMU_TESTMODE | SFSWP | SFSIN | GND | GND | GND | GPIO36 | SRCLKENAI | BPI3 | FREF | G |
| H | AVDD33_VRF | AVSS33_VRF | FB_VRF | FB_VPA | AVSS33_LDO | GPIO32 | GPIO34 | GPIO33 | VDDK | MIPI_SCLK | MIPI_SDATA | H |
| J | LX_VPA | AVSS33_VPA | PMU_SYSRSTB | FB_VCORE | VSRAM_RTC | RTC_EINT | RTC_GPIO0 | GND | GPIO31 | GPIO35 | DVDD_IO_1 | J |
| K | AVDD33_VPA | AVSS33_VCORE | AVDD33_VPA_CTRL | AVDD45_VBATSNS | PMU_PWRKEY | VFEM | XIN | GPIO30 | USB11_DM | SIM0_SIO | SIM0_SRST | K |
| L | LX_VCORE | AVDD33_VCORE | AVDD33_LDO | VIO18 | GND_VREF | AVDD33_VSIM | XOUT | AVDD33_VUSB | USB11_DP | VSIM | SIM0_SCLK | L |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |

***Figure 5.2-1. MT2625A series ball diagram and top view***

### 5.2.1. MT2625A series pin coordination

***Table 5.2-1. MT2625A series pin coordinates***

| Pin# | NETNAME | Pin# | NETNAME | Pin# | NETNAME |
|---|---|---|---|---|---|
| A1 | GPIO12 | H4 | FB_VPA | D8 | BPI0 |
| B1 | GPIO14 | J4 | FB_VCORE | E8 | BPI2 |
| C1 | DVDD_IO_0 | K4 | AVDD45_VBATSNS | F8 | BPI1 |
| D1 | GPIO23 | L4 | VIO18 | G8 | GPIO36 |
| E1 | VDDK | A5 | GPIO7 | H8 | GPIO33 |
| F1 | DVDD18_MLDO | B5 | GPIO2 | J8 | GND |

| Pin# | NETNAME | Pin# | NETNAME | Pin# | NETNAME |
|---|---|---|---|---|---|
| G1 | LX_VRF | C5 | DVDD_IO_2 | K8 | GPIO30 |
| H1 | AVDD33_VRF | D5 | GPIO13 | L8 | AVDD33_VUSB |
| J1 | LX_VPA | E5 | GND | A9 | TXO_LB |
| K1 | AVDD33_VPA | F5 | GPIO21 | B9 | TXO_ULB |
| L1 | LX_VCORE | G5 | GND | C9 | AVSS_RF |
| A2 | GPIO10 | H5 | AVSS33_LDO | D9 | AVSS_RF |
| B2 | GND | J5 | VSRAM_RTC | E9 | AVDD18_RF |
| C2 | GPIO17 | K5 | PMU_PWRKEY | F9 | BPI4 |
| D2 | GPIO22 | L5 | GND_VREF | G9 | SRCLKENAI |
| E2 | GND | A6 | GPIO0 | H9 | VDDK |
| F2 | SFSCK | B6 | GPIO1 | J9 | GPIO31 |
| G2 | PMU_TESTMODE | C6 | GPIO4 | K9 | USB11_DM |
| H2 | AVSS33_VRF | D6 | GPIO5 | L9 | USB11_DP |
| J2 | AVSS33_VPA | E6 | GND | A10 | LNA_LB |
| K2 | AVSS33_VCORE | F6 | GND | B10 | LNA_OPIS |
| L2 | AVDD33_VCORE | G6 | GND | C10 | LNA_MB2 |
| A3 | GPIO9 | H6 | GPIO32 | D10 | EXT_CLK_SEL |
| B3 | GPIO11 | J6 | RTC_EINT | E10 | XTAL2 |
| C3 | GPIO15 | K6 | VFEM | F10 | AVSS_DCXO |
| D3 | GPIO19 | L6 | AVDD33_VSIM | G10 | BPI3 |
| E3 | SFSHOLD | A7 | RESETB_OUT | H10 | MIPI_SCLK |
| F3 | SFSOUT | B7 | FSOURCE_P | J10 | GPIO35 |
| G3 | SFSWP | C7 | GPIO3 | K10 | SIM0_SIO |
| H3 | FB_VRF | D7 | GPIO8 | L10 | VSIM |
| J3 | PMU_SYSRSTB | E7 | GND | A11 | AVSS_RF |
| K3 | AVDD33_VPA_CTRL | F7 | GND | B11 | LNA_ULB |
| L3 | AVDD33_LDO | G7 | GND | C11 | LNA_MB1 |
| A4 | GPIO6 | H7 | GPIO34 | D11 | AVDD_RF |
| B4 | GND | J7 | RTC_GPIO0 | E11 | XTAL1 |
| C4 | GPIO16 | K7 | XIN | F11 | AVSS_DCXO |
| D4 | GPIO18 | L7 | XOUT | G11 | FREF |
| E4 | GPIO20 | A8 | TXO_MB1 | H11 | MIPI_SDATA |
| F4 | SFSCS0 | B8 | TXO_MB2 | J11 | DVDD_IO_1 |
| G4 | SFSIN | C8 | AVSS_RF | K11 | SIM0_SRST |
| | | | | L11 | SIM0_SCLK |

## 5.3. Pin differences between MT2625D series and MT2625A series

| Pin# | MT2625D series | MT2625A series |
|---|---|---|
| F2 | GPIO27 | SFSCK |
| E3 | GPIO25 | SFSHOLD |
| F3 | GPIO29 | SFSOUT |
| G3 | GPIO28 | SFSWP |
| F4 | GPIO24 | SFSCS0 |
| G4 | GPIO26 | SFSIN |

## 5.4. MT2625 family pin functions

***Table 5.4-1. Acronym for pin types and I/O structure***

| Name | Abbreviation | Description |
|---|---|---|
| Pin Type | AI | Analog input |
| | AO | Analog output |
| | AIO | Analog bi-direction |
| | DI | Digital input |
| | DO | Digital output |
| | DIO | Digital bi-direction |
| | P | Power |
| | G | Ground |
| IO Structure | TYPE0 | Pull-up/down<br>3.63V tolerance |
| | TYPE1 | Pull-up/down<br>5V tolerance |
| | TYPE2 | Pull-up/down<br>5V tolerance<br>SDIO characteristic support |
| | TYPE3 | Pull-up/down<br>5V tolerance<br>Analog input/output |
| | TYPE4 | Pull-up/down<br>5V tolerance<br>Keypad 2K |
| | TYPE5 | Pull-up/down<br>5V tolerance<br>Keypad 200K |
| | TYPE6 | Pull-up/down<br>3.63V tolerance<br>SIM card input/output |

| Name | Abbreviation | Description |
|---|---|---|
| | TYPE7 | Pull-up/down<br>1.98V tolerance<br>SF controller |

*Table 5.4-2. MT2625D series pin function description and power domain (group1)*

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| **System** | | | | | | |
| A7 | RESETB_OUT | DO | TYPE1 | System reset output | - | DVDD_IO_2 |
| G9 | SRCLKENAI | DI | TYPE1 | 26MHz clock request by external devices | - | DVDD_IO_1 |
| **RTC** | | | | | | |
| L7 | XOUT | AIO | - | Input pin for 32k crystal | - | AVDD33_LDO |
| K7 | XIN | AIO | - | Input pin for 32k crystal | - | AVDD33_LDO |
| J6 | RTC_EINT | DIO | Type0 | Dedicate EINT input in RTC | - | AVDD33_LDO |
| J7 | RTC_GPIO0 | DIO | Type0 | PA buck control in RTC | - | AVDD33_LDO |
| **Cellular Radio Interface** | | | | | | |
| A10 | LNA_LB | AI | - | RF input for LB | - | AVDD_RF |
| C10 | LNA_MB2 | AI | - | RF input for MB2 | - | AVDD_RF |
| B11 | LNA_ULB | AI | - | RF input for ULB | - | AVDD_RF |
| C11 | LNA_MB1 | AI | - | RF input for MB1 | - | AVDD_RF |
| B10 | LNA_OPIS | AI | - | External inductor for buck desense | - | AVDD_RF |
| A9 | TXO_LB | AO | - | RF output for LB | - | AVDD_RF |
| B8 | TXO_MB2 | AO | - | RF output for MB2 | - | AVDD_RF |
| B9 | TXO_ULB | AO | - | RF output for ULB | - | AVDD_RF |
| A8 | TXO_MB1 | AO | - | RF output for MB1 | - | AVDD_RF |
| D11 | AVDD_RF | P | - | RF supply 1.2V | - | - |
| E9 | AVDD18_RF | P | - | RF supply 1.8V | - | - |
| E11 | XTAL1 | AI | - | Crystal(external clock input) | - | AVDD18_RF |
| E10 | XTAL2 | AI | - | Crystal | - | AVDD18_RF |
| G11 | FREF | AO | - | External clock buffer output | - | AVDD18_RF |
| D10 | EXT_CLK_SEL | AI | - | 26MHz clock source selection<br>0: On-chip DCXO<br>1: External clock feed in XTAL1 | - | AVDD18_RF |
| F10/F11 | AVSS_DCXO | G | - | DCXO GND | - | - |
| A11/C8/C9/ D9 | AVSS_RF | G | - | RF GND | - | - |

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| **PMU** | | | | | | |
| H1 | AVDD33_VRF | P | - | Input power for BUCK of VRF | - | - |
| H2 | AVSS33_VRF | G | - | GND for BUCK of VRF | - | - |
| G1 | LX_VRF | AO | - | SW node of BUCK of VRF | - | - |
| H3 | FB_VRF | AI | - | Feedback of BUCK of VRF | - | - |
| L2 | AVDD33_VCORE | P | - | Input power for BUCK of VCORE | - | - |
| K2 | AVSS33_VCORE | G | - | GND for BUCK of VCORE | - | - |
| L1 | LX_VCORE | AO | - | SW node of BUCK of VCORE | - | - |
| J4 | FB_VCORE | AI | - | Feedback of BUCK of VCORE | - | - |
| K1 | AVDD33_VPA | P | - | Input power for BUCK of VPA | - | - |
| J2 | AVSS33_VPA | G | - | GND for BUCK of VPA | - | - |
| J1 | LX_VPA | AO | - | SW node of BUCK of VPA | - | - |
| H4 | FB_VPA | AI | - | Feedback of BUCK of VPA | - | - |
| L3 | AVDD33_LDO | P | - | Power for internal controller and LDO | - | - |
| H5 | AVSS33_LDO | G | - | GND for internal controller and LDO | - | - |
| L4 | VIO18 | P | - | Output of LDO of VIO18 | - | - |
| J5 | VSRAM_RTC | P | - | Output of LDO of VSRAM | - | - |
| K6 | VFEM | P | - | Output of LDO of VFEM | - | - |
| L5 | GND_VREF | G | - | GND for reference voltage | - | - |
| K5 | PMU_PWRKEY | AI | - | Power Key | - | AVDD33_LDO |
| G2 | PMU_TESTMODE | AI | - | Reserved for test mode. Tied to GND in normal mode | - | AVDD33_LDO |
| J3 | PMU_SYSRSTB | AI | - | System RSTB pin | - | AVDD33_LDO |
| K4 | AVDD45_VBATSNS | P | - | Battery sensing input | - | - |
| K3 | AVDD33_VPA_CTRL | P | - | Power of VPA controller | - | - |
| L6 | AVDD33_VSIM | P | - | Power of LDO of VSIM | - | - |
| **Digital Power Supply** | | | | | | |
| B7 | FSOURCE_P | P | - | eFuse power source | - | - |
| C1 | DVDD_IO_0 | P | - | Power input of GPIO group 0 | - | - |
| J11 | DVDD_IO_1 | P | - | Power input of GPIO group 1 | - | - |
| C5 | DVDD_IO_2 | P | - | Power input of GPIO group 2 | - | - |

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| E1 | VDDK | P | - | Core power | - | - |
| H9 | VDDK | P | - | Core power | - | - |
| F1 | DVDD18_MLDO | P | - | Power input of SF/EMI group | - | - |
| B2/B4/E2/E5/E6/E7/F6/F7/G5/G6/G7/J8 | GND | G | - | Digital ground | - | - |
| **USB 1.1** | | | | | | |
| K9 | USB11_DM | AIO | - | USB signal DM | - | AVDD33_VUSB |
| L8 | AVDD33_VUSB | P | - | USB supply 3.3V | - | AVDD33_VUSB |
| L9 | USB11_DP | AIO | - | USB signal DP | - | AVDD33_VUSB |
| **SIM** | | | | | | |
| L10 | VSIM | P | - | SIM card power | - | - |
| K10 | SIM0_SIO | DIO | TYPE 6 | SIM card IO | - | VSIM |
| K11 | SIM0_SRST | DIO | TYPE 6 | SIM card reset | - | VSIM |
| L11 | SIM0_SCLK | DIO | TYPE 6 | SIM card clock | - | VSIM |
| **General Programmable I/O** | | | | | | |
| A6 | GPIO0 | DIO | TYPE 5 | General purpose input/output, Pin 0 | PWM (0)<br>KP<br>CLKO0 | DVDD_IO_2 |
| B6 | GPIO1 | DIO | TYPE 5 | General purpose input/output, Pin 1 | UART (1)<br>I2C (0)<br>I2S (0)<br>KP<br>PWM (0) | DVDD_IO_2 |
| B5 | GPIO2 | DIO | TYPE 1 | General purpose input/output, Pin 2 | UART (0) | DVDD_IO_2 |
| C7 | GPIO3 | DIO | TYPE 4 | General purpose input/output, Pin 3 | UART (2)<br>I2C (1)<br>I2S (0)<br>KP<br>UART (1)<br>CLKO0 | DVDD_IO_2 |
| C6 | GPIO4 | DIO | TYPE 4 | General purpose input/output, Pin 4 | UART (2)<br>I2C (1)<br>I2S (0)<br>KP<br>UART (1)<br>PWM (0) | DVDD_IO_2 |
| D6 | GPIO5 | DIO | TYPE 1 | General purpose input/output, Pin 5 | UART (0) | DVDD_IO_2 |
| A4 | GPIO6 | DIO | TYPE 2 | General purpose input/output, Pin 6 | SDIO Slave<br>SPI Master (0)<br>I2S (0) | DVDD_IO_2 |

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| | | | | | I2C (0) | |
| A5 | GPIO7 | DIO | TYPE 2 | General purpose input/output, Pin 7 | SDIO Slave<br>SPI Master (0)<br>I2S (0)<br>I2C (0)<br>PWM (1) | DVDD_IO_2 |
| D7 | GPIO8 | DIO | TYPE 2 | General purpose input/output, Pin 8 | SDIO Slave<br>SPI Master (0)<br>I2S (0)<br>PWM (1) | DVDD_IO_2 |
| A3 | GPIO9 | DIO | TYPE 2 | General purpose input/output, Pin 9 | SDIO Slave<br>SPI Master (0)<br>I2S (0) | DVDD_IO_2 |
| A2 | GPIO10 | DIO | TYPE 2 | General purpose input/output, Pin 10 | SDIO Slave<br>SPI Master (0)<br>I2C (1)<br>CLKO1 | DVDD_IO_2 |
| B3 | GPIO11 | DIO | TYPE 2 | General purpose input/output, Pin 11 | SDIO Slave<br>SPI Master (0) | DVDD_IO_2 |
| A1 | GPIO12 | DIO | TYPE 2 | General purpose input/output, Pin 12 | SDIO Master (0)<br>SPI Slave (0)<br>UART (1)<br>CLKO1 | DVDD_IO_0 |
| D5 | GPIO13 | DIO | TYPE 2 | General purpose input/output, Pin 13 | SDIO Master (0)<br>SPI Slave (0)<br>UART (1)<br>PWM (2)<br>PWMSG | DVDD_IO_0 |
| B1 | GPIO14 | DIO | TYPE 2 | General purpose input/output, Pin 14 | SDIO Master (0)<br>SPI Slave (0)<br>UART (1)<br>UART (3)<br>CLKO2 | DVDD_IO_0 |
| C3 | GPIO15 | DIO | TYPE 2 | General purpose input/output, Pin 15 | SDIO Master (0)<br>SPI Slave (0)<br>UART (1)<br>UART (3)<br>PWM (2) | DVDD_IO_0 |
| C4 | GPIO16 | DIO | TYPE 2 | General purpose input/output, Pin 16 | SDIO Master (0)<br>SPI Slave (0)<br>I2C (1)<br>UART (1)<br>PWMSG | DVDD_IO_0 |
| C2 | GPIO17 | DIO | TYPE 2 | General purpose input/output, Pin 17 | SDIO Master (0)<br>SPI Slave (0)<br>I2C (1)<br>UART (1) | DVDD_IO_0 |

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| D4 | GPIO18 | DIO | TYPE 2 | General purpose input/output, Pin 18 | SDIO Master (1)<br>SPI Master (1)<br>UART (1)<br>UART (2) | DVDD_IO_2 |
| D3 | GPIO19 | DIO | TYPE 2 | General purpose input/output, Pin 19 | SDIO Master (1)<br>SPI Master (1)<br>MD JTAG<br>CLKO3 | DVDD_IO_2 |
| E4 | GPIO20 | DIO | TYPE 2 | General purpose input/output, Pin 20 | SDIO Master (1)<br>SPI Master (1)<br>MD JTAG<br>PWM (3) | DVDD_IO_2 |
| F5 | GPIO21 | DIO | TYPE 2 | General purpose input/output, Pin 21 | SDIO Master (1)<br>SPI Master (1)<br>PWMSG | DVDD_IO_2 |
| D2 | GPIO22 | DIO | TYPE 2 | General purpose input/output, Pin 22 | SDIO Master (1)<br>SPI Master (1)<br>I2C (1)<br>UART (2) | DVDD_IO_2 |
| D1 | GPIO23 | DIO | TYPE 2 | General purpose input/output, Pin 23 | SDIO Master (1)<br>SPI Master (1)<br>I2C (1)<br>UART (2)<br>UART (1) | DVDD_IO_2 |
| F4 | GPIO24 (MT2625D) | DIO | TYPE 1 | General purpose input/output, Pin 24 | I2S (0)<br>UART (1)<br>PWMSG<br>CLKO3 | DVDD_IO_2 |
| | SFSCS0 (MT2625A) | DIO | TYPE 7 | Serial flash CS interface | - | DVDD18_MLDO |
| E3 | GPIO25 (MT2625D) | DIO | TYPE 1 | General purpose input/output, Pin 25 | I2S (0)<br>UART (1)<br>PWMSG | DVDD_IO_2 |
| | SFSHOLD (MT2625A) | DIO | TYPE 7 | Serial flash HOLD interface | - | DVDD18_MLDO |
| G4 | GPIO26 (MT2625D) | DIO | TYPE 1 | General purpose input/output, Pin 26 | I2S (0)<br>UART (2)<br>UART (3)<br>PWM (3) | DVDD_IO_2 |
| | SFSIN (MT2625A) | DIO | TYPE 7 | Serial flash IN interface | - | DVDD18_MLDO |
| F2 | GPIO27 (MT2625D) | DIO | TYPE 1 | General purpose input/output, Pin 27 | I2S (0)<br>UART (2)<br>UART (3) | DVDD_IO_2 |
| | SFSCK (MT2625A) | DIO | TYPE 7 | Serial flash CK interface | - | DVDD18_MLDO |

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| G3 | GPIO28 (MT2625D) | DIO | TYPE 1 | General purpose input/output, Pin 28 | I2S (0)<br>UART (2)<br>I2C (2) | DVDD_IO_2 |
| | SFSWP (MT2625A) | DIO | TYPE 7 | Serial flash WP interface | - | DVDD18_MLDO |
| F3 | GPIO29 (MT2625D) | DIO | TYPE 1 | General purpose input/output, Pin 29 | UART (2)<br>I2C (2)<br>CLKO4 | DVDD_IO_2 |
| | SFSOUT (MT2625A) | DIO | TYPE 7 | Serial flash OUT interface | - | DVDD18_MLDO |
| K8 | GPIO30 | DIO | TYPE 3 | General purpose input/output, Pin 30 | I2S (1)<br>AP JTAG<br>CLKO3<br>MD JTAG<br>AUXADC0 | DVDD_IO_1 |
| J9 | GPIO31 | DIO | TYPE 3 | General purpose input/output, Pin 31 | I2S (1)<br>AP JTAG<br>UART (2)<br>MD JTAG<br>AUXADC1 | DVDD_IO_1 |
| H6 | GPIO32 | DIO | TYPE 3 | General purpose input/output, Pin 32 | I2S (1)<br>AP JTAG<br>UART (2)<br>CLKO4<br>AUXADC2<br>PWM (3) | DVDD_IO_1 |
| H8 | GPIO33 | DIO | TYPE 3 | General purpose input/output, Pin 33 | I2S (1)<br>AP JTAG<br>UART (3)<br>I2C (2)<br>AUXADC3 | DVDD_IO_1 |
| H7 | GPIO34 | DIO | TYPE 3 | General purpose input/output, Pin 34 | I2S (1)<br>AP JTAG<br>UART (3)<br>I2C (2)<br>AUXADC4 | DVDD_IO_1 |
| J10 | GPIO35 | DIO | TYPE 5 | General purpose input/output, Pin 35 | UART (2)<br>I2C (2)<br>KP<br>CLKO0 | DVDD_IO_1 |
| G8 | GPIO36 | DIO | TYPE 4 | General purpose input/output, Pin 36 | UART (2)<br>I2C (2)<br>KP | DVDD_IO_1 |
| **BPI** | | | | | | |
| D8 | BPI0 | DIO | TYPE 1 | BPI, pin 0 | - | DVDD_IO_1 |
| F8 | BPI1 | DIO | TYPE 1 | BPI, pin 1 | - | DVDD_IO_1 |
| E8 | BPI2 | DIO | TYPE 1 | BPI, pin 2 | - | DVDD_IO_1 |

| Pin Number MT2625 | Pin Name | Pin Type | IO Structure | Pin Description | Alternate Pin Functions | Power domain |
|---|---|---|---|---|---|---|
| G10 | BPI3 | DIO | TYPE 1 | BPI, pin 3 | - | DVDD_IO_1 |
| F9 | BPI4 | DIO | TYPE 1 | BPI, pin 4 | - | DVDD_IO_1 |
| **MIPI** | | | | | | |
| H10 | MIPI_SCLK | DIO | TYPE 1 | MIPI Clock | - | DVDD_IO_1 |
| H11 | MIPI_SDATA | DIO | TYPE 1 | MIPI Data | - | DVDD_IO_1 |

## 5.5. MT2625 family pin multiplexing

MT2625D series platform offers 37 GPIO pins, MT2625A series platform offers 31 GPIO pins. By setting up the control registers, the MCU software can control the direction, the output value and read the input values on the pins. The GPIOs and GPOs are multiplexed with other functions to reduce the pin count. To facilitate application use, the software can configure which clock to send outside the chip. There are five clock-out ports embedded in MT2625D 37 GPIO pins, MT2625A 31 GPIO pins and each clock-out can be programmed to output an appropriate clock source. In addition, when two GPIOs function for the same peripheral IP, the smaller GPIO serial number has higher priority over the bigger one.

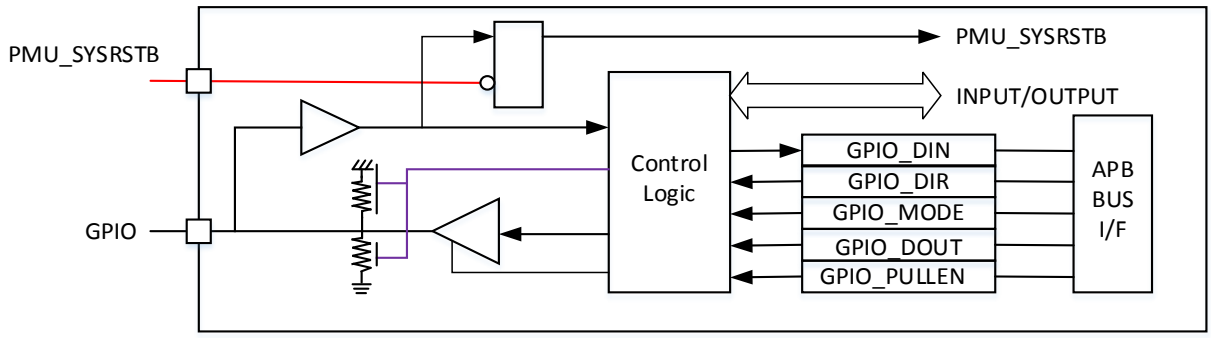



***Figure 5.5-1. GPIO block diagram***

MT2625 series has rich peripheral functions and the peripheral signals are shown in Table 5.5-1. The SDIO, SPI Master and SPI Slave can support signal group allocate on different pins.

***Table 5.5-1. Peripheral functions and signals***

| Alternate Function | Signal List |
|---|---|
| MSDC (0) | MSDC0_CLK<br>MSDC0_CMD<br>MSDC0_DAT0<br>MSDC0_DAT1<br>MSDC0_DAT2<br>MSDC0_DAT3 |
| MSDC (1) | MSDC1_CLK |

| Alternate Function | Signal List |
|---|---|
| SPI Master (0) | SPI_MST0_SCK<br>SPI_MST0_CS<br>SPI_MST0_MISO<br>SPI_MST0_MOSI<br>SPI_MST0_SIO2<br>SPI_MST0_SIO3 |
| SPI Master (1) | SPI_MST1_SCK |

| | |
|---|---|
| | MSDC1_CMD |
| | MSDC1_DAT0 |
| | MSDC1_DAT1 |
| | MSDC1_DAT2 |
| | MSDC1_DAT3 |
| SDIO Slave | SDIO_SLV0_CLK |
| | SDIO_SLV0_CMD |
| | SDIO_SLV0_DAT0 |
| | SDIO_SLV0_DAT1 |
| | SDIO_SLV0_DAT2 |
| | SDIO_SLV0_DAT3 |
| UART (0) | UART0_RXD |
| | UART0_TXD |
| UART (1) | UART1_RXD |
| | UART1_TXD |
| | UART1_RTS |
| | UART1_CTS |
| UART (2) | UART2_RXD |
| | UART2_TXD |
| | UART2_RTS |
| | UART2_CTS |
| UART (3) | UART3_RXD |
| | UART3_TXD |
| I2C (0) | I2C0_SCL |
| | I2C0_SDA |
| I2C (1) | I2C1_SCL |
| | I2C1_SDA |
| I2C (2) | I2C2_SCL |
| | I2C2_SDA |
| I2S Master/Slave (0) | I2S0_RX |
| | I2S0_TX |
| | I2S0_WS |
| | I2S0_CK |
| | I2S0_MCLK |
| I2S Master/Slave (1) | I2S1_RX |
| | I2S1_TX |
| | I2S1_WS |
| | I2S1_CK |
| | I2S1_MCLK |

| | |
|---|---|
| | SPI_MST1_CS |
| | SPI_MST1_MISO |
| | SPI_MST1_MOSI |
| | SPI_MST1_SIO2 |
| | SPI_MST1_SIO3 |
| SPI Slave (0) | SPI_SLV0_SCK |
| | SPI_SLV0_CS |
| | SPI_SLV0_MISO |
| | SPI_SLV0_MOSI |
| | SPI_SLV0_SIO2 |
| | SPI_SLV0_SIO3 |
| PWM (0) | PWM0 |
| PWM (1) | PWM1 |
| PWM (2) | PWM2 |
| PWM (3) | PWM3 |
| PWMSG | PWMSG0 |
| | PWMSG1 |
| AUXADC | AUXADCIN_0 |
| | AUXADCIN_1 |
| | AUXADCIN_2 |
| | AUXADCIN_3 |
| | AUXADCIN_4 |
| Cortex®-M4 JTAG | AP_JTDI |
| | AP_JRSTB |
| | AP_JTDO |
| | AP_JTMS |
| | AP_JTCK |
| MD JTAG | MD_JTMS |
| | MD_JTCK |
| Keypad | KP_COL0 |
| | KP_COL1 |
| | KP_COL2 |
| | KP_ROW0 |
| | KP_ROW1 |
| | KP_ROW2 |

*Figure 5.5-2. PinMux description*

| Pin Name | Mode 0 | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 5 | Mode 6 | Mode 7 |
|---|---|---|---|---|---|---|---|---|
| **GPIO_0** | GPIO0 | | | PWM0 | KP_COL0 | CLKO0 | | |
| **GPIO_1** | GPIO1 | UART1_RTS | I2C0_SDA | I2S0_RX | KP_COL1 | PWM0 | GPS_BLANKING | EINT1 |
| **GPIO_2** | GPIO2 | UART0_RXD | | | | | | EINT2 |
| **GPIO_3** | GPIO3 | UART2_RXD | I2C1_SCL | I2S0_CK | KP_ROW0 | UART1_RXD | CLKO0 | EINT3 |
| **GPIO_4** | GPIO4 | UART2_TXD | I2C1_SDA | I2S0_MCLK | KP_ROW1 | UART1_TXD | PWM0 | EINT4 |
| **GPIO_5** | GPIO5 | UART0_TXD | | | | | | EINT5 |
| **GPIO_6** | GPIO6 | SDIO_SLV0_DAT1 | SPI_MST0_SIO3 | I2S0_WS | I2C0_SCL | NBIOT_PRI | GPS_BLANKING | EINT6 |
| **GPIO_7** | GPIO7 | SDIO_SLV0_CMD | SPI_MST0_SIO2 | I2S0_TX | I2C0_SDA | PWM1 | GPS_FRAME_SYNC | EINT7 |
| **GPIO_8** | GPIO8 | SDIO_SLV0_DAT0 | SPI_MST0_CS | I2S0_CK | PWM1 | NBIOT_ACT | PAD_DFUNC_SFCK | EINT8 |
| **GPIO_9** | GPIO9 | SDIO_SLV0_CLK | SPI_MST0_MISO | I2S0_MCLK | RF_CONFL_DET_IRQ_B | WLAN_ACT | PAD_DFUNC_SFCS0 | EINT9 |
| **GPIO_10** | GPIO10 | SDIO_SLV0_DAT3 | SPI_MST0_MOSI | I2C1_SCL | GPS_FRAME_SYNC | PMU_RGU_RSTB | CLKO1 | EINT10 |
| **GPIO_11** | GPIO11 | SDIO_SLV0_DAT2 | SPI_MST0_SCK | | GPS_BLANKING | PMU_GOTO_SLEEP | PWMSG0 | EINT11 |
| **GPIO_12** | GPIO12 | MSDC0_DAT1 | SPI_SLV0_CS | UART1_RXD | CLKO1 | PMU_GOTO_SLEEP | PAD_DFUNC_SWP | EINT12 |
| **GPIO_13** | GPIO13 | MSDC0_CMD | SPI_SLV0_MOSI | UART1_TXD | PWM2 | PWMSG0 | PAD_DFUNC_SHOLD | EINT13 |
| **GPIO_14** | GPIO14 | MSDC0_DAT0 | SPI_SLV0_MISO | UART1_RTS | UART3_RXD | CLKO2 | PAD_DFUNC_SIN | EINT14 |
| **GPIO_15** | GPIO15 | MSDC0_CLK | SPI_SLV0_SCK | UART1_CTS | UART3_TXD | PWM2 | PAD_DFUNC_SOUT | EINT15 |
| **GPIO_16** | GPIO16 | MSDC0_DAT2 | SPI_SLV0_SIO2 | I2C1_SCL | UART1_RXD | GPS_FRAME_SYNC | PWMSG0 | EINT16 |
| **GPIO_17** | GPIO17 | MSDC0_DAT3 | SPI_SLV0_SIO3 | I2C1_SDA | UART1_TXD | XO_WAKEUP | | EINT17 |
| **GPIO_18** | GPIO18 | MSDC1_DAT2 | SPI_MST1_SIO2 | UART2_RXD | UART1_CTS | GPS_BLANKING | RF_CONFL_DET_IRQ_B | EINT18 |
| **GPIO_19** | GPIO19 | MSDC1_DAT1 | SPI_MST1_CS | MD_JTMS | CLKO3 | GSM_TIMING_SYNC | | EINT19 |
| **GPIO_20** | GPIO20 | MSDC1_CMD | SPI_MST1_MISO | MD_JTCK | PWM3 | GSM_RF_CONFL_DET_EN | | EINT20 |
| **GPIO_21** | GPIO21 | MSDC1_DAT0 | SPI_MST1_MOSI | | | PWMSG1 | | EINT21 |
| **GPIO_22** | GPIO22 | MSDC1_CLK | SPI_MST1_SCK | I2C1_SCL | PMU_GOTO_SLEEP | UART2_TXD | | EINT22 |
| **GPIO_23** | GPIO23 | MSDC1_DAT3 | SPI_MST1_SIO3 | I2C1_SDA | UART2_TXD | UART1_RTS | | EINT0 |

| Pin Name | Mode 0 | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Mode 5 | Mode 6 | Mode 7 |
|---|---|---|---|---|---|---|---|---|
| **GPIO_24 (MT2625D only)** | GPIO24 | I2S0_RX | UART1_RXD | PWMSG1 | XO_WAKEUP | CLKO3 | | EINT1 |
| **GPIO_25 (MT2625D only)** | GPIO25 | I2S0_TX | UART1_TXD | | PMU_RGU_RSTB | PWMSG1 | GSM_TIMING_SYNC | EINT2 |
| **GPIO_26 (MT2625D only)** | GPIO26 | I2S0_WS | UART2_RTS | UART3_RXD | PMU_GOTO_SLEEP | PWM3 | GSM_RF_CONFL_DET_EN | EINT3 |
| **GPIO_27 (MT2625D only)** | GPIO27 | I2S0_CK | UART2_CTS | UART3_TXD | NBIOT_PRI | GPS_FRAME_SYNC | RF_CONFL_DET_IRQ_B | EINT4 |
| **GPIO_28 (MT2625D only)** | GPIO28 | I2S0_MCLK | UART2_RXD | I2C2_SCL | NBIOT_ACT | GPS_BLANKING | | EINT5 |
| **GPIO_29 (MT2625D only)** | GPIO29 | | UART2_TXD | I2C2_SDA | WLAN_ACT | CLKO4 | | EINT6 |
| **GPIO_30** | GPIO30 | I2S1_RX | AP_JTDI | CLKO3 | MD_JTMS | AUXADCIN_0 | | EINT7 |
| **GPIO_31** | GPIO31 | I2S1_TX | AP_JRSTB | UART2_RXD | MD_JTCK | AUXADCIN_1 | | EINT8 |
| **GPIO_32** | GPIO32 | I2S1_WS | AP_JTDO | UART2_TXD | CLKO4 | AUXADCIN_2 | PWM3 | EINT9 |
| **GPIO_33** | GPIO33 | I2S1_CK | AP_JTMS | UART3_RXD | I2C2_SCL | AUXADCIN_3 | | EINT10 |
| **GPIO_34** | GPIO34 | I2S1_MCLK | AP_JTCK | UART3_TXD | I2C2_SDA | AUXADCIN_4 | WLAN_ACT | EINT11 |
| **GPIO_35** | GPIO35 | UART2_RXD | I2C2_SCL | | KP_COL2 | | CLKO0 | EINT12 |
| **GPIO_36** | GPIO36 | UART2_TXD | I2C2_SDA | | KP_ROW2 | GPS_BLANKING | RF_CONFL_DET_IRQ_B | EINT13 |

# 6. Electrical Characteristics

## 6.1. Absolute maximum ratings

*Table 6.1-1. Absolute maximum ratings for power supply*

| Symbol or pin name | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| AVDD33_LDO | Power for internal controller and LDO | -0.3 | 3.63 | V |
| AVDD33_VCORE | Input power for BUCK of VCORE | -0.3 | 3.63 | V |
| AVDD33_VPA | Input power for BUCK of VPA | -0.3 | 3.63 | V |
| AVDD33_VPA_CTRL | Power of VPA controller | -0.3 | 3.63 | V |
| AVDD33_VRF | Input power for BUCK of VRF | -0.3 | 3.63 | V |
| AVDD33_VSIM | Power of LDO of VSIM | -0.3 | 3.63 | V |
| AVDD_RF | Input power for RF | 1.08 | 1.32 | V |
| AVDD18_RF | Input power for RF | 1.62 | 1.98 | V |
| AVDD33_VUSB | USB supply voltage | 2.97 | 3.63 | V |

*Table 6.1-2. Absolute maximum ratings for I/O power supply*

| Symbol or pin name | Description | Min. | Typ.1 | Typ.2 | Max. | Unit |
|---|---|---|---|---|---|---|
| DVDD_IO_0 | Power supply for GPIO group 0 | 1.62 | 1.8 | 3.3 | 3.63 | V |
| DVDD_IO_1 | Power supply for GPIO group 1 | 1.62 | 1.8 | 3.3 | 3.63 | V |
| DVDD_IO_2 | Power supply for GPIO group 1 | 1.62 | 1.8 | 3.3 | 3.63 | V |
| DVDD18_MLDO | Power supply for SF/EMI IO 1.8V group | 1.65 | 1.8 | - | 1.95 | V |

*Table 6.1-3. Absolute maximum ratings for voltage input*

| Symbol or pin name | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| VIN0 | Digital input voltage for IO Type 0 | -0.3 | 3.63 | V |
| VIN1 | Digital input voltage for IO Type 1 | -0.3 | 5.5 | V |
| VIN2 | Digital input voltage for IO Type 2 | -0.3 | 5.5 | V |
| VIN3 | Digital input voltage for IO Type 3 | -0.3 | 5.5 | V |
| VIN4 | Digital input voltage for IO Type 4 | -0.3 | 5.5 | V |
| VIN5 | Digital input voltage for IO Type 5 | -0.3 | 5.5 | V |
| VIN6 | Digital input voltage for IO Type 6 | -0.3 | 3.63 | V |
| VIN7 | Digital input voltage for IO Type 7 | -0.3 | 1.98 | V |

*Table 6.1-4. Absolute maximum ratings for storage temperature*

| Symbol or pin name | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| Tstg | Storage temperature | -55 | 125 | °C |

## 6.2. Operating conditions

### 6.2.1. General operating conditions

*Table 6.2-1. MT2625DA/AA general operating conditions*

| Item | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{CPU}$ | Internal Cortex-M4 & TCM & Cache clock | VCORE = 1.1V | 0 | - | 78 | MHz |
| $F_{EMI}$ | Internal memory EMI related AHB and APB clock. Synchronous with $F_{CPU}$. | VCORE = 1.1V | 0 | - | 39 | MHz |
| $F_{SFC}$ (MT2625DA only) | Internal memory SFC related AHB and APB clock. Synchronous with $F_{CPU}$. | VCORE = 1.1V | 0 | - | 78 | MHz |

*Table 6.2-2. MT2625DPA/APA general operating conditions*

| Item | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{CPU}$ | Internal Cortex-M4 & TCM & Cache clock | VCORE = 1.3V | 0 | - | 156 | MHz |
| $F_{EMI}$ | Internal memory EMI related AHB and APB clock. Synchronous with $F_{CPU}$. | VCORE = 1.3V | 0 | - | 78 | MHz |
| $F_{SFC}$ (DPA only) | Internal memory SFC related AHB and APB clock. Synchronous with $F_{CPU}$. | VCORE = 1.3V | 0 | - | 78 | MHz |

*Table 6.2-3. Recommended operating conditions for power supply*

| Symbol or pin name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| AVDD33_LDO | Power for internal controller and LDO | 2.1 | 3.3 | 3.63 | V |
| AVDD33_VCORE | Input power for BUCK of VCORE | 2.1 | 3.3 | 3.63 | V |
| AVDD33_VPA | Input power for BUCK of VPA | - | 3.3 | 3.63 | V |
| AVDD33_VPA_CTRL | Power of VPA controller | - | 3.3 | 3.63 | V |
| AVDD33_VRF | Input power for BUCK of VRF | 2.1 | 3.3 | 3.63 | V |
| AVDD33_VSIM | Power of LDO of VSIM | - | 3.3 | 3.63 | V |

*Table 6.2-4. Recommended operating conditions for voltage input*

| Symbol or pin name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VIN0 | Digital input voltage for IO Type 0 | -0.3 | - | DVDIO+0.3 | V |
| VIN1 | Digital input voltage for IO Type 1 | -0.3 | - | DVDIO+0.3 | V |
| VIN2 | Digital input voltage for IO Type 2 | -0.3 | - | DVDIO+0.3 | V |
| VIN3 | Digital input voltage for IO Type 3 | -0.3 | - | DVDIO+0.3 | V |
| VIN4 | Digital input voltage for IO Type 4 | -0.3 | - | DVDIO+0.3 | V |

| Symbol or pin name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VIN5 | Digital input voltage for IO Type 5 | -0.3 | - | DVDIO+0.3 | V |
| VIN6 | Digital input voltage for IO Type 6 | -0.3 | - | DVDIO+0.3 | V |
| VIN7 | Digital input voltage for IO Type 7 | -0.3 | - | DVDIO+0.3 | V |

***Table 6.2-5. Recommended operating conditions for operating temperature***

| Symbol or pin name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Tc | Operating temperature | -40 | - | 85 | °C |

## 6.2.2. Input or output port characteristics

***Table 6.2-6. Electrical characteristics***

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DIIH0 | Digital high input current for IO Type 0 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>DVDIO*0.65 < VIN0 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | PU enabled<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN0 < DVDIO | 40 | - | 5 | µA |
| | | PD enabled<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN0 < DVDIO | 7 | - | 80 | µA |
| DIIL0 | Digital low input current for IO Type 0 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN0 < DVDIO*0.35 | -10 | - | 5 | µA |
| | | PU enabled,<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN0 < DVDIO*0.25 | -70 | - | -6 | µA |
| | | PD enabled,<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN0 < DVDIO*0.25 | -5 | - | 40 | µA |
| DIOH0 | Digital high output current for IO Type 0 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V | 8 | - | - | mA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | Max. driving mode | | | | |
| DIOL0 | Digital low output current for IO Type 0 | DVOL = 0.495V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOL = 0.442V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOL = 0.27V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DRPU0 | Digital I/O pull-up resistance for IO Type 0 | DVDIO = 3.3V<br>VIN0 = 0V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN0 = 0 | 40 | 75 | 190 | kΩ |
| | | DVDIO = 1.8V<br>VIN0 = 0V | 80 | 160 | 320 | kΩ |
| DRPD0 | Digital I/O pull-down resistance for IO Type 0 | DVDIO = 3.3V<br>VIN0 = 3.3V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN0 = 2.8V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 1.8V<br>VIN0 = 1.8V | 80 | 160 | 320 | kΩ |
| DVOH0 | Digital output high voltage for IO Type 0 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL0 | Digital output low voltage for IO Type 0 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH0 | Digital input high voltage for IO Type 0 | DVDIO = 3.3V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL0 | Digital input low voltage for IO Type 0 | DVDIO = 3.3V | 0 | | 0.25*DVDIO | |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |
| DIIH1 | Digital high input current for IO Type 1 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>DVDIO*0.65 < VIN1 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | DVDIO = 3.3V<br>4.5V < VIN1 < 5.5V | -5 | - | 5 | µA |
| | | PU enabled<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN1 < DVDIO | -40 | | 5 | µA |
| | | PD enabled<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN1 < DVDIO | 7 | | 80 | µA |
| DIIL1 | Digital low input current for IO Type 1 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN1 < DVDIO*0.35 | -10 | - | 5 | µA |
| | | PU enabled<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN1 < DVDIO*0.25 | -70 | - | -6 | µA |
| | | PD enabled<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN1 < DVDIO*0.25 | -5 | - | 40 | µA |
| DIOH1 | Digital high output current for IO Type 1 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DIOL1 | Digital low output current for IO Type 1 | DVOL = 0.495V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOL = 0.442V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOL = 0.27V | 8 | - | - | mA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO = 1.8V<br>Max. driving mode | | | | |
| DRPU1 | Digital I/O pull-up resistance for IO Type 1 | DVDIO = 3.3V<br>VIN1 = 0V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN1 = 0V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 1.8V<br>VIN1 = 0V | 80 | 160 | 320 | kΩ |
| DRPD1 | Digital I/O pull-down resistance for IO Type 1 | DVDIO = 3.3V<br>VIN1 = 3.3V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN1 = 2.8V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 1.8V<br>VIN1 = 1.8V | 80 | 160 | 320 | kΩ |
| DVOH1 | Digital output high voltage for IO Type 1 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL1 | Digital output low voltage for IO Type 1 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH1 | Digital input high voltage for IO Type 1 | DVDIO = 3.3V | 2.0V | | DVDIO | |
| | | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL1 | Digital input low voltage for IO Type 1 | DVDIO = 3.3V | 0 | | 0.8 | |
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |
| DIIH2 | Digital high input current for IO Type 2 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>DVDIO*0.65 < VIN2 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | DVDIO = 3.3V<br>4.5V < VIN2 < 5.5V | -5 | - | 5 | µA |
| | | PU enabled, RSEL1 | -60 | - | 5 | µA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN2 < DVDIO | | | | |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN2 < DVDIO | -120 | - | 5 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN2 < DVDIO | 10 | - | 110 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN2 < DVDIO | 20 | - | 220 | µA |
| DIIL2 | Digital low input current for IO Type 2 | PU/PD disabled,<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN2 < DVDIO*0.35 | -10 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN2 < DVDIO*0.25 | -100 | - | -10 | µA |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN2 < DVDIO*0.25 | -200 | - | -20 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN2 < DVDIO*0.25 | -5 | - | 60 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN2 < DVDIO*0.25 | -5 | - | 120 | µA |
| DIOH2 | Digital high output current for IO Type 2 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DIOL2 | Digital low output current for IO Type 2 | DVOL = 0.495V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOL = 0.42V | 20 | - | - | mA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO = 2.8V<br>Max. driving mode | | | | |
| | | DVOL = 0.27V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DRPU2 | Digital I/O pull-up resistance for IO Type 2<br>RSEL1 : (GPIO_R1, GPIO_R0) = (1, 0) or (0,1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 1) | DVDIO = 3.3V<br>VIN2 = 0V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 3.3V<br>VIN2 = 0V, RSEL2 | 10 | 23 | 50 | kΩ |
| | | DVDIO = 2.8V<br>VIN2 = 0V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN2 = 0V, RSEL2 | 10 | 23 | 50 | kΩ |
| | | DVDIO = 1.8V<br>VIN2 = 0V, RSEL1 | 50 | 100 | 200 | kΩ |
| | | DVDIO = 1.8V<br>VIN2 = 0V, RSEL2 | 25 | 50 | 100 | kΩ |
| DRPD2 | Digital I/O pull-down resistance for IO Type 2<br>RSEL1 : (GPIO_R1, GPIO_R0) = (1, 0) or (0,1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 1) | DVDIO = 3.3V<br>VIN2 = 3.3V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 3.3V<br>VIN2 = 3.3V, RSEL2 | 10 | 23 | 50 | kΩ |
| | | DVDIO = 2.8V<br>VIN2 = 2.8V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN2 = 2.8V, RSEL2 | 10 | 23 | 50 | kΩ |
| | | DVDIO = 1.8V<br>VIN2 = 1.8V, RSEL1 | 50 | 100 | 200 | kΩ |
| | | DVDIO = 1.8V<br>VIN2 = 1.8V, RSEL2 | 25 | 50 | 100 | kΩ |
| DVOH2 | Digital output high voltage for IO Type 2 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL2 | Digital output low voltage for IO Type 2 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH2 | | DVDIO = 3.3V | 2.0V | | DVDIO | |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Digital input high voltage for IO Type 2 | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL2 | Digital input low voltage for IO Type 2 | DVDIO = 3.3V | 0 | | 0.8 | |
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |
| DIIH3 | Digital high input current for IO Type 3 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>DVDIO*0.65 < VIN3 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | DVDIO = 3.3V<br>4.5V < VIN3 < 5.5V | -5 | - | 5 | µA |
| | | PU enabled<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN3 < DVDIO | -40 | | 5 | µA |
| | | PD enabled<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN3 < DVDIO | 7 | | 80 | µA |
| DIIL3 | Digital low input current for IO Type 3 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN3 < DVDIO*0.35 | -10 | - | 5 | µA |
| | | PU enabled<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN3 < DVDIO*0.25 | -70 | - | -6 | µA |
| | | PD enabled<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN3 < DVDIO*0.25 | -5 | - | 40 | µA |
| DIOH3 | Digital high output current for IO Type 3 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DIOL3 | Digital low output current for IO Type 3 | DVOL = 0.495V<br>DVDIO = 3.3V | 24 | - | - | mA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | Max. driving mode | | | | |
| | | DVOL = 0.442V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOL = 0.27V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DRPU3 | Digital I/O pull-up resistance for IO Type 3 | DVDIO = 3.3V<br>VIN3 = 0V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN3 = 0V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 1.8V<br>VIN3 = 0V | 80 | 160 | 320 | kΩ |
| DRPD3 | Digital I/O pull-down resistance for IO Type 3 | DVDIO = 3.3V<br>VIN3 = 3.3V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN3 = 2.8V | 40 | 75 | 190 | kΩ |
| | | DVDIO = 1.8V<br>VIN3 = 1.8V | 80 | 160 | 320 | kΩ |
| DVOH3 | Digital output high voltage for IO Type 3 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL3 | Digital output low voltage for IO Type 3 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH3 | Digital input high voltage for IO Type 3 | DVDIO = 3.3V | 2.0V | | DVDIO | |
| | | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL3 | Digital input low voltage for IO Type 3 | DVDIO = 3.3V | 0 | | 0.8 | |
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |
| DIIH4 | Digital high input current for IO Type 4 | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V, | -5 | - | 5 | µA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | RSEL1 : (GPIO_R1, GPIO_R0) = (0,1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) or (1, 1) | DVDIO*0.65 < VIN4 < DVDIO+0.3V | | | | |
| | | DVDIO = 3.3V<br>4.5V < VIN4 < 5.5V | -5 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN4 < DVDIO | -60 | - | 5 | µA |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN4 < DVDIO | -700 | - | 5 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN4 < DVDIO | 10 | - | 110 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN4 < DVDIO | 500 | - | 3000 | µA |
| DIIL4 | Digital low input current for IO Type 4<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0,1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) or (1, 1) | PU/PD disabled,<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN4 < DVDIO*0.35 | -10 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN4 < DVDIO*0.25 | -100 | - | -10 | µA |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN4 < DVDIO*0.25 | -3000 | - | -500 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN4 < DVDIO*0.25 | -5 | - | 60 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN4 < DVDIO*0.25 | -5 | - | **700** | µA |
| DIOH4 | Digital high output current for IO Type 4 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V | 8 | - | - | mA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | Max. driving mode | | | | |
| DIOL4 | Digital low output current for IO Type 4 | DVOL = 0.495V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOL = 0.42V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOL = 0.27V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DRPU4 | Digital I/O pull-up resistance for IO Type 4<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0,1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) or (1, 1) | DVDIO = 3.3V<br>VIN4 = 0V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 3.3V<br>VIN4 = 0V, RSEL2 | | | 2 | kΩ |
| | | DVDIO = 2.8V<br>VIN4 = 0V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN4 = 0V, RSEL2 | | | 2 | kΩ |
| | | DVDIO = 1.8V<br>VIN4 = 0V, RSEL1 | 50 | 100 | 200 | kΩ |
| | | DVDIO = 1.8V<br>VIN4 = 0V, RSEL2 | | | 2 | kΩ |
| DRPD4 | Digital I/O pull-down resistance for IO Type 4<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0,1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) or (1, 1) | DVDIO = 3.3V<br>VIN4 = 3.3V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 3.3V<br>VIN4 = 3.3V, RSEL2 | | | 2 | kΩ |
| | | DVDIO = 2.8V<br>VIN4 = 2.8V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN4 = 2.8V, RSEL2 | | | 2 | kΩ |
| | | DVDIO = 1.8V<br>VIN4 = 1.8V, RSEL1 | 50 | 100 | 200 | kΩ |
| | | DVDIO = 1.8V<br>VIN4 = 1.8V, RSEL2 | | | 2 | kΩ |
| DVOH4 | Digital output high voltage for IO Type 4 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL4 | Digital output low voltage for IO Type 4 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH4 | Digital input high voltage for IO Type 4 | DVDIO = 3.3V | 2.0V | | DVDIO | |
| | | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL4 | Digital input low voltage for IO Type 4 | DVDIO = 3.3V | 0 | | 0.8 | |
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |
| DIIH5 | Digital high input current for IO Type 5<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1) or (1, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>DVDIO*0.65 < VIN5 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | DVDIO = 3.3V<br>4.5V < VIN5 < 5.5V | -5 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN5 < DVDIO | -60 | - | 5 | µA |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN5 < DVDIO | -10 | - | 5 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN5 < DVDIO | 10 | - | 110 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN5 < DVDIO | 1 | - | 15 | µA |
| DIIL5 | Digital low input current for IO Type 5<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1) or (1, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | PU/PD disabled,<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN5 < DVDIO*0.35 | -10 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN5 < DVDIO*0.25 | -100 | - | -10 | µA |
| | | PU enabled, RSEL2 | -15 | - | -1 | µA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO = 3.3/2.8/1.8V<br>0 < VIN5 < DVDIO*0.25 | | | | |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN5 < DVDIO*0.25 | -5 | - | 60 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN5 < DVDIO*0.25 | -5 | - | 10 | µA |
| DIOH5 | Digital high output current for IO Type 5 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DIOL5 | Digital low output current for IO Type 5 | DVOL = 0.495V<br>DVDIO = 3.3V<br>Max. driving mode | 24 | - | - | mA |
| | | DVOL = 0.42V<br>DVDIO = 2.8V<br>Max. driving mode | 20 | - | - | mA |
| | | DVOL = 0.27V<br>DVDIO = 1.8V<br>Max. driving mode | 8 | - | - | mA |
| DRPU5 | Digital I/O pull-up resistance for IO Type 5<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1) or (1, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | DVDIO = 3.3V<br>VIN5 = 0V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 3.3V<br>VIN5 = 0V, RSEL2 | 200 | | | kΩ |
| | | DVDIO = 2.8V<br>VIN5 = 0V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN5 = 0V, RSEL2 | 200 | | | kΩ |
| | | DVDIO = 1.8V<br>VIN5 = 0V, RSEL1 | 50 | 100 | 200 | kΩ |
| | | DVDIO = 1.8V<br>VIN5 = 0V, RSEL2 | 200 | | | kΩ |
| DRPD5 | Digital I/O pull-down resistance for IO Type 5<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1) or (1, 1) | DVDIO = 3.3V<br>VIN5 = 3.3V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 3.3V<br>VIN5 = 3.3V, RSEL2 | 200 | | | kΩ |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | DVDIO = 2.8V<br>VIN5 = 2.8V, RSEL1 | 25 | 45 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN5 = 2.8V, RSEL2 | 200 | | | kΩ |
| | | DVDIO = 1.8V<br>VIN5 = 1.8V, RSEL1 | 50 | 100 | 200 | kΩ |
| | | DVDIO = 1.8V<br>VIN5 = 1.8V, RSEL2 | 200 | | | kΩ |
| DVOH5 | Digital output high voltage for IO Type 5 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL5 | Digital output low voltage for IO Type 5 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH5 | Digital input high voltage for IO Type 5 | DVDIO = 3.3V | 2.0V | | DVDIO | |
| | | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL5 | Digital input low voltage for IO Type 5 | DVDIO = 3.3V | 0 | | 0.8 | |
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |
| DIIH6 | Digital high input current for IO Type 6<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | PU/PD disabled<br>DVDIO = 3.3/2.8/1.8V,<br>DVDIO*0.65 < VIN6 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN6 < DVDIO | -60 | - | 5 | µA |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN6 < DVDIO | -200 | - | 5 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V | 10 | - | 80 | µA |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | DVDIO*0.75 < VIN6 < DVDIO | | | | |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>DVDIO*0.75 < VIN6 < DVDIO | 20 | - | 160 | µA |
| DIIL6 | Digital low input current for IO Type 6<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | PU/PD disabled,<br>DVDIO = 3.3/2.8/1.8V,<br>-0.3V < VIN6 < DVDIO*0.35 | -5 | - | 5 | µA |
| | | PU enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN6 < DVDIO*0.25 | -200 | - | -40 | µA |
| | | PU enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN6 < DVDIO*0.25 | -900 | - | -200 | µA |
| | | PD enabled, RSEL1<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN6 < DVDIO*0.25 | -5 | - | 40 | µA |
| | | PD enabled, RSEL2<br>DVDIO = 3.3/2.8/1.8V<br>0 < VIN6 < DVDIO*0.25 | -5 | - | 80 | µA |
| DIOH6 | Digital high output current for IO Type 6 | DVOH = 2.805V<br>DVDIO = 3.3V<br>Max. driving mode | 12 | - | - | mA |
| | | DVOH = 2.38V<br>DVDIO = 2.8V<br>Max. driving mode | 10 | - | - | mA |
| | | DVOH = 1.53V<br>DVDIO = 1.8V<br>Max. driving mode | 4 | - | - | mA |
| DIOL6 | Digital low output current for IO Type 6 | DVOL = 0.495V<br>DVDIO = 3.3V<br>Max. driving mode | 12 | - | - | mA |
| | | DVOL = 0.42V<br>DVDIO = 2.8V<br>Max. driving mode | 10 | - | - | mA |
| | | DVOL = 0.27V<br>DVDIO = 1.8V<br>Max. driving mode | 4 | - | - | mA |
| DRPU6 | Digital I/O pull-up resistance for IO Type 6 | DVDIO = 3.3V<br>VIN6 = 0V, RSEL1 | 10 | 20 | 40 | kΩ |
| | | DVDIO = 3.3V | 4 | 5 | 6 | kΩ |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | VIN6 = 0V, RSEL2 | | | | |
| | | DVDIO = 2.8V<br>VIN6 = 0V, RSEL1 | 10 | 20 | 40 | kΩ |
| | | DVDIO = 2.8V<br>VIN6 = 0V, RSEL2 | 4 | 5 | 6 | kΩ |
| | | DVDIO = 1.8V<br>VIN6 = 0V, RSEL1 | 10 | 20 | 40 | kΩ |
| | | DVDIO = 1.8V<br>VIN6 = 0V, RSEL2 | 4 | 5 | 6 | kΩ |
| DRPD6 | Digital I/O pull-down resistance for IO Type6<br>RSEL1 : (GPIO_R1, GPIO_R0) = (0, 1)<br>RSEL2 : (GPIO_R1, GPIO_R0) = (1, 0) | DVDIO = 3.3V<br>VIN6 = 3.3V, RSEL1 | 40 | 75 | 190 | kΩ |
| | | DVDIO = 3.3V<br>VIN6 = 3.3V, RSEL2 | 20 | 40 | 100 | kΩ |
| | | DVDIO = 2.8V<br>VIN6 = 2.8V, RSEL1 | 40 | 75 | 190 | kΩ |
| | | DVDIO = 2.8V<br>VIN6 = 2.8V, RSEL2 | 20 | 40 | 100 | kΩ |
| | | DVDIO = 1.8V<br>VIN6 = 1.8V, RSEL1 | 80 | 150 | 380 | kΩ |
| | | DVDIO = 1.8V<br>VIN6 = 1.8V, RSEL2 | 40 | 75 | 190 | kΩ |
| DVOH6 | Digital output high voltage for IO Type 6 | DVDIO = 3.3V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 2.8V | 0.85*DVDIO | - | - | V |
| | | DVDIO = 1.8V | 0.85*DVDD | - | - | V |
| DVOL6 | Digital output low voltage for IO Type 6 | DVDIO = 3.3V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 2.8V | - | - | 0.15*DVDIO | V |
| | | DVDIO = 1.8V | - | - | 0.15*DVDIO | V |
| VIH6 | Digital input high voltage for IO Type 6 | DVDIO = 3.3V | 2.0V | | DVDIO | |
| | | DVDIO = 2.8V | 0.75*DVDIO | | DVDIO | |
| | | DVDIO = 1.8V | 0.75*DVDIO | | DVDIO | |
| VIL6 | Digital input low voltage for IO Type 6 | DVDIO = 3.3V | 0 | | 0.8 | |
| | | DVDIO = 2.8V | 0 | | 0.25*DVDIO | |
| | | DVDIO = 1.8V | 0 | | 0.25*DVDIO | |

| Symbol | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DIIH7 | Digital high input current for IO Type 7 | PU/PD disabled<br>DVDIO = 1.8V,<br>DVDIO*0.65 < VIN7 < DVDIO+0.3V | -5 | - | 5 | µA |
| | | PU enabled<br>DVDIO = 1.8V<br>DVDIO*0.8 < VIN7 < DVDIO | -20 | - | 5 | µA |
| | | PD enabled<br>DVDIO = 1.8V<br>DVDIO*0.8 < VIN7 < DVDIO | 5 | - | 30 | µA |
| DIIL7 | Digital low input current for IO Type 7 | PU/PD disabled<br>DVDIO = 1.8V,<br>-0.3V < VIN7 < DVDIO*0.35 | -5 | - | 5 | µA |
| | | PU enabled,<br>DVDIO = 1.8V<br>0 < VIN7 < DVDIO*0.2 | -30 | - | -5 | µA |
| | | PD enabled,<br>DVDIO = 1.8V<br>0 < VIN7 < DVDIO*0.2 | -5 | - | 20 | µA |
| DIOH7 | Digital high output current for IO Type 7 | DVOH = 1.62V<br>DVDIO = 1.8V<br>Max. driving mode | 5 | - | - | mA |
| DIOL7 | Digital low output current for IO Type 7 | DVOL = 0.18V<br>DVDIO = 1.8V<br>Max. driving mode | 5 | - | - | mA |
| DRPU7 | Digital I/O pull-up resistance for IO Type 7 | DVDIO = 1.8V<br>VIN = 0V | 70 | 160 | 320 | kΩ |
| DRPD7 | Digital I/O pull-down resistance for IO Type 7 | DVDIO = 1.8V<br>VIN = 3.3V | 70 | 160 | 320 | kΩ |
| DVOH7 | Digital output high voltage for IO Type 7 | DVDIO = 1.8V | 0.9*DVDIO | - | - | V |
| DVOL7 | Digital output low voltage for IO Type 7 | DVDIO = 1.8V | - | - | 0.1*DVDIO | V |
| VIH7 | Digital input high voltage for IO Type 7 | DVDIO = 1.8V | 0.8*DVDIO | | DVDIO | |
| VIL7 | Digital input low voltage for IO Type 7 | DVDIO = 1.8V | 0 | | 0.2*DVDIO | |

### 6.2.3. Digitally controlled crystal oscillator (DCXO)

The Digitally Controlled Crystal Oscillator (DCXO) uses a two-pin 26MHz crystal resonator. Both crystals with 1612, 2016 and 3225 footprint are supported. See Table 6.2-7 for the crystal resonator capacitance load and tuning sensitivity range supported. On-chip programmable capacitor array is used for frequency-tuning, whereby the tuning range is ±50ppm. This DCXO supports 32kHz crystal-less operation.

***Table 6.2-7. DCXO Characteristics (TA = 250C, VDD = 1.8V unless otherwise stated)(1)***

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | Fref | | | 26 | | MHz |
| Crystal C load | CL | | 7 | 7.5 | | pF |
| Crystal tuning sensitivity | TS | | 10 | 33 | | ppm/pF |
| Static range | SR | CDAC from 0 to 511 | ± 40 | ± 50 | | ppm |
| Start-up time | TDCXO | Frequency error < 10ppm<br>Amplitude > 90 % | | 0.6 | 2.5 | ms |
| Pushing figure | | | | 0.2 | | ppm/V |
| Fref buffer output level | VFref | Max. loading = 10pF | | 1.1 | | $V_{p-p}$ |
| Fref buffer output phase noise | | 10kHz offset Jitter noise | | -135 | | dBc/Hz |

### 6.2.4. 32kHz crystal oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. It is designed to be a clock source of RTC for lower power platform. See Table 6.2-8 for the key performance.

The crystal parameters determine the oscillation allowance. Table 6.2-9 lists recommendations for the crystal parameters to be used well with XOSC32.

***Table 6.2-8. Functional specifications of XOSC32***

| Symbol | Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| VRTC | RTC module power | | 3.3 | | V |
| Tosc | Start-up time | | | 1 | sec |
| Dcyc | Duty cycle | 35 | 50 | | % |
| | Current consumption | | 1.8 | | µA |
| T | Operating temperature | -40 | | 85 | °C |

***Table 6.2-9. Recommended parameters for 32kHz crystal***

| Symbol | Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| F | Frequency range | | 32768 | | Hz |
| GL | Drive level | | | 0.5 | µW |
| Δf/f | Frequency tolerance | | +/- 20 | | ppm |
| ESR | Series resistance | | 50 | 90 | kΩ |

| Symbol | Parameter | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| C0 | Static capacitance | | 1.3 | | pF |
| CL1 | Load capacitance | | | 12.5 | pF |

Under such CL range and crystal, the –R is more than 3 times bigger. If larger CL is selected, the frequency accuracy will be decreased, and the –R will degrade, too.

## 6.3. Peripheral interfaces

### 6.3.1. SPI master interface characteristics

The operating characteristics of the SPI master controller at typical temperature (25°C) are shown in Figure 6.3-1, Figure 6.3-2, and Table 6.3-1. CPOL defines the clock polarity in the transmission. CPHA defines the legal timing to sample data.

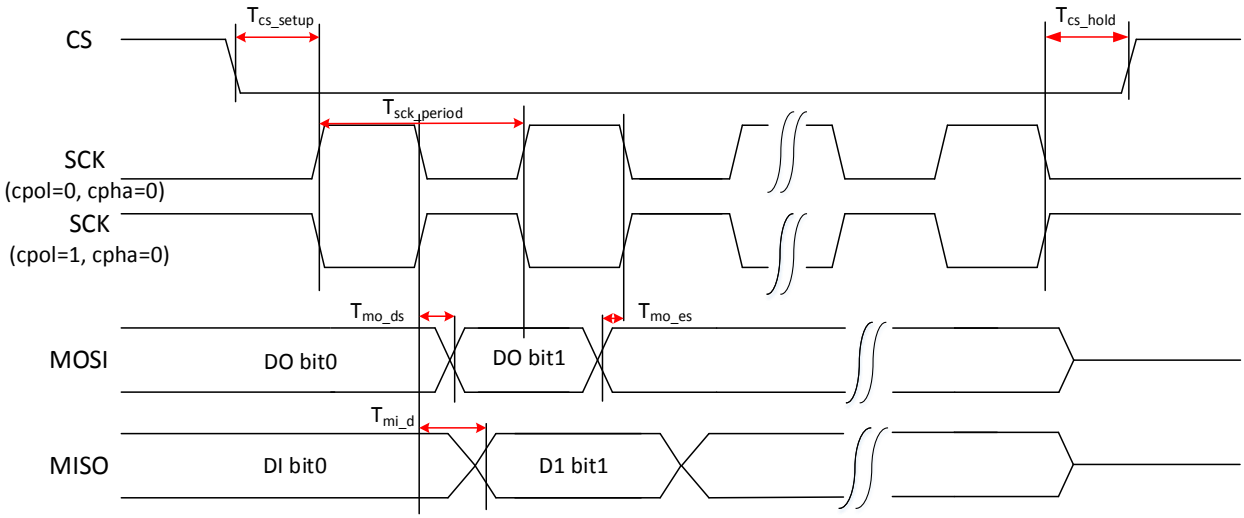



***Figure 6.3-1. SPI master interface timing diagram (CPHA=0)***

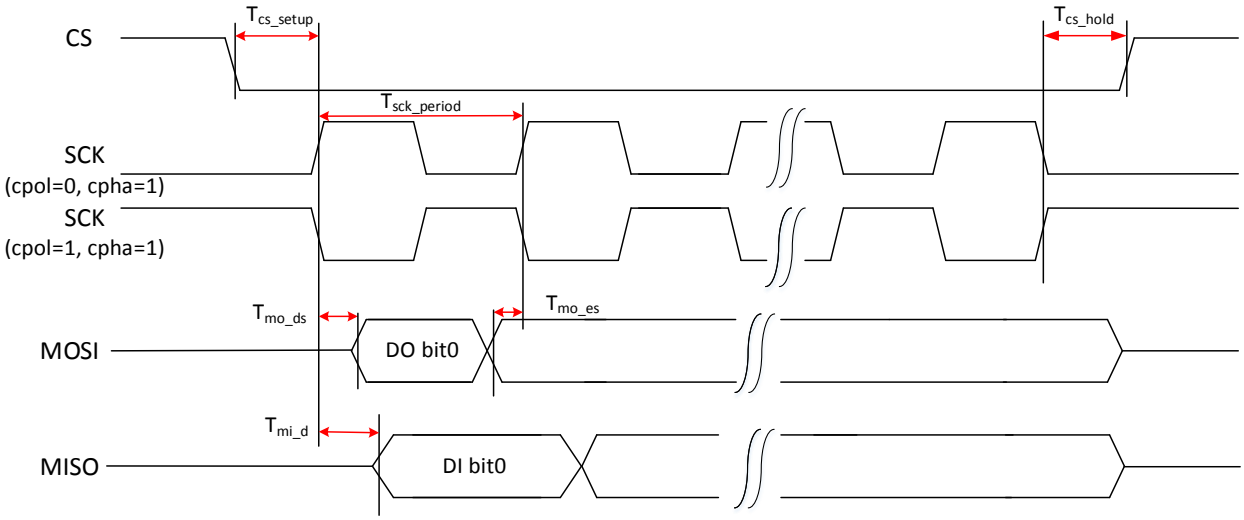



***Figure 6.3-2. SPI master interface timing diagram (CPHA=1)***

***Table 6.3-1. SPI master interface characteristics***

| Signal | Symbol | Parameter | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|---|
| CS | $T_{cs\_setup}$ | Chip select setup time | 9.615 | - | ns | |
| | $T_{cs\_hold}$ | Chip select hold time | 9.615 | - | ns | |
| SCK | $T_{sck\_period}$ | Serial clock period | 19.23 | - | ns | |
| MOSI | $T_{mo\_ds}$ | SPI master data output delay skew | - | 2 | ns | |
| | $T_{mo\_es}$ | SPI master data output early skew | - | 2 | ns | |
| MISO | $T_{mi\_d}$ | SPI master data input dalay | - | 30 | ns | received |

### 6.3.2. SPI slave interface characteristics

The operating characteristics of the SPI slave controller at typical temperature (25°C) are shown in Figure 6.3-3 and Table 6.3-2. CPOL defines the clock polarity in the transmission. CPHA defines the legal timing to sample data.

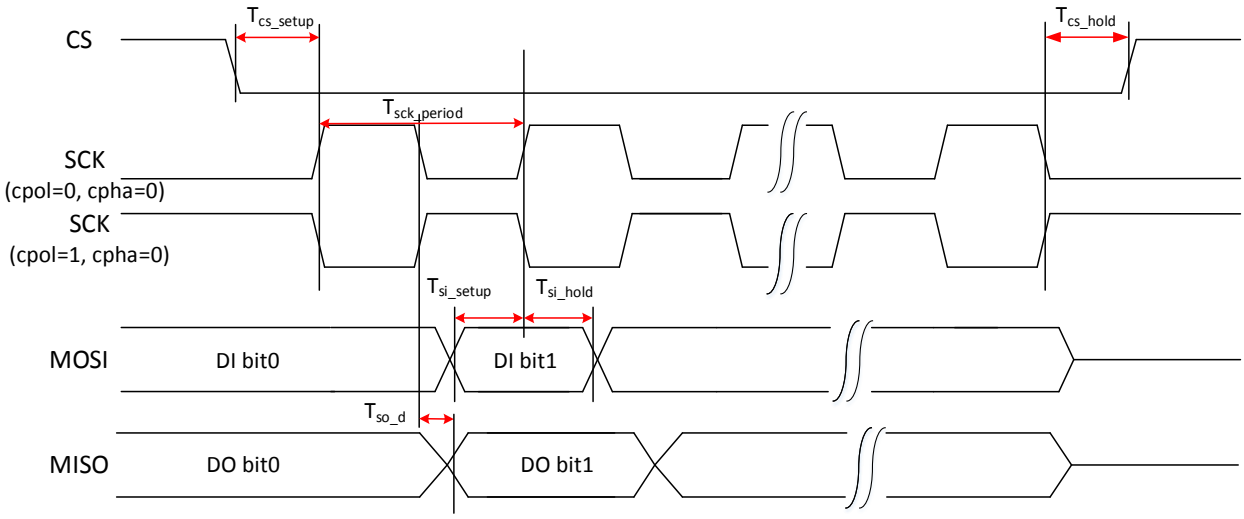



*Figure 6.3-3. SPI slave interface timing diagram (CPHA=0)*

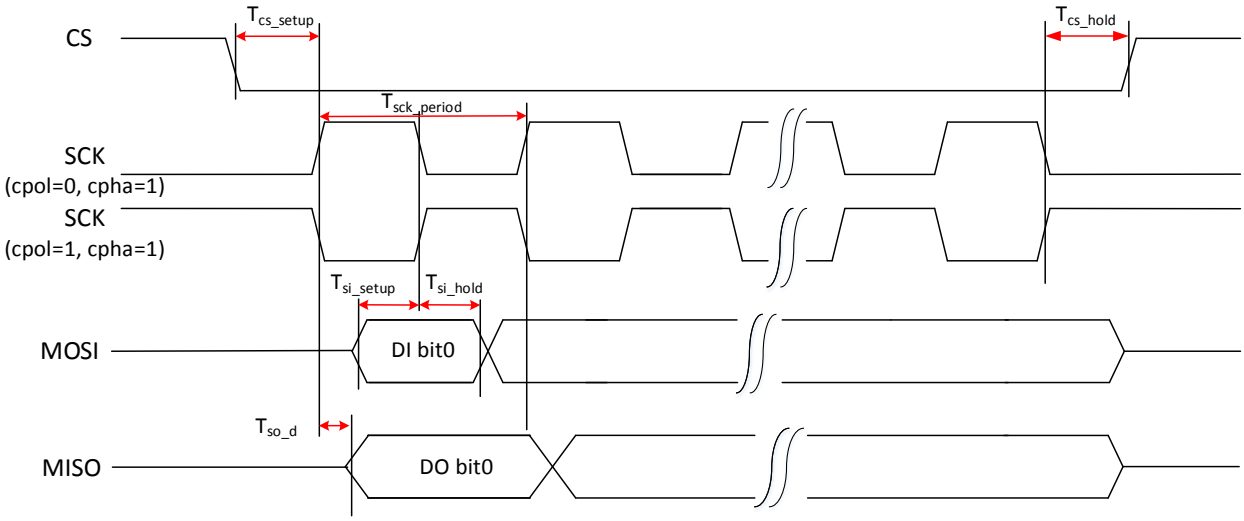



*Figure 6.3-4. SPI slave interface timing diagram (CPHA=1)*

*Table 6.3-2. SPI slave interface characteristics*

| Signal | Symbol | Parameter | Minimum | Maximum | Unit | Description |
|---|---|---|---|---|---|---|
| CS | $T_{cs\_setup}$ | Chip select setup time | 9.615 | – | ns | received |
| | $T_{cs\_hold}$ | Chip select hold time | 9.615 | – | ns | received |
| SCK | $T_{sck\_period}$ | Serial clock period | 19.23 | – | ns | received |
| MOSI | $T_{si\_setup}$ | SPI slave data input valid time | 4.8 | – | ns | received |
| | $T_{si\_hold}$ | SPI slave data input hold time | 4.8 | – | ns | received |

| Signal | Symbol | Parameter | Minimum | Maximum | Unit | Description |
|---|---|---|---|---|---|---|
| MISO | $T_{so\_d}$ | SPI slave data output delay | – | 30 | ns | |

### 6.3.3. I2S master and I2S slave interface characteristics

The operating characteristics of the I2S master and I2S slave controller at typical temperature (25°C) are shown in Figure 6.3-5 and Table 6.3-3.

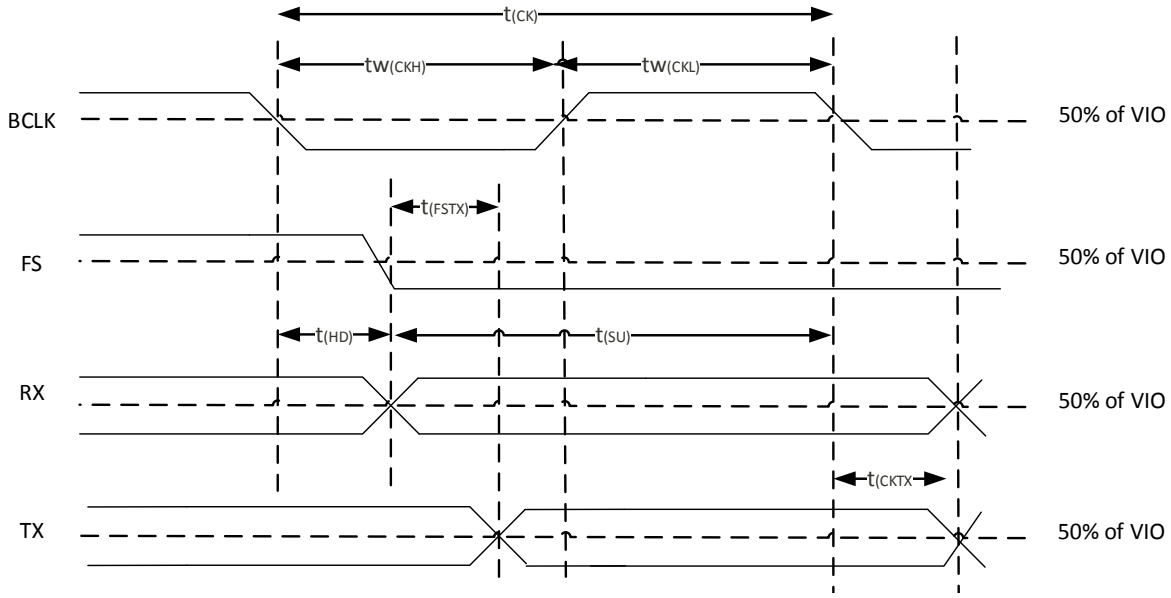



***Figure 6.3-5. I2S master and I2S slave interface timing diagram***

***Table 6.3-3. I2S master and I2S slave interface characteristics***

| Parameter | Symbol | MIN | MAX | Units |
|---|---|---|---|---|
| BCLK pulse cycle time | t(CK) | 1/(64fS) | | us |
| BCLK high pulse width | tw(CKH) | 0.35 | | % t(CK) |
| BCLK low pulse width | tw(CKL) | 0.35 | | % t(CK) |
| Data input setup time to BCLK | t(SU) | 15 | | ns |
| Data input hold time from BCLK | t(HD) | 0 | | ns |
| Data output delay from BCLK | t(CKTX) | 0 | 15 | ns |
| Data output delay from FS | t(FSTX) | 0 | 15 | ns |

### 6.3.4. SDIO2.0 Master interface characteristics

#### 6.3.4.1. DS mode

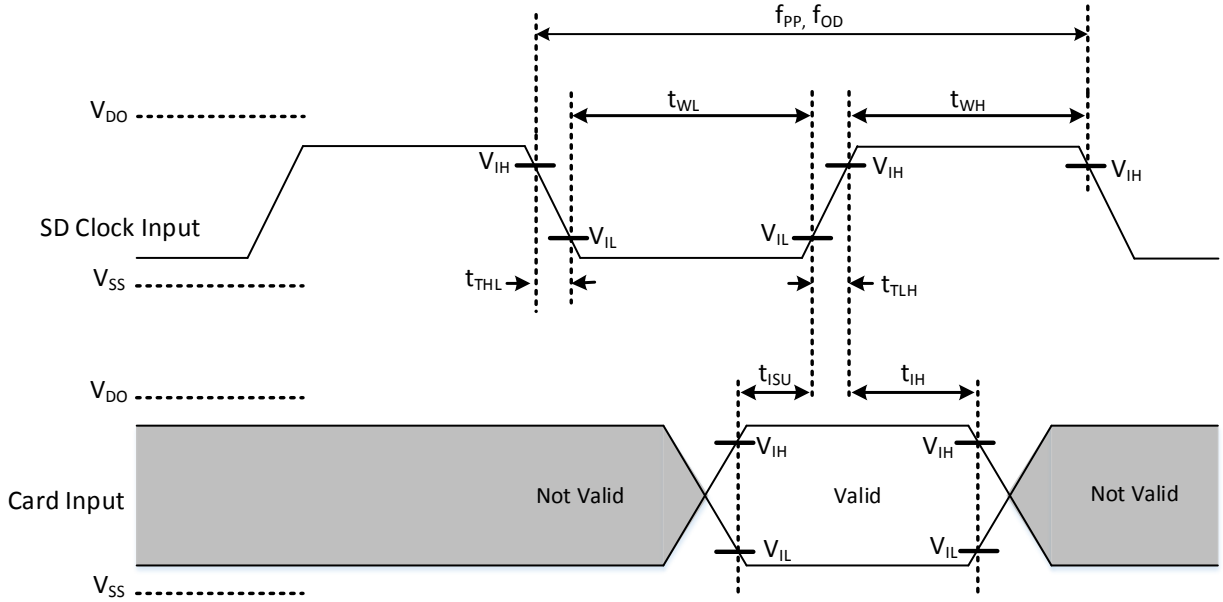



*Figure 6.3-6. Card Input Timing (Default Speed Mode)*

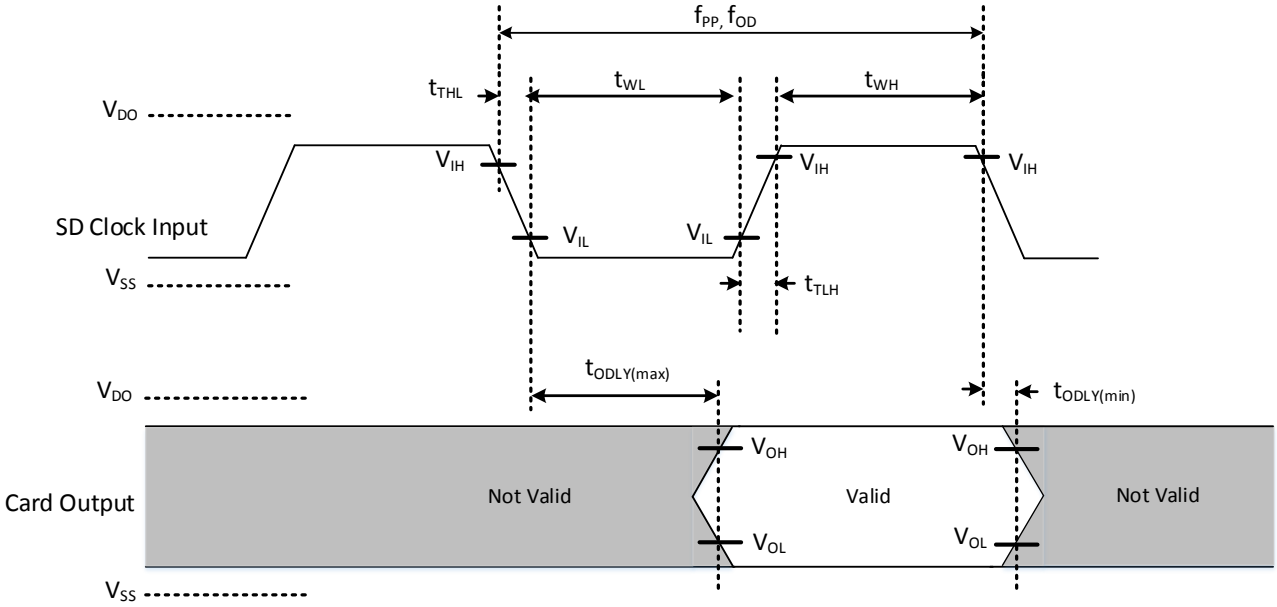



*Figure 6.3-7. Card Output Timing (Default Speed Mode)*

*Table 6.3-4. Bus Timing – Parameters Values (Default Speed)*

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage | VDO | 2.7 | 3.6 | V | |

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Output high voltage | VOH | 0.75*VDO | | V | IOH = -2mA VDO_min |
| Output low voltage | VOL | | 0.125*VDO | V | IOL = 2mA VDO_min |
| Input high voltage | VIH | 0.625*VDO | VDO+0.3 | V | |
| Input low voltage | VIL | VSS-0.3 | 0.25*VDO | V | |
| Power up time | | | 250 | ms | From 0V to VDO_min |
| **Clock CLK(All values are referred to min(VIH) and max(VIL))** | | | | | |
| Clock frequency Data Transfer Mode | fPP | 0 | 25 | MHz | CCARD ≤ 10 pF (1 card) |
| Clock frequency Identification Mode | fOD | 0(1)/100 | 400 | kHz | CCARD ≤ 10 pF (1 card) |
| Clock low time | tWL | 10 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock high time | tWH | 10 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock rise time | tTLH | | 10 | ns | CCARD ≤ 10 pF (1 card) |
| Clock fall time | tTHL | | 10 | ns | CCARD ≤ 10 pF (1 card) |
| **Input CMD,DAT (referenced to CLK)** | | | | | |
| Input setup time | tISU | 5 | | ns | CCARD ≤ 10 pF (1 card) |
| Input hold time | tIH | 5 | | ns | CCARD ≤ 10 pF (1 card) |
| **Output CMD,DAT (referenced to CLK)** | | | | | |
| Output Delay time during Data Transfer Mode | tODLY | 0 | 14 | ns | CL ≤ 40 pF (1 card) |
| Output Delay time during Identification Mode | tODLY | 0 | 50 | ns | CL ≤ 40 pF (1 card) |
| Total system capacitance for each line | $C_L$ | | 40 | pF | 1 card |

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

### 6.3.4.2. HS mode

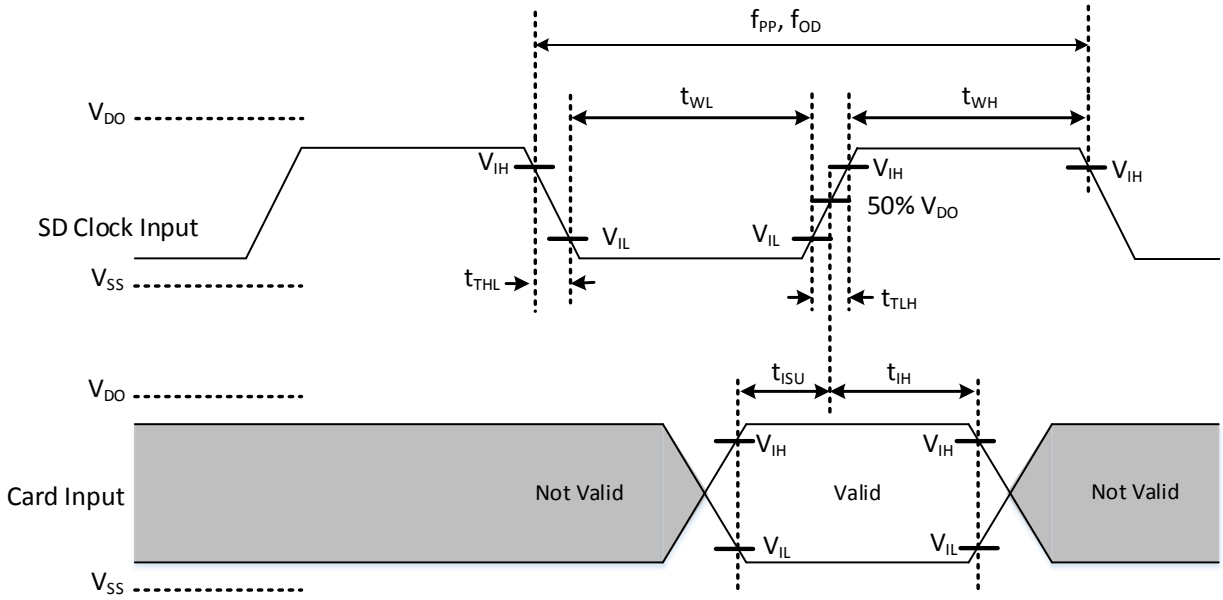



*Figure 6.3-8. Card Input Timing (High Speed Mode)*

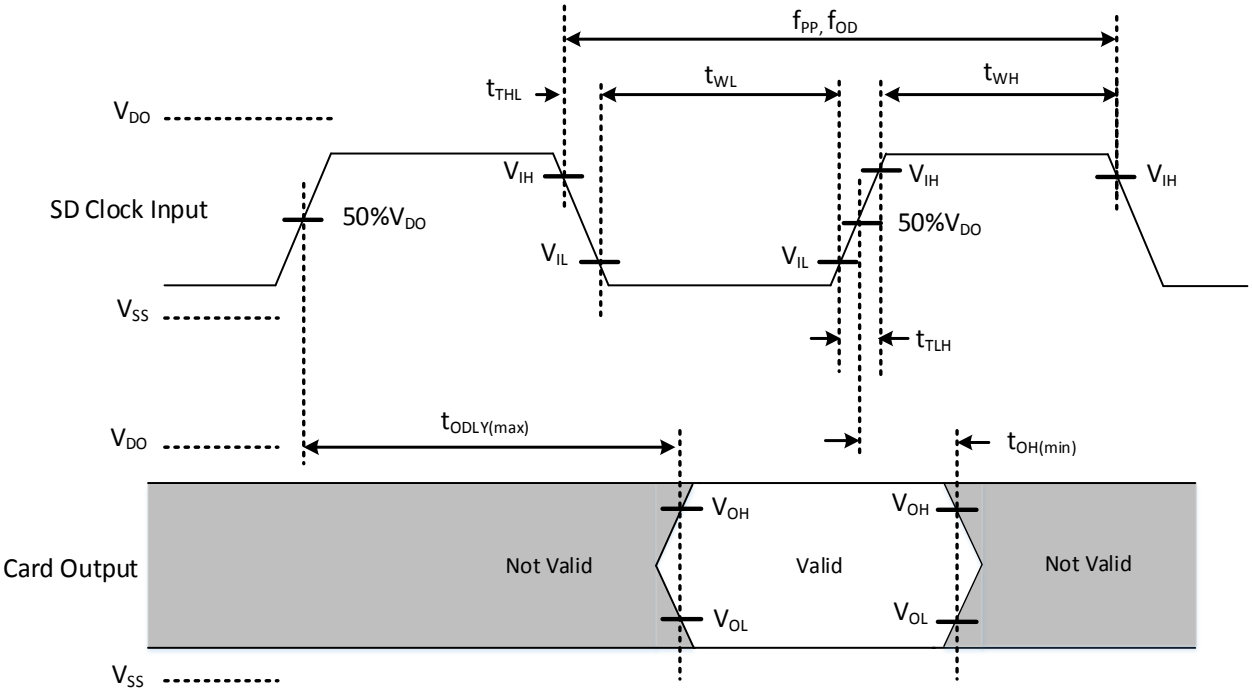



*Figure 6.3-9. Card Output Timing (High Speed Mode)*

*Table 6.3-5. Bus Timing – Parameters Values (High Speed)*

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage | VDO | 2.7 | 3.6 | V | |

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Output high voltage | VOH | 0.75*VDO | | V | IOH = -2mA VDO_min |
| Output low voltage | VOL | | 0.125*VDO | V | IOL = 2mA VDO_min |
| Input high voltage | VIH | 0.625*VDO | VDO+0.3 | V | |
| Input low voltage | VIL | VSS-0.3 | 0.25*VDO | V | |
| Power up time | | | 250 | ms | From 0V to VDO_min |
| **Clock CLK(All values are referred to min(VIH) and max(VIL))** | | | | | |
| Clock frequency Data Transfer Mode | fPP | 0 | 50 | MHz | CCARD ≤ 10 pF (1 card) |
| Clock low time | tWL | 7 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock high time | tWH | 7 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock rise time | tTLH | | 3 | ns | CCARD ≤ 10 pF (1 card) |
| Clock fall time | tTHL | | 3 | ns | CCARD ≤ 10 pF (1 card) |
| **Input CMD,DAT (referenced to CLK)** | | | | | |
| Input setup time | tISU | 6 | | ns | CCARD ≤ 10 pF (1 card) |
| Input hold time | tIH | 2 | | ns | CCARD ≤ 10 pF (1 card) |
| **Output CMD,DAT (referenced to CLK)** | | | | | |
| Output Delay time during Data Transfer Mode | tODLY | | 14 | ns | CL ≤ 40 pF (1 card) |
| Output Hold time | tOH | 2.5 | | ns | CL ≥ 15 pF (1 card) |
| Total system capacitance for each line | $C_L$ | | 40 | pF | 1 card |

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

### 6.3.5. SDIO2.0 Slave interface characteristics

#### 6.3.5.1. DS mode

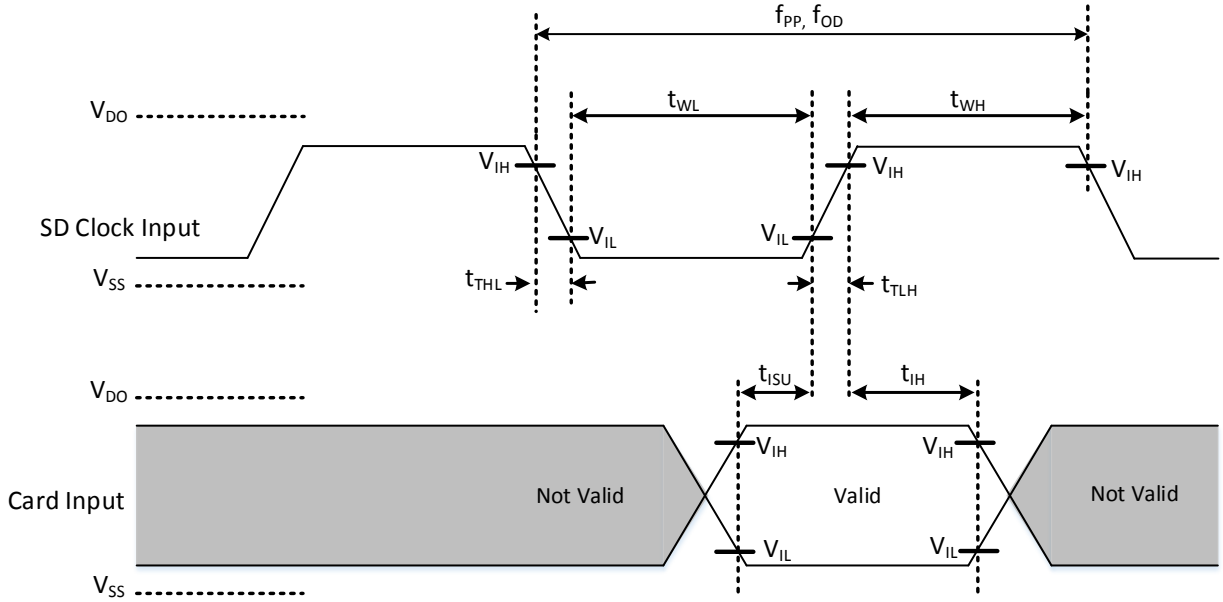



*Figure 6.3-10. Card Input Timing (Default Speed Mode)*

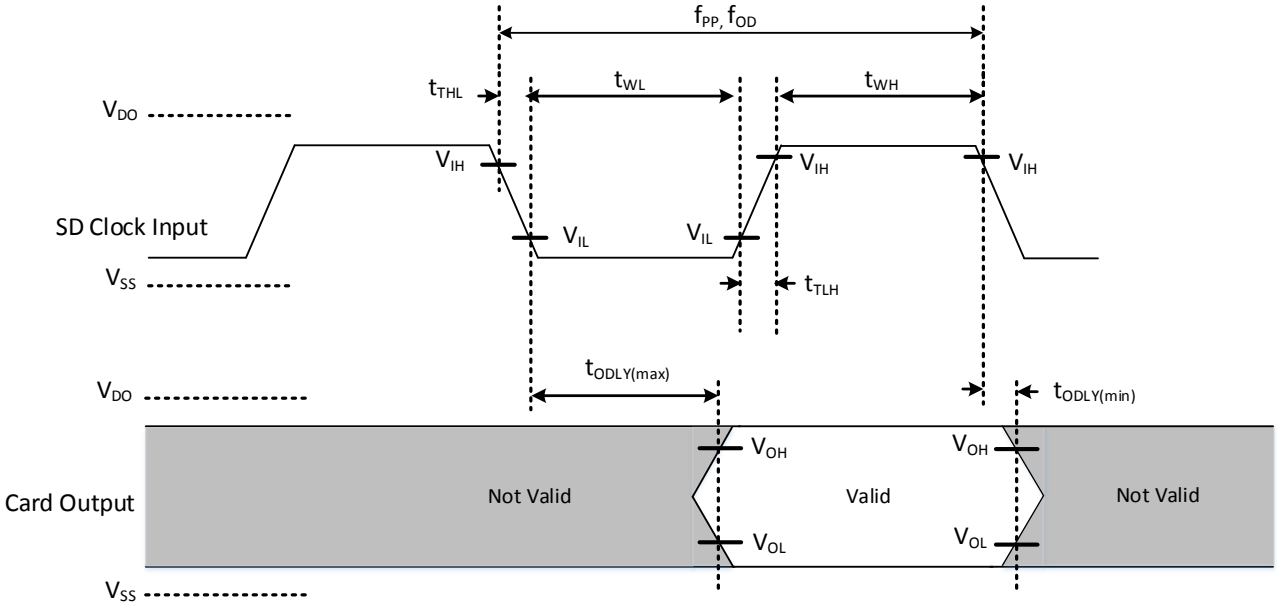



*Figure 6.3-11. Card Output Timing (Default Speed Mode)*

*Table 6.3-6. Bus Timing – Parameters Values (Default Speed)*

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage | VDO | 2.7 | 3.6 | V | |

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Output high voltage | VOH | 0.75*VDO | | V | IOH = -2mA VDO_min |
| Output low voltage | VOL | | 0.125*VDO | V | IOL = 2mA VDO_min |
| Input high voltage | VIH | 0.625*VDO | VDO+0.3 | V | |
| Input low voltage | VIL | VSS-0.3 | 0.25*VDO | V | |
| Power up time | | | 250 | ms | From 0V to VDO_min |
| **Clock CLK(All values are referred to min(VIH) and max(VIL))** | | | | | |
| Clock frequency Data Transfer Mode | fPP | 0 | 25/20(2) | MHz | CCARD ≤ 10 pF (1 card) |
| Clock frequency Identification Mode | fOD | 0(1)/100 | 400 | kHz | CCARD ≤ 10 pF (1 card) |
| Clock low time | tWL | 10 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock high time | tWH | 10 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock rise time | tTLH | | 10 | ns | CCARD ≤ 10 pF (1 card) |
| Clock fall time | tTHL | | 10 | ns | CCARD ≤ 10 pF (1 card) |
| **Input CMD,DAT (referenced to CLK)** | | | | | |
| Input setup time | tISU | 5 | | ns | CCARD ≤ 10 pF (1 card) |
| Input hold time | tIH | 5 | | ns | CCARD ≤ 10 pF (1 card) |
| **Output CMD,DAT (referenced to CLK)** | | | | | |
| Output Delay time during Data Transfer Mode | tODLY | 0 | 14/19(2) | ns | CL ≤ 40 pF (1 card) |
| Output Delay time during Identification Mode | tODLY | 0 | 50 | ns | CL ≤ 40 pF (1 card) |
| Total system capacitance for each line | $C_L$ | | 40 | pF | 1 card |

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

(2) In the case of 0.9v, the timing can't fully meet the SDIO2.0 SPEC.

### 6.3.5.2. HS mode

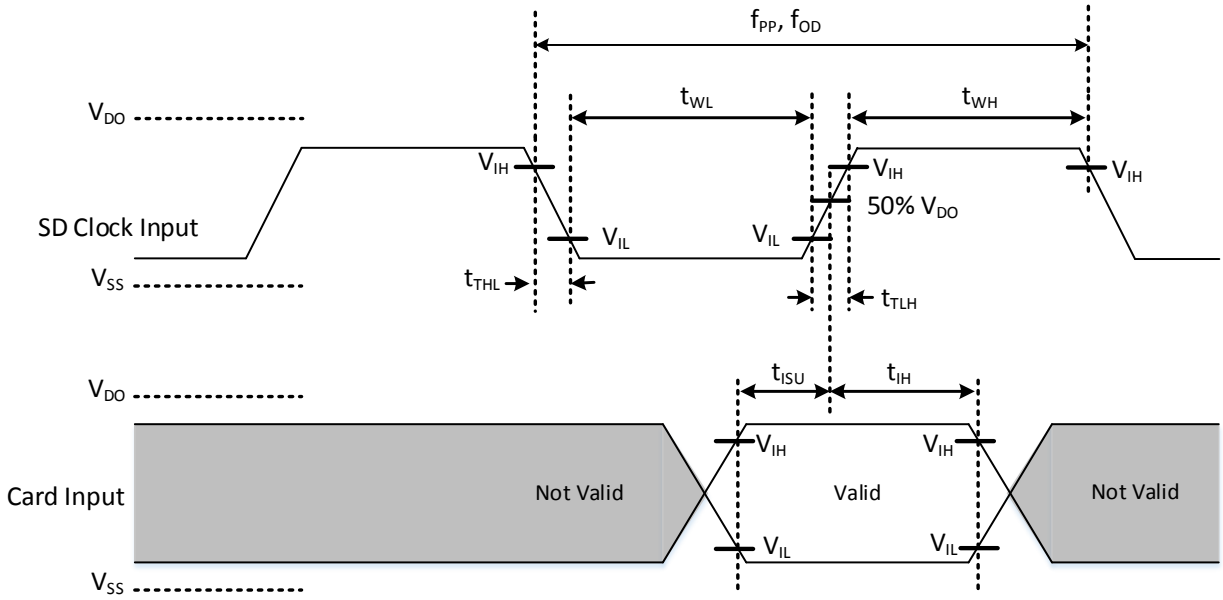



*Figure 6.3-12. Card Input Timing (High Speed Mode)*

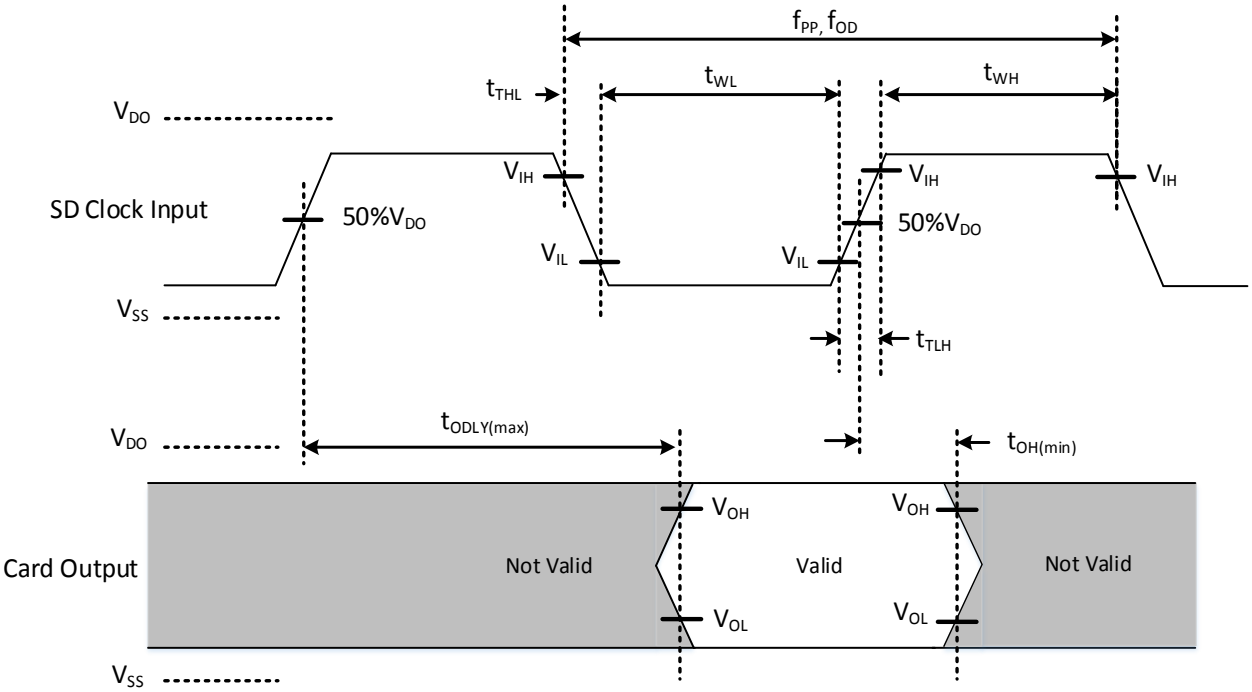



*Figure 6.3-13. Card Output Timing (High Speed Mode)*

*Table 6.3-7. Bus Timing – Parameters Values (High Speed)*

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Supply voltage | VDO | 2.7 | 3.6 | V | |

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Output high voltage | VOH | 0.75*VDO | | V | IOH = -2mA VDO_min |
| Output low voltage | VOL | | 0.125*VDO | V | IOL = 2mA VDO_min |
| Input high voltage | VIH | 0.625*VDO | VDO+0.3 | V | |
| Input low voltage | VIL | VSS-0.3 | 0.25*VDO | V | |
| Power up time | | | 250 | ms | From 0V to VDO_min |
| **Clock CLK(All values are referred to min(VIH) and max(VIL))** | | | | | |
| Clock frequency Data Transfer Mode | fPP | 0 | 50/40(2) | MHz | CCARD ≤ 10 pF (1 card) |
| Clock low time | tWL | 7 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock high time | tWH | 7 | | ns | CCARD ≤ 10 pF (1 card) |
| Clock rise time | tTLH | | 3 | ns | CCARD ≤ 10 pF (1 card) |
| Clock fall time | tTHL | | 3 | ns | CCARD ≤ 10 pF (1 card) |
| **Input CMD,DAT (referenced to CLK)** | | | | | |
| Input setup time | tISU | 6 | | ns | CCARD ≤ 10 pF (1 card) |
| Input hold time | tIH | 2 | | ns | CCARD ≤ 10 pF (1 card) |
| **Output CMD,DAT (referenced to CLK)** | | | | | |
| Output Delay time during Data Transfer Mode | tODLY | | 14/19(2) | ns | CL ≤ 40 pF (1 card) |
| Output Hold time | tOH | 2.5 | | ns | CL ≥ 15 pF (1 card) |
| Total system capacitance for each line | $C_L$ | | 40 | pF | 1 card |

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

(2) In the case of 0.9v, the timing can't fully meet the SDIO2.0 SPEC .

### 6.3.6. USB11 interface characteristics

The USB uses a differential output driver to drive the USB data signal on the USB cable. The static output swing of the driver in its low state must be below VOL (max) of 0.3V with a 1.5kΩ load to 3.6V and in its high state must be above the VOH (min) of 2.8V with a 15kΩ load to ground.

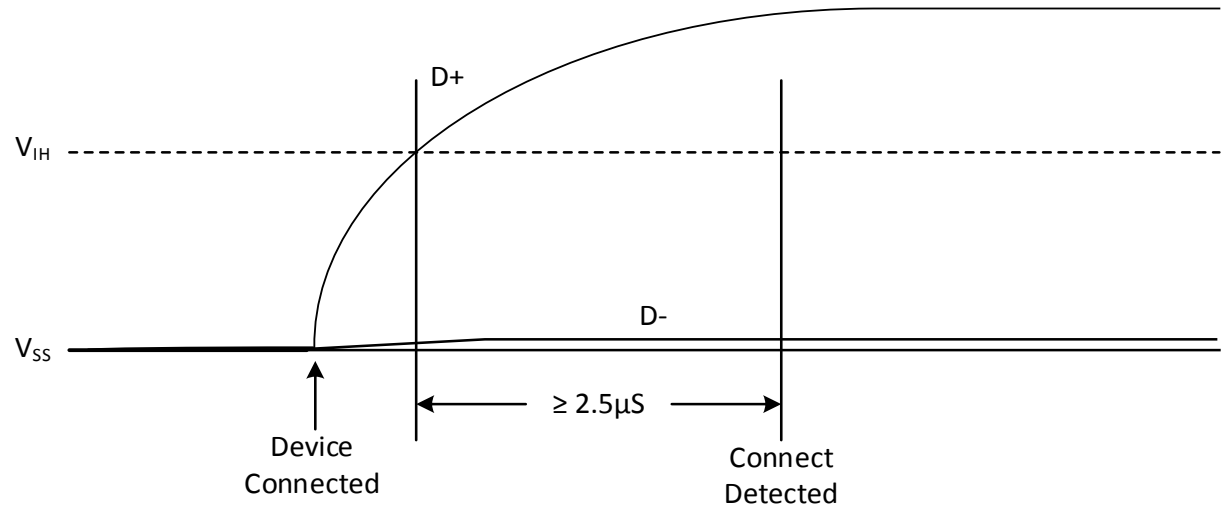



*Figure 6.3-14. Full-speed Device Connect Detection*

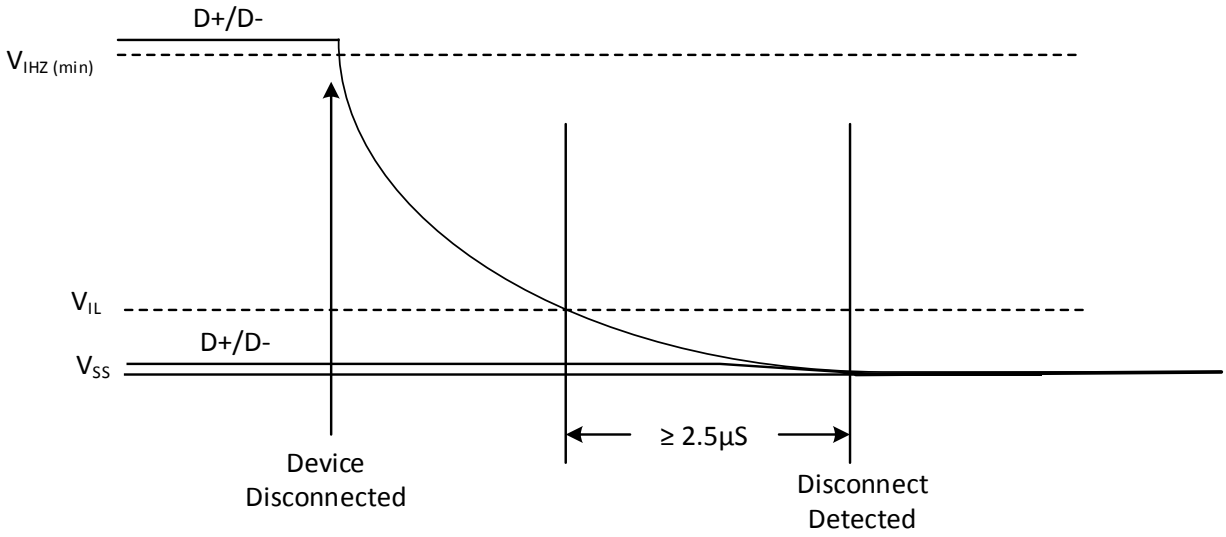



*Figure 6.3-15. Disconnect Detection*

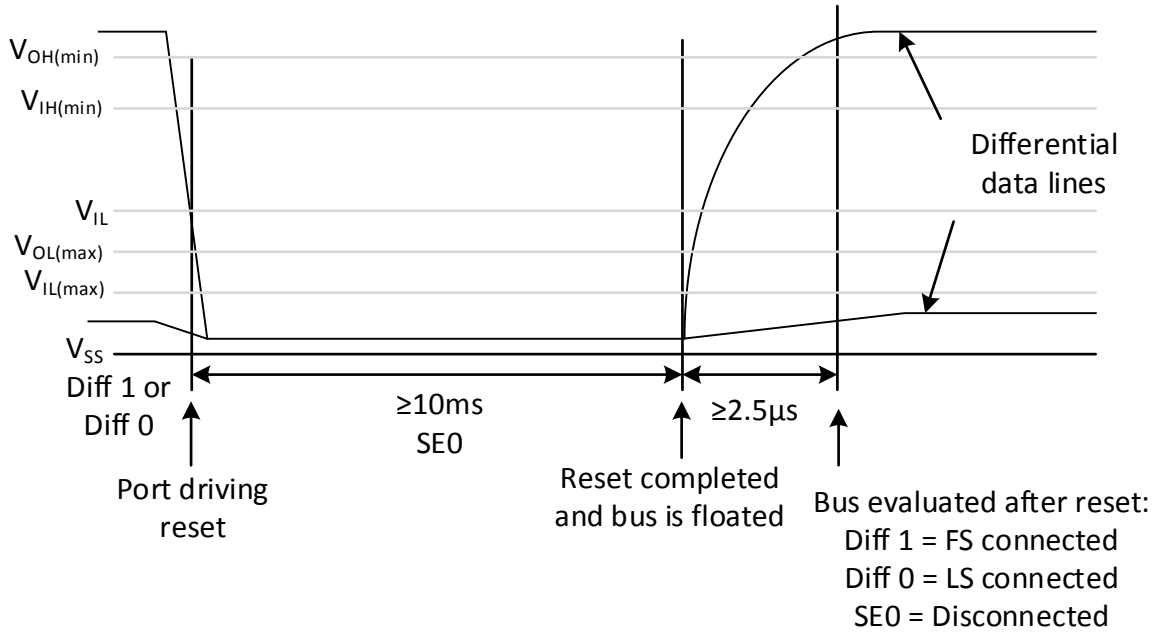



*Figure 6.3-16. Bus State Evaluation after reset*

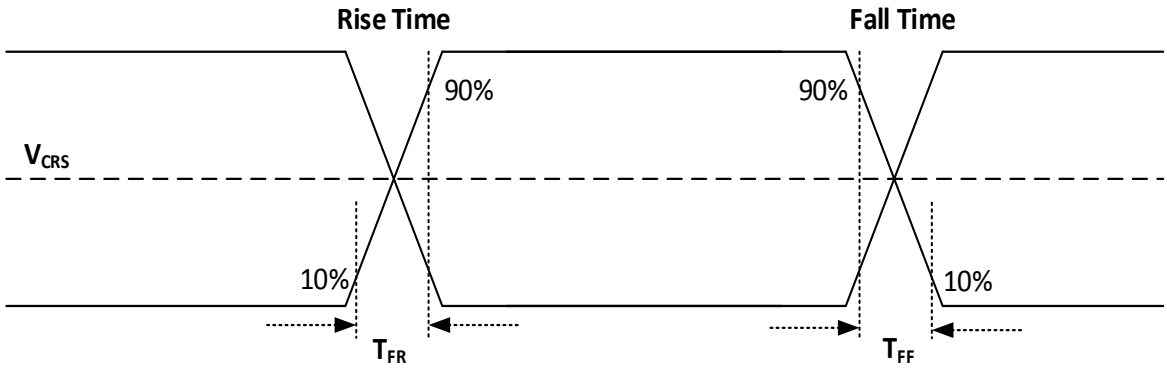



*Figure 6.3-17. Bus driver characteristics*

*Table 6.3-8. USB11 interface characteristics*

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| **Input levels for Full-Speed** | | | | |
| Differential Input Sensitivity | VDI | 0.2 | - | V |
| Differential Common Mode Range | VCM | 0.8 | 2.5 | V |
| **Output levels for Full-Speed** | | | | |
| Low | VOL | 0.0 | 0.3 | V |
| High | VOH | 2.8 | 3.6 | V |
| **Full-Speed Driver Characteristics** | | | | |

| | | | | |
|---|---|---|---|---|
| Rise Time | TFR | 4 | 20 | ns |
| Fall Time | TFF | 4 | 20 | ns |
| Output Signal Crossover Voltage | VCRS | 1.3 | 2.0 | V |
| **Terminations** | | | | |
| Pull-up Resistor | Rpu | 0.9 | 1.575 | k |
| Pull-down Resistor | Rpd | 14.25 | 24.8 | k |

### 6.3.7. eMMC interface characteristics

The I/O operating voltage characteristics of the eMMC controller at typical temperature (25°C) is shown in Table 6.3-9 and Table 6.3-10.

***Table 6.3-9. eMMC interface push-pull signal level----2.7V – 3.6V $V_{CCQ}$ range (high voltage eMMC)***

| Parameter | Symbol | Minimum | Maximum | Unit | Description |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | 0.75*$V_{CCQ}$ | | V | $I_{OH}$= -100µA at $V_{CCQ}$ min |
| Output Low Voltage | $V_{OL}$ | | 0.125*$V_{CCQ}$ | V | $I_{OL}$= 100µA at $V_{CCQ}$ min |
| Input High Voltage | $V_{IH}$ | 0.625*$V_{CCQ}$ | $V_{CCQ}$+0.3 | V | |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$-0.3 | 0.25*$V_{CCQ}$ | V | |

***Table 6.3-10. eMMC interface push-pull signal level----1.70V – 1.95V $V_{CCQ}$ voltage range***

| Parameter | Symbol | Minimum | Maximum | Unit | Description |
|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $V_{CCQ}$ -0.45V | – | V | $I_{OH}$= -2mA |
| Output Low Voltage | $V_{OL}$ | – | 0.45V | V | $I_{OL}$= 2mA |
| Input High Voltage | $V_{IH}$ | 0.65*$V_{CCQ}$ (1) | $V_{CCQ}$+0.3 | V | |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$-0.3 | 0.35*$V_{CCQ}$(2) | V | |

(1)0.7*$V_{DD}$ for MMC4.3 and older revisions

(2)0.3*$V_{DD}$ for MMC4.3 and older revisions

The eMMC bus timing is shown in Figure 6.3-18, Table 6.3-11 and Table 6.3-12.

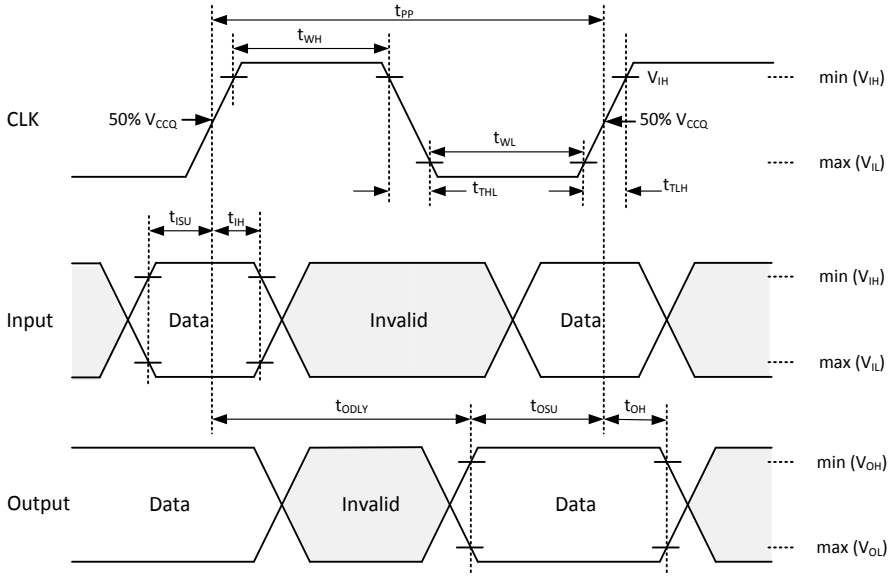



***Figure 6.3-18. eMMC interface timing diagram***

***Table 6.3-11. eMMC interface characteristics (backward-compatible device)***

| Parameter | Symbol | Minimum | Maximum | Unit | Description [1] |
|---|---|---|---|---|---|
| **Clock CLK[2]** | | | | | |
| Clock frequency data transfer Mode (PP)[3] | $f_{pp}$ | 0 | 26 | MHz | CL≦30pF |
| Clock frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | |
| Clock low time | $t_{WL}$ | 10 | – | ns | CL≦30pF |
| Clock high time | $t_{WH}$ | 10 | – | ns | CL≦30pF |
| Clock rise time[4] | $t_{TLH}$ | – | 10 | ns | CL≦30pF |
| Clock fall time | $t_{THL}$ | – | 10 | ns | CL≦30pF |
| **Inputs CMD, DAT (referenced to CLK)** | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | – | ns | CL≦30pF |
| Input hold time | $t_{IH}$ | 3 | – | ns | CL≦30pF |
| **Outputs CMD, DAT (referenced to CLK)** | | | | | |
| Output set-up time[5] | $t_{OSU}$ | 11.7 | – | ns | CL≦30pF |
| Output hold time[5] | $t_{OH}$ | 8.3 | – | ns | CL≦30pF |

[1]The device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

[2]CLK timing is measured at 50% of $V_{CCQ}$

[3]For compatibility with devices that support the v4.2 standard or earlier, host should not use frequency greater than 26MHz before switching to high-speed interface timing.

[4]CLK rise and fall times are measured by min($V_{IH}$) and max($V_{IL}$)

(5)$t_{OSU}$ and $t_{OH}$ are defined as values from clock rising edge. However, there may be devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set $t_{WL}$ values as long as possible within the range which will not go over $t_{CK}$-$t_{OH(min)}$ in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between $t_{WL}$ and $t_{OSU}$ or between $t_{CK}$ and $t_{OSU}$ for the device in its own datasheet as a note or an application notes.

***Table 6.3-12. eMMC interface characteristics (high-speed device)***

| Parameter | Symbol | Min. | Max. | Unit | Description |
|---|---|---|---|---|---|
| **Clock CLK(1)** | | | | | |
| Clock frequency Data Transfer Mode (PP)(2) | $f_{pp}$ | 0 | 52(3) | MHz | $C_L \leqq 30pF$<br>Tolerance:+100kHz |
| Clock frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | Tolerance:+20kHz |
| Clock low time | $t_{WL}$ | 6.5 | – | ns | $C_L \leqq 30pF$ |
| Clock high time | $t_{WH}$ | 6.5 | – | ns | $C_L \leqq 30pF$ |
| Clock rise time(4) | $t_{TLH}$ | – | 3 | ns | $C_L \leqq 30pF$ |
| Clock fall time | $t_{THL}$ | – | 3 | ns | $C_L \leqq 30pF$ |
| **Inputs CMD, DAT (referenced to CLK)** | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | – | ns | $C_L \leqq 30pF$ |
| Input hold time | $t_{IH}$ | 3 | – | ns | $C_L \leqq 30pF$ |
| **Outputs CMD, DAT (referenced to CLK)** | | | | | |
| Output delay time during data transfer | $t_{ODLY}$ | – | 13.7 | ns | $C_L \leqq 30pF$ |
| Output hold time | $t_{OH}$ | 2.5 | – | ns | $C_L \leqq 30pF$ |
| Signal rise time(5) | $T_{RISE}$ | – | 3 | ns | $C_L \leqq 30pF$ |
| Signal fall time | $T_{FALL}$ | – | 3 | ns | $C_L \leqq 30pF$ |

(1)CLK timing is measured at 50% of $V_{CCQ}$

(2)An eMMC shall support the full frequency range from 0MHz – 26MHz, or 0MHz – 52MHz

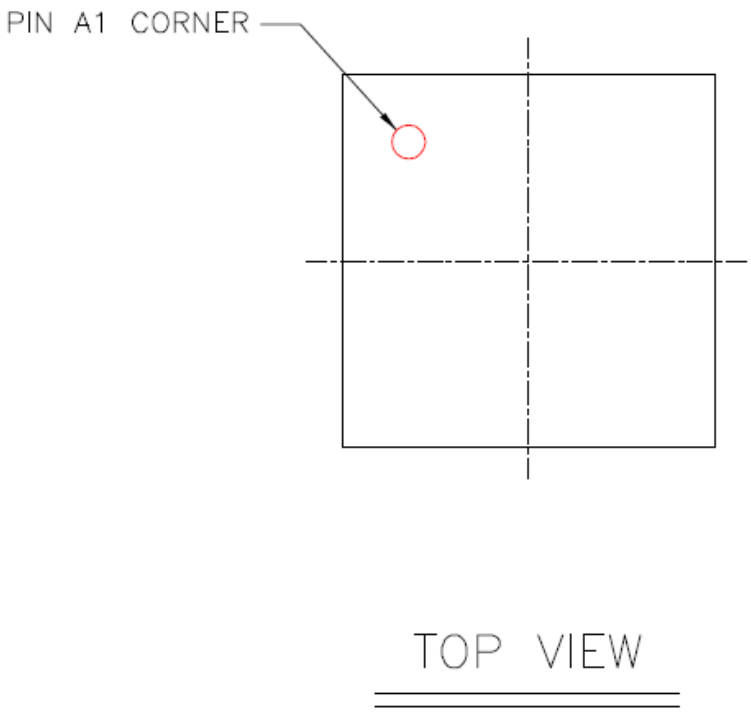
(3)Devices can operate as high-speed device interface timing at 26MHz clock frequency.

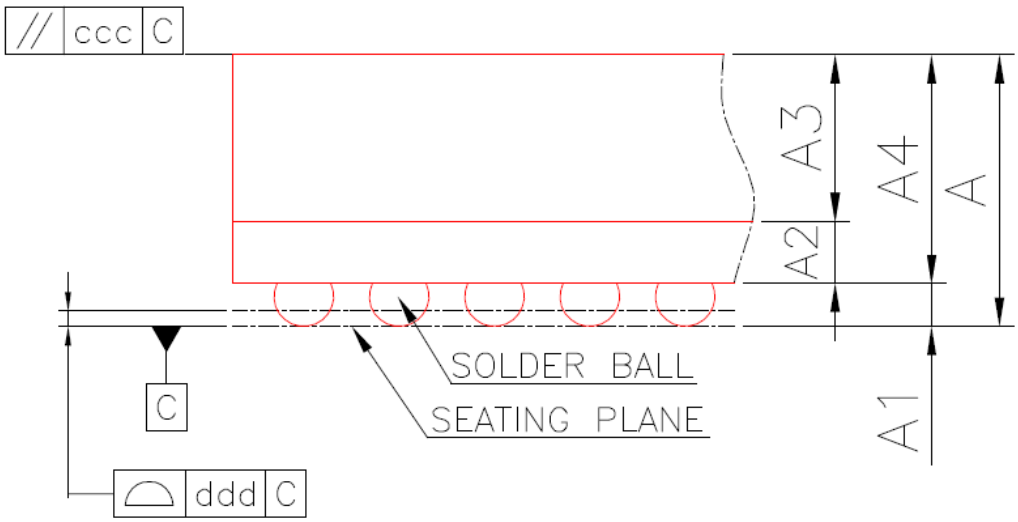
(4)CLK rise and fall times are measured by min($V_{IH}$) and max($V_{IL}$).

(5)Inputs CMD, DAT rise and fall times are measured by min($V_{IH}$) and max($V_{IL}$), and outputs CMD, DAT rise and fall times are measured by min($V_{OH}$) and max($V_{OL}$).

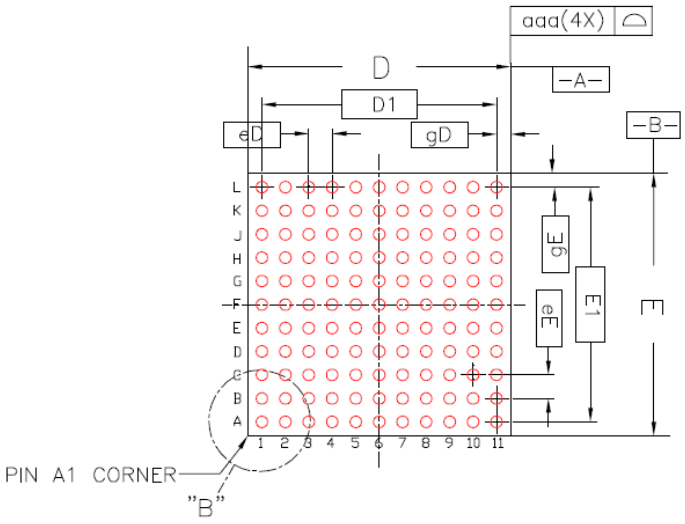
# 7. Package Information

## 7.1. MT2625 mechanical data of the package






DETAIL : "A"




BOTTOM VIEW

| Item | | Symbol | Common Dimensions | | |
|---|---|---|---|---|---|
| | | | MIN. | NOM. | MAX. |
| Package Type | | | TFBGA | | |
| Body Size | X | D | 5.50 | 5.60 | 5.70 |
| | Y | E | 5.50 | 5.60 | 5.70 |
| Ball Pitch | X | eD | | 0.50 | |
| | Y | eE | | 0.50 | |
| Mold Thickness | | A3 | | 0.70 Ref. | |
| Substrate Thickness | | A2 | | 0.13 Ref. | |
| Substrate+Mold Thickness | | A4 | 0.78 | 0.83 | 0.88 |
| Total Thickness | | A | – | – | 1.05 |
| Ball Diameter | | | | 0.25 | |
| Ball Stand Off | | A1 | 0.11 | 0.15 | 0.19 |
| Ball Width | | b | 0.22 | 0.27 | 0.32 |
| Package Edge Tolerance | | aaa | | 0.05 | |
| Mold Flatness | | ccc | | 0.10 | |
| Coplanarity | | ddd | | 0.08 | |
| Ball Offset (Package) | | eee | | 0.15 | |
| Ball Offset (Ball) | | fff | | 0.05 | |
| Ball Count | | n | | 121 | |
| Edge Ball Center to Center | X | D1 | | 5.00 | |
| | Y | E1 | | 5.00 | |
| Edge Ball Center to Package Edge | X | gD | | 0.30 | |
| | Y | gE | | 0.30 | |

***Figure 7.1-1. Outlines and dimensions of MT2625 TFBGA 5.6 mm*5.6 mm, 121-ball, 0.5mm pitch package***

## 7.2. MT2625 thermal operating specifications

***Table 7.2-1. MT2625 thermal operating specifications***

| Description | Value | Unit |
|---|---|---|
| Thermal resistance from device junction to package case (Theta-Jc) | 25.23 | C/W |
| Thermal resistance from junction to ambient (Theta-Ja) | 96.16 | C/W |
| Maximum package temperature | 125 | °C |
| Maximum power dissipation | 0.52 | W |

## 7.3. MT2625 lead-free packaging

The MT2625 platform is provided in a lead-free package and meets RoHS requirements.

# 8. Ordering Information

## 8.1. MT2625 top marking definition


Line 1 : MEDIATEK LOGO

Line 2 : ARM LOGO

Line 3 : Part Number

Line 4 : Date Code

Line 5 : Die 1 Lot no.

Line 6 : Die 2 Lot no.

Line 7 : Die 3 Lot no.

***Figure 8.1-1. Mass production top marking of MT2625DA***


Line 1 : MEDIATEK LOGO

Line 2 : ARM LOGO

Line 3 : Part Number

Line 4 : Date Code

Line 5 : Die 1 Lot no.

Line 6 : Die 2 Lot no.

***Figure 8.1-2. Mass production top marking of MT2625AA***


Line 1 : MEDIATEK LOGO

Line 2 : ARM LOGO

Line 3 : Part Number

Line 4 : Date Code

Line 5 : Die 1 Lot no.

Line 6 : Die 2 Lot no.

***Figure 8.1-3. Mass production top marking of MT2625DPA***


Line 1 : MEDIATEK LOGO

Line 2 : ARM LOGO

Line 3 : Part Number

Line 4 : Date Code

Line 5 : Die 1 Lot no.

Line 6 : Die 2 Lot no.

***Figure 8.1-4. Mass production top marking of MT2625APA***

***Table 8.1-1. Ordering information***

| Product number | Package | Description |
|---|---|---|
| MT2625DA | TFBGA | 5.6mm*5.6mm, 121-ball, 0.5mm pitch Package |
| MT2625AA | TFBGA | 5.6mm*5.6mm, 121-ball, 0.5mm pitch Package |
| MT2625DPA | TFBGA | 5.6mm*5.6mm, 121-ball, 0.5mm pitch Package |
| MT2625APA | TFBGA | 5.6mm*5.6mm, 121-ball, 0.5mm pitch Package |