MT2625 Reference Manual

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Table of Contents

Lists of Tables and Figures vi
1. Documentation General Conventions 1
1.1. Abbreviations for control modules 1
1.2. Abbreviations for registers 1
2. Bus Architecture 3
2.1. Abbreviations 3
2.2. System architecture 3
3. Cortex-M4 L1 Cache Controller 5
3.1. Overview 5
3.2. Cache optimization 7
3.3. Register mapping 12
3.4. Cacheable region controller 18
3.5. Remapping 21
4. CMSYS 25
4.1. Overview 25
4.2. Block diagram 25
4.3. Register mapping 25
5. Direct Memory Access 32
5.1. Overview 32
5.2. Abbreviations 32
5.3. Features 32
5.4. Functions 33
5.5. Application and programming sequence 35
5.6. Register mapping 37
6. External Interrupt Controller (EINT) 71
6.1. Overview 71
6.2. Abbreviations 71
6.3. Features 71
6.4. Block diagram 71
6.5. Wakeup event management 72
6.6. Functions 72
6.7. Programming guide 74
6.8. External interrupt or event line mapping 74
6.9. Register mapping 76
7. General Purpose Inputs/Outputs 88
7.1. Overview 88
7.2. Features 88
7.3. Block diagram 88
7.4. Functions 88
7.5. Register mapping 92
8. Inter-Integrated Circuit Controller 202
8.1. Overview 202
8.2. Abbreviations 202
8.3. Features 202
8.4. Block diagram 202
8.5. Functions 203

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8.6. Programming guide 205
8.7. Manual and DMA transfer modes for I2C controller 206
8.8. Register mapping 206

9. I2S 219

9.1. Introduction 219
9.2. Abbreviations 219
9.3. Features 219
9.4. Block diagram 220
9.5. IO interface 220
9.6. I2S OUT and I2S IN 221
9.7. DL FIFO and UL FIFO 222
9.8. Data format of FIFO 222
9.9. Programming guide 223
9.10. Register mapping 225

10. Interrupt 232

10.1. Overview 232

11. Keypad Scanner 235

11.1. Introduction 235
11.2. Abbreviations 235
11.3. Features and architecture 235
11.4. Keypad detection flow 238
11.5. Programming guide 243
11.6. Register mapping 244

12. SD/SDIO Card Controller 249

12.1. Introduction 249
12.2. Abbreviations 249
12.3. Features 249
12.4. Block diagram 249
12.5. Functions 250
12.6. Programming sequence 251
12.7. Register mapping 251

13. Pulse Width Modulation 314

13.1. Overview 314
13.2. Features 314
13.3. Block diagram 314
13.4. Functions 315
13.5. Register mapping 316

14. Pulse Width Modulation Signal Generator 319

14.1. Overview 319
14.2. Features 319
14.3. Block diagram 319
14.4. Functions 320
14.5. Register mapping 322

15. Reset Generation Unit 342

15.1. Introduction 342
15.2. Features 342
15.3. Block diagram 343
15.4. Function description 343
15.5. Register mapping 344

16. SDIO 355

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16.1. Overview 355
16.2. Abbreviations 355
16.3. Features 355
16.4. Block diagram 356
16.5. Functions 357
16.6. Register mapping 360

17. Serial Flash Controller 500

17.1. Introduction 500
17.2. Abbreviations 500
17.3. Features 500
17.4. Block diagram 501
17.5. Direct read 502
17.6. Macro read and write 502
17.7. Connection between internal SF and external SF 502
17.8. Programming guide 503
17.9. Register mapping 504
17.10. sf_top serial flash delay control setting 517

18. Top Miscellaneous Registers (TOP_MISC) 521

18.1. Overview 521
18.2. Register mapping 521

19. USB 1.1 Full Speed Controller 532

19.1. Introduction 532
19.2. Abbreviation 532
19.3. Feature 532
19.4. USB11 Controller Block Diagram 533
19.5. Register mapping 533

20. Serial Peripheral Interface Master Controller 555

20.1. Abbreviations 555
20.2. Features 555
20.3. Block diagram 559
20.4. Functions 559
20.5. Register mapping 560

21. Serial Peripheral Interface Slave Controller 570

21.1. Abbreviations 570
21.2. Features 570
21.3. Block diagram 572
21.4. Functions 572
21.5. Registers 576

22. Auxiliary ADC Unit 587

22.1. Overview 587
22.2. Abbreviations 587
22.3. Features 588
22.4. Block diagram 588
22.5. Functions 588
22.6. Programming sequence 589
22.7. Register mapping 592

23. General Purpose Timer 596

23.1. Overview 596
23.2. Features 596
23.3. Limitations 596
23.4. Block diagram 597

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23.5. Functions 598
23.6. Programming sequence 598
23.7. Register mapping 598

24. Operating System Timer 620

24.1. Overview 620
24.2. Features 620
24.3. Limitations 620
24.4. Block diagram 621
24.5. Functions 621
24.6. Programming sequence 621
24.7. Register mapping 622

25. Sensor Controller 630

25.1. Overview 630
25.2. Abbreviations 630
25.3. Features 630
25.4. Block diagram 631
25.5. Functions 632
25.6. Register mapping 632

26. Universal Asynchronous Receiver/Transmitter 666

26.1. Overview 666
26.2. Features 666
26.3. Block diagram 666
26.4. Functions 667
26.5. Register mapping 669

27. Real Time Clock (RTC) 685

27.1. Introduction 685
27.2. Abbreviations 685
27.3. Features 685
27.4. Block diagram 685
27.5. Functions 686

28. Power Management Unit and Low Power Control System 687

28.1. Overview 687
28.2. Low-power operating mode 687
28.3. Power performance summary 688
28.4. PMU architecture for low power system 689
28.5. PMU functional description 691

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Lists of Tables and Figures

Table 2.1-1. Abbreviations 3
Table 3.1-1. TCM address spaces for different cache size settings 7
Table 3.2-1. Write-back mode cache read or write operations 11
Table 3.2-2. Write-through mode cache R/W action summary 12
Table 3.4-1. Cacheable attribute bit encoding 19
Table 3.5-1. Region size and bit encoding 23
Table 5.2-1. Abbreviations 32
Table 5.5-1. Virtual FIFO access ports 35
Table 5.5-2. Function list of PD_DMA channels & Sensor_DMA channels 36
Table 6.2-1. Abbreviations 71
Table 6.8-1. External interrupt sources 74
Table 7.4-1. GPIO IO structure 88
Table 7.4-2. GPIO versus IO type mapping 89
Table 7.4-3. IO type 0 - pull up/down control 90
Table 7.4.1-4. IO type 3 - pull up/down control 91
Table 7.4.1-5. IO type 4 - pull up/down control 91
Table 7.4-6. IO type 5 - pull up/down control 91
Table 7.4-7. IO type 6 - pull up/down control 92
Table 7.5-1. Special registers 92
Table 8.2-1. Abbreviations 202
Table 9.2-1. Abbreviations 219
Table 9.3-1. I2S protocol specifications 219
Table 9.5-1. I2S interface signal description 220
Table 9.5-2. I2S mode interface – master mode 221
Table 9.5-3. I2S mode interface – slave mode 221
Table 9.5-4. Relationship between MCLK and sample rate 221
Table 10.1-1. Vector table for MT2625 232
Table 11.2-1. Abbreviations 235
Table 11.3-1. 3x3 single key order number in column/row matrix 235
Table 11.3-2. 3x3 double key order number in column/row matrix 236
Table 12.2-1. Abbreviations 249
Table 12.5-1. Pins of MSDC0 250
Table 12.5-2. Pins of MSDC1 251
Table 12.7-1. MSDC register definition 252
Table 14.4-1. PWMSG clock source table 320
Table 16.2-1. Abbreviations 355
Table 16.5-1. SDIO pin definitions 357
Table 16.5-2. Bus signal voltage 357
Table 16.5-3. Bus timing parameter values (default) 358
Table 16.5-4. High-speed timing parameter values 359

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Table 17.2-1. Abbreviations 500
Table 19.2-1. Abbreviations 532
Table 19.5-1. SPI master controller interface 555
Table 20.5-1. SPI slave controller interface 570
Table 21.1-1. Abbreviations 570
Table 21.4-1. SPI slave controller interface 572
Table 21.4-2. SPI slave status description (use RS command to poll SPI slave status) 574
Table 22.2-1. Abbreviations 587
Table 22.5-1. AUXADC channel description 589
Table 23.5-1. GPT operation modes 598
Table 24.5-1. OST operation modes....621
Table 25.2-1. Abbreviations 630
Table 27.2-1. Abbreviations 685
Table 28.3-1. Current consumption in different power modes 688
Table 28.4-1. BUCK / LDO characteristic....690

Figure 3.1-1. MCU, Cache, TCM and AHB bus connectivity 5
Figure 3.1-2. Cache size and TCM settings....6
Figure 3.2-1. Cache lookup for 4-way set associative 8
Figure 3.2-2. Cache miss/refill criteria 10
Figure 3.4-1. Cacheable setting example 18
Figure 3.5-1. Example settings of cache remapping 21
Figure 4.2-1. CMSYS (Cortex-M4 subsystem)....25
Figure 5.1-1. Variety data paths of DMA transfers 32
Figure 5.3-1. DMA block diagram....33
Figure 5.4-1. Ring buffer and double buffer memory data movement 34
Figure 5.4-2. Unaligned word accesses....34
Figure 5.4-3. Virtual FIFO DMA 35
Figure 6.4-1. EINT block diagram 72
Figure 6.7-1. FIRQ programming flow chart....74
Figure 7.3-1. GPIO block diagram 88
Figure 8.4-1. I2C block diagram....203
Figure 8.5-1. I2C single transfer single byte access....203
Figure 8.5-2. I2C single transfer multi byte access....204
Figure 8.5-3. I2C multi transfer multi byte access 204
Figure 8.5-4. I2C multi transfer multi byte access with RS....204
Figure 8.5-5. I2C multi transfer multi byte access with direction-change function 205
Figure 8.6-1. I2C transfer format programming guide....205
Figure 8.6-2. I2C timing format programming guide 206
Figure 9.4-1. I2S block diagram....220
Figure 11.3-1. 3x3 single keypad matrix (9 keys) 236
Figure 11.3-2. 3x3 double keypad matrix (18 keys) 237
Figure 11.3-3. One key pressed with de-bounce mechanism denoted 237
Figure 11.3-4. (a) Two keys pressed, case 1; (b) Two keys pressed, case 2 238

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Figure 11.4-1. Single keypad detection method 239
Figure 11.4-2. Brief schematic diagram of double keypad 240
Figure 11.4-3. Single key case 241
Figure 11.4-4. Row scan 242
Figure 11.4-5. Column scan 243
Figure 12.4-1. MSDC block diagram 250
Figure 13.1-1. PWM waveform 314
Figure 13.3-1. PWM block diagram 315
Figure 13.4-1. PWM waveform with register values 316
Figure 14.1-1. Generation procedure of PWMSG 319
Figure 14.3-1. PWMSG block diagram 320
Figure 14.4-1. PWMSG pulse sequence output pattern 320
Figure 14.4-2. PWMSG waveform with register values 321
Figure 14.4-3. PWMSG pulse sequence in memory mode 322
Figure 14.4-4. PWMSG pulse sequence in random mode 322
Figure 15.3-1. Block diagram of RGU 343
Figure 15.4-1. WDT time out length and interval time 343
Figure 16.4-1. SDIO controller block diagram 356
Figure 16.5-1. Signal connections to 4-bit SDIO cards 357
Figure 16.5-2. Bus signal levels 357
Figure 16.5-3. Bus timing diagram (default) 358
Figure 16.5-4. High-speed timing diagram 359
Figure 17.4-1. Serial flash controller block diagram 501
Figure 17.4-2. Serial flash device connection between macro and controller 502
Figure 17.10-1. Clock macro and clock delay select settings 517
Figure 17.10-2. Data macro and data delay select settings 517
Figure 19.4-1. USB controller block diagram 533
Figure 19.5-1. Pin connection between SPI master and SPI slave 555
Figure 20.2-1. SPI transmission formats 556
Figure 20.2-2. Operation flow with or without PAUSE mode 556
Figure 20.2-3. CS de-assert mode 557
Figure 20.2-4. SPI master controller delay sample 558
Figure 20.3-1. Block diagram of SPI master controller 559
Figure 20.4-1. SPI master single mode 559
Figure 20.4-2. SPI master dual mode write data 559
Figure 20.4-3. SPI master dual mode read data 560
Figure 20.4-4. SPI master quad mode write data 560
Figure 20.4-5. SPI master quad mode read data 560
Figure 20.5-1. Pin connection between SPI master and SPI slave 570
Figure 21.2-1. SPI transmission formats 571
Figure 21.2-2. SPI slave controller early transmit 571
Figure 21.3-1. Block diagram of SPI slave controller 572
Figure 21.4-1. SPI slave controller commands waveform 573
Figure 21.4-2. Config read/write (CR/CW) command format 573

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Figure 21.4-3. SPI slave control flow diagram 574
Figure 21.4-4. SPI slave single mode write data 575
Figure 21.4-5. SPI slave single mode read data 575
Figure 21.4-6. SPI slave dual mode write data 576
Figure 21.4-7. SPI slave dual mode read data 576
Figure 21.4-8. SPI slave quad mode write data 576
Figure 21.4-9. SPI slave quad mode read data 576
Figure 22.1-1. SAR ADC waveform 587
Figure 22.4-1. AUXADC block diagram 588
Figure 22.6-1. Immediate mode programming sequence 590
Figure 23.4-1. GPT block diagram 597
Figure 24.4-1. OST block diagram 621
Figure 25.3-1. Sensor timer sequence 630
Figure 25.4-1. Sensor controller block diagram 631
Figure 25.5-1. Sensor controller operation flow 632
Figure 26.3-1. UART block diagram 667
Figure 26.4-1 UART data format 668
Figure 27.4-1. RTC block diagram 686
Figure 28.2-1. MT2625 power states 688
Figure 28.4-1. MT2625 PMU power grid 690

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1. Documentation General Conventions

1.1. Abbreviations for control modules

Abbreviation	Full name
CMSYS	Cortex-M4 subsystem
DMA	Direct memory access
EINT	External interrupt controller
GPIO	General purpose input/output
I2C	Inter-integrated circuit interface
I2S	Inter-IC sound channel
MSDC	SD memory card controller
SDIO	Secure digital input/output
PWM	Pulse width modulation
RGU	Reset generation unit
SFC	Serial flash controller
TOP_MISC	Top miscellaneous register
USB	Universal Serial Bus
SPI master	Serial peripheral interface master controller
SPI slave	Serial peripheral interface slave controller
AUXADC	Auxiliary ADC
GPT	General purpose timer
OST	Operating system timer
UART	Universal asynchronous receiver transmitter

1.2. Abbreviations for registers

Abbreviation	Full name
RW	Read and write

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Abbreviation	Full name
RO	Read only
WO	Write only
RC	Read 1 to clear
WC	Write 1 to clear
RWC	Read or write 1 to clear
FM	Frequency measurement
FRC	Free running counter

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2. Bus Architecture

2.1. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 2.1-1. Abbreviations

Abbreviation	Definition
I-bus, D-bus, S-bus	Instruction bus, data bus, system bus
AO	Always-on
PD	Power down
SFC	Serial flash controller
DCM	Dynamic clock management
CG	Clock gater
XO	Crystal oscillator
XPLL	Audio phase-locked loop
SEJ	Security JTAG
EINT	External interrupt or event controller
GP timer	General purpose timer
OS	Operating system
USIM	Universal subscriber identity module
INFRA	Infrastructure design
MBIST	Memory built-in self-test

2.2. System architecture

MediaTek MT2625 consists of 32-bit multilayer AHB bus matrix that interconnects:

- 10 masters
  - Cortex-M4 with floating point unit (FPU) core I-bus, D-bus and S-bus
  - DMA memory bus
  - Sensor DMA memory bus
  - Sleep process manager (SPM)
  - Serial peripheral interface DMA bus (SPI)
  - Secure digital input/output DMA bus (SDIO)
  - Crypto engine DMA bus
  - Modem system (MDSYS) master bus
- 7 slaves
  - AHB peripheral including AHB to APB bridges and APB peripherals
  - Tightly-coupled memory (TCM)

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- Pseudo SRAM (PSRAM)
- Embedded flash
- Main System SRAM (SYSRAM)
- Retention SRAM (RTC SRAM)

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3. Cortex-M4 L1 Cache Controller

3.1. Overview

MediaTek MT2625 core processor is implemented with a subsystem including the core cache and tightly coupled memory (TCM). The subsystem is placed between the MCU core and AHB bus interface, as shown in Figure 3.1-1.

Figure 3.1-1. MCU, Cache, TCM and AHB bus connectivity

TCM is a high-speed (zero wait state) dedicated memory accessed exclusively by the MCU. Due to the latency penalty when the MCU accesses memory or peripherals through the on-chip bus, moving timing critical code and data into TCM can enhance the performance of the MCU and guarantee the response to particular events.

Another method to enhance MCU performance is the implementation of cache. In this case, the core cache is a small block of memory containing a copy of a small portion of cacheable data in the external memory. If the MCU reads a cacheable datum, the datum will be copied into the core cache. Once the MCU requests the same datum again, it can be obtained directly from the core cache (called cache hit) instead of fetching it again from the external memory. Consider the fact that accessing cache is much faster than accessing external memory through the bus system, a faster instruction fetching can be obtained leading to a higher instructions per cycle (IPC) which is a major factor in the evaluation of core performance. The cache can hold only a small portion of external memory. If MCU accesses a datum not found in the cache (called cache miss), one cache line must be dropped (flushed) and the required datum and its neighboring data are transferred from the external memory to cache (cache line fill). Before the cache line fill, cache write-back is required to maintain data consistency between cache and external memory. In this design, a cache line consists of eight words each with 32 bits. On the other hand, the best way to utilize TCM is to maintain the critical instruction or data in TCM. After system reset, the bootloader copies TCM content from the external storage, such as flash, to the internal TCM. If necessary, the MCU can replace TCM content with other data in the external storage during the runtime to implement an overlay mechanism. TCM is also ideal to store stack data.

The sizes of TCM and cache can be set to one of the following four configurations:

- 64KB TCM, 32KB cache
- 80KB TCM, 16KB cache
- 88KB TCM, 8KB cache
- 96KB TCM, 0KB cache (no cache)

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Figure 3.1-2. Cache size and TCM settings

The different configurations provide flexibility for software to adjust and reach optimum system performance.

The address mapping of the memories is shown in Table 3.1-1.

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Table 3.1-1. TCM address spaces for different cache size settings

SYSRAM identity	TCM start address (if memory is used as TCM)	Cache size			
		2'b00 TCM=96KB Cache=0KB	**2'b01** TCM=88KB Cache=8KB	**2'b10** TCM=80KB Cache=16KB	**2'b11** TCM=64KB Cache=43KB
SYSRAM_16KB_0	0x0400_0000	TCM	TCM	TCM	TCM
SYSRAM_16KB_1	0x0400_4000				
SYSRAM_16KB_2	0x0400_8000				
SYSRAM_16KB_3	0x0400_C000				
SYSRAM_8KB_0	0x0401_0000				Way0
SYSRAM_8KB_1	0x0401_2000				Way1
SYSRAM_4KB_0	0x0401_4000			Way0	Way2
SYSRAM_4KB_1	0x0401_5000			Way1	
SYSRAM_2KB_0	0x0401_6000		Way0	Way2	Way3
SYSRAM_2KB_1	0x0401_6800		Way1		
SYSRAM_2KB_2	0x0401_7000		Way2	Way3	
SYSRAM_2KB_3	0x0401_7800		Way3		

3.2. Cache optimization

The cache system has the following features:

1) Write back (unit: 4 words)
2) Configurable two or four way set associative
   a) 2-way set associative
      i) 128, 256, 512-set for 8, 16 or 32KB cache size, respectively.
      ii) Each way has 128, 256 or 512 cache lines with 8-word line size.
   b) 4-way set associative
      i) 64, 128, 256-set for 8, 16 or 32KB cache size, respectively.
      ii) Each way has 64, 128 or 256 cache lines with 8-word line size
3) 20-bit tag memory: 19-bit high address and 1-bit valid bit.
4) 2-bit dirty memory (each dirty bit records the dirtiness of half cache line – 4 words).

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Figure 3.2-1. Cache lookup for 4-way set associative

Each set associative cache has two memories: tag memory and data memory. The tag memory stores each line's valid bit and tag (upper 19 bits of the address). The data memory stores line data. When MCU accesses the memory, the address is compared to the content of the tag memory. First, the line index (address bits [12:5]) is used to locate a line in the tag memory. When a particular line is found in the tag memory, the upper 19 bits (address bits [31:13]), called tag, of the desired memory address are compared with the content of the identified tag line. If a match is found in both line address and tag address and the valid bit is 1, it is called a cache hit, and the data from that particular cache way is returned to the MCU. This process is shown in Figure 3.2-1.

If most memory accesses are cache hit, the MCU is able to acquire data without any delay, and the overall system performance will be higher. There are several factors that may affect the cache hit rate:

- Cache size and the organization

The larger the cache size, the higher the hit rate. However, the hit rate saturates when the cache size is larger than a threshold size. Normally the size of 16KB and above and two or four way set associative cache configuration can achieve a higher hit rate.

- 2 or 4-way set associative

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- 4-way set associative has higher hit rate than 2-way. However, the power consumption will be higher, as it accesses more memory during cache lookup.

- Program behavior

If the system has several tasks and switches between the tasks frequently, it may result in frequent cache content flush, as each time a new task is running, the cache holds its data for a certain period of time assuming it'll be used again. However, the stored data might get flushed out before being used again, if the following task requires the data occupying the same cache entries. Interrupts can cause program flow to change dynamically and reduce the benefit of using cache. The interrupt handler and the data it processes may cause cache to flush out data used by the current task. Thus, after returning from the interrupt handler to current task, the flushed data may need to be filled into the cache again if it's required by the program routine. This will cause performance degradation.

To tune the system performance, the cache controller in MT2625 records the cache hit count and number of cacheable memory accesses. The cache hit rate can be obtained by dividing these two numbers.

3.2.1. Write-back or write-through configurable cache

There are two different types of cache design to maintain data consistency. One is cache write-through and the other is cache write-back.

The write-back cache improves the performance especially when processors generate writes as fast as or faster than the writes that can be handled by the external memory. However, the implementation of write-back is more complex than that of write-through. When a cache line is dirty, four or eight words will be written back to the external memory at once and this will certainly occupy significant bus bandwidth and therefore decrease the overall efficiency. To solve this problem, a write buffer is necessary in the write-back implementation. Once the writes are written into the write buffer, the processor can continue the execution.

For systems with large memory write latency, it's possible that the burst write of cache write-back operation may cause large impact on the system performance. Change the cache to write-through mode in the software, if necessary.

3.2.1.1. Write-back implementation

When a cache hit occurs at write request, only the cache content will be modified and dirty bit will be set. The modified cache content won't match with that in the external memory, unlike cache write-through, which modifies both the cache content and the external memory synchronously.

When the cache misses the read request, line fill will be performed and a randomly selected cache line will be replaced, but before that, the dirty bits of that selected cache line have to be checked for the necessity of write-back. If the dirty bits are not set, line fill can proceed right away, and the selected cache line can be simply abandoned and replaced by a newly fetched line from the external memory that has the requested data. On the other hand, if one of or both the dirty bits are set, write-back has to be performed before line fill. In that case, half or the entire cache line is written into the write buffer. A summary is given in Figure 3.2-2.

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Figure 3.2-2. Cache miss/refill criteria

3.2.1.2. Write buffer

The write buffer consists of address buffer, data buffer, buffer for HTRANS, buffer for HSIZE, buffer for HLOCK and buffer for HBURST. The write buffer is designed as first-in-first-out (FIFO) with a depth of eight words. Since the output from the code cache meet the Advanced Microcontroller Bus Architecture (AMBA) format, the address buffer and data buffer are independent. The output of write buffer suffice the AMBA formatting guidelines and are designed for pipelining.

All CPU write accesses through the I-bus and D-bus will be buffered, no matter whether it is within the cacheable region or not.

Note: There is no control register to drain the write buffer, however software could initiate a Read access to ensure the previous data is written successfully to the external memory. This is recommended for data coherency management.

3.2.2. Cache operation

Upon power-on, the cache memory contains random values. The MCU needs to invalidate the cache content before enabling the cache usage.

The MCU needs to flush the cache data to the external memory to maintain data coherency before disabling the cache controller or MCU power-off.

The cache controller provides a register which, when written, can operate on the cache memory to fulfill the prerequisite mentioned above (called cache operation).

The operation involves:

1) Invalidate one cache line.

The user must give a memory address. If it's found within the cache, that particular cache line will be invalidated by writing 0 in the valid bit at the corresponding tag line. Alternatively, the user can invalidate a cache line by specifying a set/way mapped to that cache line.

2) Invalidate all cache lines.

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The user does not need to specify an address. The cache controller clears valid bits in all tag lines when this operation is requested.

3) Flush one cache line.

The user must give a memory address. If it is found within the cache and the dirty bit or bits are set, that particular cache line containing the given address will be flushed into the write buffer. Alternatively, the user can flush a cache line by specifying a set/way mapped to that cache line. This operation is not supported if the cache is operating in write-through mode.

4) Flush all cache lines.

The user does not need to specify an address. The cache controller flushes all the cache lines with the dirty bit or bits set. This operation is not supported if the cache is operating in write-through mode.

Note: To configure the cache size, follow the steps below to prevent cache data loss during the cache size configuration. At initialization, the cache size is set to 0. Cache operation code is highly recommended to be executed from TCM.

1) Flush all cache lines.
2) Invalidate all cache lines.
3) Configure the TCM and cache size.

3.2.3. Cache operation summary

Table 3.2-1. Write-back mode cache read or write operations

Op	Cacheable	Hit	Dirty		Action
			W0~W3	W4~W7	
Read	N	d	d	d	Single read
	Y	Y	d	d	Return data, no stall
		N	N	N	Line refill from bus using AHB WRAP8 burst
			N	Y	• Evict half line to WBuf. • Line refill from bus using AHB WRAP8 burst. • Write back half line from WBuf using AHB INCR4 burst write.
			Y	N	
			Y	Y	• Evict whole line to WBuf. • Line refill from bus using AHB WRAP8 burst. • Write back whole line from WBuf using AHB INCR8 burst write.
Write	N	d	d	d	• Wait for WBuf space. • Place write data into WBuf and let the MCU continue operating (CLKEN = 1). Stall the MCU by one cycle.
	Y	Y	d	d	• Write into cache; meanwhile set up the corresponding dirty bit. • Stall the MCU by one cycle to avoid structural hazard.

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Op	Cacheable	Hit	Dirty		Action
		N	d	d	• Wait for WBuf space. • Place write data into WBuf and let the MCU continue operating (CLKEN = 1). Stall the MCU by one cycle.

Legend Y: yes, N: no, d: don't care

Table 3.2-2. Write-through mode cache R/W action summary

Op	Cacheable	Hit	Action
Read	N	d	Single read
	Y	Y	• Return data, no stall
		N	• Line read from bus using AHB WRAP8 burst
Write	N	d	• Wait for WBuf space. • Place write data into WBuf and let the MCU continue operating (CLKEN = 1). Stall the MCU by one cycle.
	Y	N	
		Y	• Write to data SRAM. • Wait for WBuf space. • Place write data into WBuf and let the MCU continue operating (CLKEN = 1). Stall the MCU by one cycle.

Legend Y: yes, N: no, d: don't care

3.3. Register mapping

Module name: CACHE Base address: (+E0180000h)

CACHE+00h Cache general control register CACHE_CON

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						2WAYEN	CACHESIZE		MDRF				CNTEN1	CNTEN0		MCEN
Type						RW	RW		RW				RW	RW		R/W
Reset						0	00		0				0	0		0

This register determines the size of cache, cache hit counter and the enabling of MPU.

2WAYEN Enable 2-way cache look-up

0 Disable (4-way)

1 Enable (2-way)

CACHESIZE Selects cache size

00 No cache

01 8KB

10 16KB

11 32KB

MDRF Enables early restart function

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Cache does not wait for full block to be loaded before restarting the CPU. As soon as the requested word of the block arrives, it sends it to the CPU and lets the CPU continue execution.

0 Disable

1 Enable

CNTEN1 Enables cache hit counter 1

If enabled, the cache controller will increment a 48-bit counter by one when a cache hit is detected. This number is used in performance evaluation of the application. This counter increments only when the data are obtained from MPU cacheable regions 8 to 15.

0 Disable

1 Enable

CNTEN0 Enables cache hit counter 0

If enabled, the cache controller will increment a 48-bit counter by one when a cache hit is detected. This number is used in performance of the application. This counter increments only when the data are obtained from MPU cacheable regions 0 to 7.

0 Disable

1 Enable

MCEN Enables the comparison of cacheable/non-cacheable setting

If disabled, the MCU memory accesses are all non-cacheable, i.e. they will go through the AHB bus (except for TCM access). When enabled, if MCU accesses a cacheable memory region, the cache controller will return the data if it is found in cache and will get the data through the AHB bus only if a cache miss occurs.

0 Disable

1 Enable

CACHE+04h Cache operation **CACHE_OP**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TADDR[31:16]**															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TADDR[15:5]**											**OP[3:0]**				**EN**
Type	R/W											W				W1
Reset	0											0				0

This register defines the address and/or which type of cache operation to apply. When MCU writes into this register, the pipeline of MCU will be stopped for the cache controller to complete the operation. Bit 0 of the register must be written as 1 to enable the command.

TADDR[31:5] Target address

This field contains the address of invalidation operation. If OP[3:0] = 0010, TADDR[31:5] will be the address[31:5] of a memory whose line will be invalidated, if it exists in the cache. If OP[3:0] = 0100, TADDR[12:5] will indicate the set, while TADDR[19:16] indicates which way to clear:

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0001 way #0 (4-way)/way #0 first half (2-way)
0010 way #1 (4-way)/way #1 first half (2-way)
0100 way #2 (4-way)/way #0 second half (2-way)
1000 way #3 (4-way)/way #1 second half (2-way)
* For 2-way cache configuration, this operation has to be done twice in order to clear the entire way.

OP[3:0] Operation
This field determines which cache operations will be performed.
0001 invalidate all cache lines
0010 invalidate one cache line using address
0100 invalidate one cache line using set/way
1001 flush all cache lines
1010 flush one cache line using address
1100 flush one cache line using set/way

EN Enables command
This enabling bit must be written 1 to enable the command.
0 Does not enable
1 Enable

CACHE+08h Cache hit count 0 lower part **CACHE_HCNT0L**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CHIT_CNT0[31:16]**															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHIT_CNT0[15:0]**															
Type	R/W															
Reset	0															

CACHE+0Ch Cache hit count 0 upper part **CACHE_HCNT0U**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESERVED**															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CHIT_CNT0[47:32]**															
Type	R/W															
Reset	0															

When the CHIT_CNT0 bit in the CACHE_CON register is set to 1 (enabled), this register will start to record the cache hit count until it's disabled. If the value increases to above the maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. The 48-bit counter provides a recording time of 31 days even if MCU runs at 104MHz and every cycle is a cache hit. Note, that before enabling the counter, writing the initial value 0 to the counter is recommended.

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CHIT_CNT0[47:0] Cache hit count 0

WRITE Write any value to CACHE_HCNT0L or CACHE_HCNT0U clears CHIT_CNT0 to all 0.

READ Current counter value

CACHE+10h Cacheable access count 0 lower part CACHE_CCNT0L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CACC_CNT0[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT0[15:0]															
Type	R/W															
Reset	0															

CACHE+14h Cacheable access count 0 upper part CACHE_CCNT0U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT0[47:32]															
Type	R/W															
Reset	0															

When the CNTEN0 bit in the CACHE_CON register is set to 1 (enabled), this register is incremented at each cacheable memory access (no matter whether it is a cache miss or a cache hit). If the value increases to above the maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. For 104MHz MCU speed, if all memory accesses are cacheable and cache hit occurred, this counter will overflow after 2^{48}*9.6ns = 31 days. This is the shortest time for the counter to overflow. In a more realistic case, the system will have cache misses, non-cacheable accesses and idle mode that results in the counter overflow at later time.

CACC_CNT0[47:0] Cache access count 0

WRITE Write any value to CACHE_CCNT0L or CACHE_CCNT0U clears CACC_CNT0 to all 0.

READ Current counter value

The best way to use CACHE_HCNT0 and CACHE_CCNT0 is to set the initial value to 0 for both registers, enable both counters (set CNTEN0 to 1), run a portion of a program to be benchmarked, stop the counters and get their values. Therefore, during this period,

$$Cache\ hit\ rate = \frac{CACHE_HCNT}{CACHE_CCNT} \times 100\%$$

The cache hit rate value may help tune the performance of the application program. Note, that CHIT_CNT0 and CACC_CNT0 only increment if the cacheable attribute is defined in MPU cacheable region's lower half channels, such as channels 0 ~ 7 out of 16 channels.

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CACHE+18h Cache hit count 1 lower part CACHE_HCNT1L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHIT_CNT1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIT_CNT1[15:0]															
Type	R/W															
Reset	0															

CACHE+1Ch Cache hit count 1 upper part CACHE_HCNT1U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIT_CNT1[47:32]															
Type	R/W															
Reset	0															

When the CNTEN1 bit in CACHE_CON register is set to 1 (enabled), this register will start to record the cache hit count until it's disabled. If the value increases to above the maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. The 48-bit counter provides a recording time of 31 days even if MCU runs at 104MHz, and every cycle is a cache hit. Note, that before enabling the counter, writing the initial value 0 to the counter is recommended.

CHIT_CNT1[47:0] Cache hit count

WRITE Write any value to CACHE_HCNT1L or CACHE_HCNT1U clears CHIT_CNT1 to all 0.

READ Current counter value

CACHE+20h Cacheable access count 1 lower part CACHE_CCNT1L

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CACC_CNT1[31:16]															
Type	R/W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CACC_CNT1[15:0]															
Type	R/W															
Reset	0															

CACHE+24h Cacheable access count 1 upper part CACHE_CCNT1U

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESERVED															
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	CACC_CNT1[47:32]
Type	R/W
Reset	0

When CNTEN1 bit in CACHE_CON register is set to 1 (enabled), this register is incremented at each cacheable memory access (no matter whether it is a cache miss or a cache hit). If the value increases to above the maximum value (0xffffffffffff), it will be rolled over to 0 and continue counting. For 104MHz MCU speed, if all memory accesses are cacheable and cache hit, this counter will overflow after 2^{48}*9.6ns = 31 days. This is the shortest time for the counter to overflow. In a more realistic case, the system will have cache misses, non-cacheable accesses and idle mode that makes the counter overflow at later time.

CACC_CNT1[47:0] Cache access count 1

WRITE Write any value to CACHE_CCNT1L or CACHE_CCNT1U clears CACC_CNT1 to all 0.

READ Current counter value

The best way to use CACHE_HCNT1 and CACHE_CCNT1 is to set the initial value to 0 for both registers, enable both counters (set CNTEN1 to 1), run a portion of program to be benchmarked, stop the counters and get their values. Therefore, during this period,

$$Cache\ hit\ rate = \frac{CACHE_HCNT}{CACHE_CCNT} \times 100\%.$$

The cache hit rate value may help tune the performance of the application program. Note that CHIT_CNT1 and CACC_CNT1 only increment if the cacheable attribute is defined in MPU cacheable region for upper half channels (i.e. channels 8 ~ 15 of the total 16 channels).

CACHE+2C **Cache region enable** **CACHE_REGION_EN**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH9**	**CH8**	**CH7**	**CH6**	**CH5**	**CH4**	**CH3**	**CH2**	**CH1**	**CH0**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CH15~CH0 Enables/Disables the associated region

0 Disable the region setting

1 Enable the region setting

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3.4. Cacheable region controller

Cacheable region controller provides cacheable memory indication, featuring cacheable settings and attributes.

3.4.1. Cacheable settings

- Determine if a memory region is cacheable or not. If cacheable, MCU will keep a small copy in its cache after read accesses. If MCU requires the same data later, it can acquire it from the high-speed local copy, instead of low-speed external memory.
- The 4GB memory space is divided into 16 memory blocks with 256MB size each, such as MB0 to MB15. The characteristics of these memory blocks are listed below:
- All memory blocks are determined by the Cacheable Region Controller. Note, that the software should avoid making cache line access to the MB that does not support burst read or write. Usually only MB0 ~ MB1, mapped to the external memory interface (EMI), are set as cacheable regions.

3.4.2. Cacheable attribute

Figure 3.4-1. Cacheable setting example

Figure 3.4-1 provides cacheable settings in each memory block. Five regions are defined in the figure. Note, that each region can be continuous or non-continuous to each other. The address ranges not covered by any region in the cacheable settings are set to be non-cacheable automatically. There is also one restriction: different regions must not overlap.

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The user can define a maximum of 16 regions in MB0 ~ MB1. Each region has its own settings defined in a 32-bit register:

Register format

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BASEADDR[31:16]**															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASEADDR[15:12]**							**C**								
Type	**R W**							**R W**								
Reset	**0**							0								

3.4.2.1. Region base address

The region base address defines the starting point of the memory region. The user must only specify several upper address bits and align the base address to a minimum 4KB boundary.

3.4.2.2. Region size

The region size enumeration setting in the register is disabled in MT2625. Instead, use the CACHEABLE_END register to specify the end address base of a certain channel. The end address is non-inclusive, and the BASEADDR is inclusive. For example, by setting BASEADDR to 0x1000 and END BASEADDR to 0x2000, any address in the range (0x1000, 0x2000) will match this cacheable region setting.

The CACHEABLE_END register has 16 entries, starting right after the normal register and 0xE0190040 being the first entry.

Table 3.4-1. Cacheable attribute bit encoding

Bit encoding	Permission
0	Non-cacheable
1	Cacheable

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3.4.3. Register mapping

Module name: CACHE_Entry Base address: (+E0190000h)

CACHE_EMTRY_base+4*(n-1) n-th channel control CACHE_entry_n

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BASEADDR[31:16]**															
Type	R W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASEADDR[15:12]**							**C**								
Type	**R W**							**R W**								
Reset	**0**							0								

CACHE_EMTRY_base+0x40 + 4*(n-1) n-th channel control CACHE_End_entry_n

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BASEADDR[31:16]**															
Type	R W															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BASEADDR[15:12]**															
Type	**R W**															
Reset	**0**															

- MT2625 supports 16 channels.
- Refer to register format for detailed field descriptions.

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3.5. Remapping

MT2625 cache provides three sets of registers to set the actual memory address to different CPU load/store target address. Figure 3.5-1 shows the process of remapping.

The software sets 0x0xxxxxxx to cacheable and 0xFxxxxxxx to non-cacheable, but they are mapped to the same physical address.

Figure 3.5-1. Example settings of cache remapping

To achieve this:

1. Set regions beginning with 0x0000_0000 to cacheable.
2. Set regions beginning with 0x1000_0000 to non-cacheable.
3. Set BASEADDR field in Remap `EntryHi` to 0x1000_0000.
4. Set BASEADDR filed in Remap `EntryLo` to 0x0000_0000.

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3.5.1. Register definitions

Module name: NC-Remap Base address: (+E0181000h)

REMAP+0000h Remap Entry_HI0 **NCREMAP_HI0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:09]										SIZE[4:0]					EN
Type	R W										R W					R W
Reset											00000					0

This register sets up the remapping base attributes for region 0.

BASEADDR Base address of this region
SIZE Size of this region
EN **ENABLES THIS REGION**
0 DISABLE
1 ENABLE

REMAP+0004h Remap Entry_LO0 **NCREMAP_LO0**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:09]															
Type	R W															
Reset																

This register sets up the mapped address base for CPU accesses that are hits in NC-Remap Entry0_HI.

REMAP+0008h Remap Entry_HI1 **NCREMAP_HI1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:09]										SIZE[4:0]					EN
Type	R W										R W					R W
Reset											00000					0

This register sets up the remapping base attributes for region 1.

REMAP+000Ch Remap Entry_LO1 **NCREMAP_LO1**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:09]															
Type	R W															
Reset																

This register sets up the mapped address base for CPU accesses that are hits in NC-Remap Entry1_HI.

REMAP+0010h Remap Entry_HI2 **NCREMAP_HI2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:09]										SIZE[4:0]					EN
Type	R W										R W					R W
Reset											00000					0

This register sets up the remapping base attributes for region 2.

BASEADDR Base address of this region

SIZE Size of this region

EN **ENABLES THIS REGION**

- **0 DISABLE**
- **1 ENABLE**

REMAP+0014h Remap Entry_LO2 **NCREMAP_LO2**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BASEADDR[31:16]															
Type	R W															
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BASEADDR[15:09]															
Type	R W															
Reset																

This register sets up the mapped address base for CPU accesses that are hits in NC-Remap Entry2_HI.

Note, that the base and size settings in 3 `EntryHi` registers cannot be overlapped. Otherwise, the resultant mapped address will be undefined.

Table 3.5-1. Region size and bit encoding

Region size	Bit encoding	Base address
512B	`00000`	Bit [31:09] of region start address
1KB	`00001`	Bit [31:10] of region start address
2KB	`00010`	Bit [31:11] of region start address

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Region size	Bit encoding	Base address
4KB	00011	Bit [31:12] of region start address
8KB	00100	Bit [31:13] of region start address
16KB	00101	Bit [31:14] of region start address
32KB	00110	Bit [31:15] of region start address
64KB	00111	Bit [31:16] of region start address
128KB	01000	Bit [31:17] of region start address
256KB	01001	Bit [31:18] of region start address
512KB	01010	Bit [31:19] of region start address
1MB	01011	Bit [31:20] of region start address
2MB	01100	Bit [31:21] of region start address
4MB	01101	Bit [31:22] of region start address
8MB	01110	Bit [31:23] of region start address
16MB	01111	Bit [31:24] of region start address
32MB	10000	Bit [31:25] of region start address
64MB	10001	Bit [31:26] of region start address

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4. CMSYS

4.1. Overview

A Cortex-M4 subsystem layer (CMSYS) is created to wrap over the Cortex-M4 core to provide bus arbitration, instruction and data cache, interface synchronization, clock gating and several configuration options.

4.2. Block diagram

The block diagram of the CMSYS is shown in Figure 4.2-1.

Figure 4.2-1. CMSYS (Cortex-M4 subsystem)

4.3. Register mapping

Address	Name	Width (bits)	Register Function
A21E0000	CM4_BOOT0	32	Cortex-M4 boot vector 0
A21E0004	CM4_BOOT1	32	Cortex-M4 boot vector 1
A21E0008	CM4_BOOT_FROM_SLV	32	Cortex-M4 boot from slave
E0100004	STCALIB	32	Cortex-M4 system tick calibration
E0100008	Reserved	32	Reserved
E010000C	Reserved	32	Reserved
E0100010	Reserved	32	Reserved
E0100014	AHB_bufferable	32	AHB_bufferable

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Address	Name	Width (bits)	Register Function
E0100018	Reserved	32	Reserved
E010001C	Reserved	32	Reserved
E0100020	Reserved	32	Reserved
E0100024	Reserved	32	Reserved
E0100028	CG_freerun_en	32	CG_freerun_en
E010002C	CG_gate_en	32	CG_gate_en
E0100030	Reserved	32	Reserved
E0100034	INT_active_high_low_0	32	INT_active_high_low_0
E0100038	INT_active_high_low_1	32	INT_active_high_low_1
E0100040	DCM_ctrl_reg	32	DCM feature for L1 cache
E0100044	MEMsize_Config	32	EMI/SFC memory size configuration

A21E0000 CM4_BOOT0 Cortex-M4 boot vector 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CM4_BOOT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CM4_BOOT0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CM4_BOOT0	**Once Cortex-M4 reset is de-asserted, Cortex-M4 will fetch CM4_BOOT0 and CM4_BOOT1 when CM4_boot_from_slave = 1** [31:0]: Cortex-M4 MSP value

A21E0004 CM4_BOOT1 Cortex-M4 boot vector 1 04100001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CM4_BOOT1															
Type	RW															
Reset	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CM4_BOOT1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	CM4_BOOT1	**Once Cortex-M4 reset is de-asserted, Cortex-M4 will fetch CM4_BOOT0 and CM4_BOOT1 when CM4_boot_from_slave = 1**

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Bit(s)	Name	Description
		[31:0]: reset handler address for example: 32'h04100001 (boot ROM), 32'h1 (EMI), 32'h04008001 (Cortex-M4 TCM)

A21E0008 CM4_BOOT_FROM_SLV Cortex-M4 boot from slave 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CM4_boot_from_slave
Type																RW
Reset																1

Bit(s)	Name	Description
0	CM4_boot_from_slave	**Once Cortex-M4 reset is de-asserted, indicate which device Cortex-M4 has rebooted from** 0: Boot from EMI 1: Boot from boot slave

E0100004 STCALIB Cortex-M4 system tick calibration 01000147

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							NOREF	SKEW	TENMS							
Type							RW	RW	RW							
Reset							0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TENMS															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1

Bit(s)	Name	Description
25	NOREF	**Cortex-M4 system tick calibration** 1: no reference clock 0: with reference clock
24	SKEW	**Cortex-M4 system tick calibration** 1: skew 0: no skew
23:0	TENMS	**Provides an integer value to compute a 10ms (100Hz) delay from either CPU or external clock (reference clocks).**

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Bit(s)	Name	Description
		for example, set 147 in HEX (or 327 in decimal) for 32.768kHz

E0100014 AHB_bufferable AHB_bufferable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											AHB_bufferable_dis					cm4_bufferable
Type											RW					RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:1	AHB_bufferable_dis	**Disable AHB Synchronous or Asynchronous bridge write bufferable attribute** 1: disable 0: enable (bus will write early response) [1]: reserved [2]: ID bus to infrastructure design (INFRA) synchronous bridge [3]: SYS bus to infrastructure design (INFRA) synchronous bridge [4]: reserved [5]: reserved
0	cm4_bufferable	**1: Use Cortex-M4 sys bus signal hprot[2] for CMSYS bus IP** 0: Don't use

E0100028 CG_freerun_en CG_freerun_en 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CG_freerun_en					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	CG_freerun_en	**Force clock gater free run** 1: force free-run clock 0: normal function (dynamic gated by idle signals) [5]: Reserved [4]: Cortex-M4 bus slow clock [3]: Cortex-M4 bus fast clock [2]: Cortex-M4 L1 cache controller clock [1]: Cortex-M4 HCLK [0]: Cortex-M4 FCLK

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Bit(s)	Name	Description

E0100030 CG_gate_en CG_gate_en 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CG_gate_en					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	CG_gate_en	**Force clock gater gated when CG_freerun_en = 0** 1: force clock gated (turn off clock) 0: normal function (dynamic gated by idle signals) for example, if CG_freerun_en[0] = 1, then clock will free-run, CG_gate_en[0] has no effect. [5]: Reserved [4]: Cortex-M4 bus slow clock [3]: Cortex-M4 bus fast clock [2]: Cortex-M4 L1 cache controller clock [1]: Cortex-M4 HCLK [0]: Cortex-M4 FCLK

E0100034 INT_active_high_low_0 INT_active_high_low_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_active_high_low_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT_active_high_low_0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_active_high_low_0	**Interrupt source active high/low configuration (ISR 0-31)** 1:active high 0:active low [bit] : integer number

E0100038 INT_active_high_low_1 INT_active_high_low_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INT_active_high_low_1															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**INT_active_high_low_1**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_active_high_low_1	**Interrupt source active high/low configuration (ISR 32-63)** 1:active high 0:active low [bit] : integer number + 32, which means an offset + 32

E010003C INT_active_high_low_2 INT_active_high_low_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**INT_active_high_low_2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**INT_active_high_low_2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	INT_active_high_low_1	**Interrupt source active high/low configuration (ISR 64-77)** 1:active high 0:active low [13:0] : integer number + 64, which means an offset + [31:14]: Reserved

E0100040 DCM_ctrl_reg DCM feature for L1 cache 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**l1c_dcm_ctrl**								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	l1c_dcm_ctrl	**DCM for L1 cache feature is also disabled if**

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Bit(s)	Name	Description
		CG_freerun_en/CG_gate_en is activated [8]: l1c_dirty_bit_dcm_e 1: Enable DCM feature for dirty RAM 0: Disable DCM feature for dirty RAM [7:4]: l1c_dcm_wait_cnt n=0.15. Wait for the n-th cycle before stopping the clock of L1 cache. Only valid when l1c_dcm_en = 1'b1 [3]: reserved [2]: l1c_dcm_write_en 1: Enable DCM feature of L1 cache for write transaction 0: Disable DCM feature of L1 cache for write transaction [1]: l1c_dcm_read_en 1: Enable DCM feature of L1 cache for read transaction 0: Disable DCM feature of L1 cache for read transaction [0]: DCM enable 1: Enable DCM feature for L1 cache 0: Disable DCM feature for L1 cache

E0100044 MEMsize_Config Memory size configuration 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										memsize_config						
Type										RW						
Reset										0	0	0	0	0	1	1

Bit(s)	Name	Description
6:0	memsize_config	**bit[6:1] : EMI memory size configuration** 6'b000000: 1MB 6'b000001: 2MB 6'b000011: 4MB 6'b000111: 8MB vice versa 6'b11111111: 64MB bit [0] : Enable EMI memory size configuration 0:Disable 1: Enable

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5. Direct Memory Access

5.1. Overview

Two DMA controllers are placed on AHB bus to support fast data transfers and off-load the processor. With the controllers, specific devices on AHB or APB buses can benefit greatly from quick completion of data movement from or to memory modules. Such DMA controllers can also be used to connect two devices other than memory modules as long as they can be addressed in memory space. Figure 5.1-1 illustrates the system connections.

Figure 5.1-1. Variety data paths of DMA transfers

5.2. Abbreviations

Table 5.2-1 lists the abbreviations used in this section.

Table 5.2-1. Abbreviations

Abbreviation	Definition
GDMA	General DMA, full DMA. The source and destination addresses are both flexible.
PDMA	Partial DMA, half DMA. Only one of the source or destination addresses is flexible and the other is fixed, including handshake signals with peripherals.
VDMA	Virtual FIFO DMA. Only one of the source or destination addresses is flexible and the other is fixed, including handshake signals with peripherals and pointer manager.

5.3. Features

There is a round-robin arbitration mechanism to support up to 18 channels in PD_DMA and 9 channels in Sensor_DMA working simultaneously. Each channel has a similar set of registers to be configured to different schemes as required. Both interrupt and polling based schemes are supported to handle the completion events.

The operating block diagram of the DMAs is shown in Figure 5.3-1.

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Figure 5.3-1. DMA block diagram

5.4. Functions

There are three types of DMA channels in the DMA controller: full-size DMA, half-size DMA and virtual FIFO DMA. Channel 1 is a full-size DMA channel, channels 2 to 6 are half-size channels and channels 7 to 18 are virtual FIFO DMA channels. The difference between the first two types of DMA channels is that source and destination addresses are programmable as full-size DMA channels, but the address of either source or destination only can be programmed as a half-size DMA channel, while the address of the other side is fixed.

5.4.1. Ring buffer and double buffer memory data transfer

DMA channels 1 to 6 support ring-buffer and double-buffer memory data transfer. This can be achieved by programming DMA_WPPT and DMA_WPTO, as well as setting up WPEN in the DMA_CON register, as shown in Figure 5.4-1. The next address jumps to WPTO address once the transfer counter reaches WPPT.

Note, that only one side can be configured as ring-buffer or double-buffer memory, and this is controlled by WPSD in the DMA_CON register.

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Figure 5.4-1. Ring buffer and double buffer memory data movement

5.4.2. Unaligned word access

The address of word access on AHB bus must be aligned to word boundary (the address must be multiple of 4), or the two LSB are truncated to 00b. If the LSB is truncated, incorrect data may be fetched. If the data is moved from unaligned to aligned address, the word is usually split into four bytes then moved byte by byte. Thus, the four read and four write transfers will appear on the bus.

To improve bus efficiency, the unaligned word access is provided in DMA channel 4 to 15. If “byte-to-word (B2W)” function is enabled in PDMAx_CON, the DMAs will move data from the unaligned address to aligned address by executing four continuous byte-read accesses and one word-write access, reducing the number of transfers on the bus by three, as shown in Figure 5.4-2.

Figure 5.4-2. Unaligned word accesses

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5.4.3. Virtual FIFO DMA

Virtual FIFO DMA is used to ease UART control. The difference between the virtual FIFO DMA and the ordinary DMA is that the virtual FIFO DMA contains additional FIFO controllers. The read and write pointers are kept in the virtual FIFO DMA. To read from FIFO, the read pointer points to the address of the next data. To write into the FIFO, the write pointer moves to the next address. If the FIFO is empty, a FIFO read will not be allowed. Similarly, the data will not be written to the FIFO, if the FIFO is full. Due to UART flow control requirements, an alert length (VDMAx_ALTLEN) is programmed. If the FIFO space is smaller than this value, an alert signal is issued to enable the UART flow control. The type of flow control performed depends on the UART configuration settings.

Each virtual FIFO DMA can be programmed as receive (RX) or transmit (TX) FIFO. This depends on the DIR setting in the DMA_CON register. If DIR is “0” (READ), the virtual FIFO DMA is specified as a TX FIFO. On the other hand, if DIR is “1” (WRITE), the virtual FIFO DMA will be specified as an RX FIFO.

The virtual FIFO DMA provides an interrupt to MCU to notify data availability in the FIFO and the amount of data is above or under the value defined in the DMA_COUNT register. Based on this, the MCU does not need to poll the DMA to know when the data must be removed from or put into the FIFO.

Figure 5.4-3. Virtual FIFO DMA

5.5. Application and programming sequence

PD_DMA channels 7 to 18 are virtual FIFO DMA with corresponding peripherals. The access port for the MCU of each VDMA are listed in Table 5.5-1. MCU treats the virtual FIFO access port as a real FIFO, but the physical location or size is configured by the registers of each channel.

Table 5.5-1. Virtual FIFO access ports

DMA number	Address of virtual FIFO access port	Reference UART
DMA16(PD)	A100_0000h	UART2 TX
DMA17(PD)	A100_0100h	UART2 RX
DMA18(PD)	A100_0200h	UART1 TX

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DMA number	Address of virtual FIFO access port	Reference UART
DMA19(PD)	A100_0300h	UART1 RX
DMA20(PD)	A100_0400h	UART0 TX
DMA21(PD)	A100_0500h	UART0 RX
DMA22(PD)	A100_0600h	I2S0 TX
DMA23(PD)	A100_0700h	I2S0 RX
DMA24(PD)	A100_0800h	I2S1 TX
DMA25(PD)	A100_0900h	I2S1 RX
DMA26(PD)	A100_0A00h	UART3 TX
DMA27(PD)	A100_0B00h	UART3 RX

Due to different types of DMA, the limitations for each peripheral are listed below.

Table 5.5-2. Function list of PD_DMA channels & Sensor_DMA channels

DMA number	Type	Ring buffer	Double buffer	Burst mode	Unaligned word access	Peripheral
DMA1(PD)	Full size	●	●	●		application use
DMA2(PD)	Full size	●	●	●		modem system use
DMA3(Sensor)	Full size	●	●	●		
DMA4(PD)	Half size	●	●	●	●	USB1 TX
DMA5(PD)	Half size	●	●	●	●	USB1 RX
DMA6(PD)	Half size	●	●	●	●	USB2 TX
DMA7(PD)	Half size	●	●	●	●	USB2 RX
DMA8(Sensor)	Half size	●	●	●	●	I2C0_TX
DMA9(Sensor)	Half size	●	●	●	●	I2C0_RX
DMA10(Sensor)	Half size	●	●	●	●	I2C1_TX
DMA11(Sensor)	Half size	●	●	●	●	I2C1_RX
DMA12(Sensor)	Half size	●	●	●	●	I2C2_TX
DMA13(Sensor)	Half size	●	●	●	●	I2C2_RX
DMA14(Sensor)	Half size	●	●	●	●	USIM_TX
DMA15(Sensor)	Half size	●	●	●	●	USIM_RX
DMA16(PD)	Virtual FIFO	●				UART2 TX
DMA17(PD)	Virtual FIFO	●				UART2 RX
DMA18(PD)	Virtual FIFO	●				UART1 TX
DMA19(PD)	Virtual FIFO	●				UART1 RX
DMA20(PD)	Virtual FIFO	●				UART0 TX

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DMA number	Type	Ring buffer	Double buffer	Burst mode	Unaligned word access	Peripheral
DMA21(PD)	Virtual FIFO	•				UART0 RX
DMA22(PD)	Virtual FIFO	•				I2S0 TX
DMA23(PD)	Virtual FIFO	•				I2S0 RX
DMA24(PD)	Virtual FIFO	•				I2S1 TX
DMA25(PD)	Virtual FIFO	•				I2S1 RX
DMA26(PD)	Virtual FIFO	•				UART3 TX
DMA27(PD)	Virtual FIFO	•				UART3 RX

5.6. Register mapping

There are 18 DMA channels in this SoC.

5.6.1. DMA register map

Module name: DMA Base address: (+a0020000h)

Address	Name	Width (bits)	Register Function
A0020000	DMA_GLBSTA	32	DMA global status
A0020004	DMA_GLBSTA2	32	DMA global status
A0020008	DMA_GLB_CPU0_CFG	32	DMA top hierarchy interrupt configuration
A002000C	DMA_GLB_CPU0_SET	32	DMA top hierarchy interrupt set
A0020010	DMA_GLB_CPU0_CLR	32	DMA top hierarchy interrupt clear
A0020028	DMA_GLBLIMITER	32	DMA global bandwidth limiter register
A0020020	DMA_GLB_SWRST	32	DMA global software reset
A0020040	DMA_GLB_BUSY	32	DMA global busy status
A0020044	DMA_GLB_INTR	32	DMA global interrupt status
A0020100	GDMA1_SRC	32	DMA channel 1 source address
A0020104	GDMA1_DST	32	DMA channel 1 destination address
A0020108	GDMA1_WPPT	32	DMA channel 1 wrap point address
A002010C	GDMA1_WPTO	32	DMA channel 1 wrap to address
A0020110	GDMA1_COUNT	32	DMA channel 1 transfer count
A0020114	GDMA1_CON	32	DMA channel 1 control
A0020118	GDMA1_START	32	DMA channel 1 start
A002011C	GDMA1_INTSTA	32	DMA channel 1 interrupt status
A0020120	GDMA1_ACKINT	32	DMA channel 1 interrupt acknowledge
A0020124	GDMA1_RLCT	32	DMA channel 1 remaining length of current transfer
A0020128	GDMA1_LIMITER	32	DMA channel 1 bandwidth limiter

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Address	Name	Width (bits)	Register Function
A0020200	GDMA2_SRC	32	DMA channel 2 source address
A0020204	GDMA2_DST	32	DMA channel 2 destination address
A0020208	GDMA2_WPPT	32	DMA channel 2 wrap point address
A002020C	GDMA2_WPTO	32	DMA channel 2 wrap to address
A0020210	GDMA2_COUNT	32	DMA channel 2 transfer count
A0020214	GDMA2_CON	32	DMA channel 2 control
A0020218	GDMA2_START	32	DMA channel 2 start
A002021C	GDMA2_INTSTA	32	DMA channel 2 interrupt status
A0020220	GDMA2_ACKINT	32	DMA channel 2 interrupt acknowledge
A0020224	GDMA2_RLCT	32	DMA channel 2 remaining length of current transfer
A0020228	GDMA2_LIMITER	32	DMA channel 2 bandwidth limiter
A0020308	PDMA4_WPPT	32	DMA channel 4 wrap point address
A002030C	PDMA4_WPTO	32	DMA channel 4 wrap to address
A0020310	PDMA4_COUNT	32	DMA channel 4 transfer count
A0020314	PDMA4_CON	32	DMA channel 4 control
A0020318	PDMA4_START	32	DMA channel 4 start
A002031C	PDMA4_INTSTA	32	DMA channel 4 interrupt status
A0020320	PDMA4_ACKINT	32	DMA channel 4 interrupt acknowledge
A0020324	PDMA4_RLCT	32	DMA channel 4 remaining length of current transfer
A0020328	PDMA4_LIMITER	32	DMA channel 4 bandwidth limiter
A002032C	PDMA4_PGMADDR	32	DMA channel 4 programmable address
A0020408	PDMA5_WPPT	32	DMA channel 5 wrap point address
A002040C	PDMA5_WPTO	32	DMA channel 5 wrap to address
A0020410	PDMA5_COUNT	32	DMA channel 5 transfer count
A0020414	PDMA5_CON	32	DMA channel 5 control
A0020418	PDMA5_START	32	DMA channel 5 start
A002041C	PDMA5_INTSTA	32	DMA channel 5 interrupt status
A0020420	PDMA5_ACKINT	32	DMA channel 5 interrupt acknowledge
A0020424	PDMA5_RLCT	32	DMA channel 5 remaining length of current transfer
A0020428	PDMA5_LIMITER	32	DMA channel 5 bandwidth limiter
A002042C	PDMA5_PGMADDR	32	DMA channel 5 programmable address
A0020508	PDMA6_WPPT	32	DMA channel 6 wrap point address
A002050C	PDMA6_WPTO	32	DMA channel 6 wrap to address
A0020510	PDMA6_COUNT	32	DMA channel 6 transfer count
A0020514	PDMA6_CON	32	DMA channel 6 control
A0020518	PDMA6_START	32	DMA channel 6 start
A002051C	PDMA6_INTSTA	32	DMA channel 6 interrupt status
A0020520	PDMA6_ACKINT	32	DMA channel 6 interrupt acknowledge
A0020524	PDMA6_RLCT	32	DMA channel 6 remaining length of current transfer
A0020528	PDMA6_LIMITER	32	DMA channel 6 bandwidth limiter
A002052C	PDMA6_PGMADDR	32	DMA channel 6 programmable address
A0020608	PDMA7_WPPT	32	DMA channel 7 wrap point address

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Address	Name	Width (bits)	Register Function
A002060C	PDMA7_WPTO	32	DMA channel 7 wrap to address
A0020610	PDMA7_COUNT	32	DMA channel 7 transfer count
A0020614	PDMA7_CON	32	DMA channel 7 control
A0020618	PDMA7_START	32	DMA channel 7 start
A002061C	PDMA7_INTSTA	32	DMA channel 7 interrupt status
A0020620	PDMA7_ACKINT	32	DMA channel 7 interrupt acknowledge
A0020624	PDMA7_RLCT	32	DMA channel 7 remaining length of current transfer
A0020628	PDMA7_LIMITER	32	DMA channel 7 bandwidth limiter
A002062C	PDMA7_PGMADDR	32	DMA channel 7 programmable address
A0020710	VDMA16_COUNT	32	DMA channel 16 transfer count
A0020714	VDMA16_CON	32	DMA channel 16 control
A0020718	VDMA16_START	32	DMA channel 16 start register
A002071C	VDMA16_INTSTA	32	DMA channel 16 interrupt status
A0020720	VDMA16_ACKINT	32	DMA channel 16 interrupt acknowledge
A0020728	VDMA16_LIMITER	32	DMA channel 16 bandwidth limiter
A002072C	VDMA16_PGMADDR	32	DMA channel 16 programmable address
A0020730	VDMA16_WRPTR	32	DMA channel 16 write pointer
A0020734	VDMA16_RDPTR	32	DMA channel 16 read pointer
A0020738	VDMA16_FFCNT	32	DMA channel 16 FIFO count
A002073C	VDMA16_FFSTA	32	DMA channel 16 FIFO status
A0020740	VDMA16_ALTLEN	32	DMA channel 16 alert length
A0020744	VDMA16_FFSIZE	32	DMA channel 16 FIFO size
A0020810	VDMA17_COUNT	32	DMA channel 17 transfer count
A0020814	VDMA17_CON	32	DMA channel 17 control
A0020818	VDMA17_START	32	DMA channel 17 start register
A002081C	VDMA17_INTSTA	32	DMA channel 17 interrupt status
A0020820	VDMA17_ACKINT	32	DMA channel 17 interrupt acknowledge
A0020828	VDMA17_LIMITER	32	DMA channel 17 bandwidth limiter
A002082C	VDMA17_PGMADDR	32	DMA channel 17 programmable address
A0020830	VDMA17_WRPTR	32	DMA channel 17 write pointer
A0020834	VDMA17_RDPTR	32	DMA channel 17 read pointer
A0020838	VDMA17_FFCNT	32	DMA channel 17 FIFO count
A002083C	VDMA17_FFSTA	32	DMA channel 17 FIFO status
A0020840	VDMA17_ALTLEN	32	DMA channel 17 alert length
A0020844	VDMA17_FFSIZE	32	DMA channel 17 FIFO size
A0020910	VDMA18_COUNT	32	DMA channel 18 transfer count
A0020914	VDMA18_CON	32	DMA channel 18 control
A0020918	VDMA18_START	32	DMA channel 18 start register
A002091C	VDMA18_INTSTA	32	DMA channel 18 interrupt status
A0020920	VDMA18_ACKINT	32	DMA channel 18 interrupt acknowledge
A0020928	VDMA18_LIMITER	32	DMA channel 18 bandwidth limiter
A002092C	VDMA18_PGMADDR	32	DMA channel 18 programmable address
A0020930	VDMA18_WRPTR	32	DMA channel 18 write pointer

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Address	Name	Width (bits)	Register Function
A0020934	VDMA18_RDPTR	32	DMA channel 18 read pointer
A0020938	VDMA18_FFCNT	32	DMA channel 18 FIFO count
A002093C	VDMA18_FFSTA	32	DMA channel 18 FIFO status
A0020940	VDMA18_ALTLEN	32	DMA channel 18 alert length
A0020944	VDMA18_FFSIZE	32	DMA channel 18 FIFO size
A0020A10	VDMA19_COUNT	32	DMA channel 19 transfer count
A0020A14	VDMA19_CON	32	DMA channel 19 control
A0020A18	VDMA19_START	32	DMA channel 19 start register
A0020A1C	VDMA19_INTSTA	32	DMA channel 19 interrupt status
A0020A20	VDMA19_ACKINT	32	DMA channel 19 interrupt acknowledge
A0020A28	VDMA19_LIMITER	32	DMA channel 19 bandwidth limiter
A0020A2C	VDMA19_PGMADDR	32	DMA channel 19 programmable address
A0020A30	VDMA19_WRPTR	32	DMA channel 19 write pointer
A0020A34	VDMA19_RDPTR	32	DMA channel 19 read pointer
A0020A38	VDMA19_FFCNT	32	DMA channel 19 FIFO count
A0020A3C	VDMA19_FFSTA	32	DMA channel 19 FIFO status
A0020A40	VDMA19_ALTLEN	32	DMA channel 19 alert length
A0020A44	VDMA19_FFSIZE	32	DMA channel 19 FIFO size
A0020B10	VDMA20_COUNT	32	DMA channel 20 transfer count
A0020B14	VDMA20_CON	32	DMA channel 20 control
A0020B18	VDMA20_START	32	DMA channel 20 start register
A0020B1C	VDMA20_INTSTA	32	DMA channel 20 interrupt status
A0020B20	VDMA20_ACKINT	32	DMA channel 20 interrupt acknowledge
A0020B28	VDMA20_LIMITER	32	DMA channel 20 bandwidth limiter
A0020B2C	VDMA20_PGMADDR	32	DMA channel 20 programmable address
A0020B30	VDMA20_WRPTR	32	DMA channel 20 write pointer
A0020B34	VDMA20_RDPTR	32	DMA channel 20 read pointer
A0020B38	VDMA20_FFCNT	32	DMA channel 20 FIFO count
A0020B3C	VDMA20_FFSTA	32	DMA channel 20 FIFO status
A0020B40	VDMA20_ALTLEN	32	DMA channel 20 alert length
A0020B44	VDMA20_FFSIZE	32	DMA channel 20 FIFO size
A0020C10	VDMA21_COUNT	32	DMA channel 21 transfer count
A0020C14	VDMA21_CON	32	DMA channel 21 control
A0020C18	VDMA21_START	32	DMA channel 21 start register
A0020C1C	VDMA21_INTSTA	32	DMA channel 21 interrupt status
A0020C20	VDMA21_ACKINT	32	DMA channel 21 interrupt acknowledge
A0020C28	VDMA21_LIMITER	32	DMA channel 21 bandwidth limiter
A0020C2C	VDMA21_PGMADDR	32	DMA channel 21 programmable address
A0020C30	VDMA21_WRPTR	32	DMA channel 21 write pointer
A0020C34	VDMA21_RDPTR	32	DMA channel 21 read pointer
A0020C38	VDMA21_FFCNT	32	DMA channel 21 FIFO count
A0020C3C	VDMA21_FFSTA	32	DMA channel 21 FIFO status
A0020C40	VDMA21_ALTLEN	32	DMA channel 21 alert length
A0020C44	VDMA21_FFSIZE	32	DMA channel 21 FIFO size

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Address	Name	Width (bits)	Register Function
A0020D10	VDMA22_COUNT	32	DMA channel 22 transfer count
A0020D14	VDMA22_CON	32	DMA channel 22 control
A0020D18	VDMA22_START	32	DMA channel 22 start register
A0020D1C	VDMA22_INTSTA	32	DMA channel 22 interrupt status
A0020D20	VDMA22_ACKINT	32	DMA channel 22 interrupt acknowledge
A0020D28	VDMA22_LIMITER	32	DMA channel 22 bandwidth limiter
A0020D2C	VDMA22_PGMADDR	32	DMA channel 22 programmable address
A0020D30	VDMA22_WRPTR	32	DMA channel 22 write pointer
A0020D34	VDMA22_RDPTR	32	DMA channel 22 read pointer
A0020D38	VDMA22_FFCNT	32	DMA channel 22 FIFO count
A0020D3C	VDMA22_FFSTA	32	DMA channel 22 FIFO status
A0020D40	VDMA22_ALTLEN	32	DMA channel 22 alert length
A0020D44	VDMA22_FFSIZE	32	DMA channel 22 FIFO size
A0020E10	VDMA23_COUNT	32	DMA channel 23 transfer count
A0020E14	VDMA23_CON	32	DMA channel 23 control
A0020E18	VDMA23_START	32	DMA channel 23 start register
A0020E1C	VDMA23_INTSTA	32	DMA channel 23 interrupt status
A0020E20	VDMA23_ACKINT	32	DMA channel 23 interrupt acknowledge
A0020E28	VDMA23_LIMITER	32	DMA channel 23 bandwidth limiter
A0020E2C	VDMA23_PGMADDR	32	DMA channel 23 programmable address
A0020E30	VDMA23_WRPTR	32	DMA channel 23 write pointer
A0020E34	VDMA23_RDPTR	32	DMA channel 23 read pointer
A0020E38	VDMA23_FFCNT	32	DMA channel 23 FIFO count
A0020E3C	VDMA23_FFSTA	32	DMA channel 23 FIFO status
A0020E40	VDMA23_ALTLEN	32	DMA channel 23 alert length
A0020E44	VDMA23_FFSIZE	32	DMA channel 23 FIFO size
A0020F10	VDMA24_COUNT	32	DMA channel 24 transfer count
A0020F14	VDMA24_CON	32	DMA channel 24 control
A0020F18	VDMA24_START	32	DMA channel 24 start register
A0020F1C	VDMA24_INTSTA	32	DMA channel 24 interrupt status
A0020F20	VDMA24_ACKINT	32	DMA channel 24 interrupt acknowledge
A0020F28	VDMA24_LIMITER	32	DMA channel 24 bandwidth limiter
A0020F2C	VDMA24_PGMADDR	32	DMA channel 24 programmable address
A0020F30	VDMA24_WRPTR	32	DMA channel 24 write pointer
A0020F34	VDMA24_RDPTR	32	DMA channel 24 read pointer
A0020F38	VDMA24_FFCNT	32	DMA channel 24 FIFO count
A0020F3C	VDMA24_FFSTA	32	DMA channel 24 FIFO status
A0020F40	VDMA24_ALTLEN	32	DMA channel 24 alert length
A0020F44	VDMA24_FFSIZE	32	DMA channel 24 FIFO size
A0021010	VDMA25_COUNT	32	DMA channel 25 transfer count
A0021014	VDMA25_CON	32	DMA channel 25 control
A0021018	VDMA25_START	32	DMA channel 25 start register
A002101C	VDMA25_INTSTA	32	DMA channel 25 interrupt status
A0021020	VDMA25_ACKINT	32	DMA channel 25 interrupt acknowledge

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Address	Name	Width (bits)	Register Function
A0021028	VDMA25_LIMITER	32	DMA channel 25 bandwidth limiter
A002102C	VDMA25_PGMADDR	32	DMA channel 25 programmable address
A0021030	VDMA25_WRPTR	32	DMA channel 25 write pointer
A0021034	VDMA25_RDPTR	32	DMA channel 25 read pointer
A0021038	VDMA25_FFCNT	32	DMA channel 25 FIFO count
A002103C	VDMA25_FFSTA	32	DMA channel 25 FIFO status
A0021040	VDMA25_ALTLEN	32	DMA channel 25 alert length
A0021044	VDMA25_FFSIZE	32	DMA channel 25 FIFO size
A0021110	VDMA26_COUNT	32	DMA channel 26 transfer count
A0021114	VDMA26_CON	32	DMA channel 26 control
A0021118	VDMA26_START	32	DMA channel 26 start register
A002111C	VDMA26_INTSTA	32	DMA channel 26 interrupt status
A0021120	VDMA26_ACKINT	32	DMA channel 26 interrupt acknowledge
A0021128	VDMA26_LIMITER	32	DMA channel 26 bandwidth limiter
A002112C	VDMA26_PGMADDR	32	DMA channel 26 programmable address
A0021130	VDMA26_WRPTR	32	DMA channel 26 write pointer
A0021134	VDMA26_RDPTR	32	DMA channel 26 read pointer
A0021138	VDMA26_FFCNT	32	DMA channel 26 FIFO count
A002113C	VDMA26_FFSTA	32	DMA channel 26 FIFO status
A0021140	VDMA26_ALTLEN	32	DMA channel 26 alert length
A0021144	VDMA26_FFSIZE	32	DMA channel 26 FIFO size
A0021210	VDMA27_COUNT	32	DMA channel 27 transfer count
A0021214	VDMA27_CON	32	DMA channel 27 control
A0021218	VDMA27_START	32	DMA channel 27 start register
A002121C	VDMA27_INTSTA	32	DMA channel 27 interrupt status
A0021220	VDMA27_ACKINT	32	DMA channel 27 interrupt acknowledge
A0021228	VDMA27_LIMITER	32	DMA channel 27 bandwidth limiter
A002122C	VDMA27_PGMADDR	32	DMA channel 27 programmable address
A0021230	VDMA27_WRPTR	32	DMA channel 27 write pointer
A0021234	VDMA27_RDPTR	32	DMA channel 27 read pointer
A0021238	VDMA27_FFCNT	32	DMA channel 27 FIFO count
A002123C	VDMA27_FFSTA	32	DMA channel 27 FIFO status
A0021240	VDMA27_ALTLEN	32	DMA channel 27 alert length
A0021244	VDMA27_FFSIZE	32	DMA channel 27 FIFO size

A0020000 DMA_GLBSTA DMA global status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IT16	RUN16	IT15	RUN15	IT14	RUN14	IT13	RUN13	IT12	RUN12	IT11	RUN11	IT10	RUN10	IT9	RUN9
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IT8	RUN8	IT7	RUN7	IT6	RUN6	IT5	RUN5	IT4	RUN4	IT3	RUN3	IT2	RUN2	IT1	RUN1

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Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	IT16	Channel 25 interrupt status
30	RUN16	Channel 25 running status
29	IT15	Channel 24 interrupt status
28	RUN15	Channel 24 running status
27	IT14	Channel 23 interrupt status
26	RUN14	Channel 23 running status
25	IT13	Channel 22 interrupt status
24	RUN13	Channel 22 running status
23	IT12	Channel 21 interrupt status
22	RUN12	Channel 21 running status
21	IT11	Channel 20 interrupt status
20	RUN11	Channel 20 running status
19	IT10	Channel 19 interrupt status
18	RUN10	Channel 19 running status
17	IT9	Channel 18 interrupt status
16	RUN9	Channel 18 running status
15	IT8	Channel 17 interrupt status
14	RUN8	Channel 17 running status
13	IT7	Channel 16 interrupt status
12	RUN7	Channel 16 running status
11	IT6	Channel 7 interrupt status
10	RUN6	Channel 7 running status
9	IT5	Channel 6 interrupt status
8	RUN5	Channel 6 running status
7	IT4	Channel 5 interrupt status
6	RUN4	Channel 5 running status
5	IT3	Channel 4 interrupt status
4	RUN3	Channel 4 running status
3	IT2	Channel 2 interrupt status
2	RUN2	Channel 2 running status
1	IT1	Channel 1 interrupt status
0	RUN1	Channel 1 running status

A0020004 DMA_GLBSTA2 DMA global status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													IT18	RUN18	IT17	RUN17
Type													RO	RO	RO	RO
Reset													0	0	0	0

Bit(s)	Name	Description
3	IT18	Channel 27 interrupt status
2	RUN18	Channel 27 running status
1	IT17	Channel 26 interrupt status
0	RUN17	Channel 26 running status

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A0020008 DMA_GLB_CPU0_CFG DMA top hierarchy interrupt configuration 0003FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CPU0_CFG18	CPU0_CFG17
Type															RO	RO
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPU0_CFG16	CPU0_CFG15	CPU0_CFG14	CPU0_CFG13	CPU0_CFG12	CPU0_CFG11	CPU0_CFG10	CPU0_CFG9	CPU0_CFG8	CPU0_CFG7	CPU0_CFG6	CPU0_CFG5	CPU0_CFG4	CPU0_CFG3	CPU0_CFG2	CPU0_CFG1
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
17	CPU0_CFG18	Channel 27 CPU0 interrupt enable configure
16	CPU0_CFG17	Channel 26 CPU0 interrupt enable configure
15	CPU0_CFG16	Channel 25 CPU0 interrupt enable configure
14	CPU0_CFG15	Channel 24 CPU0 interrupt enable configure
13	CPU0_CFG14	Channel 23 CPU0 interrupt enable configure
12	CPU0_CFG13	Channel 22 CPU0 interrupt enable configure
11	CPU0_CFG12	Channel 21 CPU0 interrupt enable configure
10	CPU0_CFG11	Channel 20 CPU0 interrupt enable configure
9	CPU0_CFG10	Channel 19 CPU0 interrupt enable configure
8	CPU0_CFG9	Channel 18 CPU0 interrupt enable configure
7	CPU0_CFG8	Channel 17 CPU0 interrupt enable configure
6	CPU0_CFG7	Channel 16 CPU0 interrupt enable configure
5	CPU0_CFG6	Channel 7 CPU0 interrupt enable configure
4	CPU0_CFG5	Channel 6 CPU0 interrupt enable configure
3	CPU0_CFG4	Channel 5 CPU0 interrupt enable configure
2	CPU0_CFG3	Channel 4 CPU0 interrupt enable configure
1	CPU0_CFG2	Channel 2 CPU0 interrupt enable configure
0	CPU0_CFG1	Channel 1 CPU0 interrupt enable configure

A002000C DMA_GLB_CPU0_SET DMA top hierarchy interrupt set 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CPU0_SET18	CPU0_SET17
Type															WO	WO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPU0_SET16	CPU0_SET15	CPU0_SET14	CPU0_SET13	CPU0_SET12	CPU0_SET11	CPU0_SET10	CPU0_SET9	CPU0_SET8	CPU0_SET7	CPU0_SET6	CPU0_SET5	CPU0_SET4	CPU0_SET3	CPU0_SET2	CPU0_SET1
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
17	CPU0_SET18	Channel 27 CPU0 interrupt enable set
16	CPU0_SET17	Channel 26 CPU0 interrupt enable set
15	CPU0_SET16	Channel 25 CPU0 interrupt enable set
14	CPU0_SET15	Channel 24 CPU0 interrupt enable set
13	CPU0_SET14	Channel 23 CPU0 interrupt enable set
12	CPU0_SET13	Channel 22 CPU0 interrupt enable set
11	CPU0_SET12	Channel 21 CPU0 interrupt enable set
10	CPU0_SET11	Channel 20 CPU0 interrupt enable set
9	CPU0_SET10	Channel 19 CPU0 interrupt enable set
8	CPU0_SET9	Channel 18 CPU0 interrupt enable set
7	CPU0_SET8	Channel 17 CPU0 interrupt enable set
6	CPU0_SET7	Channel 16 CPU0 interrupt enable set
5	CPU0_SET6	Channel 7 CPU0 interrupt enable set
4	CPU0_SET5	Channel 6 CPU0 interrupt enable set
3	CPU0_SET4	Channel 5 CPU0 interrupt enable set
2	CPU0_SET3	Channel 4 CPU0 interrupt enable set
1	CPU0_SET2	Channel 2 CPU0 interrupt enable set
0	CPU0_SET1	Channel 1 CPU0 interrupt enable set

A0020010 DMA_GLB_CPU0_CLR DMA top hierarchy interrupt clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															CPU0_CLR18	CPU0_CLR17
Type															WO	WO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPU0_CLR16	CPU0_CLR15	CPU0_CLR14	CPU0_CLR13	CPU0_CLR12	CPU0_CLR11	CPU0_CLR10	CPU0_CLR9	CPU0_CLR8	CPU0_CLR7	CPU0_CLR6	CPU0_CLR5	CPU0_CLR4	CPU0_CLR3	CPU0_CLR2	CPU0_CLR1
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	CPU0_CLR18	Channel 27 CPU0 interrupt enable clear
16	CPU0_CLR17	Channel 26 CPU0 interrupt enable clear
15	CPU0_CLR16	Channel 25 CPU0 interrupt enable clear
14	CPU0_CLR15	Channel 24 CPU0 interrupt enable clear
13	CPU0_CLR14	Channel 23 CPU0 interrupt enable clear
12	CPU0_CLR13	Channel 22 CPU0 interrupt enable clear
11	CPU0_CLR12	Channel 21 CPU0 interrupt enable clear
10	CPU0_CLR11	Channel 20 CPU0 interrupt enable clear
9	CPU0_CLR10	Channel 19 CPU0 interrupt enable clear
8	CPU0_CLR9	Channel 18 CPU0 interrupt enable clear
7	CPU0_CLR8	Channel 17 CPU0 interrupt enable clear
6	CPU0_CLR7	Channel 16 CPU0 interrupt enable clear
5	CPU0_CLR6	Channel 7 CPU0 interrupt enable clear
4	CPU0_CLR5	Channel 6 CPU0 interrupt enable clear
3	CPU0_CLR4	Channel 5 CPU0 interrupt enable clear
2	CPU0_CLR3	Channel 4 CPU0 interrupt enable clear
1	CPU0_CLR2	Channel 2 CPU0 interrupt enable clear
0	CPU0_CLR1	Channel 1 CPU0 interrupt enable clear

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Bit(s)	Name	Description

A0020028 DMA_GLBLIMITER DMA global bandwidth limiter register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LIMITER							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	LIMITER	**Utilization suppression** This register suppresses the bus utilization of the DMA channel. From 0 to 255. 0 means no limitation, 255 means totally banned. All other values indicate bus access permission for every (4 x n) AHB clock.

A0020020 DMA_GLB_SWRST DMA global software reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SW_RESET
Type																RO
Reset																0

Bit(s)	Name	Description
0	SW_RESET	**Software reset** Write 1 to the register to reset

A0020040 DMA_GLB_BUSY DMA global busy status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															RUN18	RUN17
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RUN1	RUN15	RUN1	RUN13	RUN12	RUN11	RUN1	RUN9	RUN8	RUN7	RUN6	RUN5	RUN4	RUN3	RUN2	RUN1

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	6		4				0									
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	RUN18	Channel 27 running status
16	RUN17	Channel 26 running status
15	RUN16	Channel 25 running status
14	RUN15	Channel 24 running status
13	RUN14	Channel 23 running status
12	RUN13	Channel 22 running status
11	RUN12	Channel 21 running status
10	RUN11	Channel 20 running status
9	RUN10	Channel 19 running status
8	RUN9	Channel 18 running status
7	RUN8	Channel 17 running status
6	RUN7	Channel 16 running status
5	RUN6	Channel 7 running status
4	RUN5	Channel 6 running status
3	RUN4	Channel 5 running status
2	RUN3	Channel 4 running status
1	RUN2	Channel 2 running status
0	RUN1	Channel 1 running status

A0020044 DMA_GLB_INTR DMA global interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**IT18**	**IT17**
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**IT16**	**IT15**	**IT14**	**IT13**	**IT12**	**IT11**	**IT10**	**IT9**	**IT8**	**IT7**	**IT6**	**IT5**	**IT4**	**IT3**	**IT2**	**IT1**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	IT18	Channel 27 interrupt status
16	IT17	Channel 26 interrupt status
15	IT16	Channel 25 interrupt status
14	IT15	Channel 24 interrupt status
13	IT14	Channel 23 interrupt status
12	IT13	Channel 22 interrupt status
11	IT12	Channel 21 interrupt status
10	IT11	Channel 20 interrupt status
9	IT10	Channel 19 interrupt status
8	IT9	Channel 18 interrupt status
7	IT8	Channel 17 interrupt status
6	IT7	Channel 16 interrupt status
5	IT6	Channel 7 interrupt status
4	IT5	Channel 6 interrupt status
3	IT4	Channel 5 interrupt status
2	IT3	Channel 4 interrupt status
1	IT2	Channel 2 interrupt status
0	IT1	Channel 1 interrupt status

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A0020100 GDMA1_SRC DMA channel 1 source address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SRC															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SRC	**GDMA source address** This register contains the base or current source address that the DMA channel is operating on. • Writing into this register specifies the base address of the transfer source for a DMA channel. • Reading this register will return the address value from which the DMA is reading.

A0020104 GDMA1_DST DMA channel 1 destination address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DST															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	DST	**GDMA destination address** This register contains the base or current destination address that the DMA channel is operating on. • Writing into this register specifies the base address of the transfer destination for a DMA channel. • Reading this register will return the address value to which the DMA is writing.

A0020108 GDMA1_WPPT DMA channel 1 wrap point address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam																

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e																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WPPT	**Transfer counts before jump** This register specifies the transfer count required to perform before the jump point. This can be used to support ring buffer or double buffer memory access. To enable the wrap function, two control bits, WPEN and WPSD in the DMA control register must be programmed. If the transfer counter in the DMA engine matches this value, an address jump will occur, and the next address will be the address specified in GDMAn_WPTO. To enable this function, set up WPEN in GDMAn_CON. Note: The total size of data specified in the wrap point count in a DMA channel is determined by WPPT together with SIZE in GDMAn_CON, such as WPPT x SIZE.

A002010C GDMA1_WPTO DMA channel 1 wrap to address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WPTO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPTO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WPTO	**Jump address** This register specifies the destination address of a given DMA transfer to support ring buffer or double buffer memory access. To enable the wrap function, set the two control bits, WPEN and WPSD in the DMA control register.

A0020110 GDMA1_COUNT DMA channel 1 transfer count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNT															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	COUNT	**Total transfer counts** This register specifies the total transfer counts of the DMA channel required to perform. Upon completion, the DMA channel generates an interrupt request to the processor while ITEN in GDMAn_CON is set to 1. Note, that the total size of transferred data is determined by LEN and SIZE in GDMAn_CON, such as LEN x SIZE.

A0020114 GDMA1_CON DMA channel 1 control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								ITEN					SETTING			
Type								RW					RW			
Reset								0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SIZE						DIRECTION			
Type							RW						RW			
Reset							0	0					0	0	0	0

Bit(s)	Name	Description
24	ITEN	**Enable DMA transfer completion interrupt.** 0: Disable 1: Enable
19:16	SETTING	**[16] Throttle and handshake control for DMA transfer** The DMA master is able to throttle down the transfer rate by the request-grant handshake process. [19:18] Transfer type The burst-type transfers have better bus efficiency. Apply this type for larger data movement. Note, that the burst-type transfer will not stop until all of the beats in a burst are complete or the transfer length is reached. The transfer type is restricted by SIZE. If SIZE is 00b, i.e. byte transfer, all four transfer types can be used. If SIZE is 01b (half-word transfer), 16-beat incremental burst cannot be used. If SIZE is 10b, i.e. word transfer, only single and 4-beat incremental burst can be used. [16]DREQ: 0=No throttle control during DMA transfer or transfers occurred only between memories; 1=Hardware handshake management [19:18]BURST: 00=Single; 01=Reserved; 10=4-beat incrementing burst; 11=Reserved;
9:8	SIZE	**Data size of a bus cycle per transfer.** These bits confine the data transfer size between the source and destination to the specified value for individual bus cycle. The size is in bytes and the maximum value is 4 bytes. It is mainly determined by the data width of a DMA master. 00: Byte transfer/1 byte 01: Half-word transfer/2 bytes 10: Word transfer/4 bytes 11: Reserved

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Bit(s)	Name	Description
3:0	DIRECTION	**[0] Incremental source address** The source addresses increments after each transfer. If SIZE is in bytes, the source address will increase by 1, if it is in half-word, it will increase by 2 and if word, increase by 4. [1] Incremental destination address The destination address increments after each transfer. If SIZE is in bytes, the destination address will increase by 1, if it is in half-word, it will increase by 2 and if word, increase by 4. [2] Wrap select The side using address-wrapping function. Only one side of a DMA channel can activate the address-wrapping function at a time. [3] Wrap enable Address-wrapping for ring buffer and double buffer. The next address of DMA jumps to WRAP TO address when the current address matches WRAP POINT count. [0]SINC:0=Disable; 1=Enable [1]DINC:0=Disable; 1=Enable [2]WPSD: 0=Address-wrapping on source; 1=Address-wrapping on destination [3]WPEN: 0=Disable; 1=Enable

A0020118 GDMA1_START DMA channel 1 start 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR															
Type	RW															
Reset	0															

Bit(s)	Name	Description
15	STR	**Start control for a DMA channel** This register controls the activity of a DMA channel. Note: prior to setting STR to 1, all the register settings should be configured. Once STR is set to 1, the hardware will not clear it automatically no matter whether the DMA channel accomplishes the DMA transfer or not. In other words, the value of STR stays at 1 regardless of the completion of the DMA transfer. Therefore, the software program should reset STR to 0 before restarting another DMA transfer. If this bit is cleared to 0 when DMA transfer is active, the software should poll RUNn in DMA_GLBSTA after this bit is cleared to ensure the current DMA transfer is terminated by the DMA engine. 0: The DMA channel is stopped. 1: The DMA channel is started and running.

A002011C GDMA1_INTSTA DMA channel 1 interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**INT**															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	INT	**Interrupt status for DMA channel** 0: No interrupt request is generated. 1: One interrupt request is pending and waiting for service.

A0020120 GDMA1_ACKINT DMA channel 1 interrupt acknowledge 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**ACK**															
Type	WO															
Reset	0															

Bit(s)	Name	Description
15	ACK	**Interrupt acknowledge for the DMA channel** 0: No effect 1: Interrupt request is acknowledged and should be relinquished.

A0020124 GDMA1_RLCT DMA channel 1 remaining length of current transfer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RLCT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RLCT	**This register is to reflect the left count of the transfer.** Note, that this value is the transfer count, not the transfer data size.

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A0020128 GDMA1_LIMITER DMA channel 1 bandwidth limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LIMITER							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	LIMITER	**Utilization suppression** This register suppresses the bus utilization of the DMA channel. From 0 to 255. 0 means no limitation, 255 means totally banned, and others indicate bus access permission for every (4 x n) AHB clock.

A0020308 PDMA4_WPPT DMA channel 4 wrap point address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPPT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WPPT	**Transfer counts before jump** This register specifies the transfer count required to perform before the jump point. This can be used to support ring buffer or double buffer memory access. To enable the wrap function, two control bits, WPEN and WPSD in the DMA control register must be programmed. If the transfer counter in the DMA engine matches this value, an address jump will occur, and the next address will be the address specified in GDMAn_WPTO. To enable this function, set WPEN in GDMAn_CON. Note, that the total size of data specified in the wrap point count in a DMA channel is determined by WPPT together with SIZE in GDMAn_CON, such as WPPT x SIZE.

A002030C PDMA4_WPTO DMA channel 4 wrap to address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WPTO															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WPTO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WPTO	**Jump address** This register specifies the address of jump destination of a given DMA transfer to support ring buffer or double buffer memory access. To enable this function, set the two control bits, WPEN and WPSD in the DMA control register.

A0020310 PDMA4_COUNT DMA channel 4 transfer count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	COUNT	**Total transfer counts** This register specifies the total transfer counts of the DMA channel is required to perform. Upon completion, the DMA channel generates an interrupt request to the processor while ITEN in GDMAn_CON is set to 1. Note that the total size of transferred data is determined by LEN and SIZE in GDMAn_CON, such as LEN x SIZE.

A0020314 PDMA4_CON DMA channel 4 control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								ITEN					SETTING			
Type								RW					RW			
Reset								0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SIZE					DIRECTION				
Type							RW					RW				
Reset							0	0				0	0	0	0	0

Bit(s)	Name	Description
24	ITEN	**Enable DMA transfer completion interrupt**

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Bit(s)	Name	Description
		0: Disable 1: Enable
19:16	SETTING	**[16] Throttle and handshake control for DMA transfer** The DMA master is able to throttle down the transfer rate by the request-grant handshake process. [17]Byte to word Word to byte or byte to word transfer for the applications of transferring non-word-aligned-address data to word-aligned-address data. Note, that to enable this function BURST should be set to 4-beat burst and the SIZE to byte. [19:18] Transfer type The burst-type transfers have better bus efficiency. Apply this type for mass data movement. Note, that the burst-type transfer will not stop until all of the beats in a burst are complete or the transfer length is reached. The transfer type is restricted by SIZE. If SIZE is 00b, i.e. byte transfer, all four transfer types can be used. If SIZE is 01b (half-word transfer), 16-beat incremental burst cannot be used. If SIZE is 10b, i.e. word transfer, only single and 4-beat incremental burst can be used. [16]DREQ: 0=No throttle control during DMA transfer or transfers occurred only between memories; 1=Hardware handshake management [17]B2W: 0=Disable; 1=Enable [19:18]BURST: 00=Single; 01=Reserved; 10=4-beat incrementing burst; 11=Reserved;
9:8	SIZE	**Data size of a bus cycle per transfer.** These bits confine the data transfer size between the source and destination to the specified value for individual bus cycle. The size is in bytes and the maximum value is 4 bytes. It is mainly decided by the data width of a DMA master. 00: Byte transfer/1 byte 01: Half-word transfer/2 bytes 10: Word transfer/4 bytes 11: Reserved
4:0	DIRECTION	**[0] Incremental source address** The source addresses increment after each transfer. If SIZE is in bytes, the source address will increase by 1, if it is in half-word, it will increase by 2 and if word, increase by 4. [1] Incremental destination address The destination address increments after each transfer. If SIZE is in bytes, the destination address will increase by 1, if it is in half-word, it will increase by 2 and if word, increase by 4. [2] Wrap select The side using address-wrapping function. Only one side of a DMA channel can activate the address-wrapping function at a time. [3] Wrap enable Address-wrapping for ring buffer and double buffer. The next address of DMA jumps to WRAP TO address when the current address matches WRAP POINT count. [0]SINC:0=Disable; 1=Enable [1]DINC:0=Disable; 1=Enable [2]WPSD: 0=Address-wrapping on source; 1=Address-wrapping on destination [3]WPEN: 0=Disable; 1=Enable [4]DIR: 0=peripheral TX; 1=peripheral RX

A0020318 PDMA4_START DMA channel 4 start 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR															
Type	RW															
Reset	0															

Bit(s)	Name	Description
15	STR	**Start control for a DMA channel** This register controls the activity of a DMA channel. Note that prior to setting STR to 1, all the register settings should be configured. Once STR is set to 1, the hardware will not clear it automatically no matter whether the DMA channel accomplishes the DMA transfer or not. In other words, the value of STR stays at 1 regardless of the completion of the DMA transfer. Therefore, the software program should reset STR to 0 before restarting another DMA transfer. If this bit is cleared to 0 when DMA transfer is active, the software should poll RUNn in DMA_GLBSTA after this bit is cleared to ensure the current DMA transfer is terminated by the DMA engine. 0: The DMA channel has stopped. 1: The DMA channel is in use.

A002031C PDMA4_INTSTA DMA channel 4 interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	INT	**Interrupt status for DMA channel** 0: No interrupt request is generated. 1: One interrupt request is pending and waiting for service.

A0020320 PDMA4_ACKINT DMA channel 4 interrupt acknowledge 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	**ACK**															
Type	WO															
Reset	0															

Bit(s)	Name	Description
15	ACK	**Interrupt acknowledge for the DMA channel** 0: No effect 1: Interrupt request is acknowledged and should be relinquished.

A0020324 PDMA4_RLCT DMA channel 4 remaining length of current transfer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RLCT**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	RLCT	**This register is to reflect the remaining length of current transfer (RLCT).** Note, that this value is transfer count, not the transfer data size.

A0020328 PDMA4_LIMITER DMA channel 4 bandwidth limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**LIMITER**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	LIMITER	**Utilization suppression** This register suppresses the bus utilization of the DMA channel. From 0 to 255. 0 means no limitation, 255 means totally banned, and others indicate bus access permission for every (4 x n) AHB clock.

A002032C PDMA4_PGMADDR DMA channel 4 programmable address 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PGMADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGMADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PGMADDR	**PDMA programmable address.** The above registers specify the address for a half-size DMA channel. This address represents the source address if DIR in DMA_CON is set to 0 and represents the destination address if DIR in PDMAn_CON is set to 1.

A0020710 VDMA16_COUNT DMA channel 16 transfer count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	COUNT	**FIFO threshold** For virtual FIFO DMA, this register is used to configure the RX threshold and TX threshold. The interrupt is triggered when FIFO count is larger than or equal to RX threshold in RX path or FIFO count is less than or equal to TX threshold in TX path. Note, that the ITEN bit in the VDMAn_CON register shall be set or no interrupt will be issued (n is from 1 to 16).

A0020714 VDMA16_CON DMA channel 16 control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								ITEN								DREQ
Type								RW								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SIZE					DIRECTION				
Type							RW					RW				

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Reset							0	0				0	0	0	0	0

Bit(s)	Name	Description
24	ITEN	**Enable DMA transfer completion interrupt** 0: Disable 1: Enable
16	DREQ	**Throttle and handshake control for DMA transfer.** The DMA master is able to throttle down the transfer rate by request-grant handshake. 0: No throttle control during DMA transfer or transfers occurred only between memories 1: Hardware handshake management
9:8	SIZE	**Data size of a bus cycle per transfer.** These bits confine the data transfer size between the source and destination to the specified value for individual bus cycle. The size is in terms of byte, and the maximum value is 4 bytes. It is mainly decided by the data width of a DMA master. 00: Byte transfer/1 byte 01: Half-word transfer/2 bytes 10: Word transfer/4 bytes 11: Reserved
4:0	DIRECTION	**[4]Directions of VDMA transfer** The direction is from the perspective of the DMA masters. WRITE means reading from master and then writing to the address specified in VDMAn_PGMADDR, and vice versa. No effect on channel 1. [4]DIR: 0=peripheral TX; 1=peripheral RX

A0020718 VDMA16_START DMA channel 16 start register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STR															
Type	RW															
Reset	0															

Bit(s)	Name	Description
15	STR	**Start control for a DMA channel** This register controls the activity of a DMA channel. Note, that prior to setting STR to 1, all the register settings should be configured. Once STR is set to 1, the hardware will not clear it automatically no matter the DMA channel accomplished DMA transfer or not. In other words, the value of STR stays at 1 regardless of the completion of the DMA transfer. Therefore, the software program should reset STR to 0 before restarting another DMA transfer. If this bit is cleared to 0 when DMA transfer is active, the software should poll RUNn in DMA_GLBSTA after this bit is cleared to ensure the current DMA transfer is terminated by the DMA engine. 0: The DMA channel has stopped. 1: The DMA channel is in use.

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Bit(s)	Name	Description

A002071C VDMA16_INTSTA DMA channel 16 interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INT															
Type	RO															
Reset	0															

Bit(s)	Name	Description
15	INT	**Interrupt status for DMA channel** 0: No interrupt request is generated. 1: One interrupt request is pending and waiting for service.

A0020720 VDMA16_ACKINT DMA channel 16 interrupt acknowledge 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACK															
Type	WO															
Reset	0															

Bit(s)	Name	Description
15	ACK	**Interrupt acknowledge for the DMA channel** 0: No effect 1: Interrupt request is acknowledged and should be relinquished.

A0020728 VDMA16_LIMITER DMA channel 16 bandwidth limiter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LIMITER							
Type									RW							

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Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	LIMITER	**Utilization suppression** This register suppresses the bus utilization of the DMA channel. From 0 to 255. 0 means no limitation, 255 means totally banned, and others indicate request for bus access permission for every (4 x n) AHB clock.

A002072C VDMA16_PGMADDR DMA channel 16 programmable address 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PGMADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PGMADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	PGMADDR	**VDMA programmable address.** Specifies the address for a half-size DMA channel. This address represents the source address if DIR in DMA_CON is set to 0 and represents the destination address if DIR in VDMAn_CON is set to 1.

A0020730 VDMA16_WRPTR DMA channel 16 write pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WRPTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WRPTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WRPTR	**Virtual FIFO write pointer**

A0020734 VDMA16_RDPTR DMA channel 16 read pointer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDPTR															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDPTR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RDPTR	**Virtual FIFO read pointer**

A0020738 VDMA16_FFCNT DMA channel 16 FIFO count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFCNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FFCNT	**Displays the number of data stored in FIFO.** 0 means FIFO is empty, and FIFO is full if FFCNT is equal to FFSIZE.

A002073C VDMA16_FFSTA DMA channel 16 FIFO status 00000007

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														ALT	EMPTY	FULL
Type														RO	RO	RO
Reset														1	1	1

Bit(s)	Name	Description
2	ALT	**Indicates FIFO count is larger than ALTLEN.** DMA issues an alert signal to UART/BRIF to enable UART, I2S, USB flow control. 0: Didn't reach alert region 1: Reached alert region
1	EMPTY	**Indicates FIFO is empty** 0: Not empty 1: Empty

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Bit(s)	Name	Description
0	FULL	**Indicates FIFO is full** 0: Not full 1: Full

A0020740 VDMA16_ALTLEN DMA channel 16 alert length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ALTLEN					
Type											RW					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	ALTLEN	**Specifies the alert length of virtual FIFO DMA.** Once the remaining FIFO space is less than ALTLEN, an alert signal will be issued to UART/BRIF to enable the flow control. Normally, ALTLEN is more than 16 bytes for UART application.

A0020744 VDMA16_FFSIZE DMA channel 16 FIFO size 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FFSIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	FFSIZE	**Specifies the FIFO size of virtual FIFO DMA.**

5.6.2. DMA_Sensor register map

Module name: DMA_SENSOR Base address: (+a0150000h)

Address	Name	Width (bits)	Register Function
A0150000	DMA_GLBSTA	32	**DMA global status**
A0150008	DMA_GLB_CPU0_CFG	32	**DMA top hierarchy interrupt configuration**
A015000C	DMA_GLB_CPU0_SET	32	**DMA top hierarchy interrupt set**

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Address	Name	Width (bits)	Register Function
A0150010	DMA_GLB_CPU0_CLR	32	DMA top hierarchy interrupt clear
A0150028	DMA_GLBLIMITER	32	DMA global bandwidth limiter register
A0150030	DMA_GLB_DBG	32	DMA current chosen channel
A0150020	DMA_GLB_SWRST	32	DMA global software reset
A0150040	DMA_GLB_BUSY	32	DMA global busy status
A0150044	DMA_GLB_INTR	32	DMA global interrupt status
A0150100	GDMA3_SRC	32	DMA channel 3 source address
A0150104	GDMA3_DST	32	DMA channel 3 destination address
A0150108	GDMA3_WPPT	32	DMA channel 3 wrap point address
A015010C	GDMA3_WPTO	32	DMA channel 3 wrap to address
A0150110	GDMA3_COUNT	32	DMA channel 3 transfer count
A0150114	GDMA3_CON	32	DMA channel 3 control
A0150118	GDMA3_START	32	DMA channel 3 start
A015011C	GDMA3_INTSTA	32	DMA channel 3 interrupt status
A0150120	GDMA3_ACKINT	32	DMA channel 3 interrupt acknowledge
A0150124	GDMA3_RLCT	32	DMA channel 3 remaining length of current transfer
A0150128	GDMA3_LIMITER	32	DMA channel 3 bandwidth limiter
A0150208	PDMA8_WPPT	32	DMA channel 8 wrap point address
A015020C	PDMA8_WPTO	32	DMA channel 8 wrap to address
A0150210	PDMA8_COUNT	32	DMA channel 8 transfer count
A0150214	PDMA8_CON	32	DMA channel 8 control
A0150218	PDMA8_START	32	DMA channel 8 start
A015021C	PDMA8_INTSTA	32	DMA channel 8 interrupt status
A0150220	PDMA8_ACKINT	32	DMA channel 8 interrupt acknowledge
A0150224	PDMA8_RLCT	32	DMA channel 8 remaining length of current transfer
A0150228	PDMA8_LIMITER	32	DMA channel 8 bandwidth limiter
A015022C	PDMA8_PGMADDR	32	DMA channel 8 programmable address
A0150308	PDMA9_WPPT	32	DMA channel 9 wrap point address
A015030C	PDMA9_WPTO	32	DMA channel 9 wrap to address
A0150310	PDMA9_COUNT	32	DMA channel 9 transfer count
A0150314	PDMA9_CON	32	DMA channel 9 control
A0150318	PDMA9_START	32	DMA channel 9 start
A015031C	PDMA9_INTSTA	32	DMA channel 9 interrupt status
A0150320	PDMA9_ACKINT	32	DMA channel 9 interrupt acknowledge
A0150324	PDMA9_RLCT	32	DMA channel 9 remaining length of current transfer
A0150328	PDMA9_LIMITER	32	DMA channel 9 bandwidth limiter
A015032C	PDMA9_PGMADDR	32	DMA channel 9 programmable address
A0150408	PDMA10_WPPT	32	DMA channel 10 wrap point address
A015040C	PDMA10_WPTO	32	DMA channel 10 wrap to address
A0150410	PDMA10_COUNT	32	DMA channel 10 transfer count
A0150414	PDMA10_CON	32	DMA channel 10 control
A0150418	PDMA10_START	32	DMA channel 10 start

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Address	Name	Width (bits)	Register Function
A015041C	PDMA10_INTSTA	32	DMA channel 10 interrupt status
A0150420	PDMA10_ACKINT	32	DMA channel 10 interrupt acknowledge
A0150424	PDMA10_RLCT	32	DMA channel 10 remaining length of current transfer
A0150428	PDMA10_LIMITER	32	DMA channel 10 bandwidth limiter
A015042C	PDMA10_PGMADDR	32	DMA channel 10 programmable address
A0150508	PDMA11_WPPT	32	DMA channel 11 wrap point address
A015050C	PDMA11_WPTO	32	DMA channel 11 wrap to address
A0150510	PDMA11_COUNT	32	DMA channel 11 transfer count
A0150514	PDMA11_CON	32	DMA channel 11 control
A0150518	PDMA11_START	32	DMA channel 11 start
A015051C	PDMA11_INTSTA	32	DMA channel 11 interrupt status
A0150520	PDMA11_ACKINT	32	DMA channel 11 interrupt acknowledge
A0150524	PDMA11_RLCT	32	DMA channel 11 remaining length of current transfer
A0150528	PDMA11_LIMITER	32	DMA channel 11 bandwidth limiter
A015052C	PDMA11_PGMADDR	32	DMA channel 11 programmable address
A0150608	PDMA12_WPPT	32	DMA channel 12 wrap point address
A015060C	PDMA12_WPTO	32	DMA channel 12 wrap to address
A0150610	PDMA12_COUNT	32	DMA channel 12 transfer count
A0150614	PDMA12_CON	32	DMA channel 12 control
A0150618	PDMA12_START	32	DMA channel 12 start
A015061C	PDMA12_INTSTA	32	DMA channel 12 interrupt status
A0150620	PDMA12_ACKINT	32	DMA channel 12 interrupt acknowledge
A0150624	PDMA12_RLCT	32	DMA channel 12 remaining length of current transfer
A0150628	PDMA12_LIMITER	32	DMA channel 12 bandwidth limiter
A015062C	PDMA12_PGMADDR	32	DMA channel 12 programmable address
A0150708	PDMA13_WPPT	32	DMA channel 13 wrap point address
A015070C	PDMA13_WPTO	32	DMA channel 13 wrap to address
A0150710	PDMA13_COUNT	32	DMA channel 13 transfer count
A0150714	PDMA13_CON	32	DMA channel 13 control
A0150718	PDMA13_START	32	DMA channel 13 start
A015071C	PDMA13_INTSTA	32	DMA channel 13 interrupt status
A0150720	PDMA13_ACKINT	32	DMA channel 13 interrupt acknowledge
A0150724	PDMA13_RLCT	32	DMA channel 13 remaining length of current transfer
A0150728	PDMA13_LIMITER	32	DMA channel 13 bandwidth limiter
A015072C	PDMA13_PGMADDR	32	DMA channel 13 programmable address
A0150808	PDMA14_WPPT	32	DMA channel 14 wrap point address
A015080C	PDMA14_WPTO	32	DMA channel 14 wrap to address
A0150810	PDMA14_COUNT	32	DMA channel 14 transfer count
A0150814	PDMA14_CON	32	DMA channel 14 control
A0150818	PDMA14_START	32	DMA channel 14 start
A015081C	PDMA14_INTSTA	32	DMA channel 14 interrupt status
A0150820	PDMA14_ACKINT	32	DMA channel 14 interrupt acknowledge

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Address	Name	Width (bits)	Register Function
A0150824	PDMA14_RLCT	32	DMA channel 14 remaining length of current transfer
A0150828	PDMA14_LIMITER	32	DMA channel 14 bandwidth limiter
A015082C	PDMA14_PGMADDR	32	DMA channel 14 programmable address
A0150908	PDMA15_WPPT	32	DMA channel 15 wrap point address
A015090C	PDMA15_WPTO	32	DMA channel 15 wrap to address
A0150910	PDMA15_COUNT	32	DMA channel 15 transfer count
A0150914	PDMA15_CON	32	DMA channel 15 control
A0150918	PDMA15_START	32	DMA channel 15 start
A015091C	PDMA15_INTSTA	32	DMA channel 15 interrupt status
A0150920	PDMA15_ACKINT	32	DMA channel 15 interrupt acknowledge
A0150924	PDMA15_RLCT	32	DMA channel 15 remaining length of current transfer
A0150928	PDMA15_LIMITER	32	DMA channel 15 bandwidth limiter
A015092C	PDMA15_PGMADDR	32	DMA channel 15 programmable address

A0150000 DMA_GLBSTA DMA global status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															IT9	RUN9
Type															RO	RO
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IT8	RUN8	IT7	RUN7	IT6	RUN6	IT5	RUN5	IT4	RUN4	IT3	RUN3	IT2	RUN2	IT1	RUN1
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	IT9	channel 15 interrupt status
16	RUN9	channel 15 running status
15	IT8	Channel 14 interrupt status
14	RUN8	Channel 14 running status
13	IT7	Channel 13 interrupt status
12	RUN7	Channel 13 running status
11	IT6	Channel 12 interrupt status
10	RUN6	Channel 12 running status
9	IT5	Channel 11 interrupt status
8	RUN5	Channel 11 running status
7	IT4	Channel 10 interrupt status
6	RUN4	Channel 10 running status
5	IT3	Channel 9 interrupt status
4	RUN3	Channel 9 running status
3	IT2	Channel 8 interrupt status
2	RUN2	Channel 8 running status
1	IT1	Channel 3 interrupt status
0	RUN1	Channel 3 running status

A0150008 DMA_GLB_CPU0_CFG DMA top hierarchy interrupt 000001FF

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configuration

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CPU0_CFG9	CPU0_CFG8	CPU0_CFG7	CPU0_CFG6	CPU0_CFG5	CPU0_CFG4	CPU0_CFG3	CPU0_CFG2	CPU0_CFG1
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	CPU0_CFG9	Channel 15 CPU0 interrupt enable configure
7	CPU0_CFG8	Channel 14 CPU0 interrupt enable configure
6	CPU0_CFG7	Channel 13 CPU0 interrupt enable configure
5	CPU0_CFG6	Channel 12 CPU0 interrupt enable configure
4	CPU0_CFG5	Channel 11 CPU0 interrupt enable configure
3	CPU0_CFG4	Channel 10 CPU0 interrupt enable configure
2	CPU0_CFG3	Channel 9 CPU0 interrupt enable configure
1	CPU0_CFG2	Channel 8 CPU0 interrupt enable configure
0	CPU0_CFG1	Channel 3 CPU0 interrupt enable configure

A015000C DMA_GLB_CPU0_SET DMA top hierarchy interrupt set 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CPU0_SET9	CPU0_SET8	CPU0_SET7	CPU0_SET6	CPU0_SET5	CPU0_SET4	CPU0_SET3	CPU0_SET2	CPU0_SET1
Type								WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	CPU0_SET9	Channel 15 CPU0 interrupt enable set
7	CPU0_SET8	Channel 14 CPU0 interrupt enable set
6	CPU0_SET7	Channel 13 CPU0 interrupt enable set
5	CPU0_SET6	Channel 12 CPU0 interrupt enable set
4	CPU0_SET5	Channel 11 CPU0 interrupt enable set
3	CPU0_SET4	Channel 10 CPU0 interrupt enable set
2	CPU0_SET3	Channel 9 CPU0 interrupt enable set
1	CPU0_SET2	Channel 8 CPU0 interrupt enable set
0	CPU0_SET1	Channel 3 CPU0 interrupt enable set

A0150010 DMA_GLB_CPU0_CLR DMA top hierarchy interrupt clear 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								CPU0_CLR9	CPU0_CLR8	CPU0_CLR7	CPU0_CLR6	CPU0_CLR5	CPU0_CLR4	CPU0_CLR3	CPU0_CLR2	CPU0_CLR1
Type								WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	CPU0_CLR9	Channel 15 CPU0 interrupt enable clear
7	CPU0_CLR8	Channel 14 CPU0 interrupt enable clear
6	CPU0_CLR7	Channel 13 CPU0 interrupt enable clear
5	CPU0_CLR6	Channel 12 CPU0 interrupt enable clear
4	CPU0_CLR5	Channel 11 CPU0 interrupt enable clear
3	CPU0_CLR4	Channel 10 CPU0 interrupt enable clear
2	CPU0_CLR3	Channel 9 CPU0 interrupt enable clear
1	CPU0_CLR2	Channel 8 CPU0 interrupt enable clear
0	CPU0_CLR1	Channel 3 CPU0 interrupt enable clear

A0150028 DMA_GLBLIMITER DMA global bandwidth limiter register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LIMITER							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	LIMITER	**Utilization Suppression** This register suppresses the bus utilization of the DMA channel. From 0 to 255. 0 means no limitation, 255 means totally banned, and others indicate bus access permission for every (4 x n) AHB clock.

A0150030 DMA_GLB_DBG DMA current chosen channel 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CC															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	CC															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CC	This register is only reserved for debugging. This signal indicates the current channel.

A0150020 DMA_GLB_SWRST DMA global software reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SW_RESET
Type																RW
Reset																0

Bit(s)	Name	Description
0	SW_RESET	**Software reset** Write 1 to the register to reset

A0150040 DMA_GLB_BUSY DMA global busy status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								RUN9	RUN8	RUN7	RUN6	RUN5	RUN4	RUN3	RUN2	RUN1
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	RUN9	Channel 15 running status
7	RUN8	Channel 14 running status
6	RUN7	Channel 13 running status
5	RUN6	Channel 12 running status
4	RUN5	Channel 11 running status
3	RUN4	Channel 10 running status
2	RUN3	Channel 9 running status
1	RUN2	Channel 8 running status
0	RUN1	Channel 3 running status

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A0150044 DMA_GLB_INTR DMA global interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								IT9	IT8	IT7	IT6	IT5	IT4	IT3	IT2	IT1
Type								RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	IT9	Channel 15 interrupt status
7	IT8	Channel 14 interrupt status
6	IT7	Channel 13 interrupt status
5	IT6	Channel 12 interrupt status
4	IT5	Channel 11 interrupt status
3	IT4	Channel 10 interrupt status
2	IT3	Channel 9 interrupt status
1	IT2	Channel 8 interrupt status
0	IT1	Channel 3 interrupt status

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6. External Interrupt Controller (EINT)

6.1. Overview

The external interrupt controller (EINT) consists of up to 32 edge detectors to generate event or interrupt requests. Each input line can be independently configured to select type (event or interrupt) and the corresponding trigger event (rising edge or falling edge or both, or level). Each line can also be masked independently. A pending register maintains the status line of the interrupt requests.

6.2. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 6.2-1. Abbreviations

Abbreviation	Definition
EINT	External interrupt controller
FIRQ	Fast external interrupt

6.3. Features

The EINT controller offers the following main features:

- Independent trigger and mask on each interrupt/event line
- Dedicated status bit for each interrupt line
- Generation of up to 32 software interrupt/event requests
- Fast interrupts

6.4. Block diagram

Figure 6.4-1 shows the block diagram of the EINT controller.

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Figure 6.4-1. EINT block diagram

6.5. Wakeup event management

EINT is able to handle external or internal events in order to wake up the core (WFI). The wakeup event can be generated by:

- Configuring an external or internal EINT line in event mode. When the CPU resumes from WFI, it is not necessary to clear the peripheral interrupt pending bit or the NVIC IRQ channel pending bit as the pending bit corresponding to the event line is not set.

6.6. Functions

To generate an interrupt, an interrupt line should be configured and enabled. Program two trigger registers with desired edge detection (`EINT_SENS, EINT_DUALEDGE_SENS, EINT_POL`) and enable an interrupt request by writing “1” to the corresponding bit in the interrupt mask clear register (`EINT_MASK_CLR`). When the selected trigger occurs on the external interrupt line, an interrupt request is generated. The pending bit corresponding to the interrupt line is also set in the EINT interrupt status register (`EINT_STA`). This request is reset by writing “1” in the EINT interrupt acknowledge register (`EINT_INTACK`).

To generate an event, the event line should be configured and enabled. Program three trigger registers with desired edge detection (`EINT_SENS, EINT_DUALEDGE_SENS, EINT_POL`) and enable the event request by writing “1” to the corresponding bit in the event mask clear register (`EINT_WAKEUP_MASK_CLR`). When the selected trigger occurs on the event line, an event request is generated. The pending bit corresponding to the event line is also set in the EINT wakeup event status register (`EINT_EEVT`). This request is reset by writing “1” in the EINT wakeup event acknowledge register (`EINT_EEVTACK`).

6.6.1. Hardware interrupt

To configure 32 lines as interrupt sources:

- Configure the mask bits of 32 interrupt lines (`EINT_MASK_CLR`).

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- Configure the trigger selection bits of the interrupt lines (`EINT_SENS_SET, EINT_SENS_CLR, EINT_DUALEDGE_SENS_SET, EINT_DUALEDGE_SENS_CLR, EINT_POL_SET, EINT_POL_CLR`).

Register setting / Trigger Type	EINT_SENS_SET	EINT_SENS_CLR	EINT_DUALEDGE_ SENS_SET	EINT_DUALEDGE_ SENS_CLR	EINT_POL_SET	EINT_POL_CLR
↑ (Rising Edge)	0	1	0	1	1	0
↓ (Falling Edge)	0	1	0	1	0	1
↑ ↓ (Dual Edge)	0	1	1	0	Don't care	Don't care
(High Level)	1	0	Don't care	Don't care	1	0
(Low Level)	1	0	Don't care	Don't care	0	1

- Configure the enable and mask bits that control the NVIC IRQ channel mapped to the external interrupt controller (EINT) so that an interrupt from any of the 32 lines can be correctly acknowledged.

6.6.2. Hardware events

To configure the 32 lines as event sources:

- Configure the mask bits of 32 event lines (`EINT_WAKEUP_MASK_CLR`).
- Configure the trigger selection bits of the event lines (`EINT_SENS_SET, EINT_SENS_CLR, EINT_DUALEDGE_SENS_SET, EINT_DUALEDGE_SENS_CLR, EINT_POL_SET, EINT_POL_CLR`).

6.6.3. Software interrupt

The 32 lines can be configured as software interrupt lines. To generate a software interrupt:

- Configure the mask bits of 32 interrupt lines (`EINT_MASK_CLR`).
- Set the required bit in the software interrupt register (`EINT_SOFT_SET`).

6.6.4. Fast interrupt

To configure the 32 lines as fast interrupt sources:

- Configure the mask bits of 32 interrupt lines (`FIRQ_MASK_CLR`).
- Configure the trigger selection bits of the interrupt lines (`EINT_SENS_SET, EINT_SENS_CLR, EINT_DUALEDGE_SENS_SET, EINT_DUALEDGE_SENS_CLR, EINT_POL_SET, EINT_POL_CLR`).

Register setting / Trigger Type	EINT_SENS_SET	EINT_SENS_CLR	EINT_DUALEDGE_ SENS_SET	EINT_DUALEDGE_ SENS_CLR	EINT_POL_SET	EINT_POL_CLR
↑ (Rising Edge)	0	1	0	1	1	0
↓ (Falling Edge)	0	1	0	1	0	1

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Register setting / Trigger Type	EINT_SENS_SET	EINT_SENS_CLR	EINT_DUALEDGE_SENS_SET	EINT_DUALEDGE_SENS_CLR	EINT_POL_SET	EINT_POL_CLR
↑ ↓ **(Dual Edge)**	0	1	1	0	Don't care	Don't care
⎺⎺ **(High Level)**	1	0	Don't care	Don't care	1	0
⎽⎽ **(Low Level)**	1	0	Don't care	Don't care	0	1

- Configure the enable and mask bits that control the NVIC IRQ channel mapped to the fast external interrupt (FIRQ) so that an interrupt coming from one of the 32 lines can be correctly acknowledged.

6.7. Programming guide

The fast interrupt programming flow is shown in Figure 6.7-1, using EINT4 as an example.

Figure 6.7-1. FIRQ programming flow chart

6.8. External interrupt or event line mapping

Up to 39 GPIOs are connected to the 24 external interrupt/event lines, as shown in Table 6.8-1.

Table 6.8-1. External interrupt sources

EINT	Source pin
EINT0	PAD_GPIO_23 if (GPIO23_MODE==7)
EINT1	PAD_GPIO_1 if (GPIO1_MODE==7) PAD_GPIO_24 if (GPIO24_MODE==7)

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EINT	Source pin
EINT2	PAD_GPIO_2 if (GPIO2_MODE==7) PAD_GPIO_25 if (GPIO25_MODE==7)
EINT3	PAD_GPIO_3 if (GPIO3_MODE==7) PAD_GPIO_26 if (GPIO26_MODE==7)
EINT4	PAD_GPIO_4 if (GPIO4_MODE==7) PAD_GPIO_27 if (GPIO27_MODE==7)
EINT5	PAD_GPIO_5 if (GPIO5_MODE==7) PAD_GPIO_28 if (GPIO28_MODE==7)
EINT6	PAD_GPIO_6 if (GPIO6_MODE==7) PAD_GPIO_29 if (GPIO29_MODE==7)
EINT7	PAD_GPIO_7 if (GPIO7_MODE==7) PAD_GPIO_30 if (GPIO30_MODE==7)
EINT8	PAD_GPIO_8 if (GPIO8_MODE==7) PAD_GPIO_31 if (GPIO31_MODE==7)
EINT9	PAD_GPIO_9 if (GPIO9_MODE==7) PAD_GPIO_32 if (GPIO32_MODE==7)
EINT10	PAD_GPIO_10 if (GPIO10_MODE==7) PAD_GPIO_33 if (GPIO33_MODE==7)
EINT11	PAD_GPIO_11 if (GPIO11_MODE==7) PAD_GPIO_34 if (GPIO34_MODE==7)
EINT12	PAD_GPIO_12 if (GPIO12_MODE==7) PAD_GPIO_35 if (GPIO35_MODE==7)
EINT13	PAD_GPIO_13 if (GPIO13_MODE==7) PAD_GPIO_36 if (GPIO36_MODE==7)
EINT14	PAD_GPIO_14 if (GPIO14_MODE==7)
EINT15	PAD_GPIO_15 if (GPIO15_MODE==7)
EINT16	PAD_GPIO_16 if (GPIO16_MODE==7)
EINT17	PAD_GPIO_17 if (GPIO17_MODE==7)
EINT18	PAD_GPIO_18 if (GPIO18_MODE==7)
EINT19	PAD_GPIO_19 if (GPIO19_MODE==7)
EINT20	PAD_GPIO_20 if (GPIO20_MODE==7)
EINT21	PAD_GPIO_21 if (GPIO21_MODE==7)
EINT22	PAD_GPIO_22 if (GPIO22_MODE==7)
EINT23	WLAN_ACT if (GPIO9_MODE==5) WLAN_ACT if (GPIO29_MODE==4) WLAN_ACT if (GPIO34_MODE==6)
EINT24	uart0_rxd
EINT25	uart1_rxd
EINT26	uart2_rxd
EINT27	uart3_rxd
EINT28	rtc_event_b

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EINT	Source pin
EINT29	kp_eint
EINT30	pdn_usb11
EINT31	pmu_wakeup_intb

6.9. Register mapping

Module name: EINT Base address: (+A2100000h)

Address	Name	Width (bits)	Register Function
A2100300	EINT_STA	32	EINT interrupt status register
A2100308	EINT_INTACK	32	EINT interrupt acknowledge register
A2100310	EINT_EEVT	32	EINT wakeup event status register
A2120318	EINT_EEVTACK	32	EINT wakeup event acknowledge register
A2100320	EINT_MASK	32	EINT interrupt mask register
A2100328	EINT_MASK_SET	32	EINT interrupt mask set register
A2100330	EINT_MASK_CLR	32	EINT interrupt mask clear register
A2100340	EINT_WAKEUP_MASK	32	EINT wakeup event mask register
A2100348	EINT_WAKEUP_MASK_SET	32	EINT wakeup event mask set register
A2100350	EINT_WAKEUP_MASK_CLR	32	EINT wakeup event mask clear register
A2100360	EINT_SENS	32	EINT sensitivity register
A2100368	EINT_SENS_SET	32	EINT sensitivity set register
A2100370	EINT_SENS_CLR	32	EINT sensitivity clear register
A2100380	EINT_DUALEDGE_SENS	32	EINT dual edge sensitivity register
A2100388	EINT_DUALEDGE_SENS_SET	32	EINT dual edge sensitivity set register
A2100390	EINT_DUALEDGE_SENS_CLR	32	EINT dual edge sensitivity clear register
A21003A0	EINT_POL	32	EINT polarity register
A21003A8	EINT_POL_SET	32	EINT polarity set register
A21003B0	EINT_POL_CLR	32	EINT polarity clear register
A21003C0	EINT_SOFT	32	EINT software interrupt register
A21003C8	EINT_SOFT_SET	32	EINT software interrupt set register
A21003D0	EINT_SOFT_CLR	32	EINT software interrupt clear register
A2100400 ~ A210047C	EINTi_CON (i=0~31)	32	EINTi configuration register
A2120500	FIRQ_STA	32	EINT interrupt status register
A2120510	FIRQ_MASK	32	EINT fast interrupt mask register
A2120514	FIRQ_MASK_SET	32	EINT fast interrupt mask set register
A2120518	FIRQ_MASK_CLR	32	EINT fast interrupt mask clear register

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6.9.1. Register definitions

A2100300 EINT_STA EINT interrupt status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_STA[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_STA[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_STA	**External interrupt status** This register tracks interrupt request status generated by certain EINT sources. If the EINT sources are set to edge sensitivity, EINT_IRQ is de-asserted while the corresponding EINT_INTACK is set to 1. EINT_STA[i] for EINTi. • 0: No external interrupt request is generated. • 1: External interrupt request is pending.

A2100308 EINT_INTACK EINT interrupt acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_INTACK[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_INTACK[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_INTACK	**Interrupt acknowledgement** Writing "1" to the specific bit position will acknowledge the interrupt request corresponding to the external interrupt line source. EINT_INTACK[i] for EINTi. 0: No effect 1: Interrupt request is acknowledged.

A2120310 EINT_EEVT EINT wakeup event status register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_EEVT[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_EEVT[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_EEVT	**EINT wake up event** This register is a debug port to monitor internal signals. It is an

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Bit(s)	Mnemonic	Name	Description
			asynchronous signal. 0: EINT does not wake up the system from sleep mode. 1: EINT wakes up the system from sleep mode.

A2120318 EINT_EEVTACK EINT wakeup event acknowledge register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	EINT_EEVTACK[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	EINT_EEVTACK[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_EEVTACK	**Wakeup event acknowledgement** Writing "1" to the specific bit position will acknowledge the wakeup event request corresponding to the external interrupt line source. EINT_EEVTACK[i] for EINTi. 0: No effect 1: Wakeup event request is acknowledged.

A2100320 EINT_MASK EINT interrupt mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK	**Interrupt mask** This register controls whether the EINT source is allowed to generate an interrupt request. Setting a specific bit position to "1" will prevent activation of the external interrupt line. EINT_MASK[i] for EINTi. 0: Interrupt request is enabled. 1: Interrupt request is disabled.

A2100328 EINT_MASK_SET EINT interrupt mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_SET[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_SET [15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_SET	**Enables mask for the associated external interrupt source** This register is used to set up individual mask bits. Write 1 at each bit to set up the corresponding EINT_MASK bit (set to 1). Otherwise, EINT_MASK bits will retain the original value. EINT_MASK_SET[i] for EINTi. 0: No effect 1: Enables the corresponding MASK bit.

A2100330 EINT_MASK_CLR EINT interrupt mask clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_MASK_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_MASK_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_MASK_CLR	**Disables mask for the associated external interrupt source** This register is used to clear individual mask bits. Write 1 at each bit to clear the corresponding EINT_MASK bit (set to 0). Otherwise, EINT_MASK bits will retain the original value. EINT_MASK_CLR[i] for EINTi. 0: No effect 1: Disables the corresponding MASK bit.

A2100340 EINT_WAKEUP_MASK EINT wakeup event mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_WAKEUP_MASK[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_WAKEUP_MASK[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0		EINT_WAKEUP_MASK	**Wakeup event mask** This register controls whether the EINT source is allowed to generate a wakeup event request. Setting a specific bit position to "1" will prevent activation of the external interrupt line. EINT_WAKEUP_MASK[i] for EINTi. 0: Wakeup event request is enabled. 1: Wakeup event request is disabled.

A2100348 EINT_WAKEUP_MASK_SET EINT wakeup event mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_WAKEUP_MASK_SET[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_WAKEUP_MASK_SET[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_WAKEUP_MASK_SET	**Enables mask for the associated external interrupt source** This register is used to set up individual mask bits. Write 1 at each bit to set up the corresponding EINT_WAKEUP_MASK bit (set to 1). Otherwise, EINT_WAKEUP_MASK bits will retain the original value. EINT_WAKEUP_MASK_SET[i] for EINTi. 0: No effect 1: Enables the corresponding MASK bit.

A2100350 EINT_WAKEUP_MASK_CLR EINT wakeup event mask clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_WAKEUP_MASK_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_WAKEUP_MASK_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_WAKEUP_MASK_CLR	**Disables mask for the associated external interrupt source** This register is used to clear individual mask bits. Write 1 at each bit to clear the corresponding EINT_WAKEUP_MASK bit (set to 0). Otherwise, EINT_WAKEUP_MASK bits will retain the original value. EINT_WAKEUP_MASK_CLR[i] for EINTi. 0: No effect 1: Disables the corresponding MASK bit.

A2100360 EINT_SENS EINT sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS	**Sensitivity type of the associated external interrupt source** Sensitivity type of the external interrupt source. EINT_SENS[i] for EINTi. 0: Edge sensitivity (active high or low depends on POL setting) 1: Level sensitivity (active high or low depends on POL setting)

A2100368 EINT_SENS_SET EINT sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	EINT_SENS_SET[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_SET[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_SET	**Enables sensitivity for the associated external interrupt source.** This register is used to set up individual sensitive bits. Write 1 at each bit to set up the corresponding EINT_SENS bit (set to 1). Otherwise, EINT_SENS bits will retain the original value. EINT_SENS_SET[i] for EINTi. 0: No effect 1: Enables the corresponding SENS bit.

A2100370 EINT_SENS_CLR EINT sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SENS_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_SENS_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SENS_CLR	**Disables sensitivity for the associated external interrupt source.** This register is used to clear individual sensitive bits. Write 1 at each bit to clear the corresponding EINT_SENS bit(set to 0). Otherwise, EINT_SENS bits will retain the original value. EINT_SENS_CLR[i] for EINTi. 0: No effect 1: Disables the corresponding SENS bit.

A2100380 EINT_DUALEDGE_SENS EINT dual edge sensitivity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DUALEDGE_SENS[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DUALEDGE_SENS[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DUALEDGE_SENS	**Dual edge sensitivity type of the associated external interrupt source** Dual edge sensitivity type of external interrupt source. (EINT_SENS should be 0) EINT_DUALEDGE_SENS[i] for EINTi.

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Bit(s)	Mnemonic	Name	Description
			0: Disable 1: Enable (no dependency on POL).

A2100388 EINT_DUALEDGE_SENS_SET EINT dual edge sensitivity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DUALEDGE_SENS_SET[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DUALEDGE_SENS_SET[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DUALEDGE_SENS_SET	**Enables dual edge sensitivity for the associated external interrupt source.** This register is used to set up individual dual edge sensitive bits. (EINT_SENS should be 0) Write 1 at each bit to set up the corresponding EINT_DUALEDGE_SENS bit (set to 1). Otherwise, EINT_DUALEDGE_SENS bits will retain the original value. EINT_DUALEDGE_SENS_SET[i] for EINTi. 0: No effect 1: Enables the corresponding DUALEDGE bit.

A2100390 EINT_DUALEDGE_SENS_CLR EINT dual edge sensitivity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_DUALEDGE_SENS_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_DUALEDGE_SENS_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_DUALEDGE_SENS_CLR	**Disables dual edge sensitivity for the associated external interrupt source.** This register is used to clear individual sensitive bits. Write 1 at each bit to clear the corresponding EINT_DUALEDGE_SENS bit (set to 0). Otherwise, EINT_DUALEDGE_SENS bits will retain the original value. EINT_DUALEDGE_SENS_CLR[i] for EINTi. 0: No effect 1: Disables the corresponding DUALEDGE bit.

A21003A0 EINT_POL EINT polarity register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL[15:0]															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL	**Configures polarity of the associated external interrupt source.** Activation type of the EINT source. EINT_POL[i] for EINTi. 0: Active low 1: Active high

A21003A8 EINT_POL_SET EINT polarity set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_SET[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_SET[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_SET	**Enables polarity configuration for the associated external interrupt source** This register is used to set up individual polarity bits. Write 1 at each bit to set up the corresponding EINT_POL bit (set to 1). Otherwise, EINT_POL bits will retain the original value. EINT_POL_SET[i] for EINTi. 0: No effect 1: Enables the corresponding POL bit.

A21003B0 EINT_POL_CLR EINT polarity clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_POL_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EINT_POL_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_POL_CLR	**Polarity configuration set** This register is used to clear individual polarity bits. Write 1 at each bit to clear the corresponding EINT_POL bit (set to 0). Otherwise, EINT_POL bits will retain the original value. EINT_POL_CLR[i] for EINTi. 0: No effect 1: Disables the corresponding POL bit.

A21003C0 EINT_SOFT EINT software interrupt register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EINT_SOFT[31:16]															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT[15:0]**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT	**Software interrupt** This register is used for debugging purposes. EINT_SOFT[i] for EINTi. 0: No effect 1: Triggers an EINT

A21003C8 EINT_SOFT_SET EINT software interrupt set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SOFT_SET[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT_SET[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_SET	**Enables software for the associated external interrupt source** This register is used to set up individual software bits. Write 1 at each bit to set up the corresponding EINT_SOFT bit (set to 1). Otherwise, EINT_SOFT bits will retain the original value. EINT_SOFT_SET[i] for EINTi. 0: No effect 1: Enables the corresponding SOFT bit.

A21003D0 EINT_SOFT_CLR EINT software interrupt clear register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EINT_SOFT_CLR[31:16]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EINT_SOFT_CLR[15:0]**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0		EINT_SOFT_CLR	**Disables software for the associated external interrupt source** This register is used to clear individual software bits. Write 1 at each bit to clear the corresponding EINT_SOFT bit (set to 0). Otherwise, EINT_SOFT bits will retain the original value. EINT_SOFT_CLR[i] for EINTi. 0: No effect 1: Disables the corresponding SOFT bit.

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A2100400~A210047C (step = 0x4) **EINTi_CON (i=0~31)** **EINTi configuration register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								RSTDBC								DBC_EN
Type								WO								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		DBC_CON														
Type		RW														
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
24		RSTDBC	**EINTi debounce count reset** Write 1 to reset the debounce counter so that EINT can be updated immediately without debounce latency. This option needs 100µs latency to take effect. 0: no effect 1: reset
16		DBC_EN	**EINTi debounce circuit enable** 0: disable 1: enable
14:0		DBC_CON	**EINTi debounce count setting** DBC_CNT = DBC_CON[10:0] EINTi debounce duration configuration (clock period is determined in PRESCALER) *Note: When DBD_CON[10:0] = 0 and DBC_EN = 1, there are still two 32K clock cycles (62.5 µs) debounce. To disable the debounce function, DBC_EN should be set to 0 (zero).* PRESCALER = DBC_CON[14:12] EINTi debounce clock cycle period prescaler. 000: 32,768Hz, max. 0.0625secs 001: 16,384Hz 010: 8,192Hz 011: 4,096Hz 100: 2,048Hz, max. 1s 101: 1,024Hz 110: 512Hz 111: 256Hz, max. 8s

A2120500 **FIRQ_STA** **EINT interrupt status register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIRQ_STA[31:16]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIRQ_STA[15:0]															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
31:0		FIRQ_STA	**External fast interrupt status**

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Bit(s)	Mnemonic	Name	Description
			This register keeps up with the current status of the EINT source generating a fast interrupt request. If the EINT sources are set to edge sensitivity, EINT_IRQ is de-asserted while the corresponding EINT_INTACK is programmed by 1. FIRQ_STA[i] for EINTi. 0: No external fast interrupt request is generated. 1: External fast interrupt request is pending.

A2120510 FIRQ_MASK EINT fast interrupt mask register FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIRQ_MASK[31:16]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIRQ_MASK[15:0]															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview

Bit(s)	Mnemonic	Name	Description
31:0		FIRQ_MASK	**Interrupt mask** This register controls whether the EINT source is allowed to generate an interrupt request. Setting a specific bit position to "1" will prevent the external interrupt line activation. EINT_MASK[i] for EINTi. 0: Interrupt request is enabled. 1: Interrupt request is disabled.

A2120514 FIRQ_MASK_SET EINT fast interrupt mask set register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIRQ_MASK_SET[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIRQ_MASK_SET[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
31:0		FIRQ_MASK_SET	**Enables mask for the associated external interrupt source** This register is used to set up individual mask bits. Write 1 at each bit to set up the corresponding FIRQ_MASK bit (set to 1). Otherwise, FIRQ_MASK bits will retain the original value. FIRQ_MASK_SET[i] for EINTi. 0: No effect 1: Enable the corresponding MASK bit

A2120518 FIRQ_MASK_CLR EINT fast interrupt mask clear register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIRQ_MASK_CLR[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIRQ_MASK_CLR[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview

Bit(s)	Mnemonic	Name	Description
31:0		FIRQ_MASK_CLR	**Disables mask for the associated external interrupt source** This register is used to clear individual mask bits. Write 1 at each bit to clear the corresponding FIRQ_MASK bit (set to 0). Otherwise, FIRQ_MASK bits will retain the original value. FIRQ_MASK_CLR[i] for EINTi. 0: No effect 1: Disable the corresponding MASK bit

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7. General Purpose Inputs/Outputs

7.1. Overview

MediaTek MT2625 platform offers 37 general purpose input/output (GPIO) pins. By setting up the control registers, the MCU software can control the direction, the output value and read the input values on these pins. The GPIOs and GPOs are multiplexed with other functions to reduce the pin count.

7.2. Features

The clock to send outside the chip is software configurable. There are five clock-out ports and each clock-out can be programmed to output the appropriate clock. In addition, when two GPIOs are multiplexed to the same peripheral IP input, the smaller the GPIO serial number the higher the priority

7.3. Block diagram

The block diagram for the GPIO is shown in Figure 7.3-1.

Figure 7.3-1. GPIO block diagram

7.4. Functions

Table 7.4-1. GPIO IO structure

IO Structure	**TYPE0**	Pull-up/down
		3.63V tolerance
	TYPE1	Pull-up/down
		5V tolerance
	TYPE2	Pull-up/down
		5V tolerance
		SDIO characteristic support
	TYPE3	Pull-up/down
		5V tolerance
		Analog input/output
	TYPE4	Pull-up/down
		5V tolerance

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		Keypad 2K characteristic support
	TYPE5	Pull-up/down
		5V tolerance
		Keypad 200K characteristic support
	TYPE6	Pull-up/down
		3.63V tolerance
		SIM characteristic support

Table 7.4-2. GPIO versus IO type mapping

GPIO Name	IO Type	GPIO Name	IO Type
GPIO0	IO TYPE 5	GPIO25	IO TYPE 1
GPIO1	IO TYPE 5	GPIO26	IO TYPE 1
GPIO2	IO TYPE 1	GPIO27	IO TYPE 1
GPIO3	IO TYPE 4	GPIO28	IO TYPE 1
GPIO4	IO TYPE 4	GPIO29	IO TYPE 1
GPIO5	IO TYPE 1	GPIO30	IO TYPE 3
GPIO6	IO TYPE 2	GPIO31	IO TYPE 3
GPIO7	IO TYPE 2	GPIO32	IO TYPE 3
GPIO8	IO TYPE 2	GPIO33	IO TYPE 3
GPIO9	IO TYPE 2	GPIO34	IO TYPE 3
GPIO10	IO TYPE 2	GPIO35	IO TYPE 5
GPIO11	IO TYPE 2	GPIO36	IO TYPE 4
GPIO12	IO TYPE 2	BPI0	IO TYPE 1
GPIO13	IO TYPE 2	BPI1	IO TYPE 1
GPIO14	IO TYPE 2	BPI2	IO TYPE 1
GPIO15	IO TYPE 2	BPI3	IO TYPE 1
GPIO16	IO TYPE 2	BPI4	IO TYPE 1
GPIO17	IO TYPE 2	MIPI_SCLK	IO TYPE 1
GPIO18	IO TYPE 2	MIPI_SDATA	IO TYPE 1
GPIO19	IO TYPE 2	SIM0_SIO	IO TYPE 6
GPIO20	IO TYPE 2	SIM0_SRST	IO TYPE 6
GPIO21	IO TYPE 2	SIM0_SCLK	IO TYPE 6
GPIO22	IO TYPE 2	RESETB_OUT	IO TYPE 1
GPIO23	IO TYPE 2	SRCLKENAI	IO TYPE 1
GPIO24	IO TYPE 1		

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Table 7.4-3. IO type 0 - pull up/down control

GPIO_DIR	GPIO_PU	GPIO_PD	Resistance (Ω), DVDIO=3.3V
0	0	0	High-Z
0	0	1	Pull-down, 75K
0	1	0	Pull-up, 75K
0	1	1	Keeper, 75K
1	0	0	Output mode

Table 7.4-4. IO type 1 - pull up/down control

GPIO_DIR	GPIO_PU	GPIO_PD	Resistance (Ω) , DVDIO=3.3V
0	0	0	High-Z
0	0	1	Pull-down, 75K
0	1	0	Pull-up, 75K
0	1	1	Keeper, 75K
1	0	0	Output mode

Table 7.4-5. IO type 2 - pull up/down control

GPIO_DIR	GPIO_PUPD	GPIO_R1	GPIO_R0	Resistance (Ω) , DVDIO=3.3V
0	0	0	0	High-Z
0	0	0	1	Pull-up, 45k
0	0	1	0	Pull-up, 45k
0	0	1	1	Pull-up, 23k
0	1	0	0	High-Z
0	1	0	1	Pull-down, 45k
0	1	1	0	Pull-down, 45k
0	1	1	1	Pull-down, 23k
1	X	X	X	Output mode

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Table 7.4.1-4. IO type 3 - pull up/down control

GPIO_DIR	GPIO_PU	GPIO_PD	Resistance (Ω) , DVDIO=3.3V
0	0	0	High-Z
0	0	1	Pull-down, 75K
0	1	0	Pull-up, 75K
0	1	1	Keeper, 75K
1	0	0	Output mode

Table 7.4.1-5. IO type 4 - pull up/down control

GPIO_DIR	GPIO_PUPD	GPIO_R1	GPIO_R0	Resistance (Ω) , DVDIO=3.3V
0	0	0	0	High-Z
0	0	0	1	Pull-up, 45k
0	0	1	0	Pull-up, 2k
0	0	1	1	Pull-up, 2k
0	1	0	0	High-Z
0	1	0	1	Pull-down, 45k
0	1	1	0	Pull-down, 2k
0	1	1	1	Pull-down, 2k
1	X	X	X	Output mode

Table 7.4-6. IO type 5 - pull up/down control

GPIO_DIR	GPIO_PUPD	GPIO_R1	GPIO_R0	Resistance (Ω) , DVDIO=3.3V
0	0	0	0	High-Z
0	0	0	1	Pull-up, 45k
0	0	1	0	Pull-up, 200k
0	0	1	1	Pull-up, 45k

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GPIO_DIR	GPIO_PUPD	GPIO_R1	GPIO_R0	Resistance (Ω) , DVDIO=3.3V
0	1	0	0	High-Z
0	1	0	1	Pull-down, 45k
0	1	1	0	Pull-down, 200k
0	1	1	1	Pull-down, 45k
1	X	X	X	Output mode

Table 7.4-7. IO type 6 - pull up/down control

GPIO_DIR	GPIO_PUPD	GPIO_R1	GPIO_R0	Resistance (Ω), DVDIO=3.3V
0	0	0	0	High-Z
0	0	0	1	Pull-up, 20K
0	0	1	0	Pull-up, 5K
0	1	0	0	High-Z
0	1	0	1	Pull-down, 75K
0	1	1	0	Pull-down, 40K
1	X	X	X	Output mode

7.5. Register mapping

Table 7.5-1. Special registers

TDSEL	TX duty select
TDSEL0	Output level shifter duty high when asserted (high pulse width adjustment)
TDSEL1	Output level shifter duty low when asserted (low pulse width adjustment)
RDSEL	RX duty select
RDSEL0	Input buffer duty high when asserted (high pulse width adjustment)
RDSEL1	Input buffer duty low when asserted (low pulse width adjustment)
SR[1:0]	High asserted output slew rate (SR) control. If SR is 1, slew is slower; if SR is 0, no slew rate is controlled.

7.5.1. GPIO register mapping

Module name: GPIO Base address: (+a20b0000h)

Address	Name	Width (bits)	Register Function
A20B0000	GPIO_DIR_A	32	GPIO Direction Control

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Address	Name	Width (bits)	Register Function
A20B0004	GPIO_DIR_B	32	GPIO Direction Control
A20B0008	GPIO_DIR_A_SET	32	GPIO Direction Control
A20B000C	GPIO_DIR_B_SET	32	GPIO Direction Control
A20B0010	GPIO_DIR_A_CLR	32	GPIO Direction Control
A20B0014	GPIO_DIR_B_CLR	32	GPIO Direction Control
A20B0020	GPIO_DOUT_A	32	GPIO Output Data Control
A20B0024	GPIO_DOUT_B	32	GPIO Output Data Control
A20B0028	GPIO_DOUT_A_SET	32	GPIO Output Data Control
A20B002C	GPIO_DOUT_B_SET	32	GPIO Output Data Control
A20B0030	GPIO_DOUT_A_CLR	32	GPIO Output Data Control
A20B0034	GPIO_DOUT_B_CLR	32	GPIO Output Data Control
A20B0040	GPIO_DIN_A	32	GPIO Input Data Value
A20B0044	GPIO_DIN_B	32	GPIO Input Data Value
A20B0050	GPIO_MODE_A	32	GPIO Mode Control
A20B0054	GPIO_MODE_B	32	GPIO Mode Control
A20B0058	GPIO_MODE_C	32	GPIO Mode Control
A20B005C	GPIO_MODE_D	32	GPIO Mode Control
A20B0060	GPIO_MODE_E	32	GPIO Mode Control
A20B0064	GPIO_MODE_F	32	GPIO Mode Control
A20B0068	GPIO_MODE_G	8	GPIO Mode Control
A20B0070	GPIO_MODE_A_SET	32	GPIO Mode Control
A20B0074	GPIO_MODE_B_SET	32	GPIO Mode Control
A20B0078	GPIO_MODE_C_SET	32	GPIO Mode Control
A20B007C	GPIO_MODE_D_SET	32	GPIO Mode Control
A20B0080	GPIO_MODE_E_SET	32	GPIO Mode Control
A20B0084	GPIO_MODE_F_SET	32	GPIO Mode Control
A20B0088	GPIO_MODE_G_SET	32	GPIO Mode Control
A20B0090	GPIO_MODE_A_CLR	32	GPIO Mode Control
A20B0094	GPIO_MODE_B_CLR	32	GPIO Mode Control
A20B0098	GPIO_MODE_C_CLR	32	GPIO Mode Control
A20B009C	GPIO_MODE_D_CLR	32	GPIO Mode Control
A20B00A0	GPIO_MODE_E_CLR	32	GPIO Mode Control
A20B00A4	GPIO_MODE_F_CLR	32	GPIO Mode Control
A20B00A8	GPIO_MODE_G_CLR	32	GPIO Mode Control

7.5.2. IO_CFG_0 register mapping

Module name: IO_CFG_0 Base address: (+a20c0000h)

Address	Name	Width (bits)	Register Function
A20C0000	DRV_CFG0	32	GPIO TX driving strength control

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Address	Name	Width (bits)	Register Function
A20C0004	DRV_CFG1	32	**GPIO TX driving strength control**
A20C0018	IES_CFG0	32	**GPIO IES control.** RX input buffer enable. High asserted. Datapath is from IO to O. IES =0, O=0.
A20C001C	IES_CFG0_SET	32	**GPIO IES control.** RX input buffer enable. High asserted. Datapath is from IO to O. IES =0, O=0.
A20C0020	IES_CFG0_CLR	32	**GPIO IES control for bitwise access**
A20C0024	PD_CFG0	32	**GPIO PD control**
A20C0028	PD_CFG0_SET	32	**GPIO PD control for bitwise access**
A20C002C	PD_CFG0_CLR	32	**GPIO PD control for bitwise access**
A20C0030	PUPD_CFG0	32	**GPIO PUPD control**
A20C0034	PUPD_CFG0_SET	32	**GPIO PUPD control for bitwise access**
A20C0038	PUPD_CFG0_CLR	32	**GPIO PUPD control for bitwise access**
A20C003C	PU_CFG0	32	**GPIO PU control**
A20C0040	PU_CFG0_SET	32	**GPIO PU control for bitwise access**
A20C0044	PU_CFG0_CLR	32	**GPIO PU control for bitwise access**
A20C0048	R0_CFG0	32	**GPIO R0 control**
A20C004C	R0_CFG0_SET	32	**GPIO R0 control for bitwise access**
A20C0050	R0_CFG0_CLR	32	**GPIO R0 control for bitwise access**
A20C0054	R1_CFG0	32	**GPIO R1 control**
A20C0058	R1_CFG0_SET	32	**GPIO R1 control for bitwise access**
A20C005C	R1_CFG0_CLR	32	**GPIO R1 control for bitwise access**
A20C0060	RDSEL_CFG0	32	**GPIO RX duty select** RDSEL[0]: level shifter duty high when asserted RDSEL[1]: level shifter duty low when asserted
A20C0064	RDSEL_CFG1	32	**GPIO RX duty select** RDSEL[0]: level shifter duty high when asserted RDSEL[1]: level shifter duty low when asserted
A20C0078	SMT_CFG0	32	**GPIO SMT control**
A20C007C	SMT_CFG0_SET	32	**GPIO SMT control for bitwise access**
A20C0080	SMT_CFG0_CLR	32	**GPIO SMT control for bitwise access**
A20C0084	SR_CFG0	32	**GPIO output slew rate control.** High asserted. SR=1, slower slew. SR=0, no slew rate controlled.
A20C0088	SR_CFG0_SET	32	**GPIO slew rate control for bitwise access**
A20C008C	SR_CFG0_CLR	32	**GPIO slew rate control for bitwise access**
A20C0090	TDSEL_CFG0	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted
A20C0094	TDSEL_CFG1	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted
A20C0098	TDSEL_CFG2	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted

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Address	Name	Width (bits)	Register Function
A20C009C	TDSEL_CFG3	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted

7.5.3. IO_CFG_1 register map

Module name: IO_CFG_1 Base address: (+a20d0000h)

Address	Name	Width (bits)	Register Function
A20D0000	DRV_CFG0	32	**GPIO TX driving strength control**
A20D0004	DRV_CFG1	32	**GPIO TX driving strength control**
A20D0018	G_CFG0	32	**GPIO analog input control**
A20D001C	G_CFG0_SET	32	**GPIO analog input control for bitwise access**
A20D0020	G_CFG0_CLR	32	**GPIO analog input control for bitwise access**
A20D0024	IES_CFG0	32	**GPIO IES control.** RX input buffer enable. High asserted. Datapath: from IO to O. IES =0, O=0.
A20D0028	IES_CFG0_SET	32	**GPIO IES control for bitwise access**
A20D002C	IES_CFG0_CLR	32	**GPIO IES control for bitwise access**
A20D0030	PD_CFG0	32	**GPIO PD control**
A20D0034	PD_CFG0_SET	32	**GPIO PD control for bitwise access**
A20D0038	PD_CFG0_CLR	32	**GPIO PD control for bitwise access**
A20D003C	PUPD_CFG0	32	**GPIO PUPD control**
A20D0040	PUPD_CFG0_SET	32	**GPIO PUPD control for bitwise access**
A20D0044	PUPD_CFG0_CLR	32	**GPIO PUPD control for bitwise access**
A20D0048	PU_CFG0	32	**GPIO PU control**
A20D004C	PU_CFG0_SET	32	**GPIO PU control for bitwise access**
A20D0050	PU_CFG0_CLR	32	**GPIO PU control for bitwise access**
A20D0054	R0_CFG0	32	**GPIO R0 control**
A20D0058	R0_CFG0_SET	32	**GPIO R0 control for bitwise access**
A20D005C	R0_CFG0_CLR	32	**GPIO R0 control for bitwise access**
A20D0060	R1_CFG0	32	**GPIO R1 control**
A20D0064	R1_CFG0_SET	32	**GPIO R1 control for bitwise access**
A20D0068	R1_CFG0_CLR	32	**GPIO R1 control for bitwise access**
A20D006C	RDSEL_CFG0	32	**GPIO RX duty select** RDSEL[0]: level shifter duty high when asserted RDSEL[1]: level shifter duty low when asserted
A20D0070	RDSEL_CFG1	32	**GPIO RX duty select** RDSEL[0]: level shifter duty high when asserted RDSEL[1]: level shifter duty low when asserted
A20D0084	SMT_CFG0	32	**GPIO RX input buffer Schmitt trigger hysteresis control enable.** High asserted.
A20D0088	SMT_CFG0_SET	32	**GPIO SMT control for bitwise access**
A20D008C	SMT_CFG0_CLR	32	**GPIO SMT control for bitwise access**

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Address	Name	Width (bits)	Register Function
A20D0090	SR_CFG0	32	**GPIO output slew rate control.** High asserted. SR=1, slower slew. SR=0, no slew rate controlled.
A20D0094	SR_CFG0_SET	32	**GPIO slew rate control for bitwise access**
A20D0098	SR_CFG0_CLR	32	**GPIO slew rate control for bitwise access**
A20D009C	TDSEL_CFG0	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted
A20D00A0	TDSEL_CFG1	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted
A20D00A4	TDSEL_CFG2	32	**GPIO TX duty select** TDSEL[0]: output level shifter duty high when asserted TDSEL[1]: output level shifter duty low when asserted

A20B0000 GPIO_DIR_A GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DIR	GPIO30_DIR	GPIO29_DIR	GPIO28_DIR	GPIO27_DIR	GPIO26_DIR	GPIO25_DIR	GPIO24_DIR	GPIO23_DIR	GPIO22_DIR	GPIO21_DIR	GPIO20_DIR	GPIO19_DIR	GPIO18_DIR	GPIO17_DIR	GPIO16_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIR	GPIO14_DIR	GPIO13_DIR	GPIO12_DIR	GPIO11_DIR	GPIO10_DIR	GPIO9_DIR	GPIO8_DIR	GPIO7_DIR	GPIO6_DIR	GPIO5_DIR	GPIO4_DIR	GPIO3_DIR	GPIO2_DIR	GPIO1_DIR	GPIO0_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIR	**GPIO31 direction control** 0: GPIO as input 1: GPIO as output
30	**GPIO30**	GPIO30_DIR	**GPIO30 direction control** 0: GPIO as input 1: GPIO as output
29	**GPIO29**	GPIO29_DIR	**GPIO29 direction control** 0: GPIO as input 1: GPIO as output
28	**GPIO28**	GPIO28_DIR	**GPIO28 direction control** 0: GPIO as input 1: GPIO as output
27	**GPIO27**	GPIO27_DIR	**GPIO27 direction control** 0: GPIO as input 1: GPIO as output
26	**GPIO26**	GPIO26_DIR	**GPIO26 direction control** 0: GPIO as input 1: GPIO as output

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Bit(s)	Mnemonic	Name	Description
25	**GPIO25**	GPIO25_DIR	**GPIO25 direction control** 0: GPIO as input 1: GPIO as output
24	**GPIO24**	GPIO24_DIR	**GPIO24 direction control** 0: GPIO as input 1: GPIO as output
23	**GPIO23**	GPIO23_DIR	**GPIO23 direction control** 0: GPIO as input 1: GPIO as output
22	**GPIO22**	GPIO22_DIR	**GPIO22 direction control** 0: GPIO as input 1: GPIO as output
21	**GPIO21**	GPIO21_DIR	**GPIO21 direction control** 0: GPIO as input 1: GPIO as output
20	**GPIO20**	GPIO20_DIR	**GPIO20 direction control** 0: GPIO as input 1: GPIO as output
19	**GPIO19**	GPIO19_DIR	**GPIO19 direction control** 0: GPIO as input 1: GPIO as output
18	**GPIO18**	GPIO18_DIR	**GPIO18 direction control** 0: GPIO as input 1: GPIO as output
17	**GPIO17**	GPIO17_DIR	**GPIO17 direction control** 0: GPIO as input 1: GPIO as output
16	**GPIO16**	GPIO16_DIR	**GPIO16 direction control** 0: GPIO as input 1: GPIO as output
15	**GPIO15**	GPIO15_DIR	**GPIO15 direction control** 0: GPIO as input 1: GPIO as output
14	**GPIO14**	GPIO14_DIR	**GPIO14 direction control** 0: GPIO as input 1: GPIO as output
13	**GPIO13**	GPIO13_DIR	**GPIO13 direction control** 0: GPIO as input 1: GPIO as output
12	**GPIO12**	GPIO12_DIR	**GPIO12 direction control** 0: GPIO as input 1: GPIO as output
11	**GPIO11**	GPIO11_DIR	**GPIO11 direction control** 0: GPIO as input 1: GPIO as output
10	**GPIO10**	GPIO10_DIR	**GPIO10 direction control** 0: GPIO as input 1: GPIO as output
9	**GPIO9**	GPIO9_DIR	**GPIO9 direction control** 0: GPIO as input 1: GPIO as output
8	**GPIO8**	GPIO8_DIR	**GPIO8 direction control** 0: GPIO as input 1: GPIO as output
7	**GPIO7**	GPIO7_DIR	**GPIO7 direction control**

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Bit(s)	Mnemonic	Name	Description
			0: GPIO as input 1: GPIO as output
6	**GPIO6**	GPIO6_DIR	**GPIO6 direction control** 0: GPIO as input 1: GPIO as output
5	**GPIO5**	GPIO5_DIR	**GPIO5 direction control** 0: GPIO as input 1: GPIO as output
4	**GPIO4**	GPIO4_DIR	**GPIO4 direction control** 0: GPIO as input 1: GPIO as output
3	**GPIO3**	GPIO3_DIR	**GPIO3 direction control** 0: GPIO as input 1: GPIO as output
2	**GPIO2**	GPIO2_DIR	**GPIO2 direction control** 0: GPIO as input 1: GPIO as output
1	**GPIO1**	GPIO1_DIR	**GPIO1 direction control** 0: GPIO as input 1: GPIO as output
0	**GPIO0**	GPIO0_DIR	**GPIO0 direction control** 0: GPIO as input 1: GPIO as output

A20B0004 GPIO_DIR_B GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_DIR
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DIR	GPIO46_DIR	GPIO45_DIR	GPIO44_DIR	GPIO43_DIR	GPIO42_DIR	GPIO41_DIR	GPIO40_DIR	GPIO39_DIR	GPIO38_DIR	GPIO37_DIR	GPIO36_DIR	GPIO35_DIR	GPIO34_DIR	GPIO33_DIR	GPIO32_DIR
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_DIR	**GPIO48 direction control** 0: GPIO as input 1: GPIO as output
15	**GPIO47**	GPIO47_DIR	**GPIO47 direction control** 0: GPIO as input 1: GPIO as output
14	**GPIO46**	GPIO46_DIR	**GPIO46 direction control** 0: GPIO as input 1: GPIO as output
13	**GPIO45**	GPIO45_DIR	**GPIO45 direction control** 0: GPIO as input 1: GPIO as output
12	**GPIO44**	GPIO44_DIR	**GPIO44 direction control** 0: GPIO as input 1: GPIO as output

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Bit(s)	Mnemonic	Name	Description
11	**GPIO43**	GPIO43_DIR	**GPIO43 direction control** 0: GPIO as input 1: GPIO as output
10	**GPIO42**	GPIO42_DIR	**GPIO42 direction control** 0: GPIO as input 1: GPIO as output
9	**GPIO41**	GPIO41_DIR	**GPIO41 direction control** 0: GPIO as input 1: GPIO as output
8	**GPIO40**	GPIO40_DIR	**GPIO40 direction control** 0: GPIO as input 1: GPIO as output
7	**GPIO39**	GPIO39_DIR	**GPIO39 direction control** 0: GPIO as input 1: GPIO as output
6	**GPIO38**	GPIO38_DIR	**GPIO38 direction control** 0: GPIO as input 1: GPIO as output
5	**GPIO37**	GPIO37_DIR	**GPIO37 direction control** 0: GPIO as input 1: GPIO as output
4	**GPIO36**	GPIO36_DIR	**GPIO36 direction control** 0: GPIO as input 1: GPIO as output
3	**GPIO35**	GPIO35_DIR	**GPIO35 direction control** 0: GPIO as input 1: GPIO as output
2	**GPIO34**	GPIO34_DIR	**GPIO34 direction control** 0: GPIO as input 1: GPIO as output
1	**GPIO33**	GPIO33_DIR	**GPIO33 direction control** 0: GPIO as input 1: GPIO as output
0	**GPIO32**	GPIO32_DIR	**GPIO32 direction control** 0: GPIO as input 1: GPIO as output

A20B0008 GPIO_DIR_A_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DIR_SET	GPIO30_DIR_SET	GPIO29_DIR_SET	GPIO28_DIR_SET	GPIO27_DIR_SET	GPIO26_DIR_SET	GPIO25_DIR_SET	GPIO24_DIR_SET	GPIO23_DIR_SET	GPIO22_DIR_SET	GPIO21_DIR_SET	GPIO20_DIR_SET	GPIO19_DIR_SET	GPIO18_DIR_SET	GPIO17_DIR_SET	GPIO16_DIR_SET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIR_SET	GPIO14_DIR_SET	GPIO13_DIR_SET	GPIO12_DIR_SET	GPIO11_DIR_SET	GPIO10_DIR_SET	GPIO9_DIR_SET	GPIO8_DIR_SET	GPIO7_DIR_SET	GPIO6_DIR_SET	GPIO5_DIR_SET	GPIO4_DIR_SET	GPIO3_DIR_SET	GPIO2_DIR_SET	GPIO1_DIR_SET	GPIO0_DIR_SET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIR_SET	**Bitwise SET operation of GPIO31 direction**

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Bit(s)	Mnemonic	Name	Description
			0: Keep 1: SET bits
30	**GPIO30**	GPIO30_DIR_SET	**Bitwise SET operation of GPIO30 direction** 0: Keep 1: SET bits
29	**GPIO29**	GPIO29_DIR_SET	**Bitwise SET operation of GPIO29 direction** 0: Keep 1: SET bits
28	**GPIO28**	GPIO28_DIR_SET	**Bitwise SET operation of GPIO28 direction** 0: Keep 1: SET bits
27	**GPIO27**	GPIO27_DIR_SET	**Bitwise SET operation of GPIO27 direction** 0: Keep 1: SET bits
26	**GPIO26**	GPIO26_DIR_SET	**Bitwise SET operation of GPIO26 direction** 0: Keep 1: SET bits
25	**GPIO25**	GPIO25_DIR_SET	**Bitwise SET operation of GPIO25 direction** 0: Keep 1: SET bits
24	**GPIO24**	GPIO24_DIR_SET	**Bitwise SET operation of GPIO24 direction** 0: Keep 1: SET bits
23	**GPIO23**	GPIO23_DIR_SET	**Bitwise SET operation of GPIO23 direction** 0: Keep 1: SET bits
22	**GPIO22**	GPIO22_DIR_SET	**Bitwise SET operation of GPIO22 direction** 0: Keep 1: SET bits
21	**GPIO21**	GPIO21_DIR_SET	**Bitwise SET operation of GPIO21 direction** 0: Keep 1: SET bits
20	**GPIO20**	GPIO20_DIR_SET	**Bitwise SET operation of GPIO20 direction** 0: Keep 1: SET bits
19	**GPIO19**	GPIO19_DIR_SET	**Bitwise SET operation of GPIO19 direction** 0: Keep 1: SET bits
18	**GPIO18**	GPIO18_DIR_SET	**Bitwise SET operation of GPIO18 direction** 0: Keep 1: SET bits
17	**GPIO17**	GPIO17_DIR_SET	**Bitwise SET operation of GPIO17 direction** 0: Keep 1: SET bits
16	**GPIO16**	GPIO16_DIR_SET	**Bitwise SET operation of GPIO16 direction** 0: Keep 1: SET bits
15	**GPIO15**	GPIO15_DIR_SET	**Bitwise SET operation of GPIO15 direction** 0: Keep 1: SET bits
14	**GPIO14**	GPIO14_DIR_SET	**Bitwise SET operation of GPIO14 direction** 0: Keep 1: SET bits
13	**GPIO13**	GPIO13_DIR_SET	**Bitwise SET operation of GPIO13 direction** 0: Keep

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Bit(s)	Mnemonic	Name	Description
			1: SET bits
12	**GPIO12**	GPIO12_DIR_SET	**Bitwise SET operation of GPIO12 direction** 0: Keep 1: SET bits
11	**GPIO11**	GPIO11_DIR_SET	**Bitwise SET operation of GPIO11 direction** 0: Keep 1: SET bits
10	**GPIO10**	GPIO10_DIR_SET	**Bitwise SET operation of GPIO10 direction** 0: Keep 1: SET bits
9	**GPIO9**	GPIO9_DIR_SET	**Bitwise SET operation of GPIO9 direction** 0: Keep 1: SET bits
8	**GPIO8**	GPIO8_DIR_SET	**Bitwise SET operation of GPIO8 direction** 0: Keep 1: SET bits
7	**GPIO7**	GPIO7_DIR_SET	**Bitwise SET operation of GPIO7 direction** 0: Keep 1: SET bits
6	**GPIO6**	GPIO6_DIR_SET	**Bitwise SET operation of GPIO6 direction** 0: Keep 1: SET bits
5	**GPIO5**	GPIO5_DIR_SET	**Bitwise SET operation of GPIO5 direction** 0: Keep 1: SET bits
4	**GPIO4**	GPIO4_DIR_SET	**Bitwise SET operation of GPIO4 direction** 0: Keep 1: SET bits
3	**GPIO3**	GPIO3_DIR_SET	**Bitwise SET operation of GPIO3 direction** 0: Keep 1: SET bits
2	**GPIO2**	GPIO2_DIR_SET	**Bitwise SET operation of GPIO2 direction** 0: Keep 1: SET bits
1	**GPIO1**	GPIO1_DIR_SET	**Bitwise SET operation of GPIO1 direction** 0: Keep 1: SET bits
0	**GPIO0**	GPIO0_DIR_SET	**Bitwise SET operation of GPIO0 direction** 0: Keep 1: SET bits

A20B000C GPIO_DIR_B_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_DIR_SET
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DIR_SET	GPIO46_DIR_SET	GPIO45_DIR_SET	GPIO44_DIR_SET	GPIO43_DIR_SET	GPIO42_DIR_SET	GPIO41_DIR_SET	GPIO40_DIR_SET	GPIO39_DIR_SET	GPIO38_DIR_SET	GPIO37_DIR_SET	GPIO36_DIR_SET	GPIO35_DIR_SET	GPIO34_DIR_SET	GPIO33_DIR_SET	GPIO32_DIR_SET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_DIR_SET	**Bitwise SET operation of GPIO48 direction** 0: Keep 1: SET bits
15	**GPIO47**	GPIO47_DIR_SET	**Bitwise SET operation of GPIO47 direction** 0: Keep 1: SET bits
14	**GPIO46**	GPIO46_DIR_SET	**Bitwise SET operation of GPIO46 direction** 0: Keep 1: SET bits
13	**GPIO45**	GPIO45_DIR_SET	**Bitwise SET operation of GPIO45 direction** 0: Keep 1: SET bits
12	**GPIO44**	GPIO44_DIR_SET	**Bitwise SET operation of GPIO44 direction** 0: Keep 1: SET bits
11	**GPIO43**	GPIO43_DIR_SET	**Bitwise SET operation of GPIO43 direction** 0: Keep 1: SET bits
10	**GPIO42**	GPIO42_DIR_SET	**Bitwise SET operation of GPIO42 direction** 0: Keep 1: SET bits
9	**GPIO41**	GPIO41_DIR_SET	**Bitwise SET operation of GPIO41 direction** 0: Keep 1: SET bits
8	**GPIO40**	GPIO40_DIR_SET	**Bitwise SET operation of GPIO40 direction** 0: Keep 1: SET bits
7	**GPIO39**	GPIO39_DIR_SET	**Bitwise SET operation of GPIO39 direction** 0: Keep 1: SET bits
6	**GPIO38**	GPIO38_DIR_SET	**Bitwise SET operation of GPIO38 direction** 0: Keep 1: SET bits
5	**GPIO37**	GPIO37_DIR_SET	**Bitwise SET operation of GPIO37 direction** 0: Keep 1: SET bits
4	**GPIO36**	GPIO36_DIR_SET	**Bitwise SET operation of GPIO36 direction** 0: Keep 1: SET bits
3	**GPIO35**	GPIO35_DIR_SET	**Bitwise SET operation of GPIO35 direction** 0: Keep 1: SET bits
2	**GPIO34**	GPIO34_DIR_SET	**Bitwise SET operation of GPIO34 direction** 0: Keep 1: SET bits
1	**GPIO33**	GPIO33_DIR_SET	**Bitwise SET operation of GPIO33 direction** 0: Keep 1: SET bits
0	**GPIO32**	GPIO32_DIR_SET	**Bitwise SET operation of GPIO32 direction** 0: Keep 1: SET bits

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A20B0010 GPIO_DIR_A_CLR GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DIR_CLR	GPIO30_DIR_CLR	GPIO29_DIR_CLR	GPIO28_DIR_CLR	GPIO27_DIR_CLR	GPIO26_DIR_CLR	GPIO25_DIR_CLR	GPIO24_DIR_CLR	GPIO23_DIR_CLR	GPIO22_DIR_CLR	GPIO21_DIR_CLR	GPIO20_DIR_CLR	GPIO19_DIR_CLR	GPIO18_DIR_CLR	GPIO17_DIR_CLR	GPIO16_DIR_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIR_CLR	GPIO14_DIR_CLR	GPIO13_DIR_CLR	GPIO12_DIR_CLR	GPIO11_DIR_CLR	GPIO10_DIR_CLR	GPIO9_DIR_CLR	GPIO8_DIR_CLR	GPIO7_DIR_CLR	GPIO6_DIR_CLR	GPIO5_DIR_CLR	GPIO4_DIR_CLR	GPIO3_DIR_CLR	GPIO2_DIR_CLR	GPIO1_DIR_CLR	GPIO0_DIR_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIR_CLR	**Bitwise CLEAR operation of GPIO31 direction** 0: Keep 1: CLEAR bits
30	**GPIO30**	GPIO30_DIR_CLR	**Bitwise CLEAR operation of GPIO30 direction** 0: Keep 1: CLEAR bits
29	**GPIO29**	GPIO29_DIR_CLR	**Bitwise CLEAR operation of GPIO29 direction** 0: Keep 1: CLEAR bits
28	**GPIO28**	GPIO28_DIR_CLR	**Bitwise CLEAR operation of GPIO28 direction** 0: Keep 1: CLEAR bits
27	**GPIO27**	GPIO27_DIR_CLR	**Bitwise CLEAR operation of GPIO27 direction** 0: Keep 1: CLEAR bits
26	**GPIO26**	GPIO26_DIR_CLR	**Bitwise CLEAR operation of GPIO26 direction** 0: Keep 1: CLEAR bits
25	**GPIO25**	GPIO25_DIR_CLR	**Bitwise CLEAR operation of GPIO25 direction** 0: Keep 1: CLEAR bits
24	**GPIO24**	GPIO24_DIR_CLR	**Bitwise CLEAR operation of GPIO24 direction** 0: Keep 1: CLEAR bits
23	**GPIO23**	GPIO23_DIR_CLR	**Bitwise CLEAR operation of GPIO23 direction** 0: Keep 1: CLEAR bits
22	**GPIO22**	GPIO22_DIR_CLR	**Bitwise CLEAR operation of GPIO22 direction** 0: Keep 1: CLEAR bits
21	**GPIO21**	GPIO21_DIR_CLR	**Bitwise CLEAR operation of GPIO21 direction** 0: Keep 1: CLEAR bits
20	**GPIO20**	GPIO20_DIR_CLR	**Bitwise CLEAR operation of GPIO20 direction** 0: Keep 1: CLEAR bits
19	**GPIO19**	GPIO19_DIR_CLR	**Bitwise CLEAR operation of GPIO19 direction** 0: Keep 1: CLEAR bits
18	**GPIO18**	GPIO18_DIR_CLR	**Bitwise CLEAR operation of GPIO18 direction** 0: Keep

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Bit(s)	Mnemonic	Name	Description
			1: CLEAR bits
17	**GPIO17**	GPIO17_DIR_CLR	**Bitwise CLEAR operation of GPIO17 direction** 0: Keep 1: CLEAR bits
16	**GPIO16**	GPIO16_DIR_CLR	**Bitwise CLEAR operation of GPIO16 direction** 0: Keep 1: CLEAR bits
15	**GPIO15**	GPIO15_DIR_CLR	**Bitwise CLEAR operation of GPIO15 direction** 0: Keep 1: CLEAR bits
14	**GPIO14**	GPIO14_DIR_CLR	**Bitwise CLEAR operation of GPIO14 direction** 0: Keep 1: CLEAR bits
13	**GPIO13**	GPIO13_DIR_CLR	**Bitwise CLEAR operation of GPIO13 direction** 0: Keep 1: CLEAR bits
12	**GPIO12**	GPIO12_DIR_CLR	**Bitwise CLEAR operation of GPIO12 direction** 0: Keep 1: CLEAR bits
11	**GPIO11**	GPIO11_DIR_CLR	**Bitwise CLEAR operation of GPIO11 direction** 0: Keep 1: CLEAR bits
10	**GPIO10**	GPIO10_DIR_CLR	**Bitwise CLEAR operation of GPIO10 direction** 0: Keep 1: CLEAR bits
9	**GPIO9**	GPIO9_DIR_CLR	**Bitwise CLEAR operation of GPIO9 direction** 0: Keep 1: CLEAR bits
8	**GPIO8**	GPIO8_DIR_CLR	**Bitwise CLEAR operation of GPIO8 direction** 0: Keep 1: CLEAR bits
7	**GPIO7**	GPIO7_DIR_CLR	**Bitwise CLEAR operation of GPIO7 direction** 0: Keep 1: CLEAR bits
6	**GPIO6**	GPIO6_DIR_CLR	**Bitwise CLEAR operation of GPIO6 direction** 0: Keep 1: CLEAR bits
5	**GPIO5**	GPIO5_DIR_CLR	**Bitwise CLEAR operation of GPIO5 direction** 0: Keep 1: CLEAR bits
4	**GPIO4**	GPIO4_DIR_CLR	**Bitwise CLEAR operation of GPIO4 direction** 0: Keep 1: CLEAR bits
3	**GPIO3**	GPIO3_DIR_CLR	**Bitwise CLEAR operation of GPIO3 direction** 0: Keep 1: CLEAR bits
2	**GPIO2**	GPIO2_DIR_CLR	**Bitwise CLEAR operation of GPIO2 direction** 0: Keep 1: CLEAR bits
1	**GPIO1**	GPIO1_DIR_CLR	**Bitwise CLEAR operation of GPIO1 direction** 0: Keep 1: CLEAR bits
0	**GPIO0**	GPIO0_DIR_CLR	**Bitwise CLEAR operation of GPIO0 direction** 0: Keep 1: CLEAR bits

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Bit(s)	Mnemonic	Name	Description

A20B0014 GPIO_DIR_B_CLR GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_DIR_CLR
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DIR_CLR	GPIO46_DIR_CLR	GPIO45_DIR_CLR	GPIO44_DIR_CLR	GPIO43_DIR_CLR	GPIO42_DIR_CLR	GPIO41_DIR_CLR	GPIO40_DIR_CLR	GPIO39_DIR_CLR	GPIO38_DIR_CLR	GPIO37_DIR_CLR	GPIO36_DIR_CLR	GPIO35_DIR_CLR	GPIO34_DIR_CLR	GPIO33_DIR_CLR	GPIO32_DIR_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_DIR_CLR	**Bitwise CLEAR operation of GPIO48 direction** 0: Keep 1: CLEAR bits
15	**GPIO47**	GPIO47_DIR_CLR	**Bitwise CLEAR operation of GPIO47 direction** 0: Keep 1: CLEAR bits
14	**GPIO46**	GPIO46_DIR_CLR	**Bitwise CLEAR operation of GPIO46 direction** 0: Keep 1: CLEAR bits
13	**GPIO45**	GPIO45_DIR_CLR	**Bitwise CLEAR operation of GPIO45 direction** 0: Keep 1: CLEAR bits
12	**GPIO44**	GPIO44_DIR_CLR	**Bitwise CLEAR operation of GPIO44 direction** 0: Keep 1: CLEAR bits
11	**GPIO43**	GPIO43_DIR_CLR	**Bitwise CLEAR operation of GPIO43 direction** 0: Keep 1: CLEAR bits
10	**GPIO42**	GPIO42_DIR_CLR	**Bitwise CLEAR operation of GPIO42 direction** 0: Keep 1: CLEAR bits
9	**GPIO41**	GPIO41_DIR_CLR	**Bitwise CLEAR operation of GPIO41 direction** 0: Keep 1: CLEAR bits
8	**GPIO40**	GPIO40_DIR_CLR	**Bitwise CLEAR operation of GPIO40 direction** 0: Keep 1: CLEAR bits
7	**GPIO39**	GPIO39_DIR_CLR	**Bitwise CLEAR operation of GPIO39 direction** 0: Keep 1: CLEAR bits
6	**GPIO38**	GPIO38_DIR_CLR	**Bitwise CLEAR operation of GPIO38 direction** 0: Keep 1: CLEAR bits
5	**GPIO37**	GPIO37_DIR_CLR	**Bitwise CLEAR operation of GPIO37 direction** 0: Keep 1: CLEAR bits
4	**GPIO36**	GPIO36_DIR_CLR	**Bitwise CLEAR operation of GPIO36 direction**

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Bit(s)	Mnemonic	Name	Description
			0: Keep 1: CLEAR bits
3	**GPIO35**	GPIO35_DIR_CLR	**Bitwise CLEAR operation of GPIO35 direction** 0: Keep 1: CLEAR bits
2	**GPIO34**	GPIO34_DIR_CLR	**Bitwise CLEAR operation of GPIO34 direction** 0: Keep 1: CLEAR bits
1	**GPIO33**	GPIO33_DIR_CLR	**Bitwise CLEAR operation of GPIO33 direction** 0: Keep 1: CLEAR bits
0	**GPIO32**	GPIO32_DIR_CLR	**Bitwise CLEAR operation of GPIO32 direction** 0: Keep 1: CLEAR bits

A20B0020 GPIO_DOUT_A GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_OUT	GPIO30_OUT	GPIO29_OUT	GPIO28_OUT	GPIO27_OUT	GPIO26_OUT	GPIO25_OUT	GPIO24_OUT	GPIO23_OUT	GPIO22_OUT	GPIO21_OUT	GPIO20_OUT	GPIO19_OUT	GPIO18_OUT	GPIO17_OUT	GPIO16_OUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_OUT	GPIO14_OUT	GPIO13_OUT	GPIO12_OUT	GPIO11_OUT	GPIO10_OUT	GPIO9_OUT	GPIO8_OUT	GPIO7_OUT	GPIO6_OUT	GPIO5_OUT	GPIO4_OUT	GPIO3_OUT	GPIO2_OUT	GPIO1_OUT	GPIO0_OUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_OUT	**GPIO31 data output value** 0: GPIO output LO 1: GPIO output HI
30	**GPIO30**	GPIO30_OUT	**GPIO30 data output value** 0: GPIO output LO 1: GPIO output HI
29	**GPIO29**	GPIO29_OUT	**GPIO29 data output value** 0: GPIO output LO 1: GPIO output HI
28	**GPIO28**	GPIO28_OUT	**GPIO28 data output value** 0: GPIO output LO 1: GPIO output HI
27	**GPIO27**	GPIO27_OUT	**GPIO27 data output value** 0: GPIO output LO 1: GPIO output HI
26	**GPIO26**	GPIO26_OUT	**GPIO26 data output value** 0: GPIO output LO 1: GPIO output HI
25	**GPIO25**	GPIO25_OUT	**GPIO25 data output value** 0: GPIO output LO 1: GPIO output HI
24	**GPIO24**	GPIO24_OUT	**GPIO24 data output value** 0: GPIO output LO 1: GPIO output HI
23	**GPIO23**	GPIO23_OUT	**GPIO23 data output value**

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Bit(s)	Mnemonic	Name	Description
			0: GPIO output LO 1: GPIO output HI
22	**GPIO22**	GPIO22_OUT	**GPIO22 data output value** 0: GPIO output LO 1: GPIO output HI
21	**GPIO21**	GPIO21_OUT	**GPIO21 data output value** 0: GPIO output LO 1: GPIO output HI
20	**GPIO20**	GPIO20_OUT	**GPIO20 data output value** 0: GPIO output LO 1: GPIO output HI
19	**GPIO19**	GPIO19_OUT	**GPIO19 data output value** 0: GPIO output LO 1: GPIO output HI
18	**GPIO18**	GPIO18_OUT	**GPIO18 data output value** 0: GPIO output LO 1: GPIO output HI
17	**GPIO17**	GPIO17_OUT	**GPIO17 data output value** 0: GPIO output LO 1: GPIO output HI
16	**GPIO16**	GPIO16_OUT	**GPIO16 data output value** 0: GPIO output LO 1: GPIO output HI
15	**GPIO15**	GPIO15_OUT	**GPIO15 data output value** 0: GPIO output LO 1: GPIO output HI
14	**GPIO14**	GPIO14_OUT	**GPIO14 data output value** 0: GPIO output LO 1: GPIO output HI
13	**GPIO13**	GPIO13_OUT	**GPIO13 data output value** 0: GPIO output LO 1: GPIO output HI
12	**GPIO12**	GPIO12_OUT	**GPIO12 data output value** 0: GPIO output LO 1: GPIO output HI
11	**GPIO11**	GPIO11_OUT	**GPIO11 data output value** 0: GPIO output LO 1: GPIO output HI
10	**GPIO10**	GPIO10_OUT	**GPIO10 data output value** 0: GPIO output LO 1: GPIO output HI
9	**GPIO9**	GPIO9_OUT	**GPIO9 data output value** 0: GPIO output LO 1: GPIO output HI
8	**GPIO8**	GPIO8_OUT	**GPIO8 data output value** 0: GPIO output LO 1: GPIO output HI
7	**GPIO7**	GPIO7_OUT	**GPIO7 data output value** 0: GPIO output LO 1: GPIO output HI
6	**GPIO6**	GPIO6_OUT	**GPIO6 data output value** 0: GPIO output LO 1: GPIO output HI
5	**GPIO5**	GPIO5_OUT	**GPIO5 data output value** 0: GPIO output LO

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Bit(s)	Mnemonic	Name	Description
			1: GPIO output HI
4	**GPIO4**	GPIO4_OUT	**GPIO4 data output value** 0: GPIO output LO 1: GPIO output HI
3	**GPIO3**	GPIO3_OUT	**GPIO3 data output value** 0: GPIO output LO 1: GPIO output HI
2	**GPIO2**	GPIO2_OUT	**GPIO2 data output value** 0: GPIO output LO 1: GPIO output HI
1	**GPIO1**	GPIO1_OUT	**GPIO1 data output value** 0: GPIO output LO 1: GPIO output HI
0	**GPIO0**	GPIO0_OUT	**GPIO0 data output value** 0: GPIO output LO 1: GPIO output HI

A20B0024 GPIO_DOUT_B GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_OUT
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_OUT	GPIO46_OUT	GPIO45_OUT	GPIO44_OUT	GPIO43_OUT	GPIO42_OUT	GPIO41_OUT	GPIO40_OUT	GPIO39_OUT	GPIO38_OUT	GPIO37_OUT	GPIO36_OUT	GPIO35_OUT	GPIO34_OUT	GPIO33_OUT	GPIO32_OUT
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_OUT	**GPIO48 data output value** 0: GPIO output LO 1: GPIO output HI
15	**GPIO47**	GPIO47_OUT	**GPIO47 data output value** 0: GPIO output LO 1: GPIO output HI
14	**GPIO46**	GPIO46_OUT	**GPIO46 data output value** 0: GPIO output LO 1: GPIO output HI
13	**GPIO45**	GPIO45_OUT	**GPIO45 data output value** 0: GPIO output LO 1: GPIO output HI
12	**GPIO44**	GPIO44_OUT	**GPIO44 data output value** 0: GPIO output LO 1: GPIO output HI
11	**GPIO43**	GPIO43_OUT	**GPIO43 data output value** 0: GPIO output LO 1: GPIO output HI
10	**GPIO42**	GPIO42_OUT	**GPIO42 data output value** 0: GPIO output LO 1: GPIO output HI
9	**GPIO41**	GPIO41_OUT	**GPIO41 data output value**

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Bit(s)	Mnemonic	Name	Description
			0: GPIO output LO 1: GPIO output HI
8	**GPIO40**	GPIO40_OUT	**GPIO40 data output value** 0: GPIO output LO 1: GPIO output HI
7	**GPIO39**	GPIO39_OUT	**GPIO39 data output value** 0: GPIO output LO 1: GPIO output HI
6	**GPIO38**	GPIO38_OUT	**GPIO38 data output value** 0: GPIO output LO 1: GPIO output HI
5	**GPIO37**	GPIO37_OUT	**GPIO37 data output value** 0: GPIO output LO 1: GPIO output HI
4	**GPIO36**	GPIO36_OUT	**GPIO36 data output value** 0: GPIO output LO 1: GPIO output HI
3	**GPIO35**	GPIO35_OUT	**GPIO35 data output value** 0: GPIO output LO 1: GPIO output HI
2	**GPIO34**	GPIO34_OUT	**GPIO34 data output value** 0: GPIO output LO 1: GPIO output HI
1	**GPIO33**	GPIO33_OUT	**GPIO33 data output value** 0: GPIO output LO 1: GPIO output HI
0	**GPIO32**	GPIO32_OUT	**GPIO32 data output value** 0: GPIO output LO 1: GPIO output HI

A20B0028 GPIO_DOUT_A_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_OUT_SET	GPIO30_OUT_SET	GPIO29_OUT_SET	GPIO28_OUT_SET	GPIO27_OUT_SET	GPIO26_OUT_SET	GPIO25_OUT_SET	GPIO24_OUT_SET	GPIO23_OUT_SET	GPIO22_OUT_SET	GPIO21_OUT_SET	GPIO20_OUT_SET	GPIO19_OUT_SET	GPIO18_OUT_SET	GPIO17_OUT_SET	GPIO16_OUT_SET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_OUT_SET	GPIO14_OUT_SET	GPIO13_OUT_SET	GPIO12_OUT_SET	GPIO11_OUT_SET	GPIO10_OUT_SET	GPIO9_OUT_SET	GPIO8_OUT_SET	GPIO7_OUT_SET	GPIO6_OUT_SET	GPIO5_OUT_SET	GPIO4_OUT_SET	GPIO3_OUT_SET	GPIO2_OUT_SET	GPIO1_OUT_SET	GPIO0_OUT_SET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_OUT_SET	**Bitwise SET operation of GPIO31 data output value** 0: Keep 1: SET bits
30	**GPIO30**	GPIO30_OUT_SET	**Bitwise SET operation of GPIO30 data output value** 0: Keep 1: SET bits

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Bit(s)	Mnemonic	Name	Description
29	**GPIO29**	GPIO29_OUT_SET	**Bitwise SET operation of GPIO29 data output value** 0: Keep 1: SET bits
28	**GPIO28**	GPIO28_OUT_SET	**Bitwise SET operation of GPIO28 data output value** 0: Keep 1: SET bits
27	**GPIO27**	GPIO27_OUT_SET	**Bitwise SET operation of GPIO27 data output value** 0: Keep 1: SET bits
26	**GPIO26**	GPIO26_OUT_SET	**Bitwise SET operation of GPIO26 data output value** 0: Keep 1: SET bits
25	**GPIO25**	GPIO25_OUT_SET	**Bitwise SET operation of GPIO25 data output value** 0: Keep 1: SET bits
24	**GPIO24**	GPIO24_OUT_SET	**Bitwise SET operation of GPIO24 data output value** 0: Keep 1: SET bits
23	**GPIO23**	GPIO23_OUT_SET	**Bitwise SET operation of GPIO23 data output value** 0: Keep 1: SET bits
22	**GPIO22**	GPIO22_OUT_SET	**Bitwise SET operation of GPIO22 data output value** 0: Keep 1: SET bits
21	**GPIO21**	GPIO21_OUT_SET	**Bitwise SET operation of GPIO21 data output value** 0: Keep 1: SET bits
20	**GPIO20**	GPIO20_OUT_SET	**Bitwise SET operation of GPIO20 data output value** 0: Keep 1: SET bits
19	**GPIO19**	GPIO19_OUT_SET	**Bitwise SET operation of GPIO19 data output value** 0: Keep 1: SET bits
18	**GPIO18**	GPIO18_OUT_SET	**Bitwise SET operation of GPIO18 data output value** 0: Keep 1: SET bits
17	**GPIO17**	GPIO17_OUT_SET	**Bitwise SET operation of GPIO17 data output value** 0: Keep 1: SET bits
16	**GPIO16**	GPIO16_OUT_SET	**Bitwise SET operation of GPIO16 data output value** 0: Keep 1: SET bits
15	**GPIO15**	GPIO15_OUT_SET	**Bitwise SET operation of GPIO15 data output**

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Bit(s)	Mnemonic	Name	Description
			value 0: Keep 1: SET bits
14	**GPIO14**	GPIO14_OUT_SET	**Bitwise SET operation of GPIO14 data output value** 0: Keep 1: SET bits
13	**GPIO13**	GPIO13_OUT_SET	**Bitwise SET operation of GPIO13 data output value** 0: Keep 1: SET bits
12	**GPIO12**	GPIO12_OUT_SET	**Bitwise SET operation of GPIO12 data output value** 0: Keep 1: SET bits
11	**GPIO11**	GPIO11_OUT_SET	**Bitwise SET operation of GPIO11 data output value** 0: Keep 1: SET bits
10	**GPIO10**	GPIO10_OUT_SET	**Bitwise SET operation of GPIO10 data output value** 0: Keep 1: SET bits
9	**GPIO9**	GPIO9_OUT_SET	**Bitwise SET operation of GPIO9 data output value** 0: Keep 1: SET bits
8	**GPIO8**	GPIO8_OUT_SET	**Bitwise SET operation of GPIO8 data output value** 0: Keep 1: SET bits
7	**GPIO7**	GPIO7_OUT_SET	**Bitwise SET operation of GPIO7 data output value** 0: Keep 1: SET bits
6	**GPIO6**	GPIO6_OUT_SET	**Bitwise SET operation of GPIO6 data output value** 0: Keep 1: SET bits
5	**GPIO5**	GPIO5_OUT_SET	**Bitwise SET operation of GPIO5 data output value** 0: Keep 1: SET bits
4	**GPIO4**	GPIO4_OUT_SET	**Bitwise SET operation of GPIO4 data output value** 0: Keep 1: SET bits
3	**GPIO3**	GPIO3_OUT_SET	**Bitwise SET operation of GPIO3 data output value** 0: Keep 1: SET bits
2	**GPIO2**	GPIO2_OUT_SET	**Bitwise SET operation of GPIO2 data output value** 0: Keep 1: SET bits
1	**GPIO1**	GPIO1_OUT_SET	**Bitwise SET operation of GPIO1 data output value**

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Bit(s)	Mnemonic	Name	Description
			0: Keep 1: SET bits
0	**GPIO0**	GPIO0_OUT_SET	**Bitwise SET operation of GPIO0 data output value** 0: Keep 1: SET bits

A20B002C GPIO_DOUT_B_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_OUT_SET
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_OUT_SET	GPIO46_OUT_SET	GPIO45_OUT_SET	GPIO44_OUT_SET	GPIO43_OUT_SET	GPIO42_OUT_SET	GPIO41_OUT_SET	GPIO40_OUT_SET	GPIO39_OUT_SET	GPIO38_OUT_SET	GPIO37_OUT_SET	GPIO36_OUT_SET	GPIO35_OUT_SET	GPIO34_OUT_SET	GPIO33_OUT_SET	GPIO32_OUT_SET
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_OUT_SET	**Bitwise SET operation of GPIO48 data output value** 0: Keep 1: SET bits
15	**GPIO47**	GPIO47_OUT_SET	**Bitwise SET operation of GPIO47 data output value** 0: Keep 1: SET bits
14	**GPIO46**	GPIO46_OUT_SET	**Bitwise SET operation of GPIO46 data output value** 0: Keep 1: SET bits
13	**GPIO45**	GPIO45_OUT_SET	**Bitwise SET operation of GPIO45 data output value** 0: Keep 1: SET bits
12	**GPIO44**	GPIO44_OUT_SET	**Bitwise SET operation of GPIO44 data output value** 0: Keep 1: SET bits
11	**GPIO43**	GPIO43_OUT_SET	**Bitwise SET operation of GPIO43 data output value** 0: Keep 1: SET bits
10	**GPIO42**	GPIO42_OUT_SET	**Bitwise SET operation of GPIO42 data output value** 0: Keep 1: SET bits
9	**GPIO41**	GPIO41_OUT_SET	**Bitwise SET operation of GPIO41 data output value** 0: Keep 1: SET bits

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Bit(s)	Mnemonic	Name	Description
8	**GPIO40**	GPIO40_OUT_SET	**Bitwise SET operation of GPIO40 data output value** 0: Keep 1: SET bits
7	**GPIO39**	GPIO39_OUT_SET	**Bitwise SET operation of GPIO39 data output value** 0: Keep 1: SET bits
6	**GPIO38**	GPIO38_OUT_SET	**Bitwise SET operation of GPIO38 data output value** 0: Keep 1: SET bits
5	**GPIO37**	GPIO37_OUT_SET	**Bitwise SET operation of GPIO37 data output value** 0: Keep 1: SET bits
4	**GPIO36**	GPIO36_OUT_SET	**Bitwise SET operation of GPIO36 data output value** 0: Keep 1: SET bits
3	**GPIO35**	GPIO35_OUT_SET	**Bitwise SET operation of GPIO35 data output value** 0: Keep 1: SET bits
2	**GPIO34**	GPIO34_OUT_SET	**Bitwise SET operation of GPIO34 data output value** 0: Keep 1: SET bits
1	**GPIO33**	GPIO33_OUT_SET	**Bitwise SET operation of GPIO33 data output value** 0: Keep 1: SET bits
0	**GPIO32**	GPIO32_OUT_SET	**Bitwise SET operation of GPIO32 data output value** 0: Keep 1: SET bits

A20B0030 GPIO_DOUT_A_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_OUT_CLR	GPIO30_OUT_CLR	GPIO29_OUT_CLR	GPIO28_OUT_CLR	GPIO27_OUT_CLR	GPIO26_OUT_CLR	GPIO25_OUT_CLR	GPIO24_OUT_CLR	GPIO23_OUT_CLR	GPIO22_OUT_CLR	GPIO21_OUT_CLR	GPIO20_OUT_CLR	GPIO19_OUT_CLR	GPIO18_OUT_CLR	GPIO17_OUT_CLR	GPIO16_OUT_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_OUT_CLR	GPIO14_OUT_CLR	GPIO13_OUT_CLR	GPIO12_OUT_CLR	GPIO11_OUT_CLR	GPIO10_OUT_CLR	GPIO9_OUT_CLR	GPIO8_OUT_CLR	GPIO7_OUT_CLR	GPIO6_OUT_CLR	GPIO5_OUT_CLR	GPIO4_OUT_CLR	GPIO3_OUT_CLR	GPIO2_OUT_CLR	GPIO1_OUT_CLR	GPIO0_OUT_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_OUT_CLR	**Bitwise CLEAR operation of GPIO31 data output value**

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Bit(s)	Mnemonic	Name	Description
			0: Keep 1: CLEAR bits
30	**GPIO30**	GPIO30_OUT_CLR	**Bitwise CLEAR operation of GPIO30 data output value** 0: Keep 1: CLEAR bits
29	**GPIO29**	GPIO29_OUT_CLR	**Bitwise CLEAR operation of GPIO29 data output value** 0: Keep 1: CLEAR bits
28	**GPIO28**	GPIO28_OUT_CLR	**Bitwise CLEAR operation of GPIO28 data output value** 0: Keep 1: CLEAR bits
27	**GPIO27**	GPIO27_OUT_CLR	**Bitwise CLEAR operation of GPIO27 data output value** 0: Keep 1: CLEAR bits
26	**GPIO26**	GPIO26_OUT_CLR	**Bitwise CLEAR operation of GPIO26 data output value** 0: Keep 1: CLEAR bits
25	**GPIO25**	GPIO25_OUT_CLR	**Bitwise CLEAR operation of GPIO25 data output value** 0: Keep 1: CLEAR bits
24	**GPIO24**	GPIO24_OUT_CLR	**Bitwise CLEAR operation of GPIO24 data output value** 0: Keep 1: CLEAR bits
23	**GPIO23**	GPIO23_OUT_CLR	**Bitwise CLEAR operation of GPIO23 data output value** 0: Keep 1: CLEAR bits
22	**GPIO22**	GPIO22_OUT_CLR	**Bitwise CLEAR operation of GPIO22 data output value** 0: Keep 1: CLEAR bits
21	**GPIO21**	GPIO21_OUT_CLR	**Bitwise CLEAR operation of GPIO21 data output value** 0: Keep 1: CLEAR bits
20	**GPIO20**	GPIO20_OUT_CLR	**Bitwise CLEAR operation of GPIO20 data output value** 0: Keep 1: CLEAR bits
19	**GPIO19**	GPIO19_OUT_CLR	**Bitwise CLEAR operation of GPIO19 data output value** 0: Keep 1: CLEAR bits
18	**GPIO18**	GPIO18_OUT_CLR	**Bitwise CLEAR operation of GPIO18 data output value** 0: Keep 1: CLEAR bits
17	**GPIO17**	GPIO17_OUT_CLR	**Bitwise CLEAR operation of GPIO17 data output value** 0: Keep

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Bit(s)	Mnemonic	Name	Description
			1: CLEAR bits
16	**GPIO16**	GPIO16_OUT_CLR	**Bitwise CLEAR operation of GPIO16 data output value** 0: Keep 1: CLEAR bits
15	**GPIO15**	GPIO15_OUT_CLR	**Bitwise CLEAR operation of GPIO15 data output value** 0: Keep 1: CLEAR bits
14	**GPIO14**	GPIO14_OUT_CLR	**Bitwise CLEAR operation of GPIO14 data output value** 0: Keep 1: CLEAR bits
13	**GPIO13**	GPIO13_OUT_CLR	**Bitwise CLEAR operation of GPIO13 data output value** 0: Keep 1: CLEAR bits
12	**GPIO12**	GPIO12_OUT_CLR	**Bitwise CLEAR operation of GPIO12 data output value** 0: Keep 1: CLEAR bits
11	**GPIO11**	GPIO11_OUT_CLR	**Bitwise CLEAR operation of GPIO11 data output value** 0: Keep 1: CLEAR bits
10	**GPIO10**	GPIO10_OUT_CLR	**Bitwise CLEAR operation of GPIO10 data output value** 0: Keep 1: CLEAR bits
9	**GPIO9**	GPIO9_OUT_CLR	**Bitwise CLEAR operation of GPIO9 data output value** 0: Keep 1: CLEAR bits
8	**GPIO8**	GPIO8_OUT_CLR	**Bitwise CLEAR operation of GPIO8 data output value** 0: Keep 1: CLEAR bits
7	**GPIO7**	GPIO7_OUT_CLR	**Bitwise CLEAR operation of GPIO7 data output value** 0: Keep 1: CLEAR bits
6	**GPIO6**	GPIO6_OUT_CLR	**Bitwise CLEAR operation of GPIO6 data output value** 0: Keep 1: CLEAR bits
5	**GPIO5**	GPIO5_OUT_CLR	**Bitwise CLEAR operation of GPIO5 data output value** 0: Keep 1: CLEAR bits
4	**GPIO4**	GPIO4_OUT_CLR	**Bitwise CLEAR operation of GPIO4 data output value** 0: Keep 1: CLEAR bits
3	**GPIO3**	GPIO3_OUT_CLR	**Bitwise CLEAR operation of GPIO3 data output value** 0: Keep 1: CLEAR bits

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Bit(s)	Mnemonic	Name	Description
2	**GPIO2**	GPIO2_OUT_CLR	**Bitwise CLEAR operation of GPIO2 data output value** 0: Keep 1: CLEAR bits
1	**GPIO1**	GPIO1_OUT_CLR	**Bitwise CLEAR operation of GPIO1 data output value** 0: Keep 1: CLEAR bits
0	**GPIO0**	GPIO0_OUT_CLR	**Bitwise CLEAR operation of GPIO0 data output value** 0: Keep 1: CLEAR bits

A20B0034 GPIO_DOUT_B_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_OUT_CLR
Type																WO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_OUT_CLR	GPIO46_OUT_CLR	GPIO45_OUT_CLR	GPIO44_OUT_CLR	GPIO43_OUT_CLR	GPIO42_OUT_CLR	GPIO41_OUT_CLR	GPIO40_OUT_CLR	GPIO39_OUT_CLR	GPIO38_OUT_CLR	GPIO37_OUT_CLR	GPIO36_OUT_CLR	GPIO35_OUT_CLR	GPIO34_OUT_CLR	GPIO33_OUT_CLR	GPIO32_OUT_CLR
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_OUT_CLR	**Bitwise CLEAR operation of GPIO48 data output value** 0: Keep 1: CLEAR bits
15	**GPIO47**	GPIO47_OUT_CLR	**Bitwise CLEAR operation of GPIO47 data output value** 0: Keep 1: CLEAR bits
14	**GPIO46**	GPIO46_OUT_CLR	**Bitwise CLEAR operation of GPIO46 data output value** 0: Keep 1: CLEAR bits
13	**GPIO45**	GPIO45_OUT_CLR	**Bitwise CLEAR operation of GPIO45 data output value** 0: Keep 1: CLEAR bits
12	**GPIO44**	GPIO44_OUT_CLR	**Bitwise CLEAR operation of GPIO44 data output value** 0: Keep 1: CLEAR bits
11	**GPIO43**	GPIO43_OUT_CLR	**Bitwise CLEAR operation of GPIO43 data output value** 0: Keep 1: CLEAR bits
10	**GPIO42**	GPIO42_OUT_CLR	**Bitwise CLEAR operation of GPIO42 data output value**

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Bit(s)	Mnemonic	Name	Description
			0: Keep 1: CLEAR bits
9	**GPIO41**	GPIO41_OUT_CLR	**Bitwise CLEAR operation of GPIO41 data output value** 0: Keep 1: CLEAR bits
8	**GPIO40**	GPIO40_OUT_CLR	**Bitwise CLEAR operation of GPIO40 data output value** 0: Keep 1: CLEAR bits
7	**GPIO39**	GPIO39_OUT_CLR	**Bitwise CLEAR operation of GPIO39 data output value** 0: Keep 1: CLEAR bits
6	**GPIO38**	GPIO38_OUT_CLR	**Bitwise CLEAR operation of GPIO38 data output value** 0: Keep 1: CLEAR bits
5	**GPIO37**	GPIO37_OUT_CLR	**Bitwise CLEAR operation of GPIO37 data output value** 0: Keep 1: CLEAR bits
4	**GPIO36**	GPIO36_OUT_CLR	**Bitwise CLEAR operation of GPIO36 data output value** 0: Keep 1: CLEAR bits
3	**GPIO35**	GPIO35_OUT_CLR	**Bitwise CLEAR operation of GPIO35 data output value** 0: Keep 1: CLEAR bits
2	**GPIO34**	GPIO34_OUT_CLR	**Bitwise CLEAR operation of GPIO34 data output value** 0: Keep 1: CLEAR bits
1	**GPIO33**	GPIO33_OUT_CLR	**Bitwise CLEAR operation of GPIO33 data output value** 0: Keep 1: CLEAR bits
0	**GPIO32**	GPIO32_OUT_CLR	**Bitwise CLEAR operation of GPIO32 data output value** 0: Keep 1: CLEAR bits

A20B0040 GPIO_DIN_A GPIO Input Data Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31_DIN	GPIO30_DIN	GPIO29_DIN	GPIO28_DIN	GPIO27_DIN	GPIO26_DIN	GPIO25_DIN	GPIO24_DIN	GPIO23_DIN	GPIO22_DIN	GPIO21_DIN	GPIO20_DIN	GPIO19_DIN	GPIO18_DIN	GPIO17_DIN	GPIO16_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIN	GPIO14_DIN	GPIO13_DIN	GPIO12_DIN	GPIO11_DIN	GPIO10_DIN	GPIO9_DIN	GPIO8_DIN	GPIO7_DIN	GPIO6_DIN	GPIO5_DIN	GPIO4_DIN	GPIO3_DIN	GPIO2_DIN	GPIO1_DIN	GPIO0_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIN	**GPIO31 data input value**
30	**GPIO30**	GPIO30_DIN	**GPIO30 data input value**
29	**GPIO29**	GPIO29_DIN	**GPIO29 data input value**
28	**GPIO28**	GPIO28_DIN	**GPIO28 data input value**
27	**GPIO27**	GPIO27_DIN	**GPIO27 data input value**
26	**GPIO26**	GPIO26_DIN	**GPIO26 data input value**
25	**GPIO25**	GPIO25_DIN	**GPIO25 data input value**
24	**GPIO24**	GPIO24_DIN	**GPIO24 data input value**
23	**GPIO23**	GPIO23_DIN	**GPIO23 data input value**
22	**GPIO22**	GPIO22_DIN	**GPIO22 data input value**
21	**GPIO21**	GPIO21_DIN	**GPIO21 data input value**
20	**GPIO20**	GPIO20_DIN	**GPIO20 data input value**
19	**GPIO19**	GPIO19_DIN	**GPIO19 data input value**
18	**GPIO18**	GPIO18_DIN	**GPIO18 data input value**
17	**GPIO17**	GPIO17_DIN	**GPIO17 data input value**
16	**GPIO16**	GPIO16_DIN	**GPIO16 data input value**
15	**GPIO15**	GPIO15_DIN	**GPIO15 data input value**
14	**GPIO14**	GPIO14_DIN	**GPIO14 data input value**
13	**GPIO13**	GPIO13_DIN	**GPIO13 data input value**
12	**GPIO12**	GPIO12_DIN	**GPIO12 data input value**
11	**GPIO11**	GPIO11_DIN	**GPIO11 data input value**
10	**GPIO10**	GPIO10_DIN	**GPIO10 data input value**
9	**GPIO9**	GPIO9_DIN	**GPIO9 data input value**
8	**GPIO8**	GPIO8_DIN	**GPIO8 data input value**
7	**GPIO7**	GPIO7_DIN	**GPIO7 data input value**
6	**GPIO6**	GPIO6_DIN	**GPIO6 data input value**
5	**GPIO5**	GPIO5_DIN	**GPIO5 data input value**
4	**GPIO4**	GPIO4_DIN	**GPIO4 data input value**
3	**GPIO3**	GPIO3_DIN	**GPIO3 data input value**
2	**GPIO2**	GPIO2_DIN	**GPIO2 data input value**
1	**GPIO1**	GPIO1_DIN	**GPIO1 data input value**
0	**GPIO0**	GPIO0_DIN	**GPIO0 data input value**

A20B0044 GPIO_DIN_B GPIO Input Data Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																GPIO48_DIN
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47_DIN	GPIO46_DIN	GPIO45_DIN	GPIO44_DIN	GPIO43_DIN	GPIO42_DIN	GPIO41_DIN	GPIO40_DIN	GPIO39_DIN	GPIO38_DIN	GPIO37_DIN	GPIO36_DIN	GPIO35_DIN	GPIO34_DIN	GPIO33_DIN	GPIO32_DIN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**GPIO48**	GPIO48_DIN	**GPIO48 data input value**
15	**GPIO47**	GPIO47_DIN	**GPIO47 data input value**
14	**GPIO46**	GPIO46_DIN	**GPIO46 data input value**
13	**GPIO45**	GPIO45_DIN	**GPIO45 data input value**
12	**GPIO44**	GPIO44_DIN	**GPIO44 data input value**
11	**GPIO43**	GPIO43_DIN	**GPIO43 data input value**
10	**GPIO42**	GPIO42_DIN	**GPIO42 data input value**
9	**GPIO41**	GPIO41_DIN	**GPIO41 data input value**
8	**GPIO40**	GPIO40_DIN	**GPIO40 data input value**
7	**GPIO39**	GPIO39_DIN	**GPIO39 data input value**

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Bit(s)	Mnemonic	Name	Description
6	**GPIO38**	GPIO38_DIN	**GPIO38 data input value**
5	**GPIO37**	GPIO37_DIN	**GPIO37 data input value**
4	**GPIO36**	GPIO36_DIN	**GPIO36 data input value**
3	**GPIO35**	GPIO35_DIN	**GPIO35 data input value**
2	**GPIO34**	GPIO34_DIN	**GPIO34 data input value**
1	**GPIO33**	GPIO33_DIN	**GPIO33 data input value**
0	**GPIO32**	GPIO32_DIN	**GPIO32 data input value**

A20B0050 GPIO_MODE_A GPIO Mode Control 00100100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_GPIO7				MODE_GPIO6				MODE_GPIO5				MODE_GPIO4			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_GPIO3				MODE_GPIO2				MODE_GPIO1				MODE_GPIO0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_GPIO7	**Auxiliary mode of GPIO_7** 0:GPIO7(IO) 1:SDIO_SLV0_CMD(IO) 2:SPI_MST0_SIO2(IO) 3:I2S0_TX(O) 4:I2C0_SDA(IO) 5:PWM1(O) 6:GPS_FRAME_SYNC(O) 7:EINT7(I) 8:DEBUGMON7(IO)
27:24		MODE_GPIO6	**Auxiliary mode of GPIO_6** 0:GPIO6(IO) 1:SDIO_SLV0_DAT1(IO) 2:SPI_MST0_SIO3(IO) 3:I2S0_WS(IO) 4:I2C0_SCL(IO) 5:NBIOT_PRI(O) 6:GPS_BLANKING(O) 7:EINT6(I) 8:DEBUGMON6(IO)
23:20		MODE_GPIO5	**Auxiliary mode of GPIO_5** 0:GPIO5(IO) 1:UART0_TXD(O) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:EINT5(I) 8:DEBUGMON5(IO)
19:16		MODE_GPIO4	**Auxiliary mode of GPIO_4** 0:GPIO4(IO) 1:UART2_TXD(O) 2:I2C1_SDA(IO) 3:I2S0_MCLK(O) 4:KP_ROW1(IO) 5:UART1_TXD(O) 6:PWM0(O) 7:EINT4(I) 8:DEBUGMON4(IO)

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Bit(s)	Mnemonic	Name	Description
15:12		MODE_GPIO3	**Auxiliary mode of GPIO_3** 0:GPIO3(IO) 1:UART2_RXD(I) 2:I2C1_SCL(IO) 3:I2S0_CK(IO) 4:KP_ROW0(IO) 5:UART1_RXD(I) 6:CLKO0(O) 7:EINT3(I) 8:DEBUGMON3(IO)
11:8		MODE_GPIO2	**Auxiliary mode of GPIO_2** 0:GPIO2(IO) 1:UART0_RXD(I) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:EINT2(I) 8:DEBUGMON2(IO)
7:4		MODE_GPIO1	**Auxiliary mode of GPIO_1** 0:GPIO1(IO) 1:UART1_RTS(O) 2:I2C0_SDA(IO) 3:I2S0_RX(I) 4:KP_COL1(IO) 5:PWM0(O) 6:GPS_BLANKING(O) 7:EINT1(I) 8:DEBUGMON1(IO)
3:0		MODE_GPIO0	**Auxiliary mode of GPIO_0** 0:GPIO0(IO) 1:Reserved 2:Reserved 3:PWM0(O) 4:KP_COL0(IO) 5:CLKO0(O) 6:Reserved 7:Reserved 8:DEBUGMON0(IO)

A20B0054 GPIO_MODE_B GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_GPIO15				MODE_GPIO14				MODE_GPIO13				MODE_GPIO12			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_GPIO11				MODE_GPIO10				MODE_GPIO9				MODE_GPIO8			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_GPIO15	**Auxiliary mode of GPIO_15** 0:GPIO15(IO) 1:MSDC0_CLK(O) 2:SPI_SLV0_SCK(I) 3:UART1_CTS(I) 4:UART3_TXD(O) 5:PWM2(O)

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Bit(s)	Mnemonic	Name	Description
			6:PAD_DFUNC_SOUT(IO) 7:EINT15(I) 8:DEBUGMON15(IO)
27:24		MODE_GPIO14	**Auxiliary mode of GPIO_14** 0:GPIO14(IO) 1:MSDC0_DAT0(IO) 2:SPI_SLV0_MISO(IO) 3:UART1_RTS(O) 4:UART3_RXD(I) 5:CLKO2(O) 6:PAD_DFUNC_SIN(IO) 7:EINT14(I) 8:DEBUGMON14(IO)
23:20		MODE_GPIO13	**Auxiliary mode of GPIO_13** 0:GPIO13(IO) 1:MSDC0_CMD(IO) 2:SPI_SLV0_MOSI(IO) 3:UART1_TXD(O) 4:PWM2(O) 5:PWMSG0(O) 6:PAD_DFUNC_SHOLD(IO) 7:EINT13(I) 8:DEBUGMON13(IO)
19:16		MODE_GPIO12	**Auxiliary mode of GPIO_12** 0:GPIO12(IO) 1:MSDC0_DAT1(IO) 2:SPI_SLV0_CS(I) 3:UART1_RXD(I) 4:CLKO1(O) 5:PMU_GOTO_SLEEP(O) 6:PAD_DFUNC_SWP(IO) 7:EINT12(I) 8:DEBUGMON12(IO)
15:12		MODE_GPIO11	**Auxiliary mode of GPIO_11** 0:GPIO11(IO) 1:SDIO_SLV0_DAT2(IO) 2:SPI_MST0_SCK(O) 3:Reserved 4:GPS_BLANKING(O) 5:PMU_GOTO_SLEEP(O) 6:PWMSG0(O) 7:EINT11(I) 8:DEBUGMON11(IO)
11:8		MODE_GPIO10	**Auxiliary mode of GPIO_10** 0:GPIO10(IO) 1:SDIO_SLV0_DAT3(IO) 2:SPI_MST0_MOSI(IO) 3:I2C1_SCL(IO) 4:GPS_FRAME_SYNC(O) 5:PMU_RGU_RSTB(O) 6:CLKO1(O) 7:EINT10(I) 8:DEBUGMON10(IO)
7:4		MODE_GPIO9	**Auxiliary mode of GPIO_9** 0:GPIO9(IO) 1:SDIO_SLV0_CLK(IO) 2:SPI_MST0_MISO(IO) 3:I2S0_MCLK(O) 4:RF_CONFL_DET_IRQ_B(O) 5:WLAN_ACT(I) 6:PAD_DFUNC_SFCS0(O) 7:EINT9(I) 8:DEBUGMON9(IO)

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Bit(s)	Mnemonic	Name	Description
3:0		MODE_GPIO8	**Auxiliary mode of GPIO_8** 0:GPIO8(IO) 1:SDIO_SLV0_DAT0(IO) 2:SPI_MST0_CS(O) 3:I2S0_CK(IO) 4:PWM1(O) 5:NBIOT_ACT(O) 6:PAD_DFUNC_SFCK(O) 7:EINT8(I) 8:DEBUGMON8(IO)

A20B0058 GPIO_MODE_C GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_GPIO23				MODE_GPIO22				MODE_GPIO21				MODE_GPIO20			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_GPIO19				MODE_GPIO18				MODE_GPIO17				MODE_GPIO16			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_GPIO23	**Auxiliary mode of GPIO_23** 0:GPIO23(IO) 1:MSDC1_DAT3(IO) 2:SPI_MST1_SIO3(IO) 3:I2C1_SDA(IO) 4:UART2_TXD(O) 5:UART1_RTS(O) 6:Reserved 7:EINT0(I) 8:DEBUGMON3(IO)
27:24		MODE_GPIO22	**Auxiliary mode of GPIO_22** 0:GPIO22(IO) 1:MSDC1_CLK(O) 2:SPI_MST1_SCK(O) 3:I2C1_SCL(IO) 4:PMU_GOTO_SLEEP(O) 5:UART2_TXD(O) 6:Reserved 7:EINT22(I) 8:DEBUGMON2(IO)
23:20		MODE_GPIO21	**Auxiliary mode of GPIO_21** 0:GPIO21(IO) 1:MSDC1_DAT0(IO) 2:SPI_MST1_MOSI(IO) 3:Reserved 4:Reserved 5:PWMSG1(O) 6:Reserved 7:EINT21(I) 8:DEBUGMON1(IO)
19:16		MODE_GPIO20	**Auxiliary mode of GPIO_20** 0:GPIO20(IO) 1:MSDC1_CMD(IO) 2:SPI_MST1_MISO(IO) 3:MD_JTCK(I) 4:PWM3(O) 5:GSM_RF_CONFL_DET_EN(I)

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Bit(s)	Mnemonic	Name	Description
			6:Reserved 7:EINT20(I) 8:DEBUGMON0(IO)
15:12		MODE_GPIO19	**Auxiliary mode of GPIO_19** 0:GPIO19(IO) 1:MSDC1_DAT1(IO) 2:SPI_MST1_CS(O) 3:MD_JTMS(IO) 4:CLKO3(O) 5:GSM_TIMING_SYNC(I) 6:Reserved 7:EINT19(I) 8:DEBUGMON11(IO)
11:8		MODE_GPIO18	**Auxiliary mode of GPIO_18** 0:GPIO18(IO) 1:MSDC1_DAT2(IO) 2:SPI_MST1_SIO2(IO) 3:UART2_RXD(I) 4:UART1_CTS(I) 5:GPS_BLANKING(O) 6:RF_CONFL_DET_IRQ_B(O) 7:EINT18(I) 8:DEBUGMON10(IO)
7:4		MODE_GPIO17	**Auxiliary mode of GPIO_17** 0:GPIO17(IO) 1:MSDC0_DAT3(IO) 2:SPI_SLV0_SIO3(IO) 3:I2C1_SDA(IO) 4:UART1_TXD(O) 5:XO_WAKEUP(O) 6:Reserved 7:EINT17(I) 8:DEBUGMON5(IO)
3:0		MODE_GPIO16	**Auxiliary mode of GPIO_16** 0:GPIO16(IO) 1:MSDC0_DAT2(IO) 2:SPI_SLV0_SIO2(IO) 3:I2C1_SCL(IO) 4:UART1_RXD(I) 5:GPS_FRAME_SYNC(O) 6:PWMSG0(O) 7:EINT16(I)

A20B005C GPIO_MODE_D GPIO Mode Control 44000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_GPIO31				MODE_GPIO30				MODE_GPIO29				MODE_GPIO28			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_GPIO27				MODE_GPIO26				MODE_GPIO25				MODE_GPIO24			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_GPIO31	**Auxiliary mode of GPIO_31** 0:GPIO31(IO) 1:I2S1_TX(O) 2:AP_JRSTB(I) 3:UART2_RXD(I)

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Bit(s)	Mnemonic	Name	Description
			4:MD_JTCK(I) 5:Reserved 6:Reserved 7:EINT8(I) 8:DEBUGMON3(IO)
27:24		MODE_GPIO30	**Auxiliary mode of GPIO_30** 0:GPIO30(IO) 1:I2S1_RX(I) 2:AP_JTDI(I) 3:CLKO3(O) 4:MD_JTMS(IO) 5:Reserved 6:Reserved 7:EINT7(I) 8:DEBUGMON2(IO)
23:20		MODE_GPIO29	**Auxiliary mode of GPIO_29** 0:GPIO29(IO) 1:Reserved 2:UART2_TXD(O) 3:I2C2_SDA(IO) 4:WLAN_ACT(I) 5:CLKO4(O) 6:Reserved 7:EINT6(I) 8:DEBUGMON1(IO)
19:16		MODE_GPIO28	**Auxiliary mode of GPIO_28** 0:GPIO28(IO) 1:I2S0_MCLK(O) 2:UART2_RXD(I) 3:I2C2_SCL(IO) 4:NBIOT_ACT(O) 5:GPS_BLANKING(O) 6:Reserved 7:EINT5(I) 8:DEBUGMON0(IO)
15:12		MODE_GPIO27	**Auxiliary mode of GPIO_27** 0:GPIO27(IO) 1:I2S0_CK(IO) 2:UART2_CTS(I) 3:UART3_TXD(O) 4:NBIOT_PRI(O) 5:GPS_FRAME_SYNC(O) 6:RF_CONFL_DET_IRQ_B(O) 7:EINT4(I) 8:DEBUGMON6(IO)
11:8		MODE_GPIO26	**Auxiliary mode of GPIO_26** 0:GPIO26(IO) 1:I2S0_WS(IO) 2:UART2_RTS(O) 3:UART3_RXD(I) 4:PMU_GOTO_SLEEP(O) 5:PWM3(O) 6:GSM_RF_CONFL_DET_EN(I) 7:EINT3(I) 8:DEBUGMON5(IO)
7:4		MODE_GPIO25	**Auxiliary mode of GPIO_25** 0:GPIO25(IO) 1:I2S0_TX(O) 2:UART1_TXD(O) 3:Reserved 4:PMU_RGU_RSTB(O) 5:PWMSG1(O) 6:GSM_TIMING_SYNC(I)

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Bit(s)	Mnemonic	Name	Description
			7:EINT2(I) 8:DEBUGMON4(IO)
3:0		MODE_GPIO24	**Auxiliary mode of GPIO_24** 0:GPIO24(IO) 1:I2S0_RX(I) 2:UART1_RXD(I) 3:PWMSG1(O) 4:XO_WAKEUP(O) 5:CLKO3(O) 6:Reserved 7:EINT1(I) 8:DEBUGMON3(IO)

A20B0060 GPIO_MODE_E GPIO Mode Control 11100220

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_GPIO39				MODE_GPIO38				MODE_GPIO37				MODE_GPIO36			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_GPIO35				MODE_GPIO34				MODE_GPIO33				MODE_GPIO32			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_GPIO39	**Auxiliary mode of GPIO_39** 0:GPIO39(IO) 1:BPI2(O) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:DEBUGMON11(IO)
27:24		MODE_GPIO38	**Auxiliary mode of GPIO_38** 0:GPIO38(IO) 1:BPI1(O) 2:Reserved 3:Reserved 4:Reserved 5:NBIOT_ACT(O) 6:Reserved 7:Reserved 8:DEBUGMON10(IO)
23:20		MODE_GPIO37	**Auxiliary mode of GPIO_37** 0:GPIO37(IO) 1:BPI0(O) 2:Reserved 3:Reserved 4:Reserved 5:NBIOT_PRI(O) 6:Reserved 7:Reserved 8:DEBUGMON9(IO)
19:16		MODE_GPIO36	**Auxiliary mode of GPIO_36** 0:GPIO36(IO) 1:UART2_TXD(O) 2:I2C2_SDA(IO) 3:Reserved

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Bit(s)	Mnemonic	Name	Description
			4:KP_ROW2(IO) 5:GPS_BLANKING(O) 6:RF_CONFL_DET_IRQ_B(O) 7:EINT13(I) 8:DEBUGMON8(IO)
15:12		MODE_GPIO35	**Auxiliary mode of GPIO_35** 0:GPIO35(IO) 1:UART2_RXD(I) 2:I2C2_SCL(IO) 3:Reserved 4:KP_COL2(IO) 5:Reserved 6:CLKO0(O) 7:EINT12(I) 8:DEBUGMON7(IO)
11:8		MODE_GPIO34	**Auxiliary mode of GPIO_34** 0:GPIO34(IO) 1:I2S1_MCLK(O) 2:AP_JTCK(I) 3:UART3_TXD(O) 4:I2C2_SDA(IO) 5:Reserved 6:WLAN_ACT(I) 7:EINT11(I) 8:Reserved
7:4		MODE_GPIO33	**Auxiliary mode of GPIO_33** 0:GPIO33(IO) 1:I2S1_CK(IO) 2:AP_JTMS(IO) 3:UART3_RXD(I) 4:I2C2_SCL(IO) 5:Reserved 6:Reserved 7:EINT10(I) 8:Reserved
3:0		MODE_GPIO32	**Auxiliary mode of GPIO_32** 0:GPIO32(IO) 1:I2S1_WS(IO) 2:AP_JTDO(O) 3:UART2_TXD(O) 4:CLKO4(O) 5:Reserved 6:PWM3(O) 7:EINT9(I) 8:DEBUGMON6(IO)

A20B0064 GPIO_MODE_F GPIO Mode Control 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_GPIO47				MODE_GPIO46				MODE_GPIO45				MODE_GPIO44			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_GPIO43				MODE_GPIO42				MODE_GPIO41				MODE_GPIO40			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:28		MODE_GPIO47	**Auxiliary mode of GPIO_47** 0:GPIO47(IO)

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Bit(s)	Mnemonic	Name	Description
			1:RESETB_OUT(O) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:Reserved
27:24		MODE_GPIO46	**Auxiliary mode of GPIO_46** 0:GPIO46(IO) 1:SIM0_SCLK(IO) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:Reserved
23:20		MODE_GPIO45	**Auxiliary mode of GPIO_45** 0:GPIO45(IO) 1:SIM0_SRST(IO) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:Reserved
19:16		MODE_GPIO44	**Auxiliary mode of GPIO_44** 0:GPIO44(IO) 1:SIM0_SIO(IO) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:Reserved
15:12		MODE_GPIO43	**Auxiliary mode of GPIO_43** 0:GPIO43(IO) 1:MIPI_SDATA(IO) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:DEBUGMON15(IO)
11:8		MODE_GPIO42	**Auxiliary mode of GPIO_42** 0:GPIO42(IO) 1:MIPI_SCLK(O) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:DEBUGMON14(IO)
7:4		MODE_GPIO41	**Auxiliary mode of GPIO_41** 0:GPIO41(IO) 1:BPI4(O) 2:Reserved 3:Reserved

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Bit(s)	Mnemonic	Name	Description
3:0		MODE_GPIO40	4:Reserved 5:PMU_GOTO_SLEEP(O) 6:RF_CONFL_DET_IRQ_B(O) 7:Reserved 8:DEBUGMON13(IO) **Auxiliary mode of GPIO_40** 0:GPIO40(IO) 1:BPI3(O) 2:Reserved 3:Reserved 4:Reserved 5:PMU_RGU_RSTB(O) 6:Reserved 7:Reserved 8:DEBUGMON12(IO)

A20B0068 GPIO_MODE_G GPIO Mode Control 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MODE_GPIO48			
Type													RW			
Reset													0	0	0	1

Bit(s)	Mnemonic	Name	Description
3:0		MODE_GPIO48	**Auxiliary mode of GPIO_48** 0:GPIO48(IO) 1:SRCLKENAI(I) 2:Reserved 3:Reserved 4:Reserved 5:Reserved 6:Reserved 7:Reserved 8:Reserved

A20B0070 GPIO_MODE_A_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_SET_GPIO7				MODE_SET_GPIO6				MODE_SET_GPIO5				MODE_SET_GPIO4			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_SET_GPIO3				MODE_SET_GPIO2				MODE_SET_GPIO1				MODE_SET_GPIO0			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_SET_GPIO7	**Bitwise SET operation for auxiliary mode of GPIO_7** 0: Keep 1: SET bits
27:24		MODE_SET_GPIO6	**Bitwise SET operation for auxiliary mode of**

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Bit(s)	Mnemonic	Name	Description
			GPIO_6 0: Keep 1: SET bits
23:20		MODE_SET_GPIO5	**Bitwise SET operation for auxiliary mode of GPIO_5** 0: Keep 1: SET bits
19:16		MODE_SET_GPIO4	**Bitwise SET operation for auxiliary mode of GPIO_4** 0: Keep 1: SET bits
15:12		MODE_SET_GPIO3	**Bitwise SET operation for auxiliary mode of GPIO_3** 0: Keep 1: SET bits
11:8		MODE_SET_GPIO2	**Bitwise SET operation for auxiliary mode of GPIO_2** 0: Keep 1: SET bits
7:4		MODE_SET_GPIO1	**Bitwise SET operation for auxiliary mode of GPIO_1** 0: Keep 1: SET bits
3:0		MODE_SET_GPIO0	**Bitwise SET operation for auxiliary mode of GPIO_0** 0: Keep 1: SET bits

A20B0074 GPIO_MODE_B_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_SET_GPIO15				MODE_SET_GPIO14				MODE_SET_GPIO13				MODE_SET_GPIO12			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_SET_GPIO11				MODE_SET_GPIO10				MODE_SET_GPIO9				MODE_SET_GPIO8			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_SET_GPIO15	**Bitwise SET operation for auxiliary mode of GPIO_15** 0: Keep 1: SET bits
27:24		MODE_SET_GPIO14	**Bitwise SET operation for auxiliary mode of GPIO_14** 0: Keep 1: SET bits
23:20		MODE_SET_GPIO13	**Bitwise SET operation for auxiliary mode of GPIO_13** 0: Keep 1: SET bits
19:16		MODE_SET_GPIO12	**Bitwise SET operation for auxiliary mode of GPIO_12** 0: Keep 1: SET bits

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Bit(s)	Mnemonic	Name	Description
15:12		MODE_SET_GPIO11	**Bitwise SET operation for auxiliary mode of GPIO_11** 0: Keep 1: SET bits
11:8		MODE_SET_GPIO10	**Bitwise SET operation for auxiliary mode of GPIO_10** 0: Keep 1: SET bits
7:4		MODE_SET_GPIO9	**Bitwise SET operation for auxiliary mode of GPIO_9** 0: Keep 1: SET bits
3:0		MODE_SET_GPIO8	**Bitwise SET operation for auxiliary mode of GPIO_8** 0: Keep 1: SET bits

A20B0078 GPIO_MODE_C_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_SET_GPIO23				MODE_SET_GPIO22				MODE_SET_GPIO21				MODE_SET_GPIO20			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_SET_GPIO19				MODE_SET_GPIO18				MODE_SET_GPIO17				MODE_SET_GPIO16			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_SET_GPIO23	**Bitwise SET operation for auxiliary mode of GPIO_23** 0: Keep 1: SET bits
27:24		MODE_SET_GPIO22	**Bitwise SET operation for auxiliary mode of GPIO_22** 0: Keep 1: SET bits
23:20		MODE_SET_GPIO21	**Bitwise SET operation for auxiliary mode of GPIO_21** 0: Keep 1: SET bits
19:16		MODE_SET_GPIO20	**Bitwise SET operation for auxiliary mode of GPIO_20** 0: Keep 1: SET bits
15:12		MODE_SET_GPIO19	**Bitwise SET operation for auxiliary mode of GPIO_19** 0: Keep 1: SET bits
11:8		MODE_SET_GPIO18	**Bitwise SET operation for auxiliary mode of GPIO_18** 0: Keep 1: SET bits
7:4		MODE_SET_GPIO17	**Bitwise SET operation for auxiliary mode of GPIO_17** 0: Keep

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Bit(s)	Mnemonic	Name	Description
			1: SET bits
3:0		MODE_SET_GPIO16	**Bitwise SET operation for auxiliary mode of GPIO_16** 0: Keep 1: SET bits

A20B007C GPIO_MODE_D_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_SET_GPIO31				MODE_SET_GPIO30				MODE_SET_GPIO29				MODE_SET_GPIO28			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_SET_GPIO27				MODE_SET_GPIO26				MODE_SET_GPIO25				MODE_SET_GPIO24			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_SET_GPIO31	**Bitwise SET operation for auxiliary mode of GPIO_31** 0: Keep 1: SET bits
27:24		MODE_SET_GPIO30	**Bitwise SET operation for auxiliary mode of GPIO_30** 0: Keep 1: SET bits
23:20		MODE_SET_GPIO29	**Bitwise SET operation for auxiliary mode of GPIO_29** 0: Keep 1: SET bits
19:16		MODE_SET_GPIO28	**Bitwise SET operation for auxiliary mode of GPIO_28** 0: Keep 1: SET bits
15:12		MODE_SET_GPIO27	**Bitwise SET operation for auxiliary mode of GPIO_27** 0: Keep 1: SET bits
11:8		MODE_SET_GPIO26	**Bitwise SET operation for auxiliary mode of GPIO_26** 0: Keep 1: SET bits
7:4		MODE_SET_GPIO25	**Bitwise SET operation for auxiliary mode of GPIO_25** 0: Keep 1: SET bits
3:0		MODE_SET_GPIO24	**Bitwise SET operation for auxiliary mode of GPIO_24** 0: Keep 1: SET bits

A20B0080 GPIO_MODE_E_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_SET_GPIO39				MODE_SET_GPIO38				MODE_SET_GPIO37				MODE_SET_GPIO36			

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Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_SET_GPIO35				MODE_SET_GPIO34				MODE_SET_GPIO33				MODE_SET_GPIO32			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_SET_GPIO39	**Bitwise SET operation for auxiliary mode of GPIO_39** 0: Keep 1: SET bits
27:24		MODE_SET_GPIO38	**Bitwise SET operation for auxiliary mode of GPIO_38** 0: Keep 1: SET bits
23:20		MODE_SET_GPIO37	**Bitwise SET operation for auxiliary mode of GPIO_37** 0: Keep 1: SET bits
19:16		MODE_SET_GPIO36	**Bitwise SET operation for auxiliary mode of GPIO_36** 0: Keep 1: SET bits
15:12		MODE_SET_GPIO35	**Bitwise SET operation for auxiliary mode of GPIO_35** 0: Keep 1: SET bits
11:8		MODE_SET_GPIO34	**Bitwise SET operation for auxiliary mode of GPIO_34** 0: Keep 1: SET bits
7:4		MODE_SET_GPIO33	**Bitwise SET operation for auxiliary mode of GPIO_33** 0: Keep 1: SET bits
3:0		MODE_SET_GPIO32	**Bitwise SET operation for auxiliary mode of GPIO_32** 0: Keep 1: SET bits

A20B0084 GPIO_MODE_F_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_SET_GPIO47				MODE_SET_GPIO46				MODE_SET_GPIO45				MODE_SET_GPIO44			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_SET_GPIO43				MODE_SET_GPIO42				MODE_SET_GPIO41				MODE_SET_GPIO40			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_SET_GPIO47	**Bitwise SET operation for auxiliary mode of GPIO_47** 0: Keep 1: SET bits

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Bit(s)	Mnemonic	Name	Description
27:24		MODE_SET_GPIO46	**Bitwise SET operation for auxiliary mode of GPIO_46** 0: Keep 1: SET bits
23:20		MODE_SET_GPIO45	**Bitwise SET operation for auxiliary mode of GPIO_45** 0: Keep 1: SET bits
19:16		MODE_SET_GPIO44	**Bitwise SET operation for auxiliary mode of GPIO_44** 0: Keep 1: SET bits
15:12		MODE_SET_GPIO43	**Bitwise SET operation for auxiliary mode of GPIO_43** 0: Keep 1: SET bits
11:8		MODE_SET_GPIO42	**Bitwise SET operation for auxiliary mode of GPIO_42** 0: Keep 1: SET bits
7:4		MODE_SET_GPIO41	**Bitwise SET operation for auxiliary mode of GPIO_41** 0: Keep 1: SET bits
3:0		MODE_SET_GPIO40	**Bitwise SET operation for auxiliary mode of GPIO_40** 0: Keep 1: SET bits

A20B0088 GPIO_MODE_G_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MODE_SET_GPIO48			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		MODE_SET_GPIO48	**Bitwise SET operation for auxiliary mode of GPIO_48** 0: Keep 1: SET bits

A20B0090 GPIO_MODE_A_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CLR_GPIO7				MODE_CLR_GPIO6				MODE_CLR_GPIO5				MODE_CLR_GPIO4			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_CLR_GPIO3				MODE_CLR_GPIO2				MODE_CLR_GPIO1				MODE_CLR_GPIO0			

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Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_CLR_GPIO7	**Bitwise CLEAR operation for auxiliary mode of GPIO_7** 0: Keep 1: CLEAR bits
27:24		MODE_CLR_GPIO6	**Bitwise CLEAR operation for auxiliary mode of GPIO_6** 0: Keep 1: CLEAR bits
23:20		MODE_CLR_GPIO5	**Bitwise CLEAR operation for auxiliary mode of GPIO_5** 0: Keep 1: CLEAR bits
19:16		MODE_CLR_GPIO4	**Bitwise CLEAR operation for auxiliary mode of GPIO_4** 0: Keep 1: CLEAR bits
15:12		MODE_CLR_GPIO3	**Bitwise CLEAR operation for auxiliary mode of GPIO_3** 0: Keep 1: CLEAR bits
11:8		MODE_CLR_GPIO2	**Bitwise CLEAR operation for auxiliary mode of GPIO_2** 0: Keep 1: CLEAR bits
7:4		MODE_CLR_GPIO1	**Bitwise CLEAR operation for auxiliary mode of GPIO_1** 0: Keep 1: CLEAR bits
3:0		MODE_CLR_GPIO0	**Bitwise CLEAR operation for auxiliary mode of GPIO_0** 0: Keep 1: CLEAR bits

A20B0094 GPIO_MODE_B_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CLR_GPIO15				MODE_CLR_GPIO14				MODE_CLR_GPIO13				MODE_CLR_GPIO12			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_CLR_GPIO11				MODE_CLR_GPIO10				MODE_CLR_GPIO9				MODE_CLR_GPIO8			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_CLR_GPIO15	**Bitwise CLEAR operation for auxiliary mode of GPIO_15** 0: Keep 1: CLEAR bits
27:24		MODE_CLR_GPIO14	**Bitwise CLEAR operation for auxiliary mode of GPIO_14** 0: Keep 1: CLEAR bits

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Bit(s)	Mnemonic	Name	Description
23:20		MODE_CLR_GPIO13	**Bitwise CLEAR operation for auxiliary mode of GPIO_13** 0: Keep 1: CLEAR bits
19:16		MODE_CLR_GPIO12	**Bitwise CLEAR operation for auxiliary mode of GPIO_12** 0: Keep 1: CLEAR bits
15:12		MODE_CLR_GPIO11	**Bitwise CLEAR operation for auxiliary mode of GPIO_11** 0: Keep 1: CLEAR bits
11:8		MODE_CLR_GPIO10	**Bitwise CLEAR operation for auxiliary mode of GPIO_10** 0: Keep 1: CLEAR bits
7:4		MODE_CLR_GPIO9	**Bitwise CLEAR operation for auxiliary mode of GPIO_9** 0: Keep 1: CLEAR bits
3:0		MODE_CLR_GPIO8	**Bitwise CLEAR operation for auxiliary mode of GPIO_8** 0: Keep 1: CLEAR bits

A20B0098 GPIO_MODE_C_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CLR_GPIO23				MODE_CLR_GPIO22				MODE_CLR_GPIO21				MODE_CLR_GPIO20			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_CLR_GPIO19				MODE_CLR_GPIO18				MODE_CLR_GPIO17				MODE_CLR_GPIO16			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_CLR_GPIO23	**Bitwise CLEAR operation for auxiliary mode of GPIO_23** 0: Keep 1: CLEAR bits
27:24		MODE_CLR_GPIO22	**Bitwise CLEAR operation for auxiliary mode of GPIO_22** 0: Keep 1: CLEAR bits
23:20		MODE_CLR_GPIO21	**Bitwise CLEAR operation for auxiliary mode of GPIO_21** 0: Keep 1: CLEAR bits
19:16		MODE_CLR_GPIO20	**Bitwise CLEAR operation for auxiliary mode of GPIO_20** 0: Keep 1: CLEAR bits
15:12		MODE_CLR_GPIO19	**Bitwise CLEAR operation for auxiliary mode of GPIO_19** 0: Keep

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Bit(s)	Mnemonic	Name	Description
			1: CLEAR bits
11:8		MODE_CLR_GPIO18	**Bitwise CLEAR operation for auxiliary mode of GPIO_18** 0: Keep 1: CLEAR bits
7:4		MODE_CLR_GPIO17	**Bitwise CLEAR operation for auxiliary mode of GPIO_17** 0: Keep 1: CLEAR bits
3:0		MODE_CLR_GPIO16	**Bitwise CLEAR operation for auxiliary mode of GPIO_16** 0: Keep 1: CLEAR bits

A20B009C GPIO_MODE_D_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CLR_GPIO31				MODE_CLR_GPIO30				MODE_CLR_GPIO29				MODE_CLR_GPIO28			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_CLR_GPIO27				MODE_CLR_GPIO26				MODE_CLR_GPIO25				MODE_CLR_GPIO24			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_CLR_GPIO31	**Bitwise CLEAR operation for auxiliary mode of GPIO_31** 0: Keep 1: CLEAR bits
27:24		MODE_CLR_GPIO30	**Bitwise CLEAR operation for auxiliary mode of GPIO_30** 0: Keep 1: CLEAR bits
23:20		MODE_CLR_GPIO29	**Bitwise CLEAR operation for auxiliary mode of GPIO_29** 0: Keep 1: CLEAR bits
19:16		MODE_CLR_GPIO28	**Bitwise CLEAR operation for auxiliary mode of GPIO_28** 0: Keep 1: CLEAR bits
15:12		MODE_CLR_GPIO27	**Bitwise CLEAR operation for auxiliary mode of GPIO_27** 0: Keep 1: CLEAR bits
11:8		MODE_CLR_GPIO26	**Bitwise CLEAR operation for auxiliary mode of GPIO_26** 0: Keep 1: CLEAR bits
7:4		MODE_CLR_GPIO25	**Bitwise CLEAR operation for auxiliary mode of GPIO_25** 0: Keep 1: CLEAR bits
3:0		MODE_CLR_GPIO24	**Bitwise CLEAR operation for auxiliary mode of GPIO_24**

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Bit(s)	Mnemonic	Name	Description
			0: Keep 1: CLEAR bits

A20B00A0 GPIO_MODE_E_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CLR_GPIO39				MODE_CLR_GPIO38				MODE_CLR_GPIO37				MODE_CLR_GPIO36			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MODE_CLR_GPIO35				MODE_CLR_GPIO34				MODE_CLR_GPIO33				MODE_CLR_GPIO32			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_CLR_GPIO39	**Bitwise CLEAR operation for auxiliary mode of GPIO_39** 0: Keep 1: CLEAR bits
27:24		MODE_CLR_GPIO38	**Bitwise CLEAR operation for auxiliary mode of GPIO_38** 0: Keep 1: CLEAR bits
23:20		MODE_CLR_GPIO37	**Bitwise CLEAR operation for auxiliary mode of GPIO_37** 0: Keep 1: CLEAR bits
19:16		MODE_CLR_GPIO36	**Bitwise CLEAR operation for auxiliary mode of GPIO_36** 0: Keep 1: CLEAR bits
15:12		MODE_CLR_GPIO35	**Bitwise CLEAR operation for auxiliary mode of GPIO_35** 0: Keep 1: CLEAR bits
11:8		MODE_CLR_GPIO34	**Bitwise CLEAR operation for auxiliary mode of GPIO_34** 0: Keep 1: CLEAR bits
7:4		MODE_CLR_GPIO33	**Bitwise CLEAR operation for auxiliary mode of GPIO_33** 0: Keep 1: CLEAR bits
3:0		MODE_CLR_GPIO32	**Bitwise CLEAR operation for auxiliary mode of GPIO_32** 0: Keep 1: CLEAR bits

A20B00A4 GPIO_MODE_F_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MODE_CLR_GPIO47				MODE_CLR_GPIO46				MODE_CLR_GPIO45				MODE_CLR_GPIO44			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	MODE_CLR_GPIO43				MODE_CLR_GPIO42				MODE_CLR_GPIO41				MODE_CLR_GPIO40			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:28		MODE_CLR_GPIO47	**Bitwise CLEAR operation for auxiliary mode of GPIO_47** 0: Keep 1: CLEAR bits
27:24		MODE_CLR_GPIO46	**Bitwise CLEAR operation for auxiliary mode of GPIO_46** 0: Keep 1: CLEAR bits
23:20		MODE_CLR_GPIO45	**Bitwise CLEAR operation for auxiliary mode of GPIO_45** 0: Keep 1: CLEAR bits
19:16		MODE_CLR_GPIO44	**Bitwise CLEAR operation for auxiliary mode of GPIO_44** 0: Keep 1: CLEAR bits
15:12		MODE_CLR_GPIO43	**Bitwise CLEAR operation for auxiliary mode of GPIO_43** 0: Keep 1: CLEAR bits
11:8		MODE_CLR_GPIO42	**Bitwise CLEAR operation for auxiliary mode of GPIO_42** 0: Keep 1: CLEAR bits
7:4		MODE_CLR_GPIO41	**Bitwise CLEAR operation for auxiliary mode of GPIO_41** 0: Keep 1: CLEAR bits
3:0		MODE_CLR_GPIO40	**Bitwise CLEAR operation for auxiliary mode of GPIO_40** 0: Keep 1: CLEAR bits

A20B00A8 GPIO_MODE_G_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													MODE_CLR_GPIO48			
Type													WO			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		MODE_CLR_GPIO48	**Bitwise CLEAR operation for auxiliary mode of GPIO_48** 0: Keep 1: CLEAR bits

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A20C0000 DRV_CFG0 **GPIO TX driving strength control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	drv_cfg_gpio_15		drv_cfg_gpio_14		drv_cfg_gpio_13		drv_cfg_gpio_12		drv_cfg_gpio_11		drv_cfg_gpio_10		drv_cfg_gpio_9		drv_cfg_gpio_8	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drv_cfg_gpio_7		drv_cfg_gpio_6		drv_cfg_gpio_5		drv_cfg_gpio_4		drv_cfg_gpio_3		drv_cfg_gpio_2		drv_cfg_gpio_1		drv_cfg_gpio_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		drv_cfg_gpio_15	**PAD_GPIO_15** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
29:28		drv_cfg_gpio_14	**PAD_GPIO_14** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
27:26		drv_cfg_gpio_13	**PAD_GPIO_13** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
25:24		drv_cfg_gpio_12	**PAD_GPIO_12** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
23:22		drv_cfg_gpio_11	**PAD_GPIO_11** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
21:20		drv_cfg_gpio_10	**PAD_GPIO_10** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
19:18		drv_cfg_gpio_9	**PAD_GPIO_9** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
17:16		drv_cfg_gpio_8	**PAD_GPIO_8** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]

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Bit(s)	Mnemonic	Name	Description
15:14		drv_cfg_gpio_7	**PAD_GPIO_7** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
13:12		drv_cfg_gpio_6	**PAD_GPIO_6** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
11:10		drv_cfg_gpio_5	**PAD_GPIO_5** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
9:8		drv_cfg_gpio_4	**PAD_GPIO_4** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
7:6		drv_cfg_gpio_3	**PAD_GPIO_3** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
5:4		drv_cfg_gpio_2	**PAD_GPIO_2** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
3:2		drv_cfg_gpio_1	**PAD_GPIO_1** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
1:0		drv_cfg_gpio_0	**PAD_GPIO_0** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]

A20C0004 DRV_CFG1 **GPIO TX driving strength control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			drv_cfg_resetb_out		drv_cfg_gpio_29		drv_cfg_gpio_28		drv_cfg_gpio_27		drv_cfg_gpio_26		drv_cfg_gpio_25		drv_cfg_gpio_24	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drv_cfg_gpio_23		drv_cfg_gpio_22		drv_cfg_gpio_21		drv_cfg_gpio_20		drv_cfg_gpio_19		drv_cfg_gpio_18		drv_cfg_gpio_17		drv_cfg_gpio_16	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
29:28		drv_cfg_resetb_out	**PAD_RESETB_OUT** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
27:26		drv_cfg_gpio_29	**PAD_GPIO_29** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
25:24		drv_cfg_gpio_28	**PAD_GPIO_28** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
23:22		drv_cfg_gpio_27	**PAD_GPIO_27** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
21:20		drv_cfg_gpio_26	**PAD_GPIO_26** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
19:18		drv_cfg_gpio_25	**PAD_GPIO_25** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
17:16		drv_cfg_gpio_24	**PAD_GPIO_24** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
15:14		drv_cfg_gpio_23	**PAD_GPIO_23** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
13:12		drv_cfg_gpio_22	**PAD_GPIO_22** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
11:10		drv_cfg_gpio_21	**PAD_GPIO_21** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
9:8		drv_cfg_gpio_20	**PAD_GPIO_20**

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Bit(s)	Mnemonic	Name	Description
			4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
7:6		drv_cfg_gpio_19	**PAD_GPIO_19** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
5:4		drv_cfg_gpio_18	**PAD_GPIO_18** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
3:2		drv_cfg_gpio_17	**PAD_GPIO_17** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
1:0		drv_cfg_gpio_16	**PAD_GPIO_16** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]

A20C0018 **IES_CFG0** **GPIO IES Control.** **7FFFFFFF**

RX input buffer enable. High asserted.
Datapath: from IO to O. IES =0, O=0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ies_cfg_resetb_out	ies_cfg_gpio_29	ies_cfg_gpio_28	ies_cfg_gpio_27	ies_cfg_gpio_26	ies_cfg_gpio_25	ies_cfg_gpio_24	ies_cfg_gpio_23	ies_cfg_gpio_22	ies_cfg_gpio_21	ies_cfg_gpio_20	ies_cfg_gpio_19	ies_cfg_gpio_18	ies_cfg_gpio_17	ies_cfg_gpio_16
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ies_cfg_gpio_15	ies_cfg_gpio_14	ies_cfg_gpio_13	ies_cfg_gpio_12	ies_cfg_gpio_11	ies_cfg_gpio_10	ies_cfg_gpio_9	ies_cfg_gpio_8	ies_cfg_gpio_7	ies_cfg_gpio_6	ies_cfg_gpio_5	ies_cfg_gpio_4	ies_cfg_gpio_3	ies_cfg_gpio_2	ies_cfg_gpio_1	ies_cfg_gpio_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
30		ies_cfg_resetb_out	**PAD_RESETB_OUT** 0: Disable; 1: Enable;
29		ies_cfg_gpio_29	**PAD_GPIO_29** 0: Disable; 1: Enable;
28		ies_cfg_gpio_28	**PAD_GPIO_28** 0: Disable; 1: Enable;
27		ies_cfg_gpio_27	**PAD_GPIO_27** 0: Disable; 1: Enable;
26		ies_cfg_gpio_26	**PAD_GPIO_26** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description
25		ies_cfg_gpio_25	**PAD_GPIO_25** 0: Disable; 1: Enable;
24		ies_cfg_gpio_24	**PAD_GPIO_24** 0: Disable; 1: Enable;
23		ies_cfg_gpio_23	**PAD_GPIO_23** 0: Disable; 1: Enable;
22		ies_cfg_gpio_22	**PAD_GPIO_22** 0: Disable; 1: Enable;
21		ies_cfg_gpio_21	**PAD_GPIO_21** 0: Disable; 1: Enable;
20		ies_cfg_gpio_20	**PAD_GPIO_20** 0: Disable; 1: Enable;
19		ies_cfg_gpio_19	**PAD_GPIO_19** 0: Disable; 1: Enable;
18		ies_cfg_gpio_18	**PAD_GPIO_18** 0: Disable; 1: Enable;
17		ies_cfg_gpio_17	**PAD_GPIO_17** 0: Disable; 1: Enable;
16		ies_cfg_gpio_16	**PAD_GPIO_16** 0: Disable; 1: Enable;
15		ies_cfg_gpio_15	**PAD_GPIO_15** 0: Disable; 1: Enable;
14		ies_cfg_gpio_14	**PAD_GPIO_14** 0: Disable; 1: Enable;
13		ies_cfg_gpio_13	**PAD_GPIO_13** 0: Disable; 1: Enable;
12		ies_cfg_gpio_12	**PAD_GPIO_12** 0: Disable; 1: Enable;
11		ies_cfg_gpio_11	**PAD_GPIO_11** 0: Disable; 1: Enable;
10		ies_cfg_gpio_10	**PAD_GPIO_10** 0: Disable; 1: Enable;
9		ies_cfg_gpio_9	**PAD_GPIO_9** 0: Disable; 1: Enable;
8		ies_cfg_gpio_8	**PAD_GPIO_8** 0: Disable; 1: Enable;
7		ies_cfg_gpio_7	**PAD_GPIO_7** 0: Disable; 1: Enable;
6		ies_cfg_gpio_6	**PAD_GPIO_6** 0: Disable; 1: Enable;
5		ies_cfg_gpio_5	**PAD_GPIO_5** 0: Disable; 1: Enable;
4		ies_cfg_gpio_4	**PAD_GPIO_4** 0: Disable; 1: Enable;
3		ies_cfg_gpio_3	**PAD_GPIO_3** 0: Disable; 1: Enable;
2		ies_cfg_gpio_2	**PAD_GPIO_2** 0: Disable; 1: Enable;
1		ies_cfg_gpio_1	**PAD_GPIO_1** 0: Disable; 1: Enable;
0		ies_cfg_gpio_0	**PAD_GPIO_0** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description

A20C001C **IES_CFG0_SET** **GPIO IES Control.** **00000000**

RX input buffer enable. High asserted.
Datapath: from IO to O. IES =0, O=0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ies_cfg_set_resetb_out	ies_cfg_set_gpio_29	ies_cfg_set_gpio_28	ies_cfg_set_gpio_27	ies_cfg_set_gpio_26	ies_cfg_set_gpio_25	ies_cfg_set_gpio_24	ies_cfg_set_gpio_23	ies_cfg_set_gpio_22	ies_cfg_set_gpio_21	ies_cfg_set_gpio_20	ies_cfg_set_gpio_19	ies_cfg_set_gpio_18	ies_cfg_set_gpio_17	ies_cfg_set_gpio_16
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ies_cfg_set_gpio_15	ies_cfg_set_gpio_14	ies_cfg_set_gpio_13	ies_cfg_set_gpio_12	ies_cfg_set_gpio_11	ies_cfg_set_gpio_10	ies_cfg_set_gpio_9	ies_cfg_set_gpio_8	ies_cfg_set_gpio_7	ies_cfg_set_gpio_6	ies_cfg_set_gpio_5	ies_cfg_set_gpio_4	ies_cfg_set_gpio_3	ies_cfg_set_gpio_2	ies_cfg_set_gpio_1	ies_cfg_set_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		ies_cfg_set_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: SET bit;
29		ies_cfg_set_gpio_29	**PAD_GPIO_29** 0: Keep; 1: SET bit;
28		ies_cfg_set_gpio_28	**PAD_GPIO_28** 0: Keep; 1: SET bit;
27		ies_cfg_set_gpio_27	**PAD_GPIO_27** 0: Keep; 1: SET bit;
26		ies_cfg_set_gpio_26	**PAD_GPIO_26** 0: Keep; 1: SET bit;
25		ies_cfg_set_gpio_25	**PAD_GPIO_25** 0: Keep; 1: SET bit;
24		ies_cfg_set_gpio_24	**PAD_GPIO_24** 0: Keep; 1: SET bit;
23		ies_cfg_set_gpio_23	**PAD_GPIO_23** 0: Keep; 1: SET bit;
22		ies_cfg_set_gpio_22	**PAD_GPIO_22** 0: Keep; 1: SET bit;
21		ies_cfg_set_gpio_21	**PAD_GPIO_21** 0: Keep; 1: SET bit;
20		ies_cfg_set_gpio_20	**PAD_GPIO_20** 0: Keep; 1: SET bit;
19		ies_cfg_set_gpio_19	**PAD_GPIO_19** 0: Keep; 1: SET bit;
18		ies_cfg_set_gpio_18	**PAD_GPIO_18** 0: Keep; 1: SET bit;
17		ies_cfg_set_gpio_17	**PAD_GPIO_17** 0: Keep; 1: SET bit;
16		ies_cfg_set_gpio_16	**PAD_GPIO_16** 0: Keep; 1: SET bit;
15		ies_cfg_set_gpio_15	**PAD_GPIO_15** 0: Keep; 1: SET bit;

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Bit(s)	Mnemonic	Name	Description
14		ies_cfg_set_gpio_14	**PAD_GPIO_14** 0: Keep; 1: SET bit;
13		ies_cfg_set_gpio_13	**PAD_GPIO_13** 0: Keep; 1: SET bit;
12		ies_cfg_set_gpio_12	**PAD_GPIO_12** 0: Keep; 1: SET bit;
11		ies_cfg_set_gpio_11	**PAD_GPIO_11** 0: Keep; 1: SET bit;
10		ies_cfg_set_gpio_10	**PAD_GPIO_10** 0: Keep; 1: SET bit;
9		ies_cfg_set_gpio_9	**PAD_GPIO_9** 0: Keep; 1: SET bit;
8		ies_cfg_set_gpio_8	**PAD_GPIO_8** 0: Keep; 1: SET bit;
7		ies_cfg_set_gpio_7	**PAD_GPIO_7** 0: Keep; 1: SET bit;
6		ies_cfg_set_gpio_6	**PAD_GPIO_6** 0: Keep; 1: SET bit;
5		ies_cfg_set_gpio_5	**PAD_GPIO_5** 0: Keep; 1: SET bit;
4		ies_cfg_set_gpio_4	**PAD_GPIO_4** 0: Keep; 1: SET bit;
3		ies_cfg_set_gpio_3	**PAD_GPIO_3** 0: Keep; 1: SET bit;
2		ies_cfg_set_gpio_2	**PAD_GPIO_2** 0: Keep; 1: SET bit;
1		ies_cfg_set_gpio_1	**PAD_GPIO_1** 0: Keep; 1: SET bit;
0		ies_cfg_set_gpio_0	**PAD_GPIO_0** 0: Keep; 1: SET bit;

A20C0020 IES_CFG0_CLR GPIO IES Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		ies_cfg_clr_resetb_out	ies_cfg_clr_gpio_29	ies_cfg_clr_gpio_28	ies_cfg_clr_gpio_27	ies_cfg_clr_gpio_26	ies_cfg_clr_gpio_25	ies_cfg_clr_gpio_24	ies_cfg_clr_gpio_23	ies_cfg_clr_gpio_22	ies_cfg_clr_gpio_21	ies_cfg_clr_gpio_20	ies_cfg_clr_gpio_19	ies_cfg_clr_gpio_18	ies_cfg_clr_gpio_17	ies_cfg_clr_gpio_16
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ies_cfg_clr_gpio_15	ies_cfg_clr_gpio_14	ies_cfg_clr_gpio_13	ies_cfg_clr_gpio_12	ies_cfg_clr_gpio_11	ies_cfg_clr_gpio_10	ies_cfg_clr_gpio_9	ies_cfg_clr_gpio_8	ies_cfg_clr_gpio_7	ies_cfg_clr_gpio_6	ies_cfg_clr_gpio_5	ies_cfg_clr_gpio_4	ies_cfg_clr_gpio_3	ies_cfg_clr_gpio_2	ies_cfg_clr_gpio_1	ies_cfg_clr_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		ies_cfg_clr_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: CLEAR bit
29		ies_cfg_clr_gpio_29	**PAD_GPIO_29** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
28		ies_cfg_clr_gpio_28	**PAD_GPIO_28** 0: Keep; 1: CLEAR bit
27		ies_cfg_clr_gpio_27	**PAD_GPIO_27** 0: Keep; 1: CLEAR bit
26		ies_cfg_clr_gpio_26	**PAD_GPIO_26** 0: Keep; 1: CLEAR bit
25		ies_cfg_clr_gpio_25	**PAD_GPIO_25** 0: Keep; 1: CLEAR bit
24		ies_cfg_clr_gpio_24	**PAD_GPIO_24** 0: Keep; 1: CLEAR bit
23		ies_cfg_clr_gpio_23	**PAD_GPIO_23** 0: Keep; 1: CLEAR bit
22		ies_cfg_clr_gpio_22	**PAD_GPIO_22** 0: Keep; 1: CLEAR bit
21		ies_cfg_clr_gpio_21	**PAD_GPIO_21** 0: Keep; 1: CLEAR bit
20		ies_cfg_clr_gpio_20	**PAD_GPIO_20** 0: Keep; 1: CLEAR bit
19		ies_cfg_clr_gpio_19	**PAD_GPIO_19** 0: Keep; 1: CLEAR bit
18		ies_cfg_clr_gpio_18	**PAD_GPIO_18** 0: Keep; 1: CLEAR bit
17		ies_cfg_clr_gpio_17	**PAD_GPIO_17** 0: Keep; 1: CLEAR bit
16		ies_cfg_clr_gpio_16	**PAD_GPIO_16** 0: Keep; 1: CLEAR bit
15		ies_cfg_clr_gpio_15	**PAD_GPIO_15** 0: Keep; 1: CLEAR bit
14		ies_cfg_clr_gpio_14	**PAD_GPIO_14** 0: Keep; 1: CLEAR bit
13		ies_cfg_clr_gpio_13	**PAD_GPIO_13** 0: Keep; 1: CLEAR bit
12		ies_cfg_clr_gpio_12	**PAD_GPIO_12** 0: Keep; 1: CLEAR bit
11		ies_cfg_clr_gpio_11	**PAD_GPIO_11** 0: Keep; 1: CLEAR bit
10		ies_cfg_clr_gpio_10	**PAD_GPIO_10** 0: Keep; 1: CLEAR bit
9		ies_cfg_clr_gpio_9	**PAD_GPIO_9** 0: Keep; 1: CLEAR bit
8		ies_cfg_clr_gpio_8	**PAD_GPIO_8** 0: Keep; 1: CLEAR bit
7		ies_cfg_clr_gpio_7	**PAD_GPIO_7** 0: Keep; 1: CLEAR bit
6		ies_cfg_clr_gpio_6	**PAD_GPIO_6** 0: Keep; 1: CLEAR bit
5		ies_cfg_clr_gpio_5	**PAD_GPIO_5** 0: Keep; 1: CLEAR bit
4		ies_cfg_clr_gpio_4	**PAD_GPIO_4** 0: Keep; 1: CLEAR bit
3		ies_cfg_clr_gpio_3	**PAD_GPIO_3** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
2		ies_cfg_clr_gpio_2	**PAD_GPIO_2** 0: Keep; 1: CLEAR bit
1		ies_cfg_clr_gpio_1	**PAD_GPIO_1** 0: Keep; 1: CLEAR bit
0		ies_cfg_clr_gpio_0	**PAD_GPIO_0** 0: Keep; 1: CLEAR bit

A20C0024 PD_CFG0 GPIO PD Control 000000FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								pd_cfg_resetb_out	pd_cfg_gpio_29	pd_cfg_gpio_28	pd_cfg_gpio_27	pd_cfg_gpio_26	pd_cfg_gpio_25	pd_cfg_gpio_24	pd_cfg_gpio_5	pd_cfg_gpio_2
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	1	1	1	1	1	1	1	0

Bit(s)	Mnemonic	Name	Description
8		pd_cfg_resetb_out	**PAD_RESETB_OUT** 0: Disable; 1: Enable;
7		pd_cfg_gpio_29	**PAD_GPIO_29** 0: Disable; 1: Enable;
6		pd_cfg_gpio_28	**PAD_GPIO_28** 0: Disable; 1: Enable;
5		pd_cfg_gpio_27	**PAD_GPIO_27** 0: Disable; 1: Enable;
4		pd_cfg_gpio_26	**PAD_GPIO_26** 0: Disable; 1: Enable;
3		pd_cfg_gpio_25	**PAD_GPIO_25** 0: Disable; 1: Enable;
2		pd_cfg_gpio_24	**PAD_GPIO_24** 0: Disable; 1: Enable;
1		pd_cfg_gpio_5	**PAD_GPIO_5** 0: Disable; 1: Enable;
0		pd_cfg_gpio_2	**PAD_GPIO_2** 0: Disable; 1: Enable;

A20C0028 PD_CFG0_SET GPIO PD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								pd_cfg_set_resetb_out	pd_cfg_set_gpio_29	pd_cfg_set_gpio_28	pd_cfg_set_gpio_27	pd_cfg_set_gpio_26	pd_cfg_set_gpio_25	pd_cfg_set_gpio_24	pd_cfg_set_gpio_5	pd_cfg_set_gpio_2

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Type								WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		pd_cfg_set_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: SET bit;
7		pd_cfg_set_gpio_29	**PAD_GPIO_29** 0: Keep; 1: SET bit;
6		pd_cfg_set_gpio_28	**PAD_GPIO_28** 0: Keep; 1: SET bit;
5		pd_cfg_set_gpio_27	**PAD_GPIO_27** 0: Keep; 1: SET bit;
4		pd_cfg_set_gpio_26	**PAD_GPIO_26** 0: Keep; 1: SET bit;
3		pd_cfg_set_gpio_25	**PAD_GPIO_25** 0: Keep; 1: SET bit;
2		pd_cfg_set_gpio_24	**PAD_GPIO_24** 0: Keep; 1: SET bit;
1		pd_cfg_set_gpio_5	**PAD_GPIO_5** 0: Keep; 1: SET bit;
0		pd_cfg_set_gpio_2	**PAD_GPIO_2** 0: Keep; 1: SET bit;

A20C002C PD_CFG0_CLR GPIO PD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**pd_cfg_clr_resetb_out**	**pd_cfg_clr_gpio_29**	**pd_cfg_clr_gpio_28**	**pd_cfg_clr_gpio_27**	**pd_cfg_clr_gpio_26**	**pd_cfg_clr_gpio_25**	**pd_cfg_clr_gpio_24**	**pd_cfg_clr_gpio_5**	**pd_cfg_clr_gpio_2**
Type								WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		pd_cfg_clr_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: CLEAR bit
7		pd_cfg_clr_gpio_29	**PAD_GPIO_29** 0: Keep; 1: CLEAR bit
6		pd_cfg_clr_gpio_28	**PAD_GPIO_28** 0: Keep; 1: CLEAR bit
5		pd_cfg_clr_gpio_27	**PAD_GPIO_27** 0: Keep; 1: CLEAR bit
4		pd_cfg_clr_gpio_26	**PAD_GPIO_26** 0: Keep; 1: CLEAR bit
3		pd_cfg_clr_gpio_25	**PAD_GPIO_25** 0: Keep; 1: CLEAR bit
2		pd_cfg_clr_gpio_24	**PAD_GPIO_24** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
1		pd_cfg_clr_gpio_5	**PAD_GPIO_5** 0: Keep; 1: CLEAR bit
0		pd_cfg_clr_gpio_2	**PAD_GPIO_2** 0: Keep; 1: CLEAR bit

A20C0030 PUPD_CFG0 GPIO PUPD Control 003FFFFC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											pupd_cfg_gpio_23	pupd_cfg_gpio_22	pupd_cfg_gpio_21	pupd_cfg_gpio_20	pupd_cfg_gpio_19	pupd_cfg_gpio_18
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pupd_cfg_gpio_17	pupd_cfg_gpio_16	pupd_cfg_gpio_15	pupd_cfg_gpio_14	pupd_cfg_gpio_13	pupd_cfg_gpio_12	pupd_cfg_gpio_11	pupd_cfg_gpio_10	pupd_cfg_gpio_9	pupd_cfg_gpio_8	pupd_cfg_gpio_7	pupd_cfg_gpio_6	pupd_cfg_gpio_4	pupd_cfg_gpio_3	pupd_cfg_gpio_1	pupd_cfg_gpio_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

Bit(s)	Mnemonic	Name	Description
21		pupd_cfg_gpio_23	**PAD_GPIO_23** 0: Disable; 1: Enable;
20		pupd_cfg_gpio_22	**PAD_GPIO_22** 0: Disable; 1: Enable;
19		pupd_cfg_gpio_21	**PAD_GPIO_21** 0: Disable; 1: Enable;
18		pupd_cfg_gpio_20	**PAD_GPIO_20** 0: Disable; 1: Enable;
17		pupd_cfg_gpio_19	**PAD_GPIO_19** 0: Disable; 1: Enable;
16		pupd_cfg_gpio_18	**PAD_GPIO_18** 0: Disable; 1: Enable;
15		pupd_cfg_gpio_17	**PAD_GPIO_17** 0: Disable; 1: Enable;
14		pupd_cfg_gpio_16	**PAD_GPIO_16** 0: Disable; 1: Enable;
13		pupd_cfg_gpio_15	**PAD_GPIO_15** 0: Disable; 1: Enable;
12		pupd_cfg_gpio_14	**PAD_GPIO_14** 0: Disable; 1: Enable;
11		pupd_cfg_gpio_13	**PAD_GPIO_13** 0: Disable; 1: Enable;
10		pupd_cfg_gpio_12	**PAD_GPIO_12** 0: Disable; 1: Enable;
9		pupd_cfg_gpio_11	**PAD_GPIO_11** 0: Disable; 1: Enable;
8		pupd_cfg_gpio_10	**PAD_GPIO_10** 0: Disable; 1: Enable;
7		pupd_cfg_gpio_9	**PAD_GPIO_9** 0: Disable; 1: Enable;
6		pupd_cfg_gpio_8	**PAD_GPIO_8**

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Bit(s)	Mnemonic	Name	Description
			0: Disable; 1: Enable;
5		pupd_cfg_gpio_7	**PAD_GPIO_7** 0: Disable; 1: Enable;
4		pupd_cfg_gpio_6	**PAD_GPIO_6** 0: Disable; 1: Enable;
3		pupd_cfg_gpio_4	**PAD_GPIO_4** 0: Disable; 1: Enable;
2		pupd_cfg_gpio_3	**PAD_GPIO_3** 0: Disable; 1: Enable;
1		pupd_cfg_gpio_1	**PAD_GPIO_1** 0: Disable; 1: Enable;
0		pupd_cfg_gpio_0	**PAD_GPIO_0** 0: Disable; 1: Enable;

A20C0034 PUPD_CFG0_SET GPIO PUPD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											pupd_cfg_set_gpio_23	pupd_cfg_set_gpio_22	pupd_cfg_set_gpio_21	pupd_cfg_set_gpio_20	pupd_cfg_set_gpio_19	pupd_cfg_set_gpio_18
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pupd_cfg_set_gpio_17	pupd_cfg_set_gpio_16	pupd_cfg_set_gpio_15	pupd_cfg_set_gpio_14	pupd_cfg_set_gpio_13	pupd_cfg_set_gpio_12	pupd_cfg_set_gpio_11	pupd_cfg_set_gpio_10	pupd_cfg_set_gpio_9	pupd_cfg_set_gpio_8	pupd_cfg_set_gpio_7	pupd_cfg_set_gpio_6	pupd_cfg_set_gpio_4	pupd_cfg_set_gpio_3	pupd_cfg_set_gpio_1	pupd_cfg_set_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		pupd_cfg_set_gpio_23	**PAD_GPIO_23** 0: Keep; 1: SET bit;
20		pupd_cfg_set_gpio_22	**PAD_GPIO_22** 0: Keep; 1: SET bit;
19		pupd_cfg_set_gpio_21	**PAD_GPIO_21** 0: Keep; 1: SET bit;
18		pupd_cfg_set_gpio_20	**PAD_GPIO_20** 0: Keep; 1: SET bit;
17		pupd_cfg_set_gpio_19	**PAD_GPIO_19** 0: Keep; 1: SET bit;
16		pupd_cfg_set_gpio_18	**PAD_GPIO_18** 0: Keep; 1: SET bit;
15		pupd_cfg_set_gpio_17	**PAD_GPIO_17** 0: Keep; 1: SET bit;
14		pupd_cfg_set_gpio_16	**PAD_GPIO_16** 0: Keep; 1: SET bit;
13		pupd_cfg_set_gpio_15	**PAD_GPIO_15** 0: Keep; 1: SET bit;
12		pupd_cfg_set_gpio_14	**PAD_GPIO_14** 0: Keep; 1: SET bit;

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Bit(s)	Mnemonic	Name	Description
11		pupd_cfg_set_gpio_13	**PAD_GPIO_13** 0: Keep; 1: SET bit;
10		pupd_cfg_set_gpio_12	**PAD_GPIO_12** 0: Keep; 1: SET bit;
9		pupd_cfg_set_gpio_11	**PAD_GPIO_11** 0: Keep; 1: SET bit;
8		pupd_cfg_set_gpio_10	**PAD_GPIO_10** 0: Keep; 1: SET bit;
7		pupd_cfg_set_gpio_9	**PAD_GPIO_9** 0: Keep; 1: SET bit;
6		pupd_cfg_set_gpio_8	**PAD_GPIO_8** 0: Keep; 1: SET bit;
5		pupd_cfg_set_gpio_7	**PAD_GPIO_7** 0: Keep; 1: SET bit;
4		pupd_cfg_set_gpio_6	**PAD_GPIO_6** 0: Keep; 1: SET bit;
3		pupd_cfg_set_gpio_4	**PAD_GPIO_4** 0: Keep; 1: SET bit;
2		pupd_cfg_set_gpio_3	**PAD_GPIO_3** 0: Keep; 1: SET bit;
1		pupd_cfg_set_gpio_1	**PAD_GPIO_1** 0: Keep; 1: SET bit;
0		pupd_cfg_set_gpio_0	**PAD_GPIO_0** 0: Keep; 1: SET bit;

A20C0038 PUPD_CFG0_CLR GPIO PUPD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											pupd_cfg_clr_gpio_23	pupd_cfg_clr_gpio_22	pupd_cfg_clr_gpio_21	pupd_cfg_clr_gpio_20	pupd_cfg_clr_gpio_19	pupd_cfg_clr_gpio_18
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pupd_cfg_clr_gpio_17	pupd_cfg_clr_gpio_16	pupd_cfg_clr_gpio_15	pupd_cfg_clr_gpio_14	pupd_cfg_clr_gpio_13	pupd_cfg_clr_gpio_12	pupd_cfg_clr_gpio_11	pupd_cfg_clr_gpio_10	pupd_cfg_clr_gpio_9	pupd_cfg_clr_gpio_8	pupd_cfg_clr_gpio_7	pupd_cfg_clr_gpio_6	pupd_cfg_clr_gpio_4	pupd_cfg_clr_gpio_3	pupd_cfg_clr_gpio_1	pupd_cfg_clr_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		pupd_cfg_clr_gpio_23	**PAD_GPIO_23** 0: Keep; 1: CLEAR bit
20		pupd_cfg_clr_gpio_22	**PAD_GPIO_22** 0: Keep; 1: CLEAR bit
19		pupd_cfg_clr_gpio_21	**PAD_GPIO_21** 0: Keep; 1: CLEAR bit
18		pupd_cfg_clr_gpio_20	**PAD_GPIO_20** 0: Keep; 1: CLEAR bit
17		pupd_cfg_clr_gpio_19	**PAD_GPIO_19**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: CLEAR bit
16		pupd_cfg_clr_gpio_18	**PAD_GPIO_18** 0: Keep; 1: CLEAR bit
15		pupd_cfg_clr_gpio_17	**PAD_GPIO_17** 0: Keep; 1: CLEAR bit
14		pupd_cfg_clr_gpio_16	**PAD_GPIO_16** 0: Keep; 1: CLEAR bit
13		pupd_cfg_clr_gpio_15	**PAD_GPIO_15** 0: Keep; 1: CLEAR bit
12		pupd_cfg_clr_gpio_14	**PAD_GPIO_14** 0: Keep; 1: CLEAR bit
11		pupd_cfg_clr_gpio_13	**PAD_GPIO_13** 0: Keep; 1: CLEAR bit
10		pupd_cfg_clr_gpio_12	**PAD_GPIO_12** 0: Keep; 1: CLEAR bit
9		pupd_cfg_clr_gpio_11	**PAD_GPIO_11** 0: Keep; 1: CLEAR bit
8		pupd_cfg_clr_gpio_10	**PAD_GPIO_10** 0: Keep; 1: CLEAR bit
7		pupd_cfg_clr_gpio_9	**PAD_GPIO_9** 0: Keep; 1: CLEAR bit
6		pupd_cfg_clr_gpio_8	**PAD_GPIO_8** 0: Keep; 1: CLEAR bit
5		pupd_cfg_clr_gpio_7	**PAD_GPIO_7** 0: Keep; 1: CLEAR bit
4		pupd_cfg_clr_gpio_6	**PAD_GPIO_6** 0: Keep; 1: CLEAR bit
3		pupd_cfg_clr_gpio_4	**PAD_GPIO_4** 0: Keep; 1: CLEAR bit
2		pupd_cfg_clr_gpio_3	**PAD_GPIO_3** 0: Keep; 1: CLEAR bit
1		pupd_cfg_clr_gpio_1	**PAD_GPIO_1** 0: Keep; 1: CLEAR bit
0		pupd_cfg_clr_gpio_0	**PAD_GPIO_0** 0: Keep; 1: CLEAR bit

A20C003C PU_CFG0 **GPIO PU Control** **00000101**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								pu_cfg_resetb_out	pu_cfg_gpio_29	pu_cfg_gpio_28	pu_cfg_gpio_27	pu_cfg_gpio_26	pu_cfg_gpio_25	pu_cfg_gpio_24	pu_cfg_gpio_5	pu_cfg_gpio_2
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
8		pu_cfg_resetb_out	**PAD_RESETB_OUT**

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Bit(s)	Mnemonic	Name	Description
			0: Disable; 1: Enable;
7		pu_cfg_gpio_29	**PAD_GPIO_29** 0: Disable; 1: Enable;
6		pu_cfg_gpio_28	**PAD_GPIO_28** 0: Disable; 1: Enable;
5		pu_cfg_gpio_27	**PAD_GPIO_27** 0: Disable; 1: Enable;
4		pu_cfg_gpio_26	**PAD_GPIO_26** 0: Disable; 1: Enable;
3		pu_cfg_gpio_25	**PAD_GPIO_25** 0: Disable; 1: Enable;
2		pu_cfg_gpio_24	**PAD_GPIO_24** 0: Disable; 1: Enable;
1		pu_cfg_gpio_5	**PAD_GPIO_5** 0: Disable; 1: Enable;
0		pu_cfg_gpio_2	**PAD_GPIO_2** 0: Disable; 1: Enable;

A20C0040 PU_CFG0_SET GPIO PU Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								pu_cfg_set_resetb_out	pu_cfg_set_gpio_29	pu_cfg_set_gpio_28	pu_cfg_set_gpio_27	pu_cfg_set_gpio_26	pu_cfg_set_gpio_25	pu_cfg_set_gpio_24	pu_cfg_set_gpio_5	pu_cfg_set_gpio_2
Type								WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		pu_cfg_set_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: SET bit;
7		pu_cfg_set_gpio_29	**PAD_GPIO_29** 0: Keep; 1: SET bit;
6		pu_cfg_set_gpio_28	**PAD_GPIO_28** 0: Keep; 1: SET bit;
5		pu_cfg_set_gpio_27	**PAD_GPIO_27** 0: Keep; 1: SET bit;
4		pu_cfg_set_gpio_26	**PAD_GPIO_26** 0: Keep; 1: SET bit;
3		pu_cfg_set_gpio_25	**PAD_GPIO_25** 0: Keep; 1: SET bit;
2		pu_cfg_set_gpio_24	**PAD_GPIO_24** 0: Keep; 1: SET bit;
1		pu_cfg_set_gpio_5	**PAD_GPIO_5** 0: Keep; 1: SET bit;
0		pu_cfg_set_gpio_2	**PAD_GPIO_2** 0: Keep; 1: SET bit;

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A20C0044 PU_CFG0_CLR GPIO PU Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								pu_cfg_clr_resetb_out	pu_cfg_clr_gpio_29	pu_cfg_clr_gpio_28	pu_cfg_clr_gpio_27	pu_cfg_clr_gpio_26	pu_cfg_clr_gpio_25	pu_cfg_clr_gpio_24	pu_cfg_clr_gpio_5	pu_cfg_clr_gpio_2
Type								WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
8		pu_cfg_clr_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: CLEAR bit
7		pu_cfg_clr_gpio_29	**PAD_GPIO_29** 0: Keep; 1: CLEAR bit
6		pu_cfg_clr_gpio_28	**PAD_GPIO_28** 0: Keep; 1: CLEAR bit
5		pu_cfg_clr_gpio_27	**PAD_GPIO_27** 0: Keep; 1: CLEAR bit
4		pu_cfg_clr_gpio_26	**PAD_GPIO_26** 0: Keep; 1: CLEAR bit
3		pu_cfg_clr_gpio_25	**PAD_GPIO_25** 0: Keep; 1: CLEAR bit
2		pu_cfg_clr_gpio_24	**PAD_GPIO_24** 0: Keep; 1: CLEAR bit
1		pu_cfg_clr_gpio_5	**PAD_GPIO_5** 0: Keep; 1: CLEAR bit
0		pu_cfg_clr_gpio_2	**PAD_GPIO_2** 0: Keep; 1: CLEAR bit

A20C0048 R0_CFG0 GPIO R0 Control 003FFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											r0_cfg_gpio_23	r0_cfg_gpio_22	r0_cfg_gpio_21	r0_cfg_gpio_20	r0_cfg_gpio_19	r0_cfg_gpio_18
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r0_cfg_gpio_17	r0_cfg_gpio_16	r0_cfg_gpio_15	r0_cfg_gpio_14	r0_cfg_gpio_13	r0_cfg_gpio_12	r0_cfg_gpio_11	r0_cfg_gpio_10	r0_cfg_gpio_9	r0_cfg_gpio_8	r0_cfg_gpio_7	r0_cfg_gpio_6	r0_cfg_gpio_4	r0_cfg_gpio_3	r0_cfg_gpio_1	r0_cfg_gpio_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
21		r0_cfg_gpio_23	**PAD_GPIO_23** 0: Disable; 1: Enable;
20		r0_cfg_gpio_22	**PAD_GPIO_22** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description
19		r0_cfg_gpio_21	**PAD_GPIO_21** 0: Disable; 1: Enable;
18		r0_cfg_gpio_20	**PAD_GPIO_20** 0: Disable; 1: Enable;
17		r0_cfg_gpio_19	**PAD_GPIO_19** 0: Disable; 1: Enable;
16		r0_cfg_gpio_18	**PAD_GPIO_18** 0: Disable; 1: Enable;
15		r0_cfg_gpio_17	**PAD_GPIO_17** 0: Disable; 1: Enable;
14		r0_cfg_gpio_16	**PAD_GPIO_16** 0: Disable; 1: Enable;
13		r0_cfg_gpio_15	**PAD_GPIO_15** 0: Disable; 1: Enable;
12		r0_cfg_gpio_14	**PAD_GPIO_14** 0: Disable; 1: Enable;
11		r0_cfg_gpio_13	**PAD_GPIO_13** 0: Disable; 1: Enable;
10		r0_cfg_gpio_12	**PAD_GPIO_12** 0: Disable; 1: Enable;
9		r0_cfg_gpio_11	**PAD_GPIO_11** 0: Disable; 1: Enable;
8		r0_cfg_gpio_10	**PAD_GPIO_10** 0: Disable; 1: Enable;
7		r0_cfg_gpio_9	**PAD_GPIO_9** 0: Disable; 1: Enable;
6		r0_cfg_gpio_8	**PAD_GPIO_8** 0: Disable; 1: Enable;
5		r0_cfg_gpio_7	**PAD_GPIO_7** 0: Disable; 1: Enable;
4		r0_cfg_gpio_6	**PAD_GPIO_6** 0: Disable; 1: Enable;
3		r0_cfg_gpio_4	**PAD_GPIO_4** 0: Disable; 1: Enable;
2		r0_cfg_gpio_3	**PAD_GPIO_3** 0: Disable; 1: Enable;
1		r0_cfg_gpio_1	**PAD_GPIO_1** 0: Disable; 1: Enable;
0		r0_cfg_gpio_0	**PAD_GPIO_0** 0: Disable; 1: Enable;

A20C004C R0_CFG0_SET GPIO R0 Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											r0_cfg_set_gpio_23	r0_cfg_set_gpio_22	r0_cfg_set_gpio_21	r0_cfg_set_gpio_20	r0_cfg_set_gpio_19	r0_cfg_set_gpio_18
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set	r0_cfg_set

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	_gpio_17	_gpio_16	_gpio_15	_gpio_14	_gpio_13	_gpio_12	_gpio_11	_gpio_10	_gpio_9	_gpio_8	_gpio_7	_gpio_6	_gpio_4	_gpio_3	_gpio_1	_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		r0_cfg_set_gpio_23	**PAD_GPIO_23** 0: Keep; 1: SET bit;
20		r0_cfg_set_gpio_22	**PAD_GPIO_22** 0: Keep; 1: SET bit;
19		r0_cfg_set_gpio_21	**PAD_GPIO_21** 0: Keep; 1: SET bit;
18		r0_cfg_set_gpio_20	**PAD_GPIO_20** 0: Keep; 1: SET bit;
17		r0_cfg_set_gpio_19	**PAD_GPIO_19** 0: Keep; 1: SET bit;
16		r0_cfg_set_gpio_18	**PAD_GPIO_18** 0: Keep; 1: SET bit;
15		r0_cfg_set_gpio_17	**PAD_GPIO_17** 0: Keep; 1: SET bit;
14		r0_cfg_set_gpio_16	**PAD_GPIO_16** 0: Keep; 1: SET bit;
13		r0_cfg_set_gpio_15	**PAD_GPIO_15** 0: Keep; 1: SET bit;
12		r0_cfg_set_gpio_14	**PAD_GPIO_14** 0: Keep; 1: SET bit;
11		r0_cfg_set_gpio_13	**PAD_GPIO_13** 0: Keep; 1: SET bit;
10		r0_cfg_set_gpio_12	**PAD_GPIO_12** 0: Keep; 1: SET bit;
9		r0_cfg_set_gpio_11	**PAD_GPIO_11** 0: Keep; 1: SET bit;
8		r0_cfg_set_gpio_10	**PAD_GPIO_10** 0: Keep; 1: SET bit;
7		r0_cfg_set_gpio_9	**PAD_GPIO_9** 0: Keep; 1: SET bit;
6		r0_cfg_set_gpio_8	**PAD_GPIO_8** 0: Keep; 1: SET bit;
5		r0_cfg_set_gpio_7	**PAD_GPIO_7** 0: Keep; 1: SET bit;
4		r0_cfg_set_gpio_6	**PAD_GPIO_6** 0: Keep; 1: SET bit;
3		r0_cfg_set_gpio_4	**PAD_GPIO_4** 0: Keep; 1: SET bit;
2		r0_cfg_set_gpio_3	**PAD_GPIO_3** 0: Keep; 1: SET bit;
1		r0_cfg_set_gpio_1	**PAD_GPIO_1** 0: Keep; 1: SET bit;
0		r0_cfg_set_gpio_0	**PAD_GPIO_0** 0: Keep; 1: SET bit;

A20C0050 R0_CFG0_CLR GPIO R0 Control for Bitwise Access 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											r0_cfg_clr_gpio_23	r0_cfg_clr_gpio_22	r0_cfg_clr_gpio_21	r0_cfg_clr_gpio_20	r0_cfg_clr_gpio_19	r0_cfg_clr_gpio_18
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r0_cfg_clr_gpio_17	r0_cfg_clr_gpio_16	r0_cfg_clr_gpio_15	r0_cfg_clr_gpio_14	r0_cfg_clr_gpio_13	r0_cfg_clr_gpio_12	r0_cfg_clr_gpio_11	r0_cfg_clr_gpio_10	r0_cfg_clr_gpio_9	r0_cfg_clr_gpio_8	r0_cfg_clr_gpio_7	r0_cfg_clr_gpio_6	r0_cfg_clr_gpio_4	r0_cfg_clr_gpio_3	r0_cfg_clr_gpio_1	r0_cfg_clr_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		r0_cfg_clr_gpio_23	**PAD_GPIO_23** 0: Keep; 1: CLEAR bit
20		r0_cfg_clr_gpio_22	**PAD_GPIO_22** 0: Keep; 1: CLEAR bit
19		r0_cfg_clr_gpio_21	**PAD_GPIO_21** 0: Keep; 1: CLEAR bit
18		r0_cfg_clr_gpio_20	**PAD_GPIO_20** 0: Keep; 1: CLEAR bit
17		r0_cfg_clr_gpio_19	**PAD_GPIO_19** 0: Keep; 1: CLEAR bit
16		r0_cfg_clr_gpio_18	**PAD_GPIO_18** 0: Keep; 1: CLEAR bit
15		r0_cfg_clr_gpio_17	**PAD_GPIO_17** 0: Keep; 1: CLEAR bit
14		r0_cfg_clr_gpio_16	**PAD_GPIO_16** 0: Keep; 1: CLEAR bit
13		r0_cfg_clr_gpio_15	**PAD_GPIO_15** 0: Keep; 1: CLEAR bit
12		r0_cfg_clr_gpio_14	**PAD_GPIO_14** 0: Keep; 1: CLEAR bit
11		r0_cfg_clr_gpio_13	**PAD_GPIO_13** 0: Keep; 1: CLEAR bit
10		r0_cfg_clr_gpio_12	**PAD_GPIO_12** 0: Keep; 1: CLEAR bit
9		r0_cfg_clr_gpio_11	**PAD_GPIO_11** 0: Keep; 1: CLEAR bit
8		r0_cfg_clr_gpio_10	**PAD_GPIO_10** 0: Keep; 1: CLEAR bit
7		r0_cfg_clr_gpio_9	**PAD_GPIO_9** 0: Keep; 1: CLEAR bit
6		r0_cfg_clr_gpio_8	**PAD_GPIO_8** 0: Keep; 1: CLEAR bit
5		r0_cfg_clr_gpio_7	**PAD_GPIO_7** 0: Keep; 1: CLEAR bit
4		r0_cfg_clr_gpio_6	**PAD_GPIO_6** 0: Keep; 1: CLEAR bit
3		r0_cfg_clr_gpio_4	**PAD_GPIO_4** 0: Keep; 1: CLEAR bit
2		r0_cfg_clr_gpio_3	**PAD_GPIO_3**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: CLEAR bit
1		r0_cfg_clr_gpio_1	**PAD_GPIO_1**
			0: Keep; 1: CLEAR bit
0		r0_cfg_clr_gpio_0	**PAD_GPIO_0**
			0: Keep; 1: CLEAR bit

A20C0054 R1_CFG0 GPIO R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											r1_cfg_gpio_23	r1_cfg_gpio_22	r1_cfg_gpio_21	r1_cfg_gpio_20	r1_cfg_gpio_19	r1_cfg_gpio_18
Type											RW	RW	RW	RW	RW	RW
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r1_cfg_gpio_17	r1_cfg_gpio_16	r1_cfg_gpio_15	r1_cfg_gpio_14	r1_cfg_gpio_13	r1_cfg_gpio_12	r1_cfg_gpio_11	r1_cfg_gpio_10	r1_cfg_gpio_9	r1_cfg_gpio_8	r1_cfg_gpio_7	r1_cfg_gpio_6	r1_cfg_gpio_4	r1_cfg_gpio_3	r1_cfg_gpio_1	r1_cfg_gpio_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		r1_cfg_gpio_23	**PAD_GPIO_23**
			0: Disable; 1: Enable;
20		r1_cfg_gpio_22	**PAD_GPIO_22**
			0: Disable; 1: Enable;
19		r1_cfg_gpio_21	**PAD_GPIO_21**
			0: Disable; 1: Enable;
18		r1_cfg_gpio_20	**PAD_GPIO_20**
			0: Disable; 1: Enable;
17		r1_cfg_gpio_19	**PAD_GPIO_19**
			0: Disable; 1: Enable;
16		r1_cfg_gpio_18	**PAD_GPIO_18**
			0: Disable; 1: Enable;
15		r1_cfg_gpio_17	**PAD_GPIO_17**
			0: Disable; 1: Enable;
14		r1_cfg_gpio_16	**PAD_GPIO_16**
			0: Disable; 1: Enable;
13		r1_cfg_gpio_15	**PAD_GPIO_15**
			0: Disable; 1: Enable;
12		r1_cfg_gpio_14	**PAD_GPIO_14**
			0: Disable; 1: Enable;
11		r1_cfg_gpio_13	**PAD_GPIO_13**
			0: Disable; 1: Enable;
10		r1_cfg_gpio_12	**PAD_GPIO_12**
			0: Disable; 1: Enable;
9		r1_cfg_gpio_11	**PAD_GPIO_11**
			0: Disable; 1: Enable;
8		r1_cfg_gpio_10	**PAD_GPIO_10**
			0: Disable; 1: Enable;
7		r1_cfg_gpio_9	**PAD_GPIO_9**
			0: Disable; 1: Enable;
6		r1_cfg_gpio_8	**PAD_GPIO_8**

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Bit(s)	Mnemonic	Name	Description
			0: Disable; 1: Enable;
5		r1_cfg_gpio_7	**PAD_GPIO_7** 0: Disable; 1: Enable;
4		r1_cfg_gpio_6	**PAD_GPIO_6** 0: Disable; 1: Enable;
3		r1_cfg_gpio_4	**PAD_GPIO_4** 0: Disable; 1: Enable;
2		r1_cfg_gpio_3	**PAD_GPIO_3** 0: Disable; 1: Enable;
1		r1_cfg_gpio_1	**PAD_GPIO_1** 0: Disable; 1: Enable;
0		r1_cfg_gpio_0	**PAD_GPIO_0** 0: Disable; 1: Enable;

A20C0058 R1_CFG0_SET GPIO R1 Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											r1_cfg_set_gpio_23	r1_cfg_set_gpio_22	r1_cfg_set_gpio_21	r1_cfg_set_gpio_20	r1_cfg_set_gpio_19	r1_cfg_set_gpio_18
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r1_cfg_set_gpio_17	r1_cfg_set_gpio_16	r1_cfg_set_gpio_15	r1_cfg_set_gpio_14	r1_cfg_set_gpio_13	r1_cfg_set_gpio_12	r1_cfg_set_gpio_11	r1_cfg_set_gpio_10	r1_cfg_set_gpio_9	r1_cfg_set_gpio_8	r1_cfg_set_gpio_7	r1_cfg_set_gpio_6	r1_cfg_set_gpio_4	r1_cfg_set_gpio_3	r1_cfg_set_gpio_1	r1_cfg_set_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		r1_cfg_set_gpio_23	**PAD_GPIO_23** 0: Keep; 1: SET bit;
20		r1_cfg_set_gpio_22	**PAD_GPIO_22** 0: Keep; 1: SET bit;
19		r1_cfg_set_gpio_21	**PAD_GPIO_21** 0: Keep; 1: SET bit;
18		r1_cfg_set_gpio_20	**PAD_GPIO_20** 0: Keep; 1: SET bit;
17		r1_cfg_set_gpio_19	**PAD_GPIO_19** 0: Keep; 1: SET bit;
16		r1_cfg_set_gpio_18	**PAD_GPIO_18** 0: Keep; 1: SET bit;
15		r1_cfg_set_gpio_17	**PAD_GPIO_17** 0: Keep; 1: SET bit;
14		r1_cfg_set_gpio_16	**PAD_GPIO_16** 0: Keep; 1: SET bit;
13		r1_cfg_set_gpio_15	**PAD_GPIO_15** 0: Keep; 1: SET bit;
12		r1_cfg_set_gpio_14	**PAD_GPIO_14** 0: Keep; 1: SET bit;
11		r1_cfg_set_gpio_13	**PAD_GPIO_13** 0: Keep; 1: SET bit;

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Bit(s)	Mnemonic	Name	Description
10		r1_cfg_set_gpio_12	**PAD_GPIO_12** 0: Keep; 1: SET bit;
9		r1_cfg_set_gpio_11	**PAD_GPIO_11** 0: Keep; 1: SET bit;
8		r1_cfg_set_gpio_10	**PAD_GPIO_10** 0: Keep; 1: SET bit;
7		r1_cfg_set_gpio_9	**PAD_GPIO_9** 0: Keep; 1: SET bit;
6		r1_cfg_set_gpio_8	**PAD_GPIO_8** 0: Keep; 1: SET bit;
5		r1_cfg_set_gpio_7	**PAD_GPIO_7** 0: Keep; 1: SET bit;
4		r1_cfg_set_gpio_6	**PAD_GPIO_6** 0: Keep; 1: SET bit;
3		r1_cfg_set_gpio_4	**PAD_GPIO_4** 0: Keep; 1: SET bit;
2		r1_cfg_set_gpio_3	**PAD_GPIO_3** 0: Keep; 1: SET bit;
1		r1_cfg_set_gpio_1	**PAD_GPIO_1** 0: Keep; 1: SET bit;
0		r1_cfg_set_gpio_0	**PAD_GPIO_0** 0: Keep; 1: SET bit;

A20C005C R1_CFG0_CLR GPIO R1 Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											r1_cfg_clr_gpio_23	r1_cfg_clr_gpio_22	r1_cfg_clr_gpio_21	r1_cfg_clr_gpio_20	r1_cfg_clr_gpio_19	r1_cfg_clr_gpio_18
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	r1_cfg_clr_gpio_17	r1_cfg_clr_gpio_16	r1_cfg_clr_gpio_15	r1_cfg_clr_gpio_14	r1_cfg_clr_gpio_13	r1_cfg_clr_gpio_12	r1_cfg_clr_gpio_11	r1_cfg_clr_gpio_10	r1_cfg_clr_gpio_9	r1_cfg_clr_gpio_8	r1_cfg_clr_gpio_7	r1_cfg_clr_gpio_6	r1_cfg_clr_gpio_4	r1_cfg_clr_gpio_3	r1_cfg_clr_gpio_1	r1_cfg_clr_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
21		r1_cfg_clr_gpio_23	**PAD_GPIO_23** 0: Keep; 1: CLEAR bit
20		r1_cfg_clr_gpio_22	**PAD_GPIO_22** 0: Keep; 1: CLEAR bit
19		r1_cfg_clr_gpio_21	**PAD_GPIO_21** 0: Keep; 1: CLEAR bit
18		r1_cfg_clr_gpio_20	**PAD_GPIO_20** 0: Keep; 1: CLEAR bit
17		r1_cfg_clr_gpio_19	**PAD_GPIO_19** 0: Keep; 1: CLEAR bit
16		r1_cfg_clr_gpio_18	**PAD_GPIO_18** 0: Keep; 1: CLEAR bit
15		r1_cfg_clr_gpio_17	**PAD_GPIO_17**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: CLEAR bit
14		r1_cfg_clr_gpio_16	**PAD_GPIO_16** 0: Keep; 1: CLEAR bit
13		r1_cfg_clr_gpio_15	**PAD_GPIO_15** 0: Keep; 1: CLEAR bit
12		r1_cfg_clr_gpio_14	**PAD_GPIO_14** 0: Keep; 1: CLEAR bit
11		r1_cfg_clr_gpio_13	**PAD_GPIO_13** 0: Keep; 1: CLEAR bit
10		r1_cfg_clr_gpio_12	**PAD_GPIO_12** 0: Keep; 1: CLEAR bit
9		r1_cfg_clr_gpio_11	**PAD_GPIO_11** 0: Keep; 1: CLEAR bit
8		r1_cfg_clr_gpio_10	**PAD_GPIO_10** 0: Keep; 1: CLEAR bit
7		r1_cfg_clr_gpio_9	**PAD_GPIO_9** 0: Keep; 1: CLEAR bit
6		r1_cfg_clr_gpio_8	**PAD_GPIO_8** 0: Keep; 1: CLEAR bit
5		r1_cfg_clr_gpio_7	**PAD_GPIO_7** 0: Keep; 1: CLEAR bit
4		r1_cfg_clr_gpio_6	**PAD_GPIO_6** 0: Keep; 1: CLEAR bit
3		r1_cfg_clr_gpio_4	**PAD_GPIO_4** 0: Keep; 1: CLEAR bit
2		r1_cfg_clr_gpio_3	**PAD_GPIO_3** 0: Keep; 1: CLEAR bit
1		r1_cfg_clr_gpio_1	**PAD_GPIO_1** 0: Keep; 1: CLEAR bit
0		r1_cfg_clr_gpio_0	**PAD_GPIO_0** 0: Keep; 1: CLEAR bit

A20C0060 RDSEL_CFG0 **GPIO RX Duty Select** **00000000**

RDSEL[0]: level shifter duty high when asserted
RDSEL[1]: level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdsel_cfg_gpio_15		rdsel_cfg_gpio_14		rdsel_cfg_gpio_13		rdsel_cfg_gpio_12		rdsel_cfg_gpio_11		rdsel_cfg_gpio_10		rdsel_cfg_gpio_9		rdsel_cfg_gpio_8	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdsel_cfg_gpio_7		rdsel_cfg_gpio_6		rdsel_cfg_gpio_5		rdsel_cfg_gpio_4		rdsel_cfg_gpio_3		rdsel_cfg_gpio_2		rdsel_cfg_gpio_1		rdsel_cfg_gpio_0	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		rdsel_cfg_gpio_15	**PAD_GPIO_15**
29:28		rdsel_cfg_gpio_14	**PAD_GPIO_14**
27:26		rdsel_cfg_gpio_13	**PAD_GPIO_13**

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Bit(s)	Mnemonic	Name	Description
25:24		rdsel_cfg_gpio_12	**PAD_GPIO_12**
23:22		rdsel_cfg_gpio_11	**PAD_GPIO_11**
21:20		rdsel_cfg_gpio_10	**PAD_GPIO_10**
19:18		rdsel_cfg_gpio_9	**PAD_GPIO_9**
17:16		rdsel_cfg_gpio_8	**PAD_GPIO_8**
15:14		rdsel_cfg_gpio_7	**PAD_GPIO_7**
13:12		rdsel_cfg_gpio_6	**PAD_GPIO_6**
11:10		rdsel_cfg_gpio_5	**PAD_GPIO_5**
9:8		rdsel_cfg_gpio_4	**PAD_GPIO_4**
7:6		rdsel_cfg_gpio_3	**PAD_GPIO_3**
5:4		rdsel_cfg_gpio_2	**PAD_GPIO_2**
3:2		rdsel_cfg_gpio_1	**PAD_GPIO_1**
1:0		rdsel_cfg_gpio_0	**PAD_GPIO_0**

A20C0064 **RDSEL_CFG1** **GPIO RX Duty Select** **00000000**

RDSEL[0]: level shifter duty high when asserted
RDSEL[1]: level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			rdsel_cfg_resetb_out		rdsel_cfg_gpio_29		rdsel_cfg_gpio_28		rdsel_cfg_gpio_27		rdsel_cfg_gpio_26		rdsel_cfg_gpio_25		rdsel_cfg_gpio_24	
Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdsel_cfg_gpio_23		rdsel_cfg_gpio_22		rdsel_cfg_gpio_21		rdsel_cfg_gpio_20		rdsel_cfg_gpio_19		rdsel_cfg_gpio_18		rdsel_cfg_gpio_17		rdsel_cfg_gpio_16	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:28		rdsel_cfg_resetb_out	**PAD_RESETB_OUT**
27:26		rdsel_cfg_gpio_29	**PAD_GPIO_29**
25:24		rdsel_cfg_gpio_28	**PAD_GPIO_28**
23:22		rdsel_cfg_gpio_27	**PAD_GPIO_27**
21:20		rdsel_cfg_gpio_26	**PAD_GPIO_26**
19:18		rdsel_cfg_gpio_25	**PAD_GPIO_25**
17:16		rdsel_cfg_gpio_24	**PAD_GPIO_24**
15:14		rdsel_cfg_gpio_23	**PAD_GPIO_23**
13:12		rdsel_cfg_gpio_22	**PAD_GPIO_22**
11:10		rdsel_cfg_gpio_21	**PAD_GPIO_21**
9:8		rdsel_cfg_gpio_20	**PAD_GPIO_20**
7:6		rdsel_cfg_gpio_19	**PAD_GPIO_19**
5:4		rdsel_cfg_gpio_18	**PAD_GPIO_18**
3:2		rdsel_cfg_gpio_17	**PAD_GPIO_17**
1:0		rdsel_cfg_gpio_16	**PAD_GPIO_16**

A20C0078 **SMT_CFG0** **GPIO SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		smt_cfg_re	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_gp	smt_cfg_g

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		setb_out	io_29	io_28	io_27	io_26	io_25	io_24	io_23	io_22	io_21	io_20	io_19	io_18	io_17	pio_16
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smt_cfg_gpio_15	smt_cfg_gpio_14	smt_cfg_gpio_13	smt_cfg_gpio_12	smt_cfg_gpio_11	smt_cfg_gpio_10	smt_cfg_gpio_9	smt_cfg_gpio_8	smt_cfg_gpio_7	smt_cfg_gpio_6	smt_cfg_gpio_5	smt_cfg_gpio_4	smt_cfg_gpio_3	smt_cfg_gpio_2	smt_cfg_gpio_1	smt_cfg_gpio_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		smt_cfg_resetb_out	**PAD_RESETB_OUT** 0: Disable; 1: Enable;
29		smt_cfg_gpio_29	**PAD_GPIO_29** 0: Disable; 1: Enable;
28		smt_cfg_gpio_28	**PAD_GPIO_28** 0: Disable; 1: Enable;
27		smt_cfg_gpio_27	**PAD_GPIO_27** 0: Disable; 1: Enable;
26		smt_cfg_gpio_26	**PAD_GPIO_26** 0: Disable; 1: Enable;
25		smt_cfg_gpio_25	**PAD_GPIO_25** 0: Disable; 1: Enable;
24		smt_cfg_gpio_24	**PAD_GPIO_24** 0: Disable; 1: Enable;
23		smt_cfg_gpio_23	**PAD_GPIO_23** 0: Disable; 1: Enable;
22		smt_cfg_gpio_22	**PAD_GPIO_22** 0: Disable; 1: Enable;
21		smt_cfg_gpio_21	**PAD_GPIO_21** 0: Disable; 1: Enable;
20		smt_cfg_gpio_20	**PAD_GPIO_20** 0: Disable; 1: Enable;
19		smt_cfg_gpio_19	**PAD_GPIO_19** 0: Disable; 1: Enable;
18		smt_cfg_gpio_18	**PAD_GPIO_18** 0: Disable; 1: Enable;
17		smt_cfg_gpio_17	**PAD_GPIO_17** 0: Disable; 1: Enable;
16		smt_cfg_gpio_16	**PAD_GPIO_16** 0: Disable; 1: Enable;
15		smt_cfg_gpio_15	**PAD_GPIO_15** 0: Disable; 1: Enable;
14		smt_cfg_gpio_14	**PAD_GPIO_14** 0: Disable; 1: Enable;
13		smt_cfg_gpio_13	**PAD_GPIO_13** 0: Disable; 1: Enable;
12		smt_cfg_gpio_12	**PAD_GPIO_12** 0: Disable; 1: Enable;
11		smt_cfg_gpio_11	**PAD_GPIO_11** 0: Disable; 1: Enable;
10		smt_cfg_gpio_10	**PAD_GPIO_10** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description
9		smt_cfg_gpio_9	**PAD_GPIO_9** 0: Disable; 1: Enable;
8		smt_cfg_gpio_8	**PAD_GPIO_8** 0: Disable; 1: Enable;
7		smt_cfg_gpio_7	**PAD_GPIO_7** 0: Disable; 1: Enable;
6		smt_cfg_gpio_6	**PAD_GPIO_6** 0: Disable; 1: Enable;
5		smt_cfg_gpio_5	**PAD_GPIO_5** 0: Disable; 1: Enable;
4		smt_cfg_gpio_4	**PAD_GPIO_4** 0: Disable; 1: Enable;
3		smt_cfg_gpio_3	**PAD_GPIO_3** 0: Disable; 1: Enable;
2		smt_cfg_gpio_2	**PAD_GPIO_2** 0: Disable; 1: Enable;
1		smt_cfg_gpio_1	**PAD_GPIO_1** 0: Disable; 1: Enable;
0		smt_cfg_gpio_0	**PAD_GPIO_0** 0: Disable; 1: Enable;

A20C007C SMT_CFG0_SET GPIO SMT Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		smt_cfg_set_resetb_out	smt_cfg_set_gpio_29	smt_cfg_set_gpio_28	smt_cfg_set_gpio_27	smt_cfg_set_gpio_26	smt_cfg_set_gpio_25	smt_cfg_set_gpio_24	smt_cfg_set_gpio_23	smt_cfg_set_gpio_22	smt_cfg_set_gpio_21	smt_cfg_set_gpio_20	smt_cfg_set_gpio_19	smt_cfg_set_gpio_18	smt_cfg_set_gpio_17	smt_cfg_set_gpio_16
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smt_cfg_set_gpio_15	smt_cfg_set_gpio_14	smt_cfg_set_gpio_13	smt_cfg_set_gpio_12	smt_cfg_set_gpio_11	smt_cfg_set_gpio_10	smt_cfg_set_gpio_9	smt_cfg_set_gpio_8	smt_cfg_set_gpio_7	smt_cfg_set_gpio_6	smt_cfg_set_gpio_5	smt_cfg_set_gpio_4	smt_cfg_set_gpio_3	smt_cfg_set_gpio_2	smt_cfg_set_gpio_1	smt_cfg_set_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		smt_cfg_set_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: SET bit;
29		smt_cfg_set_gpio_29	**PAD_GPIO_29** 0: Keep; 1: SET bit;
28		smt_cfg_set_gpio_28	**PAD_GPIO_28** 0: Keep; 1: SET bit;
27		smt_cfg_set_gpio_27	**PAD_GPIO_27** 0: Keep; 1: SET bit;
26		smt_cfg_set_gpio_26	**PAD_GPIO_26** 0: Keep; 1: SET bit;
25		smt_cfg_set_gpio_25	**PAD_GPIO_25** 0: Keep; 1: SET bit;
24		smt_cfg_set_gpio_24	**PAD_GPIO_24** 0: Keep; 1: SET bit;

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Bit(s)	Mnemonic	Name	Description
23		smt_cfg_set_gpio_23	**PAD_GPIO_23** 0: Keep; 1: SET bit;
22		smt_cfg_set_gpio_22	**PAD_GPIO_22** 0: Keep; 1: SET bit;
21		smt_cfg_set_gpio_21	**PAD_GPIO_21** 0: Keep; 1: SET bit;
20		smt_cfg_set_gpio_20	**PAD_GPIO_20** 0: Keep; 1: SET bit;
19		smt_cfg_set_gpio_19	**PAD_GPIO_19** 0: Keep; 1: SET bit;
18		smt_cfg_set_gpio_18	**PAD_GPIO_18** 0: Keep; 1: SET bit;
17		smt_cfg_set_gpio_17	**PAD_GPIO_17** 0: Keep; 1: SET bit;
16		smt_cfg_set_gpio_16	**PAD_GPIO_16** 0: Keep; 1: SET bit;
15		smt_cfg_set_gpio_15	**PAD_GPIO_15** 0: Keep; 1: SET bit;
14		smt_cfg_set_gpio_14	**PAD_GPIO_14** 0: Keep; 1: SET bit;
13		smt_cfg_set_gpio_13	**PAD_GPIO_13** 0: Keep; 1: SET bit;
12		smt_cfg_set_gpio_12	**PAD_GPIO_12** 0: Keep; 1: SET bit;
11		smt_cfg_set_gpio_11	**PAD_GPIO_11** 0: Keep; 1: SET bit;
10		smt_cfg_set_gpio_10	**PAD_GPIO_10** 0: Keep; 1: SET bit;
9		smt_cfg_set_gpio_9	**PAD_GPIO_9** 0: Keep; 1: SET bit;
8		smt_cfg_set_gpio_8	**PAD_GPIO_8** 0: Keep; 1: SET bit;
7		smt_cfg_set_gpio_7	**PAD_GPIO_7** 0: Keep; 1: SET bit;
6		smt_cfg_set_gpio_6	**PAD_GPIO_6** 0: Keep; 1: SET bit;
5		smt_cfg_set_gpio_5	**PAD_GPIO_5** 0: Keep; 1: SET bit;
4		smt_cfg_set_gpio_4	**PAD_GPIO_4** 0: Keep; 1: SET bit;
3		smt_cfg_set_gpio_3	**PAD_GPIO_3** 0: Keep; 1: SET bit;
2		smt_cfg_set_gpio_2	**PAD_GPIO_2** 0: Keep; 1: SET bit;
1		smt_cfg_set_gpio_1	**PAD_GPIO_1** 0: Keep; 1: SET bit;
0		smt_cfg_set_gpio_0	**PAD_GPIO_0** 0: Keep; 1: SET bit;

A20C0080 SMT_CFG0_CLR GPIO SMT Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name		smt_cfg_clr_resetb_out	smt_cfg_clr_gpio_29	smt_cfg_clr_gpio_28	smt_cfg_clr_gpio_27	smt_cfg_clr_gpio_26	smt_cfg_clr_gpio_25	smt_cfg_clr_gpio_24	smt_cfg_clr_gpio_23	smt_cfg_clr_gpio_22	smt_cfg_clr_gpio_21	smt_cfg_clr_gpio_20	smt_cfg_clr_gpio_19	smt_cfg_clr_gpio_18	smt_cfg_clr_gpio_17	smt_cfg_clr_gpio_16
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smt_cfg_clr_gpio_15	smt_cfg_clr_gpio_14	smt_cfg_clr_gpio_13	smt_cfg_clr_gpio_12	smt_cfg_clr_gpio_11	smt_cfg_clr_gpio_10	smt_cfg_clr_gpio_9	smt_cfg_clr_gpio_8	smt_cfg_clr_gpio_7	smt_cfg_clr_gpio_6	smt_cfg_clr_gpio_5	smt_cfg_clr_gpio_4	smt_cfg_clr_gpio_3	smt_cfg_clr_gpio_2	smt_cfg_clr_gpio_1	smt_cfg_clr_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		smt_cfg_clr_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: CLEAR bit
29		smt_cfg_clr_gpio_29	**PAD_GPIO_29** 0: Keep; 1: CLEAR bit
28		smt_cfg_clr_gpio_28	**PAD_GPIO_28** 0: Keep; 1: CLEAR bit
27		smt_cfg_clr_gpio_27	**PAD_GPIO_27** 0: Keep; 1: CLEAR bit
26		smt_cfg_clr_gpio_26	**PAD_GPIO_26** 0: Keep; 1: CLEAR bit
25		smt_cfg_clr_gpio_25	**PAD_GPIO_25** 0: Keep; 1: CLEAR bit
24		smt_cfg_clr_gpio_24	**PAD_GPIO_24** 0: Keep; 1: CLEAR bit
23		smt_cfg_clr_gpio_23	**PAD_GPIO_23** 0: Keep; 1: CLEAR bit
22		smt_cfg_clr_gpio_22	**PAD_GPIO_22** 0: Keep; 1: CLEAR bit
21		smt_cfg_clr_gpio_21	**PAD_GPIO_21** 0: Keep; 1: CLEAR bit
20		smt_cfg_clr_gpio_20	**PAD_GPIO_20** 0: Keep; 1: CLEAR bit
19		smt_cfg_clr_gpio_19	**PAD_GPIO_19** 0: Keep; 1: CLEAR bit
18		smt_cfg_clr_gpio_18	**PAD_GPIO_18** 0: Keep; 1: CLEAR bit
17		smt_cfg_clr_gpio_17	**PAD_GPIO_17** 0: Keep; 1: CLEAR bit
16		smt_cfg_clr_gpio_16	**PAD_GPIO_16** 0: Keep; 1: CLEAR bit
15		smt_cfg_clr_gpio_15	**PAD_GPIO_15** 0: Keep; 1: CLEAR bit
14		smt_cfg_clr_gpio_14	**PAD_GPIO_14** 0: Keep; 1: CLEAR bit
13		smt_cfg_clr_gpio_13	**PAD_GPIO_13** 0: Keep; 1: CLEAR bit
12		smt_cfg_clr_gpio_12	**PAD_GPIO_12** 0: Keep; 1: CLEAR bit
11		smt_cfg_clr_gpio_11	**PAD_GPIO_11**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: CLEAR bit
10		smt_cfg_clr_gpio_10	**PAD_GPIO_10** 0: Keep; 1: CLEAR bit
9		smt_cfg_clr_gpio_9	**PAD_GPIO_9** 0: Keep; 1: CLEAR bit
8		smt_cfg_clr_gpio_8	**PAD_GPIO_8** 0: Keep; 1: CLEAR bit
7		smt_cfg_clr_gpio_7	**PAD_GPIO_7** 0: Keep; 1: CLEAR bit
6		smt_cfg_clr_gpio_6	**PAD_GPIO_6** 0: Keep; 1: CLEAR bit
5		smt_cfg_clr_gpio_5	**PAD_GPIO_5** 0: Keep; 1: CLEAR bit
4		smt_cfg_clr_gpio_4	**PAD_GPIO_4** 0: Keep; 1: CLEAR bit
3		smt_cfg_clr_gpio_3	**PAD_GPIO_3** 0: Keep; 1: CLEAR bit
2		smt_cfg_clr_gpio_2	**PAD_GPIO_2** 0: Keep; 1: CLEAR bit
1		smt_cfg_clr_gpio_1	**PAD_GPIO_1** 0: Keep; 1: CLEAR bit
0		smt_cfg_clr_gpio_0	**PAD_GPIO_0** 0: Keep; 1: CLEAR bit

A20C0084 SR_CFG0 **GPIO Output Slew Rate Control.** **00000000**

High asserted. SR=1, slower slew. SR=0, no slew rate controlled.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		sr_cfg_resetb_out	sr_cfg_gpio_29	sr_cfg_gpio_28	sr_cfg_gpio_27	sr_cfg_gpio_26	sr_cfg_gpio_25	sr_cfg_gpio_24	sr_cfg_gpio_23	sr_cfg_gpio_22	sr_cfg_gpio_21	sr_cfg_gpio_20	sr_cfg_gpio_19	sr_cfg_gpio_18	sr_cfg_gpio_17	sr_cfg_gpio_16
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sr_cfg_gpio_15	sr_cfg_gpio_14	sr_cfg_gpio_13	sr_cfg_gpio_12	sr_cfg_gpio_11	sr_cfg_gpio_10	sr_cfg_gpio_9	sr_cfg_gpio_8	sr_cfg_gpio_7	sr_cfg_gpio_6	sr_cfg_gpio_5	sr_cfg_gpio_4	sr_cfg_gpio_3	sr_cfg_gpio_2	sr_cfg_gpio_1	sr_cfg_gpio_0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		sr_cfg_resetb_out	**PAD_RESETB_OUT** 0: Disable; 1: Enable;
29		sr_cfg_gpio_29	**PAD_GPIO_29** 0: Disable; 1: Enable;
28		sr_cfg_gpio_28	**PAD_GPIO_28** 0: Disable; 1: Enable;
27		sr_cfg_gpio_27	**PAD_GPIO_27** 0: Disable; 1: Enable;
26		sr_cfg_gpio_26	**PAD_GPIO_26** 0: Disable; 1: Enable;
25		sr_cfg_gpio_25	**PAD_GPIO_25**

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Bit(s)	Mnemonic	Name	Description
			0: Disable; 1: Enable;
24		sr_cfg_gpio_24	**PAD_GPIO_24** 0: Disable; 1: Enable;
23		sr_cfg_gpio_23	**PAD_GPIO_23** 0: Disable; 1: Enable;
22		sr_cfg_gpio_22	**PAD_GPIO_22** 0: Disable; 1: Enable;
21		sr_cfg_gpio_21	**PAD_GPIO_21** 0: Disable; 1: Enable;
20		sr_cfg_gpio_20	**PAD_GPIO_20** 0: Disable; 1: Enable;
19		sr_cfg_gpio_19	**PAD_GPIO_19** 0: Disable; 1: Enable;
18		sr_cfg_gpio_18	**PAD_GPIO_18** 0: Disable; 1: Enable;
17		sr_cfg_gpio_17	**PAD_GPIO_17** 0: Disable; 1: Enable;
16		sr_cfg_gpio_16	**PAD_GPIO_16** 0: Disable; 1: Enable;
15		sr_cfg_gpio_15	**PAD_GPIO_15** 0: Disable; 1: Enable;
14		sr_cfg_gpio_14	**PAD_GPIO_14** 0: Disable; 1: Enable;
13		sr_cfg_gpio_13	**PAD_GPIO_13** 0: Disable; 1: Enable;
12		sr_cfg_gpio_12	**PAD_GPIO_12** 0: Disable; 1: Enable;
11		sr_cfg_gpio_11	**PAD_GPIO_11** 0: Disable; 1: Enable;
10		sr_cfg_gpio_10	**PAD_GPIO_10** 0: Disable; 1: Enable;
9		sr_cfg_gpio_9	**PAD_GPIO_9** 0: Disable; 1: Enable;
8		sr_cfg_gpio_8	**PAD_GPIO_8** 0: Disable; 1: Enable;
7		sr_cfg_gpio_7	**PAD_GPIO_7** 0: Disable; 1: Enable;
6		sr_cfg_gpio_6	**PAD_GPIO_6** 0: Disable; 1: Enable;
5		sr_cfg_gpio_5	**PAD_GPIO_5** 0: Disable; 1: Enable;
4		sr_cfg_gpio_4	**PAD_GPIO_4** 0: Disable; 1: Enable;
3		sr_cfg_gpio_3	**PAD_GPIO_3** 0: Disable; 1: Enable;
2		sr_cfg_gpio_2	**PAD_GPIO_2** 0: Disable; 1: Enable;
1		sr_cfg_gpio_1	**PAD_GPIO_1** 0: Disable; 1: Enable;
0		sr_cfg_gpio_0	**PAD_GPIO_0** 0: Disable; 1: Enable;

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A20C0088 SR_CFG0_SET **GPIO Slew Rate Control for Bitwise Access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		sr_cfg_set_resetb_out	sr_cfg_set_gpio_29	sr_cfg_set_gpio_28	sr_cfg_set_gpio_27	sr_cfg_set_gpio_26	sr_cfg_set_gpio_25	sr_cfg_set_gpio_24	sr_cfg_set_gpio_23	sr_cfg_set_gpio_22	sr_cfg_set_gpio_21	sr_cfg_set_gpio_20	sr_cfg_set_gpio_19	sr_cfg_set_gpio_18	sr_cfg_set_gpio_17	sr_cfg_set_gpio_16
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sr_cfg_set_gpio_15	sr_cfg_set_gpio_14	sr_cfg_set_gpio_13	sr_cfg_set_gpio_12	sr_cfg_set_gpio_11	sr_cfg_set_gpio_10	sr_cfg_set_gpio_9	sr_cfg_set_gpio_8	sr_cfg_set_gpio_7	sr_cfg_set_gpio_6	sr_cfg_set_gpio_5	sr_cfg_set_gpio_4	sr_cfg_set_gpio_3	sr_cfg_set_gpio_2	sr_cfg_set_gpio_1	sr_cfg_set_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		sr_cfg_set_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: SET bit;
29		sr_cfg_set_gpio_29	**PAD_GPIO_29** 0: Keep; 1: SET bit;
28		sr_cfg_set_gpio_28	**PAD_GPIO_28** 0: Keep; 1: SET bit;
27		sr_cfg_set_gpio_27	**PAD_GPIO_27** 0: Keep; 1: SET bit;
26		sr_cfg_set_gpio_26	**PAD_GPIO_26** 0: Keep; 1: SET bit;
25		sr_cfg_set_gpio_25	**PAD_GPIO_25** 0: Keep; 1: SET bit;
24		sr_cfg_set_gpio_24	**PAD_GPIO_24** 0: Keep; 1: SET bit;
23		sr_cfg_set_gpio_23	**PAD_GPIO_23** 0: Keep; 1: SET bit;
22		sr_cfg_set_gpio_22	**PAD_GPIO_22** 0: Keep; 1: SET bit;
21		sr_cfg_set_gpio_21	**PAD_GPIO_21** 0: Keep; 1: SET bit;
20		sr_cfg_set_gpio_20	**PAD_GPIO_20** 0: Keep; 1: SET bit;
19		sr_cfg_set_gpio_19	**PAD_GPIO_19** 0: Keep; 1: SET bit;
18		sr_cfg_set_gpio_18	**PAD_GPIO_18** 0: Keep; 1: SET bit;
17		sr_cfg_set_gpio_17	**PAD_GPIO_17** 0: Keep; 1: SET bit;
16		sr_cfg_set_gpio_16	**PAD_GPIO_16** 0: Keep; 1: SET bit;
15		sr_cfg_set_gpio_15	**PAD_GPIO_15** 0: Keep; 1: SET bit;
14		sr_cfg_set_gpio_14	**PAD_GPIO_14** 0: Keep; 1: SET bit;
13		sr_cfg_set_gpio_13	**PAD_GPIO_13**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: SET bit;
12		sr_cfg_set_gpio_12	**PAD_GPIO_12** 0: Keep; 1: SET bit;
11		sr_cfg_set_gpio_11	**PAD_GPIO_11** 0: Keep; 1: SET bit;
10		sr_cfg_set_gpio_10	**PAD_GPIO_10** 0: Keep; 1: SET bit;
9		sr_cfg_set_gpio_9	**PAD_GPIO_9** 0: Keep; 1: SET bit;
8		sr_cfg_set_gpio_8	**PAD_GPIO_8** 0: Keep; 1: SET bit;
7		sr_cfg_set_gpio_7	**PAD_GPIO_7** 0: Keep; 1: SET bit;
6		sr_cfg_set_gpio_6	**PAD_GPIO_6** 0: Keep; 1: SET bit;
5		sr_cfg_set_gpio_5	**PAD_GPIO_5** 0: Keep; 1: SET bit;
4		sr_cfg_set_gpio_4	**PAD_GPIO_4** 0: Keep; 1: SET bit;
3		sr_cfg_set_gpio_3	**PAD_GPIO_3** 0: Keep; 1: SET bit;
2		sr_cfg_set_gpio_2	**PAD_GPIO_2** 0: Keep; 1: SET bit;
1		sr_cfg_set_gpio_1	**PAD_GPIO_1** 0: Keep; 1: SET bit;
0		sr_cfg_set_gpio_0	**PAD_GPIO_0** 0: Keep; 1: SET bit;

A20C008C **SR_CFG0_CLR** **GPIO Slew Rate Control for Bitwise Access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		sr_cfg_clr_resetb_out	sr_cfg_clr_gpio_29	sr_cfg_clr_gpio_28	sr_cfg_clr_gpio_27	sr_cfg_clr_gpio_26	sr_cfg_clr_gpio_25	sr_cfg_clr_gpio_24	sr_cfg_clr_gpio_23	sr_cfg_clr_gpio_22	sr_cfg_clr_gpio_21	sr_cfg_clr_gpio_20	sr_cfg_clr_gpio_19	sr_cfg_clr_gpio_18	sr_cfg_clr_gpio_17	sr_cfg_clr_gpio_16
Type		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sr_cfg_clr_gpio_15	sr_cfg_clr_gpio_14	sr_cfg_clr_gpio_13	sr_cfg_clr_gpio_12	sr_cfg_clr_gpio_11	sr_cfg_clr_gpio_10	sr_cfg_clr_gpio_9	sr_cfg_clr_gpio_8	sr_cfg_clr_gpio_7	sr_cfg_clr_gpio_6	sr_cfg_clr_gpio_5	sr_cfg_clr_gpio_4	sr_cfg_clr_gpio_3	sr_cfg_clr_gpio_2	sr_cfg_clr_gpio_1	sr_cfg_clr_gpio_0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30		sr_cfg_clr_resetb_out	**PAD_RESETB_OUT** 0: Keep; 1: CLEAR bit
29		sr_cfg_clr_gpio_29	**PAD_GPIO_29** 0: Keep; 1: CLEAR bit
28		sr_cfg_clr_gpio_28	**PAD_GPIO_28** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
27		sr_cfg_clr_gpio_27	**PAD_GPIO_27** 0: Keep; 1: CLEAR bit
26		sr_cfg_clr_gpio_26	**PAD_GPIO_26** 0: Keep; 1: CLEAR bit
25		sr_cfg_clr_gpio_25	**PAD_GPIO_25** 0: Keep; 1: CLEAR bit
24		sr_cfg_clr_gpio_24	**PAD_GPIO_24** 0: Keep; 1: CLEAR bit
23		sr_cfg_clr_gpio_23	**PAD_GPIO_23** 0: Keep; 1: CLEAR bit
22		sr_cfg_clr_gpio_22	**PAD_GPIO_22** 0: Keep; 1: CLEAR bit
21		sr_cfg_clr_gpio_21	**PAD_GPIO_21** 0: Keep; 1: CLEAR bit
20		sr_cfg_clr_gpio_20	**PAD_GPIO_20** 0: Keep; 1: CLEAR bit
19		sr_cfg_clr_gpio_19	**PAD_GPIO_19** 0: Keep; 1: CLEAR bit
18		sr_cfg_clr_gpio_18	**PAD_GPIO_18** 0: Keep; 1: CLEAR bit
17		sr_cfg_clr_gpio_17	**PAD_GPIO_17** 0: Keep; 1: CLEAR bit
16		sr_cfg_clr_gpio_16	**PAD_GPIO_16** 0: Keep; 1: CLEAR bit
15		sr_cfg_clr_gpio_15	**PAD_GPIO_15** 0: Keep; 1: CLEAR bit
14		sr_cfg_clr_gpio_14	**PAD_GPIO_14** 0: Keep; 1: CLEAR bit
13		sr_cfg_clr_gpio_13	**PAD_GPIO_13** 0: Keep; 1: CLEAR bit
12		sr_cfg_clr_gpio_12	**PAD_GPIO_12** 0: Keep; 1: CLEAR bit
11		sr_cfg_clr_gpio_11	**PAD_GPIO_11** 0: Keep; 1: CLEAR bit
10		sr_cfg_clr_gpio_10	**PAD_GPIO_10** 0: Keep; 1: CLEAR bit
9		sr_cfg_clr_gpio_9	**PAD_GPIO_9** 0: Keep; 1: CLEAR bit
8		sr_cfg_clr_gpio_8	**PAD_GPIO_8** 0: Keep; 1: CLEAR bit
7		sr_cfg_clr_gpio_7	**PAD_GPIO_7** 0: Keep; 1: CLEAR bit
6		sr_cfg_clr_gpio_6	**PAD_GPIO_6** 0: Keep; 1: CLEAR bit
5		sr_cfg_clr_gpio_5	**PAD_GPIO_5** 0: Keep; 1: CLEAR bit
4		sr_cfg_clr_gpio_4	**PAD_GPIO_4** 0: Keep; 1: CLEAR bit
3		sr_cfg_clr_gpio_3	**PAD_GPIO_3** 0: Keep; 1: CLEAR bit
2		sr_cfg_clr_gpio_2	**PAD_GPIO_2** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
1		sr_cfg_clr_gpio_1	**PAD_GPIO_1** 0: Keep; 1: CLEAR bit
0		sr_cfg_clr_gpio_0	**PAD_GPIO_0** 0: Keep; 1: CLEAR bit

A20C0090 TDSEL_CFG0 **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			tdsel_cfg_gpio_7				tdsel_cfg_gpio_6				tdsel_cfg_gpio_5				tdsel_cfg_gpio_4	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_gpio_3				tdsel_cfg_gpio_2				tdsel_cfg_gpio_1				tdsel_cfg_gpio_0	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
29:28		tdsel_cfg_gpio_7	**PAD_GPIO_7**
25:24		tdsel_cfg_gpio_6	**PAD_GPIO_6**
21:20		tdsel_cfg_gpio_5	**PAD_GPIO_5**
17:16		tdsel_cfg_gpio_4	**PAD_GPIO_4**
13:12		tdsel_cfg_gpio_3	**PAD_GPIO_3**
9:8		tdsel_cfg_gpio_2	**PAD_GPIO_2**
5:4		tdsel_cfg_gpio_1	**PAD_GPIO_1**
1:0		tdsel_cfg_gpio_0	**PAD_GPIO_0**

A20C0094 TDSEL_CFG1 **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			tdsel_cfg_gpio_15				tdsel_cfg_gpio_14				tdsel_cfg_gpio_13				tdsel_cfg_gpio_12	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_gpio_11				tdsel_cfg_gpio_10				tdsel_cfg_gpio_9				tdsel_cfg_gpio_8	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
29:28		tdsel_cfg_gpio_15	**PAD_GPIO_15**
25:24		tdsel_cfg_gpio_14	**PAD_GPIO_14**
21:20		tdsel_cfg_gpio_13	**PAD_GPIO_13**

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Bit(s)	Mnemonic	Name	Description
17:16		tdsel_cfg_gpio_12	**PAD_GPIO_12**
13:12		tdsel_cfg_gpio_11	**PAD_GPIO_11**
9:8		tdsel_cfg_gpio_10	**PAD_GPIO_10**
5:4		tdsel_cfg_gpio_9	**PAD_GPIO_9**
1:0		tdsel_cfg_gpio_8	**PAD_GPIO_8**

A20C0098 TDSEL_CFG2 **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			tdsel_cfg_gpio_23				tdsel_cfg_gpio_22				tdsel_cfg_gpio_21				tdsel_cfg_gpio_20	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_gpio_19				tdsel_cfg_gpio_18				tdsel_cfg_gpio_17				tdsel_cfg_gpio_16	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
29:28		tdsel_cfg_gpio_23	**PAD_GPIO_23**
25:24		tdsel_cfg_gpio_22	**PAD_GPIO_22**
21:20		tdsel_cfg_gpio_21	**PAD_GPIO_21**
17:16		tdsel_cfg_gpio_20	**PAD_GPIO_20**
13:12		tdsel_cfg_gpio_19	**PAD_GPIO_19**
9:8		tdsel_cfg_gpio_18	**PAD_GPIO_18**
5:4		tdsel_cfg_gpio_17	**PAD_GPIO_17**
1:0		tdsel_cfg_gpio_16	**PAD_GPIO_16**

A20C009C TDSEL_CFG3 **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							tdsel_cfg_resetb_out				tdsel_cfg_gpio_29				tdsel_cfg_gpio_28	
Type							RW				RW				RW	
Reset							0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_gpio_27				tdsel_cfg_gpio_26				tdsel_cfg_gpio_25				tdsel_cfg_gpio_24	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
25:24		tdsel_cfg_resetb_out	**PAD_RESETB_OUT**
21:20		tdsel_cfg_gpio_29	**PAD_GPIO_29**

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Bit(s)	Mnemonic	Name	Description
17:16		tdsel_cfg_gpio_28	**PAD_GPIO_28**
13:12		tdsel_cfg_gpio_27	**PAD_GPIO_27**
9:8		tdsel_cfg_gpio_26	**PAD_GPIO_26**
5:4		tdsel_cfg_gpio_25	**PAD_GPIO_25**
1:0		tdsel_cfg_gpio_24	**PAD_GPIO_24**

A20D0000 DRV_CFG0 GPIO TX driving strength control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	drv_cfg_sim0_srst		drv_cfg_sim0_sio		drv_cfg_mipi_sdata		drv_cfg_mipi_sclk		drv_cfg_bpi4		drv_cfg_bpi3		drv_cfg_bpi2		drv_cfg_bpi1	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	drv_cfg_bpi0		drv_cfg_gpio_36		drv_cfg_gpio_35		drv_cfg_gpio_34		drv_cfg_gpio_33		drv_cfg_gpio_32		drv_cfg_gpio_31		drv_cfg_gpio_30	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		drv_cfg_sim0_srst	**PAD_SIM0_SRST** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
29:28		drv_cfg_sim0_sio	**PAD_SIM0_SIO** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
27:26		drv_cfg_mipi_sdata	**PAD_MIPI_SDATA** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
25:24		drv_cfg_mipi_sclk	**PAD_MIPI_SCLK** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
23:22		drv_cfg_bpi4	**PAD_BPI4** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
21:20		drv_cfg_bpi3	**PAD_BPI3** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
19:18		drv_cfg_bpi2	**PAD_BPI2** 4mA:[00] 8mA:[10]

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Bit(s)	Mnemonic	Name	Description
			12mA:[01] 16mA:[11]
17:16		drv_cfg_bpi1	**PAD_BPI1** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
15:14		drv_cfg_bpi0	**PAD_BPI0** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
13:12		drv_cfg_gpio_36	**PAD_GPIO_36** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
11:10		drv_cfg_gpio_35	**PAD_GPIO_35** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
9:8		drv_cfg_gpio_34	**PAD_GPIO_34** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
7:6		drv_cfg_gpio_33	**PAD_GPIO_33** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
5:4		drv_cfg_gpio_32	**PAD_GPIO_32** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
3:2		drv_cfg_gpio_31	**PAD_GPIO_31** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
1:0		drv_cfg_gpio_30	**PAD_GPIO_30** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]

A20D0004 DRV_CFG1 GPIO TX driving strength control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**drv_cfg_bond_rsv**		**drv_cfg_bond_sf_sip**		**drv_cfg_bond_psram_sip**		**drv_cfg_srclkenai**		**drv_cfg_sim0_sclk**	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:8		drv_cfg_bond_rsv	**PAD_BOND_RSV** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
7:6		drv_cfg_bond_sf_sip	**PAD_BOND_SF_SIP** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
5:4		drv_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
3:2		drv_cfg_srclkenai	**PAD_SRCLKENAI** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]
1:0		drv_cfg_sim0_sclk	**PAD_SIM0_SCLK** 4mA:[00] 8mA:[10] 12mA:[01] 16mA:[11]

A20D0018 G_CFG0 **GPIO analog input control** **0000001F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**g_cfg_gpio_34**	**g_cfg_gpio_33**	**g_cfg_gpio_32**	**g_cfg_gpio_31**	**g_cfg_gpio_30**
Type												RW	RW	RW	RW	RW
Reset												1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
4		g_cfg_gpio_34	**PAD_GPIO_34** 0: Disable; 1: Enable;
3		g_cfg_gpio_33	**PAD_GPIO_33**

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Bit(s)	Mnemonic	Name	Description
			0: Disable; 1: Enable;
2		g_cfg_gpio_32	**PAD_GPIO_32** 0: Disable; 1: Enable;
1		g_cfg_gpio_31	**PAD_GPIO_31** 0: Disable; 1: Enable;
0		g_cfg_gpio_30	**PAD_GPIO_30** 0: Disable; 1: Enable;

A20D001C G_CFG0_SET **GPIO analog input control for bitwise access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												g_cfg_set_gpio_34	g_cfg_set_gpio_33	g_cfg_set_gpio_32	g_cfg_set_gpio_31	g_cfg_set_gpio_30
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		g_cfg_set_gpio_34	**PAD_GPIO_34** 0: Keep; 1: SET bit;
3		g_cfg_set_gpio_33	**PAD_GPIO_33** 0: Keep; 1: SET bit;
2		g_cfg_set_gpio_32	**PAD_GPIO_32** 0: Keep; 1: SET bit;
1		g_cfg_set_gpio_31	**PAD_GPIO_31** 0: Keep; 1: SET bit;
0		g_cfg_set_gpio_30	**PAD_GPIO_30** 0: Keep; 1: SET bit;

A20D0020 G_CFG0_CLR **GPIO analog input control for bitwise access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												g_cfg_clr_gpio_34	g_cfg_clr_gpio_33	g_cfg_clr_gpio_32	g_cfg_clr_gpio_31	g_cfg_clr_gpio_30
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		g_cfg_clr_gpio_34	**PAD_GPIO_34** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
3		g_cfg_clr_gpio_33	**PAD_GPIO_33** 0: Keep; 1: CLEAR bit
2		g_cfg_clr_gpio_32	**PAD_GPIO_32** 0: Keep; 1: CLEAR bit
1		g_cfg_clr_gpio_31	**PAD_GPIO_31** 0: Keep; 1: CLEAR bit
0		g_cfg_clr_gpio_30	**PAD_GPIO_30** 0: Keep; 1: CLEAR bit

A20D0024 IES_CFG0 **GPIO IES Control.** **001FFFFF**

RX input buffer enable. High asserted.
Datapath: from IO to O. IES =0, O=0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												ies_cfg_bond_rsv	ies_cfg_bond_sf_sip	ies_cfg_bond_psram_sip	ies_cfg_srclkenai	ies_cfg_sim0_sclk
Type												RW	RW	RW	RW	RW
Reset												1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ies_cfg_sim0_srst	ies_cfg_sim0_sio	ies_cfg_mipi_sdata	ies_cfg_mipi_sclk	ies_cfg_bpi4	ies_cfg_bpi3	ies_cfg_bpi2	ies_cfg_bpi1	ies_cfg_bpi0	ies_cfg_gpio_36	ies_cfg_gpio_35	ies_cfg_gpio_34	ies_cfg_gpio_33	ies_cfg_gpio_32	ies_cfg_gpio_31	ies_cfg_gpio_30
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
20		ies_cfg_bond_rsv	**PAD_BOND_RSV** 0: Disable; 1: Enable;
19		ies_cfg_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Disable; 1: Enable;
18		ies_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Disable; 1: Enable;
17		ies_cfg_srclkenai	**PAD_SRCLKENAI** 0: Disable; 1: Enable;
16		ies_cfg_sim0_sclk	**PAD_SIM0_SCLK** 0: Disable; 1: Enable;
15		ies_cfg_sim0_srst	**PAD_SIM0_SRST** 0: Disable; 1: Enable;
14		ies_cfg_sim0_sio	**PAD_SIM0_SIO** 0: Disable; 1: Enable;
13		ies_cfg_mipi_sdata	**PAD_MIPI_SDATA** 0: Disable; 1: Enable;
12		ies_cfg_mipi_sclk	**PAD_MIPI_SCLK** 0: Disable; 1: Enable;
11		ies_cfg_bpi4	**PAD_BPI4** 0: Disable; 1: Enable;
10		ies_cfg_bpi3	**PAD_BPI3** 0: Disable; 1: Enable;
9		ies_cfg_bpi2	**PAD_BPI2** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description
8		ies_cfg_bpi1	**PAD_BPI1** 0: Disable; 1: Enable;
7		ies_cfg_bpi0	**PAD_BPI0** 0: Disable; 1: Enable;
6		ies_cfg_gpio_36	**PAD_GPIO_36** 0: Disable; 1: Enable;
5		ies_cfg_gpio_35	**PAD_GPIO_35** 0: Disable; 1: Enable;
4		ies_cfg_gpio_34	**PAD_GPIO_34** 0: Disable; 1: Enable;
3		ies_cfg_gpio_33	**PAD_GPIO_33** 0: Disable; 1: Enable;
2		ies_cfg_gpio_32	**PAD_GPIO_32** 0: Disable; 1: Enable;
1		ies_cfg_gpio_31	**PAD_GPIO_31** 0: Disable; 1: Enable;
0		ies_cfg_gpio_30	**PAD_GPIO_30** 0: Disable; 1: Enable;

A20D0028 IES_CFG0_SET GPIO IES Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												ies_cfg_set_bond_rsv	ies_cfg_set_bond_sf_sip	ies_cfg_set_bond_psram_sip	ies_cfg_set_srclkenai	ies_cfg_set_sim0_sclk
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ies_cfg_set_sim0_srst	ies_cfg_set_sim0_sio	ies_cfg_set_mipi_sdata	ies_cfg_set_mipi_sclk	ies_cfg_set_bpi4	ies_cfg_set_bpi3	ies_cfg_set_bpi2	ies_cfg_set_bpi1	ies_cfg_set_bpi0	ies_cfg_set_gpio_36	ies_cfg_set_gpio_35	ies_cfg_set_gpio_34	ies_cfg_set_gpio_33	ies_cfg_set_gpio_32	ies_cfg_set_gpio_31	ies_cfg_set_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		ies_cfg_set_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: SET bit;
19		ies_cfg_set_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: SET bit;
18		ies_cfg_set_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: SET bit;
17		ies_cfg_set_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: SET bit;
16		ies_cfg_set_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: SET bit;
15		ies_cfg_set_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: SET bit;
14		ies_cfg_set_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: SET bit;
13		ies_cfg_set_mipi_sdata	**PAD_MIPI_SDATA**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: SET bit;
12		ies_cfg_set_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: SET bit;
11		ies_cfg_set_bpi4	**PAD_BPI4** 0: Keep; 1: SET bit;
10		ies_cfg_set_bpi3	**PAD_BPI3** 0: Keep; 1: SET bit;
9		ies_cfg_set_bpi2	**PAD_BPI2** 0: Keep; 1: SET bit;
8		ies_cfg_set_bpi1	**PAD_BPI1** 0: Keep; 1: SET bit;
7		ies_cfg_set_bpi0	**PAD_BPI0** 0: Keep; 1: SET bit;
6		ies_cfg_set_gpio_36	**PAD_GPIO_36** 0: Keep; 1: SET bit;
5		ies_cfg_set_gpio_35	**PAD_GPIO_35** 0: Keep; 1: SET bit;
4		ies_cfg_set_gpio_34	**PAD_GPIO_34** 0: Keep; 1: SET bit;
3		ies_cfg_set_gpio_33	**PAD_GPIO_33** 0: Keep; 1: SET bit;
2		ies_cfg_set_gpio_32	**PAD_GPIO_32** 0: Keep; 1: SET bit;
1		ies_cfg_set_gpio_31	**PAD_GPIO_31** 0: Keep; 1: SET bit;
0		ies_cfg_set_gpio_30	**PAD_GPIO_30** 0: Keep; 1: SET bit;

A20D002C IES_CFG0_CLR GPIO IES Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												ies_cfg_clr_bond_rsv	ies_cfg_clr_bond_sf_sip	ies_cfg_clr_bond_psram_sip	ies_cfg_clr_srclkenai	ies_cfg_clr_sim0_sclk
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ies_cfg_clr_sim0_srst	ies_cfg_clr_sim0_sio	ies_cfg_clr_mipi_sdata	ies_cfg_clr_mipi_sclk	ies_cfg_clr_bpi4	ies_cfg_clr_bpi3	ies_cfg_clr_bpi2	ies_cfg_clr_bpi1	ies_cfg_clr_bpi0	ies_cfg_clr_gpio_36	ies_cfg_clr_gpio_35	ies_cfg_clr_gpio_34	ies_cfg_clr_gpio_33	ies_cfg_clr_gpio_32	ies_cfg_clr_gpio_31	ies_cfg_clr_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		ies_cfg_clr_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: CLEAR bit
19		ies_cfg_clr_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: CLEAR bit
18		ies_cfg_clr_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
17		ies_cfg_clr_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: CLEAR bit
16		ies_cfg_clr_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: CLEAR bit
15		ies_cfg_clr_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: CLEAR bit
14		ies_cfg_clr_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: CLEAR bit
13		ies_cfg_clr_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: CLEAR bit
12		ies_cfg_clr_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: CLEAR bit
11		ies_cfg_clr_bpi4	**PAD_BPI4** 0: Keep; 1: CLEAR bit
10		ies_cfg_clr_bpi3	**PAD_BPI3** 0: Keep; 1: CLEAR bit
9		ies_cfg_clr_bpi2	**PAD_BPI2** 0: Keep; 1: CLEAR bit
8		ies_cfg_clr_bpi1	**PAD_BPI1** 0: Keep; 1: CLEAR bit
7		ies_cfg_clr_bpi0	**PAD_BPI0** 0: Keep; 1: CLEAR bit
6		ies_cfg_clr_gpio_36	**PAD_GPIO_36** 0: Keep; 1: CLEAR bit
5		ies_cfg_clr_gpio_35	**PAD_GPIO_35** 0: Keep; 1: CLEAR bit
4		ies_cfg_clr_gpio_34	**PAD_GPIO_34** 0: Keep; 1: CLEAR bit
3		ies_cfg_clr_gpio_33	**PAD_GPIO_33** 0: Keep; 1: CLEAR bit
2		ies_cfg_clr_gpio_32	**PAD_GPIO_32** 0: Keep; 1: CLEAR bit
1		ies_cfg_clr_gpio_31	**PAD_GPIO_31** 0: Keep; 1: CLEAR bit
0		ies_cfg_clr_gpio_30	**PAD_GPIO_30** 0: Keep; 1: CLEAR bit

A20D0030 PD_CFG0 **GPIO PD Control** **00001FE4**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd_cfg_bond_rsv	pd_cfg_bond_sf_sip	pd_cfg_bond_psram_sip	pd_cfg_srclkenai	pd_cfg_mipi_sdata	pd_cfg_mipi_sclk	pd_cfg_bpi4	pd_cfg_bpi3	pd_cfg_bpi2	pd_cfg_bpi1	pd_cfg_bpi0	pd_cfg_gpio_34	pd_cfg_gpio_33	pd_cfg_gpio_32	pd_cfg_gpio_31	pd_cfg_gpio_30
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	1	1	1	1	1	1	0	0	1	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
15		pd_cfg_bond_rsv	**PAD_BOND_RSV** 0: Disable; 1: Enable;
14		pd_cfg_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Disable; 1: Enable;
13		pd_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Disable; 1: Enable;
12		pd_cfg_srclkenai	**PAD_SRCLKENAI** 0: Disable; 1: Enable;
11		pd_cfg_mipi_sdata	**PAD_MIPI_SDATA** 0: Disable; 1: Enable;
10		pd_cfg_mipi_sclk	**PAD_MIPI_SCLK** 0: Disable; 1: Enable;
9		pd_cfg_bpi4	**PAD_BPI4** 0: Disable; 1: Enable;
8		pd_cfg_bpi3	**PAD_BPI3** 0: Disable; 1: Enable;
7		pd_cfg_bpi2	**PAD_BPI2** 0: Disable; 1: Enable;
6		pd_cfg_bpi1	**PAD_BPI1** 0: Disable; 1: Enable;
5		pd_cfg_bpi0	**PAD_BPI0** 0: Disable; 1: Enable;
4		pd_cfg_gpio_34	**PAD_GPIO_34** 0: Disable; 1: Enable;
3		pd_cfg_gpio_33	**PAD_GPIO_33** 0: Disable; 1: Enable;
2		pd_cfg_gpio_32	**PAD_GPIO_32** 0: Disable; 1: Enable;
1		pd_cfg_gpio_31	**PAD_GPIO_31** 0: Disable; 1: Enable;
0		pd_cfg_gpio_30	**PAD_GPIO_30** 0: Disable; 1: Enable;

A20D0034 PD_CFG0_SET GPIO PD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd_cfg_set_bond_rsv	pd_cfg_set_bond_sf_sip	pd_cfg_set_bond_psram_sip	pd_cfg_set_srclkenai	pd_cfg_set_mipi_sdata	pd_cfg_set_mipi_sclk	pd_cfg_set_bpi4	pd_cfg_set_bpi3	pd_cfg_set_bpi2	pd_cfg_set_bpi1	pd_cfg_set_bpi0	pd_cfg_set_gpio_34	pd_cfg_set_gpio_33	pd_cfg_set_gpio_32	pd_cfg_set_gpio_31	pd_cfg_set_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		pd_cfg_set_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: SET bit;
14		pd_cfg_set_bond_sf_sip	**PAD_BOND_SF_SIP**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: SET bit;
13		pd_cfg_set_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: SET bit;
12		pd_cfg_set_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: SET bit;
11		pd_cfg_set_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: SET bit;
10		pd_cfg_set_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: SET bit;
9		pd_cfg_set_bpi4	**PAD_BPI4** 0: Keep; 1: SET bit;
8		pd_cfg_set_bpi3	**PAD_BPI3** 0: Keep; 1: SET bit;
7		pd_cfg_set_bpi2	**PAD_BPI2** 0: Keep; 1: SET bit;
6		pd_cfg_set_bpi1	**PAD_BPI1** 0: Keep; 1: SET bit;
5		pd_cfg_set_bpi0	**PAD_BPI0** 0: Keep; 1: SET bit;
4		pd_cfg_set_gpio_34	**PAD_GPIO_34** 0: Keep; 1: SET bit;
3		pd_cfg_set_gpio_33	**PAD_GPIO_33** 0: Keep; 1: SET bit;
2		pd_cfg_set_gpio_32	**PAD_GPIO_32** 0: Keep; 1: SET bit;
1		pd_cfg_set_gpio_31	**PAD_GPIO_31** 0: Keep; 1: SET bit;
0		pd_cfg_set_gpio_30	**PAD_GPIO_30** 0: Keep; 1: SET bit;

A20D0038 PD_CFG0_CLR GPIO PD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pd_cfg_clr_bond_rsv	pd_cfg_clr_bond_sf_sip	pd_cfg_clr_bond_psram_sip	pd_cfg_clr_srclkenai	pd_cfg_clr_mipi_sdata	pd_cfg_clr_mipi_sclk	pd_cfg_clr_bpi4	pd_cfg_clr_bpi3	pd_cfg_clr_bpi2	pd_cfg_clr_bpi1	pd_cfg_clr_bpi0	pd_cfg_clr_gpio_34	pd_cfg_clr_gpio_33	pd_cfg_clr_gpio_32	pd_cfg_clr_gpio_31	pd_cfg_clr_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		pd_cfg_clr_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: CLEAR bit
14		pd_cfg_clr_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: CLEAR bit
13		pd_cfg_clr_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
12		pd_cfg_clr_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: CLEAR bit
11		pd_cfg_clr_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: CLEAR bit
10		pd_cfg_clr_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: CLEAR bit
9		pd_cfg_clr_bpi4	**PAD_BPI4** 0: Keep; 1: CLEAR bit
8		pd_cfg_clr_bpi3	**PAD_BPI3** 0: Keep; 1: CLEAR bit
7		pd_cfg_clr_bpi2	**PAD_BPI2** 0: Keep; 1: CLEAR bit
6		pd_cfg_clr_bpi1	**PAD_BPI1** 0: Keep; 1: CLEAR bit
5		pd_cfg_clr_bpi0	**PAD_BPI0** 0: Keep; 1: CLEAR bit
4		pd_cfg_clr_gpio_34	**PAD_GPIO_34** 0: Keep; 1: CLEAR bit
3		pd_cfg_clr_gpio_33	**PAD_GPIO_33** 0: Keep; 1: CLEAR bit
2		pd_cfg_clr_gpio_32	**PAD_GPIO_32** 0: Keep; 1: CLEAR bit
1		pd_cfg_clr_gpio_31	**PAD_GPIO_31** 0: Keep; 1: CLEAR bit
0		pd_cfg_clr_gpio_30	**PAD_GPIO_30** 0: Keep; 1: CLEAR bit

A20D003C PUPD_CFG0 **GPIO PUPD Control** **0000001A**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												pupd_cfg_sim0_sclk	pupd_cfg_sim0_srst	pupd_cfg_sim0_sio	pupd_cfg_gpio_36	pupd_cfg_gpio_35
Type												RW	RW	RW	RW	RW
Reset												1	1	0	1	0

Bit(s)	Mnemonic	Name	Description
4		pupd_cfg_sim0_sclk	**PAD_SIM0_SCLK** 0: Disable; 1: Enable;
3		pupd_cfg_sim0_srst	**PAD_SIM0_SRST** 0: Disable; 1: Enable;
2		pupd_cfg_sim0_sio	**PAD_SIM0_SIO** 0: Disable; 1: Enable;
1		pupd_cfg_gpio_36	**PAD_GPIO_36** 0: Disable; 1: Enable;
0		pupd_cfg_gpio_35	**PAD_GPIO_35** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description

A20D0040 PUPD_CFG0_SET GPIO PUPD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												pupd_cfg_set_sim0_sclk	pupd_cfg_set_sim0_srst	pupd_cfg_set_sim0_sio	pupd_cfg_set_gpio_36	pupd_cfg_set_gpio_35
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		pupd_cfg_set_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: SET bit;
3		pupd_cfg_set_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: SET bit;
2		pupd_cfg_set_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: SET bit;
1		pupd_cfg_set_gpio_36	**PAD_GPIO_36** 0: Keep; 1: SET bit;
0		pupd_cfg_set_gpio_35	**PAD_GPIO_35** 0: Keep; 1: SET bit;

A20D0044 PUPD_CFG0_CLR GPIO PUPD Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												pupd_cfg_clr_sim0_sclk	pupd_cfg_clr_sim0_srst	pupd_cfg_clr_sim0_sio	pupd_cfg_clr_gpio_36	pupd_cfg_clr_gpio_35
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		pupd_cfg_clr_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: CLEAR bit
3		pupd_cfg_clr_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: CLEAR bit
2		pupd_cfg_clr_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: CLEAR bit
1		pupd_cfg_clr_gpio_36	**PAD_GPIO_36** 0: Keep; 1: CLEAR bit
0		pupd_cfg_clr_gpio_35	**PAD_GPIO_35**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: CLEAR bit

A20D0048 PU_CFG0 GPIO PU Control 0000E01B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pu_cfg_bond_rsv	pu_cfg_bond_sf_sip	pu_cfg_bond_psram_sip	pu_cfg_srclkenai	pu_cfg_mipi_sdata	pu_cfg_mipi_sclk	pu_cfg_bpi4	pu_cfg_bpi3	pu_cfg_bpi2	pu_cfg_bpi1	pu_cfg_bpi0	pu_cfg_gpio_34	pu_cfg_gpio_33	pu_cfg_gpio_32	pu_cfg_gpio_31	pu_cfg_gpio_30
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	0	0	0	0	0	0	0	0	1	1	0	1	1

Bit(s)	Mnemonic	Name	Description
15		pu_cfg_bond_rsv	**PAD_BOND_RSV** 0: Disable; 1: Enable;
14		pu_cfg_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Disable; 1: Enable;
13		pu_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Disable; 1: Enable;
12		pu_cfg_srclkenai	**PAD_SRCLKENAI** 0: Disable; 1: Enable;
11		pu_cfg_mipi_sdata	**PAD_MIPI_SDATA** 0: Disable; 1: Enable;
10		pu_cfg_mipi_sclk	**PAD_MIPI_SCLK** 0: Disable; 1: Enable;
9		pu_cfg_bpi4	**PAD_BPI4** 0: Disable; 1: Enable;
8		pu_cfg_bpi3	**PAD_BPI3** 0: Disable; 1: Enable;
7		pu_cfg_bpi2	**PAD_BPI2** 0: Disable; 1: Enable;
6		pu_cfg_bpi1	**PAD_BPI1** 0: Disable; 1: Enable;
5		pu_cfg_bpi0	**PAD_BPI0** 0: Disable; 1: Enable;
4		pu_cfg_gpio_34	**PAD_GPIO_34** 0: Disable; 1: Enable;
3		pu_cfg_gpio_33	**PAD_GPIO_33** 0: Disable; 1: Enable;
2		pu_cfg_gpio_32	**PAD_GPIO_32** 0: Disable; 1: Enable;
1		pu_cfg_gpio_31	**PAD_GPIO_31** 0: Disable; 1: Enable;
0		pu_cfg_gpio_30	**PAD_GPIO_30** 0: Disable; 1: Enable;

A20D004C PU_CFG0_SET GPIO PU Control for Bitwise Access 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pu_cfg_set_bond_rsv	pu_cfg_set_bond_sf_sip	pu_cfg_set_bond_psram_sip	pu_cfg_set_srclkenai	pu_cfg_set_mipi_sdata	pu_cfg_set_mipi_sclk	pu_cfg_set_bpi4	pu_cfg_set_bpi3	pu_cfg_set_bpi2	pu_cfg_set_bpi1	pu_cfg_set_bpi0	pu_cfg_set_gpio_34	pu_cfg_set_gpio_33	pu_cfg_set_gpio_32	pu_cfg_set_gpio_31	pu_cfg_set_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		pu_cfg_set_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: SET bit;
14		pu_cfg_set_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: SET bit;
13		pu_cfg_set_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: SET bit;
12		pu_cfg_set_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: SET bit;
11		pu_cfg_set_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: SET bit;
10		pu_cfg_set_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: SET bit;
9		pu_cfg_set_bpi4	**PAD_BPI4** 0: Keep; 1: SET bit;
8		pu_cfg_set_bpi3	**PAD_BPI3** 0: Keep; 1: SET bit;
7		pu_cfg_set_bpi2	**PAD_BPI2** 0: Keep; 1: SET bit;
6		pu_cfg_set_bpi1	**PAD_BPI1** 0: Keep; 1: SET bit;
5		pu_cfg_set_bpi0	**PAD_BPI0** 0: Keep; 1: SET bit;
4		pu_cfg_set_gpio_34	**PAD_GPIO_34** 0: Keep; 1: SET bit;
3		pu_cfg_set_gpio_33	**PAD_GPIO_33** 0: Keep; 1: SET bit;
2		pu_cfg_set_gpio_32	**PAD_GPIO_32** 0: Keep; 1: SET bit;
1		pu_cfg_set_gpio_31	**PAD_GPIO_31** 0: Keep; 1: SET bit;
0		pu_cfg_set_gpio_30	**PAD_GPIO_30** 0: Keep; 1: SET bit;

A20D0050 PU_CFG0_CLR GPIO PU Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	pu_cfg_clr_bond_rsv	pu_cfg_clr_bond_sf_sip	pu_cfg_clr_bond_psram_sip	pu_cfg_clr_srclkenai	pu_cfg_clr_mipi_sdata	pu_cfg_clr_mipi_sclk	pu_cfg_clr_bpi4	pu_cfg_clr_bpi3	pu_cfg_clr_bpi2	pu_cfg_clr_bpi1	pu_cfg_clr_bpi0	pu_cfg_clr_gpio_34	pu_cfg_clr_gpio_33	pu_cfg_clr_gpio_32	pu_cfg_clr_gpio_31	pu_cfg_clr_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15		pu_cfg_clr_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: CLEAR bit
14		pu_cfg_clr_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: CLEAR bit
13		pu_cfg_clr_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: CLEAR bit
12		pu_cfg_clr_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: CLEAR bit
11		pu_cfg_clr_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: CLEAR bit
10		pu_cfg_clr_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: CLEAR bit
9		pu_cfg_clr_bpi4	**PAD_BPI4** 0: Keep; 1: CLEAR bit
8		pu_cfg_clr_bpi3	**PAD_BPI3** 0: Keep; 1: CLEAR bit
7		pu_cfg_clr_bpi2	**PAD_BPI2** 0: Keep; 1: CLEAR bit
6		pu_cfg_clr_bpi1	**PAD_BPI1** 0: Keep; 1: CLEAR bit
5		pu_cfg_clr_bpi0	**PAD_BPI0** 0: Keep; 1: CLEAR bit
4		pu_cfg_clr_gpio_34	**PAD_GPIO_34** 0: Keep; 1: CLEAR bit
3		pu_cfg_clr_gpio_33	**PAD_GPIO_33** 0: Keep; 1: CLEAR bit
2		pu_cfg_clr_gpio_32	**PAD_GPIO_32** 0: Keep; 1: CLEAR bit
1		pu_cfg_clr_gpio_31	**PAD_GPIO_31** 0: Keep; 1: CLEAR bit
0		pu_cfg_clr_gpio_30	**PAD_GPIO_30** 0: Keep; 1: CLEAR bit

A20D0054 R0_CFG0 GPIO R0 Control 0000001F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name												r0_cfg_sim0_sclk	r0_cfg_sim0_srst	r0_cfg_sim0_sio	r0_cfg_gpio_36	r0_cfg_gpio_35

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Type												RW	RW	RW	RW	RW
Reset												1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
4		r0_cfg_sim0_sclk	**PAD_SIM0_SCLK** 0: Disable; 1: Enable;
3		r0_cfg_sim0_srst	**PAD_SIM0_SRST** 0: Disable; 1: Enable;
2		r0_cfg_sim0_sio	**PAD_SIM0_SIO** 0: Disable; 1: Enable;
1		r0_cfg_gpio_36	**PAD_GPIO_36** 0: Disable; 1: Enable;
0		r0_cfg_gpio_35	**PAD_GPIO_35** 0: Disable; 1: Enable;

A20D0058 R0_CFG0_SET GPIO R0 Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**r0_cfg_set_sim0_sclk**	**r0_cfg_set_sim0_srst**	**r0_cfg_set_sim0_sio**	**r0_cfg_set_gpio_36**	**r0_cfg_set_gpio_35**
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		r0_cfg_set_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: SET bit;
3		r0_cfg_set_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: SET bit;
2		r0_cfg_set_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: SET bit;
1		r0_cfg_set_gpio_36	**PAD_GPIO_36** 0: Keep; 1: SET bit;
0		r0_cfg_set_gpio_35	**PAD_GPIO_35** 0: Keep; 1: SET bit;

A20D005C R0_CFG0_CLR GPIO R0 Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**r0_cfg_clr_sim0_sclk**	**r0_cfg_clr_sim0_srst**	**r0_cfg_clr_sim0_sio**	**r0_cfg_clr_gpio_36**	**r0_cfg_clr_gpio_35**

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Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		r0_cfg_clr_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: CLEAR bit
3		r0_cfg_clr_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: CLEAR bit
2		r0_cfg_clr_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: CLEAR bit
1		r0_cfg_clr_gpio_36	**PAD_GPIO_36** 0: Keep; 1: CLEAR bit
0		r0_cfg_clr_gpio_35	**PAD_GPIO_35** 0: Keep; 1: CLEAR bit

A20D0060 R1_CFG0 GPIO R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**r1_cfg_sim0_sclk**	**r1_cfg_sim0_srst**	**r1_cfg_sim0_sio**	**r1_cfg_gpio_36**	**r1_cfg_gpio_35**
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		r1_cfg_sim0_sclk	**PAD_SIM0_SCLK** 0: Disable; 1: Enable;
3		r1_cfg_sim0_srst	**PAD_SIM0_SRST** 0: Disable; 1: Enable;
2		r1_cfg_sim0_sio	**PAD_SIM0_SIO** 0: Disable; 1: Enable;
1		r1_cfg_gpio_36	**PAD_GPIO_36** 0: Disable; 1: Enable;
0		r1_cfg_gpio_35	**PAD_GPIO_35** 0: Disable; 1: Enable;

A20D0064 R1_CFG0_SET GPIO R1 Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**r1_cfg_set_sim0_sclk**	**r1_cfg_set_sim0_srst**	**r1_cfg_set_sim0_sio**	**r1_cfg_set_gpio_36**	**r1_cfg_set_gpio_35**
Type												WO	WO	WO	WO	WO

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Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		r1_cfg_set_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: SET bit;
3		r1_cfg_set_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: SET bit;
2		r1_cfg_set_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: SET bit;
1		r1_cfg_set_gpio_36	**PAD_GPIO_36** 0: Keep; 1: SET bit;
0		r1_cfg_set_gpio_35	**PAD_GPIO_35** 0: Keep; 1: SET bit;

A20D0068 R1_CFG0_CLR **GPIO R1 Control for Bitwise Access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												r1_cfg_clr_sim0_sclk	r1_cfg_clr_sim0_srst	r1_cfg_clr_sim0_sio	r1_cfg_clr_gpio_36	r1_cfg_clr_gpio_35
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		r1_cfg_clr_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: CLEAR bit
3		r1_cfg_clr_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: CLEAR bit
2		r1_cfg_clr_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: CLEAR bit
1		r1_cfg_clr_gpio_36	**PAD_GPIO_36** 0: Keep; 1: CLEAR bit
0		r1_cfg_clr_gpio_35	**PAD_GPIO_35** 0: Keep; 1: CLEAR bit

A20D006C RDSEL_CFG0 **GPIO RX Duty Select** **00000000**

RDSEL[0]: level shifter duty high when asserted
RDSEL[1]: level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	rdsel_cfg_sim0_srst		rdsel_cfg_sim0_sio		rdsel_cfg_mipi_sdata		rdsel_cfg_mipi_sclk		rdsel_cfg_bpi4		rdsel_cfg_bpi3		rdsel_cfg_bpi2		rdsel_cfg_bpi1	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rdsel_cfg_b		rdsel_cfg_g		rdsel_cfg_g		rdsel_cfg_g		rdsel_cfg_g		rdsel_cfg_g		rdsel_cfg_g		rdsel_cfg_g	

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	pi0		pio_36		pio_35		pio_34		pio_33		pio_32		pio_31		pio_30	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:30		rdsel_cfg_sim0_srst	**PAD_SIM0_SRST**
29:28		rdsel_cfg_sim0_sio	**PAD_SIM0_SIO**
27:26		rdsel_cfg_mipi_sdata	**PAD_MIPI_SDATA**
25:24		rdsel_cfg_mipi_sclk	**PAD_MIPI_SCLK**
23:22		rdsel_cfg_bpi4	**PAD_BPI4**
21:20		rdsel_cfg_bpi3	**PAD_BPI3**
19:18		rdsel_cfg_bpi2	**PAD_BPI2**
17:16		rdsel_cfg_bpi1	**PAD_BPI1**
15:14		rdsel_cfg_bpi0	**PAD_BPI0**
13:12		rdsel_cfg_gpio_36	**PAD_GPIO_36**
11:10		rdsel_cfg_gpio_35	**PAD_GPIO_35**
9:8		rdsel_cfg_gpio_34	**PAD_GPIO_34**
7:6		rdsel_cfg_gpio_33	**PAD_GPIO_33**
5:4		rdsel_cfg_gpio_32	**PAD_GPIO_32**
3:2		rdsel_cfg_gpio_31	**PAD_GPIO_31**
1:0		rdsel_cfg_gpio_30	**PAD_GPIO_30**

A20D0070 RDSEL_CFG1 **GPIO RX Duty Select** **00000000**

RDSEL[0]: level shifter duty high when asserted
RDSEL[1]: level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							rdsel_cfg_bond_rsv		rdsel_cfg_bond_sf_sip		rdsel_cfg_bond_psram_sip		rdsel_cfg_srclkenai		rdsel_cfg_sim0_sclk	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
9:8		rdsel_cfg_bond_rsv	**PAD_BOND_RSV**
7:6		rdsel_cfg_bond_sf_sip	**PAD_BOND_SF_SIP**
5:4		rdsel_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP**
3:2		rdsel_cfg_srclkenai	**PAD_SRCLKENAI**
1:0		rdsel_cfg_sim0_sclk	**PAD_SIM0_SCLK**

A20D0084 SMT_CFG0 **GPIO RX Input Buffer Schmitt Trigger Hysteresis Control Enable.** **00000000**

High asserted.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												smt_cfg_bond_rs	smt_cfg_bond_sf	smt_cfg_bond_p	smt_cfg_srclken	smt_cfg_sim0_s

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												v	_sip	sram _sip	ai	clk
Type												RW	RW	RW	RW	RW
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smt_cfg_sim0_srst	smt_cfg_sim0_sio	smt_cfg_mipi_sdata	smt_cfg_mipi_sclk	smt_cfg_bpi4	smt_cfg_bpi3	smt_cfg_bpi2	smt_cfg_bpi1	smt_cfg_bpi0	smt_cfg_gpio_36	smt_cfg_gpio_35	smt_cfg_gpio_34	smt_cfg_gpio_33	smt_cfg_gpio_32	smt_cfg_gpio_31	smt_cfg_gpio_30
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		smt_cfg_bond_rsv	**PAD_BOND_RSV** 0: Disable; 1: Enable;
19		smt_cfg_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Disable; 1: Enable;
18		smt_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Disable; 1: Enable;
17		smt_cfg_srclkenai	**PAD_SRCLKENAI** 0: Disable; 1: Enable;
16		smt_cfg_sim0_sclk	**PAD_SIM0_SCLK** 0: Disable; 1: Enable;
15		smt_cfg_sim0_srst	**PAD_SIM0_SRST** 0: Disable; 1: Enable;
14		smt_cfg_sim0_sio	**PAD_SIM0_SIO** 0: Disable; 1: Enable;
13		smt_cfg_mipi_sdata	**PAD_MIPI_SDATA** 0: Disable; 1: Enable;
12		smt_cfg_mipi_sclk	**PAD_MIPI_SCLK** 0: Disable; 1: Enable;
11		smt_cfg_bpi4	**PAD_BPI4** 0: Disable; 1: Enable;
10		smt_cfg_bpi3	**PAD_BPI3** 0: Disable; 1: Enable;
9		smt_cfg_bpi2	**PAD_BPI2** 0: Disable; 1: Enable;
8		smt_cfg_bpi1	**PAD_BPI1** 0: Disable; 1: Enable;
7		smt_cfg_bpi0	**PAD_BPI0** 0: Disable; 1: Enable;
6		smt_cfg_gpio_36	**PAD_GPIO_36** 0: Disable; 1: Enable;
5		smt_cfg_gpio_35	**PAD_GPIO_35** 0: Disable; 1: Enable;
4		smt_cfg_gpio_34	**PAD_GPIO_34** 0: Disable; 1: Enable;
3		smt_cfg_gpio_33	**PAD_GPIO_33** 0: Disable; 1: Enable;
2		smt_cfg_gpio_32	**PAD_GPIO_32** 0: Disable; 1: Enable;
1		smt_cfg_gpio_31	**PAD_GPIO_31** 0: Disable; 1: Enable;
0		smt_cfg_gpio_30	**PAD_GPIO_30** 0: Disable; 1: Enable;

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Bit(s)	Mnemonic	Name	Description

A20D0088 SMT_CFG0_SET GPIO SMT Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												smt_cfg_set_bond_rsv	smt_cfg_set_bond_sf_sip	smt_cfg_set_bond_psram_sip	smt_cfg_set_srclkenai	smt_cfg_set_sim0_sclk
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smt_cfg_set_sim0_srst	smt_cfg_set_sim0_sio	smt_cfg_set_mipi_sdata	smt_cfg_set_mipi_sclk	smt_cfg_set_bpi4	smt_cfg_set_bpi3	smt_cfg_set_bpi2	smt_cfg_set_bpi1	smt_cfg_set_bpi0	smt_cfg_set_gpio_36	smt_cfg_set_gpio_35	smt_cfg_set_gpio_34	smt_cfg_set_gpio_33	smt_cfg_set_gpio_32	smt_cfg_set_gpio_31	smt_cfg_set_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		smt_cfg_set_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: SET bit;
19		smt_cfg_set_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: SET bit;
18		smt_cfg_set_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: SET bit;
17		smt_cfg_set_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: SET bit;
16		smt_cfg_set_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: SET bit;
15		smt_cfg_set_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: SET bit;
14		smt_cfg_set_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: SET bit;
13		smt_cfg_set_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: SET bit;
12		smt_cfg_set_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: SET bit;
11		smt_cfg_set_bpi4	**PAD_BPI4** 0: Keep; 1: SET bit;
10		smt_cfg_set_bpi3	**PAD_BPI3** 0: Keep; 1: SET bit;
9		smt_cfg_set_bpi2	**PAD_BPI2** 0: Keep; 1: SET bit;
8		smt_cfg_set_bpi1	**PAD_BPI1** 0: Keep; 1: SET bit;
7		smt_cfg_set_bpi0	**PAD_BPI0** 0: Keep; 1: SET bit;
6		smt_cfg_set_gpio_36	**PAD_GPIO_36** 0: Keep; 1: SET bit;
5		smt_cfg_set_gpio_35	**PAD_GPIO_35** 0: Keep; 1: SET bit;
4		smt_cfg_set_gpio_34	**PAD_GPIO_34**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: SET bit;
3		smt_cfg_set_gpio_33	**PAD_GPIO_33** 0: Keep; 1: SET bit;
2		smt_cfg_set_gpio_32	**PAD_GPIO_32** 0: Keep; 1: SET bit;
1		smt_cfg_set_gpio_31	**PAD_GPIO_31** 0: Keep; 1: SET bit;
0		smt_cfg_set_gpio_30	**PAD_GPIO_30** 0: Keep; 1: SET bit;

A20D008C SMT_CFG0_CLR GPIO SMT Control for Bitwise Access 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												smt_cfg_clr_bond_rsv	smt_cfg_clr_bond_sf_sip	smt_cfg_clr_bond_psram_sip	smt_cfg_clr_srclkenai	smt_cfg_clr_sim0_sclk
Type												WO	WO	WO	WO	WO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	smt_cfg_clr_sim0_srst	smt_cfg_clr_sim0_sio	smt_cfg_clr_mipi_sdata	smt_cfg_clr_mipi_sclk	smt_cfg_clr_bpi4	smt_cfg_clr_bpi3	smt_cfg_clr_bpi2	smt_cfg_clr_bpi1	smt_cfg_clr_bpi0	smt_cfg_clr_gpio_36	smt_cfg_clr_gpio_35	smt_cfg_clr_gpio_34	smt_cfg_clr_gpio_33	smt_cfg_clr_gpio_32	smt_cfg_clr_gpio_31	smt_cfg_clr_gpio_30
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
20		smt_cfg_clr_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: CLEAR bit
19		smt_cfg_clr_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: CLEAR bit
18		smt_cfg_clr_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: CLEAR bit
17		smt_cfg_clr_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: CLEAR bit
16		smt_cfg_clr_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: CLEAR bit
15		smt_cfg_clr_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: CLEAR bit
14		smt_cfg_clr_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: CLEAR bit
13		smt_cfg_clr_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: CLEAR bit
12		smt_cfg_clr_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: CLEAR bit
11		smt_cfg_clr_bpi4	**PAD_BPI4** 0: Keep; 1: CLEAR bit
10		smt_cfg_clr_bpi3	**PAD_BPI3** 0: Keep; 1: CLEAR bit
9		smt_cfg_clr_bpi2	**PAD_BPI2** 0: Keep; 1: CLEAR bit

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Bit(s)	Mnemonic	Name	Description
8		smt_cfg_clr_bpi1	**PAD_BPI1** 0: Keep; 1: CLEAR bit
7		smt_cfg_clr_bpi0	**PAD_BPI0** 0: Keep; 1: CLEAR bit
6		smt_cfg_clr_gpio_36	**PAD_GPIO_36** 0: Keep; 1: CLEAR bit
5		smt_cfg_clr_gpio_35	**PAD_GPIO_35** 0: Keep; 1: CLEAR bit
4		smt_cfg_clr_gpio_34	**PAD_GPIO_34** 0: Keep; 1: CLEAR bit
3		smt_cfg_clr_gpio_33	**PAD_GPIO_33** 0: Keep; 1: CLEAR bit
2		smt_cfg_clr_gpio_32	**PAD_GPIO_32** 0: Keep; 1: CLEAR bit
1		smt_cfg_clr_gpio_31	**PAD_GPIO_31** 0: Keep; 1: CLEAR bit
0		smt_cfg_clr_gpio_30	**PAD_GPIO_30** 0: Keep; 1: CLEAR bit

A20D0090 SR_CFG0 **GPIO Output Slew Rate Control.** **00000000**

High asserted. SR=1, slower slew. SR=0, no slew rate controlled.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									sr_cfg_bond_rsv	sr_cfg_bond_sf_sip	sr_cfg_bond_psram_sip	sr_cfg_srclkenai	sr_cfg_sim0_sclk		sr_cfg_sim0_srst	
Type									RW	RW	RW	RW	RW		RW	
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sr_cfg_sim0_sio		sr_cfg_mipi_sdata	sr_cfg_mipi_sclk	sr_cfg_bpi4	sr_cfg_bpi3	sr_cfg_bpi2	sr_cfg_bpi1	sr_cfg_bpi0	sr_cfg_gpio_36	sr_cfg_gpio_35	sr_cfg_gpio_34	sr_cfg_gpio_33	sr_cfg_gpio_32	sr_cfg_gpio_31	sr_cfg_gpio_30
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		sr_cfg_bond_rsv	**PAD_BOND_RSV** 0: Disable; 1: Enable;
22		sr_cfg_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Disable; 1: Enable;
21		sr_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Disable; 1: Enable;
20		sr_cfg_srclkenai	**PAD_SRCLKENAI** 0: Disable; 1: Enable;
19:18		sr_cfg_sim0_sclk	**PAD_SIM0_SCLK** 00: non-SIM card mode; 11: SIM card mode;
17:16		sr_cfg_sim0_srst	**PAD_SIM0_SRST** 00: non-SIM card mode; 11: SIM card mode;

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Bit(s)	Mnemonic	Name	Description
15:14		sr_cfg_sim0_sio	**PAD_SIM0_SIO** 00: non-SIM card mode; 11: SIM card mode;
13		sr_cfg_mipi_sdata	**PAD_MIPI_SDATA** 0: Disable; 1: Enable;
12		sr_cfg_mipi_sclk	**PAD_MIPI_SCLK** 0: Disable; 1: Enable;
11		sr_cfg_bpi4	**PAD_BPI4** 0: Disable; 1: Enable;
10		sr_cfg_bpi3	**PAD_BPI3** 0: Disable; 1: Enable;
9		sr_cfg_bpi2	**PAD_BPI2** 0: Disable; 1: Enable;
8		sr_cfg_bpi1	**PAD_BPI1** 0: Disable; 1: Enable;
7		sr_cfg_bpi0	**PAD_BPI0** 0: Disable; 1: Enable;
6		sr_cfg_gpio_36	**PAD_GPIO_36** 0: Disable; 1: Enable;
5		sr_cfg_gpio_35	**PAD_GPIO_35** 0: Disable; 1: Enable;
4		sr_cfg_gpio_34	**PAD_GPIO_34** 0: Disable; 1: Enable;
3		sr_cfg_gpio_33	**PAD_GPIO_33** 0: Disable; 1: Enable;
2		sr_cfg_gpio_32	**PAD_GPIO_32** 0: Disable; 1: Enable;
1		sr_cfg_gpio_31	**PAD_GPIO_31** 0: Disable; 1: Enable;
0		sr_cfg_gpio_30	**PAD_GPIO_30** 0: Disable; 1: Enable;

A20D0094 SR_CFG0_SET **GPIO Slew Rate Control for Bitwise Access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									sr_cfg_set_bond_rsv	sr_cfg_set_bond_sf_sip	sr_cfg_set_bond_psram_sip	sr_cfg_set_srclkenai	sr_cfg_set_sim0_sclk		sr_cfg_set_sim0_srst	
Type									WO	WO	WO	WO	WO		WO	
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sr_cfg_set_sim0_sio		sr_cfg_set_mipi_sdata	sr_cfg_set_mipi_sclk	sr_cfg_set_bpi4	sr_cfg_set_bpi3	sr_cfg_set_bpi2	sr_cfg_set_bpi1	sr_cfg_set_bpi0	sr_cfg_set_gpio_36	sr_cfg_set_gpio_35	sr_cfg_set_gpio_34	sr_cfg_set_gpio_33	sr_cfg_set_gpio_32	sr_cfg_set_gpio_31	sr_cfg_set_gpio_30
Type	WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		sr_cfg_set_bond_rsv	**PAD_BOND_RSV**

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Bit(s)	Mnemonic	Name	Description
			0: Keep; 1: SET bit;
22		sr_cfg_set_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: SET bit;
21		sr_cfg_set_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: SET bit;
20		sr_cfg_set_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: SET bit;
19:18		sr_cfg_set_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: SET bit;
17:16		sr_cfg_set_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: SET bit;
15:14		sr_cfg_set_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: SET bit;
13		sr_cfg_set_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: SET bit;
12		sr_cfg_set_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: SET bit;
11		sr_cfg_set_bpi4	**PAD_BPI4** 0: Keep; 1: SET bit;
10		sr_cfg_set_bpi3	**PAD_BPI3** 0: Keep; 1: SET bit;
9		sr_cfg_set_bpi2	**PAD_BPI2** 0: Keep; 1: SET bit;
8		sr_cfg_set_bpi1	**PAD_BPI1** 0: Keep; 1: SET bit;
7		sr_cfg_set_bpi0	**PAD_BPI0** 0: Keep; 1: SET bit;
6		sr_cfg_set_gpio_36	**PAD_GPIO_36** 0: Keep; 1: SET bit;
5		sr_cfg_set_gpio_35	**PAD_GPIO_35** 0: Keep; 1: SET bit;
4		sr_cfg_set_gpio_34	**PAD_GPIO_34** 0: Keep; 1: SET bit;
3		sr_cfg_set_gpio_33	**PAD_GPIO_33** 0: Keep; 1: SET bit;
2		sr_cfg_set_gpio_32	**PAD_GPIO_32** 0: Keep; 1: SET bit;
1		sr_cfg_set_gpio_31	**PAD_GPIO_31** 0: Keep; 1: SET bit;
0		sr_cfg_set_gpio_30	**PAD_GPIO_30** 0: Keep; 1: SET bit;

A20D0098 SR_CFG0_CLR **GPIO Slew Rate Control for Bitwise Access** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									sr_cfg_clr_bond_rsv	sr_cfg_clr_bond_sf_sip	sr_cfg_clr_bond_psram_sip	sr_cfg_clr_srclkenai	sr_cfg_clr_sim0_sclk		sr_cfg_clr_sim0_srst	
Type									WO	WO	WO	WO	WO		WO	

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Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sr_cfg_clr_sim0_sio		sr_cfg_clr_mipi_sdata	sr_cfg_clr_mipi_sclk	sr_cfg_clr_bpi4	sr_cfg_clr_bpi3	sr_cfg_clr_bpi2	sr_cfg_clr_bpi1	sr_cfg_clr_bpi0	sr_cfg_clr_gpio_36	sr_cfg_clr_gpio_35	sr_cfg_clr_gpio_34	sr_cfg_clr_gpio_33	sr_cfg_clr_gpio_32	sr_cfg_clr_gpio_31	sr_cfg_clr_gpio_30
Type	WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
23		sr_cfg_clr_bond_rsv	**PAD_BOND_RSV** 0: Keep; 1: CLEAR bit
22		sr_cfg_clr_bond_sf_sip	**PAD_BOND_SF_SIP** 0: Keep; 1: CLEAR bit
21		sr_cfg_clr_bond_psram_sip	**PAD_BOND_PSRAM_SIP** 0: Keep; 1: CLEAR bit
20		sr_cfg_clr_srclkenai	**PAD_SRCLKENAI** 0: Keep; 1: CLEAR bit
19:18		sr_cfg_clr_sim0_sclk	**PAD_SIM0_SCLK** 0: Keep; 1: CLEAR bit
17:16		sr_cfg_clr_sim0_srst	**PAD_SIM0_SRST** 0: Keep; 1: CLEAR bit
15:14		sr_cfg_clr_sim0_sio	**PAD_SIM0_SIO** 0: Keep; 1: CLEAR bit
13		sr_cfg_clr_mipi_sdata	**PAD_MIPI_SDATA** 0: Keep; 1: CLEAR bit
12		sr_cfg_clr_mipi_sclk	**PAD_MIPI_SCLK** 0: Keep; 1: CLEAR bit
11		sr_cfg_clr_bpi4	**PAD_BPI4** 0: Keep; 1: CLEAR bit
10		sr_cfg_clr_bpi3	**PAD_BPI3** 0: Keep; 1: CLEAR bit
9		sr_cfg_clr_bpi2	**PAD_BPI2** 0: Keep; 1: CLEAR bit
8		sr_cfg_clr_bpi1	**PAD_BPI1** 0: Keep; 1: CLEAR bit
7		sr_cfg_clr_bpi0	**PAD_BPI0** 0: Keep; 1: CLEAR bit
6		sr_cfg_clr_gpio_36	**PAD_GPIO_36** 0: Keep; 1: CLEAR bit
5		sr_cfg_clr_gpio_35	**PAD_GPIO_35** 0: Keep; 1: CLEAR bit
4		sr_cfg_clr_gpio_34	**PAD_GPIO_34** 0: Keep; 1: CLEAR bit
3		sr_cfg_clr_gpio_33	**PAD_GPIO_33** 0: Keep; 1: CLEAR bit
2		sr_cfg_clr_gpio_32	**PAD_GPIO_32** 0: Keep; 1: CLEAR bit
1		sr_cfg_clr_gpio_31	**PAD_GPIO_31** 0: Keep; 1: CLEAR bit
0		sr_cfg_clr_gpio_30	**PAD_GPIO_30** 0: Keep; 1: CLEAR bit

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A20D009C TDSEL_CFG0 **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			tdsel_cfg_bpi0				tdsel_cfg_gpio_36				tdsel_cfg_gpio_35				tdsel_cfg_gpio_34	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_gpio_33				tdsel_cfg_gpio_32				tdsel_cfg_gpio_31				tdsel_cfg_gpio_30	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
29:28		tdsel_cfg_bpi0	**PAD_BPI0**
25:24		tdsel_cfg_gpio_36	**PAD_GPIO_36**
21:20		tdsel_cfg_gpio_35	**PAD_GPIO_35**
17:16		tdsel_cfg_gpio_34	**PAD_GPIO_34**
13:12		tdsel_cfg_gpio_33	**PAD_GPIO_33**
9:8		tdsel_cfg_gpio_32	**PAD_GPIO_32**
5:4		tdsel_cfg_gpio_31	**PAD_GPIO_31**
1:0		tdsel_cfg_gpio_30	**PAD_GPIO_30**

A20D00A0 TDSEL_CFG1 **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			tdsel_cfg_sim0_sclk		tdsel_cfg_sim0_srst		tdsel_cfg_sim0_sio				tdsel_cfg_mipi_sdata				tdsel_cfg_mipi_sclk	
Type			RW		RW		RW				RW				RW	
Reset			0	0	0	0	0	0			0	0			0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_bpi4				tdsel_cfg_bpi3				tdsel_cfg_bpi2				tdsel_cfg_bpi1	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
29:28		tdsel_cfg_sim0_sclk	**PAD_SIM0_SCLK**
27:26		tdsel_cfg_sim0_srst	**PAD_SIM0_SRST**
25:24		tdsel_cfg_sim0_sio	**PAD_SIM0_SIO**
21:20		tdsel_cfg_mipi_sdata	**PAD_MIPI_SDATA**
17:16		tdsel_cfg_mipi_sclk	**PAD_MIPI_SCLK**
13:12		tdsel_cfg_bpi4	**PAD_BPI4**
9:8		tdsel_cfg_bpi3	**PAD_BPI3**
5:4		tdsel_cfg_bpi2	**PAD_BPI2**
1:0		tdsel_cfg_bpi1	**PAD_BPI1**

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Bit(s)	Mnemonic	Name	Description

A20D00A4 **TDSEL_CFG2** **GPIO TX Duty Select** **00000000**

TDSEL[0]: output level shifter duty high when asserted
TDSEL[1]: output level shifter duty low when asserted

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			tdsel_cfg_bond_rsv				tdsel_cfg_bond_sf_sip				tdsel_cfg_bond_psram_sip				tdsel_cfg_srclkenai	
Type			RW				RW				RW				RW	
Reset			0	0			0	0			0	0			0	0

Bit(s)	Mnemonic	Name	Description
13:12		tdsel_cfg_bond_rsv	**PAD_BOND_RSV**
9:8		tdsel_cfg_bond_sf_sip	**PAD_BOND_SF_SIP**
5:4		tdsel_cfg_bond_psram_sip	**PAD_BOND_PSRAM_SIP**
1:0		tdsel_cfg_srclkenai	**PAD_SRCLKENAI**

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8. Inter-Integrated Circuit Controller

8.1. Overview

Inter-Integrated Circuit (I2C) is a two-wire serial interface. The two signals are SCL and SDA. SCL is a clock signal driven by the master. SDA is a bi-directional data signal that can be driven by either the master or the slave. This generic controller supports master role and conforms to the I2C specification.

8.2. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 8.2-1. Abbreviations

Abbreviation	Definition
SCL	Serial clock line
SDA	Serial data line
ACK	Acknowledgement; SDA is set to 1'b0 in the I2C protocol.
NACK	No acknowledgement; SDA is set to 1'b1 in the I2C protocol.

8.3. Features

- I2C compliant master mode operation
- Adjustable clock speed for Low-Speed and Fast-Speed mode operations
- Supports 7-bit/10-bit addressing
- Supports high-speed mode
- Supports slave clock extension under open-drain mode
- START/STOP/REPEATED START condition
- Polling/DMA transfer mode
- Multi-write per transfer (up to 65535 data bytes)
- Multi-read per transfer (up to 65535 data bytes)
- Multi-transfer per transaction (up to 65535 data bytes)
- Combined format transfer with length change capability
- Active drive/wired-and I/O configuration

8.4. Block diagram

The block diagram of the I2C is shown in Figure 7.3-1.

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Figure 8.4-1. I2C block diagram

8.5. Functions

The controller is designed to be as generic as possible in order to support a wide range of devices for different combinations of transfer formats. Transfer format types supported through different software configurations are listed below:

Note: Terms used in the context of this document.

- Transfer. Any content encapsulated between a pair of Start, Stop and Repeated Start (RS).
- Transfer length. Number of bytes within the transfer.
- Transaction. A transaction contains multiple transfers and is sent after START register is set to 1.
- Transaction length. Number of transfers.

1) Single-byte access. In this case, TRANSAC_LEN and TRANSFER_LEN are both set to 1.

Figure 8.5-1. I2C single transfer single byte access

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2) Multi-byte access. In this case, TRANSAC_LEN is set to 1 and TRANSFER_LEN is set to N. Overall multi-byte transfer is N bytes with ACKs.

Figure 8.5-2. I2C single transfer multi byte access

3) Multi-byte transfer and multi-transfer (same direction, either read or write). In this case, TRANSAC_LEN is set to X and TRANSFER_LEN is set to N.

Figure 8.5-3. I2C multi transfer multi byte access

4) Multi-byte transfer and multi-transfer with RS (same direction). If RS_STOP is set to 1, the Stop then Start in the middle of transaction will be replaced by Repeated Start.

Figure 8.5-4. I2C multi transfer multi byte access with RS

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5) Combined write or read with Repeated Start (direction change). In this case, TRANSAC_LEN is set to 2, TRANSFER_LEN is set to N and TRANSFER_LEN_AUX is set to M. If DIR_CHANGE is 1, the SLAVE_ADDR LSB will change from 0 to 1, which means write to read, after first transfer. Also the TRANSFER_LEN_AUX will be used after first transfer.

Note:

1) This format only supports write and then read sequence. Read and then write is not supported.
2) The transaction length in Figure 8.5-5 is 2.

Figure 8.5-5. I2C multi transfer multi byte access with direction-change function

8.6. Programming guide

Common transfer programmable parameters

Figure 8.6-1. I2C transfer format programming guide

After all the parameters above are set, set START register to 1. The START register will auto clear to 0 after transaction is over. To learn if the transaction is complete, one can poll the START register or disable INTR_MASK and wait for interrupt.

Output waveform timing programmable parameters

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Figure 8.6-2. I2C timing format programming guide

8.7. Manual and DMA transfer modes for I2C controller

The controller offers two types of transfer modes, manual and DMA.

- In manual mode, in addition to the slave address register, the controller has a built-in 8 byte deep FIFO that allows the MCU to prepare up to 8 bytes of data for a write transfer or read up to 8 bytes of data for a read transfer.
- In DMA mode, the data to and from the FIFO is controlled by DMA transfer and can therefore support up to 65535 bytes of consecutive read or write data read from or written into another memory space. When DMA mode is enabled, the flow control mechanism is also implemented to hold the bus clock (SCL) when FIFO underflow or overflow condition is encountered.

Note: After enabling DMA_EN register in I2C, starting data transfer is not controlled by the START register in I2C, but by a register in DMA (PDMAx_START). To avoid errors, it is suggested to use SOFTRESET and FIFO_ADDR_CLR registers when PDMAx_START is 0.

DMA number	START register	Peripheral
SENSOR_DMA2	PDMA2_START	I2C_0 TX
SENSOR_DMA3	PDMA3_START	I2C_0 RX
SENSOR_DMA4	PDMA4_START	I2C_1 TX
SENSOR_DMA5	PDMA5_START	I2C_1 RX
SENSOR_DMA6	PDMA6_START	I2C_2 TX
SENSOR_DMA7	PDMA7_START	I2C_2 RX

8.8. Register mapping

There are three I2C channels in this SoC.

I2C number	Base address	Feature	Source clock
I2C_0	0xA0110000	Supports DMA mode	Crystal clock 26MHz

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I2C number	Base address	Feature	Source clock
I2C_1	0xA0120000	Supports DMA mode	Crystal clock 26MHz
I2C_2	0xA0130000	Supports DMA mode	Crystal clock 26MHz

Module name: I2C_0 Base address: (+A0110000h)

Address	Name	Width (bits)	Register Function
A0110000	DATA_PORT	32	Data port
A0110004	SLAVE_ADDR	32	Slave address
A0110008	INTR_MASK	32	Interrupt mask
A011000C	INTR_STAT	32	Interrupt status
A0110010	CONTROL	32	Control
A0110014	CONTROL2	32	Control2
A0110020	TRANSFER_LEN	32	Number of bytes per transfer
A0110024	TRANSFER_LEN_AUX	32	Number of bytes per transfer
A0110028	TRANSAC_LEN	32	Number of transfers per transaction
A011002C	DELAY_LEN	32	Inter delay length
A0110030	TIMING	32	Timing control register
A0110034	CLOCK_DIV	32	Clock divergence of I2C source clock
A0110038	START	32	Start the I2C transfer
A0110040	FIFO_STAT	32	FIFO status
A0110048	FIFO_ADDR_CLR	32	FIFO address clear
A0110050	IO_CONFIG	32	IO configuration
A0110060	HS	32	High speed mode
A0110070	SOFTRESET	32	Soft reset
A0110074	DEBUGSTAT	32	Debug status
A0110078	DEBUGCTRL	32	Debug control
A0110080	SPARE	32	SPARE
A0110090	ACK_ERR_REC	32	ACK error recorder

A0110000 DATA_PORT Data port 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA_PORT							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	DATA_PORT	FIFO access port. During master write sequence (slave_addr[0] = 0), this port can be written by APB and during master read sequence (slave_addr[0] = 1), this port can be read by APB.

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Bit(s)	Name	Description
		Note, that slave_addr must be set correctly before accessing the FIFO. (DEBUG ONLY) If the fifo_apb_debug bit is set, then the FIFO can be read and written by the APB.

A0110004 SLAVE_ADDR Slave address 000000BF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SLAVE_ADDR							
Type									RW							
Reset									1	0	1	1	1	1	1	1

Bit(s)	Name	Description
7:0	SLAVE_ADDR	**This specifies the slave address of the device to be accessed. Bit 0 is defined by the I2C protocol to indicate the direction of a transfer.** 1: master read 0: master write

A0110008 INTR_MASK Interrupt mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MASK_HS_NACKERR
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MASK_ACKERR								MASK_TRANSAC_COMP
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
16	MASK_HS_NACKERR	**Mask of HS Mode NACK error interrupt** 0:disable
8	MASK_ACKERR	**Mask of ACK error interrupt**

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Bit(s)	Name	Description
		0:disable
0	MASK_TRANSAC_COMP	**Mask of transaction complete interrupt** 0:disable

A011000C INTR_STAT Interrupt status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																HS_NACKERR
Type																W1C
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ACKERR								TRANSAC_COMP
Type								W1C								W1C
Reset								0								0

Bit(s)	Name	Description
16	HS_NACKERR	**This status is asserted if the HS master code NACK error detection is enabled. If enabled, the transaction will be stopped.**
8	ACKERR	**This status is asserted if ACK error detection is enabled. If enabled, the transaction will be stopped.**
0	TRANSAC_COMP	**This status is asserted when a transaction is complete.**

A0110010 CONTROL Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								TRANSFER_LEN_CHANGE								DIR_CHANGE
Type								RW								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								DMA_EN								RS_STOP
Type								RW								RW
Reset								0								0

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Bit(s)	Name	Description
24	TRANSFER_LEN_CHANGE	**This option specifies whether to change the transfer length after the first transfer is complete. If enabled, the transfers after the first transfer will use the TRANSFER_LEN_AUX parameter.** 0:disable
16	DIR_CHANGE	**This option is used for combined transfer format, where the direction of transfer is to be changed from write to read after the FIRST RS condition. Note: when set to 1, the transfers after the direction change will be based on the TRANSFER_LEN_AUX parameter.** 0:disable
8	DMA_EN	**By default, this option is disabled, and FIFO data shall be manually prepared by MCU. This setting is used for transfer sizes of less than 8 bytes and no multiple transfer is configured. When enabled, DMA requests are turned on, and the FIFO data is prepared in memory.** 0:disable
0	RS_STOP	**In LS/FS mode, this bit affects multi-transfer transaction only. It controls whether REPEATED-START condition is used between transfers. The last transfer always ends with a STOP.** In HS mode, this bit must be set to 1. 0: use STOP 1: use REPEATED-START

A0110014 CONTROL2 Control2 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																CLK_EXT_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								ACKERR_DET_EN								HS_NACKERR_DET_EN
Type								RW								RW
Reset								0								1

Bit(s)	Name	Description
16	CLK_EXT_EN	**I2C specification enables a slave device to hold the SCL line low if it's not yet ready for further processing. Therefore, if this bit is set to 1, master controller will enter a high wait state until the slave releases the SCL line. Note, that this feature is only supported under open-drain mode.** 0:disable
8	ACKERR_DET_EN	**This option enables slave ACK error detection. When enabled, if slave ACK error is detected, the master**

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Bit(s)	Name	Description
		terminates the transaction issuing a STOP condition and then asserts ACK error interrupt. The user software handles the error and then resets the FIFO address before reissuing transaction. If this option is disabled, the controller will ignore the slave ACK error and continue with the scheduled transaction. 0:disable
0	HS_NACKERR_DET_EN	**This enables NACKERR detection during the master code transmission. When enabled, if NACK is not received after master code has been transmitted, the transaction will terminate with a STOP condition.** 0:disable

A0110020 TRANSFER_LEN Number of bytes per transfer 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	TRANSFER_LEN	**This indicates the number of data bytes to be transferred in 1 transfer unit (excluding slave address byte).** Note, no data will be transferred if the value is less than 1.

A0110024 TRANSFER_LEN_AUX Number of bytes per transfer 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSFER_LEN_AUX															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	TRANSFER_LEN_AUX	**This field is valid only when DIR_CHANGE is set to 1. This indicates the number of data bytes to transfer in a single transfer unit (excluding slave address byte) for the transfers following the direction change. If DIR_CHANGE is 1, the first write transfer length depends on TRANSFER_LEN, while the second read transfer length depends on TRANSFER_LEN_AUX. Direction change is always after the first transfer.**

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Bit(s)	Name	Description
		Note, no data will be transferred if the value is less than 1.

A0110028 TRANSAC_LEN Number of transfers per transaction 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TRANSAC_LEN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	TRANSAC_LEN	**This indicates the number of transfers in a single transaction.** Note, no data will be transferred if the value is less than 1.

A011002C DELAY_LEN Inter delay length 00000002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DELAY_LEN							
Type									RW							
Reset									0	0	0	0	0	0	1	0

Bit(s)	Name	Description
7:0	DELAY_LEN	**This sets the wait delay between consecutive transfers when RS_STOP bit is set to 0 (the unit is the same as half pulse width).**

A0110030 TIMING Timing control register 00010303

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								DATA_READ_ADJ						DATA_READ_TIME		
Type								RW						RW		
Reset								0						0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name						SAMPLE_CNT_DIV					STEP_CNT_DIV					
Type						RW					RW					
Reset						0	1	1			0	0	0	0	1	1

Bit(s)	Name	Description
24	DATA_READ_ADJ	**When set to 1, data latch in sampling time during master reads are adjusted according to DATA_READ_TIME value. Otherwise, by default, data is latched at half of the high pulse width point.**
18:16	DATA_READ_TIME	**This value is valid only when DATA_READ_ADJ is set to 1. This can be used to adjust so that data is latched in at earlier sampling points (assuming data is settled by then) This value must be set to less than or equal to half the high pulse width.**
10:8	SAMPLE_CNT_DIV	**Used for LS/FS only. This adjusts the width of each sample.**
5:0	STEP_CNT_DIV	**This specifies the number of samples per half pulse width (each high or low pulse).**

A0110034 CLOCK_DIV Clock divergence of I2C source clock 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														CLOCK_DIV		
Type														RW		
Reset														1	0	0

Bit(s)	Name	Description
2:0	CLOCK_DIV	**f_clock_div is equal to SCK / (CLOCK_DIV+1)**

A0110038 START Start the I2C transfer 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																START
Type																RW
Reset																0

Bit(s)	Name	Description
0	START	**This register starts the transaction on the bus. It is automatically de-asserted at the end of the transaction.**

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Bit(s)	Name	Description

A0110040 FIFO_STAT FIFO status 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RD_ADDR								WR_ADDR			
Type					RO								RO			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FIFO_OFFSET										WR_FULL_RD_EMPTY_	
Type					RO										RO	
Reset					0	0	0	0							0	1

Bit(s)	Name	Description
27:24	RD_ADDR	**The current read address pointer. (Only bit [2:0] has physical meaning.)**
19:16	WR_ADDR	**The current write address pointer. (Only bit [2:0] has physical meaning.)**
11:8	FIFO_OFFSET	**WR_ADDR[3:0] - RD_ADDR[3:0]**
1:0	WR_FULL_RD_EMPTY_	**Bit 0: FIFO is empty; Bit 1: FIFO is full.**

A0110048 FIFO_ADDR_CLR FIFO address clear 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FIFO_ADDR_CLR
Type																WO
Reset																0

Bit(s)	Name	Description
0	FIFO_ADDR_CLR	**When written with a 1'b1, a 1 pulse FIFO_ADDR_CLR is generated to clear the FIFO address back to 0.**

A0110050 IO_CONFIG IO configuration 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								IDLE_OE_EN							SDA_SCL_IO_CONFIG	
Type								RW							RW	
Reset								0							0	0

Bit(s)	Name	Description
8	IDLE_OE_EN	**In open-drain mode, this bit should be set to 0. In push-pull mode, this bit determines whether to drive bus in idle state.** 0: don't drive the bus to logic 1 when the master is in idle state 1: drive the bus to logic 1 when the master is in idle state 0: don't drive bus in idle state 1: drive bus in idle state
1:0	SDA_SCL_IO_CONFIG	**Bit 0 configures SCL IO; Bit 1 configures SDA IO** 00: normal tri-state IO mode (push-pull mode) 11: open-drain mode 0: normal tri-state IO mode 1: open-drain mode

A0110060 HS High speed mode 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						HS_SAMPLE_CNT_DIV								HS_STEP_CNT_DIV		
Type						RW								RW		
Reset						0	0	0						0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						MASTER_CODE										HS_EN
Type						RW										RW
Reset						0	0	0								0

Bit(s)	Name	Description
26:24	HS_SAMPLE_CNT_DIV	**Entering high-speed mode after the master code transfer is complete the sample width becomes dependent on this parameter.**
18:16	HS_STEP_CNT_DIV	**Entering high-speed mode after the master code transfer is complete the number of samples per half pulse width becomes dependent on this value.**
10:8	MASTER_CODE	**This is a 3-bit programmable value to transmit the master code. When set to HS mode, the frequency of master code is defined by TIMING register and the frequency after the master code is defined by HS register.**
0	HS_EN	**This enables high-speed transaction. Note, set the RS_STOP to 1.**

A0110070 SOFTRESET Soft Reset 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SOFT_RESET**
Type																WO
Reset																0

Bit(s)	Name	Description
0	SOFT_RESET	**When written with a 1'b1, a 1 pulse soft reset is used as synchronous reset to reset the I2C internal hardware circuits.**

A0110074 DEBUGSTAT Debug status 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**MASTER_WRITE**
Type																RO
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**MASTER_READ**				**MASTER_STATE**				
Type								RO				RO				
Reset								1				0	0	0	0	0

Bit(s)	Name	Description
16	MASTER_WRITE	**DEBUG ONLY: 1 = current transfer is in the master write direction**
8	MASTER_READ	**DEBUG ONLY: 1 = current transfer is in the master read direction**
4:0	MASTER_STATE	**DEBUG ONLY: reads back the current master_state.** 0: idle state; 1: I2C master is preparing to send out the start bit, SCL=1, SDA=1; 2: I2C master is sending out the start bit, SCL=1, SDA=0; 3: I2C master/slave is preparing to transmit data bit, SCL=0, SDA=data bit (data bit can be changed when SCL=0); 4: I2C master/slave is transmitting data bit, SCL=1, SDA=data bit (data bit is stable when SCL=1); 5: I2C master/slave is preparing to transmit ACK bit, SCL=0, SDA=ACK (ACK bit can be changed when SCL=0); 6: I2C master/slave is transmitting ACK bit, SCL=1, SDA=0 (ACK bit is stable when SCL=1); 7: I2C master is preparing to send out stop bit or repeated-start bit, SCL=0, SDA=0/1 (0: means stop bit; 1: means repeated-start bit); 8: I2C master is sending out stop bit or repeated-start bit, SCL=1,

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Bit(s)	Name	Description
		SDA=1/0 (1: means stop bit; 0: means repeated-start bit); 9: I2C master is in delay start between two transfers, SCL=1, SDA=1; 10: I2C master is in FIFO wait state; For write transaction, it means FIFO is empty and I2C master is waiting for DMA controller to write data into FIFO; for read transaction, it means FIFO is full and I2C master is waiting for DMA controller to read data from FIFO, SCL=0, SDA=don't care; 12: I2C master is preparing to send out the data bit of master code. This state is used only in high-speed transaction, SCL=0, SDA=data bit of master code (the data bit of master code can be changed when SCL=0); 13: I2C master is sending out the data bit of master code. This state is used only in high-speed transaction, SCL=1, SDA=data bit of master code (the data bit of master code is stable when SCL=1); 14: I2C master/slave is preparing to transmit NACK bit, SCL=0, SDA=NACK bit (NACK bit can be changed when SCL=0); this state is used only in high-speed transaction; 15: I2C master/slave is transmitting NACK bit, SCL=1, SDA=1; this state is used only in high-speed transaction;

A0110078 DEBUGCTRL Debug control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								APB_DEBUG_RD								FIFO_APB_DEBUG
Type								WO								RW
Reset								0								0

Bit(s)	Name	Description
8	APB_DEBUG_RD	**This bit is only valid when FIFO_APB_DEBUG is set to 1. Writing to this register will generate a single pulsed read signal for reading the FIFO data.**
0	FIFO_APB_DEBUG	**This is used for debug purposes. Use debugging tools to view the memory map. Turning this bit on will block the normal APB read access. APB read access to the FIFO is then enabled by writing to APB_DEBUG_RD.** 0:disable

A0110080 SPARE SPARE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SPARE			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SPARE	

A0110090 ACK_ERR_REC ACK error recorder 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACK_ERR_TRANSAC_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACK_ERR_TRANSFER_NO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	ACK_ERR_TRANSAC_NO	**Record transaction number when ACK error happens. It will be automatically cleared after START register**
15:0	ACK_ERR_TRANSFER_NO	**Record transfer number when ACK error happens. It will be automatically cleared after START register**

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9. I2S

9.1. Introduction

Inter-IC sound (I2S), is an electrical serial bus interface standard connecting digital audio devices. It is used for Pulse Code Modulation (PCM) audio data communication between integrated circuits in an electronic device. Clock and serial data signals are separated by the I2S bus, resulting in a lower jitter than average of communications systems that recover the clock from the data stream. There are two I2S interfaces in this SoC.

9.2. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 9.2-1. Abbreviations

Abbreviation	Definition
I2S	Inter-IC sound
PCM	Pulse code modulation
XO	Crystal oscillator
XPLL	Audio phase-locked loop
DMA	Direct memory access
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CR	Control register
DL FIFO	First in first out for download
UL FIFO	First In first out for upload
HD	High definition
GPIO	General purpose input-output

9.3. Features

- I2S can be selected as master or slave
- Supports 16-bit or 24-bit addressing
- Supports mono or stereo transaction
- I2S controllers can be served by the DMA controller
- Sample rate can support either 8, 12, 16, 24, 32, 48, 96 and 192kHz, or 11.025, 22.05, 44.1, 88.2 and 176.4kHz when sharing only one internal PLL.

Detailed specifications of I2S are shown in Table 9.3-1.

Table 9.3-1. I2S protocol specifications

I2S Protocol	Bit Width	Input/output Sample
Master Mode	16b/24b	XO 26MHz: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48kHz, mono/stereo XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4kHz, mono/stereo

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I2S Protocol	Bit Width	Input/output Sample
		XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192kHz, mono/stereo
Slave Mode	16b/24b	XO 26MHz: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz, mono/stereo XPLL 22.5792MHz: 11.025, 22.05, 44.1, 88.2, 176.4 kHz, mono/stereo XPLL 24.576MHz: 8, 12, 16, 24, 32, 48, 96, 192 kHz, mono/stereo

9.4. Block diagram

I2S is placed on AHB bus to support fast data transfers and has APB interface for setting the control register (CR). I2S contains a clock controller, I2S OUT, I2S IN, first in first out for download (DL FIFO) and first in first out for upload (UL FIFO). The block diagram is shown in Figure 7.3-1.

Figure 9.4-1. I2S block diagram

Keywords: Audio Codec, XPLL, CLKCON, I2S, AHB slave, DMA, UL DL FIFO, I2S CR, APB slave, XO (26MHz only), PLL1, PLL2.

9.5. IO interface

- AHB slave interface (refer to AMBA v2.0)
- APB slave interface (refer to AMBA v3.0)
- Maximum internal delay of each interface is 13.3ns. Only supports 16bits per channel.

The I2S mode interface signal description is shown in Table 9.5-1, and the I2S interface for master mode and slave mode is shown in Table 9.5-2 and Table 9.5-3.

Table 9.5-1. I2S interface signal description

PIN name	Signal Description
I2S_MCLK	The base clock of the function.

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PIN name	Signal Description
I2S_BCLK	The bit clock of the interface
I2S_FS (I2S_WS)	The left/right word select or frame sync line of the interface
I2S_TX	Digital audio output
I2S_RX	Digital audio input

Table 9.5-2. I2S mode interface – master mode

PIN name	Direction	Description
I2S_MCLK	Output	26/24.576/22.5792MHz
I2S_BCLK	Master: Output	I2S_FS*32, I2S_FS*64
I2S_FS	Master: Output	11.025, 22.05, 44.1, 88.2, 176.4kHz 8, 12, 16, 24, 32, 48, 96, 192kHz
I2S_TX	Output	TX data
I2S_RX	Input	RX data

Table 9.5-3. I2S mode interface – slave mode

PIN name	Direction	Description
I2S_MCLK	Output	26/24.576/22.5792MHz
I2S_BCLK	Slave: Input	I2S_FS*32, I2S_FS*64
I2S_FS	Slave: Input	11.025, 22.05, 44.1, 88.2, 176.4kHz 8, 12, 16, 24, 32, 48, 96, 192kHz
I2S_TX	Output	TX data
I2S_RX	Input	RX data

Note, for master mode, I2S_MCLK frequencies only support relative sample rates listed in Table 9.5-4**,** I2S_MCLK from 24.576 or 22.5792MHz is for high definition (HD) mode.

Table 9.5-4. Relationship between MCLK and sample rate

I2S_MCLK	Sample Rate
26MHz (XO or XPLL)	8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 kHz
24.576MHz (XPLL)	8, 12, 16, 24, 32, 48, 96, 192kHz
22.5792MHz (XPLL)	11.025, 22.05, 44.1, 88.2, 176.4kHz

9.6. I2S OUT and I2S IN

I2S OUT and I2S IN support standard I2S protocol and both master/slave mode. The 16bits and 24bits I2S protocol is shown in Figure 9.6-1.

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I2S 16bit word length

I2S 24bit word length in 32bit channel length

Figure 9.6-1. I2S protocol waveform

Keywords: I2S_BCLK, I2S_FS, I2S_TX/RX

If the 16bits I2S OUT operates in mono mode, R[15:0] will be the same as L[15:0]. If I2S IN operates in mono mode, R[15:0] will not affect I2S IN's output to UL FIFO. Operation for 24bits I2S is also the same.

Note: When I2S acts as slave and connects to the external codec, I2S IN and I2S OUT will use the same BCLK/FS from the external codec. Therefore, the sample rate of TX/RX should be the same.

9.7. DL FIFO and UL FIFO

DL FIFO and UL FIFO are asynchronous FIFO with depth 8. One side of these asynchronous FIFO is in BUS clock domain and the other is in XPLL or I2S_BCLK clock domain.

9.8. Data format of FIFO

16bits I2S and 24bits I2S data format of FIFO are shown in Table 9.8-1 and Table 9.8-2.

Table 9.8-1. 16bits I2S data format of FIFO

	Byte 3	Byte 2	Byte 1	Byte 0
Stereo	R[15:8]	R[7:0]	L[15:8]	L[7:0]

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	Byte 3	Byte 2	Byte 1	Byte 0
Mono	8'b0	8'b0	L[15:8]	L[7:0]

Table 9.8-2. 24bits I2S data format of FIFO

	Byte 3	Byte 2	Byte 1	Byte 0
Left Channel	L0[23:16]	L0[15:8]	L0[7:0]	8'b0
	Byte 7	**Byte 6**	**Byte 5**	**Byte 4**
Right Channel	R0[23:16]	R0[15:8]	R0[7:0]	8'b0

9.9. Programming guide

I2S supports two I2S interface modes: 16bits I2S Mode and 24bits I2S Mode. Before I2S transfer, GPIO should be set to related modes in the software, please refer to the GPIO section in this manual.

DMA should be turned on to prevent FIFO overflow. For the related DMA register map, please refer to the DMA section in this manual. The I2S_0 DMA programming guide for PSRAM data input is as follows (for I2S_1, change DMA13 to DMA15 and DMA14 to DMA16):

To turn on DMA clock:

- Write: PDN_CLRD0 = 0x1;

To set DMA channel for I2S_TX:

- Write: VDMA13_PGMADDR = 0x10000; //to set start address
- Write: VDMA13_COUNT = 0x9C4; //to set transfer threshold
- Write: VDMA13_FFSIZE = 0x9C4; //to set transfer length
- Write: VDMA13_CON = 0x10200; //[16]: to enable hardware hand shake, [9:8]: to set word size = 2, [4]: to set DIR: 0=peripheral TX

To set DMA channel for I2S_RX:

- Write: VDMA14_PGMADDR = 0x10000; //to set start address
- Write: VDMA14_COUNT = 0x9C4; //to set transfer threshold
- Write: VDMA14_FFSIZE = 0x9C4; //to set transfer length
- Write: VDMA14_CON = 0x10210; //[16]: to enable hardware hand shake, [9:8]: to set word size = 2, [4]: to set DIR: 1=peripheral RX

To start DMA transfer:

- Write: VDMA13_START = 0x8000;
- Write: VDMA14_START = 0x8000;

To use HD mode, please refer to the chapter, "Audio Phase-Locked Loop Controller" to enable XPLL.

9.9.1. I2S general programming guide

1) Select 26MHz source, if XPLL is on,

- Write: I2S1_GLOBAL_CONTROL = 0x40028;

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2) Or XO is 26MHz

- Write: I2S1_GLOBAL_CONTROL= 0x00028;

3) For data loopback test,

- Write: I2S1_GLOBAL_CONTROL[31]=1

4) Select MCLK source I2S1_GLOBAL_CONTROL[29:28]

- For 24.576MHz : 00
- 22.5792MHz : 01
- 26 MHz: 10

9.9.2. 16bits I2S mode

If in master mode,

- Write: I2S1_DL_CONTROL=0x20009;
- Write: I2S1_UL_CONTROL=0x28009;

Or

- Write: I2S1_DL_CONTROL=0x2000D;
- Write: I2S1_UL_CONTROL=0x2800D;

9.9.3. 24bits I2S mode

If in master mode,

- Write: I2S1_DL_CONTROL=0x6008B;
- Write: I2S1_UL_CONTROL=0x6800B;

Or

- Write: I2S1_DL_CONTROL=0x6008F;
- Write: I2S1_UL_CONTROL=0x6800F;

9.9.4. Set sample rate and enable I2S

To set sample rate:

- Write: I2S1_DL_SR_EN_CONTROL__F_CR_I2S1_OUT_SR = 0x0~0x1E; // bit[4]: HD mode
- Write: I2S1_UL_SR_EN_CONTROL__F_CR_I2S1_IN_SR = 0x0~0x1E; // bit[4]: HD mode

To enable clock,

For I2S_0,

- Write: PDN_CLRD0 = 0x20;

For I2S_1,

- Write: PDN_CLRD0 = 0x2;

- Write: I2S1_GLOBAL_EN_CONTROL__F_CR_PDN_AUD_26M = 0;
- Write: I2S1_UL_SR_EN_CONTROL__F_CR_PDN_I2SIN1 = 0;

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- Write: I2S1_DL_SR_EN_CONTROL__F_CR_PDN_I2SO1= 0;

To do soft reset before active,

- Write: I2S1_SOFT_RESET = 0x1;
- Write: I2S1_SOFT_RESET = 0x0;

To enable FIFO and I2S,

- Write: I2S1_GLOBAL_EN_CONTROL__F_CR_I2S1_UL_FIFO_EN = 1;
- Write: I2S1_GLOBAL_EN_CONTROL__F_CR_I2S1_DL_FIFO_EN = 1;
- Write: I2S1_UL_SR_EN_CONTROL__F_CR_I2S1_IN_EN = 1;
- Write: I2S1_DL_SR_EN_CONTROL__F_CR_I2S1_OUT_EN = 1;
- Write: I2S1_GLOBAL_EN_CONTROL__F_CR_I2S1_ENABLE = 1;

To read RX data from FIFO,

For I2S_0,

- Read = ((UINT32P)(0xA1000700))

For I2S_1,

- Read = ((UINT32P)(0xA1000900))

To write data to TX FIFO,

For I2S_0,

- Write: ((UINT32P)(0xA1000600)) = write_data

For I2S_1,

- Write: ((UINT32P)(0xA1000800)) = write_data

9.10. Register mapping

There are two I2S interfaces in this SoC.

I2S number	Base address	Feature	Source clock
I2S_0	0xA0070000	Supports 16-bit/24-bit addressing	Crystal clock 26MHz or XPLL
I2S_1	0xA0080000	Supports 16-bit/24-bit addressing	Crystal clock 26MHz or XPLL

Module name: I2S_0 Base address: (+a0070000h)

Address	Name	Width (bits)	Register Function
A0070000	I2S1_GLOBAL_CONTROL	32	AUDIO TOP CONTROL REGISTER
A0070004	I2S1_DL_CONTROL	32	DL I2S CONTROL REGISTER
A0070008	I2S1_UL_CONTROL	32	UL I2S CONTROL REGISTER
A007000C	I2S1_SOFT_RESET	32	DLUL SOFT RESET REGISTER
A0070030	I2S1_GLOBAL_EN_CONTROL	32	AUDIO TOP ENABLE CONTROL REGISTER
A0070034	I2S1_DL_SR_EN_CON	32	DL I2S SAMPLE RATE ENABLE CONTROL

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Address	Name	Width (bits)	Register Function
	TROL		REGISTER
A0070038	I2S1_UL_SR_EN_CONTROL	32	UL I2S SAMPLE RATE ENABLE CONTROL REGISTER
A007003C	I2S_MONITOR	32	I2S_MONITOR

A0070000 I2S1_GLOBAL_CONTROL AUDIO TOP CONTROL REGISTER 00020028

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CR_I2S1_GLOBAL_CONTROL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CR_I2S1_GLOBAL_CONTROL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Bit(s)	Name	Description
31:0	CR_I2S1_GLOBAL_CONTROL	**[31] CR_I2S_LOOPBACK_DAT** I2S out to I2S in data loopback 0: disable 1: enable [29:28] CR_EXT_MCLK_SEL Reserved [27] CR_I2S_LOOPBACK I2S in/out clk, ws loopback 0: disable 1: enable [18] CR_CK_SEL 26M clock source selection 0 : XTAL 26M 1 : XPLL 26M [17] CR_CODEC_26M_EN cg of internal codec (default on) [14:10] CR_DBG_SEL [9] CR_DL_MONO_DUP When DL_MONO=1, if right channel send duplicate data. 0: right channel send all 0. 1: right channel send the same data as the left. [8] CR_DL_MONO DL MONO mode 0: STEREO 1: MONO [7] CR_DL_LRSW DL with LR switch 0: LR no swap 1: LR swap [5] CR_EXT_MODE External codec mode (slave) 0: internal codec 1: external codec [4] CR_EXT_IO_CK Clock source of external codec mode (slave) 0: from i2s_in

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Bit(s)	Name	Description
		1: from i2s_out [3] CR_ENGEN_EN Engen enable (reserved) [2] CR_UL_MONO_DUP When UL_MONO=1, if right channel send duplicate data. 0: right channel send all 0. 1: right channel send the same data as the left. [1] CR_UL_MONO UL MONO mode 0: STEREO 1: MONO [0] CR_UL_LRSW UL with LR switch 0: LR no swap 1: LR swap

A0070004 I2S1_DL_CONTROL DL I2S CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CR_I2S1_DL_CONTROL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CR_I2S1_DL_CONTROL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CR_I2S1_DL_CONTROL	**[30] I2S_soft_reset** [27] i2s_in_ck_inv [26] i2s_in_ws_inv [17] i2s in out couple mode [7] DL FIFIO 2D EQ Mode [5] I2S ws invert [3] I2S FMT 0: EIAJ 1: I2S [2] I2S slave mode select 0: master mode 1: slave mode [1] I2S WLEN 0: 16 bits 1: 32 bits

A0070008 I2S1_UL_CONTROL UL I2S CONTROL REGISTER 00000008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CR_I2S1_UL_CONTROL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam	CR_I2S1_UL_CONTROL															

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e																
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
31:0	CR_I2S1_UL_CONTROL	**[30] I2S_soft_reset** [27] i2s_in_ck_inv [26] i2s_in_ws_inv [17] i2s in out couple mode [15] low fill zero (when lrck cycle number is 32 and the 24/16 bit is valid, the low 16/24 bit is zero) 0: high bit fill zero (32) 1: low bit fill zero (32) [6] I2S positive edge latch 0: bit_ck negative edge latch in data 1: bit_ck positive edge latch in data [5] I2S ws invert [3] I2S FMT 0: EIAJ (right adjust) 1: I2S [2] I2S slave mode select 0: master mode 1: slave mode [1] I2S WLEN 0: 16 bits 1: 32 bits

A007000C I2S1_SOFT_RESET DLUL SOFT RESET REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CR_I2S1_SOFT_RSTB
Type																RW
Reset																0

Bit(s)	Name	Description
0	CR_I2S1_SOFT_RSTB	**soft reset audio_top and codec, active high.** To reset, please write this bit to 1 and then write 0.

A0070030 I2S1_GLOBAL_EN_CONTROL AUDIO TOP ENABLE CONTROL REGISTER 01000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								CR_PDN								CR_I2S1_

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								_AUD_26M								**UL_FIFO_EN**
Type								RW								RW
Reset								1								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**CR_I2S1_DL_FIFO_EN**								**CR_I2S1_ENABLE**
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
24	CR_PDN_AUD_26M	**0: Normal** 1: Power down
16	CR_I2S1_UL_FIFO_EN	**UL_FIFO enable** 0: disable 1: enable
8	CR_I2S1_DL_FIFO_EN	**DL_FIFO enable** 0: disable 1: enable
0	CR_I2S1_ENABLE	**Audio top enable** 0: disable 1: enable

A0070034 **I2S1_DL_SR_EN_CONTROL** **DL I2S SAMPLE RATE ENABLE CONTROL REGISTER** **00010000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**CR_PDN_I2SO1**
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**CR_I2S1_OUT_SR**												**CR_I2S1_OUT_EN**
Type				RW												RW
Reset				0	0	0	0	0								0

Bit(s)	Name	Description
16	CR_PDN_I2SO1	**0: Normal** 1: Power down
12:8	CR_I2S1_OUT_SR	**[11:8]I2S mode select:** 0000b: 8kHz

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Bit(s)	Name	Description
		0001b: 11.025kHz 0010b: 12kHz 0100b: 16kHz 0101b: 22.05kHz 0110b: 24kHz 1000b: 32kHz 1001b: 44.1kHz 1010b: 48kHz 1011b: 88.2kHz 1100b: 96kHz 1101b: 176.4kHz 1110b: 192kHz 0011b: 384kHz [12] hd_en 0: disable 1: enable
0	CR_I2S1_OUT_EN	**I2S out enable** 0: disable 1: enable

A0070038 I2S1_UL_SR_EN_CONTROL UL I2S SAMPLE RATE ENABLE CONTROL REGISTER 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																CR_PDN_I2SIN1
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				CR_I2S1_IN_SR												CR_I2S1_IN_EN
Type				RW												RW
Reset				0	0	0	0	0								0

Bit(s)	Name	Description
16	CR_PDN_I2SIN1	**0: Normal** 1: Power down
12:8	CR_I2S1_IN_SR	**[11:8]I2S mode select:** 0000b: 8kHz 0001b: 11.025kHz 0010b: 12kHz 0100b: 16kHz 0101b: 22.05kHz 0110b: 24kHz 1000b: 32kHz 1001b: 44.1kHz 1010b: 48kHz 1011b: 88.2kHz 1100b: 96kHz 1101b: 176.4kHz

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Bit(s)	Name	Description
		1110b: 192kHz 0011b: 384kHz [12] hd_en 0: disable 1: enable
0	CR_I2S1_IN_EN	**I2S out enable** 0: disable 1: enable

A007003C I2S_MONITOR I2S_MONITOR 00000101

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CR_I2S_MONITOR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CR_I2S_MONITOR															
Type	RO															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	CR_I2S_MONITOR	**[15:8] i2s_out_bcount_monitor** [7:0] i2s_in_bcount_monitor

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10. Interrupt

10.1. Overview

Mediatek MT2625 supports 77 interrupts each with up to 128 levels of priority. The priority can be changed dynamically. The Nested Vectored Interrupt Controller (NVIC) and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable interrupt tail-chaining.

The processor supports both level and pulse interrupts. A level interrupt is held asserted until it is cleared by the interrupt service routine (ISR) accessing the device. A pulse interrupt is a variant of an edge model.

The vector table is shown in Table 1.1-1.

Table 10.1-1. Vector table for MT2625

Position	Acronym	Description
0	MD_BUS_ERROR	MDSYS Bus Error interrupt
1	TIMER_TICK1	MDSYS PHY_Timer interrupt1
2	TIMER_TICK2	MDSYS PHY_Timer interrupt2
3	TIMER_TICK3	MDSYS PHY_Timer interrupt3
4	LET_WAKEUP	LTE Wakeup interrupt
5	LTE_SLEEP	LTE Sleep interrupt
6	RF_CONFLICT	RF conflict detect interrupt
7	FM	FM interrupt
8	L1_SW_ISR	L1 software interrupt
9	L2_SW_ISR	L2 software interrupt
10		Reserved
11		Reserved
12	FIRQ	Fast External interrupt
13	OS_GPT	OS Timer interrupt
14	DMA_MCU	MCU DMA interrupt
15	DMA_SENSOR	Sensor DMA interrupt
16	SPI_MST0	SPI Master 0 interrupt
17	SPI_MST1	SPI Master 1 interrupt
18	SPI_SLV	SPI Slave interrupt
19	SDIO_SLV	SDIO Slave interrupt
20	SDIO_MST0	SDIO Master0 interrupt
21	SDIO_MST1	SDIO Master1 interrupt
22	SDIO_MST0_WAKEUP	SDIO Master0 Wakeup interrupt
23	SDIO_MST1_WAKEUP	SDIO Master1 Wakeup interrupt
24	TRNG	TRNG interrupt
25	CRYPTO	CRYPTO_ENGINE interrupt

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Position	Acronym	Description
26	UART0	UART0 interrupt
27	UART1	UART1 interrupt
28	UART2	UART2 interrupt
29	UART3	UART3 interrupt
30	I2S0	I2S_0 interrupt
31	I2S1	I2S_1 interrupt
32	I2C0	I2C0 interrupt
33	I2C1	I2C1 interrupt
34	I2C2	I2C2 interrupt
35	RTC	RTC interrupt
36	GPT	GPTIMER interrupt
37	SPM	SPM interrupt
38	WDT	Watchdog Timer interrupt
39	PMU	PMU Digital Macro interrupt
40	EINT	EINT interrupt
41	SFC	SFC interrupt
42	SENSOR_PD	PD Sensor Control interrupt
43	SENSOR_AO_0	AO Sensor Control interrupt
44	SENSOR_AO_1	AO Sensor Control interrupt
45	SENSOR_AO_2	AO Sensor Control interrupt
46	SENSOR_AO_3	AO Sensor Control interrupt
47	KP	KP interrupt
48	USB	USB interrupt
49	USIM	USIM interrupt
50	CIPHER	CIPHER interrupt
51	DMA_PWM	PWMSG interrupt
52	ULS	ULS interrupt
53	MD32_TASK_DONE	MDSYS MCU Task Done interrupt
54	FFT_MCU	FFT MCU interrupt
55	FFT_ERROR	FFT Error interrupt
56	FFT_DSP	FFT DSP interrupt
57	DFE_ERR	DFE Error interrupt
58	CS_IRQ	CS interrupt
59	CS_ERR	CS Error interrupt
60	BRP_VIT_CRC_PASS	Viterbi CRC pass interrupt
61	BRP_VIT_CRC_FAIL	Viterbi CRC fail interrupt
62	BRP_TXBRP	TXBRP done interrupt
63	BRP_RXBRP	RXBRP done interrupt

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Position	Acronym	Description
64	DFT	DFE Error interrupt
65	BaseBand_Reserved_1	Baseband reserve interrupt
66	BaseBand_Reserved_2	Baseband reserve interrupt
67	BaseBand_Reserved_3	Baseband reserve interrupt
68	CM2SYSRQM_OPFETCH_VIO	Security Violation interrupt
69	BSIBPI0	BSIBPI0 interrupt
70	BSIBPI1	BSIBPI1 interrupt
71		Reserved
72		Reserved
73	CSCI_AP_READ	AP Read Software interrupt
74	CSCI_AP_WRITE	AP Write Software interrupt
75	CSCI_MD_READ	MD Read Software interrupt
76	CSCI_MD_WRITE	MD Write Software interrupt

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11. Keypad Scanner

11.1. Introduction

The device supports two types of keypads, 3x3 single keys and 3x3 configurable double keys, and the keypad will not be powered off to support the system wake-up events.

11.2. Abbreviations

Table 11.2-1 lists the abbreviations used in this section.

Table 11.2-1. Abbreviations

Abbreviation	Full Name
KROWx	Keypad row IO
KCOLx	Keypad column IO
PD	Pull-down resistor
PU	Pull-up resistor

11.3. Features and architecture

The 3x3 keypad can be divided into two parts:

1) The keypad interface includes three columns and three rows (see **Figure 11.3-1** and **Figure 11.3-2**);

2) The key detection block provides key pressed, key released and de-bounce mechanisms.

Each time a key is pressed or released, the key detection block senses the change and recognizes if the key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ is issued. The MCU can then read the key(s) pressed directly in registers KP_MEM1 and KP_MEM2. To ensure the key pressed information is not missed, the status register in keypad will not be read-cleared by the Advanced Peripheral Bus (APB) read command. The status register can only be changed by the key-pressed detection Finite State Machine (FSM).

The 3x3 keypad supports 3x3x2 = 18 keys matrix. The 18 keys are divided into 9 subgroups and each group consists of 2 keys and a 20Ω resistor. Based on the 3x3 keypad hardware design description above, there is a limitation where the keypad cannot detect two keys pressed simultaneously if the two keys are in one group, such that the 3*3 keypad cannot detect key 0 and key 1 or key 15 and key 16 pressed simultaneously.

Since the key pressed detection depends on the HIGH or LOW level of the external keypad interface, if the keys are pressed at the same time and there is a key sharing the same column and row with other keys, the pressed key cannot be correctly decoded. For example, if there are three keys pressed: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), both key3 and key4 = (x2, y1) will be detected, and therefore they cannot be distinguished correctly. Hence, the keypad detects only one or two keys pressed simultaneously in any combination. More than two keys pressed simultaneously in a specific pattern will retrieve wrong information.

Table 11.3-1. 3x3 single key order number in column/row matrix

	COL0	COL1	COL2
ROW2	18	19	20
ROW1	9	10	11

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	COL0	COL1	COL2
ROW0	0	1	2

Table 11.3-2. ***3x3 double key order number in column/row matrix***

	COL0	COL1	COL2
ROW2	26/27	28/29	30/31
ROW1	13/14	15/16	17/18
ROW0	0/1	2/3	4/5

Figure 11.3-1. 3x3 single keypad matrix (9 keys)

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Figure 11.3-2. ***3x3 double keypad matrix (18 keys)***

11.3.1. Waveforms

This 3x3 keypad detects one or two keys pressed simultaneously with any combination. **Figure 11.3-3** shows the condition when one key is pressed. **Figure 11.3-4**(a) and **Figure 11.3-4**(b) illustrate the cases of two keys pressed. When keypad detects the key is pressed and then 32kHz pulse width signal (KP_IRQ) is asserted. The Key-pressed Status is asserted, too. Once the key is released, a 32kHz pulse KP_IRQ is asserted again and the Key-pressed status is set to low.

Figure 11.3-3. ***One key pressed with de-bounce mechanism denoted***

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Figure 11.3-4. ***(a) Two keys pressed, case 1; (b) Two keys pressed, case 2***

11.4. Keypad detection flow

11.4.1. Single keypad detection

In single keypad, KROWx is always in output mode and KCOLx always in input mode. KCOLx has low detection capability, which means if there are no keys pressed, KCOLx will be pulled up and KROWx will be pulled low.

In **Figure 11.4-1**, assume A1 key is pressed, KCOLx can detect key pressed by the low pulse signal. According to the order of low pulse time occurrence, t1, t2 and t3 decide which KROWx is pressed. In this example, KCOL0 can detect a low pulse signal at t1 to know A1 key has been pressed.

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Figure 11.4-1. ***Single keypad detection method***

11.4.2. Double keypad detection flow

Figure 11.4-2 is the brief schematic diagram of double keypad internal circuit, including the following characteristics:

1) 20kΩ resistors on new added keys are required.
2) KCOL requires 200kΩ internal PD/PU resistors.
3) KROW requires 2kΩ internal PD resistors.
4) KROW, KCOL data flow should be bi-directional.

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Figure 11.4-2. ***Brief schematic diagram of double keypad***

The detection flow of a single keypad case in double keypad hardware is described in **Figure 11.4-3, Figure 11.4-4 and Figure 11.4-5.**

In Figure 11.4-3, KCOLx is initialized as an input and KROWx as an output. In step 1, internal pull up resistor is enabled to set the KCOLx to high and output low to all of KROWx in step 2. In step 4, if the KCOL0 is pressed, the falling edge signal can be detected from KCOL0 to scan the keys. From step 1 to step 4, we know the KCOL0 is pressed, but we still don't know the key is pressed in which KROWx.

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Figure 11.4-3. ***Single key case***

The keypad row scan is shown in Figure 11.4-4. The pull-up resistor is disabled and the pull-down resistor is enabled to let KCOL0 remain at low in steps 5 and 6. In step 7, KROW0 sends logic high pulse at time t1 if KCOL0 receives high pulse signal at time t1 as key B is still pressed. After step 6 to step 8, the keypad in KROW0 determines whether key B but not key A is pressed**.**

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Figure 11.4-4. ***Row scan***

The row position is decided after the row scan. In Figure 11.4-4, column scanning is conducted to locate the final position of a key is A or B. All KROWx are changed to input mode and pull-down resistor is enabled in step 9. Switch KCOL0 to output mode and send logic high pulse in step 10. According to Voltage Divider Rule, if KROW0 receives logic low level and we can identify that key B is pressed but not key D in the final step 11.

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Figure 11.4-5. ***Column scan***

11.5. Programming guide

11.5.1. Single keypad command sequence example

Step	Address	Register name	R/W		Value	Loop	Register function
1	A21A0020	KP_SEL		W	0x1c70		Select single keypad; Enable 3 rows and 3 columns
2	A21A0018	KP_DEBOUNCE		W	0x0018		Set up de-bounce time
3	A21A0018	KP_DEBOUNCE	R		0x0018	Loop	
4	A21A0024	KP_EN		W	0x0001		Enable keypad

11.5.2. Double keypad command sequence example

Step	Address	Register name	R/W		Value	Loop	Register function
1	A21A0020	KP_SEL		W	0x1c71		Select double keypad; Enable 3 rows and 3 columns

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Step	Address	Register name	R/W		Value	Loop	Register function
2	A21A0018	KP_DEBOUNCE		W	0x0018		Set up de-bounce time
3	A21A001C	KP_SCAN_TIMING		W	0x0011		
4	A21A0018	KP_DEBOUNCE	R		0x0018	Loop	
	A21A0024	KP_EN		W	0x0001		Enable keypad

11.6. Register mapping

Module name: KP Base address: (+A21A0000h)

Address	Name	Width (bits)	Register Function
A21A0000	**KP_STA**	16	**Keypad Status**
A21A0004	**KP_MEM1**	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 0 (LSB) ~ key 15. Refer to Table 11.3-1 and Table 11.3-2.
A21A0008	**KP_MEM2**	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 0 (LSB) ~ key 15. Refer to Table 11.3-1 and Table 11.3-2.
A21A0018	**KP_DEBOUNCE**	16	**De-bounce Period Setting** Defines the waiting period before key pressing or release events are considered stable. If the de-bounce setting is too small, the keypad will be too sensitive and detect too many unexpected key presses. The suitable de-bounce time setting must be adjusted according to the user's habit.
A21A001C	**KP_SCAN_TIMING**	16	**Keypad Scan Timing Adjustment Register** Sets up the 3x3 keypad scan timing. Note: ROW_SCAN_DIV > ROW_ HIGH_PULSE and COL_SCAN_DIV > COL_ HIGH_PULSE. ROW_ HIGH_PULSE /COL_ HIGH_PULSE are used to lower the power consumption for it decreases the actual scan number during the de-bounce time.
A21A0020	**KP_SEL**	16	**Keypad Selection Register** 1: To use single keypad or double keypad 2: Which columns and rows are used when double keypad is used
A21A0024	**KP_EN**	16	**Keypad Enable Register** Enables/Disables keypad.

A21A0000 KP_STA Keypad Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																RO
Reset																0

Overview

Bit(s)	Mnemonic	Name	Description
0	**STA**	STA	**Indicates keypad status** This register will not be cleared by the read operation. 0: No key pressed 1: Key pressed

A21A0004 KP_MEM1 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 0 (LSB) ~ key 15, and the key value "1" means key-released state; "0" means key-pressed state Refer to Table 11.3-1 and Table 11.3-2.

Bit(s)	Mnemonic	Name	Description
15	**KEY15**	KEY15	
14	**KEY14**	KEY14	
13	**KEY13**	KEY13	
12	**KEY12**	KEY12	
11	**KEY11**	KEY11	
10	**KEY10**	KEY10	
9	**KEY9**	KEY9	
8	**KEY8**	KEY8	
7	**KEY7**	KEY7	
6	**KEY6**	KEY6	
5	**KEY5**	KEY5	
4	**KEY4**	KEY4	
3	**KEY3**	KEY3	
2	**KEY2**	KEY2	
1	**KEY1**	KEY1	
0	**KEY0**	KEY0	

A21A0008 KP_MEM2 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY31	KEY30	KEY29	KEY28	KEY27	KEY26	KEY25	KEY24	KEY23	KEY22	KEY21	KEY20	KEY19	KEY18	KEY17	KEY16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview Shows the key-pressed status of key 16 (LSB) ~ key 31. Refer to Table 1.3-1 and Table 1.3-2.

Bit(s)	Mnemonic	Name	Description
15	**KEY31**	KEY31	

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Bit(s)	Mnemonic	Name	Description
14	**KEY30**	KEY30	
13	**KEY29**	KEY29	
12	**KEY28**	KEY28	
11	**KEY27**	KEY27	
10	**KEY26**	KEY26	
9	**KEY25**	KEY25	
8	**KEY24**	KEY24	
7	**KEY23**	KEY23	
6	**KEY22**	KEY22	
5	**KEY21**	KEY21	
4	**KEY20**	KEY20	
3	**KEY19**	KEY19	
2	**KEY18**	KEY18	
1	**KEY17**	KEY17	
0	**KEY16**	KEY16	

A21A0018 KP_DEBOUNCE De-bounce Period Setting 0400

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			DEBOUNCE													
Type			RW													
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

Overview Defines the waiting period before key pressing or release events are considered stable. If the de-bounce setting is too small, the keypad will be too sensitive and detect too many unexpected key presses. The suitable de-bounce time setting must be adjusted according to the user's habit.

Bit(s)	Mnemonic	Name	Description
13:0	**DEBOUNCE**	DEBOUNCE	

A21A001C KP_SCAN_TIMING Keypad Scan Timing Adjustment Register 0011

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_ HIGH_PULSE				ROW_ HIGH_PULSE				COL_SCAN_DIV				ROW_SCAN_DIV			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

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Overview Sets up the 3*3 keypad scan timing for double keypad.

Note: ROW_SCAN_DIV > ROW_ HIGH_PULSE and COL_SCAN_DIV > COL_ HIGH_PULSE. ROW_ HIGH_PULSE /COL_ HIGH_PULSE are used to lower the power consumption for it decreases the actual scan number during the de-bounce time.

Bit(s)	Mnemonic	Name	Description
15:12	**COL_ HIGH_PULSE**	COL_HIGH_PULSE	**Sets up the COL SCAN high pulse, i.e. cycles of the scan high pulse** Default 0 means the high scan pulse needs 1 cycle.
11:8	**ROW_ HIGH_PULSE**	ROW_HIGH_PULSE	**Sets up the ROW SCAN high pulse, i.e. cycles of the scan high pulse** Default 0 means the high scan pulse needs 1 cycle.
7:4	**COL_SCAN_DIV**	COL_SCAN_DIV	**Sets up the COL SCAN cycle which includes COL_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.
3:0	**ROW_SCAN_DIV**	ROW_SCAN_DIV	**Sets up the ROW SCAN cycle which includes ROW_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.

A21A0020 KP_SEL Keypad Selection Register 1C70

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KP1_COL_SEL						KP1_ROW_SEL									KP_SEL
Type	RW						RW									RW
Reset	0	0	0	1	1	1	0	0	0	1	1	1				0

Overview For selecting:
1) To use single keypad or double keypad;
2) Which columns and rows are used when double keypad is used

Bit(s)	Mnemonic	Name	Description
15:10	**KP1_COL_SEL**	KP1_COL_SEL	**Selects which columns are used when double keypad is used** MT2625 supports maximum 3*3 double. col2, col1 and col0 can be used. 0: Disable corresponding column 1: Enable corresponding column
9:4	**KP1_ROW_SEL**	KP1_ROW_SEL	**Selects which rows are used when double keypad is used** MT2625 supports maximum 3*3 double. row2, row1 and row0 can be used. 0: Disable corresponding row 1: Enable corresponding row
0	**KP_SEL**	KP_SEL	**Selects to use single keypad or double keypad** 0: Use single keypad 1: Use double keypad

A21A0024 KP_EN Keypad Enable Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																KP_EN
Type																RW
Reset																0

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Overview Enables/Disables keypad.

Bit(s)	Mnemonic	Name	Description
0	**KP_EN**	KP_EN	0: Disable keypad (both single and double keypad will not work). 1: Enable keypad (either single or double keypad will work).

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12. SD/SDIO Card Controller

12.1. Introduction

The SD card controller (MSDC) supports:

1) SD memory card specification version 2.0
2) SDIO card specification version 2.0

The controller can be configured as a host for the SD/SDIO card. There are two MSDCs in MT2625.

12.2. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 12.2-1. Abbreviations

Abbreviation	Definition
MSDC	SD card controller
PIO	Programmed input/output (PIO), a method for transferring data between the CPU and a peripheral

12.3. Features

The main features of the controller:

- 32-bit access for control registers
- 8, 16, 32-bit access for FIFO in PIO mode
- Built-in CRC circuit
- Supports PIO mode, basic DMA mode, descriptor DMA mode for SD/SDIO
- Interrupt capabilities
- Data rate of up to 52Mbps in 1-bit mode, 52 x 4 Mbps in 4-bit mode, the module is targeted at 52MHz operating clock at 1.1V and 1.3V, and 26MHz at 0.9V
- Programmable serial clock rate on the SD bus (256 gears)
- Card detection capabilities: MT2625 uses the EINT controller for card detection
- Does not support SPI mode for SD memory card
- Does not support suspend or resume for SD memory card

12.4. Block diagram

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Figure 12.4-1Figure 7.3-1 shows the MSDC block diagram.

Figure 12.4-1. MSDC block diagram

12.5. Functions

12.5.1. Pin assignment

Table 12.5-1 and

Table 12.5-2 present the pins required for the SD memory card. Each pin corresponds to one IO pad. Note, that all IO pads have embedded pull-up and pull-down resistors as they are shared by the SD memory card. The resistors are controlled by the MSDC top register. The pull-down resistors for these pins can be used to save power.

Table 12.5-1. Pins of MSDC0

No.	Name	Type	SD Bus	Description
1	MSDC0_CLK	O	CLK	Clock
2	MSDC0_DAT0	I/O/PP	DAT0	Data line bit 0
3	MSDC0_DAT1	I/O/PP	DAT1	Data line bit 1
4	MSDC0_DAT2	I/O/PP	DAT2	Data line bit 2
5	MSDC0_DAT3	I/O/PP	DAT3	Data line bit 3
6	MSDC0_CMD	I/O/PP	CMD	Command/bus state

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Table 12.5-2. Pins of MSDC1

No.	Name	Type	SD Bus	Description
1	MSDC1_CLK	O	CLK	Clock
2	MSDC1_DAT0	I/O/PP	DAT0	Data line bit 0
3	MSDC1_DAT1	I/O/PP	DAT1	Data line bit 1
4	MSDC1_DAT2	I/O/PP	DAT2	Data line bit 2
5	MSDC1_DAT3	I/O/PP	DAT3	Data line bit 3
6	MSDC1_CMD	I/O/PP	CMD	Command/bus state

12.6. Programming sequence

12.6.1. MSDC recommended command sequence

1) SD command without response.

- Check, if SDC_STS.SDCBUSY is 0 before issuing this command.
- Check the status for MSDC_INT.SD_CMDRDY, MSDC_INT.SD_CMDTO and MSDC_INT.SD_RESP_CRCERR bits.

2) SD command with response or R1B.

- Check, if SDC_STS.SDCBUSY is 0 before issuing this command.
- Check the status for MSDC_INT.SD_CMDRDY, MSDC_INT.SD_CMDTO and MSDC_INT.SD_RESP_CRCERR bits.
- The response can be found in SDC_RESP0 to SDC_RESP3.

3) SD command with data read/write transfer.

- Check, if SDC_STS.SDCBUSY is 0 before issuing this command.
- Check MSDC_INT.SD_CMDRDY/SD_CMDTO/SD_RESP_CRCERR bits for command phase status.
- The response can be found in SDC_RESP0 to SDC_RESP3.
- Enable DMA, if needed (DMA_CTRL register should be programmed).

  Note, that DMA_CTRL register should be programmed after command register is programmed.
- PIO mode can also be used to move data (MSDC_FIFOCS, MSDC_RXDATA, MSDC_TXDATA registers).
- PIO mode and DMA mode cannot be switched during transfer or the result will be unexpected.
- Check MSDC_INT.SD_XFER_COMPLETE/ DMA_DONE/ SD_DATTO/ SD_DATA_CRCERR for data phase status.

4) Software can choose to always check the status of SDC_STS.SDCBUSY before issuing a new command. SDC_STS_CMDBUSY represents the command status.

12.7. Register mapping

There are two MSDCs in this SOC. The register definitions are the same except for the module base address.

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Table 12.7-1. MSDC register definition

MSDC number	Base address	Feature
MSDC0	0xA1030000	SD2.0/SDIO2.0
MSDC1	0xA1040000	SD2.0/SDIO2.0

12.7.1. MSDC0 register map

Module name: MSDC0 Base address: (+A1030000h)

Address	Name	Width (bits)	Register Function
A1030000	MSDC_CFG	32	MSDC Configuration Register
A1030004	MSDC_IOCON	32	MSDC IO Configuration Register
A1030008	MSDC_PS	32	MSDC Pin Status Register
A103000C	MSDC_INT	32	MSDC Interrupt Register
A1030010	MSDC_INTEN	32	MSDC Interrupt Enable Register
A1030014	MSDC_FIFOCS	32	MSDC FIFO Control and Status Register
A1030018	MSDC_TXDATA	32	MSDC TX Data Port Register
A103001C	MSDC_RXDATA	32	MSDC RX Data Port Register
A1030030	SDC_CFG	32	SD Configuration Register
A1030034	SDC_CMD	32	SD Command Register
A1030038	SDC_ARG	32	SD Argument Register
A103003C	SDC_STS	32	SD Status Register
A1030040	SDC_RESP0	32	SD Response Register 0
A1030044	SDC_RESP1	32	SD Response Register 1
A1030048	SDC_RESP2	32	SD Response Register 2
A103004C	SDC_RESP3	32	SD Response Register 3
A1030050	SDC_BLK_NUM	32	SD Block Number Register
A1030058	SDC_CSTS	32	SD Card Status Register
A103005C	SDC_CSTS_EN	32	SD Card Status Enable Register
A1030060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register
A1030080	SD_ACMD_RESP	32	SD Auto Command Response Register
A1030090	DMA_SA	32	DMA Start Address Register
A1030094	DMA_CA	32	DMA Current Address Register
A1030098	DMA_CTRL	32	DMA Control Register
A103009C	DMA_CFG	32	DMA Configuration Register
A10300A0	SW_DBG_SEL	32	MSDC Software Debug Selection Register
A10300A4	SW_DBG_OUT	32	MSDC Software Debug Output Register
A10300A8	DMA_LENGTH	32	DMA Length Register
A10300B0	PATCH_BIT0	32	MSDC Patch Bit Register 0
A10300B4	PATCH_BIT1	32	MSDC Patch Bit Register 1
A10300EC	PAD_TUNE	32	MSDC Pad Tuning Register
A10300F0	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0
A10300F4	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1
A10300F8	HW_DBG_SEL	32	MSDC Hardware Debug Selection Register

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Address	Name	Width (bits)	Register Function
A1030100	MAIN_VER	32	MSDC Main Version Register
A1030104	ECO_VER	32	MSDC ECO Version Register

A1030000 MSDC_CFG MSDC Configuration Register 00000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																CARD_CK_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE			CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU			RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1			1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
16	**CCKMD**	CARD_CK_MODE	**MS/SD card clock mode** 1'b0: Use clock divider output where msdc_ ck is divided by msdc_src_ck and program the bits bit[15]~bit[8]. 1'b1: Use msdc_src_ck as msdc_ck, bit[15]~bit[8] are ignored.
15:8	**CCKDIV**	CARD_CK_DIV	**MS/SD card clock divider** The register field controls serial clock frequency on MS/SD bus. In non-DDR mode, msdc_ck is the SD bus clock. For example, for SDR25 or HS, msdc_ck and SD bus clock will be the same at 50MHz. In DDR mode, msdc_ck is twice the SD bus clock. For example, for DDR50, msdc_ck should be set to 100MHz and bus clock will be 50MHz. 8'b00000000: msdc_ck = (1/2) * msdc_src_ck 8'b00000001: msdc_ck = (1/(4*1)) * msdc_src_ck 8'b00000010: msdc_ck = (1/(4*2)) * msdc_src_ck 8'b00000011: msdc_ck = (1/(4*3))* msdc_src_ck 8'b00010000: msdc_ck = (1/(4*16))* msdc_src_ck 8'b11111111: msdc_ck = (1/(4*255)) * msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock stability** After programming the CARD_CK_MODE or CARD_CK_DIV, this bit will immediately go to "0" and return to "1", if the clock output is stable. User should poll this register to ensure the safety control of MSDC. 1'b0: Clock output is not stable 1'b1: Clock output is stable
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS card bus clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver.

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			The default bus state depends on MSDC_CFG[1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN = 1, the default clock is in freerun state. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state is gated to 0. Set this bit to 0 to put the bus state into tri-state. Default is 1. 1'b0: Set the clock pad into tri-state. 1'b1: Enable MSDC to drive the clock pad, the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN
3	**PIO**	PIO_MODE	**MS/SD PIO mode** PIO mode selection. Default is in PIO mode. 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause MS/SD controller internal synchronous reset, and it will not reset register settings and DMA controller. The controller resets when this bit is 0. Software should wait for this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state 1'b1: MS/SD controller is in reset state
1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power down mode** This bit controls the card clock power down mode. 1'b0: Clock is gated to 0, if no command or data is transmitted. 1'b1: Clock is in freerun state even if no command or data is transmitted. The clock may still be stopped when MSDC write data is not enough or there is no space for next read data.
0	**MSDC**	MSDC	**MS/SD mode selection** The register bit is used to configure the controller as the host of a removable storage device or as the host of SD/MMC memory card. The default value is to configure the controller as the host of a removable storage device. 1'b0: Configure the controller as the host of removable storage device. 1'b1: Configure the controller as the host of SD/MMC memory card

A1030004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL		D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL
Type			RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW
Reset			0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Read data 7 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Read data 6 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Read data 5 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Read data 4 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Read data 3 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Read data 2 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Read data 1 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising

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			edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Read data 0 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**CRC Status and SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in write transaction** 1'b0: All data lines share the same value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**CRC Status and SDIO interrupt sample selection** 1'b0: Sample CRC status and SDIO interrupt by

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			external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in read transaction** 1'b0: All data lines share the same value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
3	**DDLSEL**	D_DLYLINE_SEL	**Data line delay line fine tune selection** 1'b0: All data lines share the same delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Read data sample selection** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Command response sample selection** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** This bit is only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output is the inverted msdc_src_ck 1'b1: Bus clock output is the msdc_src_ck

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A1030008 MSDC_PS **MSDC Pin Status Register** **81FF0002**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write protection switch status on SD memory card** The register bit shows the status of the write protection switch on the SD memory card. There is no default reset value. The write protection pin is only used when the controller is configured for the SD memory card. 1'b0: Write protection switch is ON. It means that memory card is write-protected. 1'b1: Write protection Switch is OFF. It means that memory card is writable.
24	**CMD**	CMD	**Command line status** This bit reflects the command line value of the MSDC bus.
23:16	**DAT**	DAT	**Data line status** This bit reflects the data line value of the MSDC bus (8-bits).
15:12	-	Reserved	
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low 1'b1: Card detection pin status is logic high
0	**CDEN**	CDEN	**Card detect enable** The register bit is used to control the card detection circuit. 1'b0: Card detection is disabled 1'b1: Card detection is enabled

A103000C MSDC_INT **MSDC Interrupt Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	
Type													W1C	W1C	W1C	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLET	SD_CSTA	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY	SD_SDIOIRQ	DMA_Q_EMPTY	SD_AUTOCMD_RESP	SD_AUTOCMD_CMD	SD_AUTOCMD_CMD		MSDC_CDSC	MMC_IRQ

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				E							_CRC ERR	TO	RDY			
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**DMAPROTECT**	DMA_PROTECT	**This register identifies if there is a write operation to the DMA start address, length, start bit or last buffer bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD data CRC error interrupt** MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line
14	**SDDTO**	SD_DATTO	**SD data timeout interrupt** Indicates that SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data is not presented. For SD data write, timeout will occur when the write data CRC status is not presented, if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1. 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line.
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** The register bit indicates the status of data block transfer. 1'b0: Otherwise 1'b1: A data block was successfully transferred
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD data transfer complete interrupt** This bit indicates the transaction is complete. While performing tuning procedure (execute tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTA**	SD_CSTA	**SD CSTA update interrupt** This register bit indicates if any bit in the register SDC_CSTA is active, this bit will be set to 1. Software should clear the SDC_CSTA and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt

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			1'b1: SD memory card interrupt exists
10	**SDRCRCER**	SD_RESP_CRCERR	**SD command CRC error interrupt** Indicates that SD/MMC controller detected a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a CRC error after reading a response from the CMD line
9	**SDCTO**	SD_CMDTO	**SD command timeout interrupt** Indicates that SD/MMC controller detected a timeout while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a timeout condition while waiting for a response on the CMD line
8	**SDCRDY**	SD_CMDRDY	**SD command ready interrupt** For a command without response, the register bit will be 1 once the command is complete on SD/MMC bus. For a command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For a command with response with busy in DAT0, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 switched from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without a CRC error.
7	**SDIOIRQ**	SD_SDIOIRQ	**SD SDIO interrupt** This bit indicates an interrupt occurred in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** This bit is used to indicate that the current DMA queue is empty. Only for Descriptor mode and Enhanced mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** This bit is set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** This bit is set if no response is returned within a specified cycle (64 clock cycles in the specification) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** This bit is set if auto command is executed without CRC error or time out.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC card detection status change interrupt**

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			The register bit indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e., the register bit CDEN in the register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: Indicates that MMC card interrupt event occurred

A1030010 MSDC_INTEN MSDC Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BD_CS_ERR	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SD_DATA_CRCERR	EN_SD_DATTO	EN_SD_DMA_XFER_DONE	EN_SD_XFER_COMPLETE	EN_SD_CSTA	EN_SD_RESP_CRCERR	EN_SD_CMDTO	EN_SD_CMDRDY	EN_SD_SDIOIRQ	EN_DMA_Q_EMPTY	EN_SD_AUTOCMD_RESP_CRCERR	EN_SD_AUTOCMD_CMDTO	EN_AUTOCMD_CMDRDY		EN_MSDC_CDSC	EN_MMC_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**DMA protection interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**GPD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**BD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRCERR	**SD data CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**SD data timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER_DONE	**DMA transfer done interrupt enable** 1'b0: Disable interrupt

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			1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COMPLETE	**SD data transfer complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**SD CSTA update interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**SD command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**SD command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**SD command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**SD SDIO interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**DMA queue empty interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**SD auto command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**MSDC card detection status change interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**MMC card interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

A1030014 **MSDC_FIFOCS** **MSDC FIFO Control and Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO CLR								TXFIFOCNT							

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Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RXFIFOCNT**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Embedded FIFO clear** Write 1 into this bit to clear the FIFO. It returns to 0 when FIFO is cleared. Software needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has an error.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1 byte data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read** 8'd0: No data in FIFO 8'd1: 1 byte data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved

A1030018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIO_TXDATA**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PIO_TXDATA**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

A103001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PIO_RXDATA**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

A1030030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSWIDTH	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WAKEUP_INS_EN	WAKEUP_SDIOINT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data Timeout Counter** The period from the end of initial host read command or the last read data block in a multiple block read operation to the start bit of next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1048576 serial clocks. 8'b00000000: Extend 1048576 more serial clock cycles 8'b00000001: Extend 1048576 x 2 more serial clock cycles 8'b00000010: Extend 1048576 x 3 more serial clock cycles 8'b11111111: Extend 1048576 x 256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If

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			the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. 1'b0: Disable interrupt detection at the block gap 1'b1: Enable interrupt detection at the block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**SDIO interrupt detection enable** This bit is to inform the SD controller to sense the SDIO interrupt 1'b0: SDIO interrupt detection is disabled 1'b1: SDIO interrupt detection is enabled if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** This bit is to enable the support to sense the SDIO interrupt and disable the R4 response CRC check for SDIO card 1'b0: SDIO mode is disabled 1'b1: SDIO mode is enabled
17:16	**BUSWD**	BUSWIDTH	**Bus width configuration** This field is used to define the SD/MMC bus width 2'b00: 1 bit mode 2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

A1030034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AUTO_CMD	LEN											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**ACMD**	AUTO_CMD	**Auto command enable**

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			This field determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operations. (1) Auto CMD12 Enable Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when last block transfer completes. Auto CMD12 error is indicated to the MSDC_INT register. The Host Driver shall not set this bit, if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. (2) Auto CMD23 Enable When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later supports this function. By writing the Command register, MSDC issues a CMD23 first and then issues a command specified by the CMD field in SDC_CMD register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit block count value for CMD23 is set to SDC_BLOCK_NUM register. 1'b0: Disable Auto Command 1'b1: Enable Auto CMD12
27:16	**LEN**	LEN	**Length** The register field is used to define the length of one block in unit of byte in a data transaction of block mode or the data length in unit of byte in data transaction of byte mode. The maximum value of block length is 2048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 bytes 12'b011111111111: Block length is 2047 bytes 12'b100000000000: Block length is 2048 bytes
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** The register bit indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** The register bit indicates, if the command is a stop

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			transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Command read write selection** The register bit defines if the command is a read command or write command. The register bit is valid only when the command will cause a transaction with data token. 1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Data block selection** The register field defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction (only available in block mode) 2'b11: Stream operation. It shall only be used in MMC protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bits with CRC check (for SD/MMC/SDIO) (Not including the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Abort a pending MMC GO_IRQ command** It is only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a break command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD memory card command**

A1030038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ARG	ARG	Memory card controller argument register

A103003C **SDC_STS** **SD Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL															CMD_WR_BUSY
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMDBUSY	SDCBUSY
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC Stream mode write data is all flushed to MMC card** Software can use this bit to confirm last write data are flushed to MMC then issue a STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11. 1'b0: Last data are partially inside MSDC 1'b1: Last data are flushed to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD command line busy status** Software should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, software should check the SDCBUSY bit, too. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto command 12 finishes. 1'b0: No transmission in CMD line on SD bus 1'b1: There is transmission in CMD line on SD bus
0	**SDCBSY**	SDCBUSY	**SD controller busy status**

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	1'b0: SD controller is idle 1'b1: SD controller is busy

A1030040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	**Memory card controller response register 0**

A1030044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RESP1	RESP1	Memory card controller response register 1

A1030048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RESP2	RESP2	Memory card controller response register 2

A103004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP3															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP3															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RESP3	RESP3	Memory card controller response register 3

A1030050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BLOCK_NUMBER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BLOCK_NUMBER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** This field indicates the block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data block 32'd3: 3 data block 32'hffffffff: 4GB-1 data block

A1030058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CSTS**															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CSTS**															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	The register provides SD/MMC card status in the response R1 or R1b field. 32'h0: keep the current value Others: write 1 to each bit to clear the corresponding bit.

A103005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CSTS_EN**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	This register is used to control the CSTA bit that will generate MSDC_INT.SDCSTA

A1030060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DAT_CRCSTS_POS							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status** This register reflects the CRC status of data line[7:0]. This register is only for MSDC Read. 1'b0: No CRC error 1'b1: CRC error

A1030080 SD_ACMD_RESP SD Auto Command Response Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD auto command response register** This register stores the response [39:8] of ACMD12/ACMD23/ACMD19.

A1030090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**The start address of the DMA address** This register is used to set the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer, which depends on the command. In Descriptor DMA mode, this is the descriptor chain start address.

A1030094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**The current address of the DMA address** This register is used to read the current address of the DMA descriptor chain.

A1030098 DMA_CTRL DMA Control Register 00006000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE						DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW						WO	A0	WO
Reset		1	1	0	0	0	0	0						0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** This field is used to specify the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**This field is used to specify whether to split burst when it crosses the 1K address boundary** 1'b0:1K boundary not split

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			1'b1:1K boundary split
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** This field indicates the last buffer in the basic DMA mode
9	**DMAALIGN**	DMA_ALIGN	**This field is used to specify whether there is address alignment burst size** 1'b0:No DMA burst size alignment 1'b1:DMA burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** This field indicates the operation mode of DMA 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
2	**DMARSM**	DMA_RESUME	**DMA resume control register** This bit is used to resume the DMA transaction. Read always returns 0
1	**DMASTOP**	DMA_STOP	**DMA stop control register** This bit is used to stop the DMA transaction. When software issues STOP command, it must wait for this bit to de-assert or inactivate the DMA to guarantee a complete stop.
0	**DMASTART**	DMA_START	**DMA start control register** This bit is used to start the DMA transaction. Read always returns 0

A103009C DMA_CFG DMA Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DMA_CHK_SUM_12B
Type																RW
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN								DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW								RW	RU
Reset			0	0			0	0							0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**This register indicates GPD/BD checksum length is 16bytes or 12bytes** 1'b0: GPD/BD checksum cover 16byte 1'b1: GPD/BD checksum only cover 12byte
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**This register indicates how to control msdc_active** 2'b00: dynamic control msdc_active 2'b01: msdc_active = 0

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			2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**This register determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and Basic DMA Mode, all write transfers of a burst are accessed in bufferable mode except the last DMA burst. AHB_HPROT2_2_EN=2'b00, and Descriptor DMA Mode, all write transfers of a burst are accessed in bufferable mode except the hardware's own update transfer. 2'b00: dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**DMA descriptor checksum enable** This bit is used to enable or disable the checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** This bit is used to indicate the status of the DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

A10300A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**MSDC debug selection** Reserved

A10300A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32 bit output selected by SW_DBG_SEL register

A10300A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** This field is used to specify the number of DMA transfer bytes. This field is only valid in basic DMA mode.

A10300B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C004F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV_RESP	DETECT_WR_CRC_TIMEOUT	SPC_ALWAYS_PUSH	SDIO_INT_DLY_SEL	SDC_CMD_CMDFAIL_SEL	SDC_CMD_IDRT_SEL	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INTC_SEL	
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS						INT_DAT_LATCH_CK_SEL			reserved1				DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_ODD_8BIT_SUP	reserved0
Type	RW						RW			RW				RW	RW	RW
Reset	0						0	0	0	1	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enable MSDC always drives the bus, when the output is a wakeup response, such as BREAK.** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**MSDC write data CRC phase timeout detection** 1'b0: Does not detect CRC phase timeout 1'b1: Detects CRC phase timeout

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29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**SDIO interrupt latch time selection** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**SDIO interrupt period recovery selection** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**SD identification response time selection** The register bit indicates if the command has a response with NID (that is, 5 serial clock cycles as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise. 1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD write data output delay** The period from response finish for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in the unit of one serial clock. 4'b0000: Not extended. 4'b0001: Extended by one more serial clock cycle. 4'b0010: Extended by two more serial clock cycles. 4'b1111: Extended by fifteen more serial clock cycles.
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC memory card have finished. The

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			register field is used to extend the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: Not extended. 4'b0001: Extended by one more serial clock cycle. 4'b0010: Extended by two more serial clock cycles. 4'b1111: Extended by fifteen more serial clock cycles.
17	**PTCH17**	SDIO_CFG_INTC_SEL	**SDIO Interrupt model selection** 1'b0: Only when data line [1] = 0 and then trigger SDIO interrupt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interrupt event
15	**PTCH15**	MSDC_FIFO_RD_DIS	**MSDC RXFIFO Read Disable** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Internal MSDC clock phase selection** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck
6:3		reserved1	
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enable SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enable SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0		reserved0	

A10300B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFFE0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CKEN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN	reserved2						ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW						RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BIAS_EXTBIAS_28NM	BIAS_EN18IO_28NM	BIAS_TUNE_28NM				GET_CRC_MARGIN	GET_BUSY_MARGIN	CMD_RSP_TA_CNTR			WRDAT_CRCS_TA_CNTR		

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Type			RW	RW	RW				RW	RW	RW			RW		
Reset			0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable 1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit for SPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22:17		reserved2	
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**The AHB bus will not support incr1 burst type, it only supports the single burst type. It will only affect the AHB bus MSDC design, but not the AXI bus design** 1'b0: hardware will send incr1 burst type 1'b1: hardware will send single burst type instead of incr1 type
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS Controller register 2**

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7	**GETCRCMARGIN**	GET_CRC_MARGIN	**This will add margin for getting the CRC status when the card response CRC does not match with the 2 cycles (described in the SD specification) starting from the end bit** 1'b0: 8 cycles are reserved to get the CRC status from write data CRC end bit 1'b1: 16 cycles reserved for getting CRC status from write data CRC end bit
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**This will add margin for the get busy state of data0** 1'b0: 1 cycle reserved for get busy state from SRC status end bit 1'b1: 3 cycles reserved for get busy state from SRC status end bit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turnaround period** The turnaround cycle = CMD_RSP_TA_CNTR + 2 is only for USH104 mode, this register should be set to 0 in non-UHS104 mode
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turnaround period** The turnaround cycle = WRDAT_CRCS_TA_CNTR + 2 is only for USH104 mode, this register should be set to 0 in non-UHS104 mode

A10300EC PAD_TUNE MSDC Pad Tuning Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAD_CLK_TXDLY					PAD_CMD_RESP_RXDLY					PAD_CMD_RD_RXDLY_SEL	PAD_CMD_RXDLY				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PAD_DAT_RD_RXDLY_SEL	PAD_DAT_RD_RXDLY					DELAY_EN			PAD_DAT_WR_RXDLY				
Type			RW	RW					RW			RW				
Reset			0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**CLK Pad TX Delay Control** This register is used to add delay to CLK phase. Total 32 stages
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**CMD Response Internal Delay Line Control** This register is used to fine-tune response phase latched by MSDC internal clock

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			Total 32 stages
21	**CMDRRDLYSEL**	PAD_CMD_RD_RXDLY_SEL	**Determines, if CMD Response passes through data delay line1 or not** 1'b0: pass 1'b1: do not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**CMD Pad RX Delay Line Control** This register is used to fine-tune CMD pad macro response latch timing Total 32 stages
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Determines, if RX data passes through data delay line1 or not** 1'b0: pass 1'b1: do not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**DAT Pad RX Delay Line Control (for MSDC read only)** This register is used to fine-tune DAT pad macro read data latch timing Total 32 stages
7	**DELAYEN**	DELAY_EN	**Enable all delay cell toggling when powered on** 1'b0: disable delay cell toggling default 1'b1: enable delay cell toggling default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Write Data Status Internal Delay Line Control** This register is used to fine-tune write status phase latched by MSDC internal clock Total 32 stages

A10300F0 DAT_RD_DLY0 MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**DAT0 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**DAT1 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**DAT2 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**DAT3 Pad RX Delay Line Control (for MSDC**

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		Read) Total 32 stages

A10300F4 DAT_RD_DLY1 MSDC Data Delay Line Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4_RD_DLY								DAT5_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6_RD_DLY								DAT7_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY**	DAT4_RD_DLY	**DAT4 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
20:16	**DAT5RDDLY**	DAT5_RD_DLY	**DAT5 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
12:8	**DAT6RDDLY**	DAT6_RD_DLY	**DAT6 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
4:0	**DAT7RDDLY**	DAT7_RD_DLY	**DAT7 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages

A10300F8 HW_DBG_SEL MSDC H/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		HW_DBG_WRAP_SEL	HW_DBG0_SEL						HW_DBG_WRAP_TYPE_SEL		HW_DBG1_SEL					
Type		RW	RW						RW		RW					
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			HW_DBG2_SEL						HW_DBG3_SEL							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**DBGWSEL**	HW_DBG_WRAP_SEL	**Hardware debug output selection for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
29:24	**DBG0SEL**	HW_DBG0_SEL	**Hardware debug output selection**
23:22	**DBGWTSEL**	HW_DBG_WRAP_TYPE_SEL	**Hardware debug output selection for wrapper** 2'd0: Select dbg_in20~dbg_in3b = DRAM_DBG 2'd1: Select dbg_in20~dbg_in3b = RISC_DBG

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			2'd2: Select dbg_in20~dbg_in3b = AHBM_DBG 2'd3: Select dbg_in20~dbg_in3b = AHBS_DBG
21:16	**DBG1SEL**	HW_DBG1_SEL	**Hardware debug output selection**
13:8	**DBG2SEL**	HW_DBG2_SEL	**Hardware debug output selection**
7:0	**DBG3SEL**	HW_DBG3_SEL	**Hardware debug output selection**

A1030100 MAIN_VER MSDC Main Version Register 20160503

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	**Main Version**

A1030104 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	**ECO Version**

12.7.2. MSDC1 register map

Module name: MSDC1 Base address: (+A1040000h)

Address	Name	Width (bits)	Register Function
A1040000	**MSDC_CFG**	32	**MSDC Configuration Register**
A1040004	**MSDC_IOCON**	32	**MSDC IO Configuration Register**
A1040008	**MSDC_PS**	32	**MSDC Pin Status Register**
A104000C	**MSDC_INT**	32	**MSDC Interrupt Register**
A1040010	**MSDC_INTEN**	32	**MSDC Interrupt Enable Register**
A1040014	**MSDC_FIFOCS**	32	**MSDC FIFO Control and Status Register**
A1040018	**MSDC_TXDATA**	32	**MSDC TX Data Port Register**
A104001C	**MSDC_RXDATA**	32	**MSDC RX Data Port Register**
A1040030	**SDC_CFG**	32	**SD Configuration Register**
A1040034	**SDC_CMD**	32	**SD Command Register**
A1040038	**SDC_ARG**	32	**SD Argument Register**

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Address	Name	Width (bits)	Register Function
A104003C	SDC_STS	32	SD Status Register
A1040040	SDC_RESP0	32	SD Response Register 0
A1040044	SDC_RESP1	32	SD Response Register 1
A1040048	SDC_RESP2	32	SD Response Register 2
A104004C	SDC_RESP3	32	SD Response Register 3
A1040050	SDC_BLK_NUM	32	SD Block Number Register
A1040058	SDC_CSTS	32	SD Card Status Register
A104005C	SDC_CSTS_EN	32	SD Card Status Enable Register
A1040060	SDC_DATCRC_STS	32	SD Card Data CRC Status Register
A1040080	SD_ACMD_RESP	32	SD Auto Command Response Register
A1040090	DMA_SA	32	DMA Start Address Register
A1040094	DMA_CA	32	DMA Current Address Register
A1040098	DMA_CTRL	32	DMA Control Register
A104009C	DMA_CFG	32	DMA Configuration Register
A10400A0	SW_DBG_SEL	32	MSDC Software Debug Selection Register
A10400A4	SW_DBG_OUT	32	MSDC Software Debug Output Register
A10400A8	DMA_LENGTH	32	DMA Length Register
A10400B0	PATCH_BIT0	32	MSDC Patch Bit Register 0
A10400B4	PATCH_BIT1	32	MSDC Patch Bit Register 1
A10400EC	PAD_TUNE	32	MSDC Pad Tuning Register
A10400F0	DAT_RD_DLY0	32	MSDC Data Delay Line Register 0
A10400F4	DAT_RD_DLY1	32	MSDC Data Delay Line Register 1
A10400F8	HW_DBG_SEL	32	MSDC Hardware Debug Selection Register
A1040100	MAIN_VER	32	MSDC Main Version Register
A1040104	ECO_VER	32	MSDC ECO Version Register

A1040000 MSDC_CFG MSDC Configuration Register 00000099

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																CARD_CK_MODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CARD_CK_DIV								CARD_CK_STABLE			CARD_CK_DRV_EN	PIO_MODE	RST	CARD_CK_PWDN	MSDC
Type	RW								RU			RW	RW	A0	RW	RW
Reset	0	0	0	0	0	0	0	0	1			1	1	0	0	1

Bit(s)	Mnemonic	Name	Description
16	CCKMD	CARD_CK_MODE	**MS/SD card clock mode** 1'b0: Use clock divider output where msdc_ ck is divided by msdc_src_ck and program the bits bit[15]~bit[8].

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			1'b1: Use msdc_src_ck as msdc_ck, bit[15]~bit[8] is ignored.
15:8	**CCKDIV**	CARD_CK_DIV	**MS/SD card clock divider** The register field controls clock frequency of serial clock on MS/SD bus. In non-DDR mode, msdc_ck equals SD bus clock. For example, for SDR25 or HS, msdc_ck and SD bus clock will be the same at 50MHz. In DDR mode, msdc_ck is twice the SD bus clock. For example, for DDR50, msdc_ck should be set to 100MHz and bus clock will be 50MHz. 8'b00000000: msdc_ck =(1/2) * msdc_src_ck 8'b00000001: msdc_ck = (1/(4*1)) * msdc_src_ck 8'b00000010: msdc_ck = (1/(4*2)) * msdc_src_ck 8'b00000011: msdc_ck = (1/(4*3))* msdc_src_ck 8'b00010000: msdc_ck = (1/(4*16))* msdc_src_ck 8'b11111111: msdc_ck = (1/(4*255)) * msdc_src_ck
7	**CCKSB**	CARD_CK_STABLE	**MS/SD card clock stability** After programming the CARD_CK_MODE or CARD_CK_DIV, this bit will immediately go to "0" and return to "1", if the clock output is stable. User should poll this register to ensure the safety control of MSDC. 1'b0: Clock output is not stable 1'b1: Clock output is stable
4	**CCKDRVE**	CARD_CK_DRV_EN	**SD/MS Card Bus Clock drive enable bit** Set this bit to 1 to enable MSDC bus clock driver. The default bus state depends on MSDC_CFG[1] CARD_CK_PWDN bit. If MSDC_CFG[1] CARD_CK_PWDN= 1, the default clock is in freerun state. If MSDC_CFG[1] CARD_CK_PWDN = 0, the default clock state is gated to 0. Set this bit to 0 to put the bus state into tri-state. Default is 1. 1'b0: Set the clock pad into tri-state. 1'b1: Enable MSDC to drive the clock pad, the state of CLK depends on MSDC_CFG[1] CARD_CK_PWDN
3	**PIO**	PIO_MODE	**MS/SD PIO mode** PIO mode selection. Default is in PIO mode. 1'b0: DMA mode 1'b1: PIO mode
2	**RST**	RST	**Software reset** Writing 1 to this register will cause internal synchronous reset of MS/SD controller, and it will not reset register settings and DMA controller. The controller resets when this bit is 0. Software should wait for this bit to return to 0 after writing 1. 1'b0: MS/SD controller is not in reset state 1'b1: MS/SD controller is in reset state

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1	**CCKPD**	CARD_CK_PWDN	**MSDC bus clock power down mode** This bit controls the card clock power down mode. 1'b0: Clock is gated to 0, if no command or data is transmitted. 1'b1: Clock is in freerun state even if no command or data is transmitted. The clock may still be stopped when MSDC write data is not enough or there is no space for next read data.
0	**MSDC**	MSDC	**MS/SD mode selection** The register bit is used to configure the controller as the host of a removable storage device or as the host of SD/MMC memory card. The default value is to configure the controller as the host of a removable storage device. 1'b0: Configure the controller as the host of removable storage device. 1'b1: Configure the controller as the host of SD/MMC memory card

A1040004 MSDC_IOCON MSDC IO Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									R_D7_SMPL	R_D6_SMPL	R_D5_SMPL	R_D4_SMPL	R_D3_SMPL	R_D2_SMPL	R_D1_SMPL	R_D0_SMPL
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			W_D3_SMPL	W_D2_SMPL	W_D1_SMPL	W_D0_SMPL	W_D_SMPL_SEL	W_D_SMPL			R_D_SMPL_SEL		D_DLYLINE_SEL	R_D_SMPL	R_SMPL	SDR104_CLK_SEL
Type			RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW
Reset			0	0	0	0	0	0			0		0	0	0	0

Bit(s)	Mnemonic	Name	Description
23	**RD7SPL**	R_D7_SMPL	**Read data 7 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
22	**RD6SPL**	R_D6_SMPL	**Read data 6 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
21	**RD5SPL**	R_D5_SMPL	**Read data 5 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising

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			edge 1'b1: Sample read data by external bus clock falling edge
20	**RD4SPL**	R_D4_SMPL	**Read data 4 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
19	**RD3SPL**	R_D3_SMPL	**Read data 3 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
18	**RD2SPL**	R_D2_SMPL	**Read data 2 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
17	**RD1SPL**	R_D1_SMPL	**Read data 1 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
16	**RD0SPL**	R_D0_SMPL	**Read data 0 sample selection** This bit is only valid when bit 5 is ON 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
13	**WD3SPL**	W_D3_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
12	**WD2SPL**	W_D2_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
11	**WD1SPL**	W_D1_SMPL	**SDIO interrupt sample selection** This bit is only valid when bit 9 is ON

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			1'b0: Sample SDIO interrupt by external bus clock rising edge 1'b1: Sample SDIO interrupt by external bus clock falling edge
10	**WD0SPL**	W_D0_SMPL	**CRC Status and SDIO interrupt sample selection** This bit is only valid when bit 9 is ON 1'b0: Sample CRC Status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC Status and SDIO interrupt by external bus clock falling edge
9	**WDSPLSEL**	W_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in write transaction** 1'b0: All data lines share the same value indicated by MSDC_IOCON.W_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.W_D0_SMPL Data line 1: MSDC_IOCON.W_D1_SMPL Data line 2: MSDC_IOCON.W_D2_SMPL Data line 3: MSDC_IOCON.W_D3_SMPL
8	**WDSPL**	W_D_SMPL	**CRC Status and SDIO interrupt sample selection** 1'b0: Sample CRC status and SDIO interrupt by external bus clock rising edge 1'b1: Sample CRC status and SDIO interrupt by external bus clock falling edge
5	**RDSPLSEL**	R_D_SMPL_SEL	**Data line rising/falling latch fine tune selection in read transaction** 1'b0: All data lines share the same value indicated by MSDC_IOCON.R_D_SMPL 1'b1: Each data line has its own selection value indicated by Data line 0: MSDC_IOCON.R_D0_SMPL Data line 1: MSDC_IOCON.R_D1_SMPL Data line 2: MSDC_IOCON.R_D2_SMPL Data line 3: MSDC_IOCON.R_D3_SMPL Data line 4: MSDC_IOCON.R_D4_SMPL Data line 5: MSDC_IOCON.R_D5_SMPL Data line 6: MSDC_IOCON.R_D6_SMPL Data line 7: MSDC_IOCON.R_D7_SMPL
3	**DDLSEL**	D_DLYLINE_SEL	**Data line delay line fine tune selection** 1'b0: All data lines share the same delay selection value indicated by PAD_TUNE.PAD_DAT_RD_RXDLY 1'b1: Each data line has its own delay selection value indicated by

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			Data line 0: DAT_RD_DLY0.DAT0_RD_DLY Data line 1: DAT_RD_DLY0.DAT1_RD_DLY Data line 2: DAT_RD_DLY0.DAT2_RD_DLY Data line 3: DAT_RD_DLY0.DAT3_RD_DLY Data line 4: DAT_RD_DLY1.DAT4_RD_DLY Data line 5: DAT_RD_DLY1.DAT5_RD_DLY Data line 6: DAT_RD_DLY1.DAT6_RD_DLY Data line 7: DAT_RD_DLY1.DAT7_RD_DLY
2	**RDSPL**	R_D_SMPL	**Read data sample selection** 1'b0: Sample read data by external bus clock rising edge 1'b1: Sample read data by external bus clock falling edge
1	**RSPL**	R_SMPL	**Command response sample selection** 1'b0: Sample response by external bus clock rising edge 1'b1: Sample response by external bus clock falling edge
0	**SDR104CKS**	SDR104_CLK_SEL	**SDR104 SCLK output clock control** This bit is only used when MSDC_CFG[17:16] CARD_CK_MODE is 2'b01. 1'b0: Bus clock output equals inverted msdc_src_ck 1'b1: Bus clock output equals msdc_src_ck

A1040008 MSDC_PS MSDC Pin Status Register 81FF0002

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SD_WP							CMD	DAT							
Type	RU							RU	RU							
Reset	1							1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved														CDSTS	CDEN
Type	RW														RU	RW
Reset	0	0	0	0											1	0

Bit(s)	Mnemonic	Name	Description
31	**SDWP**	SD_WP	**Write protection switch status on SD memory card** The register bit shows the status of the write protection switch on the SD memory card. There is no default reset value. The write protection pin is only used when the controller is configured for the SD memory card. 1'b0: Write protection switch is ON. It means that memory card is write-protected. 1'b1: Write protection Switch is OFF. It means that memory card is writable.
24	**CMD**	CMD	**Command line status** This bit reflects the command line value of the MSDC

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			bus.
23:16	**DAT**	DAT	**Data line status** This bit reflects the data line value of MSDC bus (8-bits).
15:12		Reserved	
1	**CDSTS**	CDSTS	**Card detection status** 1'b0: Card detection pin status is logic low 1'b1: Card detection pin status is logic high
0	**CDEN**	CDEN	**Card detect enable** The register bit is used to control the card detection circuit. 1'b0: Card detection is disabled 1'b1: Card detection is enabled

A104000C MSDC_INT MSDC Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													DMA_PROTECT	GPD_CS_ERR	BD_CS_ERR	
Type													W1C	W1C	W1C	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SD_DATA_CRCERR	SD_DATTO	DMA_XFER_DONE	SD_XFER_COMPLETE	SD_CSTA	SD_RESP_CRCERR	SD_CMDTO	SD_CMDRDY	SD_SDIOIRQ	DMA_Q_EMPTY	SD_AUTOCMD_RESP_CRCERR	SD_AUTOCMD_CMDTO	SD_AUTOCMD_CMDRDY		MSDC_CDSC	MMC_IRQ
Type	W1C	W1C	W1C	W1C	RU	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C		W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**DMAPROTECT**	DMA_PROTECT	**This register identifies if there is a write operation to the DMA start address, length, start bit or last buffer bit.**
18	**GPDCSERR**	GPD_CS_ERR	**GPD checksum error detected**
17	**BDCSERR**	BD_CS_ERR	**BD checksum error detected**
15	**SDDCRCERR**	SD_DATA_CRCERR	**SD Data CRC error interrupt** Indicates that MS/SD controller detects a CRC error after reading a block of data from the DAT line or SD/MMC signals a CRC error after writing a block of data to the DAT line. 1'b0: Otherwise 1'b1: MS/SD controller detected a CRC error after reading a block of data from the DAT line or SD/MMC signaled a CRC error after writing a block of data to the DAT line
14	**SDDTO**	SD_DATTO	**SD data timeout interrupt**

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			Indicates that SD/MMC controller detects a timeout condition while waiting for data token on the DAT line. This bit is for both data read and data write. For SD data read, timeout will occur when the read data is not presented. For SD data write, timeout will occur when the write data CRC status is not presented if PATCH_BIT[30] DETECT_WR_CRC_TIMEOUT = 1 1'b0: Otherwise 1'b1: SD/MMC controller detects a timeout condition while waiting for data token on the DAT line
13	**DMAXFDNE**	DMA_XFER_DONE	**DMA transfer done interrupt** The register bit indicates the status of data block transfer. 1'b0: Otherwise 1'b1: A data block was successfully transferred
12	**SDXFCPL**	SD_XFER_COMPLETE	**SD Data transfer complete interrupt** This bit indicates the transaction is complete. While performing tuning procedure (execute tuning is set to 1), SD_XFER_COMPLETE is not set to 1.
11	**SDCSTA**	SD_CSTA	**SD CSTA update interrupt** This register bit indicates if any bit in the register SDC_CSTA is active, this bit will be set to 1. Software should clear the SDC_CSTA and this bit will be de-asserted automatically. 1'b0: No SD memory card interrupt 1'b1: SD memory card interrupt exists
10	**SDRCRCER**	SD_RESP_CRCERR	**SD Command CRC error interrupt** Indicates that SD/MMC controller detected a CRC error after reading a response from the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a CRC error after reading a response from the CMD line
9	**SDCTO**	SD_CMDTO	**SD Command timeout interrupt** Indicates that SD/MMC controller detected a timeout while waiting for a response on the CMD line. 1'b0: Otherwise 1'b1: SD/MMC controller detected a timeout condition while waiting for a response on the CMD line
8	**SDCRDY**	SD_CMDRDY	**SD Command ready interrupt** For the command without response, the register bit will be 1 once the command is complete on SD/MMC bus. For a command with response without busy, the register bit will be 1 whenever the command is issued onto SD/MMC bus and its corresponding response is received without CRC error. For a command with response with busy in DAT0, the register bit will be 1 whenever the command is issued

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			onto SD/MMC bus and its corresponding response is received without CRC error and the DAT0 transited from busy to idle. 1'b0: Otherwise 1'b1: Command finished successfully without a CRC error
7	**SDIOIRQ**	SD_SDIOIRQ	**SD SDIO interrupt** This bit indicates an interrupt occurred in the SDIO bus. 1'b0: No interrupt on SDIO bus 1'b1: Interrupt on SDIO bus
6	**DMAQEPTY**	DMA_Q_EMPTY	**DMA queue empty interrupt** This bit is used to indicate that the current DMA queue is empty. Only for Descriptor mode and Enhanced mode.
5	**SDACDRCRCER**	SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt** This bit is set when detecting a CRC error in the auto command response.
4	**SDACDCTO**	SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt** This bit is set if no response is returned within a specified cycle (64 clock cycles in the specification) from the end bit of auto command.
3	**SDACDCRDY**	SD_AUTOCMD_CMDRDY	**SD auto command ready interrupt** This bit is set if auto command is executed without CRC error or time out.
1	**MSDCCDSC**	MSDC_CDSC	**MSDC Card detection status change interrupt** The register bit indicates if any interrupt for memory card insertion/removal exists. Whenever memory card is inserted or removed and card detection circuit is enabled, i.e., the register bit CDEN in the register MSDC_PS is set to 1, the register bit will be set to 1. It will be reset when the register is read. 1'b0: Otherwise 1'b1: Card is inserted or removed
0	**MMCIRQ**	MMC_IRQ	**MMC card interrupt** 1'b0: Otherwise 1'b1: Indicates that MMC card interrupt event occurred

A1040010 **MSDC_INTEN** **MSDC Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													EN_DMA_PROTECT	EN_GPD_CS_ERR	EN_BD_CS_ERR	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EN_SD_	EN_SD_	EN_SD_	EN_SD_	EN_SD_	EN_SD_	EN_SD_	EN_SD_	EN_SD_S	EN_DMA	EN_SD_	EN_SD_	EN_AUT		EN_MSD	EN_MMC

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	DATA_CRCERR	DATTO	DMA_XFER_DONE	XFER_COMPLETE	CSTA	RESP_CRCERR	CMDTO	CMDRDY	DIOIRQ	_Q_EMPTY	AUTOCMD_RESP_CRCERR	AUTOCMD_CMDTO	OCMD_CMDRDY		C_CDSC	_IRQ
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
19	**ENDMAPROTECT**	EN_DMA_PROTECT	**DMA protection interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
18	**ENGPDCSERR**	EN_GPD_CS_ERR	**GPD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
17	**ENBDCSERR**	EN_BD_CS_ERR	**BD checksum error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
15	**ENSDDCRCERR**	EN_SD_DATA_CRCERR	**SD Data CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
14	**ENSDDTO**	EN_SD_DATTO	**SD Data timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
13	**ENDMAXFDNE**	EN_SD_DMA_XFER_DONE	**DMA transfer done interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
12	**ENSDXFCPL**	EN_SD_XFER_COMPLETE	**SD Data transfer complete interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
11	**ENSDCSTA**	EN_SD_CSTA	**SD CSTA update interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
10	**ENSDRCRCER**	EN_SD_RESP_CRCERR	**SD Command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
9	**ENSDCTO**	EN_SD_CMDTO	**SD Command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
8	**ENSDCRDY**	EN_SD_CMDRDY	**SD Command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
7	**ENSDIOIRQ**	EN_SD_SDIOIRQ	**SD SDIO interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
6	**ENDMAQEPTY**	EN_DMA_Q_EMPTY	**DMA queue empty interrupt enable**

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			1'b0: Disable interrupt 1'b1: Enable interrupt
5	**ENSDACDRCRCER**	EN_SD_AUTOCMD_RESP_CRCERR	**SD auto command CRC error interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
4	**ENSDACDCTO**	EN_SD_AUTOCMD_CMDTO	**SD auto command timeout interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
3	**ENSDACDCRDY**	EN_AUTOCMD_CMDRDY	**SD auto command ready interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
1	**ENMSDCCDSC**	EN_MSDC_CDSC	**MSDC Card detection status change interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt
0	**ENMMCIRQ**	EN_MMC_IRQ	**MMC card interrupt enable** 1'b0: Disable interrupt 1'b1: Enable interrupt

A1040014 MSDC_FIFOCS MSDC FIFO Control and Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FIFO CLR								TXFIFOCNT							
Type	A0								RU							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									RXFIFOCNT							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31	**FIFOCLR**	FIFOCLR	**Embedded FIFO clear** Write 1 into this bit to clear the FIFO. It returns to 0 when FIFO is cleared. Software needs to check this bit to make sure clearing FIFO sequence is done. This bit can be used when the data read/write sequence has an error.
23:16	**TXFIFOCNT**	TXFIFOCNT	**TX FIFO count for MSDC write** 8'd0: No data in FIFO 8'd1: 1 byte data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved
7:0	**RXFIFOCNT**	RXFIFOCNT	**RX FIFO count for MSDC read**

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	8'd0: No data in FIFO 8'd1: 1 byte data in FIFO 8'd2: 2 bytes data in FIFO 8'd131: Maximum 131 bytes data in FIFO Others: reserved

A1040018 MSDC_TXDATA MSDC TX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_TXDATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIOTXDATA**	PIO_TXDATA	**PIO mode TXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

A104001C MSDC_RXDATA MSDC RX Data Port Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PIO_RXDATA															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PIORXDATA**	PIO_RXDATA	**PIO mode RXDATA port** This register can be accessed by byte, half-word or word. This port can only be accessed in PIO mode. Otherwise, the transaction will be discarded.

A1040030 SDC_CFG SD Configuration Register 00100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DTOC										INT_AT_BLOCK_GAP	SDIO_INT_DET_EN	SDIO		BUSWIDTH	
Type	RW										RW	RW	RW		RW	
Reset	0	0	0	0	0	0	0	0			0	1	0		0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WAKEUP_INS	WAKEUP_SDI

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															_EN	OINT_EN
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31:24	**DTOC**	DTOC	**Data Timeout Counter** The period from the end of initial host read command or the last read data block in a multiple block read operation to the start bit of next read data block requires at least two serial clock cycles. The counter is used to extend the period (Read Data Access Time) in unit of 1048576 serial clocks. 8'b00000000: Extend 1048576 more serial clock cycles 8'b00000001: Extend 1048576 x 2 more serial clock cycles 8'b00000010: Extend 1048576 x 3 more serial clock cycles 8'b11111111: Extend 1048576 x 256 more serial clock cycles
21	**INTBGP**	INT_AT_BLOCK_GAP	**Interrupt at block gap** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. Setting to 0 disables interrupt detection during a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the Host Driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. 1'b0: Disable interrupt detection at the block gap 1'b1: Enable interrupt detection at the block gap
20	**SDIOIDE**	SDIO_INT_DET_EN	**SDIO interrupt detection enable** This bit is to inform the SD controller to sense the SDIO interrupt 1'b0: SDIO interrupt detection is disabled 1'b1: SDIO interrupt detection is enabled if the SDIO bit is also on
19	**SDIO**	SDIO	**SDIO mode enable bit** This bit is to enable the support to sense the SDIO interrupt and disable the R4 response CRC check for SDIO card 1'b0: SDIO mode is disabled 1'b1: SDIO mode is enabled
17:16	**BUSWD**	BUSWIDTH	**Bus width configuration** This field is used to define the SD/MMC bus width 2'b00: 1 bit mode

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			2'b01: 4 bit mode 2'b10: 8 bit mode 2'b11: reserved
1	**ENWKUPINS**	WAKEUP_INS_EN	**Card status change wakeup event enable bit** 1'b0: Disable wakeup event for card status change 1'b1: Enable wakeup event for card status change
0	**ENWKUPSDIOINT**	WAKEUP_SDIOINT_EN	**SDIO card interrupt wakeup event enable bit** 1'b0: Disable wakeup event for SDIO card interrupt 1'b1: Enable wakeup event for SDIO card interrupt

A1040034 SDC_CMD SD Command Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				AUTO_CMD	LEN											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GO_IRQ	STOP	RW	DTYPE			RSPTYP			BREAK	CMD					
Type	RW	RW	RW	RW			RW			RW	RW					
Reset	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28	**ACMD**	AUTO_CMD	**Auto command enable** This field determines use of auto command functions. This function can be used in all modes including PIO/Basic DMA/Descriptor DMA/Enhanced Mode. There are two methods to stop multiple-block read and write operation. (1) Auto CMD12 Enable Multiple-block read and write commands for memory require CMD12 to stop the operation. When ACMD-12 is used, MSDC issues CMD12 automatically when last block transfer completes. Auto CMD12 error is indicated to the MSDC_INT register. The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12. (2) Auto CMD23 Enable When ACMD-23 is used, MSDC issues a CMD23 automatically before issuing a command specified in the CMD field. The Host Controller Version 3.00 and later shall support this function. By writing the Command register, MSDC issues a CMD23 first and then issues a command specified by the CMD field in SDC_CMD register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the MSDC_INT register. 32-bit

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			block count value for CMD23 is set to SDC_BLOCK_NUM register. 1'b0: Disable Auto Command 1'b1: Enable Auto CMD12
27:16	**LEN**	LEN	**Length** The register field is used to define the length of one block in unit of byte in a data transaction of block mode or the data length in unit of byte in data transaction of byte mode. The maximal value of block length is 2048 bytes. 12'b000000000000: Reserved 12'b000000000001: Block length is 1 byte 12'b000000000010: Block length is 2 byte 12'b011111111111: Block length is 2047 byte 12'b100000000000: Block length is 2048 byte
15	**GOIRQ**	GO_IRQ	**GO_IRQ command** The register bit indicates if the command is GO_IRQ_STATE (CMD40) and used only for MMC protocol. If the command is GO_IRQ_STATE, the period between command token and response token will not be limited. 1'b0: The command is not GO_IRQ_STATE 1'b1: The command is GO_IRQ_STATE
14	**STOP**	STOP	**Stop command** The register bit indicates if the command is a stop transmission command. It should be set to 1 when CMD12 (SD/MMC) or CMD52 with I/O abort (SDIO) is to be issued. 1'b0: The command is not a stop transmission command 1'b1: The command is a stop transmission command
13	**RW**	RW	**Command read write selection** The register bit defines if the command is a read command or write command. The register bit is valid only when the command will cause a transaction with data token. 1'b0: The command is a read command 1'b1: The command is a write command
12:11	**DTYPE**	DTYPE	**Data block selection** The register field defines data token type for the command. 2'b00: No data token for the command 2'b01: Single block transaction (only available in block mode) 2'b10: Multiple block transaction (only available in block mode) 2'b11: Stream operation. It shall only be used in MMC

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			protocol. (only available in block mode)
9:7	**RSPTYP**	RSPTYP	**Command response type** 3'b000: This command has no response. 3'b001: The command has R1/R5/R6/R7 response. The response token is 48-bit with CRC check (For SD/MMC/SDIO) (Not including the SDIO abort command) 3'b010: The command has R2 response. The response token is 136-bit (For SD/MMC) 3'b011: The command has R3 response. The response token is 48-bit response, no CRC check (For SD/MMC) 3'b100: The command has R4 response. The response token is 48-bit without CRC check (For SDIO) The response token is 48-bit with CRC check (For MMC) 3'b111: The command has R1b response. The response token is 48-bit (For SD/MMC/SDIO)
6	**BREAK**	BREAK	**Abort a pending MMC GO_IRQ command** It is only valid for a pending GO_IRQ_MODE command waiting for MMC interrupt response. 1'b0: Not a break command 1'b1: Break a pending MMC GO_IRQ_MODE command in the controller.
5:0	**CMD**	CMD	**SD Memory Card command**

A1040038 SDC_ARG SD Argument Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ARG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	ARG	ARG	Memory card controller argument register

A104003C SDC_STS SD Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MMC_STREAM_WR_COMPL															CMD_WR_BUSY
Type	RU															W1C
Reset	0															0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CMD BUS	SDC BUS

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															Y	Y
Type															RU	RU
Reset															0	0

Bit(s)	Mnemonic	Name	Description
31	**MMCSWRCPL**	MMC_STREAM_WR_COMPL	**MMC Stream mode write data is all flushed to MMC card** Software can use this bit to confirm last write data are flushed to MMC then issue a STOP command. This bit is only valid when the command SDC_CMD.DTYPE=2'b11. 1'b0: Last Data are partially inside MSDC 1'b1: Last data are flushed to MMC card
16		CMD_WR_BUSY	
1	**CMDBSY**	CMDBUSY	**SD Command line busy status** Software should always read this bit to make sure the command line is not busy before sending the next command. If the command is R1B or data read/write command, Software should check the SDCBUSY bit, too. Note: When auto command 12 is enabled, this bit will be asserted immediately after SDC_CMD is written and de-asserted after auto command 12 finishes. 1'b0: No transmission in the CMD line on SD bus 1'b1: There is transmission in the CMD line on SD bus
0	**SDCBSY**	SDCBUSY	**SD controller busy status** 1'b0: SD controller is idle 1'b1: SD controller is busy

A1040040 SDC_RESP0 SD Response Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**RESP0**	RESP0	**Memory card controller response register 0**

A1040044 SDC_RESP1 SD Response Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESP1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESP1															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RESP1	RESP1	Memory card controller response register 1

A1040048 SDC_RESP2 SD Response Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESP2**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP2**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RESP2	RESP2	Memory card controller response register 2

A104004C SDC_RESP3 SD Response Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESP3**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESP3**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	RESP3	RESP3	Memory card controller response register 3

A1040050 SDC_BLK_NUM SD Block Number Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BLOCK_NUMBER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BLOCK_NUMBER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**BLKNUM**	BLOCK_NUMBER	**Memory card controller block number** This field indicates the block number of data transaction. 32'd0: Reserved 32'd1: 1 data block 32'd2: 2 data blocks

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	32'd3: 3 data blocks 32'hffffffff: 4GB-1 data blocks

A1040058 SDC_CSTS SD Card Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS**	CSTS	The register provides SD/MMC card status in the response R1 or R1b field. 32'h0: keep the current value Others: write 1 to each bit to clear the corresponding bit.

A104005C SDC_CSTS_EN SD Card Status Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CSTS_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CSTS_EN**	CSTS_EN	This register is used to control the CSTA bit that will generate MSDC_INT.SDCSTA

A1040060 SDC_DATCRC_STS SD Card Data CRC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DAT_CRCSTS_POS							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**DCSSP**	DAT_CRCSTS_POS	**MSDC read DATA CRC status** This register reflects the CRC status of data lines[7:0]. This register is only for MSDC Read.

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	1'b0: No CRC error 1'b1: CRC error

A1040080 SD_ACMD_RESP SD Auto Command Response Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AUTOCMD_RESP															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ACMDRESP**	AUTOCMD_RESP	**SD Auto command response register** This register stores the response [39:8] of ACMD12/ACMD23/ACMD19.

A1040090 DMA_SA DMA Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_STR_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMASA**	DMA_STR_ADDR	**The start address of the DMA address** This register is used to set the start address of the DMA. In DMA basic mode, this field indicates the source or destination address of the data transfer, which depends on the command. In Descriptor DMA mode, this is the descriptor chain start address.

A1040094 DMA_CA DMA Current Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DMA_CURR_ADDR															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**DMACA**	DMA_CURR_ADDR	**The current address of the DMA address** This register is used to read the current address of the DMA descriptor chain.

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A1040098 DMA_CTRL DMA Control Register 00006000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		BURST_SIZE			DMA_SPLIT_1K	LAST_BUF	DMA_ALIGN	DMA_MODE						DMA_RESUME	DMA_STOP	DMA_START
Type		RW			RW	RW	RW	RW						WO	A0	WO
Reset		1	1	0	0	0	0	0						0	0	0

Bit(s)	Mnemonic	Name	Description
14:12	**BSTSZ**	BURST_SIZE	**DMA burst size** This field is used to specify the maximum transfer bytes allowed at the device per DMA burst. This field cannot be modified when the DMA status is 1. 3'd3: 8 Bytes 3'd4: 16 Bytes 3'd5: 32 Bytes 3'd6: 64 Bytes Other: Reserved
11	**SPLIT1K**	DMA_SPLIT_1K	**This field is used to specify whether to split burst when it crosses the 1K address boundary** 1'b0:1K boundary not split 1'b1:1K boundary split
10	**LASTBF**	LAST_BUF	**Last buffer of the basic DMA mode** This field indicates the last buffer in the basic DMA mode
9	**DMAALIGN**	DMA_ALIGN	**This field is used to specify whether there is address alignment burst size** 1'b0:No DMA burst size alignment 1'b1:DMA burst size alignment
8	**DMAMOD**	DMA_MODE	**DMA operation mode** This field indicates the operation mode of DMA 1'b0: Basic DMA mode 1'b1: Descriptor base DMA mode
2	**DMARSM**	DMA_RESUME	**DMA resume control register** This bit is used to resume the DMA transaction. Read always returns 0
1	**DMASTOP**	DMA_STOP	**DMA Stop control register** This bit is used to stop the DMA transaction. When software issues STOP command, it must wait for this bit to de-assert or inactivate the DMA to guarantee a complete stop.
0	**DMASTART**	DMA_START	**DMA start control register** This bit is used to start the DMA transaction. Read

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	always returns 0

A104009C DMA_CFG DMA Configuration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																DMA_CHK_SUM_12B
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MSDC_ACTIVE_EN				AHB_HPROT_2_EN								DMA_DSCP_CS_EN	DMA_STATUS
Type			RW				RW								RW	RU
Reset			0	0			0	0							0	0

Bit(s)	Mnemonic	Name	Description
16	**DMACHKSUM12B**	DMA_CHK_SUM_12B	**This register indicates GPD/BD checksum length is 16bytes or 12bytes** 1'b0: GPD/BD checksum cover 16byte 1'b1: GPD/BD checksum only cover 12byte
13:12	**MSDCACTIVEEN**	MSDC_ACTIVE_EN	**This register indicates how to control msdc_active** 2'b00: dynamic control msdc_active 2'b01: msdc_active = 0 2'b10: msdc_active = 1 2'b11: Reserved
9:8	**AHBHPROT2EN**	AHB_HPROT_2_EN	**This register determines how to control hprot_2 pin of AHB bus** AHB_HPROT_2_EN = 2'b00, and Basic DMA Mode, all write transfers of a burst are accessed in bufferable mode except the last DMA burst AHB_HPROT2_2_EN=2'b00, and Descriptor DMA Mode, all write transfers of a burst are accessed in bufferable mode except the hardware's own update transfer. 2'b00: dynamic control hprot_2 2'b01: hprot_2 = 0 2'b10: hprot_2 = 1
1	**DSCPCSEN**	DMA_DSCP_CS_EN	**DMA descriptor checksum enable** This bit is used to enable or disable the checksum validation function for the descriptor. This field cannot be modified when the DMA status is 1.
0	**DMASTS**	DMA_STATUS	**DMA status** This bit is used to indicate the status of the DMA. 1'b0: DMA engine is inactive 1'b1: DMA engine is active

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A10400A0 SW_DBG_SEL MSDC S/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_SEL															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SWDBGSEL**	DBG_SEL	**MSDC debug selection** Reserved

A10400A4 SW_DBG_OUT MSDC S/W Debug Output Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_OUT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SWDBGO**	DBG_OUT	**MSDC debug output** 32 bit output selected by SW_DBG_SEL register

A10400A8 DMA_LENGTH DMA Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**XFSZ**	XFER_SIZE	**DMA total transfer size** This field is used to specify the number of DMA transfer bytes. This field is only valid in basic DMA mode.

A10400B0 PATCH_BIT0 MSDC Patch Bit Register 0 403C004F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EN_MMC_DRV	DETECT_WR_	SPC_ALWAYS_	SDIO_INT_DLY	SDC_CMD_CM	SDC_CMD_IDR	SDC_CFG_WDOD				SDC_CFG_BSYDLY				SDIO_CFG_INT	

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	_RESP	CRC_TIMEOUT	PUSH	_SEL	DFAIL_SEL	T_SEL									C_SEL	
Type	RW	RW	RW	RW	RW	RW	RW				RW				RW	
Reset	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSDC_FIFO_RD_DIS						INT_DAT_LATCH_CK_SEL			reserved1				DIS_REFLECT_CMDWR_WHEN_BSY	EN_SDC_ODD_8BIT_SUP	reserved0
Type	RW						RW			RW				RW	RW	RW
Reset	0						0	0	0	1	0	0	1	1	1	1

Bit(s)	Mnemonic	Name	Description
31	**PTCH31**	EN_MMC_DRV_RESP	**Enable MSDC always drives the bus, when the output is a wakeup response, such as BREAK.** 1'b0: Disable 1'b1: Enable
30	**PTCH30**	DETECT_WR_CRC_TIMEOUT	**MSDC write data CRC phase timeout detection** 1'b0: Does not detect CRC phase timeout 1'b1: Detects CRC phase timeout
29	**PTCH29**	SPC_ALWAYS_PUSH	**SPC Buffer push mechanism** 1'b0: Push the buffer only when read transfer is on-going 1'b1: Always push the buffer
28	**PTCH28**	SDIO_INT_DLY_SEL	**SDIO interrupt latch time selection** 1'b0: Latch the data line value in internal SDIO interrupt period 1'b1: Latch the data line value in 1 clock delay of internal SDIO interrupt period
27	**PTCH27**	SDC_CMD_CMDFAIL_SEL	**SDIO interrupt period recovery selection** 1'b0: SDIO interrupt period will re-start after a CMD12 or CMD52 command is issued 1'b1: SDIO interrupt period whenever DAT line is not busy
26	**PTCH26**	SDC_CMD_IDRT_SEL	**SD identification response time selection** The register bit indicates if the command has a response with NID (that is, 5 serial clock cycles as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 1.0) response time. The register bit is valid only when the command has a response token. Thus, the register bit must be set to 1 for CMD2 (ALL_SEND_CID) and ACMD41 (SD_APP_OP_CMD). 1'b0: Otherwise.

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			1'b1: The command has a response with NID response time.
25:22	**PTCH22**	SDC_CFG_WDOD	**SD Write Data Output Delay** The period from response finish for the initial host write command or the last write data block in a multiple block write operation to the start bit of the next write data block requires at least two serial clock cycles. The register field is used to extend the period (Write Data Output Delay) in the unit of one serial clock. 4'b0000: Not extended. 4'b0001: Extended by one more serial clock cycle. 4'b0010: Extended by two more serial clock cycles. 4'b1111: Extended by fifteen more serial clock cycles.
21:18	**PTCH18**	SDC_CFG_BSYDLY	**SD R1B busy detection mode** The register field is only valid for the commands with R1b response. If the command has a response of R1b type, MS/SD controller must monitor the data line 0 for card busy status from the bit time that is two serial clock cycles after the command end bit to check if operations in SD/MMC Memory Card have finished. The register field is used to expand the time between the command end bit and end of detection period to detect card busy status. If time is up and there is no card busy status on data line 0, then the controller will abandon the detection. 4'b0000: Not extended. 4'b0001: Extended by one more serial clock cycle. 4'b0010: Extended by two more serial clock cycles. 4'b1111: Extended by fifteen more serial clock cycles.
17	**PTCH17**	SDIO_CFG_INTC_SEL	**SDIO Interrupt model selection** 1'b0: Only when data line [1] = 0 and then trigger SDIO interrupt event 1'b1: Only when data line [3:0] = 4'b1101 and then trigger SDIO interrupt event
15	**PTCH15**	MSDC_FIFO_RD_DIS	**MSDC RXFIFO Read Disable** 1'b0: Disable FIFO read permission to RXFIFO in PIO mode 1'b1: Enable FIFO read permission to RXFIFO in PIO mode
9:7	**INTCKS**	INT_DAT_LATCH_CK_SEL	**Internal MSDC clock phase selection** Total 8 stages, each stage can delay 1 clock period of msdc_src_ck

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6:3		reserved1	
2	**PTCH02**	DIS_REFLECT_CMDWR_WHEN_BSY	**Enable SD command register write monitor** 1'b0: Enable monitor function 1'b1: Disable monitor function
1	**PTCH01**	EN_SDC_ODD_8BIT_SUP	**Enable SD odd number support for 8-bit data bus** 1'b0: Disable 1'b1: Enable
0		reserved0	

A10400B4 PATCH_BIT1 MSDC Patch Bit Register 1 FFFE0009

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MSDC_CK_SHBFF_CKEN	MSDC_CK_RCTL_CKEN	MSDC_CK_WCTL_CKEN	MSDC_CK_SD_CKEN	MSDC_CK_ACMD_CKEN	MSDC_CK_VOLDET_CKEN	MSDC_CK_PSC_CKEN	MSDC_CK_SPC_CKEN	AHB_CK_GDMA_CKEN	reserved2						ENABLE_SINGLE_BURST
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW						RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			BIAS_EXTBIAS_28NM	BIAS_EN18IO_28NM	BIAS_TUNE_28NM				GET_CRC_MARGIN	GET_BUSY_MARGIN	CMD_RSP_TA_CNTR			WRDAT_CRCS_TA_CNTR		
Type			RW	RW	RW				RW	RW	RW			RW		
Reset			0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit(s)	Mnemonic	Name	Description
31	**MSHBFCKEN**	MSDC_CK_SHBFF_CKEN	**msdc_src_ck clock enable bit for SHBFF** 1'b0: Disable 1'b1: Enable
30	**MRCTLCKEN**	MSDC_CK_RCTL_CKEN	**msdc_src_ck clock enable bit for RCTL** 1'b0: Disable 1'b1: Enable
29	**MWCTLCKEN**	MSDC_CK_WCTL_CKEN	**msdc_src_ck clock enable bit for WCTL** 1'b0: Disable 1'b1: Enable
28	**MSDCKEN**	MSDC_CK_SD_CKEN	**msdc_src_ck clock enable bit for SD** 1'b0: Disable 1'b1: Enable
27	**MACMDCKEN**	MSDC_CK_ACMD_CKEN	**msdc_src_ck clock enable bit for ACMD** 1'b0: Disable 1'b1: Enable
26	**MVOLDTCKEN**	MSDC_CK_VOLDET_CKEN	**msdc_src_ck clock enable bit for VOLDET** 1'b0: Disable

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			1'b1: Enable
25	**MPSCCKEN**	MSDC_CK_PSC_CKEN	**msdc_src_ck clock enable bit for PSC** 1'b0: Disable 1'b1: Enable
24	**MSPCCKEN**	MSDC_CK_SPC_CKEN	**msdc_src_ck clock enable bit for SPC** 1'b0: Disable 1'b1: Enable
23	**HGDMACKEN**	AHB_CK_GDMA_CKEN	**hclk_ck clock enable bit for GDMA** 1'b0: Disable 1'b1: Enable
22:17		reserved2	
16	**SINGLEBURST**	ENABLE_SINGLE_BURST	**The AHB bus will not support incr1 burst type, it only supports the single burst type. It will only affect the AHB bus MSDC design, but not the AXI bus design** 1'b0:hardware will send incr1 burst type 1'b1: hardware will send single burst type instead of incr1 type
13	**BIAS28R0**	BIAS_EXTBIAS_28NM	**28NM BIAS Controller register 0**
12	**BIAS28R1**	BIAS_EN18IO_28NM	**28NM BIAS Controller register 1**
11:8	**BIAS28R2**	BIAS_TUNE_28NM	**28NM BIAS Controller register 2**
7	**GETCRCMARGIN**	GET_CRC_MARGIN	**This will add margin to get the CRC status when the card response CRC does not match with the 2 cycles (described in the SD specification) starting from the end bit** 1'b0: 8 cycles are reserved to get the CRC status from write data CRC end bit 1'b1: 16 cycles reserved for getting CRC status from write data CRC end bit
6	**GETBUSYMARGIN**	GET_BUSY_MARGIN	**This will add margin for the get busy state of data0** 1'b0: 1 cycle reserved for get busy state from SRC status end bit 1'b1: 3 cycles reserved for get busy state from SRC status end bit
5:3	**CMDTA**	CMD_RSP_TA_CNTR	**CMD response turnaround period** The turnaround cycle = CMD_RSP_TA_CNTR + 2 is only for USH104 mode, this register should be set to 0 in non-UHS104 mode
2:0	**WRTA**	WRDAT_CRCS_TA_CNTR	**Write data and CRC status turnaround period** The turnaround cycle = WRDAT_CRCS_TA_CNTR + 2 is only for USH104 mode, this register should be set to 0 in non-UHS104 mode

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A10400EC PAD_TUNE MSDC Pad Tuning Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PAD_CLK_TXDLY					PAD_CMD_RESP_RXDLY					PAD_CMD_RD_RXDLY_SEL	PAD_CMD_RXDLY				
Type	RW					RW					RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PAD_DAT_RD_RXDLY_SEL	PAD_DAT_RD_RXDLY					DELAY_EN			PAD_DAT_WR_RXDLY				
Type			RW	RW					RW			RW				
Reset			0	0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:27	**CLKTDLY**	PAD_CLK_TXDLY	**CLK Pad TX Delay Control** This register is used to add delay to CLK phase. Total 32 stages
26:22	**CMDRRDLY**	PAD_CMD_RESP_RXDLY	**CMD Response Internal Delay Line Control** This register is used to fine-tune response phase latched by MSDC internal clock Total 32 stages
21	**CMDRRDLYSEL**	PAD_CMD_RD_RXDLY_SEL	**Determines, if CMD Response passes through data delay line1 or not** 1'b0: pass 1'b1: do not pass
20:16	**CMDRDLY**	PAD_CMD_RXDLY	**CMD Pad RX Delay Line Control** This register is used to fine-tune CMD pad macro response latch timing Total 32 stages
13	**DATRRDLYSEL**	PAD_DAT_RD_RXDLY_SEL	**Determines, if RX data passes through data delay line1 or not** 1'b0: pass 1'b1: do not pass
12:8	**DATRRDLY**	PAD_DAT_RD_RXDLY	**DAT Pad RX Delay Line Control (for MSDC read only)** This register is used to fine-tune DAT pad macro read data latch timing Total 32 stages
7	**DELAYEN**	DELAY_EN	**Enable all delay cell toggling when powered on** 1'b0: disable delay cell toggling default 1'b1: enable delay cell toggling default
4:0	**DATWRDLY**	PAD_DAT_WR_RXDLY	**Write Data Status Internal Delay Line Control** This register is used to fine-tune write status phase latched by MSDC internal clock Total 32 stages

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A10400F0 DAT_RD_DLY0 MSDC Data Delay Line Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT0_RD_DLY								DAT1_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT2_RD_DLY								DAT3_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT0RDDLY**	DAT0_RD_DLY	**DAT0 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
20:16	**DAT1RDDLY**	DAT1_RD_DLY	**DAT1 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
12:8	**DAT2RDDLY**	DAT2_RD_DLY	**DAT2 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
4:0	**DAT3RDDLY**	DAT3_RD_DLY	**DAT3 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages

A10400F4 DAT_RD_DLY1 MSDC Data Delay Line Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				DAT4_RD_DLY								DAT5_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DAT6_RD_DLY								DAT7_RD_DLY				
Type				RW								RW				
Reset				0	0	0	0	0				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
28:24	**DAT4RDDLY**	DAT4_RD_DLY	**DAT4 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
20:16	**DAT5RDDLY**	DAT5_RD_DLY	**DAT5 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
12:8	**DAT6RDDLY**	DAT6_RD_DLY	**DAT6 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages
4:0	**DAT7RDDLY**	DAT7_RD_DLY	**DAT7 Pad RX Delay Line Control (for MSDC Read)** Total 32 stages

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A10400F8 HW_DBG_SEL MSDC H/W Debug Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		HW_DBG_WRAP_SEL	HW_DBG0_SEL						HW_DBG_WRAP_TYPE_SEL		HW_DBG1_SEL					
Type		RW	RW						RW		RW					
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			HW_DBG2_SEL						HW_DBG3_SEL							
Type			RW						RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
30	**DBGWSEL**	HW_DBG_WRAP_SEL	**Hardware debug output selection for wrapper** 0: Select original debug pins 1: Select wrapper debug pins
29:24	**DBG0SEL**	HW_DBG0_SEL	**Hardware debug output selection**
23:22	**DBGWTSEL**	HW_DBG_WRAP_TYPE_SEL	**Hardware debug output selection for wrapper** 2'd0: Select dbg_in20~dbg_in3b = DRAM_DBG 2'd1: Select dbg_in20~dbg_in3b = RISC_DBG 2'd2: Select dbg_in20~dbg_in3b = AHBM_DBG 2'd3: Select dbg_in20~dbg_in3b = AHBS_DBG
21:16	**DBG1SEL**	HW_DBG1_SEL	**Hardware debug output selection**
13:8	**DBG2SEL**	HW_DBG2_SEL	**Hardware debug output selection**
7:0	**DBG3SEL**	HW_DBG3_SEL	**Hardware debug output selection**

A1040100 MAIN_VER MSDC Main Version Register 20160503

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAIN_VER															
Type	RO															
Reset	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAIN_VER															
Type	RO															
Reset	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**MAINVER**	MAIN_VER	**Main Version**

A1040104 ECO_VER MSDC ECO Version Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ECO_VER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ECO_VER															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**ECOVER**	ECO_VER	**ECO Version**

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13. Pulse Width Modulation

13.1. Overview

Generic pulse width modulators (PWM) are implemented to generate pulse sequences with programmable frequency and duty cycle for LCD backlight. The duration of the PWM output signal is high as long as the internal counter value is between the threshold up and threshold down values. The waveform is shown in Figure 13.1-1.

Figure 13.1-1. PWM waveform

13.2. Features

Classic mode — the output waveform is specified by the internal counter (`PWM_COUNT`), threshold up value (`PWM_THRESH_UP`), threshold down value (`PWM_THRESH_DOWN`), clock source select (`PWM_CLK_CTRL[3:2]`) and clock prescaler scale (`PWM_CLK_CTRL[1:0]`).

13.3. Block diagram

The block diagram for the PWM is shown in

Figure 13.3-1.

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Figure 13.3-1. PWM block diagram

13.4. Functions

- Classic mode

The frequency and volume of the PWM output signal are determined by registers PWM_CLK_CTRL, PWM_THRESH_UP, PWM_THRESH_DOWN and PWM_COUNT. The power down signal (pwm_pdn) is applied to power down the PWM module. When PWM is deactivated (pwm_pdn = 1), the output will be in LOW state. The clock source (CLK_SRC) is all internal clock (not from GPIO).

The output PWM frequency is determined by:

$$\frac{CLK}{CLOCK_DIV \times (PWM_COUNT + 1)}$$

CLK = 13MHz, when PWM_CLK_CTRL[3:2] = 2'b00

CLK = 32kHz, when PWM_CLK_CTRL[3:2] = 2'b01

CLK = 48MHz, when PWM_CLK_CTRL[3:2] = 2'b10

CLOCK_DIV = 1, when PWM_CLK_CTRL[1:0] = 2'b00

CLOCK_DIV = 2, when PWM_CLK_CTRL[1:0] = 2'b01

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CLOCK_DIV = 4, when PWM_CLK_CTRL[1:0] = 2'b10

CLOCK_DIV = 8, when PWM_CLK_CTRL[1:0] = 2'b11

The output PWM duty cycle is determined by:

$$\frac{PWM_THRESH_UP - PWM_THRESH_DOWN + 1}{PWM_COUNT + 1}$$

Note, that PWM_THRESH_UP should be less than PWM_COUNT, and PWM_THRESH_DOWN should be less than PWM_THRESH_UP. If this condition is not satisfied, the output pulse of the PWM will be always high or always low. Figure 13.4-1 is the PWM waveform with indicated register values.

Figure 13.4-1. PWM waveform with register values

13.5. Register mapping

There are four PWM channels in this SoC. The channels and their base addresses are shown in the table below.

PWM number	Base address
PWM0	0xA2140000
PWM1	0xA2150000
PWM2	0xA2160000
PWM3	0xA2170000

Module name: PWM0 Base address: (+a2140000h)

Address	Name	Width (bits)	Register functionality
A2140000	**PWM_CTRL**	16	**PWM control register**
A2140004	**PWM_COUNT**	16	**PWM maximum counter value register**
A2140008	**PWM_THRESH_UP**	16	**PWM threshold_up value register**
A214000C	**PWM_THRESH_DOWN**	16	**PWM threshold_down value register**

A2140000 PWM_CTRL PWM control register 00000000

/Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWM_CLK_CTRL			
Type													RW			

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Reset													0	0	0	0

Bit(s)	Name	Description
3:0	PWM_CLK_CTRL	**Bit [1:0] : Selects clock prescaler scale of PWM** [1:0] = 2'b00 : f = fclk [1:0] = 2'b01 : f = fclk/2 [1:0] = 2'b10 : f = fclk/4 [1:0] = 2'b11 : f = fclk/8 **Bit [3:2] : Selects source clock frequency of PWM** [3:2] = 2'b00 : CLK = 13MHz [3:2] = 2'b01 : CLK = 32kHz (able to work in sleep mode) [3:2] = 2'b10 : CLK = 48MHz [3:2] = 2'b11 : CLK = 48MHz

A2140004 PWM_COUNT PWM maximum counter value register 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM_COUNT												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	PWM_COUNT	**PWM maximum counter value** This is the initial value for the internal counter. Regardless of the operation mode, if PWM_COUNT is written when the internal counter is counting backwards, the new initial value will not take effect until the internal counter counts down to 0, consider a complete period as an example.

A2140008 PWM_THRESH_UP PWM threshold_up value register 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM_THRESH_UP												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	PWM_THRESH_UP	**PWM threshold-up value** • When the internal counter value is greater than or equal to PWM_THRESH_UP and less than PWM_THRESH_DOWN, the PWM output signal will be "1". • When the internal counter value is less than PWM_THRESH_UP or bigger than PWM_THRESH_DOWN, the PWM output signal

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		will be "0".

A214000C PWM_THRESH_DOWN PWM threshold_down value register 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM_THRESH_DOWN												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	PWM_THRESH_DOWN	**PWM threshold-down value** • When the internal counter value is greater than or equal to PWM_THRESH_UP and less than PWM_THRESH_DOWN, the PWM output signal will be "1". • When the internal counter value is less than PWM_THRESH_UP or bigger than PWM_THRESH_DOWN, the PWM output signal will be "0".

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14. Pulse Width Modulation Signal Generator

14.1. Overview

Two pulse width modulation signal generators (PWMSG) are implemented to generate pulse sequences with programmable frequency and duration for LCD backlight, charging, or other purposes. Before enabling PWMSG, the pulse sequences must be prepared in the memory or registers. Then PWMSG will read the pulse sequences to generate random waveforms. A simple flow is shown in Figure 13.1-1.

Figure 14.1-1. Generation procedure of PWMSG

14.2. Features

1) Classic mode — The output waveform is specified by the internal counter (**PWMSG_DATA_WIDTH**) and threshold value (**PWMSG_THERSH**).
2) FIFO mode — Periodic waveform data is stored in 2x32-bit registers (**SEND_DATA0** and **SEND_DATA1**).
3) Memory mode — Periodic waveform data is stored in external memory where the address is set by the register **BUF0_BASE_ADDR** and the length is **BUF0_SIZE**.
4) Random mode – Non-periodic waveform data is stored in external memory where the addresses of two buffers can be set by registers **BUF0_BASE_ADDR** and **BUF1_BASE_ADDR**.

14.3. Block diagram

The block diagram for the PWMSG is shown in

Figure 13.3-1.

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PWMSG_Data_Access: PWMSG data transform unit

PWMSG generation: PWMSG waveform output unit

Figure 14.3-1. PWMSG block diagram

14.4. Functions

14.4.1. General configuration function

There are several registers that can be used to generate PWMSG waveform. PWMSG_EN determines which PWMSG unit is active. PWMSG_WAVE_NUM determines the number waveforms generated by PWMSG . For example, if PWM_WAVE_NUM is 2, the SEND_DATA0 and SEND_DATA1 will run twice. Note, that if WAVE_NUM=0, the waveform generation will not stop until it is disabled.

PWMSG_HDURATION and PWMSG_LDURATION determine high and low durations of the PWMSG output signal (the duration of PWMSG must not be 0). PWMSG_GDURATION and PWMSG_CON [8] (GUARD_VALUE) determine the value and duration between each pulse sequence (the guard duration of classic mode is useless). The pulse sequence output pattern is shown in Figure 14.4-1. PWMSG_CON [9:14] (STOP_BITPOS [5:0]) is used to indicate the stop bit position in a total of 64-bits.

Figure 14.4-1. PWMSG pulse sequence output pattern

14.4.2. Clock source selection

Table 14.4-1. PWMSG clock source table

Mode	CLKSEL_OLD	CLKSEL	CLKSRC
Classic mode	Don't care	0	26MHz

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Mode	CLKSEL_OLD	CLKSEL	CLKSRC
Classic mode	1	1	32kHz (only used in classic mode)
Classic mode	0	1	26MHz/1625
FIFO/Memory mode	Don't care	0	26MHz
FIFO/Memory mode	Don't care	1	26MHz/1625

14.4.3. Classic mode

The frequency and volume of the PWMSG output signal are determined by registers PWMSG_THRESH and PWMSG_DATA_WIDTH. BUF_SIZE and STOP_POSIT are not used in classic mode.

The output PWMSG frequency is determined by:

$$\frac{CLKSRC}{CLK_DIV \times (PWMSG_DATA_WIDTH + 1)}$$

The output PWMSG duty cycle is determined by:

$$\frac{PWMSG_THRESH}{PWMSG_DATA_WIDTH + 1}$$

Note, that PWMSG_THRESH should be less than PWMSG_DATA_WIDTH. If this condition is not satisfied, the output pulse of the PWMSG will always be high. Figure 13.4-1 is the PWMSG waveform with indicated register values.

Figure 14.4-2. PWMSG waveform with register values

14.4.4. FIFO mode

Waveform data is stored in 2x32-bit registers (SEND_DATA0 and SEND_DATA1) which can control different high and low periods for each pulse sequence. The waveform is shown in Figure 14.4-1. PWMSG_CON [9:14] (STOP_BITPOS [5:0]) is used to indicate the stop bit position in a total of 64-bits (2x32-bit). For example, if STOP_BITPOS [5:0] is 0, only SEND_DATA0[0] will be generated and so on until **SEND_DATA1[31]**.

14.4.5. Memory mode

The pulse sequence data are stored at an address set by BUF0_BASE_ADDR with a length of BUF0_SIZE. The pulse sequence in memory mode is shown in Figure 14.4-3. In memory mode, PWMSG_CON [9:14] (STOP_BITPOS [5:0]) is for the stop bit position of the last 32 bits.

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Figure 14.4-3. PWMSG pulse sequence in memory mode

14.4.6. Random mode

Non-periodic waveform data is stored in external memory where the addresses of two buffers are set by the registers `BUF0_BASE_ADDR` and `BUF1_BASE_ADDR`. Valid bit (`BUF_VALID`) is used to indicate data is ready in the respective memory buffer. The PWMSG generation will clear this bit after all data are fetched. The program should prepare the pulse sequence and set the valid bit to 1 in time before all data in the other memory buffer are fetched, otherwise the hardware will issue an interrupt to inform the MCU, and pulse generation will be stopped because there is no valid data. The pulse sequence in random mode is shown in Figure 14.4-4. The stop bit position must be at 32-bit in random mode, so `PWMSG_CON [9:14] (STOP_BITPOS [5:0])` is not used.

Figure 14.4-4. PWMSG pulse sequence in random mode

14.5. Register mapping

Module name: PWMSG Base address: (+a0170000h)

Address	Name	Width (bits)	Register Function
A0170050	PWM1_CON	32	PWM1 Control Register
A0170054	PWM1_HDURATION	32	PWM1 High Duration Register
A0170058	PWM1_LDURATION	32	PWM1 Low Duration Register
A017005C	PWM1_GDURATION	32	PWM1 Guard Duration Register
A0170060	PWM1_BUF0_BASE_ADDR	32	
A0170064	PWM1_BUF0_SIZE	32	PWM1 Buffer 0 Size Register

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Address	Name	Width (bits)	Register Function
A0170068	PWM1_BUF1_BASE_ADDR	32	PWM1 Buffer 1 Base Address register
A017006C	PWM1_BUF1_SIZE	32	PWM1 Buffer 1 Size Register
A0170070	PWM1_SEND_DATA0	32	PWM1 Send Data 0 Register
A0170074	PWM1_SEND_DATA1	32	PWM1 Send Data 1 Register
A0170078	PWM1_WAVE_NUM	32	PWM1 Wave Number Register
A017007C	PWM1_DATA_WIDTH	32	PWM1 Data Width Register
A0170080	PWM1_THRESH	32	PWM1 Thresh Register
A0170084	PWM1_SEND_WAVENUM	32	PWM1 Send Wave Number register
A0170088	PWM1_VALID	32	PWM1 Valid Register
A017008C	PWM1_BUF_BASE_ADDR2	32	
A0170010	PWM0_CON	32	PWM0 Control Register
A0170014	PWM0_HDURATION	32	PWM0 High Duration Register
A0170018	PWM0_LDURATION	32	PWM0 Low Duration Register
A017001C	PWM0_GDURATION	32	PWM0 Guard Duration Register
A0170020	PWM0_BUF0_BASE_ADDR	32	
A0170024	PWM0_BUF0_SIZE	32	PWM0 Buffer 0 Size Register
A0170028	PWM0_BUF1_BASE_ADDR	32	PWM0 Buffer 1 Base Address register
A017002C	PWM0_BUF1_SIZE	32	PWM0 Buffer 1 Size Register
A0170030	PWM0_SEND_DATA0	32	PWM0 Send Data 0 Register
A0170034	PWM0_SEND_DATA1	32	PWM0 Send Data 1 Register
A0170038	PWM0_WAVE_NUM	32	PWM0 Wave Number Register
A017003C	PWM0_DATA_WIDTH	32	PWM0 Data Width Register
A0170040	PWM0_THRESH	32	PWM0 Thresh Register
A0170044	PWM0_SEND_WAVENUM	32	PWM0 Send Wave Number register
A0170048	PWM0_VALID	32	PWM0 Valid Register
A017004C	PWM0_BUF_BASE_ADDR2	32	
A0170000	PWM_ENABLE	32	PWM Enable Register
A01701CC	PWM_LOOP_BACK_TEST	32	PWM Loop Back Test
A01701D0	PWM_3DLCM	32	PWM Support For 3D LCM
A0170200	PWM_INT_ENABLE	32	PWM Interrupt Enable Register
A0170204	PWM_INT_STATUS	32	PWM Interrupt Status Register
A0170208	PWM_INT_ACK	32	PWM Interrupt Acknowledge Register
A017020C	PWM_EN_STATUS	32	PWM Enable Status Register
A0170210	PWM_CK_26M_SEL	32	PWM BCLK Selection

A0170050 PWM1_CON PWM1 Control Register 00007E00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OLD_PWM_MODE**	**STOP_BITPOS**						**GUARD_VALUE**	**IDLE_VALUE**	**MODE**	**SRCSEL**	**CLKSEL_OLD**	**CLKSEL**	**CLKDIV**		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	OLD_PWM_MODE	0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	
8	GUARD_VALUE	
7	IDLE_VALUE	
6	MODE	0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	000b: CLK Hz 001b: CLK/2Hz 010b: CLK/4Hz 011b: CLK/8Hz 100b: CLK/16Hz 101b: CLK/32Hz 110b: CLK/64Hz 111b: CLK/128Hz

A0170054 PWM1_HDURATION PWM1 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**HDURATION**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	

A0170058 PWM1_LDURATION PWM1 Low Duration Register 00000001

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	LDURATION	

A017005C PWM1_GDURATION PWM1 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	

A0170060 PWM1_BUF0_BASE_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	

A0170064 PWM1_BUF0_SIZE PWM1 Buffer 0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF0_SIZE	

A0170068 PWM1_BUF1_BASE_ADDR PWM1 Buffer 1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	

A017006C PWM1_BUF1_SIZE PWM1 Buffer 1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	

A0170070 PWM1_SEND_DATA0 PWM1 Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam	SEND_DATA0															

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e																
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA0	

A0170074 PWM1_SEND_DATA1 PWM1 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	

A0170078 PWM1_WAVE_NUM PWM1 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	

A017007C PWM1_DATA_WIDTH PWM1 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**DATA_WIDTH**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	

A0170080 PWM1_THRESH PWM1 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**THRESH**												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	

A0170084 PWM1_SEND_WAVENUM PWM1 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SEND_WAVENUM**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	

A0170088 PWM1_VALID PWM1 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**BUF1_VALID**	**BUF0_VALID**
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

A017008C **PWM1_BUF_BASE_ADDR2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**BUF_BASE_ADDR2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**BUF_BASE_ADDR2**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF_BASE_ADDR2	

A0170010 **PWM0_CON** **PWM0 Control Register** **00007E00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**OLD_PWM_MODE**	**STOP_BITPOS**						**GUARD_VALUE**	**IDLE_VALUE**	**MODE**	**SRCSEL**	**CLKSEL_OLD**	**CLKSEL**	**CLKDIV**		
Type	RW	RW						RW	RW	RW	RW	RW	RW	RW		
Reset	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15	OLD_PWM_MODE	0: New PWM mode 1: Old PWM mode
14:9	STOP_BITPOS	
8	GUARD_VALUE	
7	IDLE_VALUE	
6	MODE	0: Periodical PWM mode 1: Random PWM mode
5	SRCSEL	0: FIFO mode 1: Memory mode
4	CLKSEL_OLD	0: CLK=32K; CLK is not used. 1: CLK=32K; CLK can be used.
3	CLKSEL	0: CLK=CLKSRC 1: CLK=CLKSRC/1625
2:0	CLKDIV	000b: CLK Hz 001b: CLK/2Hz 010b: CLK/4Hz 011b: CLK/8Hz 100b: CLK/16Hz 101b: CLK/32Hz 110b: CLK/64Hz 111b: CLK/128Hz

A0170014 PWM0_HDURATION PWM0 High Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:0	HDURATION	

A0170018 PWM0_LDURATION PWM0 Low Duration Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LDURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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Bit(s)	Name	Description
15:0	LDURATION	

A017001C PWM0_GDURATION PWM0 Guard Duration Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GUARD_DURATION															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	GUARD_DURATION	

A0170020 PWM0_BUF0_BASE_ADDR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF0_BS_ADDR	

A0170024 PWM0_BUF0_SIZE PWM0 Buffer 0 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF0_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
15:0	BUF0_SIZE	

A0170028 PWM0_BUF1_BASE_ADDR PWM0 Buffer 1 Base Address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_BS_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF1_BS_ADDR	

A017002C PWM0_BUF1_SIZE PWM0 Buffer 1 Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF1_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BUF1_SIZE	

A0170030 PWM0_SEND_DATA0 PWM0 Send Data 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	SEND_DATA0	

A0170034 PWM0_SEND_DATA1 PWM0 Send Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_DATA1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SEND_DATA1	

A0170038 PWM0_WAVE_NUM PWM0 Wave Number Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAVE_NUM															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	WAVE_NUM	

A017003C PWM0_DATA_WIDTH PWM0 Data Width Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DATA_WIDTH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	DATA_WIDTH	

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Bit(s)	Name	Description

A0170040 PWM0_THRESH PWM0 Thresh Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				THRESH												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	THRESH	

A0170044 PWM0_SEND_WAVENUM PWM0 Send Wave Number register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEND_WAVENUM															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SEND_WAVENUM	

A0170048 PWM0_VALID PWM0 Valid Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															BUF1_VALID	BUF0_VALID
Type															RW	RW
Reset															0	0

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Bit(s)	Name	Description
1	BUF1_VALID	0: Memory 1 is empty. 1: Memory 1 is not empty. When finishing writing data to memory 1, write 1 to inform PWM the data in memory 1 are ready.
0	BUF0_VALID	0: Memory 0 is empty. 1: Memory 0 is not empty. When finishing writing data to memory 0, write 1 to inform PWM the data in memory 0 are ready.

A017004C PWM0_BUF_BASE_ADDR2 **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUF_BASE_ADDR2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUF_BASE_ADDR2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	BUF_BASE_ADDR2	

A0170000 PWM_ENABLE **PWM Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PWM1_EN	PWM0_EN
Type															RW	RW
Reset															0	0

Bit(s)	Name	Description
1	PWM1_EN	0: Disabe PWM1 1: Enable PWM1
0	PWM0_EN	0: Disabe PWM0 1: Enable PWM0

A01701CC PWM_LOOP_BACK_TEST **PWM Loop Back Test** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										**PWM6_STATUS**	**PWM5_STATUS**	**PWM4_STATUS**	**PWM3_STATUS**	**PWM2_STATUS**	**PWM1_STATUS**	**PWM0_STATUS**
Type										RU	RU	RU	RU	RU	RU	RU
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	PWM6_STATUS	0: PWM6 output is low. 1: PWM6 output is high.
5	PWM5_STATUS	0: PWM5 output is low. 1: PWM5 output is high.
4	PWM4_STATUS	0: PWM4 output is low. 1: PWM4 output is high.
3	PWM3_STATUS	0: PWM3 output is low. 1: PWM3 output is high.
2	PWM2_STATUS	0: PWM2 output is low. 1: PWM2 output is high.
1	PWM1_STATUS	0: PWM1 output is low. 1: PWM1 output is high.
0	PWM0_STATUS	0: PWM0 output is low. 1: PWM0 output is high.

A01701D0 PWM_3DLCM PWM Support For 3D LCM 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**PWM_3DLCM_4**	**PWM_3DLCM_3**	**PWM_3DLCM_2**	**PWM_3DLCM_1**
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PWM_3DLCM_SYNC**			**PWM_3DLCM_5_base**	**PWM_3DLCM_4_base**	**PWM_3DLCM_3_base**	**PWM_3DLCM_2_base**	**PWM_3DLCM_1_base**				**PWM_3DLCM_4_INV**	**PWM_3DLCM_3_INV**	**PWM_3DLCM_2_INV**	**PWM_3DLCM_1_INV**	**PWM_3DLCM_EN**
Type	RW			RW	RW	RW	RW	RW				RW	RW	RW	RW	RW
Reset	0			0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
19	PWM_3DLCM_4	0: PWM3 is not selected as PWM auxiliary channel. 1: PWM3 is selected as PWM auxiliary channel.
18	PWM_3DLCM_3	0: PWM2 is not selected as PWM auxiliary channel. 1: PWM2 is selected as PWM auxiliary channel.

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Bit(s)	Name	Description
17	PWM_3DLCM_2	0: PWM1 is not selected as PWM auxiliary channel. 1: PWM1 is selected as PWM auxiliary channel.
16	PWM_3DLCM_1	0: PWM0 is not selected as PWM auxiliary channel. 1: PWM0 is selected as PWM auxiliary channel.
15	PWM_3DLCM_SYNC	0: PWM auxiliary channel does not keep low when PWM base channel is disabled. 1: PWM auxiliary channel keeps low when PWM base channel is disabled.
12	PWM_3DLCM_5_base	0: PWM4 is not selected as PWM base channel. 1: PWM4 is selected as PWM base channel.
11	PWM_3DLCM_4_base	0: PWM3 is not selected as PWM base channel. 1: PWM3 is selected as PWM base channel.
10	PWM_3DLCM_3_base	0: PWM2 is not selected as PWM base channel. 1: PWM2 is selected as PWM base channel.
9	PWM_3DLCM_2_base	0: PWM1 is not selected as PWM base channel. 1: PWM1 is selected as PWM base channel.
8	PWM_3DLCM_1_base	0: PWM0 is not selected as PWM base channel. 1: PWM0 is selected as PWM base channel.
4	PWM_3DLCM_4_INV	0: PWM3 is the same as PWM base channel when PWM3 is selected as auxiliary channel. 1: PWM3 is inversion of PWM base channel when PWM3 is selected as auxiliary channel.
3	PWM_3DLCM_3_INV	0: PWM2 is the same as PWM base channel when PWM2 is selected as auxiliary channel. 1: PWM2 is inversion of PWM base channel when PWM2 is selected as auxiliary channel.
2	PWM_3DLCM_2_INV	0: PWM1 is the same as PWM base channel when PWM1 is selected as auxiliary channel. 1: PWM1 is inversion of PWM base channel when PWM1 is selected as auxiliary channel.
1	PWM_3DLCM_1_INV	0: PWM0 is the same as PWM base channel when PWM0 is selected as auxiliary channel. 1: PWM0 is inversion of PWM base channel when PWM0 is selected as auxiliary channel.
0	PWM_3DLCM_EN	0: Disable 3D_LCM for PWM 1: Enable 3D_LCM for PWM

A0170200 PWM_INT_ENABLE PWM Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PWM5_INT_UNDERFLOW_EN	PWM5_INT_FINISH_EN	PWM4_INT_UNDERFLOW_EN	PWM4_INT_FINISH_EN	PWM3_INT_UNDERFLOW_EN	PWM3_INT_FINISH_EN	PWM2_INT_UNDERFLOW_EN	PWM2_INT_FINISH_EN	PWM1_INT_UNDERFLOW_EN	PWM1_INT_FINISH_EN	PWM0_INT_UNDERFLOW_EN	PWM0_INT_FINISH_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
11	PWM5_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM5 1: Enable underflow interrupt for PWM5
10	PWM5_INT_FINISH_EN	0: Disable finished interrupt for PWM5 1: Enable finished interrupt for PWM5
9	PWM4_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM4 1: Enable underflow interrupt for PWM4
8	PWM4_INT_FINISH_EN	0: Disable finished interrupt for PWM4 1: Enable finished interrupt for PWM4
7	PWM3_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM3 1: Enable underflow interrupt for PWM3
6	PWM3_INT_FINISH_EN	0: Disable finished interrupt for PWM3 1: Enable finished interrupt for PWM3
5	PWM2_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM2 1: Enable underflow interrupt for PWM2
4	PWM2_INT_FINISH_EN	0: Disable finished interrupt for PWM2 1: Enable finished interrupt for PWM2
3	PWM1_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM1 1: Enable underflow interrupt for PWM1
2	PWM1_INT_FINISH_EN	0: Disable finished interrupt for PWM1 1: Enable finished interrupt for PWM1
1	PWM0_INT_UNDERFLOW_EN	0: Disable underflow interrupt for PWM0 1: Enable underflow interrupt for PWM0
0	PWM0_INT_FINISH_EN	0: Disable finished interrupt for PWM0 1: Enable finished interrupt for PWM0

A0170204 PWM_INT_STATUS PWM Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PWM6_INT_UNDERFLOW_ST	PWM6_INT_FINISH_ST	PWM5_INT_UNDERFLOW_ST	PWM5_INT_FINISH_ST	PWM4_INT_UNDERFLOW_ST	PWM4_INT_FINISH_ST	PWM3_INT_UNDERFLOW_ST	PWM3_INT_FINISH_ST	PWM2_INT_UNDERFLOW_ST	PWM2_INT_FINISH_ST	PWM1_INT_UNDERFLOW_ST	PWM1_INT_FINISH_ST	PWM0_INT_UNDERFLOW_ST	PWM0_INT_FINISH_ST
Type			RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU	RU
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	PWM6_INT_UNDERFLOW_ST	0: PWM6 underflow interrupt has not come. 1: PWM6 underflow interrupt has come.
12	PWM6_INT_FINISH_ST	0: PWM6 finished interrupt has not come. 1: PWM6 finished interrupt has come.
11	PWM5_INT_UNDERFLOW_ST	0: PWM5 underflow interrupt has not come. 1: PWM5 underflow interrupt has come.
10	PWM5_INT_FINISH_ST	0: PWM5 finished interrupt has not come.

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Bit(s)	Name	Description
		1: PWM5 finished interrupt has come.
9	PWM4_INT_UNDERFLOW_ST	0: PWM4 underflow interrupt has not come. 1: PWM4 underflow interrupt has come.
8	PWM4_INT_FINISH_ST	0: PWM4 finished interrupt has not come. 1: PWM4 finished interrupt has come.
7	PWM3_INT_UNDERFLOW_ST	0: PWM3 underflow interrupt has not come. 1: PWM3 underflow interrupt has come.
6	PWM3_INT_FINISH_ST	0: PWM3 finished interrupt has not come. 1: PWM3 finished interrupt has come.
5	PWM2_INT_UNDERFLOW_ST	0: PWM2 underflow interrupt has not come. 1: PWM2 underflow interrupt has come.
4	PWM2_INT_FINISH_ST	0: PWM2 finished interrupt has not come. 1: PWM2 finished interrupt has come.
3	PWM1_INT_UNDERFLOW_ST	0: PWM1 underflow interrupt has not come. 1: PWM1 underflow interrupt has come.
2	PWM1_INT_FINISH_ST	0: PWM1 finished interrupt has not come. 1: PWM1 finished interrupt has come.
1	PWM0_INT_UNDERFLOW_ST	0: PWM0 underflow interrupt has not come. 1: PWM0 underflow interrupt has come.
0	PWM0_INT_FINISH_ST	0: PWM0 finished interrupt has not come. 1: PWM0 finished interrupt has come.

A0170208 PWM_INT_ACK PWM Interrupt Acknowledge Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PWM6_INT_UNDERFLOW_ACK	PWM6_INT_FINISH_ACK	PWM5_INT_UNDERFLOW_ACK	PWM5_INT_FINISH_ACK	PWM4_INT_UNDERFLOW_ACK	PWM4_INT_FINISH_ACK	PWM3_INT_UNDERFLOW_ACK	PWM3_INT_FINISH_ACK	PWM2_INT_UNDERFLOW_ACK	PWM2_INT_FINISH_ACK	PWM1_INT_UNDERFLOW_ACK	PWM1_INT_FINISH_ACK	PWM0_INT_UNDERFLOW_ACK	PWM0_INT_FINISH_ACK
Type			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	PWM6_INT_UNDERFLOW_ACK	0: Not clear PWM6 underflow acknowledgement 1: Clear PWM6 underflow interrupt
12	PWM6_INT_FINISH_ACK	0: Not clear PWM6 finished interrupt 1: Clear PWM6 finished interrupt
11	PWM5_INT_UNDERFLOW_ACK	0: Not clear PWM5 underflow interrupt 1: Clear PWM5 underflow interrupt
10	PWM5_INT_FINISH_ACK	0: Not clear PWM5 finished interrupt 1: Clear PWM5 finished interrupt
9	PWM4_INT_UNDERFLOW_ACK	0: Not clear PWM4 underflow interrupt 1: Clear PWM4 underflow interrupt
8	PWM4_INT_FINISH_ACK	0: Not clear PWM4 finished interrupt

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Bit(s)	Name	Description
		1: Clear PWM4 finished interrupt
7	PWM3_INT_UNDERFLOW_ACK	0: Not clear PWM3 underflow interrupt 1: Clear PWM3 underflow interrupt
6	PWM3_INT_FINISH_ACK	0: Not clear PWM3 finished interrupt 1: Clear PWM3 finished interrupt
5	PWM2_INT_UNDERFLOW_ACK	0: Not clear PWM2 underflow interrupt 1: Clear PWM2 underflow interrupt
4	PWM2_INT_FINISH_ACK	0: Not clear PWM2 finished interrupt 1: Clear PWM2 finished interrupt
3	PWM1_INT_UNDERFLOW_ACK	0: Not clear PWM1 underflow interrupt 1: Clear PWM1 underflow interrupt
2	PWM1_INT_FINISH_ACK	0: Not clear PWM1 finished interrupt 1: Clear PWM1 finished interrupt
1	PWM0_INT_UNDERFLOW_ACK	0: Not clear PWM0 underflow interrupt 1: Clear PWM0 underflow interrupt
0	PWM0_INT_FINISH_ACK	0: Not clear PWM0 finished interrupt 1: Clear PWM0 finished interrupt

A017020C PWM_EN_STATUS PWM Enable Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PWM6_EN_ST	PWM5_EN_ST	PWM4_EN_ST	PWM3_EN_ST	PWM2_EN_ST	PWM1_EN_ST	PWM0_EN_ST
Type										RO	RO	RO	RO	RO	RO	RO
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	PWM6_EN_ST	
5	PWM5_EN_ST	
4	PWM4_EN_ST	
3	PWM3_EN_ST	
2	PWM2_EN_ST	
1	PWM1_EN_ST	
0	PWM0_EN_ST	

A0170210 PWM_CK_26M_SEL PWM BCLK Selection 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																PWM_26

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																M_SEL
Type																RW
Reset																1

Bit(s)	Name	Description
0	PWM_26M_SEL	0: Select bus CLK as BCLK 1: Select 26MHz fixed CLK as BCLK

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15. Reset Generation Unit

15.1. Introduction

MediaTek MT2625 reset generation unit (RGU) provides three types of resets: hardware reset, watchdog reset and software reset:

- Hardware reset

This reset is input through the `xreset_rstb` pin, which is driven low during PMU power-on. The hardware reset has a global effect on the chip; all digital and analog circuits are initialized.

- Watchdog reset

The watchdog reset is generated when the watchdog timer expires. CMSYS, MDSYS, SDCTL and INFRASYS are affected by the watchdog reset.

- Software reset

Software resets are local reset signals that initialize specific hardware components or external devices (PAD output). Subsystems with this feature are MDSYS and SDCTL.

15.2. Features

- Watchdog timer (WDT) timeout length and interval time can be configured by registers `WDT_LENGTH` and `WDT_INTERVAL`.
- The reset generation unit includes four external trigger sources: `xreset_rstb`, `JTAG_rstb`, `AIRCR_rstb` and `PCM_wdt_rstb`. The latter three signals can be masked independently by registers `MODULE0_RST_MASK`, `MODULE1_RST_MASK` and `MODULE2_RST_MASK`.
- The `AIRCR_rstb` reset source can be extended by register `AIRCR_RST_INTERVAL` for special applications.
- Each register can be protected by corresponding keys to avoid unexpected register settings.
- The RGU includes six retention flags and six retention data, these registers will only be reset by whole chip reset (`xreset_rstb`).

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15.3. Block diagram

Figure 15.3-1. Block diagram of RGU

15.4. Function description

The WDT timeout length is generated by a 16-bit counter and the counter clock period is 15.625ms. The WDT interval time is generated by a 16-bit counter and the counter clock period is 3.05µs. The detailed diagram is shown in Figure 15.4-1.

Figure 15.4-1. WDT time out length and interval time

The AIRCR reset extender is an 8-bit counter with a counter clock period of 3.05µs. The operation range of the AIRCR interval extender is from 0 to 7.78µs.

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15.5. Register mapping

Module name: RGU Base address: (+A2090000h)

Address	Name	Width (bits)	Register Function
A2090000	WDT_EN	32	Watchdog Timer Enable Register
A2090004	WDT_LENGTH	32	Watchdog Length Register
A2090008	WDT_INTERVAL	32	Watchdog Interval Register
A209000C	WDT_SW_RESTART	32	Watchdog Timer Software Restart Register
A2090010	WDT_SW_RST	32	Watchdog Timer Software Reset Register
A2090014	WDT_AUTO_RESTART_EN	32	Watchdog Timer Auto Restart Register
A2090018	WDT_IE	32	Watchdog Timer Interrupt Enable Register
A209001C	WDT_INT	32	Watchdog Timer Interrupt Register
A2090020	WDT_STA	32	Watchdog Timer Status Register
A2090024	SW_RSTSYS	32	Software Reset System Register
A2090028	SW_RST0	32	Software Reset 0 Register
A209002C	SW_RST1	32	Software Reset 1 Register
A2090030	RST_MASK0	32	Reset Mask 0 Register
A2090034	RST_MASK1	32	Reset Mask 1 Register
A2090038	CM4_RST_INTERVAL	32	Cortex-M4 Reset Interval Register
A209003C	RETN_FLAG0	32	Retention Flag 0 Register
A2090040	RETN_FLAG1	32	Retention Flag 1 Register
A2090044	RETN_FLAG2	32	Retention Flag 2 Register
A2090048	RETN_FLAG3	32	Retention Flag 3 Register
A209004C	RETN_FLAG4	32	Retention Flag 4 Register
A2090050	RETN_FLAG5	32	Retention Flag 5 Register
A2090054	RETN_DAT0	32	Retention Data 0 Register
A2090058	RETN_DAT1	32	Retention Data 1 Register
A209005C	RETN_DAT2	32	Retention Data 2 Register
A2090060	RETN_DAT3	32	Retention Data 3 Register
A2090064	RETN_DAT4	32	Retention Data 4 Register
A2090068	RETN_DAT5	32	Retention Data 5 Register

A2090000 **WDT_EN** **Watchdog Timer Enable Register** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								WDT_EN	KEY							
Type								RW	WO							
Reset								1	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
8	WDT_EN	**Watchdog timer enable** 0: Disable watchdog timer 1: Enable watchdog timer
7:0	KEY	**Configure WDT enable register if KEY= 8'h11**

A2090004 **WDT_LENGTH** **Watchdog Length Register** **07FF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDT_LENGTH															
Type	RW															
Reset	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	WDT_LENGTH	**Watchdog timer length** The length counter unit is 15.625 ms.
7:0	KEY	**Configure WDT length if KEY= 8'h12**

A2090008 **WDT_INTERVAL** **Watchdog Interval Register** **0FFF0000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDT_INTERVAL															
Type	RW															
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	WDT_INTERVAL	**Watchdog timer interval** Indicates reset duration when watchdog timer timeout occurs. However, the register will not be valid when WDT_IE is 1. The interval counter unit is 3.05 µs.
7:0	KEY	**Configure WDT interval if KEY= 8'h13**

A209000C **WDT_SW_RESTART** **Watchdog Timer Software Restart Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KEY[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	KEY	**Watchdog timer software restart** Software restart watchdog timer, if KEY= 32'h1456789a

A2090010 **WDT_SW_RST** **Watchdog Timer Software Reset Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	KEY[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	KEY	**Watchdog timer software reset** Software trigger watchdog timer reset, if KEY= 32'h156789ab

A2090014 **WDT_AUTO_RESTART_EN** **Watchdog Timer Auto Restart Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								WDT_AUTO_RESTART_EN	KEY							
Type								RW	WO							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	WDT_AUTO_RESTART_EN	**Watchdog timer automatic restart enable** Hardware auto restart after watchdog timer reset 0: Disable 1: Enable
7:0	KEY	**Configure WDT automatic restart enable register if KEY= 8'h16**

A2090018 **WDT_IE** **Watchdog Timer Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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A2090018 WDT_IE Watchdog Timer Interrupt Enable Register 00000000

Name								WDT_IE	KEY							
Type								RW	WO							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	WDT_IE	**Watchdog timer interrupt enable** Issues an interrupt instead of a watchdog timer reset
7:0	KEY	**Configure WDT interrupt enable if KEY= 8'h17**

A209001C WDT_INT Watchdog Timer Interrupt Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																WDT_INT
Type																RC
Reset																0

Bit(s)	Name	Description
0	WDT_INT	**Watchdog timer interrupt** WDT interrupt read clear register

A2090020 WDT_STA Watchdog Timer Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WDT_STA	
Type															RO	
Reset															0	0

Bit(s)	Name	Description
1:0	WDT_STA	**Watchdog timer status** [1]: HW_WDT, indicates the cause of watchdog reset 0: Reset not due to watchdog timer. 1: Reset due to watchdog timer expired timeout. [0]: SW_WDT, indicates if watchdog timer reset is triggered by software 0: Reset not due to software triggered watchdog timer 1: Reset due to software triggered watchdog timer

A2090024 SW_RSTSYS Software Reset System Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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A2090024 SW_RSTSYS Software Reset System Register 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SYSTEM_SW_RST	KEY0							
Type								RW	WO							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8	SYSTEM_SW_RST	**SYSTEM_SW_RST** 0: no reset 1: Invoke a reset
7:0	KEY0	**Configure SYSTEM software reset, if KEY= 8'h18**

A2090028 SW_RST0 Software Reset 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MODULE1_SW_RST	KEY1							
Type								RW	WO							
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MODULE0_SW_RST	KEY0							
Type								RW	WO							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	MODULE1_SW_RST	**Reserved**
23:16	KEY1	**KEY= 8'h1a**
8	MODULE0_SW_RST	**MDSYS_SW_RST** 0: no reset 1: Invoke a reset
7:0	KEY0	**Configure MDSYS software reset if KEY= 8'h19**

A209002C SW_RST1 Software Reset 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MODULE3_SW_RST	KEY1							
Type								RW	WO							

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A209002C SW_RST1 Software Reset 1 Register 00000000

Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**MODULE2_SW_RST**	**KEY0**							
Type								RW	WO							
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	MODULE3_SW_RST	**Reserved**
23:16	KEY1	**KEY= 8'h1c**
8	MODULE2_SW_RST	**SDCTL_SW_RST** 0: no reset 1: Invoke a reset
7:0	KEY0	**Configure SDCTL software reset, if KEY= 8'h1b**

A2090030 RST_MASK0 Reset Mask 0 Register 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**MODULE1_RST_MASK**	**KEY1**							
Type								RW	WO							
Reset								1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**MODULE0_RST_MASK**	**KEY0**							
Type								RW	WO							
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	MODULE1_RST_MASK	**AIRCR reset require mask** Mask reset source from AIRCR, default enable. 0: disable mask 1: enable mask
23:16	KEY1	**Configure AIRCR reset mask, if KEY= 8'h1e**
8	MODULE0_RST_MASK	**JTAG reset mask** Mask reset source from JTAG, default enable. 0: disable mask 1: enable mask
7:0	KEY0	**Configure JTAG reset mask, if KEY= 8'h1d**

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A2090034 RST_MASK1 Reset Mask 1 Register 01000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								MODULE3_RST_MASK	KEY1							
Type								RW	WO							
Reset								1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								MODULE2_RST_MASK	KEY0							
Type								RW	WO							
Reset								1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	MODULE3_RST_MASK	**PMU reset mask** Mask reset to PMU, default enable. 0: disable mask 1: enable mask
23:16	KEY1	**Configure PMU reset mask, if KEY= 8'h21**
8	MODULE2_RST_MASK	**PCM reset require mask** Mask reset source from PCM, default enable. 0: disable mask 1: enable mask
7:0	KEY0	**Configure PCM reset mask, if KEY= 8'h1f**

A2090038 CM4_RST_INTERVAL Cortex-M4 Reset Interval Register 00000700

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CM4_RST_INTERVAL								KEY							
Type	RW								WO							
Reset	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	CM4_RST_INTERVAL	**Cortex-M4 (AIRCR) reset interval** Indicates reset duration when Cortex-M4 AIRCR is enabled. The interval counter unit is 3.05 us.
7:0	KEY	**KEY= 8'h22**

A209003C RETN_FLAG0 Retention Flag 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG0															

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A209003C **RETN_FLAG0** **Retention Flag 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RETN_FLAG0	**Retention flag 0** This register will only be reset by hardware reset.
7:0	KEY	**Configure Retention flag 0 reset mask, if KEY= 8'h23**

A2090040 **RETN_FLAG1** **Retention Flag 1 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RETN_FLAG1	**Retention flag 1** This register will only be reset by hardware reset.
7:0	KEY	**Configure Retention flag 1 reset mask, if KEY= 8'h24**

A2090044 **RETN_FLAG2** **Retention Flag 2 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RETN_FLAG2	**Retention flag 2** This register will only be reset by hardware reset.
7:0	KEY	**Configure Retention flag 2 reset mask if KEY= 8'h25**

A2090048 **RETN_FLAG3** **Retention Flag 3 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG3															
Type	RW															

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A2090048 **RETN_FLAG3** **Retention Flag 3 Register** **00000000**

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RETN_FLAG3	**Retention flag 3** This register will only be reset by hardware reset.
7:0	KEY	**Configure Retention flag 3 reset mask, if KEY= 8'h26**

A209004C **RETN_FLAG4** **Retention Flag 4 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RETN_FLAG4	**Retention flag 4** This register will only be reset by hardware reset.
7:0	KEY	**Configure Retention flag 4 reset mask, if KEY= 8'h27**

A2090050 **RETN_FLAG5** **Retention Flag 5 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_FLAG5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									KEY							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RETN_FLAG5	**Retention flag 5** This register will only be reset by hardware reset.
7:0	KEY	**Configure Retention flag 5 reset mask, if KEY= 8'h28**

A2090054 **RETN_DAT0** **Retention Data 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_DAT0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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A2090054 RETN_DAT0 Retention Data 0 Register 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RETN_DAT0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RETN_DAT0	**Retention data 0** This register will only be reset by hardware reset.

A2090058 RETN_DAT1 Retention Data 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_DAT1[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RETN_DAT1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RETN_DAT1	**Retention data 1** This register will only be reset by hardware reset.

A209005C RETN_DAT2 Retention Data 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_DAT2[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RETN_DAT2[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RETN_DAT2	**Retention data 2** This register will only be reset by hardware reset.

A2090060 RETN_DAT3 Retention Data 3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_DAT3[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RETN_DAT3[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RETN_DAT3	**Retention data 3**

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Bit(s)	Name	Description
		This register will only be reset by hardware reset.

A2090064 RETN_DAT4 Retention Data 4 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_DAT4[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RETN_DAT4[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RETN_DAT4	**Retention data 4** This register will only be reset by hardware reset.

A2090068 RETN_DAT5 Retention Data 5 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RETN_DAT5[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RETN_DAT5[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RETN_DAT5	**Retention data 5** This register will only be reset by hardware reset.

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16. SDIO

16.1. Overview

The SD Input/Output (SDIO) card is based on and compatible with the SD memory card. The controller fully supports the SD memory card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 and SDIO Specification version 2.0.

SDIO provides high-speed data IO with low power consumption. MT2625 SDIO module provides an SDIO2.0 card interface connected to the host and can support multiple speed modes including default speeds, SDR12 and SDR25.

16.2. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 16.2-1. Abbreviations

Abbreviation	Definition
SDIO	Secure digital input/output
SDR	Single data rate
CIS	Card information structure
CSR	Control and status register
GPD	Generic packet descriptor
BD	Buffer descriptor
IOC	Interrupt on completion
DW	Double word

16.3. Features

- Provides SDIO 2.0 host interfaces
  - SDIO 2.0:
    - 1-bit and 4-bit SD data transfer modes
    - Default mode: Variable clock rate 0-25MHz, up to 12.5MB/sec interface speed (using 4 parallel data lines)
    - High-Speed mode: Variable clock rate 0-50 MHz, up to 25MB/sec interface speed (using 4 data lines)
    - Data rate up to 50Mbps in serial mode, 50 x 4 Mbps in parallel mode, the module is targeted at 50MHz operating clock.
    - 32-bit access for control registers
    - 32-bit access for FIFO
    - Built-in 32 bytes FIFO buffers to transmit and receive, FIFO is shared for transmit and receive operations.
    - Built-in cyclic redundancy check (CRC) circuit
    - Interrupt capabilities

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- Does not support SPI
- Supports DMA
- WLAN TX packet de-aggregation and WLAN RX packet aggregation
- WLAN WHISR/ RX enhanced read mode

- CR and data port access
  - Supports control register (CR) port single read/write access (AHB slave)
  - Supports data port single and burst read/write access (AHB master)
- DMA function
  - One TX channel and two RX channels
  - AHB master interface
  - Moves TX data from HIF buffer to system, EMI, retention memory
  - Moves RX data or firmware prepared data from system, EMI, retention memory to HIF buffer

16.4. Block diagram

The block diagram of the SDIO controller is shown in Figure 16.4-1.

Figure 16.4-1. SDIO controller block diagram

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16.5. Functions

From the external view, the SDIO interface mainly includes the SD bus and AHB master and slave. The AHB master is used for DMA operations and the AHB slave is used for register access from the MCU. The SD bus provides an interface for SD specification.

16.5.1. Signal pins

Figure 16.5-1. Signal connections to 4-bit SDIO cards

Table 16.5-1. SDIO pin definitions

Pin	Name	SD 4-bit mode		SD 1-bit mode	
1	SLV_MC0_DA3	DAT[3]	Data line3	N/C	Not used
2	SLV_MC0_CM0	CMD	Command line	CMD	Command line
3	VSS1	VSS1	Ground	VSS1	Ground
4	VDD	VDD	Supply voltage	VDD	Supply voltage
5	SLV_MC0_CK	CLK	Clock	CLK	Clock
6	VSS2	VSS2	Ground	VSS2	Ground
7	SLV_MC0_DA0	DAT[0]	Data line0	DATA	Data line
8	SLV_MC0_DA1	DAT[1]	Data line1 or interrupt	IRQ	Interrupt
9	SLV_MC0_DA2	DAT[2]	Data line2	RW	Not used

16.5.2. SDIO timing waveform (3.3V)

Figure 16.5-2. Bus signal levels

Table 16.5-2. Bus signal voltage

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD min

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Parameter	Symbol	Min.	Max.	Unit	Conditions
Output Low Voltage	VOL		0.125*VDD	V	IOL = 2mA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	Vss-0.3	0.25*VDD	V	

Figure 16.5-3. Bus timing diagram (default)

Table 16.5-3. Bus timing parameter values (default)

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	$C_{CARD} \leq 10$ pF (1 card)
Clock frequency identification mode	f_{OD}	0/100	400	kHz	$C_{CARD} \leq 10$ pF (1 card)
Clock low time	t_{WL}	10		ns	$C_{CARD} \leq 10$ pF (1 card)
Clock high time	t_{WH}	10		ns	$C_{CARD} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{CARD} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		10	ns	$C_{CARD} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_{CARD} \leq 10$ pF (1 card)
Input hold time	t_{IH}	5		ns	$C_{CARD} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{OLDY}	0	14	ns	$C_L \leq 40$ pF (1 card)

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Parameter	Symbol	Minimum	Maximum	Unit	Remark
Output delay time during identification mode	t_{OLDY}	0	50	ns	$C_L \leq 40$ pF (1 card)

Figure 16.5-4. High-speed timing diagram

Table 16.5-4. High-speed timing parameter values

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	$C_{CARD} \leq 10$ pF (1 card)
Clock low time	t_{WL}	7		ns	$C_{CARD} \leq 10$ pF (1 card)
Clock high time	t_{WH}	7		ns	$C_{CARD} \leq 10$ pF (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{CARD} \leq 10$ pF (1 card)
Clock fall time	t_{THL}		3	ns	$C_{CARD} \leq 10$ pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{CARD} \leq 10$ pF (1 card)
Input hold time	t_{IH}	2		ns	$C_{CARD} \leq 10$ pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{OLDY}		14	ns	$C_L \leq 40$ pF (1 card)
Output hold time	t_{OH}	2.5		ns	$C_L \geq 40$ pF (1 card)
Total system capacitance for each line (1)	C_L		40	pF	1 card

(1) In order to satisfy the serving time, the host shall drive only one card

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16.6. Register mapping

16.6.1. Firmware register

Module name: SDIO_FW Base address: (+A1050000h)

Address	Name	Width (bits)	Register Functionality
A1050000	HGFCR	32	HIF Global Firmware Configuration Register
A1050004	HGFISR	32	HIF Global Firmware Interrupt Status Register
A1050008	HGFIER	32	HIF Global Firmware Interrupt Enable Register
A1050010	HSDBDLSR	32	HIF SDIO Bus Delay Selection Register
A1050014	HSDLSR	32	HIF SRAM Delay Selection Register
A1050018	HCSDCR	32	HIF Clock Stop Detection register
A105001C	HGH2DR	32	HIF Global Host to Device Register
A1050020	HDBGCR	32	HIF Debug Control Register
A105002C	FWDSIOCR	32	DS Pad Macro IO Control Register
A1050030	HGTMTCR	32	Test Mode Trigger Control Register
A1050034	HGTMCR	32	Test Mode Control Register
A1050038	HGTMDPCR0	32	Test Mode Data Pattern Control Register 0
A105003C	HGTMDPCR1	32	Test Mode Data Pattern Control Register 1
A1050040	FWCLKIOCR_T28LP	32	Clock Pad Macro IO Control Register
A1050044	FWCMDIOCR_T28LP	32	Command Pad Macro IO Control Register
A1050048	FWDAT0IOCR_T28LP	32	Data 0 Pad Macro IO Control Register
A105004C	FWDAT1IOCR_T28LP	32	Data 1 Pad Macro IO Control Register
A1050050	FWDAT2IOCR_T28LP	32	Data 2 Pad Macro IO Control Register
A1050054	FWDAT3IOCR_T28LP	32	Data 3 Pad Macro IO Control Register
A1050058	FWCLKDLYCR	32	Clock Pad Macro Delay Chain Control Register
A105005C	FWCMDDLYCR	32	Command Pad Macro Delay Chain Control Register
A1050060	FWODATDLYCR	32	SDIO Output Data Delay Chain Control Register
A1050064	FWIDATDLYCR1	32	SDIO Input Data Delay Chain Control Register 1
A1050068	FWIDATDLYCR2	32	SDIO Input Data Delay Chain Control Register 2
A105006C	FWILCHCR	32	SDIO Input Data Latch Time Control Register

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A1050070	**CIS0R00**	32	**CIS0 Register 0**
A1050074	**CIS0R01**	32	**CIS0 Register 1**
A1050078	**CIS0R02**	32	**CIS0 Register 2**
A105007C	**CIS0R03**	32	**CIS0 Register 3**
A1050080	**CIS0R04**	32	**CIS0 Register 4**
A1050084	**CIS0R05**	32	**CIS0 Register 5**
A1050088	**CIS0R06**	32	**CIS0 Register 6**
A105008C	**CIS0R07**	32	**CIS0 Register 7**
A1050090	**CIS0R08**	32	**CIS0 Register 8**
A1050094	**CIS0R09**	32	**CIS0 Register 9**
A1050098	**CIS0R0A**	32	**CIS0 Register A**
A105009C	**CIS0R0B**	32	**CIS0 Register B**
A10500A0	**CIS0R0C**	32	**CIS0 Register C**
A10500A4	**CIS0R0D**	32	**CIS0 Register D**
A10500A8	**CIS0R0E**	32	**CIS0 Register E**
A10500AC	**CIS0R0F**	32	**CIS0 Register F**
A10500B0	**CIS1R00**	32	**CIS1 Register 0**
A10500B4	**CIS1R01**	32	**CIS1 Register 1**
A10500B8	**CIS1R02**	32	**CIS1 Register 2**
A10500BC	**CIS1R03**	32	**CIS1 Register 3**
A10500C0	**CIS1R04**	32	**CIS1 Register 4**
A10500C4	**CIS1R05**	32	**CIS1 Register 5**
A10500C8	**CIS1R06**	32	**CIS1 Register 6**
A10500CC	**CIS1R07**	32	**CIS1 Register 7**
A10500D0	**CIS1R08**	32	**CIS1 Register 8**
A10500D4	**CIS1R09**	32	**CIS1 Register 9**
A10500D8	**CIS1R0A**	32	**CIS1 Register A**
A10500DC	**CIS1R0B**	32	**CIS1 Register B**
A10500E0	**CIS1R0C**	32	**CIS1 Register C**
A10500E4	**CIS1R0D**	32	**CIS1 Register D**
A10500E8	**CIS1R0E**	32	**CIS1 Register E**
A10500EC	**CIS1R0F**	32	**CIS1 Register F**
A10500F0	**CISRDY**	32	**CIS Ready Flag Register**
A10500F4	**CCCR0**	32	**CC Register 0**
A10500F8	**CCCR1**	32	**CC Register 1**
A10500FC	**CCRDY**	32	**CC Ready Flag Register**
A1050100	**HWFISR**	32	**HIF WLAN Firmware Interrupt Status Register**
A1050104	**HWFIER**	32	**HIF WLAN Firmware Interrupt Enable Register**
A1050108	**HWFISR1**	32	**Reserved for HWFISR1**
A105010C	**HWFIER1**	32	**Reserved for HWFIER1**

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A1050110	**HWFTE0SR**	32	**HIF WLAN Firmware TX Event 0 Status Register**
A1050114	**HWFTE1SR**	32	**Reserved for HWFTE1SR**
A1050118	**HWFTE2SR**	32	**Reserved for HWFTE2SR**
A105011C	**HWFTE3SR**	32	**Reserved for HWFTE3SR**
A1050120	**HWFTE0ER**	32	**HIF WLAN Firmware TX Event 0 Enable Register**
A1050124	**HWFTE1ER**	32	**Reserved for HWFTE1ER**
A1050128	**HWFTE2ER**	32	**Reserved for HWFTE2ER**
A105012C	**HWFTE3ER**	32	**Reserved for HWFTE3ER**
A1050130	**HWFRE0SR**	32	**HIF WLAN Firmware RX Event 0 Status Register**
A1050134	**HWFRE1SR**	32	**HIF WLAN Firmware RX Event 1 Status Register**
A1050138	**HWFRE2SR**	32	**Reserve for HWFRE2SR**
A105013C	**HWFRE3SR**	32	**Reserve for HWFRE3SR**
A1050140	**HWFRE0ER**	32	**HIF WLAN Firmware RX Event 0 Enable Register**
A1050144	**HWFRE1ER**	32	**HIF WLAN Firmware RX Event 1 Enable Register**
A1050148	**HWFRE2ER**	32	**Reserve for HWFRE2ER**
A105014C	**HWFRE3ER**	32	**Reserve for HWFRE3ER**
A1050150	**HWFICR**	32	**HIF WLAN Firmware Interrupt Control Register**
A1050154	**HWFCR**	32	**HIF WLAN Firmware Control Register**
A1050158	**HWTDCR**	32	**HIF WLAN TX DMA Control Register**
A105015C	**HWTPCCR**	32	**HIF WLAN TX Packet Count Control Register**
A1050160	**HWFTQ0SAR**	32	**HIF WLAN Firmware TX Queue 0 Start Address Register**
A1050164	**HWFTQ1SAR**	32	**HIF WLAN Firmware TX Queue 1 Start Address Register**
A1050168	**HWFTQ2SAR**	32	**HIF WLAN Firmware TX Queue 2 Start Address Register**
A105016C	**HWFTQ3SAR**	32	**HIF WLAN Firmware TX Queue 3 Start Address Register**
A1050170	**HWFTQ4SAR**	32	**HIF WLAN Firmware TX Queue 4 Start Address Register**
A1050174	**HWFTQ5SAR**	32	**Reserved for HIF WLAN Firmware TX Queue 5 Start Address Register**
A1050178	**HWFTQ6SAR**	32	**Reserved for HIF WLAN Firmware TX Queue 6 Start Address Register**
A105017C	**HWFTQ7SAR**	32	**Reserved for HIF WLAN Firmware TX Queue 7 Start Address Register**
A1050180	**HWFRQ0SAR**	32	**HIF WLAN Firmware RX Queue 0 Start Address Register**

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A1050188	HWFRQ2SAR	32	HIF WLAN Firmware RX Queue 2 Start Address Register
A105018C	HWFRQ3SAR	32	HIF WLAN Firmware RX Queue 3 Start Address Register
A1050190	HWFRQ4SAR	32	Reserve for HIF WLAN Firmware RX Queue 4 Start Address Register
A1050194	HWFRQ5SAR	32	Reserve for HIF WLAN Firmware RX Queue 5 Start Address Register
A1050198	HWFRQ6SAR	32	Reserved for HIF WLAN Firmware RX Queue 6 Start Address Register
A105019C	HWFRQ7SAR	32	Reserved for HIF WLAN Firmware RX Queue 7 Start Address Register
A10501A0	H2DRM0R	32	Host to Device Receive Mailbox 0 Register
A10501A4	H2DRM1R	32	Host to Device Receive Mailbox 1 Register
A10501A8	D2HSM0R	32	Device to Host Send Mailbox 0 Register
A10501AC	D2HSM1R	32	Device to Host Send Mailbox 1 Register
A10501B0	D2HSM2R	32	Device to Host Send Mailbox 2 Register
A10501C0	HWRQ0CR	32	HIF WLAN RX Queue 0 Control Register
A10501C4	HWRQ1CR	32	HIF WLAN RX Queue 1 Control Register
A10501C8	HWRQ2CR	32	HIF WLAN RX Queue 2 Control Register
A10501CC	HWRQ3CR	32	HIF WLAN RX Queue 3 Control Register
A10501D0	HWRQ4CR	32	Reserved for HWRQ4CR
A10501D4	HWRQ5CR	32	Reserved for HWRQ5CR
A10501D8	HWRQ6CR	32	Reserved for HWRQ6CR
A10501DC	HWRQ7CR	32	Reserved for HWRQ7CR
A10501E0	HWRLFACR	32	HIF WLAN RX Length FIFO Available Count Register
A10501E4	HWRLFACR1	32	Reserved for HWRLFACR1
A10501E8	HWDMACR	32	HIF WLAN DMA Control Register
A10501EC	HWFIOCDR	32	HIF WLAN Firmware GPD IOC Bit Disable Register
A10501F0	HSDIOTOCR	32	HIF SDIO Time-Out Control Register
A1050200	HWFTSR0	32	HIF WLAN Firmware TX Status Register 0
A1050204	HWFTSR1	32	HIF WLAN Firmware TX Status Register 1
A1050210	HWDBGCR	32	HIF WLAN Debug Control Register
A1050214	HWDBGPLR	32	HIF WLAN Debug Packet Length Register
A1050218	HSPICSR	32	WLAN SPI Control Status Register (SPI Only)
A1050220	HWRX0CGPD	32	DMA RX0 Current GPD Address Register
A1050224	HWRX1CGPD	32	DMA RX1 Current GPD Address Register
A1050228	HWRX2CGPD	32	DMA RX2 Current GPD Address Register
A105022C	HWRX3CGPD	32	DMA RX3 Current GPD Address Register

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A1050230	HWTX0CGPD	32	DMA TX0 Current GPD Address Register
A1050234	HWTX1Q1CGPD	32	DMA TX1 Queue Type 1 Current GPD Address Register
A1050238	HWTX1Q2CGPD	32	DMA TX1 Queue Type 2 Current GPD Address Register
A105023C	HWTX1Q3CGPD	32	DMA TX1 Queue Type 3 Current GPD Address Register
A1050240	HWTX1Q4CGPD	32	DMA TX1 Queue Type 4 Current GPD Address Register
A1050244	HWTX1Q5CGPD	32	DMA TX1 Queue Type 5 Current GPD Address Register
A1050248	HWTX1Q6CGPD	32	DMA TX1 Queue Type 6 Current GPD Address Register
A105024C	HWTX1Q7CGPD	32	DMA TX1 Queue Type 7 Current GPD Address Register
A10503F4	HSDIOCRCR	32	HIF SDIO CRC Status Register
A10503F8	HSDIORCR	32	HIF SDIO Read Control Register

A1050000 HGFCR **HIF Global Firmware Configuration Register** **40020041**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SW_SEL_CLKBLC	SW_SET_CLK_NONBLC	PAD_CR_SET_BY_FW	PB_HCLK_DIS	EHPI_HCLK_DIS	SPI_HCLK_DIS	SDIO_HCLK_DIS						FORCE_SD_HS	HCLK_NO_GATED	INT_TER_CYC_MASK
Type		RW	RW	RW	RW	RW	RW	RW						RW	RW	RW
Reset		1	0	0	0	0	0	0						0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SDCTL_BUSY	CARD_IS_18V	HINT_AS_FW_OB		SDIO_PIO_SEL	EHPI_MODE	SPI_MODE		DB_HIF_SEL		
Type						RO	RW	RW		RO	RO	RO		RO		
Reset						0	0	0		1	0	0		0	0	1

Bit(s)	Name	Description
30	SW_SEL_CLKBLC	Software enables this bit to take over balance and non-balance SD clock control for pad macro. The need for non-balance SD clock for pad macro is due to tight output timing specifications. The default setting is controlled by hardware to decide the clock balance. However, the software is flexible to determine the balance or non-balance clock tree for the SDIO pad macro.

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		• 0: The balance/non-balance SD clock for pad macro is controlled by hardware. • 1: The balance/non-balance SD clock for pad macro is controlled by software.
29	SW_SET_CLK_NONBLC	**Software enables this bit to use balance and non-balance SD clock for pad macro.** • 0: Use balance SD clock for pad macro. • 1: Use non-balance SD clock for pad macro.
28	PAD_CR_SET_BY_FW	**Enable the pad macro control register test mode. Firmware writes this bit and then gets the ownership to access the pad macro control registers.** • 0: Pad macro control register set by the host driver (normal mode). • 1: Pad macro control register set by the firmware (test mode).
27	PB_HCLK_DIS	**Used to disable the AHB clock for PIO-based function design. It is set when PIO-based function is not used in some specific configurations. Otherwise, the PIO-based function might fail.** • 0: AHB clock is not disabled. • 1: Disable AHB clock.
26	EHPI_HCLK_DIS	**Used to disable the AHB clock for EHPI interface. It would be set when EHPI is not used in some specific configuration. Otherwise, the EHPI operation will fail.** • 0: AHB clock is not disabled. • 1: Disable AHB clock.
25	SPI_HCLK_DIS	**Used to disable the AHB clock for SPI interface. It would be set when SPI is not used in some specific configurations. Otherwise, the SPI operation will fail.** • 0: AHB clock is not disabled. • 1: Disable AHB clock.
24	SDIO_HCLK_DIS	**Used to disable the AHB clock for SDIO1 interface. It would be set when SDIO is not used in some specific configurations. Otherwise, the SDIO operation will fail.** • 0: AHB clock is not disabled. • 1: Disable AHB clock.
18	FORCE_SD_HS	**Note, that the card can operate in high-speed mode using an external eFUSE or read or write interface to enable this function according to IP configuration.** • 0: SDIO is in the operation mode specified in EHS of CCCR. • 1: FORCE SDIO to operate in high-speed mode despite the values of EHS of CCCR.
17	HCLK_NO_GATED	• 0: SDIO controller will automatically close the AHB clock for the DMA function (if it's not in use) by the clock gating cell. • 1: The AHB clock inside SDIO controller is always on.
16	INT_TER_CYC_MASK	**This field is used to determine whether SDIO should drive**

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		high to bus bit1 during the interrupt termination cycle. • 0: Always drive high during the termination cycle. • 1: Drive high during the termination cycle only if it is in interrupt period.
10	SDCTL_BUSY	**Indicates whether SDIO controller is busy.** • 0: SDIO controller is not busy. • 1: SDIO controller is still busy.
9	CARD_IS_18V	**Firmware writes 1 to this field to indicate the voltage has switched and if the card is in 1.8V state.** • 0: Card is not in 1.8V state. • 1: Card is in 1.8V state (UHS mode).
8	HINT_AS_FW_OB	**Use an interrupt to host as a firmware ownership back control** • 0: Interrupt to host will not trigger back the firmware ownership • 1: Interrupt to host will trigger firmware ownership back
6	SDIO_PIO_SEL	**Host interface for SDIO PIO-based function is used.** • 0: SDIO PIO mode is not used. • 1: SDIO PIO mode is used.
5	EHPI_MODE	**This bit indicates if EHPI8-mode or EHPI16-mode is used.** • 0: EHPI16-mode of EHPI is used. • 1: EHPI8-mode of EHPI is used.
4	SPI_MODE	**This bit indicates if TI-mode or Motor-mode is used.** • 0: Motor-mode of SPI is used. • 1: TI-mode of SPI is used.
2:0	DB_HIF_SEL	**Host interface for DMA-based function is used;** • 0x1: SDIO1 • 0x2: SPI • 0x4: EHPI

A1050004 HGFISR **HIF Global Firmware Interrupt Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SD1_SET_DS_INT	SD1_SET_XTAL_UPD_INT	CHG_TO_18V_REQ_INT	CRC_ERROR_INT	PB_INT	DB_INT	SDIO_SET_ABT	SDIO_SET_RES	DRV_SET_PB_IOE	DRV_SET_DB_IOE	DRV_CLR_PB_IOE	DRV_CLR_DB_IOE

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Type					W1C	W1C	W1C	W1C	RO	RO	W1C	W1C	W1C	W1C	W1C	W1C
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	SD1_SET_DS_INT	**This bit is for SDIO interface only.** If the CCCR deep sleep register is set by the host, this bit will be set, too. Once the firmware detects this event, it will set the device to deep sleep mode. Firmware can clear this bit by writing 1. Writing 0 does nothing.
10	SD1_SET_XTAL_UPD_INT	**This bit is for SDIO interface only.** If the CCCR XTAL frequency update register is set in the host, this bit will be set, too. Once the firmware detects this event, it will know that the host has updated the XTAL frequency. Firmware can then read HGH2DR to find the updated frequency value. Firmware can clear this bit by writing 1. Writing 0 does nothing.
9	CHG_TO_18V_REQ_INT	**Host sends command 11 to request the device to change the voltage to 1.8V. Firmware receives an interrupt or polling status to switch the voltage. Then the firmware writes the card is in 1.8V status to HGFCR.**
8	CRC_ERROR_INT	**The status bit of TX data port CRC error interrupt.**
7	PB_INT	**The status bit of PIO-based function firmware interrupt.**
6	DB_INT	**The status bit of DMA-based function firmware interrupt.**
5	SDIO_SET_ABT	**SDIO writes 1 to SDIO CCCR.ABORT to abort the transaction. Once the firmware detects this event, the TX and RX queues are stopped and the data in the buffer is discarded.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
4	SDIO_SET_RES	**SDIO writes 1 to SDIO CCCR.RES to assert software reset. Once the firmware detects this event, it disables the sub-systems on SDIO interface.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
3	DRV_SET_PB_IOE	**This bit is for SDIO interface only.** This bit is set if the host sets the CCCR.IOE bit of PIO-based functional block. Once the firmware detects this event, it enables the subsystem that uses a PIO-based function. Firmware can clear this bit by writing 1. Writing 0 does nothing.
2	DRV_SET_DB_IOE	**This bit is for SDIO interface only.** This bit is set if the host sets the CCCR.IOE bit of DMA-based functional block. Once the firmware detects this event, it enables the subsystem that uses a DMA-based function. Firmware can clear this bit by writing 1. Writing 0 does nothing.
1	DRV_CLR_PB_IOE	**This bit is for SDIO interface only.** This bit is set, if the host clears the CCCR.IOE bit of PIO-based functional block. Once the firmware detects this event, it disables the subsystem that uses a PIO-based function. Firmware can clear this bit by writing 1. Writing 0 does nothing.
0	DRV_CLR_DB_IOE	**This bit is for SDIO interface only.**

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		This bit is set if the host clears the CCCR.IOE bit of DMA-based functional block. Once the firmware detects this event, it disables the subsystem that uses a DMA-based function. Firmware can clear this bit by writing 1. Writing 0 does nothing.

A1050008 HGFIER **HIF Global Firmware Interrupt Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SD1_SET_DS_INT_EN	SD1_SET_XTAL_UPD_INT_EN	CHG_TO_18V_REQ_INT_EN	CRC_ERROR_INT_EN	PB_INT_EN	DB_INT_EN	SDIO_SET_ABT_INT_EN	SDIO_SET_RES_INT_EN	DRV_SET_PB_IOE_INT_EN	DRV_SET_DB_IOE_INT_EN	DRV_CLR_PB_IOE_INT_EN	DRV_CLR_DB_IOE_INT_EN
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11	SD1_SET_DS_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is • 0: Disable the interrupt output. • 1: Enable the interrupt output.
10	SD1_SET_XTAL_UPD_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is • 0: Disable the interrupt output. • 1: Enable the interrupt output.
9	CHG_TO_18V_REQ_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is • 0: Disable the interrupt output. • 1: Enable the interrupt output.
8	CRC_ERROR_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is • 0: Disable the interrupt output. • 1: Enable the interrupt output.
7	PB_INT_EN	**Common firmware interrupt output control for each bit**

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		corresponding to bits defined in HGFISR. If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
6	DB_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
5	SDIO_SET_ABT_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
4	SDIO_SET_RES_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
3	DRV_SET_PB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
2	DRV_SET_DB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
1	DRV_CLR_PB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.
0	DRV_CLR_DB_IOE_INT_EN	**Common firmware interrupt output control for each bit corresponding to bits defined in HGFISR.** If the related bit is ● 0: Disable the interrupt output. ● 1: Enable the interrupt output.

A1050010 HSDBDLSR HIF SDIO Bus Delay Selection Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SD1_DAT3_DELSEL				SD1_DAT2_DELSEL				SD1_DAT1_DELSEL				SD1_DAT0_DELSEL		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Bit(s)	Name	Description
14:12	SD1_DAT3_DELSEL	**It is used to tune the SDIO1 bit3 bus delay for desensitization** • 7: about 1.4ns. • 6: about 1.2ns. • 5: about 1.0ns. • 4: about 0.8ns. • 3: about 0.6ns. • 2: about 0.4ns. • 1: about 0.2ns. • 0: no delay.
10:8	SD1_DAT2_DELSEL	**It is used to tune the SDIO1 bit2 bus delay for desensitization (bit 2)** • 7: about 1.4ns. • 6: about 1.2ns. • 5: about 1.0ns. • 4: about 0.8ns. • 3: about 0.6ns. • 2: about 0.4ns. • 1: about 0.2ns. • 0: no delay.
6:4	SD1_DAT1_DELSEL	**It is used to tune the SDIO1 bit1 bus delay for desensitization** • 7: about 1.4ns. • 6: about 1.2ns. • 5: about 1.0ns. • 4: about 0.8ns. • 3: about 0.6ns. • 2: about 0.4ns. • 1: about 0.2ns. • 0: no delay
2:0	SD1_DAT0_DELSEL	**It is used to tune the SDIO1 bit0 bus delay for desensitization** • 7: about 1.4ns. • 6: about 1.2ns.

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		• 5: about 1.0ns • 4: about 0.8ns • 3: about 0.6ns. • 2: about 0.4ns. • 1: about 0.2ns. • 0: no delay

A1050014 HSDLSR HIF SRAM Delay Selection Register 00000F0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					PB_DELSEL_3_2		PB_DELSEL_1_0						DB_DELSEL_3_2		DB_DELSEL_1_0	
Type					RW		RW						RW		RW	
Reset					1	1	1	1					1	0	1	0

Bit(s)	Name	Description
11:10	PB_DELSEL_3_2	**Delay selection of SRAM of PIO-based part of SDIO controller** Note, that the default value is different for different processes.
9:8	PB_DELSEL_1_0	**Delay selection of SRAM of PIO-based part of SDIO controller** Note, that the default value is different for different processes.
3:2	DB_DELSEL_3_2	**Delay selection of SRAM of DMA-based part of SDIO controller** Note, that the default value is different for different processes.
1:0	DB_DELSEL_1_0	**Delay selection of SRAM of DMA-based part of SDIO controller** Note, that the default value is different for different processes.

A1050018 HCSDCR HIF Clock Stop Detection register 0000FDE8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SDCLK_STOP_NUM			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SDCLK_STOP_NUM															
Type	RW															
Reset	1	1	1	1	1	1	0	1	1	1	1	0	1	0	0	0

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Bit(s)	Name	Description
19:0	SDCLK_STOP_NUM	For SDIO 3.0 design, host driver needs to issue CMD11 to switch the voltage to 1.8V to enter UHS mode. This field is to set the hardware timer threshold for SDIO hardware to determine whether the SD clock has stopped. According to SDIO 3.0 specifications, the host should stop the clock at least 5ms for the device to switch the voltage from 3.3V to 1.8V. The unit of this field is based on the AHB clock cycle number.

A105001C HGH2DR HIF Global Host to Device Register 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														XTAL_FREQ		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	XTAL_FREQ	The host can write this CCCR vendor unique register to update the XTAL frequency information for firmware. When the host writes 1 to this field, hardware would send an interrupt to firmware to notify that the host has updated the XTAL frequency. Firmware can read the firmware domain HGH2DR register to derive the XTAL frequency that is updated through a command sent from the host.

A1050020 HDBGCR HIF Debug Control Register 11110000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEBUG_MONH								DEBUG_MONL							
Type	RO								RO							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FLAG_HSEL								FLAG_LSEL							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	DEBUG_MONH	**Debug flag monitor for High byte** Shows the flag value specified in FLAG_HSEL.
23:16	DEBUG_MONL	**Debug flag monitor for Low byte** Shows the flag value specified in FLAG_LSEL.

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Bit(s)	Name	Description
15:8	FLAG_HSEL	**Flag number of High byte for debug** Selects the flag to debug in high byte.
7:0	FLAG_LSEL	**Flag number of Low byte for debug** Selects the flag to debug in low byte.

A105002C FWDSIOCR DS Pad Macro IO Control Register 80000422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DS_RESP_EN		DS_RDSEL										DS_TDSEL			
Type	RW		RW										RW			
Reset	1		0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DS_E8E4E2					DS_SMT	DS_PUPD	DS_R1	DS_R0	DS_IES	DS_SR
Type						RW					RW	RW	RW	RW	RW	RW
Reset						1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
31	DS_RESP_EN	**HS400 mode response DS toggle enable bit** 0: Response DS toggle disable 1: Response DS toggle enable
29:24	DS_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DS_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
10:8	DS_E8E4E2	**TX Driving Strength Control.**
5	DS_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DS_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor CLK pad default no pull
3	DS_R1	**Select 50K resistor (0: not select, 1: select)**
2	DS_R0	**Select 10K resistor (0: not select, 1: select)**
1	DS_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DS_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

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A1050030 HGTMTCR Test Mode Trigger Control Register 00001300

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**TM_BUS_WIDTH**		**TM_BSS**									**FW_TRIGGER_CRC_STS**	**FW_TRIGGER_TM_DATA**
Type				RW		RW									RW	RW
Reset				1	0	0	1	1							0	0

Bit(s)	Name	Description
12:11	TM_BUS_WIDTH	**For Test Mode, set the bus width of SDIO bus interface** 0x0: SD1-bit 0x1: Reserved 0x2: SD4-bit 0x3: SD8-bit
10:8	TM_BSS	**For Test Mode, set the bus speed of SDIO bus interface** 0x0: SDR12 0x1: SDR25 0x2: SDR50 0x3: SDR104 0x4: DDR50
1	FW_TRIGGER_CRC_STS	**For Test Mode: Send a good CRC status after firmware trigger is enabled. The firmware polls this bit to make it 0 to trigger another event.** 0: Disable SDIO Device Send CRC Status 1: Enable SDIO Device Send CRC Status
0	FW_TRIGGER_TM_DATA	**For Test Mode: Send a specific response and block data after firmware trigger is enabled. The firmware polls this bit to make it 0 to trigger another event.** Note, that the content is configured similar to the host initiated pattern generation 0: Disable SDIO Device Send Response and block data. 1: Enable SDIO Device Send Response and block data.

A1050034 HGTMCR Test Mode Control Register 00080000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**TEST_MODE_FW_OWN**	**PRBS_INIT_VAL**							
Type								RW	RW							

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Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**TEST_MODE_STATUS**							**TEST_MODE_SELECT**	
Type								RO							RW	
Reset								0							0	0

Bit(s)	Name	Description
24	TEST_MODE_FW_OWN	**Indicates the ownership of Test Mode Control Register : WTMCR,WTMDPCR0,WTMDPCR1** 0: Host has the ownership. 1: Firmware has the ownership.
23:16	PRBS_INIT_VAL	**Initial Value For PRBS generator**
8	TEST_MODE_STATUS	**To record the comparison result of the latest Test Mode write operation.** 0: Data comparison of Test Mode write is Pass 1: Data comparison of Test Mode write is Fail
1:0	TEST_MODE_SELECT	**Select the test mode data pattern** -64-bits configurable data register (WTMDPCR0:WTMDPCR1) -32-bits configurable data register -PRBS 00: the 32bit data pattern 01: the 64bit data pattern 10: the PRBS data pattern 11: reserved

A1050038 HGTMDPCR0 Test Mode Data Pattern Control Register 0 F0F0F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TEST_MODE_DATA_PATTERN_0**															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TEST_MODE_DATA_PATTERN_0**															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	TEST_MODE_DATA_PATTERN_0	**Data pattern for Test Mode read**

A105003C HGTMDPCR1 Test Mode Data Pattern Control Register 1 F0F0F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TEST_MODE_DATA_PATTERN_1															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST_MODE_DATA_PATTERN_1															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	TEST_MODE_DATA_PATTERN_1	**Data pattern for Test Mode write**

A1050040 FWCLKIOCR_T28LP Clock Pad Macro IO Control Register 00000422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CLK_RDSEL										CLK_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						CLK_E8E4E2					CLK_SMT	CLK_PUPD	CLK_R1	CLK_R0	CLK_IES	CLK_SR
Type						RW					RW	RW	RW	RW	RW	RW
Reset						1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	CLK_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	CLK_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
10:8	CLK_E8E4E2	**TX Driving Strength Control.**
5	CLK_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	CLK_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor CLK pad default no pull
3	CLK_R1	**Select 50K resistor (0: not select, 1: select)**
2	CLK_R0	**Select 10K resistor (0: not select, 1: select)**
1	CLK_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	CLK_SR	**Output Slew Rate Control. High asserted.**

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Bit(s)	Name	Description
		SR=1, slower slew. SR=0, no slew rate controlled.

A1050044 FWCMDIOCR_T28LP Command Pad Macro IO Control Register 00000422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CMD_RDSEL										CMD_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_CMD_SAMPLE		CMD_E8E4E2					CMD_SMT	CMD_PUPD	CMD_R1	CMD_R0	CMD_IES	CMD_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	CMD_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	CMD_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_CMD_SAMPLE	**Select clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input command 1: Use negative SD clock edge to latch input command
10:8	CMD_E8E4E2	**TX Driving Strength Control.**
5	CMD_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	CMD_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor CMD pad default no pull
3	CMD_R1	**Select 50K resistor (0: not select, 1: select)**
2	CMD_R0	**Select 10K resistor (0: not select, 1: select)**
1	CMD_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	CMD_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

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A1050048 FWDAT0IOCR_T28LP Data 0 Pad Macro IO Control Register 00000422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA0_RDSEL										DATA0_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_DATA0_SAMPLE		DATA0_E8E4E2					DATA0_SMT	DATA0_PUPD	DATA0_R1	DATA0_R0	DATA0_IES	DATA0_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DATA0_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA0_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_DATA0_SAMPLE	**Select clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 0 1: Use negative SD clock edge to latch input data 0
10:8	DATA0_E8E4E2	**TX Driving Strength Control.**
5	DATA0_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA0_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 0 pad default no pull
3	DATA0_R1	**Select 50K resistor (0: not select, 1: select)**
2	DATA0_R0	**Select 10K resistor (0: not select, 1: select)**
1	DATA0_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA0_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

A105004C FWDAT1IOCR_T28LP Data 1 Pad Macro IO Control Register 00000422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA1_RDSEL										DATA1_TDSEL			
Type			RW										RW			

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Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**REG_DATA1_SAMPLE**		**DATA1_E8E4E2**					**DATA1_SMT**	**DATA1_PUPD**	**DATA1_R1**	**DATA1_R0**	**DATA1_IES**	**DATA1_SR**
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DATA1_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA1_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_DATA1_SAMPLE	**Select clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 1 1: Use negative SD clock edge to latch input data 1
10:8	DATA1_E8E4E2	**TX Driving Strength Control.**
5	DATA1_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA1_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 1 pad default no pull
3	DATA1_R1	**Select 50K resistor (0: not select, 1: select)**
2	DATA1_R0	**Select 10K resistor (0: not select, 1: select)**
1	DATA1_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA1_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

A1050050 FWDAT2IOCR_T28LP Data 2 Pad Macro IO Control Register 00000422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**DATA2_RDSEL**										**DATA2_TDSEL**			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**REG_DATA**		**DATA2_E8E4E2**					**DATA2_SM**	**DATA2_PU**	**DATA2_R1**	**DATA2_R0**	**DATA2_IES**	**DATA2_SR**

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				2_SAMPLE							T	PD				
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DATA2_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA2_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted(low pulse width adjustment)
12	REG_DATA2_SAMPLE	**Select clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 2 1: Use negative SD clock edge to latch input data 2
10:8	DATA2_E8E4E2	**TX Driving Strength Control.**
5	DATA2_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA2_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 2 pad default no pull
3	DATA2_R1	**Select 50K resistor (0: not select, 1: select)**
2	DATA2_R0	**Select 10K resistor (0: not select, 1: select)**
1	DATA2_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA2_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

A1050054 FWDAT3IOCR_T28LP Data 3 Pad Macro IO Control Register 0000042A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA3_RDSEL										DATA3_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_DATA3_SAMPLE		DATA3_E8E4E2					DATA3_SMT	DATA3_PUPD	DATA3_R1	DATA3_R0	DATA3_IES	DATA3_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	1	0	1	0

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Bit(s)	Name	Description
29:24	DATA3_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA3_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_DATA3_SAMPLE	**Select clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 3 1: Use negative SD clock edge to latch input data 3
10:8	DATA3_E8E4E2	**TX Driving Strength Control.**
5	DATA3_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA3_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 3 pad default would pull up with 50K resistor. (for card detection) After host driver writes cd_disable to CCCR register, data 3 pad would become no pull.
3	DATA3_R1	**Select 50K resistor (0: not select, 1: select)**
2	DATA3_R0	**Select 10K resistor (0: not select, 1: select)**
1	DATA3_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA3_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

A1050058 FWCLKDLYCR Clock Pad Macro Delay Chain Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									REG_CK_DLY_EN			CLK_DLY_SEL				
Type									RW			RW				
Reset									0			0	0	0	0	0

Bit(s)	Name	Description
7	REG_CK_DLY_EN	**Enables input clock through delay chain.**

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Bit(s)	Name	Description
4:0	CLK_DLY_SEL	0: Input clock does not pass through delay chain. 1: Input clock pass through delay chain. **Clock (CLK) Pad Input Delay Control** This register is used to add delay to CLK phase. Total 32 stages

A105005C FWCMDDLYCR Command Pad Macro Delay Chain Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REG_CMD_O_DLY_EN	REG_CMD_OE_DLY_EN		CMD_O_DLY				
Type									RW	RW		RW				
Reset									0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_CMD_NEG_I_DLY_EN			CMD_NEG_I_DLY					REG_CMD_POS_I_DLY_EN			CMD_POS_I_DLY				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
23	REG_CMD_O_DLY_EN	**Enable output response through delay chain. (to I of IOCUP)** 0: Output response does not pass through delay chain. 1: Output response passes through delay chain.
22	REG_CMD_OE_DLY_EN	**Enable response output enable through delay chain. (to E of IOCUP)** 0: Response output enable does not pass through delay chain. 1: Response output enable passes through delay chain.
20:16	CMD_O_DLY	**Command (CMD) Pad Output Delay Control** This register is used to add delay to an output response phase. Total of 32 stages
15	REG_CMD_NEG_I_DLY_EN	**Enables input command through delay chain to be latched with negative clock edge.** 0: Input command does not pass through delay chain. 1: Input command passes through delay chain.
12:8	CMD_NEG_I_DLY	**CMD Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input command phase. Total of 32 stages
7	REG_CMD_POS_I_DLY_EN	**Enables input command through delay chain to be latched with positive clock edge.** 0: Input command does not pass through delay chain. 1: Input command passes through delay chain.
4:0	CMD_POS_I_DLY	**CMD Pad Input Delay Control for data latch with positive**

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Bit(s)	Name	Description
		clock edge. This register is used to add delay to an input command phase. Total of 32 stages

A1050060 FWODATDLYCR SDIO Output Data Delay Chain Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_DAT3_O_DLY_EN	REG_DAT3_OE_DLY_EN		DAT3_O_DLY					REG_DAT2_O_DLY_EN	REG_DAT2_OE_DLY_EN		DAT2_O_DLY				
Type	RW	RW		RW					RW	RW		RW				
Reset	0	0		0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_DAT1_O_DLY_EN	REG_DAT1_OE_DLY_EN		DAT1_O_DLY					REG_DAT0_O_DLY_EN	REG_DAT0_OE_DLY_EN		DAT0_O_DLY				
Type	RW	RW		RW					RW	RW		RW				
Reset	0	0		0	0	0	0	0	0	0		0	0	0	0	0

Bit(s)	Name	Description
31	REG_DAT3_O_DLY_EN	**Enable output data 3 through delay chain. (to I of IOCUP)** 0: Output data 3 does not pass through delay chain. 1: Output data 3 passes through delay chain.
30	REG_DAT3_OE_DLY_EN	**Enables data 3 output enable through delay chain. (to E of IOCUP)** 0: Data 3 output enable does not pass through delay chain. 1: Data 3 output enable passes through delay chain.
28:24	DAT3_O_DLY	**DATA 3 Pad Output Delay Control** This register is used to add delay to output response phase. Total 32 stages
23	REG_DAT2_O_DLY_EN	**Enables output data 2 through delay chain. (to I of IOCUP)** 0: Output data 2 does not pass through delay chain. 1: Output data 2 passes through delay chain.
22	REG_DAT2_OE_DLY_EN	**Enables data 2 output enable through delay chain. (to E of IOCUP)** 0: Data 2 output enable does not pass through delay chain. 1: Data 2 output enable pass through delay chain.
20:16	DAT2_O_DLY	**DATA 2 Pad Output Delay Control** This register is used to add delay to output response phase. Total of 32 stages
15	REG_DAT1_O_DLY_EN	**Enables output data 1 through delay chain. (to I of IOCUP)** 0: Output data 1 does not pass through delay chain. 1: Output data 1 passes through delay chain.
14	REG_DAT1_OE_DLY_EN	**Enables data 1 output enable through delay chain. (to E of IOCUP)** 0: Data 1 output enable does not pass through delay chain. 1: Data 1 output enable passes through delay chain.

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Bit(s)	Name	Description
12:8	DAT1_O_DLY	**DATA 1 Pad Output Delay Control** This register is used to add delay to output response phase. Total of 32 stages
7	REG_DAT0_O_DLY_EN	**Enables output data 0 through delay chain. (to I of IOCUP)** 0: Output data 0 does not pass through delay chain. 1: Output data 0 passes through delay chain.
6	REG_DAT0_OE_DLY_EN	**Enables data 0 output enable through delay chain. (to E of IOCUP)** 0: Data 0 output enable does not pass through delay chain. 1: Data 0 output enable passes through delay chain.
4:0	DAT0_O_DLY	**DATA 0 Pad Output Delay Control** This register is used to add delay to output response phase. Total of 32 stages

A1050064 FWIDATDLYCR1 SDIO Input Data Delay Chain Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_DAT3_POS_I_DLY_EN			DAT3_POS_I_DLY					REG_DAT2_POS_I_DLY_EN			DAT2_POS_I_DLY				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_DAT1_POS_I_DLY_EN			DAT1_POS_I_DLY					REG_DAT0_POS_I_DLY_EN			DAT0_POS_I_DLY				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	REG_DAT3_POS_I_DLY_EN	**Enables input data 3 through delay chain to be latched with positive clock edge.** 0: Input data 3 does not pass through delay chain. 1: Input data 3 passes through delay chain.
28:24	DAT3_POS_I_DLY	**DATA 3 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 3 phase. Total of 32 stages
23	REG_DAT2_POS_I_DLY_EN	**Enables input data 2 through delay chain to be latched with positive clock edge.** 0: Input data 2 does not pass through delay chain. 1: Input data 2 passes through delay chain.
20:16	DAT2_POS_I_DLY	**DATA 2 Pad Input Delay Control for data latch with positive clock edge.**

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Bit(s)	Name	Description
		This register is used to add delay to input data 2 phase. Total of 32 stages
15	REG_DAT1_POS_I_DLY_EN	**Enables input data 1 through delay chain to be latched with positive clock edge.** 0: Input data 1 does not pass through delay chain. 1: Input data 1 passes through delay chain.
12:8	DAT1_POS_I_DLY	**DATA 1 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 1 phase. Total of 32 stages
7	REG_DAT0_POS_I_DLY_EN	**Enables input data 0 through delay chain to be latched with positive clock edge.** 0: Input data 0 does not pass through delay chain. 1: Input data 0 passes through delay chain.
4:0	DAT0_POS_I_DLY	**DATA 0 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 0 phase. Total of 32 stages

A1050068 FWIDATDLYCR2 SDIO Input Data Delay Chain Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_DAT3_NEG_I_DLY_EN			DAT3_NEG_I_DLY					REG_DAT2_NEG_I_DLY_EN			DAT2_NEG_I_DLY				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_DAT1_NEG_I_DLY_EN			DAT1_NEG_I_DLY					REG_DAT0_NEG_I_DLY_EN			DAT0_NEG_I_DLY				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	REG_DAT3_NEG_I_DLY_EN	**Enables input data 3 through delay chain to be latched with negative clock edge.** 0: Input data 3 does not pass through delay chain. 1: Input data 3 passes through delay chain.
28:24	DAT3_NEG_I_DLY	**DATA 3 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 3 phase. Total of 32 stages
23	REG_DAT2_NEG_I_DLY_EN	**Enables input data 2 through delay chain to be latched with negative clock edge.**

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Bit(s)	Name	Description
		0: Input data 2 does not pass through delay chain. 1: Input data 2 passes through delay chain.
20:16	DAT2_NEG_I_DLY	**DATA 2 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 2 phase. Total of 32 stages
15	REG_DAT1_NEG_I_DLY_EN	**Enables input data 1 through delay chain to be latched with negative clock edge.** 0: Input data 1 does not pass through delay chain. 1: Input data 1 passes through delay chain.
12:8	DAT1_NEG_I_DLY	**DATA 1 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 1 phase. Total of 32 stages
7	REG_DAT0_NEG_I_DLY_EN	**Enables input data 0 through delay chain to be latched with negative clock edge.** 0: Input data 0 does not pass through delay chain. 1: Input data 0 passes through delay chain.
4:0	DAT0_NEG_I_DLY	**DATA 0 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 0 phase. Total of 32 stages

A105006C **FWILCHCR** **SDIO Input Data Latch Time Control Register** **00011111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															REG_CMD_LATCH_SEL	
Type															RW	
Reset															0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			REG_DAT3_LATCH_SEL				REG_DAT2_LATCH_SEL				REG_DAT1_LATCH_SEL				REG_DAT0__LATCH_SEL	
Type			RW				RW				RW				RW	
Reset			0	1			0	1			0	1			0	1

Bit(s)	Name	Description
17:16	REG_CMD_LATCH_SEL	**Controls the input command latch timing based on the SDIO output enable signal to avoid latching device output data when host transfers data in UHS104 mode.** 2'b00: latch input command after 1 cycle of output enable is asserted. 2'b01: latch input command after 2 cycles of output enable is asserted 2'b10: latch input command after 3 cycles of output enable is asserted 2'b11: latch input command after 4 cycles of output enable is asserted
13:12	REG_DAT3_LATCH_SEL	**Controls the input data 3 latch timing based on the SDIO output enable signal to avoid latching device output data when host transfers data in UHS104 mode.** 2'b00: latch input data 3 after 1T of output enable asserted 2'b01: latch input data 3 after 2T of output enable asserted 2'b10: latch input data 3 after 3T of output enable asserted

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Bit(s)	Name	Description
		2'b11: latch input data 3 after 4T of output enable asserted
9:8	REG_DAT2_LATCH_SEL	**Control the input data 2 latch timing depending on SDIO output enable signal to avoid latching device output data when host transferred data in UHS104 mode.** 2'b00: latch input data 2 after 1T of output enable asserted 2'b01: latch input data 2 after 2T of output enable asserted 2'b10: latch input data 2 after 3T of output enable asserted 2'b11: latch input data 2 after 4T of output enable asserted
5:4	REG_DAT1_LATCH_SEL	**Control the input data 1 latch timing based on SDIO output enable signal to avoid latching device output data when host transfers data in UHS104 mode.** 2'b00: latch input data 1 after 1T of output enable asserted 2'b01: latch input data 1 after 2T of output enable asserted 2'b10: latch input data 1 after 3T of output enable asserted 2'b11: latch input data 1 after 4T of output enable asserted
1:0	REG_DAT0__LATCH_SEL	**Control the input data 0 latch timing based on SDIO output enable signal to avoid latching device output data when host transfers data in UHS104 mode.** 2'b00: latch input data 0 after 1T of output enable asserted 2'b01: latch input data 0 after 2T of output enable asserted 2'b10: latch input data 0 after 3T of output enable asserted 2'b11: latch input data 0 after 4T of output enable asserted

A1050070 CIS0R00 CIS0 Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W00	**CIS0 Register used in CISCC firmware register mode**

A1050074 CIS0R01 CIS0 Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	CIS0_W01	**CIS0 Register used in CISCC firmware register mode**

A1050078 CIS0R02 CIS0 Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W02	**CIS0 Register used in CISCC firmware register mode**

A105007C CIS0R03 CIS0 Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W03	**CIS0 Register used in CISCC firmware register mode**

A1050080 CIS0R04 CIS0 Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	CIS0_W04	**CIS0 Register used in CISCC firmware register mode**

A1050084 CIS0R05 CIS0 Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W05	**CIS0 Register used in CISCC firmware register mode**

A1050088 CIS0R06 CIS0 Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W06	**CIS0 Register used in CISCC firmware register mode**

A105008C CIS0R07 CIS0 Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W07	**CIS0 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A1050090 CIS0R08 CIS0 Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W08	**CIS0 Register used in CISCC firmware register mode**

A1050094 CIS0R09 CIS0 Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W09	**CIS0 Register used in CISCC firmware register mode**

A1050098 CIS0R0A CIS0 Register A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W0A															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W0A															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W0A	**CIS0 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A105009C CIS0R0B CIS0 Register B 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W0B															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W0B															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W0B	**CIS0 Register used in CISCC firmware register mode**

A10500A0 CIS0R0C CIS0 Register C 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W0C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W0C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W0C	**CIS0 Register used in CISCC firmware register mode**

A10500A4 CIS0R0D CIS0 Register D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W0D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W0D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W0D	**CIS0 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500A8 CIS0R0E **CIS0 Register E** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W0E															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W0E															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W0E	**CIS0 Register used in CISCC firmware register mode**

A10500AC CIS0R0F **CIS0 Register F** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS0_W0F															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS0_W0F															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS0_W0F	**CIS0 Register used in CISCC firmware register mode**

A10500B0 CIS1R00 **CIS1 Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W00															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W00	**CIS1 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500B4 CIS1R01 CIS1 Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W01															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W01	**CIS1 Register used in CISCC firmware register mode**

A10500B8 CIS1R02 CIS1 Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W02															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W02	**CIS1 Register used in CISCC firmware register mode**

A10500BC CIS1R03 CIS1 Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W03															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W03	**CIS1 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500C0 CIS1R04 CIS1 Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W04															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W04	**CIS1 Register used in CISCC firmware register mode**

A10500C4 CIS1R05 CIS1 Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W05															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W05	**CIS1 Register used in CISCC firmware register mode**

A10500C8 CIS1R06 CIS1 Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W06															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W06	**CIS1 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500CC CIS1R07 CIS1 Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W07															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W07	**CIS1 Register used in CISCC firmware register mode**

A10500D0 CIS1R08 CIS1 Register 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W08															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W08	**CIS1 Register used in CISCC firmware register mode**

A10500D4 CIS1R09 CIS1 Register 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W09															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W09	**CIS1 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500D8 CIS1R0A CIS1 Register A 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W0A															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W0A															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W0A	**CIS1 Register used in CISCC firmware register mode**

A10500DC CIS1R0B CIS1 Register B 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W0B															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W0B															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W0B	**CIS1 Register used in CISCC firmware register mode**

A10500E0 CIS1R0C CIS1 Register C 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W0C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W0C															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W0C	**CIS1 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500E4 CIS1R0D CIS1 Register D 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W0D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W0D															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W0D	**CIS1 Register used in CISCC firmware register mode**

A10500E8 CIS1R0E CIS1 Register E 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W0E															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W0E															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W0E	**CIS1 Register used in CISCC firmware register mode**

A10500EC CIS1R0F CIS1 Register F 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS1_W0F															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS1_W0F															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS1_W0F	**CIS1 Register used in CISCC firmware register mode**

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Bit(s)	Name	Description

A10500F0 CISRDY CIS Ready Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CIS_RDY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CIS_RDY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CIS_RDY	**CIS Ready Flag Register that is set after software decodes the CIS and finishes the SA initial flow to proceed with transfer.**

A10500F4 CCCR0 CC Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CCCR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCCR0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CCCR0	**Card Capability Register 0**

A10500F8 CCCR1 CC Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CCCR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CCCR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	CCCR1	**Card Capability Register 1**

A10500FC CCRDY CC Ready Flag Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CC_RDY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CC_RDY															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CC_RDY	**CC Ready Flag Register that is set after the CIS is programmed**

A1050100 HWFISR HIF WLAN Firmware Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SW_INT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RX_EVENT_1	RX_EVENT_0				TX_EVENT_0				WR_TIMEOUT_INT	RD_TIMEOUT_INT	D2HSM2R_RD_INT	DRV_CLR_FW_OWN	DRV_SET_FW_OWN
Type			RO	RO				RO				W1C	W1C	W1C	W1C	W1C
Reset			0	0				0				0	0	0	0	0

Bit(s)	Name	Description
31:16	H2D_SW_INT	**This field is used for software interrupt for WLAN operation.** Host driver writes 1s to WSICR [31:16] to set the corresponding bit field.
13	RX_EVENT_1	**This bit is asserted, if there is any interrupt asserted in HWFRE1SR.** **The bit will be de-asserted after software driver clears the interrupt event in HWFRE1SR.**
12	RX_EVENT_0	**This bit is asserted, if there is any interrupt asserted in HWFRE0SR. The bit will be de-asserted after software**

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Bit(s)	Name	Description
		driver clears the interrupt event in HWFRE0SR.
8	TX_EVENT_0	**This bit is asserted, if there is any interrupt asserted in HWFTE0SR. The bit will be de-asserted after software driver clears the interrupt event in HWFTE0SR.**
4	WR_TIMEOUT_INT	**Write timeout interrupt is triggered, if the host writes data and the device is unable to receive it in a pre-defined period. Firmware should receive the write timeout interrupt and tx_overflow interrupt, simultaneously.**
3	RD_TIMEOUT_INT	**A timeout interrupt is triggered, if the host reads data and the device is unable prepare the data in a pre-defined period. Firmware should receive the read timeout interrupt and rx_underflow interrupt, simultaneously.**
2	D2HSM2R_RD_INT	**This interrupt is set when the host reads the D2HRM2R register.**
1	DRV_CLR_FW_OWN	**This bit is set to 1, if software driver writes 1 into "WHLPCR.FW_OWN_REQ_CLR", to indicate that the software driver requests the control WLAN sub-system from the firmware. The firmware wakes up the WLAN sub-system from sleep mode and writes 1 into HWFICR.FW_OWN_BACK_INT_SET.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
0	DRV_SET_FW_OWN	**This bit is set to 1, if software driver writes 1 into "WHLPCR.FW_OWN_REQ_SET", to indicate that the software driver transfers the ownership of WLAN sub-system to the firmware. The firmware can force WLAN sub-system into sleep mode.** Firmware can clear this bit by writing 1. Writing 0 does nothing.

A1050104 HWFIER HIF WLAN Firmware Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SW_INT_EN															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RX_EVENT_1_INT_EN	RX_EVENT_0_INT_EN				TX_EVENT_0_INT_EN				WR_TIMEOUT_INT_EN	RD_TIMEOUT_INT_EN	D2HSM2R_RD_INT_EN	DRV_CLR_FW_OWN_INT_EN	DRV_SET_FW_OWN_INT_EN
Type			RW	RW				RW				RW	RW	RW	RW	RW

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Reset			0	0				0				0	0	0	0	0

Bit(s)	Name	Description
31:16	H2D_SW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
13	RX_EVENT_1_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
12	RX_EVENT_0_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
8	TX_EVENT_0_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
4	WR_TIMEOUT_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
3	RD_TIMEOUT_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
2	D2HSM2R_RD_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
1	DRV_CLR_FW_OWN_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
0	DRV_SET_FW_OWN_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.

A1050108 HWFISR1 Reserve for HWFISR1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFISR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFISR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	RESV_HWFISR1	**RESV_HWFISR1**

A105010C HWFIER1 Reserve for HWFIER1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFIER1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFIER1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFIER1	**RESV_HWFIER1**

A1050110 HWFTE0SR HIF WLAN Firmware TX Event 0 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX7D_LEN_ERR	TX6D_LEN_ERR	TX5D_LEN_ERR	TX4D_LEN_ERR	TX3D_LEN_ERR	TX2D_LEN_ERR	TX1D_LEN_ERR	TX0D_LEN_ERR	TX7D_CHKSUM_ERR	TX6D_CHKSUM_ERR	TX5D_CHKSUM_ERR	TX4D_CHKSUM_ERR	TX3D_CHKSUM_ERR	TX2D_CHKSUM_ERR	TX1D_CHKSUM_ERR	TX0D_CHKSUM_ERR
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							TX1_OVERFLOW	TX0_OVERFLOW	TX7_RDY	TX6_RDY	TX5_RDY	TX4_RDY	TX3_RDY	TX2_RDY	TX1_RDY	TX0_RDY
Type							W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX7D_LEN_ERR	**TX queue 7 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
30	TX6D_LEN_ERR	**TX queue 6 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
29	TX5D_LEN_ERR	**TX queue 5 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
28	TX4D_LEN_ERR	**TX queue 4 descriptor length error**

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Bit(s)	Name	Description
		A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
27	TX3D_LEN_ERR	**TX queue 3 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
26	TX2D_LEN_ERR	**TX queue 2 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
25	TX1D_LEN_ERR	**TX queue 1 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
24	TX0D_LEN_ERR	**TX queue 0 descriptor length error** A length error interrupt is triggered, when transmitted data length from the host is greater than the allowed buffer length.
23	TX7D_CHKSUM_ERR	**TX queue 7 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
22	TX6D_CHKSUM_ERR	**TX queue 6 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
21	TX5D_CHKSUM_ERR	**TX queue 5 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
20	TX4D_CHKSUM_ERR	**TX queue 4 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
19	TX3D_CHKSUM_ERR	**TX queue 3 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
18	TX2D_CHKSUM_ERR	**TX queue 2 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
17	TX1D_CHKSUM_ERR	**TX queue 1 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
16	TX0D_CHKSUM_ERR	**TX queue 0 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each TX descriptor before transferring data. This interrupt is triggered, if TX descriptor checksum error occurred.
9	TX1_OVERFLOW	**Data overflow at the WLAN TX1 port.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
8	TX0_OVERFLOW	**Data overflow at the WLAN TX0 port.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
7	TX7_RDY	**Set this bit, if a complete frame is transferred to WLAN TX7 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
6	TX6_RDY	**Set this bit, if a complete frame is transferred to WLAN**

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Bit(s)	Name	Description
		TX6 queue from host and the ownership bit of the buffer descriptor is cleared. Firmware can clear this bit by writing 1. Writing 0 does nothing.
5	TX5_RDY	**Set this bit, if a complete frame is transferred to WLAN TX5 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
4	TX4_RDY	**Set this bit, if a complete frame is transferred to WLAN TX4 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
3	TX3_RDY	**Set this bit, if a complete frame is transferred to WLAN TX3 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
2	TX2_RDY	**Set this bit, if a complete frame is transferred to WLAN TX2 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
1	TX1_RDY	**Set this bit, if a complete frame is transferred to WLAN TX1 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
0	TX0_RDY	**Set this bit, if a complete frame is transferred to WLAN TX0 queue from host and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.

A1050114 HWFTE1SR Reserve for HWFTE1SR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFTE1SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFTE1SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFTE1SR	**RESV_HWFTE1SR**

A1050118 HWFTE2SR Reserve for HWFTE2SR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFTE2SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFTE2SR															
Type	W1C															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFTE2SR	**RESV_HWFTE2SR**

A105011C **HWFTE3SR** **Reserve for HWFTE3SR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESV_HWFTE3SR**															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESV_HWFTE3SR**															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFTE3SR	**RESV_HWFTE3SR**

A1050120 **HWFTE0ER** **HIF WLAN Firmware TX Event 0 Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX7D_LEN_ERR_INT_EN**	**TX6D_LEN_ERR_INT_EN**	**TX5D_LEN_ERR_INT_EN**	**TX4D_LEN_ERR_INT_EN**	**TX3D_LEN_ERR_INT_EN**	**TX2D_LEN_ERR_INT_EN**	**TX1D_LEN_ERR_INT_EN**	**TX0D_LEN_ERR_INT_EN**	**TX7D_CHKSUM_ERR_INT_EN**	**TX6D_CHKSUM_ERR_INT_EN**	**TX5D_CHKSUM_ERR_INT_EN**	**TX4D_CHKSUM_ERR_INT_EN**	**TX3D_CHKSUM_ERR_INT_EN**	**TX2D_CHKSUM_ERR_INT_EN**	**TX1D_CHKSUM_ERR_INT_EN**	**TX0D_CHKSUM_ERR_INT_EN**
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**TX1_OVERFLOW_INT_EN**	**TX0_OVERFLOW_INT_EN**	**TX7_RDY_INT_EN**	**TX6_RDY_INT_EN**	**TX5_RDY_INT_EN**	**TX4_RDY_INT_EN**	**TX3_RDY_INT_EN**	**TX2_RDY_INT_EN**	**TX1_RDY_INT_EN**	**TX0_RDY_INT_EN**
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TX7D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is

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Bit(s)	Name	Description
		0: Disable the interrupt output. 1: Enable the interrupt output.
30	TX6D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
29	TX5D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
28	TX4D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
27	TX3D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
26	TX2D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
25	TX1D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
24	TX0D_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
23	TX7D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
22	TX6D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
21	TX5D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
20	TX4D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
19	TX3D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
18	TX2D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
17	TX1D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output.

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Bit(s)	Name	Description
		1: Enable the interrupt output.
16	TX0D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
9	TX1_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the related bit interrupt output. 1: Enable the related bit interrupt output.
8	TX0_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
7	TX7_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
6	TX6_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
5	TX5_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
4	TX4_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
3	TX3_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
2	TX2_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
1	TX1_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
0	TX0_RDY_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.

A1050124 HWFTE1ER Reserve for HWFTE1ER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFTE1ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam	RESV_HWFTE1ER															

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e																
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFTE1ER	**RESV_HWFTE1ER**

A1050128 HWFTE2ER Reserve for HWFTE2ER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFTE2ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFTE2ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFTE2ER	**RESV_HWFTE2ER**

A105012C HWFTE3ER Reserve for HWFTE3ER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFTE3ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFTE3ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFTE3ER	**RESV_HWFTE3ER**

A1050130 HWFRE0SR HIF WLAN Firmware RX Event 0 Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RX_LEN_FIFO3_OVERFL	RX_LEN_FIFO2_OVERFL	RX_LEN_FIFO1_OVERFL	RX_LEN_FIFO0_OVERFL					RX3D_CHKSUM_ERR	RX2D_CHKSUM_ERR	RX1D_CHKSUM_ERR	RX0D_CHKSUM_ERR

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					OW	OW	OW	OW								
Type					W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX3_UNDERFLOW	RX2_UNDERFLOW	RX1_UNDERFLOW	RX0_UNDERFLOW					RX3_DONE	RX2_DONE	RX1_DONE	RX0_DONE
Type					W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27	RX_LEN_FIFO3_OVERFLOW	**RX length FIFO 3 overflow** This interrupt is generated whenever the firmware attempts to set RX FIFO length by HWRQ3CR when the packet FIFO length is already full. This leads to FIFO overflow. The entry in packet length FIFO will be pushed-in by firmware, and then popped-out when corresponding RX length is read by the host driver.
26	RX_LEN_FIFO2_OVERFLOW	**RX length FIFO 2 overflow** This interrupt is generated whenever the firmware attempts to set RX FIFO length by HWRQ3CR when the packet FIFO length is already full. This leads to FIFO overflow. The entry in packet length FIFO will be pushed-in by firmware, and then popped-out when corresponding RX length is read by the host driver.
25	RX_LEN_FIFO1_OVERFLOW	**RX length FIFO 1 overflow** This interrupt is generated whenever the firmware attempts to set RX FIFO length by HWRQ3CR when the packet FIFO length is already full. This leads to FIFO overflow. The entry in packet length FIFO will be pushed-in by firmware, and then popped-out when corresponding RX length is read by the host driver.
24	RX_LEN_FIFO0_OVERFLOW	**RX length FIFO 0 overflow** This interrupt is generated whenever the firmware attempts to set RXFIFO length by HWRQ3CR when the packet FIFO length is already full. This leads to FIFO overflow. The entry in packet length FIFO will be push-in by firmware, and then popped-out when corresponding RX length is read by the host driver.
19	RX3D_CHKSUM_ERR	**RX 3 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each RX descriptor before transferring the data movement. This interrupt is generated, if RX descriptor checksum error occurred.
18	RX2D_CHKSUM_ERR	**RX 2 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware

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Bit(s)	Name	Description
		validates the checksum value of each RX descriptor before transferring the data. This interrupt is generated if RX descriptor checksum error occurred.
17	RX1D_CHKSUM_ERR	**RX 1 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each RX descriptor before transferring the data. This interrupt is generated if RX descriptor checksum error occurred.
16	RX0D_CHKSUM_ERR	**RX 0 descriptor checksum error** When HWFCR. TRX_DESC_CHKSUM_EN is enabled; hardware validates the checksum value of each RX descriptor before transferring the data. This interrupt is generated if RX descriptor checksum error occurred.
11	RX3_UNDERFLOW	**Data underflow at the WLAN RX3 port.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
10	RX2_UNDERFLOW	**Data underflow at the WLAN RX2 port.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
9	RX1_UNDERFLOW	**Data underflow at the WLAN RX1 port.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
8	RX0_UNDERFLOW	**Data underflow at the WLAN RX0 port.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
3	RX3_DONE	**Set this bit, if a complete frame is moved to host from WLAN RX3 queue (which also implies the corresponding entry is popped-out from RX3 FIFO length).** Firmware can clear this bit by writing 1. Writing 0 does nothing.
2	RX2_DONE	**Set this bit, if a complete frame is moved to host from WLAN RX2 queue (which also implies the corresponding entry is popped-out from RX2 length FIFO).** Firmware can clear this bit by writing 1. Writing 0 does nothing.
1	RX1_DONE	**Set this bit, if a complete frame is moved to host from WLAN RX1 queue (which also implies the corresponding entry is popped-out from RX0 length FIFO).** Firmware can clear this bit by writing 1. Writing 0 does nothing.
0	RX0_DONE	**Set this bit, if a complete frame is moved to host from WLAN RX0 queue (which also implies the corresponding entry is popped-out from RX0 length FIFO).** Firmware can clear this bit by writing 1. Writing 0 does nothing.

A1050134 **HWFRE1SR** **HIF WLAN Firmware RX Event 1 Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX3_LEN_ERR	RX2_LEN_ERR	RX1_LEN_ERR	RX0_LEN_ERR					RX3_OWN_CLEAR_DONE	RX2_OWN_CLEAR_DONE	RX1_OWN_CLEAR_DONE	RX0_OWN_CLEAR_DONE
Type					W1C	W1C	W1C	W1C					W1C	W1C	W1C	W1C
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11	RX3_LEN_ERR	**RX queue 3 descriptor length error** If the extension length and RX data length are zero in the generic packet descriptor or buffer descriptor, an interrupt is triggered. Firmware can clear this bit by writing 1. Writing 0 does nothing.
10	RX2_LEN_ERR	**RX queue 2 descriptor length error** If the extension length and RX data length are zero in the generic packet descriptor or buffer descriptor, an interrupt is triggered. Firmware can clear this bit by writing 1. Writing 0 does nothing.
9	RX1_LEN_ERR	**RX queue 1 descriptor length error** If the extension length and RX data length are zero in the generic packet descriptor or buffer descriptor, an interrupt is triggered. Firmware can clear this bit by writing 1. Writing 0 does nothing.
8	RX0_LEN_ERR	**RX queue 0 descriptor length error** If the extension length and RX data length are zero in the generic packet descriptor or buffer descriptor, an interrupt is triggered. Firmware can clear this bit by writing 1. Writing 0 does nothing.
3	RX3_OWN_CLEAR_DONE	**Set this bit, if a complete frame is moved to internal FIFO from WLAN RX3 queue and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
2	RX2_OWN_CLEAR_DONE	**Set this bit, if a complete frame is moved to internal FIFO from WLAN RX2 queue and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
1	RX1_OWN_CLEAR_DONE	**Set this bit, if a complete frame is moved to internal FIFO from WLAN RX1 queue and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.
0	RX0_OWN_CLEAR_DONE	**Set this bit, if a complete frame is moved to internal FIFO from WLAN RX0 queue and the ownership bit of the buffer descriptor is cleared.** Firmware can clear this bit by writing 1. Writing 0 does nothing.

A1050138 HWFRE2SR Reserve for HWFRE2SR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFRE2SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFRE2SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFRE2SR	**RESV_HWFRE2SR**

A105013C **HWFRE3SR** **Reserve for HWFRE3SR** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFRE3SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFRE3SR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFRE3SR	**RESV_HWFRE3SR**

A1050140 **HWFRE0ER** **HIF WLAN Firmware RX Event 0 Enable Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					RX_LEN_FIFO3_OVERFLOW_INT_EN	RX_LEN_FIFO2_OVERFLOW_INT_EN	RX_LEN_FIFO1_OVERFLOW_INT_EN	RX_LEN_FIFO0_OVERFLOW_INT_EN					RX3D_CHKSUM_ERR_INT_EN	RX2D_CHKSUM_ERR_INT_EN	RX1D_CHKSUM_ERR_INT_EN	RX0D_CHKSUM_ERR_INT_EN
Type					RW	RW	RW	RW					RW	RW	RW	RW
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX3_UNDERFLOW_INT_EN	RX2_UNDERFLOW_INT_EN	RX1_UNDERFLOW_INT_EN	RX0_UNDERFLOW_INT_EN					RX3_DONE_INT_EN	RX2_DONE_INT_EN	RX1_DONE_INT_EN	RX0_DONE_INT_EN

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Type					RW	RW	RW	RW					RW	RW	RW	RW
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
27	RX_LEN_FIFO3_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
26	RX_LEN_FIFO2_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
25	RX_LEN_FIFO1_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
24	RX_LEN_FIFO0_OVERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
19	RX3D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
18	RX2D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the related bit interrupt output. 1: Enable the related bit interrupt output.
17	RX1D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
16	RX0D_CHKSUM_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
11	RX3_UNDERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
10	RX2_UNDERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
9	RX1_UNDERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
8	RX0_UNDERFLOW_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the related bit interrupt output. 1: Enable the related bit interrupt output.
3	RX3_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
2	RX2_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.**

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Bit(s)	Name	Description
		If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
1	RX1_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
0	RX0_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.

A1050144 HWFRE1ER HIF WLAN Firmware RX Event 1 Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX3_LEN_ERR_INT_EN	RX2_LEN_ERR_INT_EN	RX1_LEN_ERR_INT_EN	RX0_LEN_ERR_INT_EN					RX3_OWN_CLEAR_DONE_INT_EN	RX2_OWN_CLEAR_DONE_INT_EN	RX1_OWN_CLEAR_DONE_INT_EN	RX0_OWN_CLEAR_DONE_INT_EN
Type					RW	RW	RW	RW					RW	RW	RW	RW
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11	RX3_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
10	RX2_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
9	RX1_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
8	RX0_LEN_ERR_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
3	RX3_OWN_CLEAR_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is

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Bit(s)	Name	Description
		0: Disable the interrupt output. 1: Enable the interrupt output.
2	RX2_OWN_CLEAR_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
1	RX1_OWN_CLEAR_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.
0	RX0_OWN_CLEAR_DONE_INT_EN	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.

A1050148 HWFRE2ER Reserve for HWFRE2ER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFRE2ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFRE2ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFRE2ER	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output. 1: Enable the interrupt output.

A105014C HWFRE3ER Reserve for HWFRE3ER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_HWFRE3ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_HWFRE3ER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_HWFRE3ER	**WLAN firmware interrupt output control for each bit.** If the related bit is 0: Disable the interrupt output.

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Bit(s)	Name	Description
		1: Enable the interrupt output.

A1050150 HWFICR HIF WLAN Firmware Interrupt Control Register 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SW_INT_SET															
Type	W1S															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SW_INT_SET											FW_OWN_BACK_INT_SET				
Type	W1S											W1S				
Reset	0	0	0	0	0	0	0	0				1				

Bit(s)	Name	Description
31:8	D2H_SW_INT_SET	**Firmware writes 1s to set WHISR.D2H_SW_INT. Writing 0 does nothing.** Read always returns 0. This is used as communication between firmware and driver, with interrupt trigger to host driver HIF.
4	FW_OWN_BACK_INT_SET	**Firmware writes 1 to set WHISR.FW_OWN_BACK_INT. Writing 0 does nothing. It will also clear WLAN_FW_OWN bit and set WHLPCR.WLAN_DRV_OWN bit.** Firmware sets this bit, if the driver requests firmware to return the ownership or the firmware requires waking up the driver. Reading the bit will get the status of WLAN_FW_OWN bit. WLAN_FW_OWN indicates that WLAN firmware has the ownership of the WLAN sub-system. This bit is cleared by firmware writing 1 into HWFICR.FW_OWN_BACK_INT_SET or any WLAN driver-domain interrupt. 0: WLAN firmware doesn't have any ownership. 1: WLAN firmware has an ownership.

A1050154 HWFCR HIF WLAN Firmware Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							RX_N	TX_N	RX_U	RX_T	RX_IP	RX_IP	TX_C	TRX_	TRX_	W_FU

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							O_TAIL	O_HEADER	DP_CS_OFLD_EN	CP_CS_OFLD_EN	V4_CS_OFLD_EN	V6_CS_OFLD_EN	S_OFLD_EN	DESC_CHKSUM_12B	DESC_CHKSUM_EN	NC_RDY
Type							RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9	RX_NO_TAIL	**RX packet tail is used to send the checksum offload status. If the checksum offload hardware is not configured, the tail would be 4B zero. Firmware can write 1 to prevent the RX packet from sending to host.** 0: RX packet tail will be sent to host. 1: RX packet tail will not be sent to host.
8	TX_NO_HEADER	**Firmware writes 1 to this field so that the host will send the TX packet header instead of writing it to the AHB bus.** 0: TX packet header from host will be written to AHB bus. 1: TX packet header from host will not be written to AHB bus.
7	RX_UDP_CS_OFLD_EN	**Enables the RX UDP checksum verification function** When enabled, the checksum of RX packet with UDP header is calculated and verified with the field in the original RX packet. The verified status will be padding in the last DWORD of the RX packet.
6	RX_TCP_CS_OFLD_EN	**Enables the RX TCP checksum verification function** When enabled, the checksum of RX packet with TCP header is calculated and verified with the field in the original RX packet. The verified status will be padding in the last DWORD of the RX packet.
5	RX_IPV4_CS_OFLD_EN	**Enables the RX IPv4 checksum verification function** When enabled, the checksum of RX packet with IPv4 header will be calculated and verified with the field in the original RX packet. The verified status will be padding in the last DWORD of the RX packet.
4	RX_IPV6_CS_OFLD_EN	**Enables the RX IPv6 checksum (without extension header) verification function** When enabled, packets checksum of RX packet with IPv6 header will be calculated and verified with the field in the original RX packet. The verified status will be padding in the last DWORD of the RX packet.
3	TX_CS_OFLD_EN	**Enables the TX IPV6/IPV4/TCP/UDP checksum generation function**
2	TRX_DESC_CHKSUM_12B	**Firmware writes 1 to this field to change the descriptor checksum calculation method to 12B. The default calculation method is based on the 16B descriptor checksum.** 0: Descriptor checksum calculation is based on the first 16B. 1: Descriptor checksum calculation is based on the first 12B.
1	TRX_DESC_CHKSUM_EN	**Enables the TX/ RX descriptor checksum for debugging purposes.** Hardware will validate if the sum of descriptor checksum is 0xff before data movement for the descriptor. If it is invalid, corresponding interrupt status (TXD_CHKSUM_ERR/ RXD_CHKSUM_ERR) will be generated.
0	W_FUNC_RDY	**Indicates the WLAN functional block's current status. If WLAN functional block has finished its initial procedure and it is ready for normal operation, firmware should set this bit. If WLAN functional block was disabled, this bit should be cleared.** This is a sticky bit of WCIR.W_FUNC_RDY. 0: WLAN functional block is not ready for normal operation.

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Bit(s)	Name	Description
		1: WLAN functional block is ready for normal operation.

A1050158 HWTDCR HIF WLAN TX DMA Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ7_DMA_STATUS	TXQ6_DMA_STATUS	TXQ5_DMA_STATUS	TXQ4_DMA_STATUS	TXQ3_DMA_STATUS	TXQ2_DMA_STATUS	TXQ1_DMA_STATUS	TXQ0_DMA_STATUS	TXQ7_DMA_RUM	TXQ6_DMA_RUM	TXQ5_DMA_RUM	TXQ4_DMA_RUM	TXQ3_DMA_RUM	TXQ2_DMA_RUM	TXQ1_DMA_RUM	TXQ0_DMA_RUM
Type	RO	RO	RO	RO	RO	RO	RO	RO	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ7_DMA_START	TXQ6_DMA_START	TXQ5_DMA_START	TXQ4_DMA_START	TXQ3_DMA_START	TXQ2_DMA_START	TXQ1_DMA_START	TXQ0_DMA_START	TXQ7_DMA_STOP	TXQ6_DMA_STOP	TXQ5_DMA_STOP	TXQ4_DMA_STOP	TXQ3_DMA_STOP	TXQ2_DMA_STOP	TXQ1_DMA_STOP	TXQ0_DMA_STOP
Type	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TXQ7_DMA_STATUS	**Reads the TX4 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state, by default. After receiving a START or RESUME command and executing it without an error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
30	TXQ6_DMA_STATUS	**Reads the TX6 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state, by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
29	TXQ5_DMA_STATUS	**Reads the TX5 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
28	TXQ4_DMA_STATUS	**Reads the TX4 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive

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Bit(s)	Name	Description
		1: active
27	TXQ3_DMA_STATUS	**Reads the TX3 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
26	TXQ2_DMA_STATUS	**Reads the TX2 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
25	TXQ1_DMA_STATUS	**Reads the TX1 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
24	TXQ0_DMA_STATUS	**Reads the TX0 queue DMA status.** When the HIF Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
23	TXQ7_DMA_RUM	**Resumes the TX7 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
22	TXQ6_DMA_RUM	**Resumes the TX6 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
21	TXQ5_DMA_RUM	**Resumes the TX5 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
20	TXQ4_DMA_RUM	**Resumes the TX4 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
19	TXQ3_DMA_RUM	**Resumes the TX3 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
18	TXQ2_DMA_RUM	**Resumes the TX2 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
17	TXQ1_DMA_RUM	**Resumes the TX1 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.

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Bit(s)	Name	Description
16	TXQ0_DMA_RUM	**Resumes the TX0 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
15	TXQ7_DMA_START	**Starts the TX7 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ7SAR. Software must check TXQ7_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
14	TXQ6_DMA_START	**Starts the TX6 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ6SAR. Software must check TXQ6_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
13	TXQ5_DMA_START	**Starts the TX5 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ5SAR. Software must check TXQ5_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
12	TXQ4_DMA_START	**Starts the TX4 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ4SAR. Software must check TXQ4_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
11	TXQ3_DMA_START	**Starts the TX3 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ3SAR. Software must check TXQ3_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
10	TXQ2_DMA_START	**Start the TX2 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ2SAR. Software must check TXQ2_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
9	TXQ1_DMA_START	**Starts the TX1 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ1SAR. Software must check TXQ1_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
8	TXQ0_DMA_START	**Starts the TX0 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFTQ0SAR. Software must check TXQ0_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
7	TXQ7_DMA_STOP	**Stops the TX7 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
6	TXQ6_DMA_STOP	**Stops the TX6 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
5	TXQ5_DMA_STOP	**Stops the TX5 queue DMA operation. It will NOT clear the**

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Bit(s)	Name	Description
		result of TX count set by HWTPCCR(WTSR0/ WTSR1). Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
4	TXQ4_DMA_STOP	**Stops the TX4 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
3	TXQ3_DMA_STOP	**Stop the TX3 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
2	TXQ2_DMA_STOP	**Stop the TX2 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
1	TXQ1_DMA_STOP	**Stop the TX1 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going). If one data port to multiple queues design is configured, any one of these queues stopping would cause others to stop at the same time. (e.g. If TX queue 1 stops, then TX queue 2, 3, 4, 5, 6, 7 would also be stopped by hardware since they share the same data port.)
0	TXQ0_DMA_STOP	**Stop the TX0 queue DMA operation. It will NOT clear the result of TX count set by HWTPCCR(WTSR0/ WTSR1).** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read always returns current DMA activity (0: stopped, 1: stop command is on-going).

A105015C **HWTPCCR** **HIF WLAN TX Packet Count Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TQ_CNT_RESET
Type																W1S

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Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TQ_INDEX**								**INC_TQ_CNT**							
Type	WO								WO							
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16	TQ_CNT_RESET	**Firmware writes 1 to reset the count accumulated for TQ0 ~ TQ7.** Writing 0 does nothing. Read always returns 0.
15:12	TQ_INDEX	**Firmware writes the TQ index to be increased by setting this field which leads to the same number increased in WTSR.TQX_CNT.** Writing 0 does nothing. Read always returns 0. (X depends on the TQ index)
7:0	INC_TQ_CNT	**Firmware writes the available TQ buffer count by setting this field which leads to the same number increased in WTSR.TQX_CNT.** Writing 0 does nothing. Read always returns 0. (X depends on the TQ index)

A1050160 HWFTQ0SAR HIF WLAN Firmware TX Queue 0 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ0_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ0_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ0_DMA_SADDR	**The start address of buffer chain of TX0 queue in unit of DW.**

A1050164 HWFTQ1SAR HIF WLAN Firmware TX Queue 1 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ1_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ1_DMA_SADDR**															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ1_DMA_SADDR	**The start address of buffer chain of TX1 queue in unit of DW.**

A1050168 HWFTQ2SAR HIF WLAN Firmware TX Queue 2 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ2_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ2_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ2_DMA_SADDR	**The start address of buffer chain of TX2 queue in unit of DW.**

A105016C HWFTQ3SAR HIF WLAN Firmware TX Queue 3 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ3_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ3_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ3_DMA_SADDR	**The start address of buffer chain of TX3 queue in unit of DW.**

A1050170 HWFTQ4SAR HIF WLAN Firmware TX Queue 4 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ4_DMA_SADDR**															
Type	RW															
Rese	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ4_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ4_DMA_SADDR	**The start address of buffer chain of TX4 queue in unit of DW.**

A1050174 **HWFTQ5SAR** **Reserve for HIF WLAN Firmware TX Queue 5 Start Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ5_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ5_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ5_DMA_SADDR	**The start address of buffer chain of TX5 queue in unit of DW.**

A1050178 **HWFTQ6SAR** **Reserve for HIF WLAN Firmware TX Queue 6 Start Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**WLAN_TXQ6_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_TXQ6_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ6_DMA_SADDR	**The start address of buffer chain of TX6 queue in unit of DW.**

A105017C **HWFTQ7SAR** **Reserve for HIF WLAN Firmware TX Queue 7 Start Address Register** **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_TXQ7_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_TXQ7_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_TXQ7_DMA_SADDR	**The start address of buffer chain of TX7 queue in unit of DW.**

A1050180 HWFRQ0SAR HIF WLAN Firmware RX Queue 0 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ0_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ0_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ0_DMA_SADDR	**The start address of buffer chain of RX0 queue in unit of DW.**

A1050184 HWFRQ1SAR HIF WLAN Firmware RX Queue 1 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ1_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ1_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ1_DMA_SADDR	**The start address of buffer chain of RX1 queue in unit of DW.**

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Bit(s)	Name	Description

A1050188 HWFRQ2SAR HIF WLAN Firmware RX Queue 2 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ2_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ2_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ2_DMA_SADDR	**The start address of buffer chain of RX2 queue in unit of DW.**

A105018C HWFRQ3SAR HIF WLAN Firmware RX Queue 3 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ3_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ3_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ3_DMA_SADDR	**The start address of buffer chain of RX3 queue in unit of DW.**

A1050190 HWFRQ4SAR Reserve for HIF WLAN Firmware RX Queue 4 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ4_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ4_DMA_SADDR															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ4_DMA_SADDR	**The start address of buffer chain of RX4 queue in unit of DW.**

A1050194 HWFRQ5SAR Reserve for HIF WLAN Firmware RX Queue 5 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ5_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ5_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ5_DMA_SADDR	**The start address of buffer chain of RX5 queue in unit of DW.**

A1050198 HWFRQ6SAR Reserve for HIF WLAN Firmware RX Queue 6 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ6_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WLAN_RXQ6_DMA_SADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ6_DMA_SADDR	**The start address of buffer chain of RX6 queue in unit of DW.**

A105019C HWFRQ7SAR Reserve for HIF WLAN Firmware RX Queue 7 Start Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WLAN_RXQ7_DMA_SADDR															
Type	RW															
Rese	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**WLAN_RXQ7_DMA_SADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:2	WLAN_RXQ7_DMA_SADDR	**The start address of buffer chain of RX7 queue in unit of DW.**

A10501A0 H2DRM0R Host to Device Receive Mailbox 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**H2D_RM0**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**H2D_RM0**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_RM0	**This register is used by firmware to receive data from SDIO controller, which is updated through H2DSM0R by host driver.**

A10501A4 H2DRM1R Host to Device Receive Mailbox 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**H2D_RM1**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**H2D_RM1**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_RM1	**This register is used by firmware to receive data from SDIO controller, which is updated through H2DSM1R by host driver.**

A10501A8 D2HSM0R Device to Host Send Mailbox 0 Register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_SM0	**This register is used by firmware to transmit data to SDIO controller, it will be updated to D2HRM0R and read by host driver.**

A10501AC D2HSM1R Device to Host Send Mailbox 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_SM1	**This register is used by firmware to transmit data to SDIO controller, it will be updated to D2HRM1R and read by host driver.**

A10501B0 D2HSM2R Device to Host Send Mailbox 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_SM2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_SM2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_SM2	**This register is used by firmware to transmit data to SDIO controller, it will be updated to D2HRM2R and read by host driver.**

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Bit(s)	Name	Description
		When reading this register, it may not get the value just written by the firmware, it may read the older value written before, because of hardware synchronization issue. Firmware gets the value that host is trying to read when host clock turns on. Note, that host driver could read D2HRM2R without system AHB clock. Hence, after firmware sets this register, MCU could turn off system AHB clock to save power, if necessary.

A10501C0 HWRQ0CR HIF WLAN RX Queue 0 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RXQ0_DMA_STATUS	RXQ0_DMA_RUM	RXQ0_DMA_START	RXQ0_DMA_STOP
Type													RO	W1S	W1S	W1S
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXQ0_PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	RXQ0_DMA_STATUS	**Reads the RX0 queue DMA status.** When the SDIO Controller is reset, the queue is in the inactive state, by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
18	RXQ0_DMA_RUM	**Resumes the RX0 queue DMA.** The DMA reloads the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
17	RXQ0_DMA_START	**Starts the RX0 queue DMA operation.** The DMA loads the chain descriptor from the address assigned by HWFRQ0SAR. Software must check RXQ0_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
16	RXQ0_DMA_STOP	**Stops the RX0 queue DMA operation, the content in the RXQ0 FIFO and RXQ0 length FIFO will be cleared.** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read returns current RXQ0 operation state (1: stop operation is on-going, 0: stop operation is finished).
15:0	RXQ0_PACKET_LENGTH	**When writing:** Notifies the HIF that 1 RX packet in this packet length is queued into this RX queue. **When reading:** Reads the 1st RX packet length indicated from this queue and is be 0 when the queue is empty.

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Bit(s)	Name	Description
		Firmware will write this FIFO-like port (at most 64 entries depending on the hardware configuration for each project) together with RXQ1_DMA_RUM bit that has been set, after RX packet is queued into descriptor chain. RX packet with length already set by this field is read by host driver, through reading WRPLR, or INT enhance mode, or RX enhance mode. None-empty entry will generate RX done interrupt, and corresponding entry will be cleared by hardware after this packet length is read by host driver. Writing 0 does nothing. 0: inactive 1: active

A10501C4 HWRQ1CR HIF WLAN RX Queue 1 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RXQ1_DMA_STATUS	RXQ1_DMA_RUM	RXQ1_DMA_START	RXQ1_DMA_STOP
Type													RO	W1S	W1S	W1S
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX1_PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	RXQ1_DMA_STATUS	**Reads the RXQ1 DMA status.** When the SDIO Controller is reset, the queue is in the inactive state, by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
18	RXQ1_DMA_RUM	**Resumes the RX1 queue DMA to operate.** The DMA reloads the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
17	RXQ1_DMA_START	**Starts the RX1 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFRQ1SAR. Software must check RXQ1_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
16	RXQ1_DMA_STOP	**Stops the RX1 queue DMA operation, the content in the RXQ1 FIFO and RXQ1 length FIFO will be cleared.** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read returns current RXQ1 operation state (1: active, 0: stopped).
15:0	RX1_PACKET_LENGTH	**When writing:** To indicate HIF that 1 RX packet in this packet length is queued

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Bit(s)	Name	Description
		into this RX queue. **When reading:** Read the 1st RX packet length indicated from this queue and is 0 when queue is empty. Firmware will write this FIFO-like port (at most 64 entries depending on the hardware configuration for each project) together with RXQ1_DMA_RUM bit that has been set, after RX packet is queued into descriptor chain. RX packet with length already set by this field is read by host driver, through reading WRPLR, or INT enhance mode, or RX enhance mode. Valid entry will generate RX done interrupt, and corresponding entry will be cleared by hardware after this packet length is read by host driver. Writing 0 does nothing.

A10501C8 HWRQ2CR HIF WLAN RX Queue 2 Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RXQ2_DMA_STATUS	RXQ2_DMA_RUM	RXQ2_DMA_START	RXQ2_DMA_STOP
Type													RO	W1S	W1S	W1S
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX2_PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	RXQ2_DMA_STATUS	**Reads the RXQ2 DMA status.** When the SDIO Controller is reset, the queue is in the inactive state, by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
18	RXQ2_DMA_RUM	**Resumes RX2 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
17	RXQ2_DMA_START	**Starts RX2 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFRQ1SAR. Software must check RXQ2_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.
16	RXQ2_DMA_STOP	**Stops the RX2 queue DMA operation, the content in the RXQ2 FIFO and RXQ2 length FIFO will be cleared.** Firmware writes 1 to stop the DMA. Writing 0 does nothing.

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Bit(s)	Name	Description
15:0	RX2_PACKET_LENGTH	Read returns current RXQ2 operation state (1: active, 0: stopped). **When writing:** To indicate HIF that 1 RX packet in this packet length is queued into this RX queue. **When reading:** Read the 1st RX packet length indicated from this queue and is 0 when queue is empty. Firmware will write this FIFO-like port (at most 64 entries depending on the hardware configuration for each project) together with RXQ2_DMA_RUM bit that has been set, after RX packet is queued into descriptor chain. RX packet with length already set by this field is read by host driver, through reading WRPLR, or INT enhance mode, or RX enhance mode. Valid entry will generate RX done interrupt, and corresponding entry will be cleared by hardware after this packet length is read by host driver. Writing 0 does nothing.

A10501CC **HWRQ3CR** **HIF WLAN RX Queue 3 Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													RXQ3_DMA_STATUS	RXQ3_DMA_RUM	RXQ3_DMA_START	RXQ3_DMA_STOP
Type													RO	W1S	W1S	W1S
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX3_PACKET_LENGTH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	RXQ3_DMA_STATUS	**Reads the RXQ3 DMA status.** When the SDIO Controller is reset, the queue is in the inactive state by default. After receiving a START or RESUME command and executing it without error, the queue enters the active state. When the queue is empty or stopped by a STOP command, it returns to the inactive state. 0: inactive 1: active
18	RXQ3_DMA_RUM	**Resumed the RX3 queue DMA to operate.** The DMA will reload the chain descriptor from the current address. Firmware writes 1 to enable the DMA. Writing 0 does nothing. Read always returns 0.
17	RXQ3_DMA_START	**Starts the RX3 queue DMA operation.** The DMA will load the chain descriptor from the address assigned by HWFRQ1SAR. SW must check RXQ3_DMA_STATUS is inactive before start. Writing 0 does nothing. Read always returns 0.

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Bit(s)	Name	Description
16	RXQ3_DMA_STOP	**Stops the RX3 queue DMA operation, the content in the RXQ3 FIFO and RXQ3 length FIFO will be cleared.** Firmware writes 1 to stop the DMA. Writing 0 does nothing. Read returns current RXQ3 operation state (1: active, 0: stopped).
15:0	RX3_PACKET_LENGTH	**When writing:** To indicate HIF that 1 RX packet in this packet length is queued into this RX queue. **When reading:** Read the 1st RX packet length indicated from this queue and is 0 when queue is empty. Firmware will write this FIFO-like port (at most 64 entries depending on the hardware configuration for each project) together with RXQ3_DMA_RUM bit that has been set, after RX packet is queued into descriptor chain. RX packet with length already set by this field is read by host driver, through reading WRPLR, or INT enhance mode, or RX enhance mode. Valid entry will generate RX done interrupt, and corresponding entry will be cleared by HW after this packet length is read by host driver. Writing 0 does nothing.

A10501D0 HWRQ4CR Reserve for HWRQ4CR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_FOR_HWRQ4CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_FOR_HWRQ4CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_FOR_HWRQ4CR	**RESV_FOR_HWRQ4CR**

A10501D4 HWRQ5CR Reserve for HWRQ5CR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_FOR_HWRQ5CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_FOR_HWRQ5CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	RESV_FOR_HWRQ5CR	**RESV_FOR_HWRQ5CR**

A10501D8 HWRQ6CR Reserve for HWRQ6CR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_FOR_HWRQ6CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_FOR_HWRQ6CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_FOR_HWRQ6CR	**RESV_FOR_HWRQ6CR**

A10501DC HWRQ7CR Reserve for HWRQ7CR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_FOR_HWRQ7CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_FOR_HWRQ7CR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_FOR_HWRQ7CR	**RESV_FOR_HWRQ7CR**

A10501E0 HWRLFACR HIF WLAN RX Length FIFO Available Count Register 40404040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		RX3_LEN_FIFO_AVAIL_CNT								RX2_LEN_FIFO_AVAIL_CNT						
Type		RO								RO						
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		RX1_LEN_FIFO_AVAIL_CNT								RX0_LEN_FIFO_AVAIL_CNT						
Type		RO								RO						
Reset		1	0	0	0	0	0	0		1	0	0	0	0	0	0

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Bit(s)	Name	Description
30:24	RX3_LEN_FIFO_AVAIL_CNT	**It indicates the RX3 length FIFO available count. Software should prevent push extra entries into FIFO.** If under the define of SDCTL_RX3_PACKET_LEN_64, The maximum is 64. If under the define of SDCTL_RX3_PACKET_LEN_32, The maximum is 32. If under the define of SDCTL_RX3_PACKET_LEN_16, The maximum is 16.
22:16	RX2_LEN_FIFO_AVAIL_CNT	**It indicates the RX2 length FIFO available count. Software should prevent push extra entries into FIFO.** If under the define of SDCTL_RX2_PACKET_LEN_64, The maximum is 64. If under the define of SDCTL_RX2_PACKET_LEN_32, The maximum is 32. If under the define of SDCTL_RX2_PACKET_LEN_16, The maximum is 16.
14:8	RX1_LEN_FIFO_AVAIL_CNT	**It indicates the RX1 length FIFO available count. Software should prevent push extra entries into FIFO.** If under the define of SDCTL_RXD_PACKET_LEN_64, The maximum is 64. If under the define of SDCTL_RXD_PACKET_LEN_32, The maximum is 32. If under the define of SDCTL_RXD_PACKET_LEN_16, The maximum is 16.
6:0	RX0_LEN_FIFO_AVAIL_CNT	**It indicates the RX0 length FIFO available count. Software should prevent push extra entries into FIFO.** If under the define of SDCTL_RXE_PACKET_LEN_64, The maximum is 64. If under the define of SDCTL_RXE_PACKET_LEN_32, The maximum is 32. If under the define of SDCTL_RXE_PACKET_LEN_16, The maximum is 16.

A10501E4 HWRLFACR1 Reserve for HWRLFACR1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_FOR_HWRLFACR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_FOR_HWRLFACR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_FOR_HWRLFACR1	**RESV_FOR_HWRLFACR1**

A10501E8 HWDMACR HIF WLAN DMA Control Register 0000004A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Rese																

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DMA_BST_SIZE**		**AHB_PROT2_CTL**		**ARBITER_MODE**		**DEST_BST_TYP**	**AHB_1KBNDRY_PRTCT**
Type									RW		RW		RW		RW	RW
Reset									0	1	0	0	1		1	0

Bit(s)	Name	Description
7:6	DMA_BST_SIZE	**This field is used to determine the DMA burst size** 0 : burst size = 4 DW 1: burst size = 8 DW 2: burst size = 16DW
5:4	AHB_PROT2_CTL	**This field is used to Control AHB bus Protection 2 function** 00: DMA engine would use HPROT[2] signal on AHB bus to be 0 to protect HWO write back. This is used to guarantee that MCU would receive interrupt after the HWO is written. For other data writes, HPROT[2] is set to 1 to indicate that it is Bufferable 01: The HPROT[2] signal on AHB bus is always set to 0, which means all AHB writes are not Bufferable 10: The HPROT[2] signal on AHB bus is always set to 1, which means all AHB writes are Bufferable
3	ARBITER_MODE	**For Normal Mode, the arbitration algorithm is more preferred for TX direction (from HOST to FW), which is good for reducing the duration time during write busy in SDIO interface.** And for Reserve Mode, it is more aggressive than the Normal Mode which means RX will not execute unless TX has been completed. 0: Reserve Mode 1: Normal Mode (Recommended)
1	DEST_BST_TYP	**This field is used to specify the AHB burst type for HWO write back.** 0: HIFSYS DMA engine would use non-post-write (INCR, burst type = 3'b001) to write 0 to HWO when the responding data is dealt. This access could guarantee that MCU would receive interrupt after the HWO is written. 1: HIFSYS DMA engine would use post-write (SINGLE, burst type = 3'b000) to write 0 to HWO when the responding data is dealt. This access could NOT guarantee that MCU would receive interrupt after the HWO is written.
0	AHB_1KBNDRY_PRTCT	**This field is used to specify whether to protect the 1K boundary.** 0: Don't protect. 1: DMA will guarantee the AHB will not cross 1K boundary in a burst.

A10501EC **HWFIOCDR** **HIF WLAN Firmware GPD IOC Bit Disable Register** **00000FFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**RXQ3_IOC_DIS**	**RXQ2_IOC_DIS**	**RXQ1_IOC_DIS**	**RXQ0_IOC_DIS**	**TXQ7_IOC_DIS**	**TXQ6_IOC_DIS**	**TXQ5_IOC_DIS**	**TXQ4_IOC_DIS**	**TXQ3_IOC_DIS**	**TXQ2_IOC_DIS**	**TXQ1_IOC_DIS**	**TXQ0_IOC_DIS**
Type					RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
11	RXQ3_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event based on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFRE1SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
10	RXQ2_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event based on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFRE1SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
9	RXQ1_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event based on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFRE1SR. 0: Enable IOC function. 1: Disable IOC function (always issues an interrupt when GPD is complete)
8	RXQ0_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFRE1SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
7	TXQ7_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issues an interrupt when GPD is complete)
6	TXQ6_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is**

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Bit(s)	Name	Description
		complete. If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
5	TXQ5_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issues an interrupt when GPD is complete)
4	TXQ4_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
3	TXQ3_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues an interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issues an interrupt when GPD is complete)
2	TXQ2_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
1	TXQ1_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR. 0: Enable IOC function. 1: Disable IOC function (always issue interrupt when GPD done)
0	TXQ0_IOC_DIS	**If firmware writes 1 to this register, the corresponding queue always issues interrupt event when GPD is complete.** If firmware writes 0 to this register, the corresponding queue will issue an interrupt event base on GPD IOC bit. If current GPD IOC = 1, GPD done interrupt event will be issued and latched into HWFTE0SR.

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Bit(s)	Name	Description
		0: Enable IOC function. 1: Disable IOC function (always issues an interrupt when GPD is complete)

A10501F0 HSDIOTOCR HIF SDIO Time-Out Control Register 00032000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															REG_WR_TIMEOUT_EN	REG_RD_TIMEOUT_EN
Type															RW	RW
Reset															1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_TIMEOUT_NUM															
Type	RW															
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17	REG_WR_TIMEOUT_EN	**Firmware can write 0 to this field to disable SDIO write timeout function and write 1 to enable the function.** 0: Disable SDIO timeout function. 1: Enable SDIO timeout function.
16	REG_RD_TIMEOUT_EN	**Firmware can write 0 to this field to disable SDIO read timeout function and write 1 to enable the function.** 0: Disable SDIO timeout function. 1: Enable SDIO timeout function.
15:0	REG_TIMEOUT_NUM	**Firmware can write this field to decide the timeout threshold. The unit is SDIO clock cycle number.**

A1050200 HWFTSR0 HIF WLAN Firmware TX Status Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TQ3_CNT								TQ2_CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TQ1_CNT								TQ0_CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TQ3_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by the host driver.**

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Bit(s)	Name	Description
23:16	TQ2_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**
15:8	TQ1_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**
7:0	TQ0_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**

A1050204 HWFTSR1 HIF WLAN Firmware TX Status Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TQ7_CNT								TQ6_CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TQ5_CNT								TQ4_CNT							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TQ7_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**
23:16	TQ6_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**
15:8	TQ5_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**
7:0	TQ4_CNT	**Firmware can read this field to get the accumulated TX queue count in SDIO controller not read by host driver.**

A1050210 HWDBGCR HIF WLAN Debug Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TX1_RECORD_EN	RX1_RECORD_EN	RX0_RECORD_EN	NO_DMU_DBG_MODE
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_PKTLEN_OFFSET															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
19	TX1_RECORD_EN	**Firmware can write 1 to this field to enable TX1 data port record in debug mode.**
18	RX1_RECORD_EN	**Firmware can write 1 to this field to enable RX1 data port**

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Bit(s)	Name	Description
		record in debug mode.
17	RX0_RECORD_EN	**Firmware can write 1 to this field to enable RX0 data port record in debug mode.**
16	NO_DMU_DBG_MODE	Firmware can write 1 to this field to enable the virtual direct DMA debug mode. When this mode is enabled, the data transfer between SDIO controller and SDIO wrapper is also written to the SDIO internal memory in PIO mode for debugging purposes. Firmware can enable the data port to be recorded by writing 1 to the corresponding field in this register. Only one data port should be recorded each single time for the debug mode, so that the record condition can be applied to that port correctly. The record condition would be packet size and packet length offset. Packets that meet both criteria would be recorded.
15:0	DBG_PKTLEN_OFFSET	**Since the memory used for debug is only roughly 2KB and might not be enough to record one full packet size, firmware can set this field to indicate the offset of one packet size to be recorded. This field is limited to be DW alignment size. E.g. firmware writes 20 to this field meaning that the data from byte 21 would be recorded.**

A1050214 HWDBGPLR HIF WLAN Debug Packet Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DBG_LEN_UP_BOUND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DBG_LEN_LOW_BOUND															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	DBG_LEN_UP_BOUND	**Firmware can write into this field to record the upper bound packet size. Packets that meet both the upper and lower bound criteria will be recorded.**
15:0	DBG_LEN_LOW_BOUND	**Firmware can write into this field to record the lower bound packet size. Packets that meet both the upper and lower bound criteria will be recorded.**

A1050218 HSPICSR WLAN SPI Control Status Register (SPI Only) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					D_CPOL_SET_CONTROL	D_CPHA_SET_CONTROL	D_MODE_SET_CONTROL	D_ENDIAN_SET_CONTROL				D_CPOL	D_CPHA	D_BIT_MODE		D_ENDIAN
Type					RO	RO	RO	RO				RO	RO	RO		RO

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Reset					0	0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**CPOL_SET_CONTROL**	**CPHA_SET_CONTROL**	**MODE_SET_CONTROL**	**ENDIAN_SET_CONTROL**				**CPOL**	**CPHA**	**BIT_MODE**		**ENDIAN**
Type					RW	RW	RW	RW				RW	RW	RW		RW
Reset					0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
27	D_CPOL_SET_CONTROL	**[debug bit]** 0: CPOL set by firmware or eFuse 1: CPOL set by wspicsr bit[6]
26	D_CPHA_SET_CONTROL	**[debug bit]** 0: CPHA set by firmware or eFuse 1: CPHA set by wspicsr bit[5]
25	D_MODE_SET_CONTROL	**[debug bit]** 0: BIT MODE set by firmware or eFuse 1: BIT MODE set by wspicsr bit[4:3]
24	D_ENDIAN_SET_CONTROL	**[debug bit]** 0: ENDIAN set by firmware or eFuse 1: ENDIAN set by wspicsr bit[2]
20	D_CPOL	**[debug bit]** CPOL : the final value, depends on bit 4 and bit 11.
19	D_CPHA	**[debug bit]** CPHA : the final value
18:17	D_BIT_MODE	**[debug bit]** BIT_MODE : the final value
16	D_ENDIAN	**[debug bit]** ENDIAN : the final value
11	CPOL_SET_CONTROL	0: CPOL set by eFuse 1: CPOL set by firmware
10	CPHA_SET_CONTROL	0: CPHA set by eFuse 1: CPHA set by firmware
9	MODE_SET_CONTROL	0: BIT MODE set by eFuse 1: BIT MODE set by firmware
8	ENDIAN_SET_CONTROL	0: ENDIAN set by eFuse 1: ENDIAN set by firmware
4	CPOL	**CPOL needs to be coordinated with bit[11]** 0: set CPOL 0 1: set CPOL 1
3	CPHA	**CPHA needs to be coordinated with bit[10]** 0: set CPHA 0 1: set CPHA 1
2:1	BIT_MODE	**this bit needs to be coordinated with bit[9]** 2b'00: 8bit mode 2b'01:16bit mode 2b'10:32bit mode 2b'11: 8bit mode
0	ENDIAN	**this bit needs to be coordinated with bit[8]** 0: Little Endian 1: Big Endian

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Bit(s)	Name	Description

A1050220 HWRX0CGPD DMA RX0 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX0_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX0_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX0_CURR_GPD_ADDR	**the current GPD address for RX0**

A1050224 HWRX1CGPD DMA RX1 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX1_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX1_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX1_CURR_GPD_ADDR	**the current GPD address of RX1**

A1050228 HWRX2CGPD DMA RX2 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX2_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX2_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX2_CURR_GPD_ADDR	**the current GPD address of RX2**

A105022C **HWRX3CGPD** **DMA RX3 Current GPD Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX3_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX3_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX3_CURR_GPD_ADDR	**the current GPD address of RX3**

A1050230 **HWTX0CGPD** **DMA TX0 Current GPD Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX0_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX0_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX0_CURR_GPD_ADDR	**the GPD address of TX0**

A1050234 **HWTX1Q1CGPD** **DMA TX1 Queue Type 1 Current GPD Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX1_Q1_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX1_Q1_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	TX1_Q1_CURR_GPD_ADDR	**the address of TX1 channel and queue type 1 GPD**

A1050238 HWTX1Q2CGPD DMA TX1 Queue Type 2 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX1_Q2_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX1_Q2_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_Q2_CURR_GPD_ADDR	**the address of TX1 channel and queue type 2 GPD**

A105023C HWTX1Q3CGPD DMA TX1 Queue Type 3 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX1_Q3_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX1_Q3_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_Q3_CURR_GPD_ADDR	**the address of TX1 channel and queue type 3 GPD**

A1050240 HWTX1Q4CGPD DMA TX1 Queue Type 4 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX1_Q4_CURR_GPD_ADDR															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX1_Q4_CURR_GPD_ADDR															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_Q4_CURR_GPD_ADDR	**the address of TX1 channel and queue type 4 GPD**

A1050244 HWTX1Q5CGPD DMA TX1 Queue Type 5 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX1_Q5_CURR_GPD_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX1_Q5_CURR_GPD_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_Q5_CURR_GPD_ADDR	**the address of TX1 channel and queue type 5 GPD**

A1050248 HWTX1Q6CGPD DMA TX1 Queue Type 6 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX1_Q6_CURR_GPD_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX1_Q6_CURR_GPD_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_Q6_CURR_GPD_ADDR	**the address of TX1 channel and queue type 6 GPD**

A105024C HWTX1Q7CGPD DMA TX1 Queue Type 7 Current GPD Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TX1_Q7_CURR_GPD_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TX1_Q7_CURR_GPD_ADDR**															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_Q7_CURR_GPD_ADDR	**the address of TX1 channel and queue type 7 GPD**

A10503F4 HSDIOCRCR HIF SDIO CRC status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														REG_CRC_STS_CYCLE		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	REG_CRC_STS_CYCLE	**In SDR50 and SDR104 mode, the CRC status can be sent 2 to 8 cycles after one data block, as described in the SDIO 3.0 specification. Firmware could write this register to change the response timing of SDIO IP. Default value is 2 cycles after one data block.** 0: 2 cycles after data block 1: 3 cycles after data block 2: 4 cycles after data block 3: 5 cycles after data block 4: 6 cycles after data block 5: 7 cycles after data block 6: 8 cycles after data block 7: 9 cycles after data block

A10503F8 HSDIORCR HIF SDIO Read Control Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							REG_SDIO_RD_TIMING_SEL									REG_TIMEOUT_NUM_EN
Type							RW									RW
Rese							0	0								1

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t																

Bit(s)	Name	Description
9:8	REG_SDIO_RD_TIMING_SEL	**Use this register, if the firmware is unable to prepare the data on time for the host to read. The SDIO prefetch operation can be delayed according to the data depth in current RX FIFO. Firmware can write to this field to change the data depth constraint.** 2b'00: 4B 2b'01: 8B 2b'10:16B 2b'11: 64B
0	REG_TIMEOUT_NUM_EN	**Use this register, if the firmware is unable to prepare the data on time for the host to read. The SDIO read timing adjustment function is implemented to protect the read data underflow. Firmware can write 1 to enable and write 0 to disable the function.** 0: Disable SDIO Read timing adjustment function. 1: Enable SDIO Read timing adjustment function.

16.6.2. Host domain register

Module name: SDIO_SLV Base address: (+0h)

Address	Name	Width (bits)	Register Functionality
00000000	WCIR	32	WLAN Chip ID Register
00000004	WHLPCR	32	WLAN HIF Low Power Control Register
00000008	WSDIOCSR	32	WLAN SDIO Control Status Register (SDIO Only)
0000000C	WHCR	32	WLAN HIF Control Register
00000010	WHISR	32	WLAN HIF Interrupt Status Register
00000014	WHIER	32	WLAN HIF Interrupt Enable Register
00000018	WHISR1	32	Reserved for WHISR1
0000001C	WHIER1	32	Reserved for WHIER1
00000020	WASR	32	WLAN Abnormal Status Register
00000024	WSICR	32	WLAN Software Interrupt Control Register
00000028	WTSR0	32	WLAN TX Status Register
0000002C	WTSR1	32	WLAN TX Status Register
00000030	WTDR0	32	Reserved
00000034	WTDR1	32	WLAN TX Data Register 1
00000038	WTDR2	32	Reserved for WTDR2
0000003C	WTDR3	32	Reserved for WTDR3
00000040	WTDR4	32	Reserved for WTDR4
00000044	WTDR5	32	Reserved for WTDR5
00000048	WTDR6	32	Reserved for WTDR6
0000004C	WTDR7	32	Reserved for WTDR7
00000050	WRDR0	32	WLAN RX Data Register 0
00000054	WRDR1	32	WLAN RX Data Register 1
00000058	WRDR2	32	Reserved

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Address	Name	Width (bits)	Register Functionality
0000005C	WRDR3	32	Reserved
00000060	WRDR4	32	Reserved for WRDR4
00000064	WRDR5	32	Reserved for WRDR5
00000068	WRDR6	32	Reserved for WRDR6
0000006C	WRDR7	32	Reserved for WRDR7
00000070	H2DSM0R	32	Host to Device Send Mailbox 0 Register
00000074	H2DSM1R	32	Host to Device Send Mailbox 1 Register
00000078	D2HRM0R	32	Device to Host Receive Mailbox 0 Register
0000007C	D2HRM1R	32	Device to Host Receive Mailbox 1 Register
00000080	D2HRM2R	32	Reserved
00000090	WRPLR	32	WLAN RX Packet Length Register
00000094	WRPLR1	32	WLAN RX Packet Length Register 1
00000098	WRPLR2	32	Reserved for WRPLR2
0000009C	WRPLR3	32	Reserved for WRPLR3
000000A0	EHTCR	32	EHPI transaction count register (EHPI Only)
000000AC	WOLTCR	32	On-Line Tuning Control Register
000000B0	WTMDR	32	Test Mode Data Port
000000B4	WTMCR	32	Test Mode Control Register
000000B8	WTMDPCR0	32	Test Mode Data Pattern Control Register 0
000000BC	WTMDPCR1	32	Test Mode Data Pattern Control Register 1
000000C0	FWDLDR	32	Firmware Download Data Register
000000C4	FWDLDSAR	32	Firmware Download Destination Starting Address Register
000000C8	FWDLSR	32	Firmware Download Status Register
000000CC	FWDLCMR0	32	Firmware Download Customized Register 0
000000D0	FWDLCMR1	32	Firmware Download Customized Register 1
000000D4	WPLRCR	32	WLAN Packet Length Report Control Register
000000D8	WSR	32	WLAN Snapshot Register
000000F8	VSCR	32	Version Control Register
000000FC	WSDIOAICR	32	Common SDIO Asynchronous Interrupt Control Register
00000100	CLKIOCR_T28LP	32	Clock Pad Macro IO Control Register
00000104	CMDIOCR_T28LP	32	Command Pad Macro IO Control Register
00000108	DAT0IOCR_T28LP	32	Data 0 Pad Macro IO Control Register
0000010C	DAT1IOCR_T28LP	32	Data 1 Pad Macro IO Control Register
00000110	DAT2IOCR_T28LP	32	Data 2 Pad Macro IO Control Register
00000114	DAT3IOCR_T28LP	32	Data 3 Pad Macro IO Control Register
00000118	CLKDLYCR	32	Clock Pad Macro Delay Chain Control Register
0000011C	CMDDLYCR	32	Command Pad Macro Delay Chain Control Register
00000120	ODATDLYCR	32	SDIO Output Data Delay Chain Control Register
00000124	IDATDLYCR1	32	SDIO Input Data Delay Chain Control Register 1
00000128	IDATDLYCR2	32	SDIO Input Data Delay Chain Control

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Address	Name	Width (bits)	Register Functionality
			Register 2
0000012C	**ILCHCR**	32	**SDIO Input Data Latch Time Control Register**
00000130	**WTQCR0**	32	**WLAN TXQ Count Register 0**
00000134	**WTQCR1**	32	**WLAN TXQ Count Register 1**
00000138	**WTQCR2**	32	**WLAN TXQ Count Register 2**
0000013C	**WTQCR3**	32	**WLAN TXQ Count Register 3**
00000140	**WTQCR4**	32	**WLAN TXQ Count Register 4**
00000144	**WTQCR5**	32	**WLAN TXQ Count Register 5**
00000148	**WTQCR6**	32	**WLAN TXQ Count Register 6**
0000014C	**WTQCR7**	32	**WLAN TXQ Count Register 7**
00000154	**SWPCDBGR**	32	**WLAN PC Value Debug Register**
00000158	**DSIOCR**	32	**DS Pad Macro IO Control Register**

00000000 WCIR WLAN Chip ID Register 00106630

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DEVICE_STATUS										W_FUNC_RDY	POR_INDICATOR	REVISION_ID			
Type	RO										RO	W1C	RO			
Reset	0	0	0	0	0	0	0	0			0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CHIP_ID															
Type	RO															
Reset	0	1	1	0	0	1	1	0	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31:24	DEVICE_STATUS	**These status bits are defined by users and could be read by host driver using SDIO bus interface. For example, watchdog reset status could be the one read by the host driver even when there is no AHB clock in SDIO controller.**
21	W_FUNC_RDY	**Indicates that WLAN functional block has finished its initial procedure and is ready for normal operation.** This is a sticky bit of HWFCR.W_FUNC_RDY. Driver will keep polling this bit on initialization. Once firmware is ready and corresponding bit in firmware is set, driver can do the following controls to firmware. 0: WLAN functional block is not ready for normal operation. 1: WLAN functional block is ready for normal operation.
20	POR_INDICATOR	**This bit indicates a reset including an external pin reset, power detect reset, power on reset, SDIO CCCR (0x06). Bit[3] reset (only in SDIO).** Write 1 to clear this bit. Writing 0 does nothing.
19:16	REVISION_ID	**Revision ID**
15:0	CHIP_ID	**Chip ID**

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00000004 WHLPCR **WLAN HIF Low Power Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							W_FW_OWN_REQ_CLR	W_FW_OWN_REQ_SET							W_INT_EN_CLR	W_INT_EN_SET
Type							W1S	W1S							W1S	W1S
Reset							0	0							0	0

Bit(s)	Name	Description
9	W_FW_OWN_REQ_CLR	**Write 1 to this bit to request firmware to return the ownership of chip WLAN function to host driver. Writing 0 does nothing.** Read always returns 0. This bit will be set on initialization, or by firmware writing 1 to HWFICR. FW_OWN_BACK_INT_SET or any driver-domain WLAN interrupts.
8	W_FW_OWN_REQ_SET	**Write 1 to this bit to transfer ownership of chip WLAN function to firmware. Writing 0 does nothing. Host driver should set this bit to give ownership to firmware only when the host driver has ownership.** Read will get the status of WLAN_DRV_OWN. WLAN_DRV_OWN indicates that software driver has the ownership of chip WLAN sub-system. 0: WLAN driver doesn't have ownership 1: WLAN driver has ownership
1	W_INT_EN_CLR	**Writing 0 does nothing. Write 1 to clear WLAN interrupt enable signal.** Read always returns 0.
0	W_INT_EN_SET	**Writing 0 does nothing. Write 1 to set WLAN interrupt enable signal.** Read will get the status of W_INT_EN. W_INT_EN indicates the current value of WLAN interrupt enable signal. This enable signal is used for controlling the output of WLAN interrupt signal. 0: WLAN interrupt cannot output to host. 1: WLAN interrupt can output to host.

00000008 WSDIOCSR **WLAN SDIO Control Status Register (SDIO Only)** **0000000D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam																

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e																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**DB_CMD7_RESELECT_DIS**	**DB_WR_BUSY_EN**	**DB_RD_BUSY_EN**	**SDIO_INT_CTL**	**SDIO_RE_INIT_EN**
Type												RW	RW	RW	RW	RO
Reset												0	1	1	0	1

Bit(s)	Name	Description
4	DB_CMD7_RESELECT_DIS	**Control the cmd7 with response when the card is in re-select** 0: Host use cmd7 reselect and card will have response. 1: Host use cmd7 reselect and card will NOT have response.
3	DB_WR_BUSY_EN	**Write busy function control bit. If the available space of internal TX FIFO is smaller than the pre-defined maximum block size, the write busy will be asserted. The write busy function can be used only when the block size is smaller than pre-defined FIFO size (i.e. maximum block size).** 0: DMA write busy function disable 1: DMA write busy function enable
2	DB_RD_BUSY_EN	**Read busy function control bit. If the usage of internal RX FIFO is smaller than the pre-defined maximum block size, the read busy would be triggered except the data is the last part of this transaction. The read busy function can be used only when the block size is smaller than pre-defined FIFO size (i.e. maximum block size).** 0: DMA read busy function disable 1: DMA read busy function enable
1	SDIO_INT_CTL	**Asynchronous interrupt is supported in SDIO 4-bit mode** 0: Not supported; The host should switch to 1-bit mode before it turns off SD clock. Device can wake up host via 1-bit mode asynchronous interrupt. (according to SDIO v2.0 spec) 1: Supported; The host could send asynchronous interrupt to host during asynchronous interrupt period so that the host does not need to switch to 1-bit mode before it turns off SD clock. (according to SDIO v3.0 spec)
0	SDIO_RE_INIT_EN	**When asserted, this bit is used to let SDIO IP return to idle state when a new SDIO CMD 5 is received.** You can use the fixed default value set with an engine, or use an external bus.

0000000C WHCR **WLAN HIF Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**RX_ENHANCE_M**

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																ODE
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**MAX_HIF_RX_LEN_NUM**										**RPT_OWN_RX_PACKET_LEN**	**RECV_MAILBOX_RD_CLR_EN**	**W_INT_CLR_CTRL**	
Type			RW										RW	RW	RW	
Reset			0	0	0	0	0	0					0	0	0	

Bit(s)	Name	Description
16	RX_ENHANCE_MODE	**Enables the read of TX count status, RX length, and mailbox information in RX packet enhance mode.** 0: Disables RX packet enhanced mode 1: Enables the read of TX count status, RX length and mailbox information in RX packet enhanced mode.
13:8	MAX_HIF_RX_LEN_NUM	**The maximum number of SDIO controllers to report the per-queue RX packets length in INT/RX enhanced mode.** 0: report entire 64 RX packets length in the same RX queue without limitation. Others (N): report at most N RX packet lengths for each RX queue.
3	RPT_OWN_RX_PACKET_LEN	**This field is to control the RX packet report length and structure in enhanced mode. If this bit is set to 1, each RX queue can report its own length according to the setting in WPLRCR. Also, the total report length will change, if this bit is set. Host driver should parse the enhanced mode status according to the length setting in WPLRCR to get correct information.** 0: disable the function that each RX queue can report its own packet length and the maximal report length is constrained by max_hif_rx_len_num field in WHCR. 1: enable the function that each RX queue can report its own packet length and the maximal report length can be different by each queue according to the setting in WPLRCR.
2	RECV_MAILBOX_RD_CLR_EN	**This is to control whether the received mailbox (D2HRM0R, D2HRM1R) will be read cleared (this includes read from enhanced mode structure).** 1: read clear 0: no effect after read
1	W_INT_CLR_CTRL	**This bit is used to select the clear mechanism of WLAN interrupt status (WHISR).** 0: Read clear 1: Write 1 clear

00000010 WHISR WLAN HIF Interrupt Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D2H_SW_INT**															
Type	RC															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**D2H_SW_INT**								**FW_OWN_BACK_INT**	**ABNORMAL_INT**		**RX3_DONE_INT**	**RX2_DONE_INT**	**RX1_DONE_INT**	**RX0_DONE_INT**	**TX_DONE_INT**
Type	RC								RC	RO		RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0

Bit(s)	Name	Description
31:8	D2H_SW_INT	**This field is used for software interrupt for WLAN function in firmware to host driver direction.** WLAN firmware writing 1s to HWFICR.Bit[31:8] will set corresponding bit field.
7	FW_OWN_BACK_INT	**Firmware has returned the ownership to host driver. This field is set with driver ownership-back only.** Firmware writing 1 to HWFICR. Bit[4] will set this bit.
6	ABNORMAL_INT	**Abnormal event interrupt.** The abnormal status will be shown in WASR including: Data overflow of WLAN TX0 and TX1 port. Data underflow of WLAN RX0 and RX1 port. FW_OWN_INVALID_ACCESS
4	RX3_DONE_INT	**When any of the RX length data of RX3 exists in HIF RX length FIFO, this bit will be asserted.**
3	RX2_DONE_INT	**When any of the RX length data of RX2 exists in HIF RX length FIFO, this bit will be asserted.**
2	RX1_DONE_INT	**When any of the RX length data of RX1 exists in HIF RX length FIFO, this bit will be asserted.**
1	RX0_DONE_INT	**When any of the RX length data of RX0 exists in HIF RX length FIFO, this bit will be asserted.**
0	TX_DONE_INT	**If WTSR0 or WTSR1 is not 0, this bit will be set.** 0: WTSR0 and WTSR1 is 0. 1: WTSR0 or WTSR1 is not 0.

00000014 WHIER WLAN HIF Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D2H_SW_INT_EN**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**D2H_SW_INT_EN**								**FW_OWN_BACK_INT_EN**	**ABNORMAL_INT_EN**		**RX3_DONE_INT_EN**	**RX2_DONE_INT_EN**	**RX1_DONE_INT_EN**	**RX0_DONE_INT_EN**	**TX_DONE_INT_EN**
Type	RW								RW	RW		RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0

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Bit(s)	Name	Description
31:8	D2H_SW_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
7	FW_OWN_BACK_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
6	ABNORMAL_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
4	RX3_DONE_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
3	RX2_DONE_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
2	RX1_DONE_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
1	RX0_DONE_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.
0	TX_DONE_INT_EN	**WLAN host interrupt output control bits.** If any bit is 0: Mask the WLAN related bit interrupt output, corresponding bits will still be written to WHISR without triggering interrupt. 1: Enable the WLAN related bit interrupt output.

00000018 WHISR1 Reserve for WHISR1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WHISR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WHISR1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WHISR1	**RESV_WHISR1**

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Bit(s)	Name	Description

0000001C WHIER1 **Reserve for WHIER1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WHIER1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WHIER1															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WHIER1	**RESV_WHIER1**

00000020 WASR **WLAN Abnormal Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																FW_OWN_INVALID_ACCESS
Type																RC
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RX3_UNDERFLOW	RX2_UNDERFLOW	RX1_UNDERFLOW	RX0_UNDERFLOW							TX1_OVERFLOW	TX0_OVERFLOW
Type					RC	RC	RC	RC							RC	RC
Reset					0	0	0	0							0	0

Bit(s)	Name	Description
16	FW_OWN_INVALID_ACCESS	**This will be asserted when registers other than WCIR, WHLPCR, WSPICSR, WSDIOCSR, WEHPICSR and firmware download relative registers are accessed when FW_OWN_INVALID_ACCESS = 1** This is purely for host driver debug purpose.
11	RX3_UNDERFLOW	**Data underflow of WLAN RX3 port.**
10	RX2_UNDERFLOW	**Data underflow of WLAN RX2 port.**
9	RX1_UNDERFLOW	**Data underflow of WLAN RX1 port.**
8	RX0_UNDERFLOW	**Data underflow of WLAN RX0 port.**
1	TX1_OVERFLOW	**Data overflow of WLAN TX1 port.**
0	TX0_OVERFLOW	**Data overflow of WLAN TX0 port.**

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Bit(s)	Name	Description

00000024 WSICR **WLAN Software Interrupt Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SW_INT_SET															
Type	W1S															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:16	H2D_SW_INT_SET	**Host driver writing 1s will set HWFISR. HOST_DRIVER_INT.** Writing 0 does nothing. Read always returns 0. This is used as communication between firmware and driver, with an interrupt functionality to SDIO controller.

00000028 WTSR0 **WLAN TX Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TQ3_CNT								TQ2_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TQ1_CNT								TQ0_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TQ3_CNT	**This field indicates the released packet count of TQ3 during two WTSR0 read accesses.** This field is cleared by read operation. Write does nothing.
23:16	TQ2_CNT	**This field indicates the released packet count of TQ2 during two WTSR0 read accesses.** This field is cleared by read operation. Write does nothing.
15:8	TQ1_CNT	**This field indicates the released packet count of TQ1 during two WTSR0 read accesses.** This field is cleared by read operation. Write does nothing.
7:0	TQ0_CNT	**This field indicates the released packet count of TQ0 during two WTSR0 read accesses.** This field is cleared by read operation. Write does nothing.

0000002C WTSR1 **WLAN TX Status Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TQ7_CNT								TQ6_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TQ5_CNT								TQ4_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	TQ7_CNT	**This field indicates the released packet count of TQ7 during two WTSR0 read accesses.** This field is cleared by read operation. Write does nothing.
23:16	TQ6_CNT	**This field indicates the released packet count of TQ6 during two WTSR0 read accesses.** This field is cleared by read operation. Write does nothing.
15:8	TQ5_CNT	**This field indicates the released packet count of TQ5 during two WTSR1 read accesses.** This field is cleared by read operation. Write does nothing.
7:0	TQ4_CNT	**This field indicates the released packet count of TQ4 during two WTSR1 read accesses.** This field is cleared by read operation. Write does nothing.

00000030 WTDR0 WLAN TX Data Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX0_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX0_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX0_DATA	**TX0 write data port. Read always returns 0.** Data must be padded to multiples of block size when the data to write is more than the size of a single block. Writing data with multiple blocks in one transaction and the remaining in another is prohibited with byte mode.

00000034 WTDR1 WLAN TX Data Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX1_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TX1_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX1_DATA	**TX1 write data port. Read always returns 0.** Data must be padded to multiples of block size when the data to write is more than the size of a single block. Writing data with multiple blocks in one transaction and the remaining in another is prohibited with byte mode.

00000038 WTDR2 Reserve for WTDR2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WTDR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WTDR2															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WTDR2	**RESV_WTDR2**

0000003C WTDR3 Reserve for WTDR3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WTDR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WTDR3															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WTDR3	**RESV_WTDR3**

00000040 WTDR4 Reserve for WTDR4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WTDR4															
Type	WO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESV_WTDR4**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WTDR4	**RESV_WTDR4**

00000044 WTDR5 **Reserve for WTDR5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESV_WTDR5**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESV_WTDR5**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WTDR5	**RESV_WTDR5**

00000048 WTDR6 **Reserve for WTDR6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESV_WTDR6**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RESV_WTDR6**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WTDR6	**RESV_WTDR6**

0000004C WTDR7 **Reserve for WTDR7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RESV_WTDR7**															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WTDR7															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WTDR7	**RESV_WTDR7**

00000050 WRDR0 WLAN RX Data Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX0_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX0_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX0_DATA	**RX0 read data port. Write has no effect.** The RX0 data port supports data aggregation. Driver should read all RX packet by last SDIO controller indicated information. The number of total RX aggregation packets is restricted by WHCR. MAX_HIF_RX_LEN_NUM. Length to read must be extended to multiples of block size when the data to read is more than the size of a single block. Reading data with multiple blocks in one transaction and the remaining in another is prohibited with byte mode. Also, as long as host driver knows the total available packet number and length via enhanced interrupt response and/or RX packet enhanced mode, host driver must read all RX packets in a single transaction. Reading for partial packets is prohibited.

00000054 WRDR1 WLAN RX Data Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX1_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX1_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RX1_DATA	**RX1 read data port. Write has no effect.** The RX1 data port supports data aggregation. Driver should read all RX packets by last SDIO controller indicated information. The number of total RX aggregation packets is restricted by WHCR. MAX_HIF_RX_LEN_NUM. (see chapter 3.1 for details) Data length to read must be extended to multiples of block size when the data to read is more than the size of a single block. Reading data with multiple blocks in one transaction and the remaining in another is prohibited with byte mode. Also, as long as host driver knows the total available packet number and length via enhanced interrupt response and/or RX packet enhanced mode, host driver must read all RX packets in a single transaction. Reading for partial packets is prohibited.

00000058 WRDR2 **WLAN RX Data Register 2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX2_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX2_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX2_DATA	**RX2 read data port. Write has no effect.** The RX2 data port supports data aggregation. Driver should read all RX packets by last SDIO controller indicated information. The number of total RX aggregation packets is restricted by WHCR. MAX_HIF_RX_LEN_NUM. (see chapter 3.1 for details) Data length to read must be extended to multiples of block size when the data to read is more than the size of a single block. Reading data with multiple blocks in one transaction and the remaining in another is prohibited with byte mode. Also, as long as host driver knows the total available packet number and length via enhanced interrupt response and/or RX packet enhanced mode, host driver must read all RX packets in a single transaction. Reading for partial packets is prohibited.

0000005C WRDR3 **WLAN RX Data Register 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX3_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX3_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX3_DATA	**RX3 read data port. Write has no effect.** The RX3 data port supports data aggregation. Driver should read all RX packets by last SDIO controller indicated information. The number of total RX aggregation packets is restricted by WHCR. MAX_HIF_RX_LEN_NUM. (see chapter 3.1 for details) Data length to read must be extended to multiples of block size when the data to read is more than the size of a single block. Reading data with multiple blocks in one transaction and the remaining in another is prohibited with byte mode. Also, as long as host driver knows the total available packet number and length via enhanced interrupt response and/or RX packet enhanced mode, host driver must read all RX packets in a single transaction. Reading for partial packets is prohibited.

00000060 WRDR4 **Reserve for WRDR4** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WRDR4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WRDR4															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WRDR4	**RESV_WRDR4**

00000064 WRDR5 **Reserve for WRDR5** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WRDR5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WRDR5															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	RESV_WRDR5	**RESV_WRDR5**

00000068 WRDR6 **Reserve for WRDR6** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WRDR6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WRDR6															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WRDR6	**RESV_WRDR6**

0000006C WRDR7 **Reserve for WRDR7** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WRDR7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WRDR7															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WRDR7	**RESV_WRDR7**

00000070 H2DSM0R **Host to Device Send Mailbox 0 Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H2D_SM0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:0	H2D_SM0	**This register is used by host driver to transmit data to SDIO controller, which will be updated to H2DRM0R and read by firmware.**

00000074 H2DSM1R Host to Device Send Mailbox 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	H2D_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	H2D_SM1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	H2D_SM1	**This register is used by host driver to transmit data to SDIO controller, which will be updated to H2DRM1R and read by firmware.**

00000078 D2HRM0R Device to Host Receive Mailbox 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_RM0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	D2H_RM0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_RM0	**This register is used by host driver to receive data from SDIO controller, which is updated through D2HSM0R by firmware.** The property of RO/RC is by control of WHCR. RECV_MAILBOX_RD_CLR_EN bit.

0000007C D2HRM1R Device to Host Receive Mailbox 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	D2H_RM1															
Type	RO															
Rese	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**D2H_RM1**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_RM1	**This register is used by host driver to receive data from SDIO controller, which is updated through D2HSM1R by firmware.** The property of RO/ RC is by control of WHCR. RECV_MAILBOX_RD_CLR_EN bit.

00000080 D2HRM2R Device to Host Receive Mailbox 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**D2H_RM2**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**D2H_RM2**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	D2H_RM2	**This register is used by host driver to receive data from SDIO controller, which is updated through D2HSM2R by firmware. For synchronization of hardware, it's recommended to read this register more than once to let more host clock cycles to device get the latest result, especially for EHPI interface.** Note that this register could be read when there is no AHB clock, i.e. host driver could get this message when chip is in low power mode.

00000090 WRPLR WLAN RX Packet Length Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**RX1_PACKET_LENGTH**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**RX0_PACKET_LENGTH**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
31:16	RX1_PACKET_LENGTH	**This register is used to get the next RX packet length in the RX1 length FIFO, which is updated by FW HWRQ1CR.** When this field is read, it will report only 1 RX packet length in this RX queue, and at most 1 packet will return by next RX port read.
15:0	RX0_PACKET_LENGTH	**This register is used to get the next RX packet length in the RX0 length FIFO, which is updated by FW HWRQ0CR.** When this field is read, it will report only 1 RX packet length in this RX queue, and at most 1 packet will return by next RX port read.

00000094 WRPLR1 WLAN RX Packet Length Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX3_PACKET_LENGTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX2_PACKET_LENGTH															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	RX3_PACKET_LENGTH	**This register is used to get the next RX packet length in the RX3 length FIFO, which is updated by FW HWRQ3CR.** When this field is read, it will report only 1 RX packet length in this RX queue, and at most 1 packet will return by next RX port read.
15:0	RX2_PACKET_LENGTH	**This register is used to get the next RX packet length in the RX2 length FIFO, which is updated by FW HWRQ2CR.** When this field is read, it will report only 1 RX packet length in this RX queue, and at most 1 packet will return by next RX port read.

00000098 WRPLR2 Reserve for WRPLR2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RESV_WRPLR2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WRPLR2															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WRPLR2	**RESV_WRPLR2**

0000009C WRPLR3 Reserve for WRPLR3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam	RESV_WRPLR3															

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e																
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESV_WRPLR3															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RESV_WRPLR3	**RESV_WRPLR3**

000000A0 EHTCR **EHPI transaction count register (EHPI only)** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EHPI_TRANS_CNT_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EHPI_TRANS_CNT_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
31:0	EHPI_TRANS_CNT_REG	This register is used for SDIO controller to get the transaction boundary of EHPI burst access. Accessing normal registers is limited within 4B boundary. For data port access (WTDR0, WTDR1, WRDR0 and WRDR1 etc.) and WHISR enhanced access, the length can be more than 4B. Hence, host needs to set the length before accessing these registers and SDIO controller would take the length as transaction length. The transaction count should be set with 4B alignment.

000000AC WOLTCR **On-Line Tuning Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												DAT3_OUT_OF_BOUND	DAT2_OUT_OF_BOUND	DAT1_OUT_OF_BOUND	DAT0_OUT_OF_BOUND	CMD_OUT_OF_BOUND
Type												W1C	W1C	W1C	W1C	W1C
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TRAIN_			TRAIN_WINDOW					

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								EN								
Type								RW			RW					
Reset								0			0	0	0	0	0	0

Bit(s)	Name	Description
20	DAT3_OUT_OF_BOUND	**This field is to notify host driver that the train window of data 3 is out of available delay gears.** The boundary of delay gears would be 0 and 31. If the applied training window is out of boundary then this field would be asserted. Host driver can read these fields to know if any delay training is out of boundary. Also, the host driver can write 1 to this field to clear status. This field is primary for no training window indication.
19	DAT2_OUT_OF_BOUND	**This field is to notify host driver that the train window of data 2 is out of available delay gears.** The boundary of delay gears would be 0 and 31. If the applied training window is out of boundary then this field would be asserted. Host driver can read these fields to know if any delay training is out of boundary. Also, the host driver can write 1 to this field to clear status. This field is primary for no training window indication.
18	DAT1_OUT_OF_BOUND	**This field is to notify host driver that the train window of data 1 is out of available delay gears.** The boundary of delay gears would be 0 and 31. If the applied training window is out of boundary then this field would be asserted. Host driver can read these fields to know if any delay training is out of boundary. Also, the host driver can write 1 to this field to clear status. This field is primary for no training window indication.
17	DAT0_OUT_OF_BOUND	**This field is to notify host driver that the train window of data 0 is out of available delay gears.** The boundary of delay gears would be 0 and 31. If the applied training window is out of boundary then this field would be asserted. Host driver can read these fields to know if any delay training is out of boundary. Also, the host driver can write 1 to this field to clear the status. This field is primary for no training window indication.
16	CMD_OUT_OF_BOUND	**This field is to notify host driver that the train window of command is out of available delay gears.** The boundary of delay gears would be 0 and 31. If the applied training window is out of boundary then this field would be asserted. Host driver can read these fields to know if any delay training is out of boundary. Also, the host driver can write 1 to this field to clear status. This field is primary for no training window indication.
8	TRAIN_EN	**Host driver can set this field to enable SDIO on-line tuning function.** This is a field for SDIO on-line tuning function implying that hardware could automatically tune the delay training gear to know whether the surrounding delay gears are safe or not.
5:0	TRAIN_WINDOW	**Host driver can set this field to set the training window size which decides how many gears would be involved.** This is a field for SDIO on-line tuning function implying that hardware could automatically tune the delay training gear for testing. The total delay gears for one data bus is 32, so the maximal training window size would be 32. For example, if the current delay gear is 15 and the train window is set to 5, when on-line delay training is enabled, five-time training delay gears would be 13, 14, 15, 16, and 17.

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000000B0 WTMDR **Test Mode Data Port** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST_MODE_DATA_PORT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST_MODE_DATA_PORT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TEST_MODE_DATA_PORT	**For Test Mode Read/Write.** According to the configuration of WTMCR[1:0]: -64-bits configurable data register -32-bits configurable data register -PRBS

000000B4 WTMCR **Test Mode Control Register** **00080000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								TEST_MODE_FW_OWN	PRBS_INIT_VAL							
Type								RO	RW							
Reset								0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TEST_MODE_STATUS							TEST_MODE_SELECT	
Type								RO							RW	
Reset								0							0	0

Bit(s)	Name	Description
24	TEST_MODE_FW_OWN	**Indicate the ownership of Test Mode Control Registers: WTMCR,WTMDPCR0,WTMDPCR1** 0: Host has the ownership 1: Firmware has the ownership
23:16	PRBS_INIT_VAL	**Initial Value For PRBS Generator**
8	TEST_MODE_STATUS	**To record the compare result of latest Test Mode write. This is read only for Host and Firmware.** 0: Data compare of Test Mode write is Pass 1: Data compare of Test Mode write is Fail
1:0	TEST_MODE_SELECT	**Select test mode data pattern** -64-bits configurable data register

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Bit(s)	Name	Description
		(WTMDPCR0:WTMDPCR1) -32-bits configurable data register -PRBS 00: 32bit data pattern 01: 64bit data pattern 10: PRBS data pattern 11: reserved

000000B8 WTMDPCR0 Test Mode Data Pattern Control Register 0 F0F0F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST_MODE_DATA_PATTERN_0															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST_MODE_DATA_PATTERN_0															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	TEST_MODE_DATA_PATTERN_0	**Data pattern for Test Mode read**

000000BC WTMDPCR1 Test Mode Data Pattern Control Register 1 F0F0F0F0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TEST_MODE_DATA_PATTERN_1															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TEST_MODE_DATA_PATTERN_1															
Type	RW															
Reset	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0

Bit(s)	Name	Description
31:0	TEST_MODE_DATA_PATTERN_1	**Data pattern for Test Mode write**

000000C0 FWDLDR Firmware Download Data Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWDL_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWDL_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWDL_DATA	**This register is used by host to send SDIO controller TX_HEADER with firmware scatter to specified destination address.** The first double word (DW) of the TX data is treated as HIF TX header, which shares the same format with TX packet format. SDIO controller would transmit these data to the destination address starting from FWDLDSAR in turn. Host could aggregate multiple transmission data packets in one transaction. Note that it is not allowed to cut data packet in different transactions as normal TX case. For firmware download, host could access this register without driver ownership = 1, but ensure that system AHB clock for SDIO controller, AHB bus and destination memory are on by using FWDLCMR0 and FWDLCMR1 first.

000000C4 FWDLDSAR **Firmware Download Destination Starting Address Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FWDL_DEST_STARTING_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWDL_DEST_STARTING_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	FWDL_DEST_STARTING_ADDR	**This register is used by host to specify firmware download destination starting address. Note that it should be 4B-aligned address.** Destination address is automatically increased after TX data is written to AHB, and could be read back by host software for reference. It's updated for each packet. For firmware download, host could access this register without driver ownership = 1, but ensure that system AHB clock for SDIO controller, AHB bus and destination memory are on by using FWDLCMR0 and FWDLCMR1 first.

000000C8 FWDLSR **Firmware Download Status Register** **00000100**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**FWDL_RDY**								**FWDL_MODE**
Type								RO								RW
Reset								1								0

Bit(s)	Name	Description
8	FWDL_RDY	**Host driver needs to check if this bit is 1 to set new FWDLDSAR for firmware download of new segment. Then it could write firmware content to SDIO controller.** 0: NOT ready to write firmware from host to SDIO controller. 1: Ready to write firmware from host to SDIO controller.
0	FWDL_MODE	**For firmware download, host could access this register without driver ownership = 1, but ensure the system AHB clock for SDIO controller, AHB bus and destination memory are on by using FWDLCMR0 and FWDLCMR1. Then host driver can turn on this bit to switch to firmware download mode to execute firmware download. Note that the normal TX/RX path cannot work in this mode, host driver has to turn off this mode after firmware download is complete.** 0: Firmware download mode is disabled 1: Firmware download mode is enabled

000000CC **FWDLCMR0** **Firmware Download Customized Register 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**FWDL_CMR0_15**	**FWDL_CMR0_14**	**FWDL_CMR0_13**	**FWDL_CMR0_12**	**FWDL_CMR0_11**	**FWDL_CMR0_10**	**FWDL_CMR0_9**	**FWDL_CMR0_8**	**FWDL_CMR0_7**	**FWDL_CMR0_6**	**FWDL_CMR0_5**	**FWDL_CMR0_4**	**FWDL_CMR0_3**	**FWDL_CMR0_2**	**FWDL_CMR0_1**	**FWDL_CMR0_0**
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	FWDL_CMR0_15	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some registers to request clock

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Bit(s)	Name	Description
		controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
14	FWDL_CMR0_14	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
13	FWDL_CMR0_13	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no driver ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined by the customer and the state is transparent to SDIO controller.
12	FWDL_CMR0_12	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
11	FWDL_CMR0_11	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no driver ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
10	FWDL_CMR0_10	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
9	FWDL_CMR0_9	**Function of this register is user-defined and is used in firmware download stage.**

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Bit(s)	Name	Description
		When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
8	FWDL_CMR0_8	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
7	FWDL_CMR0_7	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
6	FWDL_CMR0_6	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined by the customer and the state is transparent to SDIO controller.
5	FWDL_CMR0_5	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
4	FWDL_CMR0_4	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage.

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Bit(s)	Name	Description
3	FWDL_CMR0_3	And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller. **Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage.
2	FWDL_CMR0_2	And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller. **Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage.
1	FWDL_CMR0_1	And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller. **Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage.
0	FWDL_CMR0_0	And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller. **Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.

000000D0 FWDLCMR1 **Firmware Download Customized Register 1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL	FWDL

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	_CMR1_15	_CMR1_14	_CMR1_13	_CMR1_12	_CMR1_11	_CMR1_10	_CMR1_9	_CMR1_8	_CMR1_7	_CMR1_6	_CMR1_5	_CMR1_4	_CMR1_3	_CMR1_2	_CMR1_1	_CMR1_0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	FWDL_CMR1_15	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
14	FWDL_CMR1_14	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
13	FWDL_CMR1_13	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
12	FWDL_CMR1_12	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
11	FWDL_CMR1_11	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-

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Bit(s)	Name	Description
		defined and the state is transparent to SDIO controller.
10	FWDL_CMR1_10	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
9	FWDL_CMR1_9	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
8	FWDL_CMR1_8	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
7	FWDL_CMR1_7	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
6	FWDL_CMR1_6	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
5	FWDL_CMR1_5	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware.

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Bit(s)	Name	Description
		For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
4	FWDL_CMR1_4	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
3	FWDL_CMR1_3	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
2	FWDL_CMR1_2	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.
1	FWDL_CMR1_1	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined, and the state is transparent to SDIO controller.
0	FWDL_CMR1_0	**Function of this register is user-defined and is used in firmware download stage.** When there is no system AHB clock after power-on and host driver has no ownership, firmware could set this register to notify hardware and read this register from hardware. For example, host driver could set some register to request clock controller to turn on AHB clock of system bus and memory storage. And it could be read if the platform state is in sleep state, firmware download state or full operation state. These bits are all user-defined and the state is transparent to SDIO controller.

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000000D4 WPLRCR **WLAN Packet Length Report Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			RX3_RPT_PKT_LEN								RX2_RPT_PKT_LEN					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RX1_RPT_PKT_LEN								RX0_RPT_PKT_LEN					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Name	Description
29:24	RX3_RPT_PKT_LEN	**If the RPT_OWN_RX_PACKET_LEN bit in WHCR is set, host driver can set this field to decide the maximal report length for RX queue 3 during enhance mode.** If under the define of SDCTL_RX3_PACKET_LEN_64, the default value 0 is to report maximal packet number 64. Host driver can set the required length from 0 to 63. If under the define of SDCTL_RX3_PACKET_LEN_32, the default value 0 is to report maximal packet number 32. Host driver can set the required length from 0 to 31. If under the define of SDCTL_RX3_PACKET_LEN_16, the default value 0 is to report maximal packet number 16. Host driver can set the required length from 0 to 15. Setting this field with a value greater than the maximal packet number is not allowed.
21:16	RX2_RPT_PKT_LEN	**If the RPT_OWN_RX_PACKET_LEN bit in WHCR is set, host driver can set this field to decide the maximal report length for RX queue 2 during enhance mode.** If under the define of SDCTL_RX2_PACKET_LEN_64, the default value 0 is to report maximal packet number 64. Host driver can set the required length from 0 to 63. If under the define of SDCTL_RX2_PACKET_LEN_32, the default value 0 is to report maximal packet number 32. Host driver can set the required length from 0 to 31. If under the define of SDCTL_RX2_PACKET_LEN_16, the default value 0 is to report maximal packet number 16. Host driver can set the required length from 0 to 15. Setting this field with a value greater than the maximal packet number is not allowed.
13:8	RX1_RPT_PKT_LEN	**If the RPT_OWN_RX_PACKET_LEN bit in WHCR is set, host driver can set this field to decide the maximal report length for RX queue 1 during enhance mode.** If under the define of SDCTL_RXD_PACKET_LEN_64, the default value 0 is to report maximal packet number 64. Host driver can set the required length from 0 to 63. If under the define of SDCTL_RXD_PACKET_LEN_32, the default value 0 is to report maximal packet number 32. Host driver can set the required length from 0 to 31. If under the define of SDCTL_RXD_PACKET_LEN_16, the default value 0 is to report maximal packet number 16. Host driver can set the required length from 0 to 15. Setting this field with a value greater than the maximal packet number is not allowed.
5:0	RX0_RPT_PKT_LEN	**If the RPT_OWN_RX_PACKET_LEN bit in WHCR is set, host driver can set this field to decide the maximal report**

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Bit(s)	Name	Description
		length for RX queue 0 during enhance mode. If under the define of SDCTL_RXE_PACKET_LEN_64, the default value 0 is to report maximal packet number 64. Host driver can set the required length from 0 to 63. If under the define of SDCTL_RXE_PACKET_LEN_32, the default value 0 is to report maximal packet number 32. Host driver can set the required length from 0 to 31. If under the define of SDCTL_RXE_PACKET_LEN_16, the default value 0 is to report maximal packet number 16. Host driver can set the required length from 0 to 15. Setting this field with a value greater than the maximal packet number is not allowed.

000000D8 WSR **WLAN Snapshot Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SNAPSHOT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SNAPSHOT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SNAPSHOT	**A 32-bits register which could copy the content of the AHB clock domain register that is being read.** For registers with RC property, if there is CRC Error during the read access, host driver shall keep reading this snapshot register until there is no CRC error to avoid information loss. Software should not read other registers first, it is an atomic operation. For registers without RC property, if there is CRC Error during the read access, host could just read the original register again. Value in this register is undefined if previous read is reading register without RC property.

000000F8 VSCR **Version Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HW_VERSION															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_VERSION															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	HW_VERSION	**Indicates the hardware version**

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Bit(s)	Name	Description

000000FC WSDIOAICR **Common SDIO Asynchronous Interrupt Control Register** **00000004**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SYNC_INT_CYCLE_NUM			
Type													RW			
Reset													0	1	0	0

Bit(s)	Name	Description
3:0	SYNC_INT_CYCLE_NUM	**Controls the synchronous interrupt cycles before the asynchronous interrupt period (4 cycles in default defined in SDIO spec. 3.0). This is for some specific hosts that could stop the SD clock before the defined asynchronous interrupt period.**

00000100 CLKIOCR_T28LP **Clock Pad Macro IO Control Register** **000A0422**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CLK_RDSEL										CLK_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						CLK_E8E4E2					CLK_SMT	CLK_PUPD	CLK_R1	CLK_R0	CLK_IES	CLK_SR
Type						RW					RW	RW	RW	RW	RW	RW
Reset						1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	CLK_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	CLK_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
10:8	CLK_E8E4E2	**TX Driving Strength Control.**

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Bit(s)	Name	Description
5	CLK_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	CLK_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor CLK pad default no pull
3	CLK_R1	**Select 50K resistor (0: not selected, 1: selected)**
2	CLK_R0	**Select 10K resistor (0: not selected, 1: selected)**
1	CLK_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0 According to IOCUP spec. Power down mode, IES=0 must Quiescent mode, IES=0 suggested
0	CLK_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

00000104 CMDIOCR_T28LP Command Pad Macro IO Control Register 000A0422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			CMD_RDSEL										CMD_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_CMD_SAMPLE		CMD_E8E4E2					CMD_SMT	CMD_PUPD	CMD_R1	CMD_R0	CMD_IES	CMD_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	CMD_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	CMD_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_CMD_SAMPLE	**Selects clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input command 1: Use negative SD clock edge to latch input command
10:8	CMD_E8E4E2	**TX Driving Strength Control.**
5	CMD_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.**

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Bit(s)	Name	Description
		SMT=1, Schmitt Trigger enable
4	CMD_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor CMD pad default no pull
3	CMD_R1	**Selects 50K resistor (0: not selected, 1: selected)**
2	CMD_R0	**Selects 10K resistor (0: not selected, 1: selected)**
1	CMD_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	CMD_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

00000108 DAT0IOCR_T28LP Data 0 Pad Macro IO Control Register 000A0422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA0_RDSEL										DATA0_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_DATA0_SAMPLE		DATA0_E8E4E2					DATA0_SMT	DATA0_PUPD	DATA0_R1	DATA0_R0	DATA0_IES	DATA0_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DATA0_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA0_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted(low pulse width adjustment)
12	REG_DATA0_SAMPLE	**Selects clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 0 1: Use negative SD clock edge to latch input data 0
10:8	DATA0_E8E4E2	**TX Driving Strength Control.**
5	DATA0_SMT	**RX input buffer Schmitt trigger hysteresis control enabled. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA0_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 0 pad default no pull

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Bit(s)	Name	Description
3	DATA0_R1	**Selects 50K resistor (0: not selected, 1: selected)**
2	DATA0_R0	**Selects 10K resistor (0: not selected, 1: selected)**
1	DATA0_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA0_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

0000010C DAT1IOCR_T28LP Data 1 Pad Macro IO Control Register 000A0422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA1_RDSEL										DATA1_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_DATA1_SAMPLE		DATA1_E8E4E2					DATA1_SMT	DATA1_PUPD	DATA1_R1	DATA1_R0	DATA1_IES	DATA1_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DATA1_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA1_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_DATA1_SAMPLE	**Selects clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 1 1: Use negative SD clock edge to latch input data 1
10:8	DATA1_E8E4E2	**TX Driving Strength Control.**
5	DATA1_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA1_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 1 pad default no pull
3	DATA1_R1	**Selects 50K resistor (0: not selected, 1: selected)**
2	DATA1_R0	**Selects 10K resistor (0: not selected, 1: selected)**
1	DATA1_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA1_SR	**Output Slew Rate Control. High asserted.**

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Bit(s)	Name	Description
		SR=1, slower slew. SR=0, no slew rate controlled.

00000110 DAT2IOCR_T28LP Data 2 Pad Macro IO Control Register 000A0422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA2_RDSEL										DATA2_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_DATA2_SAMPLE		DATA2_E8E4E2					DATA2_SMT	DATA2_PUPD	DATA2_R1	DATA2_R0	DATA2_IES	DATA2_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DATA2_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA2_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_DATA2_SAMPLE	**Selects clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 2 1: Use negative SD clock edge to latch input data 2
10:8	DATA2_E8E4E2	**TX Driving Strength Control.**
5	DATA2_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA2_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 2 pad default no pull
3	DATA2_R1	**Selects 50K resistor (0: not selected, 1: selected)**
2	DATA2_R0	**Selects 10K resistor (0: not selected, 1: selected)**
1	DATA2_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA2_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

00000114 DAT3IOCR_T28LP Data 3 Pad Macro IO Control Register 000A042A

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DATA3_RDSEL										DATA3_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				REG_DATA3_SAMPLE		DATA3_E8E4E2					DATA3_SMT	DATA3_PUPD	DATA3_R1	DATA3_R0	DATA3_IES	DATA3_SR
Type				RW		RW					RW	RW	RW	RW	RW	RW
Reset				0		1	0	0			1	0	1	0	1	0

Bit(s)	Name	Description
29:24	DATA3_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)
19:16	DATA3_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
12	REG_DATA3_SAMPLE	**Selects clock edge to latch input bus signal.** 0: Use positive SD clock edge to latch input data 3 1: Use negative SD clock edge to latch input data 3
10:8	DATA3_E8E4E2	**TX Driving Strength Control.**
5	DATA3_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DATA3_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor DATA 3 pad default would pull up with 50K resistor. (for card detection) After host driver writes cd_disable to CCCR register, data 3 pad would become no pull.
3	DATA3_R1	**Selects 50K resistor (0: not selected, 1: selected)**
2	DATA3_R0	**Selects 10K resistor (0: not selected, 1: selected)**
1	DATA3_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DATA3_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

00000118 CLKDLYCR Clock Pad Macro Delay Chain Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam																

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e																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**REG_CK_DLY_EN**			**CLK_DLY_SEL**				
Type									RW			RW				
Reset									0			0	0	0	0	0

Bit(s)	Name	Description
7	REG_CK_DLY_EN	**Enablea input clock through delay chain.** 0: Input clock does not pass through delay chain. 1: Input clock pass through delay chain.
4:0	CLK_DLY_SEL	**CLK Pad Input Delay Control** This register is used to add delay to CLK phase. Total 32 stages

0000011C **CMDDLYCR** **Command Pad Macro Delay Chain Control Register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**REG_CMD_O_DLY_EN**	**REG_CMD_OE_DLY_EN**		**CMD_O_DLY**				
Type									RW	RW		RW				
Reset									0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REG_CMD_NEG_I_DLY_EN**			**CMD_NEG_I_DLY**					**REG_CMD_POS_I_DLY_EN**			**CMD_POS_I_DLY**				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
23	REG_CMD_O_DLY_EN	**Enables output response through delay chain. (to I of IOCUP)** 0: Output response does not pass through delay chain. 1: Output response passes through delay chain.
22	REG_CMD_OE_DLY_EN	**Enables response output enable through delay chain. (to E of IOCUP)**

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Bit(s)	Name	Description
		0: Response output enable does not pass through delay chain. 1: Response output enable pass through delay chain.
20:16	CMD_O_DLY	**CMD Pad Output Delay Control** This register is used to add delay to output response phase. Total 32 stages
15	REG_CMD_NEG_I_DLY_EN	**Enables input command through delay chain to be latched with negative clock edge.** 0: Input command does not pass through delay chain. 1: Input command passes through delay chain.
12:8	CMD_NEG_I_DLY	**CMD Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input command phase. Total 32 stages
7	REG_CMD_POS_I_DLY_EN	**Enables input command through delay chain to be latched with positive clock edge.** 0: Input command does not pass through delay chain. 1: Input command passes through delay chain.
4:0	CMD_POS_I_DLY	**CMD Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input command phase. Total 32 stages

00000120 ODATDLYCR SDIO Output Data Delay Chain Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_DAT3_O_DLY_EN	REG_DAT3_OE_DLY_EN		DAT3_O_DLY					REG_DAT2_O_DLY_EN	REG_DAT2_OE_DLY_EN		DAT2_O_DLY				
Type	RW	RW		RW					RW	RW		RW				
Reset	0	0		0	0	0	0	0	0	0		0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_DAT1_O_DLY_EN	REG_DAT1_OE_DLY_EN		DAT1_O_DLY					REG_DAT0_O_DLY_EN	REG_DAT0_OE_DLY_EN		DAT0_O_DLY				
Type	RW	RW		RW					RW	RW		RW				
Reset	0	0		0	0	0	0	0	0	0		0	0	0	0	0

Bit(s)	Name	Description
31	REG_DAT3_O_DLY_EN	**Enables output data 3 through delay chain. (to I of IOCUP)** 0: Output data 3 does not pass through delay chain. 1: Output data 3 pass through delay chain.
30	REG_DAT3_OE_DLY_EN	**Enables data 3 output enable through delay chain. (to E of IOCUP)** 0: Data 3 output enable does not pass through delay chain. 1: Data 3 output enable pass through delay chain.
28:24	DAT3_O_DLY	**DATA 3 Pad Output Delay Control** This register is used to add delay to output response phase.

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Bit(s)	Name	Description
		Total 32 stages
23	REG_DAT2_O_DLY_EN	**Enables output data 2 through delay chain. (to I of IOCUP)** 0: Output data 2 does not pass through delay chain. 1: Output data 2 pass through delay chain.
22	REG_DAT2_OE_DLY_EN	**Enables data 2 output enable through delay chain. (to E of IOCUP)** 0: Data 2 output enable does not pass through delay chain. 1: Data 2 output enable pass through delay chain.
20:16	DAT2_O_DLY	**DATA 2 Pad Output Delay Control** This register is used to add delay to output response phase. Total 32 stages
15	REG_DAT1_O_DLY_EN	**Enables output data 1 through delay chain. (to I of IOCUP)** 0: Output data 1 does not pass through delay chain. 1: Output data 1 pass through delay chain.
14	REG_DAT1_OE_DLY_EN	**Enables data 1 output enable through delay chain. (to E of IOCUP)** 0: Data 1 output enable does not pass through delay chain. 1: Data 1 output enable pass through delay chain.
12:8	DAT1_O_DLY	**DATA 1 Pad Output Delay Control** This register is used to add delay to output response phase. Total 32 stages
7	REG_DAT0_O_DLY_EN	**Enables output data 0 through delay chain. (to I of IOCUP)** 0: Output data 0 does not pass through delay chain. 1: Output data 0 pass through delay chain.
6	REG_DAT0_OE_DLY_EN	**Enables data 0 output enable through delay chain. (to E of IOCUP)** 0: Data 0 output enable does not pass through delay chain. 1: Data 0 output enable pass through delay chain.
4:0	DAT0_O_DLY	**DATA 0 Pad Output Delay Control** This register is used to add delay to output response phase. Total 32 stages

00000124 IDATDLYCR1 SDIO Input Data Delay Chain Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REG_DAT3_POS_I_DLY_EN			DAT3_POS_I_DLY					REG_DAT2_POS_I_DLY_EN			DAT2_POS_I_DLY				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REG_DAT1_POS_I_DLY_EN			DAT1_POS_I_DLY					REG_DAT0_POS_I_DLY_EN			DAT0_POS_I_DLY				
Type	RW			RW					RW			RW				

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Reset	0			0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	REG_DAT3_POS_I_DLY_EN	**Enables input data 3 through delay chain to be latched with positive clock edge.** 0: Input data 3 does not pass through delay chain. 1: Input data 3 pass through delay chain.
28:24	DAT3_POS_I_DLY	**DATA 3 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 3 phase. Total 32 stages
23	REG_DAT2_POS_I_DLY_EN	**Enables input data 2 through delay chain to be latched with positive clock edge.** 0: Input data 2 does not pass through delay chain. 1: Input data 2 pass through delay chain.
20:16	DAT2_POS_I_DLY	**DATA 2 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 2 phase. Total 32 stages
15	REG_DAT1_POS_I_DLY_EN	**Enables input data 1 through delay chain to be latched with positive clock edge.** 0: Input data 1 does not pass through delay chain. 1: Input data 1 pass through delay chain.
12:8	DAT1_POS_I_DLY	**DATA 1 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 1 phase. Total 32 stages
7	REG_DAT0_POS_I_DLY_EN	**Enables input data 0 through delay chain to be latched with positive clock edge.** 0: Input data 0 does not pass through delay chain. 1: Input data 0 pass through delay chain.
4:0	DAT0_POS_I_DLY	**DATA 0 Pad Input Delay Control for data latch with positive clock edge.** This register is used to add delay to input data 0 phase. Total 32 stages

00000128 IDATDLYCR2 SDIO Input Data Delay Chain Control Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**REG_DAT3_NEG_I_DLY_EN**			**DAT3_NEG_I_DLY**					**REG_DAT2_NEG_I_DLY_EN**			**DAT2_NEG_I_DLY**				
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**REG_DAT1_NEG_I_DLY**			**DAT1_NEG_I_DLY**					**REG_DAT0_NEG_I_DL**			**DAT0_NEG_I_DLY**				

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	_EN								Y_EN							
Type	RW			RW					RW			RW				
Reset	0			0	0	0	0	0	0			0	0	0	0	0

Bit(s)	Name	Description
31	REG_DAT3_NEG_I_DLY_EN	**Enables input data 3 through delay chain to be latched with negative clock edge.** 0: Input data 3 does not pass through delay chain. 1: Input data 3 pass through delay chain.
28:24	DAT3_NEG_I_DLY	**DATA 3 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 3 phase. Total 32 stages
23	REG_DAT2_NEG_I_DLY_EN	**Enables input data 2 through delay chain to be latched with negative clock edge.** 0: Input data 2 does not pass through delay chain. 1: Input data 2 pass through delay chain.
20:16	DAT2_NEG_I_DLY	**DATA 2 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 2 phase. Total 32 stages
15	REG_DAT1_NEG_I_DLY_EN	**Enables input data 1 through delay chain to be latched with negative clock edge.** 0: Input data 1 does not pass through delay chain. 1: Input data 1 pass through delay chain.
12:8	DAT1_NEG_I_DLY	**DATA 1 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 1 phase. Total 32 stages
7	REG_DAT0_NEG_I_DLY_EN	**Enables input data 0 through delay chain to be latched with negative clock edge.** 0: Input data 0 does not pass through delay chain. 1: Input data 0 pass through delay chain.
4:0	DAT0_NEG_I_DLY	**DATA 0 Pad Input Delay Control for data latch with negative clock edge.** This register is used to add delay to input data 0 phase. Total 32 stages

0000012C **ILCHCR** **SDIO Input Data Latch Time Control Register** **00011111**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															**REG_CMD_LATCH_SEL**	
Type															RW	
Reset															0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**REG_DAT3_LATCH_SEL**				**REG_DAT2_LATCH_SEL**				**REG_DAT1_LATCH_SEL**				**REG_DAT0__LATCH_SEL**	
Type			RW				RW				RW				RW	
Reset			0	1			0	1			0	1			0	1

Bit(s)	Name	Description
17:16	REG_CMD_LATCH_SEL	**Controls the input command latch timing depending on SDIO output enable signal to avoid latching device output**

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Bit(s)	Name	Description
		data as host transfers data in UHS104 mode. 2'b00: latch input command after 1T of output enable asserted 2'b01: latch input command after 2T of output enable asserted 2'b10: latch input command after 3T of output enable asserted 2'b11: latch input command after 4T of output enable asserted
13:12	REG_DAT3_LATCH_SEL	**Controls the input data 3 latch timing depending on SDIO output enable signal to avoid latching device output data as host transfers data in UHS104 mode.** 2'b00: latch input data 3 after 1T of output enable asserted 2'b01: latch input data 3 after 2T of output enable asserted 2'b10: latch input data 3 after 3T of output enable asserted 2'b11: latch input data 3 after 4T of output enable asserted
9:8	REG_DAT2_LATCH_SEL	**Controls the input data 2 latch timing depending on SDIO output enable signal to avoid latching device output data as host transfers data in UHS104 mode.** 2'b00: latch input data 2 after 1T of output enable asserted 2'b01: latch input data 2 after 2T of output enable asserted 2'b10: latch input data 2 after 3T of output enable asserted 2'b11: latch input data 2 after 4T of output enable asserted
5:4	REG_DAT1_LATCH_SEL	**Controls the input data 1 latch timing depending on SDIO output enable signal to avoid latching device output data as host transfers data in UHS104 mode.** 2'b00: latch input data 1 after 1T of output enable asserted 2'b01: latch input data 1 after 2T of output enable asserted 2'b10: latch input data 1 after 3T of output enable asserted 2'b11: latch input data 1 after 4T of output enable asserted
1:0	REG_DAT0__LATCH_SEL	**Controls the input data 0 latch timing depending on SDIO output enable signal to avoid latching device output data as host transfers data in UHS104 mode.** 2'b00: latch input data 0 after 1T of output enable asserted 2'b01: latch input data 0 after 2T of output enable asserted 2'b10: latch input data 0 after 3T of output enable asserted 2'b11: latch input data 0 after 4T of output enable asserted

00000130 WTQCR0 WLAN TXQ Count Register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ1_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ0_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ1_CNT	**This field indicates the released count of TXQ1 during two WTQCR0 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ0_CNT	**This field indicates the released count of TXQ0 during two WTQCR0 read accesses. The unit can be defined by the**

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Bit(s)	Name	Description
		driver. This field is cleared by read operation. Write does nothing.

00000134 WTQCR1 WLAN TXQ Count Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ3_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ2_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ3_CNT	**This field indicates the released count of TXQ3 during two WTQCR1 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ2_CNT	**This field indicates the released count of TXQ2 during two WTQCR1 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

00000138 WTQCR2 WLAN TXQ Count Register 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ5_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ4_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ5_CNT	**This field indicates the released count of TXQ5 during two WTQCR2 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ4_CNT	**This field indicates the released count of TXQ4 during two WTQCR2 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

0000013C WTQCR3 WLAN TXQ Count Register 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	TXQ7_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ6_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ7_CNT	**This field indicates the released count of TXQ7 during two WTQCR3 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ6_CNT	**This field indicates the released count of TXQ6 during two WTQCR3 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

00000140 WTQCR4 WLAN TXQ Count Register 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ9_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ8_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ9_CNT	**This field indicates the released count of TXQ9 during two WTQCR4 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ8_CNT	**This field indicates the released count of TXQ8 during two WTQCR4 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

00000144 WTQCR5 WLAN TXQ Count Register 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TXQ11_CNT															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXQ10_CNT															

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Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ11_CNT	**This field indicates the released count of TXQ11 during two WTQCR5 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ10_CNT	**This field indicates the released count of TXQ10 during two WTQCR5 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

00000148 WTQCR6 WLAN TXQ Count Register 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TXQ13_CNT**															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TXQ12_CNT**															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ13_CNT	**This field indicates the released count of TXQ13 during two WTQCR6 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.
15:0	TXQ12_CNT	**This field indicates the released count of TXQ12 during two WTQCR6 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

0000014C WTQCR7 WLAN TXQ Count Register 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**TXQ15_CNT**															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**TXQ14_CNT**															
Type	RC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TXQ15_CNT	**This field indicates the released count of TXQ15 during two WTQCR7 read accesses. The unit can be defined by the driver.**

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Bit(s)	Name	Description
15:0	TXQ14_CNT	This field is cleared by read operation. Write does nothing. **This field indicates the released count of TXQ14 during two WTQCR7 read accesses. The unit can be defined by the driver.** This field is cleared by read operation. Write does nothing.

00000154 SWPCDBGR WLAN PC Value debug register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CPU_PC_VALUE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CPU_PC_VALUE															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	CPU_PC_VALUE	**This field indicates the command ran by the CPU and is read out by host software to debug the slave CPU** This register is read only and can only be read out by one command 53, because the whole 32bits makes a valid CPU status and its content may be updated at every AHB clock. When reading this register SDIO AHB clock must exist and it does not need driver own right.

00000158 DSIOCR DS Pad Macro IO Control Register 000A0422

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			DS_RDSEL										DS_TDSEL			
Type			RW										RW			
Reset			0	0	0	0	0	0					1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						DS_E8E4E2					DS_SMT	DS_PUPD	DS_R1	DS_R0	DS_IES	DS_SR
Type						RW					RW	RW	RW	RW	RW	RW
Reset						1	0	0			1	0	0	0	1	0

Bit(s)	Name	Description
29:24	DS_RDSEL	**RX duty select** RDSEL[1:0]: Input buffer duty high when asserted (high pulse width adjustment) RDSEL[3:2]: Input buffer duty low when asserted (low pulse width adjustment) RDSEL[5:4]: Level shifter duty high when asserted (high pulse width adjustment) RDSEL[7:6]: Level shifter duty low when asserted (low pulse width adjustment)

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Bit(s)	Name	Description
19:16	DS_TDSEL	**TX duty select** TDSEL[1:0]: Output level shifter duty high when asserted (high pulse width adjustment) TDSEL[3:2]: Output level shifter duty low when asserted (low pulse width adjustment)
10:8	DS_E8E4E2	**TX Driving Strength Control.**
5	DS_SMT	**RX input buffer Schmitt trigger hysteresis control enable. High asserted.** SMT=1, Schmitt Trigger enable
4	DS_PUPD	**Pull-up/pull-down selection.** 0: Pull-up resistor 1: Pull-down resistor CLK pad default no pull
3	DS_R1	**Selects 50K resistor (0: not selected, 1: selected)**
2	DS_R0	**Selects 10K resistor (0: not selected, 1: selected)**
1	DS_IES	**RX input buffer enable. High asserted.** Datapath: from IO to O. IES=0, O=0
0	DS_SR	**Output Slew Rate Control. High asserted.** SR=1, slower slew. SR=0, no slew rate controlled.

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17. Serial Flash Controller

17.1. Introduction

The serial flash controller (SFC) supports convenient high-speed serial NOR flash access and flexible macro command sequence read/write.

17.2. Abbreviations

Table 17.2-1 lists the abbreviations used in this chapter.

Table 17.2-1. Abbreviations

Abbreviation	Definition
GPRAM	General purpose SRAM (stores command and data bits of macro mode for flash device)
CS	Chip select of flash device
CK	Clock of flash device
SIO[3:0]	Bidirectional data input and output of flash device. SIO[3:0] = {SHOLD, SWP, SOUT, SIN}
SF	Serial flash device
SFC	Serial flash controller
Int SF	Internal packaged flash device
Ext SF	External flash device (not packaged in the SoC)
SF_DO[3:0]	Flash Controller data output to macro
Data Macro	Macro circuit with data delay chains for both in and out directions and pad cell
Clock Delay Macro	Macro circuit with clock delay chain
sf_clk	Serial flash controller clock
hclk	AHB clock
srreq	AHB slave read request
srack	AHB slave read acknowledgement signal
sf_req	Serial flash request
sf_cs	Serial flash chip select
sck	Serial flash clock
flash_dle	Indicates serial flash buffer is full
sfbuf_count	Serial flash buffer counter

17.3. Features

- High-speed serial NOR flash access
- Flexible macro serial NOR flash command sequence read and write
- Supports 1.8V and 3V serial flash memory
- Supports 26, 62.4, 78, 104 and 124.8MHz for serial flash device

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- Supports serial flash SPI-QUAD I/O and QPI mode
- Supports serial flash memory with 3-byte and 4-byte addresses

17.4. Block diagram

Figure 17.4-1. Serial flash controller block diagram

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Figure 17.4-2. Serial flash device connection between macro and controller

17.5. Direct read

Direct read mode provides a convenient way to read data programmed in SF for the Cortex-M4 and peripherals on AHB. First, the master sends an AHB read to SFC to activate Direct Read Engine to generate an SF command or address according to register settings or bus signals. After sending an SF command or address to the device, SFC latches SF read data and puts them on AHB data bus for the master. In short, direct read mode converts an AHB read to an SF read command and returns SF contents through AHB. If other SF commands are required, it should be done using macro read and write mode.

17.6. Macro read and write

Macro read and write is designed for other SF operations, including read ID, program, erase, and more. Users should write SF command (including opcode, address and data) to GPRAM in software. Once macro read/write engine receives a trigger, it reads all user-defined SF commands in GPRAM and sends them to SF. The results of SF command execution are latched and written to GPRAM for the user. SFC registers and macro read/write mode are accessed through APB exclusively for Cortex-M4, as shown in Figure 17.4-1. This means SF contents are read-only to peripherals.

17.7. Connection between internal SF and external SF

SFC supports two types of SF connections, as shown in Figure 17.4-2. The SF control signals can be configured in internal or external serial flash. Users can place their boot ROM codes in the external SF to eliminate programming effort.

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17.8. Programming guide

17.8.1. Read back register after value change

Due to the bridge latency when setting up APB registers (seeFigure 17.4-1), registers affecting AHB, such as SF_DIRECT_CTL may be unstable if AHB is accessed immediately. Therefore, it's suggested that after changing AHB related registers, such as SF_DIRECT_CTL, the registers should be read back again before accessing AHB.

17.8.1.1. Serial flash command sequence control example

Address	Register name	R/W		Value	Loop		Flash command
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA		W	0x00000006			WE (Write Enable)
SF + 004h	SF_MAC_OUTL		W	0x00000001			
SF + 008h	SF_MAC_INL		W	0x00000000			
SF + 000h	SF_MAC_CTL		W	0x0000000C			
SF + 000h	SF_MAC_CTL	R		[1] = 1, [0] = 0	Loop		
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA		W	0x452301D8			BE (Block Erase)
SF + 004h	SF_MAC_OUTL		W	0x00000004			
SF + 008h	SF_MAC_INL		W	0x00000000			
SF + 000h	SF_MAC_CTL		W	0x0000000C			
SF + 000h	SF_MAC_CTL	R		[1] = 1, [0] = 0	Loop		
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA		W	0x00000005			RDSR (Read Status Register)
SF + 004h	SF_MAC_OUTL		W	0x00000001			
SF + 008h	SF_MAC_INL		W	0x00000001			
SF + 000h	SF_MAC_CTL		W	0x0000000C		Loop	
SF + 000h	SF_MAC_CTL	R		[1] = 1, [0] = 0	Loop		
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA	R		[8] = 0 (flash WIP)			
SF + 800h	SF_GPRAM_DATA		W	0x00000006			WE (Write Enable)
SF + 004h	SF_MAC_OUTL		W	0x00000001			
SF + 008h	SF_MAC_INL		W	0x00000000			
SF + 000h	SF_MAC_CTL		W	0x0000000C			
SF + 000h	SF_MAC_CTL	R		[1] = 1, [0] = 0	Loop		
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA		W	0x45230102			PP (Page
SF + 804h	SF_GPRAM_DATA		W	0x78563412			

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Address	Register name	R/W		Value	Loop		Flash command
SF + 808h	SF_GPRAM_DATA		W	0xddccbbaa			Program)
SF + 004h	SF_MAC_OUTL		W	0x0000000C			
SF + 008h	SF_MAC_INL		W	0x00000000			
SF + 000h	SF_MAC_CTL		W	0x0000000C			
SF + 000h	SF_MAC_CTL	R		[1] = 1, [0] = 0	Loop		
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA		W	0x00000005			RDSR (Read Status Register)
SF + 004h	SF_MAC_OUTL		W	0x00000001			
SF + 008h	SF_MAC_INL		W	0x00000001			
SF + 000h	SF_MAC_CTL		W	0x0000000C		Loop	
SF + 000h	SF_MAC_CTL	R		[1] = 1, [0] = 0	Loop		
SF + 000h	SF_MAC_CTL		W	0x00000008			
SF + 800h	SF_GPRAM_DATA	R		[8] = 0 (flash WIP)			

17.9. Register mapping

Module name: sf_top Base address: (+a0040000h)

Address	Name	Width (bits)	Register Function
A0040000	SF_MAC_CTL	32	Serial flash macro read/write control
A0040004	SF_DIRECT_CTL	32	Serial flash direct read setting
A0040008	SF_MISC_CTL1	32	Serial flash clock MISC controller setting 1
A004000C	SF_MISC_CTL2	32	Serial flash MISC control setting 2
A0040010	SF_MAC_OUTL	32	Serial flash macro output data length
A0040014	SF_MAC_INL	32	Serial flash macro input data length
A0040080	SF_PERF_MON1	32	Serial flash performance monitor 1
A0040084	SF_PERF_MON2	32	Serial flash performance monitor 2
A0040088	SF_PERF_MON3	32	Serial flash performance monitor 3
A004008C	SF_PERF_MON4	32	Serial flash performance monitor 4
A0040090	SF_PERF_MON5	32	Serial flash performance monitor 5
A0040094	SF_PERF_MON6	32	Serial flash performance monitor 6
A0040098	SF_PERF_MON7	32	Serial flash performance monitor 7
A004009C	SF_PERF_MON8	32	Serial flash performance monitor 8
A00400A0	SF_PERF_MON9	32	Serial flash performance monitor 9
A00400A4	SF_PERF_MON10	32	Serial flash performance monitor 10
A00400A8	SF_PERF_MON11	32	Serial flash performance monitor 11
A00400AC	SF_PERF_MON12	32	Serial flash performance monitor 12
A00400B0	SF_PERF_MON13	32	Serial flash performance monitor 13

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Address	Name	Width (bits)	Register Function
A0040800~ A004089c	SF_GPRAM_BASE [n] (n=0~39)	32	Serial flash macro read/write memory data (160 bytes)

sf_top serial flash delay control setting

Address	Name	Width (bits)	Register Function
A0040020	SF_DLY_CTL1	32	Serial flash delay control setting 1
A0040024	SF_DLY_CTL2	32	Serial flash delay control setting 2
A0040028	SF_DLY_CTL3	32	Serial flash delay control setting 3
A0040030	SF_DLY_CTL4	32	Serial flash delay control setting 4
A0040034	SF_DLY_CTL5	32	Serial flash delay control setting 5
A0040038	SF_DLY_CTL6	32	Serial flash delay control setting 6

A0040000 SF_MAC_CTL Serial flash macro read/write control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RELEASE_MAC
Type																RW
Reset																1
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	ABORT_CLR	SF_ABORT	SF_ABOT_REQ_SRC				SF_IRQ_EN	SF_IRQ_ACK		MAC_MASK_OP	MAC_MASK	MAC_XIO_SEL	SF_MAC_EN	SF_TRIG	WIP_READY	WIP
Type	RW	RU	RU				RW	RW		RW	RW	RW	RW	RW	RU	RU
Reset	0	0	0	0			0	0		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
16	**RELEASE_MAC**	RELEASE_MAC	**Prevents the AHB bus from hanging. As the serial flash enters MAC mode, it will raise SF_ABORT to "high" for the MCU to interrupt the current transaction and check if the AHB bus has stopped. If Release_MAC is set to 1, SF_ABORT will not be raised to 1. In the DEBUG develop segment, set this bit to 1 when the serial flash enters macro mode, and SF_ABORT will not be raised to 1. The serial flash will continue the next operation event even though the data read are wrong.** 0 Disable 1 Enable
15	**ABORT_CLR**	ABORT_CLR	**Clears serial flash abort operation. To exit the serial flash abort, ABORT_CLR must be set to 1 to clear the SF_ABORT status and then set ABORT_CLR back to 0 to detect another serial flash abort operation.**

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Bit(s)	Mnemonic	Name	Description
			0 Disable 1 Enable
14	**SF_ABORT**	SF_ABORT	**Serial flash abort status register. SF_ABORT will be 1 if Direct Engine begins accessing the Serial Flash when Macro R/W engine is active.** 0 Not abort 1 Abort
13:12	**SF_ABORT_REQ_SRC**	SF_ABOT_REQ_SRC	**Request the source to stop the serial flash** 00 Not aborted 01 Aborted through MCU. 10 Aborted through a peripheral unit.
9	**SF_IRQ_EN**	SF_IRQ_EN	**Serial flash interrupt enable during serial flash abortion** 0 Disable 1 Enable
8	**SF_IRQ_ACK**	SF_IRQ_ACK	**Serial flash interrupt acknowledged signal** 0 Not acknowledged 1 Acknowledged
6	**MAC_MASK_OP**	MAC_MASK_OP	**Serial flash hardware DIRECT/MAC mode auto switch setting. If MAC_MASK_OP=1 then SF_TRIG=1 is triggered, hardware module will automatically switch to MAC mode until MAC mode operation is finished.** 0 Disable 1 Enable
5	**MAC_MASK**	MAC_MASK	**Serial flash software DIRECT/MAC mode switch setting. If MAC_MASK is set to 1, the hardware will switch to MAC mode manually and will not permit any DIRECT mode access until MAC_MASK=0. It is suggested to run MAC mode in internal SYSRAM code if MAC_MASK = 1 by software setting.** 0 Disable 1 Enable
4	**MAC_XIO_SEL**	MAC_XIO_SEL	**MAC mode for QPI/SPI setting** 0 SPI 1 QPI
3	**SF_MAC_EN**	SF_MAC_EN	**Switches the serial flash control to update macro. Please set up this bit before triggering the update macro. It is suggested to run MAC mode in internal SYSRAM code because DIRECT/MAC mode cannot run at the same time. Another way is to switch to hardware auto switch mode by setting up MAC_MASK_OP.** 0 Disable 1 Enable (Direct read is forbidden when SF_MAC_EN = 1)
2	**SF_TRIG**	SF_TRIG	**Serial flash write macro trigger** 0 Disable 1 Enable (Fill command sequence I/O length before SF_TRIG)
1	**WIP_READY**	WIP_READY	**WIP register status ready for access. WIP_READY exits due to asynchronous latency delay before flash responds to WIP** 0 WIP not ready for read 1 WIP ready for read (Check if WIP_READY = 1 before the next command sequence)
0	**WIP**	WIP	**Serial flash command write in process** 0 Flash update finished (Check if WIP = 0 before the next command sequence) 1 Not finished

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A0040004 SF_DIRECT_CTL Serial flash direct read setting 0B0B7710

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SF_CTRL_CMD1								SF_CTRL_CMD2							
Type	RW								RW							
Reset	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CMD1_DUMMY_CYC				CMD2_DUMMY_CYC					SF_READ_MODE			CMD2_EXT_ADDR_EN	SF_CMD2_EN	CMD1_EXT_ADDR_EN	SF_QPI_EN
Type	RW				RW					RW			RW	RW	RW	RW
Reset	0	1	1	1	0	1	1	1		0	0	1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:24	**SF_CTRL_CMD1**	SF_CTRL_CMD1	**Serial flash DIRECT read mode command 1 register setting for DUAL/QIO/QPI mode.**
23:16	**SF_CTRL_CMD2**	SF_CTRL_CMD2	**Serial flash DIRECT read mode command 2 register setting for DUAL/QIO/QPI mode**
15:12	**CMD1_DUMMY_CYC**	CMD1_DUMMY_CYC	**Serial flash read mode dummy cycles for SF_CTRL_CMD1 setting** 4'b0000 1T 4'b0001 2T 4'b 0010 3T 4'b 0011 4T 4'b 0100 5T 4'b 0101 6T 4'b 0110 7T 4'b 0111 8T 4'b 1000 9T 4'b 1001 10T 4'b 1010 11T 4'b 1011 12T 4'b 1100 13T 4'b 1101 14T 4'b 1110 15T 4'b 1111 16T
11:8	**CMD2_DUMMY_CYC**	CMD2_DUMMY_CYC	**Serial flash read mode dummy cycles for SF_CTRL_CMD2 setting** 4'b 0000 1T 4'b 0001 2T 4'b 0010 3T 4'b 0011 4T 4'b 0100 5T 4'b 0101 6T 4'b 0110 7T 4'b 0111 8T 4'b 1000 9T 4'b 1001 10T 4'b 1010 11T 4'b 1011 12T 4'b 1100 13T 4'b 1101 14T 4'b 1110 15T 4'b 1111 16T
6:4	**SF_READ_MODE**	SF_READ_MODE	**Selects serial flash read mode** 3'b000 Normal read mode

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Bit(s)	Mnemonic	Name	Description
			3'b 001 Fast read mode 3'b 010 Dual output mode 3'b 011 Dual I/O mode 3'b 111 Quad I/O mode
3	**CMD2_EXT_ADDR_EN**	CMD2_EXT_ADDR_EN	**Enabled to send 4-byte address when using SF_CTRL_CMD2** 0 Disable 1 Enable
2	**SF_CMD2_EN**	SF_CMD2_EN	**Enables SF_CTRL_CMD2 command. When SF_CMD2_EN is set to 1, the serial flash controller will use the SF_CTRL_CMD2 command to read data as accessing address exceeds 24 bits.** 0 Disable 1 Enable
1	**CMD1_EXT_ADDR_EN**	CMD1_EXT_ADDR_EN	**Enables extended address mode for SF_CTRL_CMD1.** 0 Disable 1 Enable
0	**SF_QPI_EN**	SF_QPI_EN	**Serial flash QPI enable in QIO mode. Set this bit with QIO = 1 (SF_READ_MODE = 3'b111)** 0 Disable 1 Enable

A0040008 SF_MISC_CTL1 Serial flash clock MISC controller setting 1 B2C00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SF_CS_EXT_CYC						FIFO_RD_LTC		NO_RELOAD	FIFO_MACRO_RST	CS_EXT_CYC_OPT_EN	FOUR_TAP_FIFO_EN	AHB_REQ_1TLh_EN	SF_DOUBLE_SYNC	SF_SYNC_EN	REG_ADDR_SYNC_SEL
Type	RW						RW		RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1	1			1	0	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SFIO_EN_SEL	CS_SETUP_LTC					SF_REQ_IDLE	CH3_B2S	CH2_B2S	SF_FBCLK_SEL	SMPCK_INV	OUTCK_INV		DEL_LATCH_LATENcy	
Type		RW	RW					RU	RW	RW	RW	RW	RW		RW	
Reset		0	0	0				0	0	0	0	0	0		0	0

Bit(s)	Mnemonic	Name	Description
31:28	**SF_CS_EXT_CYC**	SF_CS_EXT_CYC	**CS pin pulled from high to low extension cycles.** **Default: 12 cycles** 4'b0000 1 cycle 4'b0001 2 cycles 4'b0010 3 cycles 4'b0011 4 cycles 4'b0100 5 cycles 4'b0101 6 cycles

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Bit(s)	Mnemonic	Name	Description
			4'b0110 7 cycles 4'b0111 8 cycles 4'b1000 9 cycles 4'b1001 10 cycles 4'b1010 11 cycles 4'b1011 12 cycles 4'b1100 13 cycles 4'b1101 14 cycles
25:24	**FIFO_RD_LTC**	FIFO_RD_LTC	**4 Tap FIFO read latency**
23	**NO_RELOAD**	NO_RELOAD	**NO_RELOAD setting: RELOAD means the serial flash controller keeps the CS pin low, and the CLK pin is pending after the pre-fetch buffer is full. If the next access address continues, the previous address will then start generating CLK to access the next data without resending command/address overhead to gain better bandwidth usage.** 0 CMD/ADDR is not issued if the next access address continues right after the previous address. 1 CMD/ADDR is re-issued.
22	**FIFO_MACRO_RST**	FIFO_MACRO_RST	**Serial flash IO module reset control** 0 Disable reset 1 Enable reset
21	**CS_EXT_CYC_OPT_EN**	CS_EXT_CYC_OPT_EN	**Enables CS extension cycle optimization. In DIRECT READ mode, the CS extension cycle is added before each transaction. However, before receiving a new request, CS might have been pulled up. If CS_EXT_CYC_OPT_EN is set to 1, serial flash controller will reduce CS extension cycle time by SF_CS_EXT_CYC before the new SF access.** 0 Disable 1 Enable
20	**FOUR_TAP_FIFO_EN**	FOUR_TAP_FIFO_EN	**Enables 4 Tap FIFO** 0 Disable 1 Enable
19	**AHB_REQ_1TLh_EN**	AHB_REQ_1TLh_EN	**Enables serial flash controller to delay one clock cycle (1T) to latch AHB request** 0 No delay 1 Delay 1T to latch AHB request
18	**SF_DOUBLE_SYNC**	SF_DOUBLE_SYNC	**Enables serial flash double sync. If the frequency of serial flash is twice of BUS frequency the serial flash controller is required to operate in synchronous mode, set SF_SYNC_EN and SF_DOUBLE_SYNC to 1.** 0 Disable 1 Enable
17	**SF_SYNC_EN**	SF_SYNC_EN	**Enables serial flash synchronous mode** 0 Asynchronous mode 1 Synchronous mode
16	**REG_ADDR_SYNC_SEL**	REG_ADDR_SYNC_SEL	**SF address select** 0 Synchronous mode 1 Asynchronous mode
14	**SFIO_EN_SEL**	SFIO_EN_SEL	**Serial flash IO PAD Enable signal aligned with clock positive edge select.** 0 Disable 1 Enable
13:12	**CS_SETUP_LTC**	CS_SETUP_LTC	**Serial flash CS setup time latency. Set up CS_SETUP_LTC to increase the CS setup time. Default CS setup time for both MAC and DIRECT READ mode is 1.5 serial flash clock period.** 2'b00 Does not increase serial flash CS setup time

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Bit(s)	Mnemonic	Name	Description
			2'b01 Increase 1T for CS setup time 2'b10 Increase 2T for CS setup time 2'b11 Increase 3T for CS setup time
8	**SF_REQ_IDLE**	SF_REQ_IDLE	**Serial flash controller processing transaction status register** 0 Transaction is in progress. 1 Idle
7	**CH3_B2S**	CH3_B2S	**Channel 3 of serial flash access switch to single data access mode for priority arbitration behavior setting. SPI can access the serial flash through channel 3. If CH3_B2S = 1, the arbitration will switch to another agent (Cortex-M4) access after every CH3 single access.** 0 Disable 1 Enable
6	**CH2_B2S**	CH2_B2S	**Channel 2 of serial flash access switch to single data access mode for priority arbitration behavior setting. DMA can access the serial flash through channel 2. If CH2_B2S = 1, the arbitration will switch to another agent (Cortex-M4) access after every CH2 single access.** 0 Disable 1 Enable
5	**SF_FBCLK_SEL**	SF_FBCLK_SEL	**Serial flash feedback clock selection setting** 0 Use non-feedback clock 1 Use feedback clock for serial flash
4	**SMPCK_INV**	SMPCK_INV	**Sample clock inverse for read data input** 0 No inverse 1 Inverse
3	**OUTCK_INV**	OUTCK_INV	**Output clock inverse bit** 0 No inverse 1 Inverse
1:0	**DEL_LATCH_LATENcy**	DEL_LATCH_LATENcy	**Selects serial flash latch delay latency** 2'b00 Not delay 2'b01 Delay 1T to latch serial flash data 2'b10 Delay 2T to latch serial flash data 2'b11 Delay 3T to latch serial flash data

A004000C SF_MISC_CTL2 Serial flash MISC control setting 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**WRAP_ACC_EN**
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
0	**WRAP_ACC_EN**	WRAP_ACC_EN	**Enables serial flash wrap access. If WRAP_ACC_EN is set to 1, the controller will access the serial flash from the request address first (if not aligned with pre-fetch size boundary) and fill the pre-fetch buffer.** **Note: set NO_RELOAD to 1 when WRAP_ACC_EN = 1** 0 Disable 1 Enable

A0040010 SF_MAC_OUTL Serial flash macro output data length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MAC_OUT_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MAC_OUT_LENGTH**	MAC_OUT_LENGTH	**Serial flash write data length, 1 ~ 160 bytes**

A0040014 SF_MAC_INL Serial flash macro input data length 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MAC_IN_LENGTH							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**MAC_IN_LENGTH**	MAC_IN_LENGTH	**Serial flash read data length, 1 ~ 160 bytes**

A0040080 SF_PERF_MON1 Serial flash performance monitor 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name															**PERF_MON_CLR**	**PERF_MON_EN**
Type															RW	RW
Reset															0	0

Bit(s)	Mnemonic	Name	Description
1	**PERF_MON_CLR**	PERF_MON_CLR	**Clears the performance monitor. If PERF_MON_CLR is set to 1, all data in the performance monitor will be set to 0. Set PERF_MON_CLR to 0 to clear the information in the performance monitor before re-starting the performance monitor.** 0 Disable 1 Enable
0	**PERF_MON_EN**	PERF_MON_EN	**Performance monitor enable bit.** 0 Disable 1 Enable

A0040084 SF_PERF_MON2 Serial flash performance monitor 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**PERF_MON_CYC**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**PERF_MON_CYC**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**PERf_MON_CYC**	PERf_MON_CYC	**Cycle counts after enabling performance monitor**

A0040088 SF_PERF_MON3 Serial flash performance monitor 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SF_BUSY_CYC**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SF_BUSY_CYC**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
31:0	**SF_BUSY_CYC**	SF_BUSY_CYC	**The number of serial Flash Busy Cycles after enabling the performance monitor. SF_BUSY_CYC is the sum of MAC mode and 3 AHB channels busy cycles.**

A004008C SF_PERF_MON4 Serial flash performance monitor 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SF_MAC_CYC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SF_MAC_CYC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SF_MAC_CYC**	SF_MAC_CYC	**Serial Flash MAC Mode Cycles after enabling the performance monitor**

A0040090 SF_PERF_MON5 Serial flash performance monitor 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH1_BUSY_CYC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH1_BUSY_CYC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH1_BUSY_CYC**	CH1_BUSY_CYC	**The number of serial Flash channel 1 busy cycles (access serial flash device) counts after enabling the performance monitor**

A0040094 SF_PERF_MON6 Serial flash performance monitor 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH1_REQ_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH1_REQ_COUNT															

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Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH1_REQ_COUNT**	CH1_REQ_COUNT	**The number of AHB bus requests serial flash controller channel 1 receives after enabling the performance monitor**

A0040098 SF_PERF_MON7 Serial flash performance monitor 7 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CH1_DATA_BYTE_COUNT**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH1_DATA_BYTE_COUNT**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH1_DATA_BYTE_COUNT**	CH1_DATA_BYTE_COUNT	**The number of data bytes AHB bus transferred through serial flash controller channel 1 after enabling the performance monitor**

A004009C SF_PERF_MON8 Serial flash performance monitor 8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CH2_BUSY_CYC**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH2_BUSY_CYC**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH2_BUSY_CYC**	CH2_BUSY_CYC	**The number of serial Flash channel 2 busy cycles (access serial flash device) after enabling the performance monitor**

A00400A0 SF_PERF_MON9 Serial flash performance monitor 9 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CH2_REQ_COUNT**															
Type	RU															
Rese	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH2_REQ_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH2_REQ_COUNT**	CH2_REQ_COUNT	**The number of AHB bus requests serial flash controller channel 2 received after enabling the performance monitor**

A00400A4 SF_PERF_MON10 Serial flash performance monitor 10 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH2_DATA_BYTE_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH2_DATA_BYTE_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH2_DATA_BYTE_COUNT**	CH2_DATA_BYTE_COUNT	**The number of data bytes AHB bus transferred through serial flash controller channel 2 after enabling the performance monitor**

A00400A8 SF_PERF_MON11 Serial flash performance monitor 11 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH3_BUSY_CYC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH3_BUSY_CYC															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH3_BUSY_CYC**	CH3_BUSY_CYC	**The number of serial Flash channel busy cycles (access serial flash device) after enabling the performance monitor**

A00400AC SF_PERF_MON12 Serial flash performance monitor 12 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	CH3_REQ_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH3_REQ_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH3_REQ_COUNT**	CH3_REQ_COUNT	**The number of AHB bus requests serial flash controller channel 3 received after enabling the performance monitor**

A00400B0 SF_PERF_MON13 Serial flash performance monitor 13 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH3_DATA_BYTE_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH3_DATA_BYTE_COUNT															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**CH3_DATA_BYTE_COUNT**	CH3_DATA_BYTE_COUNT	**The number of data bytes AHB bus transferred through serial flash controller channel 3 after enabling the performance monitor**

A0040800~A004089C SF_GPRAM_BASE[n](n=0~39) Serial flash macro read/write memory data (160 bytes) 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPRAM_DATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**GPRAM_DATA**	GPRAM_DATA	**Read/write SRAM data at register address (0x800 ~ 0x89f). SRAM data are MAC_OUT_LENGTH + MAC_IN_LENGTH**

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Bit(s)	Mnemonic	Name	Description
			bytes. Please read "twice" to access the data when the address is changed. (APB_CON[1] must be set to 1'b1 to read APB using 2T pclk)

17.10. sf_top serial flash delay control setting

Serial flash delay select settings are shown in Figure 17.10-1 and Figure 17.10-2.

Figure 17.10-1. Clock macro and clock delay select settings

Figure 17.10-2. Data macro and data delay select settings

A0040020 SF_DLY_CTL1 Serial flash delay control setting 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SFIO3_OUT_DLY								SFIO2_OUT_DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SFIO1_OUT_DLY								SFIO0_OUT_DLY			

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Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**SFIO3_OUT_DLY**	SFIO3_OUT_DLY	**Serial flash SFIO3 pin IO output delay setting**
19:16	**SFIO2_OUT_DLY**	SFIO2_OUT_DLY	**Serial flash SFIO2 pin IO output delay setting**
11:8	**SFIO1_OUT_DLY**	SFIO1_OUT_DLY	**Serial flash SFIO1 pin IO output delay setting**
3:0	**SFIO0_OUT_DLY**	SFIO0_OUT_DLY	**Serial flash SFIO0 pin IO output delay setting**

A0040024 SF_DLY_CTL2 Serial flash delay control setting 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**SFIO3_IN_DLY**								**SFIO2_IN_DLY**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			**SFIO1_IN_DLY**								**SFIO0_IN_DLY**					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**SFIO3_IN_DLY**	SFIO3_IN_DLY	**Serial flash SFIO3 pin IO input delay setting**
21:16	**SFIO2_IN_DLY**	SFIO2_IN_DLY	**Serial flash SFIO2 pin IO input delay setting**
13:8	**SFIO1_IN_DLY**	SFIO1_IN_DLY	**Serial flash SFIO1 pin IO input delay setting**
5:0	**SFIO0_IN_DLY**	SFIO0_IN_DLY	**Serial flash SFIO0 pin IO input delay setting**

A0040028 SF_DLY_CTL3 Serial flash delay control setting 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			**SFIFO_WR_EN_DLY_SEL**										**SFCS_DLY**			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**SFCK_OUT_DLY**						**SFCK_SAM_DLY**					
Type					RW						RW					
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**SFIFO_WR_EN_DLY_SEL**	SFIFO_WR_EN_DLY_SEL	**Serial flash FIFO write enable delay select setting**
19:16	**SFCS_DLY**	SFCS_DLY	**Serial flash SFCS pin IO output delay setting**
11:8	**SFCK_OUT_DLY**	SFCK_OUT_DLY	**Serial flash CK pin IO output delay setting**
5:0	**SFCK_SAM_DLY**	SFCK_SAM_DLY	**Serial flash sample clock delay setting**

A0040030 SF_DLY_CTL4 Serial flash delay control setting 4 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					SF2IO3_OUT_DLY								SF2IO2_OUT_DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SF2IO1_OUT_DLY								SF2IO0_OUT_DLY			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**SF2IO3_OUT_DLY**	SF2IO3_OUT_DLY	**Serial flash SF2IO3 pin IO output delay setting**
19:16	**SF2IO2_OUT_DLY**	SF2IO2_OUT_DLY	**Serial flash SF2IO2 pin IO output delay setting**
11:8	**SF2IO1_OUT_DLY**	SF2IO1_OUT_DLY	**Serial flash SF2IO1 pin IO output delay setting**
3:0	**SF2IO0_OUT_DLY**	SF2IO0_OUT_DLY	**Serial flash SF2IO0 pin IO output delay setting**

A0040034 SF_DLY_CTL5 Serial flash delay control setting 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SF2IO3_IN_DLY								SF2IO2_IN_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SF2IO1_IN_DLY								SF2IO0_IN_DLY					
Type			RW								RW					
Reset			0	0	0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
29:24	**SF2IO3_IN_DLY**	SF2IO3_IN_DLY	**Serial flash SF2IO3 pin IO input delay setting**
21:16	**SF2IO2_IN_DLY**	SF2IO2_IN_DLY	**Serial flash SF2IO2 pin IO input delay setting**
13:8	**SF2IO1_IN_DLY**	SF2IO1_IN_DLY	**Serial flash SF2IO1 pin IO input delay setting**
5:0	**SF2IO0_IN_DLY**	SF2IO0_IN_DLY	**Serial flash SF2IO0 pin IO input delay setting**

A0040038 SF_DLY_CTL6 Serial flash delay control setting 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			SF2FIFO_WR_EN_DLY_SEL										SFCS_DLY			
Type			RW										RW			
Reset			0	0	0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SFCK_OUT_DLY						SFCK_SAM_DLY					
Type					RW						RW					
Reset					0	0	0	0			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
29:24	**SF2FIFO_WR_EN_DLY_SEL**	SF2FIFO_WR_EN_DLY_SEL	**Serial flash 2 FIFO write enable delay select setting**
19:16	**SFCS_DLY**	SFCS_DLY	**Serial flash SFCS2 pin IO output delay setting**
11:8	**SFCK_OUT_DLY**	SFCK_OUT_DLY	**Serial flash 2 CK pin IO output delay setting**
5:0	**SFCK_SAM_DLY**	SFCK_SAM_DLY	**Serial flash 2 sample clock delay setting**

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18. Top Miscellaneous Registers (TOP_MISC)

18.1. Overview

The following registers are stored in the TOP_MISC module during the chip design, if:

1) Requires always-on (AO) domain attribute, but the corresponding module is in power down (PD) domain.
2) The corresponding module hierarchy is not suitable for the module control registers.

TOP_MISC register groups include:

1) GPIO related settings.
2) Software, hardware backup registers.
3) System information, including bounding, trapping, and more.
4) EMI and SF IO settings.
5) Keypad driving control.

18.2. Register mapping

Module name: top_misc_cfg Base address: (+a2010000h)

Address	Name	Width (bits)	Register Function
A2010000	GPIO_CLKO_CTRL_A	32	GPIO clock output selection
A2010004	GPIO_CLKO_CTRL_B	32	GPIO clock output selection
A2010020	SW_MISC0	32	Software miscellaneous registers
A2010040	SYSTEM_INFOD	32	System bonding and trapping information
A2010050	HW_MISC0	32	Hardware misc register
A2010054	HW_MISC1	32	Hardware misc register
A2010058	HW_MISC2	32	Hardware misc register
A201005C	HW_MISC3	32	Hardware misc register
A2010060	TOP_DEBUG	32	TOP debug register
A2010064	TOP_DEBUG_MON	32	Debug signals
A20100A0	SFC_SLT_SEL	16	Select the SF PAD at slt/dfunc mode
A20100A4	SFIO_CFG0	32	SF IO configuration registers
A20100A8	SFIO_CFG1	32	SF IO configuration registers
A20100AC	SFIO_CFG2	32	SF IO configuration registers
A20100C0	EMI_IOA	32	EMI configuration registers
A20100C4	EMI_IOB	32	EMI configuration registers
A20100C8	SDIO_DB_STATUS	32	SDIO SLAVE db status
A20100CC	TM_TRAP_REG	8	Trapping signals at test mode
A20100D0	TM_MUX_SEL	32	MUX selection at test mode for ana_mac
A20100E0	EXIT_XBOOT	16	Release the pad for external boot device
A20100F0	KEYPAD_DRV_CTRL	32	Set the pu/pd r0/r1 function for keypad

A2010000 GPIO_CLKO_CTRL_A GPIO clock output selection 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					clko_mode3								clko_mode2			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					clko_mode1								clko_mode0			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Mnemonic	Name	Description
27:24	**CLKO3**	clko_mode3	**selects the output clock source of CLKO3** 4'dxx: same as clko_mode0
19:16	**CLKO2**	clko_mode2	**selects the output clock source of CLKO2** 4'dxx: same as clko_mode0
11:8	**CLKO1**	clko_mode1	**selects the output clock source of CLKO1** 4'dxx: same as clko_mode0
3:0	**CLKO0**	clko_mode0	**selects the output clock source of CLKO0** 4'd15: hf_fcm_mclk_ck div4 4'd14: hf_fsys_emi2x_phy_hclk_ck div4 4'd13: f_fxo_mclk_ck div2 4'd12: f_fxo_hclk_ck div2 4'd11: hf_fbus_mclk_ck div2 4'd10: hf_fbus_hclk_ck div2 4'd9: hf_fbus_emi1x_phy_hclk_ck div2 4'd8: hf_fsfc_phy_hclk_ck div2 4'd7: AD_XO_BBTOP_CK 4'd6: AD_XPLL_CK 4'd5: f_f40m_ck 4'd4: f_fxo_2m_ck 4'd3: f_f48m_ck 4'd2: f_f24m_ck 4'd1: f_fxo_ck 4'd0: f_frtc_clkout_ck

A2010004 GPIO_CLKO_CTRL_B GPIO clock output selection 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													clko_mode4			
Type													RW			
Reset													0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0	**CLKO4**	clko_mode4	**selects the output clock source of CLKO4**

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Bit(s)	Mnemonic	Name	Description
			4'dxx:same as clko_mode0

A2010020 SW_MISC0 software misc registers 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SW_MISC0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**SW_MISC0**	SW_MISC0	**reserved**

A2010040 SYSTEM_INFOD system bonding and trapping information 01000400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SYSTEM_INFOD															
Type	RO															
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SYSTEM_INFOD															
Type	RO															
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
31:0	**SYSTEM_INFO**	SYSTEM_INFOD	**bit[0]: 1, the chip is trapping to download mode** bit[1]: 1, the chip is trapping to SLT mode bit[2]: reserved bit[3]: 1, enable external boot mode bit[4]: 1, external boot from SDIO, 0 means from SPI bit[5]: 1, 32kHz clock is generated from internal 26MHz clock. 0, 32kHz clock is from external crystal. bit[7:6]: reserved bit[8]: bond_psram_sip, 1, if there is PSRAM embedded inside the chip bit[9]: bond_sf_sip, 1, if there is SF (serial flash) embedded inside the chip bit[11:10]: reserved bit[15:12]: trapping mode at TESTMODE (Reserved) bit[20]: 1, the chip is at test mode

A2010050 HW_MISC0 Hardware misc register 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_MISC0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**HW_MISC0**	HW_MISC0	**Reserved for these 3 bits** Bit[0]: set 1 to inverse PMU go to sleep signals Bit[1]: set 1 to inverse PMU reset signal (to GPIO path) Bit[2]: set 1 to unmask conn2pmu_force_buck_pwm

A2010054 HW_MISC1 Hardware misc register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_MISC1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**HW_MISC1**	HW_MISC1	**reserved**

A2010058 HW_MISC2 Hardware misc register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_MISC2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**HW_MISC2**	HW_MISC2	**reserved**

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A201005C HW_MISC3 Hardware misc register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HW_MISC3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**HW_MISC3**	HW_MISC3	**reserved**

A2010060 TOP_DEBUG TOP debug register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_DEBUG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**TOP_DEBUG**	TOP_DEBUG	**reserved**

A2010064 TOP_DEBUG_MON debug signals 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TOP_DEBUG_MON															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
15:0	**TOP_DEBUG_MON**	TOP_DEBUG_MON	**reserved**

A20100A0 SFC_SLT_SEL select the SF PAD at slt/dfunc mode 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description

A20100A4 SFIO_CFG0 **SF IO configuration registers** **03270327**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sfio_cs_wp_cfg															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfio_cs_wp_cfg															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**cs_drc**	sfio_cs_wp_cfg	**bit[2 : 0]: sfio_cs_drc , default is 3'b111** bit[4 : 4]: sfio_cs_pd , default is 1'b0 bit[5 : 5]: sfio_cs_pu , default is 1'b1 bit[8 : 8]: sfio_cs_ies , default is 1'b1 bit[9 : 9]: sfio_cs_sr , default is 1'b1 bit[10:10]: sfio_cs_smt , default is 1'b0 bit[15:12]: sfio_all_tdsel,default is 4'b0000 bit[18:16]: sfio_wp_drv , default is 3'b111 bit[20:20]: sfio_wp_pd , default is 1'b0 bit[21:21]: sfio_wp_pu , default is 1'b1 bit[24:24]: sfio_wp_ies , default is 1'b1 bit[25:25]: sfio_wp_sr , default is 1'b1 bit[26:26]: sfio_wp_smt , default is 3'b0 bit[29:28]: sfio_all_rdsel, default is 2'b00

A20100A8 SFIO_CFG1 **SF IO configuration registers** **03170327**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	sfio_din_ck_cfg															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	sfio_din_ck_cfg															

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Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**din_drc**	sfio_din_ck_cfg	**bit[2 : 0]: sfio_din_drc , default is 3'b111** bit[4 : 4]: sfio_din_pd, default is 1'b0 bit[5 : 5]: sfio_din_pu, default is 1'b1 bit[8 : 8]: sfio_din_ies, default is 1'b1 bit[9 : 9]: sfio_din_sr, default is 1'b1 bit[10:10]: sfio_din_smt, default is 1'b0 bit[18:16]: sfio_ck_drv, default is 3'b111 bit[20:20]: sfio_ck_pd, default is 1'b1 bit[21:21]: sfio_ck_pu, default is 1'b0 bit[24:24]: sfio_ck_ies, default is 1'b1 bit[25:25]: sfio_ck_sr, default is 1'b1 bit[26:26]: sfio_ck_smt, default is 3'b0

A20100AC SFIO_CFG2 SF IO configuration registers 03170327

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**sfio_hold_dout_cfg**															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**sfio_hold_dout_cfg**															
Type	RW															
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1

Bit(s)	Mnemonic	Name	Description
31:0	**hold_drc**	sfio_hold_dout_cfg	**bit[2 : 0]: sfio_hold_drv, default is 3'b111** bit[4 : 4]: sfio_hold_pd, default is 1'b0 bit[5 : 5]: sfio_hold_pu, default is 1'b1 bit[8 : 8]: sfio_hold_ies, default is 1'b1 bit[9 : 9]: sfio_hold_sr, default is 1'b1 bit[10:10]: sfio_hold_smt, default is 1'b0 bit[18:16]: sfio_dout_drv, default is 3'b111 bit[20:20]: sfio_dout_pd, default is 1'b1 bit[21:21]: sfio_dout_pu, default is 1'b0 bit[24:24]: sfio_dout_ies, default is 1'b1 bit[25:25]: sfio_dout_sr, default is 1'b1 bit[26:26]: sfio_dout_smt, default is 3'b0

A20100C0 EMI_IOA EMI configuration registers 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**EMI_IOA_CFG**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**EMI_IOA_CFG**															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**ca_e2**	EMI_IOA_CFG	**bit[0 :0]: emi_ca_e2, default is 1'b1. ca pad driving current setting** bit[1 :1]: emi_ca_e4, default is 1'b0. ca pad driving current setting bit[2 :2]: emi_ca_e8, default is 1'b0. ca pad driving current setting bit[3 :3]: emi_ca_sr, default is 1'b0. ca pad slew rate setting bit[4 :4]: emi_ca_pu, default is 1'b0. ca pad pull up setting bit[5 :5]: emi_ca_pd, default is 1'b0. ca pad pull down setting bit[7 :7]: emi_ca_ies, default is 1'b0. ca pad input buffer gating control bit[11 :8]: emi_ca_tdsel, default is 4'h0. ca pad TX delay(duty) control bit[16 :16]: emi_ck_e2, default is 1'b1. ck pad driving current setting bit[17 :17]: emi_ck_e4, default is 1'b0. ck pad driving current setting bit[18 :18]: emi_ck_e8, default is 1'b0. ck pad driving current setting bit[19 :19]: emi_ck_sr, default is 1'b0. ck pad slew rate setting bit[20 :20]: emi_ck_pu, default is 1'b0. ck pad pull up setting bit[21 :21]: emi_ck_pd, default is 1'b0. ck pad pull down setting bit[22 :22]: emi_ck_smt, default is 1'b0. ck pad Schmitt trigger setting bit[23 :23]: emi_ck_ies, default is 1'b0. ck pad input buffer gating control bit[27 :24]: emi_ck_tdsel, default is 4'b0. ck pad TX delay (duty) control bit[29 :28]: emi_ck_rdsel, default is 2'b0. ck pad RX delay (duty) control

A20100C4 EMI_IOB EMI configuration registers 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EMI_IOB_CFG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EMI_IOB_CFG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Mnemonic	Name	Description
31:0	**dq_e2**	EMI_IOB_CFG	**bit[0 :0]: emi_dq_e2, default is 1'b1. dq pad driving current setting** bit[1 :1]: emi_dq_e4, default is 1'b0. dq pad driving

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Bit(s)	Mnemonic	Name	Description
			current setting bit[2 :2]: emi_dq_e8, default is 1'b0. dq pad driving current setting bit[3 :3]: emi_dq_sr, default is 1'b0. dq pad slew rate setting bit[4 :4]: emi_dq_pu, default is 1'b0. dq pad pull up setting bit[5 :5]: emi_dq_pd, default is 1'b0. dq pad pull down setting bit[6 :6]: emi_dq_smt, default is 1'b0. dq pad Schmitt trigger setting bit[7 :7]: emi_dq_ies, default is 1'b0. dq pad input buffer gating control bit[11 :8]: emi_dq_tdsel, default is 4'b0. dq pad TX delay select bit[13 :12]: emi_dq_rdsel, default is 2'b0. dq pad RX delay select bit[16 :16]: emi_dqs_e2, default is 1'b1. dqs pad driving current setting bit[17 :17]: emi_dqs_e4, default is 1'b0. dqs pad driving current setting bit[18 :18]: emi_dqs_e8, default is 1'b0. dqs pad driving current setting bit[19 :19]: emi_dqs_sr, default is 1'b0. dqs pad slew rate setting bit[20 :20]: emi_dqs_pu, default is 1'b0. dqs pad pull up setting bit[21 :21]: emi_dqs_pd, default is 1'b0. dqs pad pull down setting bit[22 :22]: emi_dqs_smt, default is 1'b0. dqs pad smitter trigger setting bit[23 :23]: emi_dqs_ies, default is 1'b0. dqs pad input buffer gating control bit[27 :24]: emi_dqs_tdsel, default is 4'b0. dqs pad TX delay (duty) control bit[29 :28]: emi_dqs_rdsel, default is 2'b0. dqs pad RX delay (duty) control

A20100C8 SDIO_DB_STATUS SDIO SLAVE db status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SDIO_DB_STATUS							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0	**SDIO_DB_STATUS**	SDIO_DB_STATUS	**SDIO slave status**

A20100CC TM_TRAP_REG trapping signals at testmode 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												TM_TRAP_REG				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		TM_TRAP_REG	**TBD**

A20100D0 TM_MUX_SEL mux selection at testmode for ana_mac 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																tm_dcxo_ctrl_sel
Type																RW
Reset																0

Bit(s)	Mnemonic	Name	Description
0		tm_dcxo_ctrl_sel	**TBD**

A20100E0 EXIT_XBOOT release the pad for external boot device 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								exit_sdio_xboot								exit_spi_xboot
Type								RW								RW
Reset								0								0

Bit(s)	Mnemonic	Name	Description

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Bit(s)	Mnemonic	Name	Description
8		exit_sdio_xboot	**TBD**
0		exit_spi_xboot	**TBD**

A20100F0 KEYPAD_DRV_CTRL set the pu/pd r0/r1 function for keypad 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							top_kp_col_r1r0									top_kp_col_pupd
Type							RW									RW
Reset							0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							top_kp_row_r1r0									top_kp_row_pupd
Type							RW									RW
Reset							0	0								0

Bit(s)	Mnemonic	Name	Description
25:24		top_kp_col_r1r0	**TBD**
16		top_kp_col_pupd	**TBD**
9:8		top_kp_row_r1r0	**TBD**
0		top_kp_row_pupd	**TBD**

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19. USB 1.1 Full Speed Controller

19.1. Introduction

The USB11 device controller supports only full-speed (12Mbps) operation. The chip can make use of this widely available USB interfaces to transmit/receive data with USB hosts, typically PC/laptop. The controller is configured for supporting 4 endpoints for IN transactions and 2 endpoints for OUT transactions. These endpoints can be individually configured in the software to handle either Bulk transfers, Interrupt transfers or Isochronous transfers. The controller features 4 DMA channels to accelerate the data transfer and the embedded RAM size is configurable size up to 352 bytes.

19.2. Abbreviation

Table 19.2-1. Abbreviations

Abbreviation	Definition
SIE	Serial Interface Engeine
CDR	Clock Data Recovery

19.3. Feature

The following table lists the unified USB IP features.

Feature list	Description
USB specifications	USB11 Device
Endpoint	4 Tx 2 Rx EP0
DMA channel	4
Embedded RAM	352 byte
CPU slave interface	AHB asynchronous design

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19.4. USB11 Controller Block Diagram

Figure 19.4-1. USB controller block diagram

The USB primarily contains the following sub-block:

Sub-block	Sub-block Description
Endpoint Control	The EP is used to communicate with opposite physical hardware. All USB transaction and protocol handshake can be executed by EP. Detailed information can refer to USB standard. In addition, EP number in USB IP can be configured easily and confirmed by SW based on USB real application.
RAM Controller	RAM controller is used to control and access USB internal SRAM
Packet Encode/Decode	The block is used to encode/decode USB packet format transferred via USB bus
Bus Asynchronous Wrapper	System bus is used to connect to platform fabric and accessed by CPU or access system memory. However, system bus may run at high speed clock frequency to gain overall system performance so the block is used to separate different clock domain and deal with the transaction between system bus clock domain and USB MAC clock domain
Serial Interface Engeine	The block is used to do USB1.1 CDR, serial-parallel from USB bus and parallel-serial to USB bus translation.

19.5. Register mapping

Address	Name	Width	Register Function
A1060000	USB_FADDR	8	USB function address register
A1060001	USB_POWER	8	USB power control register
A1060002	USB_INTRIN	16	USB IN endpoints interrupt register
A1060004	USB_INTROUT	16	USB OUT endpoints interrupt register
A1060006	USB_INTRUSB	8	USB general interrupt register
A1060007	USB_INTRINE	16	USB IN endpoints interrupt enable register
A1060009	USB_INTROUTE	16	USB OUT endpoints interrupt enable

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Address	Name	Width	Register Function
			register
A106000B	INTRUSBE	8	USB general interrupt enable register
A106000C	USB_FRAME1	8	USB frame count #1 register
A106000D	USB_FRAME2	8	USB frame count #2 register
A106000E	USB_INDEX	8	USB endpoint register index
A106000F	USB_RSTCTRL	8	USB reset control
A1060011	USB_EP0_CSR	8	USB control/status register for endpoint 0
A1060016	USB_EP0_COUNT	8	EP0 Received Bytes Count Register
A1060010	USB_EP_INMAXP	8	USB maximum packet size register for IN endpoint
A1060011	USB_EP_INCSR1	8	USB control/status register #1 for IN endpoint
A1060012	USB_EP_INCSR2	8	USB control/status register #2 for IN endpoint
A1060013	USB_EP_OUTMAXP	8	USB maximum packet size register for OUT endpoint
A1060014	USB_EP_OUTCSR1	8	USB control/status register #1 for OUT endpoint
A1060015	USB_EP_OUTCSR2	8	USB control/status register #2 for OUT endpoint
A1060016	USB_EP_COUNT1	8	USB OUT endpoint byte counter register LSB part for endpoint
A1060017	USB_EP_COUNT2	8	USB OUT endpoint byte counter register MSB part for endpoint
A1060020	USB_EP0_FIFO_DB0	8	USB Endpoint 0 FIFO Register DB0
A1060021	USB_EP0_FIFO_DB1	8	USB Endpoint 0 FIFO Register DB1
A1060022	USB_EP0_FIFO_DB2	8	USB Endpoint 0 FIFO Register DB2
A1060023	USB_EP0_FIFO_DB3	8	USB Endpoint 0 FIFO Register DB3
A1060024	USB_EP1_FIFO_DB0	8	USB endpoint 1 FIFO Register DB0
A1060025	USB_EP1_FIFO_DB1	8	USB endpoint 1 FIFO Register DB1
A1060026	USB_EP1_FIFO_DB2	8	USB endpoint 1 FIFO Register DB2
A1060027	USB_EP1_FIFO_DB3	8	USB endpoint 1 FIFO Register DB3
A1060028	USB_EP2_FIFO_DB0	8	USB endpoint 2 FIFO Register DB0
A1060029	USB_EP2_FIFO_DB1	8	USB endpoint 2 FIFO Register DB1
A106002A	USB_EP2_FIFO_DB2	8	USB endpoint 2 FIFO Register DB2
A106002B	USB_EP2_FIFO_DB3	8	USB endpoint 2 FIFO Register DB3
A106002C	USB_EP3_FIFO_DB0	8	USB endpoint 3 FIFO Register DB0
A106002D	USB_EP3_FIFO_DB1	8	USB endpoint 3 FIFO Register DB1
A106002E	USB_EP3_FIFO_DB2	8	USB endpoint 3 FIFO Register DB2
A106002F	USB_EP3_FIFO_DB3	8	USB endpoint 3 FIFO Register DB3
A1060030	USB_EP4_FIFO_DB0	8	USB endpoint 4 FIFO Register DB0
A1060031	USB_EP4_FIFO_DB1	8	USB endpoint 4 FIFO Register DB1
A1060032	USB_EP4_FIFO_DB2	8	USB endpoint 4 FIFO Register DB2
A1060033	USB_EP4_FIFO_DB3	8	USB endpoint 4 FIFO Register DB3
A1060240	USB_CON	8	USB PHY control

A1060000 USB_FADDR USB function address register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**UPD**	**FADDR**						
Type									RW	RW						
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	UPD	**This is an 8bit register that should be written with the functions 7bit address (received through a SET_ADDRESS description). It is then used for decoding the function address in subsequent token packets.** When set by the MCU, the core will wait for an SOF token from the time INPKTRDY is set before sending the packet
6:0	FADDR	**The function address of the device**

A1060001 USB_POWER USB power control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**ISOUPDATE**			**SWRSTENAB**	**RESET**	**RESUME**	**SUSPMODE**	**SUSPENAB**
Type									RW			RU	RU	RW	RU	RW
Reset									0			0	0	0	0	0

Bit(s)	Name	Description
7	ISOUPDATE	**When set by the MCU, the core will wait for an SOF token from the time INPKTRDY is set before sending the packet**
4	SWRSTENAB	**Set by the MCU to enable the mode in which the device can only be reset by the software after detecting reset signals on the bus. In case the software is delayed by other high priority process and cant make it to read the command from the buffer before the hardware reset the device after detecting the reset signal on the bus, the command will be lost. Thats why the software reset mode is effective. When the flag is enabled, the hardware state machine cant reset by itself, but rather can be reset by the software. In that sense, the software and the hardware can keep synchronous on detecting the reset signal.**
3	RESET	**The read only bit is set when Reset signaling is present on the bus**
2	RESUME	**Set by the MCU to generate Resume signaling when the function is in suspend mode. The MCU should clear this bit after 10 ms (a maximum of 15 ms) to end Resume signaling**
1	SUSPMODE	**Set by the USB core when Suspend mode is entered. It is cleared when sets the Resume bit of this register**

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Bit(s)	Name	Description
0	SUSPENAB	**Set by the MCU to enable device into Suspend mode when Suspend signaling is received on the bus**

A1060002 USB_INTRIN USB IN endpoints interrupt register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												EP4_IN	EP3_IN	EP2_IN	EP1_IN	EP0
Type												RC	RC	RC	RC	RC
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	EP4_IN	**IN Endpoint 4 interrupt event.**
3	EP3_IN	**IN Endpoint 3 interrupt event.**
2	EP2_IN	**IN Endpoint 2 interrupt event.**
1	EP1_IN	**IN Endpoint 1 interrupt event.**
0	EP0	**Endpoint0 interrupt event_x000D_**

A1060004 USB_INTROUT USB OUT endpoints interrupt register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EP2_OUT	EP1_OUT	
Type														RC	RC	
Reset														0	0	

Bit(s)	Name	Description
2	EP2_OUT	**OUT Endpoint 2 interrupt event.**
1	EP1_OUT	**OUT Endpoint 1 interrupt event.**

A1060006 USB_INTRUSB USB general interrupt register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam												PO	SO	RE	RE	SU

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e												WERDWN	F	SET	SUME	SPEND
Type												RC	RC	RC	RC	RC
Reset												0	0	0	0	0

Bit(s)	Name	Description
4	POWERDWN	**Set at SUSPMODE and LineState is JState. Programmer should have de bounce scheme in SW code when use this interrupt**
3	SOF	**Set at the start of each frame**
2	RESET	**Set when Reset signaling is detected on the bus**
1	RESUME	**Set when Resume signaling is detected on the bus while the USB core is in suspend mode**
0	SUSPEND	**Set when Suspend signaling is detected on the bus**

A1060007 USB_INTRINE USB IN endpoints interrupt enable register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												EP4_INE	EP3_INE	EP2_INE	EP1_INE	EP0_E
Type												RW	RW	RW	RW	RW
Reset												1	1	1	1	1

Bit(s)	Name	Description
4	EP4_INE	**1b0: IN Endpoint 4 interrupt event disable_x000D_** 1b1: IN Endpoint 4 interrupt event enable_x000D_
3	EP3_INE	**1b0: IN Endpoint 3 interrupt event disable_x000D_** 1b1: IN Endpoint 3 interrupt event enable_x000D_
2	EP2_INE	**1b0: IN Endpoint 2 interrupt event disable_x000D_** 1b1: IN Endpoint 2 interrupt event enable_x000D_
1	EP1_INE	**1b0: IN Endpoint 1 interrupt event disable_x000D_** 1b1: IN Endpoint 1 interrupt event enable_x000D_
0	EP0_E	**1b0: IN Endpoint 0 interrupt event disable_x000D_** 1b1: IN Endpoint 0 interrupt event enable_x000D_

A1060009 USB_INTROUTE USB OUT endpoints interrupt enable register 000000FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														EP2_OUT	EP1_OUT	

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														TE	E	
Type														RW	RW	
Reset														1	1	

Bit(s)	Name	Description
2	EP2_OUTE	**1b0: OUT Endpoint 2 interrupt event disable** 1b1: OUT Endpoint 2 interrupt event enable
1	EP1_OUTE	**1b0: OUT Endpoint 1 interrupt event disable** 1b1: OUT Endpoint 1 interrupt event enable

A106000B INTRUSBE USB general interrupt enable register 00000006

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												POWERDWN_E	SOF_E	RESET_E	RESEUM_E	SUSPEND_E
Type												RW	RW	RW	RW	RW
Reset												0	0	1	1	0

Bit(s)	Name	Description
4	POWERDWN_E	**PowerDown interrupt enable**
3	SOF_E	**SOF interrupt enable_x000D_**
2	RESET_E	**Reset/Babble interrupt enable**
1	RESEUM_E	**Resume interrupt enable**
0	SUSPEND_E	**Suspend interrupt enable._x000D_**

A106000C USB_FRAME1 USB frame count #1 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									NUML							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	NUML	**The lower 8 bits of the frame number**

A106000D USB_FRAME2 USB frame count #2 register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														**NUMH**		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	NUMH	**The upper 3 bits of the frame number**

A106000E USB_INDEX USB endpoint register index 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													**INDEX**			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	INDEX	**The register determines which endpoint control/status registers are to be accessed at addresses USB+10h to USB+17h. Each IN endpoint and each OUT endpoint have their own set of control/status registers. Only one set of IN control/status and one set of OUT control/status registers appear in the memory map at any one time. Before accessing an endpoints control/status registers, the endpoint number should be written to the USB_INDEX register to ensure that the correct control/status registers appear in the memory map.** INDEX The index of the endpoint.

A106000F USB_RSTCTRL USB reset control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SWRST**				**RSTCNTR**			
Type									RW				RW			
Rese									0				0	0	0	0

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t																

Bit(s)	Name	Description
7	SWRST	If the flag SWRSTENAB in the register USB_POWER is set to be 1, the software enable mode is enabled, and the device can be reset by writing this flag to be 1
3:0	RSTCNTR	The field signifies the duration for the reset operation to take place after detecting reset signal on the bus. Its only enabled when software reset is not enabled. If the value is equal to zero, the duration is 2.5us. Otherwise, the duration is equal to this value multiplied by 341 and then added by 2.5 in unit of us. The range consequently starts from 2.5us to 5122.5 us

A1060011 USB_EP0_CSR **USB control/status register for endpoint 0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SSETUPEND	SOUTPKTRDY	SENDSTALL	SETUPEND	DATAEND	SENTSTALL	INPKTRDY	OUTPKTRDY
Type									A0	A0	A0	RU	A0	A1	A0	RU
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	SSETUPEND	The MCU writes a 1 to this bit to clear the SETUPEND bit. Its cleared automatically. Only active when a transaction has been started
6	SOUTPKTRDY	The MCU writes a 1 to this bit to clear the OUTPKTRDY bit. Its cleared automatically. Only active when an OUT transaction has been started
5	SENDSTALL	The MCU writes a 1 to this bit to terminate the current transaction. The STALL handshake will be transmitted and then this bit will be cleared automatically
4	SETUPEND	This bit will be set when a control transaction ends before the DATAEND bit has been set. An interrupt will be generated and FIFO flushed at this time. The bit is cleared by the MCU writing a 1 to the SSETUPEND bit.
3	DATAEND	The MCU sets this bit: 1. When setting INPKTRDY for the last data packet. 2. When clearing OUTPKTRDY after unloading the last data packet. 3. When setting INPKTRDY for a zero length data packet. Its cleared automatically
2	SENTSTALL	This bit is set when a STALL handshake is transmitted. The MCU should clear this bit by writing a 0
1	INPKTRDY	The MCU sets this bit after loading a data packet into the FIFO. It is cleared automatically when the data packet has been transmitted. An interrupt is generated when this bit is set
0	OUTPKTRDY	This bit is set when a data packet has been received. An interrupt is generated when this bit is set. The MCU clears

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Bit(s)	Name	Description
		this bit by setting the SOUTPKTRDY bit

A1060016 USB_EP0_COUNT EP0 Received Bytes Count Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EP0_COUNT						
Type										RU						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	EP0_COUNT	**The register indicates the number of received data bytes in the endpoint 0. The value returned is valid while OUTPKTRDY bit of USB_EP0_CSR register is set. The register is active when USB_INDEX register is set to 0.** COUNT The number of received data bytes in the endpoint 0

A1060010 USB_EP_INMAXP USB maximum packet size register for IN endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MAXP							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	MAXP	**The register holds the maximum packet size for transactions through the currently selected IN endpoint - in units of one byte. In setting the value, the programmer should note the constraints placed by the USB Specification on packet size for bulk interrupt, and isochronous transactions in full speed operations. There is an INMAXP register for each IN endpoint except endpoint 0. The registers are active when USB_INDEX register is set to 1, 2, 3, and 4 respectively.** The value written to this register should match the wMaxPacketSize field of the standard endpoint descriptor for the associated endpoint. A mismatch could cause unexpected results. If a value greater than the configured IN FIFO size for the endpoint is written to the register, the value will be automatically changed to the IN FIFO size. If the value written to the register is less than, or equal to, half the IN FIFO size, two IN packets can be buffered. The

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Bit(s)	Name	Description
		configured IN FIFO size for the endpoint 1, 2, and 3, are 16 bytes, 64 bytes, and 64 bytes, respectively. The register is reset to 0. If the register is changed after packets have been sent from the endpoint, the endpoint IN FIFO should be completely flushed after writing the new value to the register. MAXP The maximum packet size in units of one byte

A1060011 USB_EP_INCSR1 USB control/status register #1 for IN endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**ABORTPKT_EN**	**CLRDATATOG**	**SENTSTALL**	**SENDSTALL**	**FLUSHFIFO**	**UNDERRUN**	**FIFONOTEMPTY**	**INPKTRDY**
Type									RW	A0	A1	RW	A0	A1	RU	A0
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	ABORTPKT_EN	**When MCU write ABORTPKT_EN as 1, FLUSHFIFO switch to abort packet function. This bit should be enabled before FLUSHFIFO is set. If FLUSHFIFO is set and ABORTPKT_EN is enabled the data loaded into FIFO will be discarded. After aborting packet, EP will issue an interrupt. Programmer should wait for this interrupt to make sure the packet is aborted**
6	CLRDATATOG	**The MCU writes a 1 to this bit to reset the endpoint IN data toggle to 0**
5	SENTSTALL	**The bit is set when a STALL handshake is transmitted. The FIFO is flushed and the INPKTRDY bit is cleared. The MCU should clear this bit by writing a 0 to this bit**
4	SENDSTALL	**The MCU writes a 1 to this bit to issue a STALL handshake to an IN token. The MCU clears this bit to terminate the stall condition**
3	FLUSHFIFO	**The MCU writes a 1 to this bit to flush the next packet to be transmitted from the endpoint IN FIFO. The FIFO pointer is reset and the INPKTRDY bit is cleared. If the FIFO contains two packets, FLUSHFIFO will need to be set twice to completely clear the FIFO. FLUSHFIFO should only be used when INPKTRDY is set. At other times, it may cause data to be corrupted.** If ABORTPKT_EN is enabled and this bit is set , the function of this bit becomes ABORTPKT to abort the next packet to be transmitted from the endpoint IN FIFO and doesnt need to set INPKTRDY. The same with FLUSHFIFO function, this bit is only active when endpoint is idle
2	UNDERRUN	**In isochronous mode, this bit is set when a zero length data packet is sent after receiving an IN token with the INPKTRDY bit not set. In Bulk/Interrupt mode, this bit is set when a NAK is returned in response to an IN token. The MCU should clear this bit by writing a 0 to this bit**
1	FIFONOTEMPTY	**This bit is set when there is at least 1 packet in the IN FIFO**

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Bit(s)	Name	Description
0	INPKTRDY	The MCU sets this bit after loading a data packet into the FIFO. Only active when an IN transaction has been started. It is cleared automatically when a data packet has been transmitted. An interrupt is generated (if enabled) when the bit is cleared

A1060012 USB_EP_INCSR2 USB control/status register #2 for IN endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTOSET	ISO	MODE	DMAENAB	FRCDATATOG			
Type									RW	RW	RW	RW	RW			
Reset									0	0	0	0	0			

Bit(s)	Name	Description
7	AUTOSET	If the MCU sets the bit, INPKTRDY will be automatically set when data of the maximum packet size (value in INMAXP) is loaded into the IN FIFO. If a packet of less than the maximum packet size is loaded, then INPKTRDY will have to be set manually. When 2 packets are in the IN FIFO then INPKTRDY will also be automatically set when the first packet has been sent, if the second packet is the maximum packet size
6	ISO	The MCU sets this bit to enable the IN endpoint for isochronous transfer, and clears it to enable the IN endpoint for bulk/interrupt transfers
5	MODE	The MCU sets this bit to enable the endpoint direction as IN, and clears it to enable the endpoint direction as OUT. Its valid only where the same endpoint FIFO is used for both IN and OUT transaction
4	DMAENAB	The MCU sets this bit to enable the DMA request for the IN endpoint
3	FRCDATATOG	The MCU sets this bit to force the endpoints IN data toggle to switch after each data packet is sent regardless of whether an ACK was received. This can be used by interrupt IN endpoints which are used to communicate rate feedback for isochronous endpoints

A1060013 USB_EP_OUTMAXP USB maximum packet size register for OUT endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									MAXP							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	MAXP	**This register holds the maximum packet size for transactions through the currently selected OUT endpoint - in units of one byte. In setting this value, the programmer should note the constraints placed by the USB specification on packet sizes for bulk, interrupt, and isochronous transactions in full speed operations. There is an OUTMAXP register for each OUT endpoint except endpoint 0. The registers are active when USB_INDEX register is set to 1 and 2 respectively.** The value written to this register should match the wMaxPacketSize field of the standard endpoint descriptor for the associated endpoint. A mismatch could cause unexpected results. The total amount of data represented by the value written to this register must not exceed the FIFO size for the OUT endpoint, and should not exceed half the FIFO size if double buffering is required. If a value greater than the configured OUT FIFO size for the endpoint is written to the register, the value will be automatically changed to the OUT FIFO size. If the value written to the register is less than, or equal to, half the OUT FIFO size, two OUT packets can be buffered. The configured IN FIFO size for the endpoint 1, 2, and 3 are both 16, 64, and 64 bytes, respectively. MAXP The maximum packet size in units of one byte.

A1060014 USB_EP_OUTCSR1 USB control/status register #1 for OUT endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CLRDTATOG	SENTSTALL	SENDSTALL	FLUSHFIFO	DATAERROR	OVERRUN	FIFOFULL	RXPKTRDY
Type									A0	A1	RW	A0	RU	A1	RU	A1
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	CLRDTATOG	**The MCU writes a 1 to this bit to reset the endpoint data toggle to 0**
6	SENTSTALL	**The bit is set when a STALL handshake is transmitted. The MCU should clear this bit by writing a 0.**
5	SENDSTALL	**The MCU writes a 1 to this bit to issue a STALL handshake. The MCU clears this bit to terminate the stall condition. This bit has no effect if the OUT endpoint is in isochronous mode**
4	FLUSHFIFO	**The MCU writes a 1 to this bit to flush the next packet to be**

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Bit(s)	Name	Description
		read from the endpoint OUT FIFO. If the FIFO contains two packets, FLUSHFIFO will need to be set twice to completely clear the FIFO. FLUSHFIFO should only be used when OUTPKTRDY is set. At other times, it may cause data to be corrupted
3	DATAERROR	The bit is set when OUTPKTRDY is set if the data packet has a CRC or bit stuff error. It is cleared when OUTPKTRDY is cleared. This bit is only valid in isochronous mode
2	OVERRUN	The bit is set if an OUT packet cannot be loaded into the OUT FIFO. The MCU should clear the bit by writing a zero. This bit is only valid in isochronous mode
1	FIFOFULL	This bit is set when no more packets can be loaded into the OUT FIFO
0	RXPKTRDY	The bit is set when a data packet has been received. The MCU should clear (write a 0 to) the bit when the packet has been unloaded from the OUT FIFO. An interrupt is generated when the bit is set. When receiving null packet , OUTPKTRDY has been set after USB_INTROUT1 is high.

A1060015 USB_EP_OUTCSR2 USB control/status register #2 for OUT endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									AUTOCLEAR	ISO	DMAENAB	DMAMODE				
Type									RW	RW	RW	RW				
Reset									0	0	0	0				

Bit(s)	Name	Description
7	AUTOCLEAR	If the MCU sets this bit then the OUTPKTRDY bit will be automatically cleared when a packet of OUTMAXP bytes has been unloaded from the OUT FIFO. When packets of less then the maximum packet size are unloaded, OUTPKTRDY will have to be cleared manually.
6	ISO	The MCU sets this bit to enable the OUT endpoint for isochronous transfers, and clears it to enable the OUT endpoint for bulk/interrupt transfers
5	DMAENAB	The MCU sets this bit to enable the DMA request for the OUT endpoint
4	DMAMODE	Two modes of DMA operation are supported: DMA mode 0 in which a DMA request is generated for all received packets, together with an interrupt (if enabled); and DMA mode 1 in which a DMA request (but no interrupt) is generated for OUT packets of size OUTMAXP bytes and an interrupt (but no DMA request) is generated for OUT packets of any other size. The MCU sets the bit to select DMA mode 1 and clears this bit to select DMA mode 0

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A1060016 USB_EP_COUNT1 USB OUT endpoint byte counter register LSB part for endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									NUML							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	NUML	**The register holds the lower 8 bits of the number of received data bytes in the packet in the FIFO associated with the currently selected OUT endpoint. The value returned is valid while OUTPKTRDY in the register USB_OUTCSR1 is set. The registers are active when USB_INDEX register is set to 1 and 2 respectively.** NUML The lower 8 bits of the number of received data bytes for the OUT endpoint

A1060017 USB_EP_COUNT2 USB OUT endpoint byte counter register MSB part for endpoint 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														NUMH		
Type														RU		
Reset														0	0	0

Bit(s)	Name	Description
2:0	NUMH	**The register holds the upper 3 bits of the number of received data bytes in the packet in the FIFO associated with the currently selected OUT endpoint. The value returned is valid while OUTPKTRDY in the register USB_EP_OUTCSR1 is set. The registers are active when USB_INDEX register is set to 1 and 2 respectively.** NUMH The upper 8 bits of the number of received data bytes for the OUT endpoint.

A1060020 USB_EP0_FIFO_DB0 USB Endpoint 0 FIFO Register DB0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																

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Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFO0_DB0**							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO0_DB0	**The register provides MCU access to the FIFO for the endpoint 0. Writing to this register loads data into the FIFO for the endpoint 0. Reading from this register unloads data from the FIFO for the endpoint 0.** The register provides word, half word, and byte mode access. If word or half word accesses are performed, the less significant byte corresponds to the prior byte to load in or unload from the FIFO. DB0 The first byte to be loaded into or unloaded from the FIFO.

A1060021 USB_EP0_FIFO_DB1 USB Endpoint 0 FIFO Register DB1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFO0_DB1**							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO0_DB1	**DB1 The second byte to be loaded into or unloaded from the FIFO.**

A1060022 USB_EP0_FIFO_DB2 USB Endpoint 0 FIFO Register DB2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFO0_DB2**							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO0_DB2	**DB2 The third byte to be loaded into or unloaded from the FIFO.**

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A1060023 USB_EP0_FIFO_DB3 USB Endpoint 0 FIFO Register DB3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO0_DB3							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO0_DB3	**DB3 The forth byte to be loaded into or unloaded from the FIFO.**

A1060024 USB_EP1_FIFO_DB0 USB endpoint 1 FIFO Register DB0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO1_DB0							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO1_DB0	**The register provides MCU access to the FIFO for the endpoint 1. Writing to this register loads data into the FIFO for the endpoint 1. Reading from this register unloads data from the FIFO for the endpoint 1.** The register provides word, half word, and byte mode access. If word or half word accesses are performed, the less significant byte corresponds to the prior byte to load in or unload from the FIFO. DB0 The first byte to be loaded into or unloaded from the FIFO.

A1060025 USB_EP1_FIFO_DB1 USB endpoint 1 FIFO Register DB1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO1_DB1							
Type									OTHER							

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Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO1_DB1	**DB1 The second byte to be loaded into or unloaded from the FIFO.**

A1060026 USB_EP1_FIFO_DB2 USB endpoint 1 FIFO Register DB2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO1_DB2							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO1_DB2	**DB2 The third byte to be loaded into or unloaded from the FIFO.**

A1060027 USB_EP1_FIFO_DB3 USB endpoint 1 FIFO Register DB3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO1_DB3							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO1_DB3	**DB3 The forth byte to be loaded into or unloaded from the FIFO.**

A1060028 USB_EP2_FIFO_DB0 USB endpoint 2 FIFO Register DB0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO2_DB0							

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Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO2_DB0	**The register provides MCU access to the FIFO for the endpoint 2. Writing to this register loads data into the FIFO for the endpoint 2. Reading from this register unloads data from the FIFO for the endpoint 2.** The register provides word, half word, and byte mode access. If word or half word accesses are performed, the less significant byte corresponds to the prior byte to load in or unload from the FIFO. DB0 The first byte to be loaded into or unloaded from the FIFO.

A1060029 USB_EP2_FIFO_DB1 USB endpoint 2 FIFO Register DB1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFO2_DB1**							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO2_DB1	**DB1 The second byte to be loaded into or unloaded from the FIFO.**

A106002A USB_EP2_FIFO_DB2 USB endpoint 2 FIFO Register DB2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**FIFO2_DB2**							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO2_DB2	**DB2 The third byte to be loaded into or unloaded from the FIFO.**

A106002B USB_EP2_FIFO_DB3 USB endpoint 2 FIFO Register DB3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Nam																

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e																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO2_DB3							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO2_DB3	**DB3 The forth byte to be loaded into or unloaded from the FIFO.**

A106002C USB_EP3_FIFO_DB0 USB endpoint 3 FIFO Register DB0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO3_DB0							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO3_DB0	**The register provides MCU access to the FIFO for the endpoint 3. Writing to this register loads data into the FIFO for the endpoint 3. Reading from this register unloads data from the FIFO for the endpoint 3.** The register provides word, half word, and byte mode access. If word or half word accesses are performed, the less significant byte corresponds to the prior byte to load in or unload from the FIFO. DB0 The first byte to be loaded into or unloaded from the FIFO.

A106002D USB_EP3_FIFO_DB1 USB endpoint 3 FIFO Register DB1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO3_DB1							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO3_DB1	**DB1 The second byte to be loaded into or unloaded from**

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Bit(s)	Name	Description
		the FIFO.

A106002E USB_EP3_FIFO_DB2 USB endpoint 3 FIFO Register DB2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO3_DB2							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO3_DB2	DB2 The third byte to be loaded into or unloaded from the FIFO.

A106002F USB_EP3_FIFO_DB3 USB endpoint 3 FIFO Register DB3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO3_DB3							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO3_DB3	DB3 The forth byte to be loaded into or unloaded from the FIFO.

A1060030 USB_EP4_FIFO_DB0 USB endpoint 4 FIFO Register DB0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO4_DB0							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:0	FIFO4_DB0	**The register provides MCU access to the FIFO for the endpoint 4. Writing to this register loads data into the FIFO for the endpoint 4. Reading from this register unloads data from the FIFO for the endpoint 4.** The register provides word, half word, and byte mode access. If word or half word accesses are performed, the less significant byte corresponds to the prior byte to load in or unload from the FIFO. DB0 The first byte to be loaded into or unloaded from the FIFO.

A1060031 USB_EP4_FIFO_DB1 USB endpoint 4 FIFO Register DB1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO4_DB1							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO4_DB1	**DB1 The second byte to be loaded into or unloaded from the FIFO.**

A1060032 USB_EP4_FIFO_DB2 USB endpoint 4 FIFO Register DB2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO4_DB2							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO4_DB2	**DB2 The third byte to be loaded into or unloaded from the FIFO.**

A1060033 USB_EP4_FIFO_DB3 USB endpoint 4 FIFO Register DB3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Rese																

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									FIFO4_DB3							
Type									OTHER							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	FIFO4_DB3	**DB3 The forth byte to be loaded into or unloaded from the FIFO.**

A1060240 USB_CON USB PHY control 00000020

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											NULLPKT_FIX				DMPULLUP	DPPULLUP
Type											RW				RW	RW
Reset											1				0	0

Bit(s)	Name	Description
5	NULLPKT_FIX	**If NULLPKT_FIX is setting as 1, USB controller will not issue a DMAreq when receive a null packet**
1	DMPULLUP	**Pull up enable pin. Enable the pull up 1.5KOhm pull up on D pin as a full speed device by setting it to high**
0	DPPULLUP	**Pull up enable pin. Enable the pull up 1.5KOhm pull up on D+ pin as a full speed device by setting it to high**

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20. Serial Peripheral Interface Master Controller

The Serial Peripheral Interface (SPI) is a bit-serial transmission protocol and supports single mode (four-pin), dual mode (four-pin) and quad mode (six-pin) for increased data throughput. The maximum serial clock (SCK) frequency is 52MHz. Note, that single mode can support full duplex, but dual quad mode only supports half-duplex. Figure 19.5-1 is an example of the connection between the SPI master and SPI slave. The SPI controller is a master responsible for data transmission with slave.

Figure 19.5-1. Pin connection between SPI master and SPI slave

Table 19.5-1. SPI master controller interface

Signal name	Type	Default value	Description
CS	O	1 (output)	Low active chip selection signal
SCK	O	0 (output)	The (bit) serial clock. Maximum SCK clock rate is 52MHz.
MOSI	I/O	1 (output)	Data signal 0
MISO	I/O	Pull down (input)	Data signal 1
SIO2	I/O	1 (output)	Data signal 2
SIO3	I/O	1 (output)	Data signal 3

20.1. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 20.1-2. Abbreviations

Abbreviation	Definition
MOSI	Master out slave in
MISO	Master in slave out
CPOL	Clock polarity
CPHA	Clock phase
SIO_oe	Output enable; set direction of GPIO PinMux

20.2. Features

- The SPI master controller supports single mode (four-pin), dual mode (four-pin) and quad mode (six-pin). The controller can automatically set port direction for data input/output, if registers `SPIM_TYPE` and `SPIM_RW_MODE` are already set.

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- The SCK frequency supports maximum 52MHz with CPOL and CPHA features and can be configured as 104/N MHz (where N is from 2 to 2^{17}) for different applications. CPOL defines the clock polarity in the transmission. CPHA defines the legal timing to sample data. The chip select (CS) signal setup time, hold time and idle time can be configured, too. The detailed timing diagram of the SCK and CS signals is shown in Figure 20.2-1.

- There are two configurable modes for the source of the transfer data:
  - DMA mode. The SPI master controller includes the DMA design, it can automatically read or write data from memory continuously;
  - Direct mode. The CPU directly reads data from the SPI master controller FIFO or writes data to the SPI master controller FIFO. In DMA mode, the endian order of memory data is adjustable.

Figure 20.2-1. SPI transmission formats

- Unlimited length for transmission can be achieved in Pause mode. In Pause mode, the CS signal will stay active (low) after the transmission. During this period, the SPI controller will be in **PAUSE_IDLE** state, ready to receive the resume command. Figure 20.2-2 is the state transition diagram.

Figure 20.2-2. Operation flow with or without PAUSE mode

- A configurable option to control CS de-assertion between byte transfers is available. The SPI master controller supports a special transmission format called CS de-assert mode. Figure 20.2-3 illustrates the waveform in this transmission format.

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Figure 20.2-3. CS de-assert mode

- When the SPI master controller operates in dual or quad mode, the transmission package includes three parts: command phase, dummy phase and data phase.
  - Command phase always operates at Single mode;
  - Dummy phase cannot transmit or receive data;
  - Data phase operation depends on **SPIM_TYPE** and **SPIM_RW_MODE** settings. The Command phase and Dummy phase are useful for special applications, such as read or write serial flash data.
- For high-speed transmission, the SPI master controller can enable the delay sample feature (registers **SPIM_GET_DLY** and **SAMPLE_SEL**) to resolve data path latency issues. The critical path of SPI transmission includes two parts:
  - Master transmits SCK signal to slave;
  - Slave feeds back SIO data to master. Each interval of sample delay is 9.615 ns, and **SAMPLE_SEL** defines the trigger edge of sample clock, in other words, 0 - positive edge sample data; 1 - negative edge sample data. The detailed description is shown in Figure 20.2-4.

  If the timing skew between SCK and MOSI (MISO) result in slave sampling failure, the SPI master controller can enable the delay feature (registers **SPIM_SEL_ADDR** and **SPIM_SEL_WDATA**) to resolve data path timing skew issues. The detailed description is shown in Figure 20.2-4.
  - If the latency of MOSI is worse than SCK, the received data on slave will be corrupted.
  - The SPI master can enable delay feature for SCK so that the slave can sample the data in time.
  - This example is for SCK. Any other SPI interface port, including SCK, MOSI and MISO, have similar behavior.

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Figure 20.2-4. SPI master controller delay sample

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20.3. Block diagram

Figure 20.3-1. Block diagram of SPI master controller

20.4. Functions

- SPI master single mode. Typical SPI transmission mode is single SPI, a 4-pin protocol. Set the register **SPIM_TYPE** to 0 to enter single mode. In this mode, the register settings for **SPIM_RW_MODE**, **SPIM_DUMMY_CNT** and **SPIM_COMMAND_CNT** are not supported. Set the register SPIM_TXMSBF to 1 to enable "TX data is MSB first" mode. Also, set the register **SPIM_RXMSBF** to 1 to enable "RX data is MSB first" mode. The default value of **SPIM_TXMSBF** and **SPIM_RXMSBF** is 0. The single mode data transmission diagram is shown in Figure 20.4-1.

Figure 20.4-1. SPI master single mode

- SPI master dual mode. The dual mode SPI is also a 4-pin protocol. Set the register **SPIM_TYPE** to 1 to enter this mode. In dual mode, the SPI master controller only supports half duplex, and the data transmission direction is configured by register **SPIM_RW_MODE** (0: read data, 1: write data). The registers **SPIM_DUMMY_CNT**, **SPIM_COMMAND_CNT** can be activated with user configuration. In addition, **SPIM_DUMMY_CNT** and **SPIM_COMMAND_CNT** can be set to 0 to disable these features. Set the register **SPIM_TXMSBF** to 1 to enable "TX data is MSB first" mode. Also, set the register **SPIM_RXMSBF** to 1 to enable "RX data is MSB first" mode. The default value of SPIM_TXMSBF and **SPIM_RXMSBF** is 0. The dual mode data transmission diagram is shown in Figure 20.4-2, Figure 20.4-3.

Figure 20.4-2. SPI master dual mode write data

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Figure 20.4-3. SPI master dual mode read data

- SPI master quad mode. The quad mode SPI is a 6-pin protocol. Set the register **SPIM_TYPE** to 2 to enter this mode. Similar to dual mode, in quad mode, the SPI master controller only supports half duplex, and the data transmission direction is configured by register **SPIM_RW_MODE** (0: read data, 1: write data). The registers **SPIM_DUMMY_CNT**, **SPIM_COMMAND_CNT** can also be activated. Set the register **SPIM_TXMSBF** to 1 to enable "TX data is MSB first" mode. Also, set the register **SPIM_RXMSBF** to 1 to enable "RX data is MSB first" mode. The default value of **SPIM_TXMSBF** and **SPIM_RXMSBF** is 0. The quad mode data transmission diagram is shown in Figure 20.4-4 and Figure 20.4-5.

Figure 20.4-4. SPI master quad mode write data

Figure 20.4-5. SPI master quad mode read data

20.5. Register mapping

There are two SPI_MASTER channels in this SoC. The register definitions are the same except for the module base address.

SPI_MASTER number	Base address
SPI_MASTER_0	0xA0090000
SPI_MASTER_1	0xA00A0000

Module name: SPI_MASTER_0 Base address: (+a0090000h)

Address	Name	Width (bits)	Register Function

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Address	Name	Width (bits)	Register Function
A0090000	SPIMST_CTRL0	32	SPI Master Control 0 Register
A0090004	SPIMST_CTRL1	32	SPI Master Control 1 Register
A0090008	SPIMST_TRIG	32	SPI Master Trigger Register
A009000C	SPIMST_IE	32	SPI Master Interrupt Enable
A0090010	SPIMST_INT	32	SPI Master Interrupt
A0090014	SPIMST_STA	32	SPI Master Status
A0090018	SPIMST_TX_DATA	32	SPI Master TX Data
A009001C	SPIMST_RX_DATA	32	SPI Master RX Data
A0090020	SPIMST_TX_SRC	32	SPI Master TX Source Address Register
A0090024	SPIMST_RX_DST	32	SPI Master RX Destination Address Register
A0090028	SPIMST_CFG0	32	SPI Master Configuration 0 Register
A009002C	SPIMST_CFG1	32	SPI Master Configuration 1 Register
A0090030	SPIMST_CFG2	32	SPI Master Configuration 2 Register
A0090034	SPIMST_CFG3	32	SPI Master Configuration 3 Register
A0090038	SPIMST_CFG4	32	SPI Master Configuration 4 Register

A0090000 SPIMST_CTRL0 SPI Master Control 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SPIM_PAUSE_EN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SPIM_DEASSERT_EN		SPIM_CTRL0						
Type								RW		RW						
Reset								0		0	0	0	0	0	0	0

Bit(s)	Name	Description
16	SPIM_PAUSE_EN	**Pause mode enable** Set the pause mode bit to 1 to enable this mode.
8	SPIM_DEASSERT_EN	**De-assert mode enable** Enable bit of the chip select de-assertion mode. Set it to 1 to enable this mode.
6:0	SPIM_CTRL0	**SPI master general configure set 0** • [6]: SPIM_RW_MODE, indicates SPI master received/sent data, only used in Dual/Quad SPI (SPIM_TYPE = 1 or 2). o 0: Read mode, SPI master receive data

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		o 1: Write mode, SPI master send data • [5:4]: SPIM_TYPE, indicates the SPI data transmission type o 0: Single SPI o 1: Dual SPI o 2: Quad SPI o 3: Not used • [3]: RXMSBF, indicates the RX data received is MSB first. Set RXMSBF to 1 for MSB first, otherwise set it to 0. • [2]: TXMSBF, indicates the TX data sent is MSB first or not. Set TXMSBF to 1 for MSB first, otherwise set it to 0. • [1]: CPOL, control bit of the SCK polarity. o 0: CPOL = 0 o 1: CPOL = 1 • [0]: CPHA, control bit of the SCK sample data phase. o 0: CPHA = 0 o 1: CPHA = 1

A0090004 SPIMST_CTRL1 SPI Master Control 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								SPIM_RXDMA_EN								SPIM_TXDMA_EN
Type								RW								RW
Reset								0								0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name						SPIM_GET_DLY							SPIM_CTRL1			
Type						RW							RW			
Reset						0	0	0					0	0	0	0

Bit(s)	Name	Description
24	SPIM_RXDMA_EN	**RX DMA enable** DMA mode enable bit of the data being received. Default (0) is not to enable.
16	SPIM_TXDMA_EN	**TX DMA enable** DMA mode enable bit of the data to be transmitted. Default (0) is not to enable.
10:8	SPIM_GET_DLY	**Receive data get delay** If the latency of the signal that SPI master received is too large, the register can help to tolerate get_tick timing. The timing is CLK_PERIOD (9.615 ns) * SPIM_GET_DLY.
3:0	SPIM_CTRL1	**SPI master general configure set 1** • [3]: RX_ENDIAN, defines whether to reverse the endian order of the data DMA to memory. Default (0) is not to reverse. o 0: RX data format is data[31:0] o 1: RX data format is {data[7:0], data[15:8], data[23:16], data[31:24]}

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		• [2]: TX_ENDIAN, defines whether to reverse the endian order of the data DMA from memory. Default (0) is not to reverse. o 0: TX data format is data[31:0] o 1: TX data format is {data[7:0], data[15:8], data[23:16], data[31:24]} • [1]: CS_POL, control bit of chip select polarity o 0: Active low o 1: Active high • [0]: SAMPLE_SEL, control bit of sample edge of RX data o 0: Positive edge o 1: Negative edge

A0090008 SPIMST_TRIG SPI Master Trigger Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SPIM_RST
Type																WO
Reset																0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name								SPIM_RESUME								SPIM_CMD_ACT
Type								WO								WO
Reset								0								0

Bit(s)	Name	Description
16	SPIM_RST	**Reset** Software reset bit; resets the state machine and data FIFO of SPI master controller (not the register value). When this bit is 1, software reset is active high and hardware can automatically return to 0. The default value is 0.
8	SPIM_RESUME	**Resume** This bit is used when the controller is in PAUSE IDLE state. Write 1 to this bit to trigger the SPI controller resume transfer from PAUSE IDLE state.
0	SPIM_CMD_ACT	**Command activate** Write 1 to this bit to trigger the SPI master controller to start the transmission.

A009000C SPIMST_IE SPI Master Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Rese																

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t																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**SPIM_IE**	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPIM_IE	**SPI master interrupt source enable** [1]: PAUSE_IE, interrupt enable bit of pause flag in SPI status register. [0]: FINISH_IE, interrupt enable bit of finish flag in SPI status register.

A0090010 SPIMST_INT SPI Master Interrupt 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															**SPIM_INT**	
Type															RC	
Reset															0	0

Bit(s)	Name	Description
1:0	SPIM_INT	**SPI master interrupt source** • [1]: PAUSE_INT, interrupt status bit in pause mode. It will be set by the SPI controller when it completes the transaction, entering the PAUSE IDLE state. • [0]: FINISH_INT, interrupt status bit in non-pause mode. It will be set by the SPI controller when it completes the transaction, entering the IDLE state.

A0090014 SPIMST_STA SPI Master Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SPIM_BUSY**
Type																RO
Reset																0

Bit(s)	Name	Description

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0	SPIM_BUSY	**SPI master status** This status flag reflects whether the SPI controller is busy. This bit is high active, i.e. 1 represents the SPI controller is currently busy. The state diagram is shown in Figure 20.2-2. Operation flow with or without PAUSE modeFigure 20.2-2. • 1'b1: busy • 1'b0: idle

A0090018 SPIMST_TX_DATA SPI Master TX Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIM_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIM_TX_DATA															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIM_TX_DATA	**TX data** The depth of the TX FIFO is 32 bytes. Write to this register to write 4 bytes into TX FIFO. The TX FIFO pointer will automatically move toward the next four bytes.

A009001C SPIMST_RX_DATA SPI Master RX Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIM_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIM_RX_DATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIM_RX_DATA	**RX data** The depth of the RX FIFO is 32 bytes. Read from this register to read 4 bytes from the RX FIFO. The RX FIFO pointer will automatically move toward the next four bytes.

A0090020 SPIMST_TX_SRC SPI Master TX Source Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIM_TX_SRC															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPIM_TX_SRC**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIM_TX_SRC	**TX data source address** SPIM_TX_SRC defines the memory address from which the SPI controller reads transmitted data. The address must be aligned with the word boundary. Note 1, if trying to access from unaligned memory address, the request will cause RAM to do two operations. As a result, the relatively slow memory access will become even slower. Note 2, the SPI master can access serial flash, EMI/PSRAM and SYSRAM in MT2625.

A0090024 SPIMST_RX_DST SPI Master RX Destination Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPIM_RX_DST**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPIM_RX_DST**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIM_RX_DST	**RX data destination address** SPI_RX_DST defines the memory address to which the SPI controller stores data. The address must be aligned with the word boundary. Note 1, if trying to access from unaligned memory address, the request will cause RAM to do two operations. As a result, the relatively slow memory access will become even slower. Note 2, the SPI master can access serial flash, EMI/PSRAM and SYSRAM in MT2625.

A0090028 SPIMST_CFG0 SPI Master Configuration 0 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPIM_CS_SETUP_CNT**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPIM_CS_HOLD_CNT**															
Type	RW															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SPIM_CS_SETUP_CNT	**Chip select setup time** Setup time = (SPIM_CS_SETUP_CNT+1) * CLK_PERIOD, where CLK_PERIOD (9.615 ns) is the cycle time of the clock the SPI engine adopts.
15:0	SPIM_CS_HOLD_CNT	**Chip select hold time** Hold time = (SPIM_CS_HOLD_COUNT+1) * CLK_PERIOD, where CLK_PERIOD (9.615 ns) is the cycle time of the clock the SPI engine adopts.

A009002C SPIMST_CFG1 SPI Master Configuration 1 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIM_SCK_LOW_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIM_SCK_HIGH_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SPIM_SCK_LOW_CNT	**SPI master clock low time** SCK low time = (SPIM_SCK_LOW_CNT+1) * CLK_PERIOD (9.615ns)
15:0	SPIM_SCK_HIGH_CNT	**SPI master clock high time** SCK high time = (SPIM_SCK_HIGH_CNT+1) * CLK_PERIOD (9.615ns)

A0090030 SPIMST_CFG2 SPI Master Configuration 2 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIM_PACKET_LENGTH_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIM_PACKET_LOOP_CNT								SPIM_CS_IDLE_CNT							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SPIM_PACKET_LENGTH_CNT	**Transmission package length** The number of bytes in one packet = PACKET_LENGTH_CNT + 1. Total number bytes of one transmission = (PACKET_LENGTH_CNT+1) * (PACKET_LOOP_CNT+1).

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15:8	SPIM_PACKET_LOOP_CNT	**Transmission loop times** The number of packets in one transmission = PACKET_LOOP_CNT + 1.
7:0	SPIM_CS_IDLE_CNT	**Chip select idle time** This setting is for CS de-assertion mode. It indicate that the time between two transmissions = (CS_HOLD_COUNT+1) * CLK_PERIOD.

A0090034 SPIMST_CFG3 SPI Master Configuration 3 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SPIM_DUMMY_CNT								SPIM_COMMAND_CNT			
Type					RW								RW			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	SPIM_DUMMY_CNT	**Dummy count** The number of dummy bits in one packet. Dummy phase is the second transmission of packet between command phase and data phase. Dummy phase cannot transmit or receive data, it is only used in Dual/Quad SPI (SPIM_TYPE = 1 or 2).
3:0	SPIM_COMMAND_CNT	**Command count** The number of command bytes in one packet. Command phase is the first transmission of packet before dummy phase and data phase. The command phase is used in Dual/Quad SPI (SPIM_TYPE = 1 or 2).

A0090038 SPIMST_CFG4 SPI Master Configuration 4 Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SPIM_SEL_RDATA		
Type														RO		
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						SPIM_SEL_WDATA							SPIM_SEL_ADDR			
Type						WO							RW			
Reset						0	0	0					0	0	0	0

Bit(s)	Name	Description
18:16	SPIM_SEL_RDATA	**SPI master selection read data** Read SPI master data of corresponding address

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Bit(s)	Name	Description
		(SPIM_SEL_ADDR)
10:8	SPIM_SEL_WDATA	**SPI master selection write data** Write SPI master data of corresponding address (SPIM_SEL_ADDR)
3:0	SPIM_SEL_ADDR	**SPI master selection address** 0: Configure SPI master MOSI0 delay 1: Configure SPI master MOSI1 delay 2: Configure SPI master MOSI2 delay 3: Configure SPI master MOSI3 delay 4: Configure SPI master MISO0 delay 5: Configure SPI master MISO1 delay 6: Configure SPI master MISO2 delay 7: Configure SPI master MISO3 delay 8: Configure SPI master SCK delay 9: Configure SPI master device. This register can enable the selected device only that's connected to the SPI master.

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21. Serial Peripheral Interface Slave Controller

The Serial Peripheral Interface (SPI) is a bit-serial transmission protocol and supports single mode (four-pin), dual mode (four-pin) and quad mode (six-pin) to increase data throughput. The maximum serial clock (SCK) frequency is 52MHz. Figure 20.5-1 is an example of the connection between the SPI master and SPI slave. The SPI controller is a slave responsible for data transmission with master.

Figure 20.5-1. Pin connection between SPI master and SPI slave

Table 20.5-1. SPI slave controller interface

Signal name	Type	Default value	Description
CS	I	Pull up (input)	Low active chip selection signal
SCK	I	Pull down (input)	The (bit) serial clock. Maximum SCK clock rate is 52MHz.
MOSI	I/O	Pull down (input)	Data signal 0
MISO	I/O	0 (output)	Data signal 1
SIO2	I/O	Pull down (input)	Data signal 2
SIO3	I/O	Pull down (input)	Data signal 3

21.1. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 21.1-1. Abbreviations

Abbreviation	Definition
MOSI	Master out slave in
MISO	Master in slave out
CPOL	Clock polarity
CPHA	Clock phase
`SIO_oe` (see Figure 21.3-1)	Output enable; sets direction of GPIO PinMux

21.2. Features

- The SPI slave controller supports single mode (four-pin), dual mode (four-pin) and quad mode (six-pin). The controller can automatically set port direction for data input/output if register **SPIM_TYPE** is set.
- Each databyte transmit and receive sequence can be configured separately with registers **TXMSBF** and **RXMSBF**.

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- The memory address of the SPI slave controller's internal DMA read/write data is configured by two methods: SPI master command (hardware) configure and software configure.
  - When register **SPIS_DEC_ADDR_EN** is 0, enable hardware configuration feature. The address of DMA read/write is the SPI master CR/CW configuration address and **SPISLV_BUFFER_BASE_ADDR**. For example, if the SPI master CR address is `0x1000` and **SPISLV_BUFFER_BASE_ADDR** is `0x2500`, the address of DMA read/write will be `0x3500`.
  - When register **SPIS_DEC_ADDR_EN** is 1, enable software configuration feature. The SPI master DMA reads and writes data from the address **SPISLV_BUFFER_BASE_ADDR**.
- The serial clock frequency supports maximum of 52MHz with CPOL and CPHA features. CPOL defines the clock polarity in the transmission. CPHA defines the legal timing to sample data. The detailed timing diagram of the SCK and CS signal is shown in Figure 21.2-1.

Figure 21.2-1. SPI transmission formats

- For high-speed transmission, the SPI slave controller can enable early transmission feature (register) to resolve data path latency issue. The detailed description is shown in Figure 21.2-2.

Figure 21.2-2. SPI slave controller early transmit

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21.3. Block diagram

Figure 21.3-1. Block diagram of SPI slave controller

- The SPI slave controller accesses memory through the AHB interface and the CPU can access the SPI slave controller through the APB interface.
- The SPI slave controller has an internal direct memory access (DMA) engine to access memory and FIFO to store data during transmission.
- The SPI slave controller can set the direction (in or out) of GPIO PinMux by SIO_oe (defined by SPIM_TYPE).

21.4. Functions

The SPI slave controller has nine commands that can be configured by the SPI master transmit data, the command set is shown in Table 21.4-1 and the command format is shown in

Figure ***21.4-1*** and Figure 21.4-2.

Table 21.4-1. SPI slave controller interface

Command field [7:0]	CMD default code	Data field length	Description
Power Off (PWOFF)	8'h02	0 byte	Master uses this configure command so that the MCU turns off the SPI slave controller.
Power On (PWON)	8'h04	0 byte	Master uses this configuration command to wake up the system and notify the MCU to turn on the SPI slave controller.
Read Status (RS)	8'h06	1 byte (SPI slave feedback)	Master reads the Slave status register.
Write Status (WS)	8'h08	1 byte	Master writes into the Slave status register to clean the error bit, such as write 1 to clear.
Config Read (CR)	8'h0a	SIZE_OF_ADDR • 1: 4 bytes address, 4 bytes data length.	Master configures the SPI Slave to read data.

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Command field [7:0]	CMD default code	Data field length	Description
		• 0: 2 bytes address, 2 bytes data length.	
Config Write (CW)	8'h0c	SIZE_OF_ADDR • 1: 4 bytes address, 4 bytes data length. • 0: 2 bytes address, 2 bytes data length.	Master configures the SPI Slave to write data.
Read Data (RD)	8'h81	N bytes. Burst data payload.	Master reads data.
Write Data (WD)	8'h0e	N bytes. Burst data payload.	Master writes data.
Config Type (CT)	8'h10	1 byte: • [7:3] Not used • [2] SIZE_OF_ADDR • [1:0] SPIS_TYPE	Master configures the SPI Slave type.

Figure 21.4-1. SPI slave controller commands waveform

Figure 21.4-2. Config read/write (CR/CW) command format

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21.4.1. SPI slave control flow

The SPI slave control flow is shown in Figure 21.4-3. First, the SPI master sends a “power on” command to turn on the SPI slave controller then transmits a “config read/write” command to configure the transfer data length and read/write address of the memory. After the SPI slave is configured, it can send/receive data package with SPI master by the “read/write data” command. Last, use the “power off” command to turn off the SPI slave controller. In each state, the SPI master transmits the “read status” command to poll SPI slave status. If the SPI master detects an error state flag bit, it should send a “write status” command to clear the bit and poll this bit until it turns low. The SPI master can transmit a “config type” command to configure data transmission type (Single, Dual, or Quad mode) according to user requirements. The SPI slave control flow is shown in Table 21.4-2.

Figure 21.4-3. SPI slave control flow diagram

Table 21.4-2. SPI slave status description (use RS command to poll SPI slave status)

Function	Bit	Usage (status[bit] = function)
SLV_ON	0	Master polls this bit until slave is on after sending POWERON CMD or off after sending POWEROFF CMD.
SR_CFG_SUCCESS	1	Master checks this bit for the configure write or read CW/CR command status.
SR_TXRX_FIFO_RDY	2	Set this bit when the slave is ready to send/receive data (master can send RD/WD command). Clean the bit after SPI slave receives a CR/CW command.

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Function	Bit	Usage (status[bit] = function)
SR_RD_ERR	3	After a read command, master can read this bit to check for an error in the read transfer. If there is an error, the master should send WS command to clear this bit and poll this bit until it is 0.
SR_WR_ERR	4	After a WD command, master can read this bit to check for an error in the write transfer. If there is an error, the master should send WS command to clear this bit and poll this bit until it is 0.
SR_RDWR_FINISH	5	After RD/WD transaction, master can poll this bit to check if read/write transfer is finished. Clean the bit after the SPI slave receives a CR/CW command.
SR_TIMOUT_ERR	6	A timeout error occurs in the following condition: 1. After the previous successful configure command, the SPI slave did not receive RD/WR command. 2. The period exceeds the timeout threshold value. The SPI master should send a WS command to clear this bit and poll this bit until it is 0.
SR_CMD_ERR	7	If master sends an error command in the first byte, master detects the error status through the received data. Clean it after the SPI slave receives a correct command.

21.4.2. SPI slave modes

6) SPI slave single mode.

A typical SPI transmission mode is single SPI, it is a 4-pin protocol. Set the register **SPIS_TYPE** to 0 to enter single mode. Set the register **SPIM_TXMSBF** to 1 to enable "TX data is MSB first" mode. Also, set the register **SPIM_RXMSBF** to 1 to enable "RX data is MSB first" mode. The default value of **SPIM_TXMSBF** and **SPIM_RXMSBF** is 0. Single mode data transmission diagrams are shown in Figure 21.4-4 and Figure 21.4-5.

Figure 21.4-4. SPI slave single mode write data

Figure 21.4-5. SPI slave single mode read data

7) SPI slave dual mode.

The dual mode SPI is also a 4-pin protocol. Set the register **SPIS_TYPE** to 1 to enter this mode. Set the register **SPIM_TXMSBF** to 1 to enable "TX data is MSB first" mode. Also, set the register **SPIM_RXMSBF** to 1 to enable "RX data is MSB first" mode. The default value of **SPIM_TXMSBF** and **SPIM_RXMSBF** is 0. The dual mode data transmission diagrams are shown in Figure 21.4-6 and Figure 21.4-7.

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Figure 21.4-6. SPI slave dual mode write data

Figure 21.4-7. SPI slave dual mode read data

8) SPI slave quad mode.

The quad mode SPI is a 6-pin protocol. Set the register **SPIS_TYPE** to 2 to enter this mode. Set the register **SPIM_TXMSBF** to 1 to enable "TX data is MSB first" mode. Also, set the register **SPIM_RXMSBF** to 1 to enable "RX data is MSB first" mode. The default value of **SPIM_TXMSBF** and **SPIM_RXMSBF** are 0. The quad mode transmission diagrams are shown in Figure 21.4-8 and Figure 21.4-9.

Figure 21.4-8. SPI slave quad mode write data

Figure 21.4-9. SPI slave quad mode read data

21.5. Registers

Module name: SPI_SLAVE Base address: (+a00b0000h)

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Address	Name	Width (bits)	Register Function
A00B0000	SPISLV_CTRL	32	SPI Slave Control Register
A00B0004	SPISLV_TRIG	32	SPI Slave Trigger Register
A00B0008	SPISLV_IE	32	SPI Slave Interrupt Enable
A00B000C	SPISLV_INT	32	SPI Slave Interrupt
A00B0010	SPISLV_STA	32	SPI Slave Status
A00B0014	SPISLV_TRANS_LENGTH	32	SPI Slave Transfer Length Register
A00B0018	SPISLV_TRANS_ADDR	32	SPI Slave Transfer Address Register
A00B001C	SPISLV_TMOUT_THR	32	SPI Slave Timeout Threshold Register
A00B0020	SPISLV_BUFFER_BASE_ADDR	32	SPI Slave Buffer Base Address Register
A00B0024	SPISLV_BUFFER_SIZE	32	SPI Slave Buffer Size Register
A00B0028	SPISLV_CMD_RECEIVED	32	SPI Slave Command Received

Module name: SPI_SLAVE_PAD Base address: (+a20e0000h)

Address	Name	Width (bits)	Register Function
A20E0000	SPISLV_PAD_DUMMY_CNT	32	SPI Slave Pad Dummy Count
A20E0004	SPISLV_PAD_CMD_DEF0	32	SPI Slave Pad Command Define 0
A20E0008	SPISLV_PAD_CMD_DEF1	32	SPI Slave Pad Command Define 1
A20E000C	SPISLV_PAD_CMD_DEF2	32	SPI Slave Pad Command Define 2
A20E0010	SPISLV_PAD_DLYSEL0	32	SPI Slave Pad Delay Select 0 Register
A20E0014	SPISLV_PAD_DLYSEL1	32	SPI Slave Pad Delay Select 1 Register
A20E0018	SPISLV_PAD_DLYSEL2	32	SPI Slave Pad Delay Select 2 Register

A00B0000 SPISLV_CTRL SPI Slave Control Register 00000100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SPIS_MISO_EARLY_TRANS
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SPIS_CTRL1			SPIS_CTRL0						
Type							RW			RW						

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Reset							0	1		0	0	0	0	0	0	0

Bit(s)	Name	Description
16	SPIS_MISO_EARLY_TRANS	**Early transmit data** Defines whether to transmit data half SCK cycle early. It is used to improve the SPI timing.
9:8	SPIS_CTRL1	**SPI slave general configuration setting 1** • [1]: SPIS_DEC_ADDR_EN, indicates whether software decode address is sent by the SPI master. o 0: software will not decode the address. The address of read/write memory is set by master configure read/write command. o 1: software will decode the address of read/write memory. • [0]: SPIS_SW_RDY_EN, if the value is 1, defines whether hardware automatically sets the register SPIS_TXDMA_SW_RDY or SPIS_RXDMA_SW_RDY.
6:0	SPIS_CTRL0	**SPI slave general configuration setting 0** • [6]: SIZE_OF_ADDR, defines CW/CR command format, can be configured by master command or slave software settings. o 0: Data filed includes 2 bytes of transfer address and 2 bytes of transfer length. o 1: Data filed includes 4 bytes of transfer address and 4 bytes of transfer length. • [5:4]: SPIS_TYPE, indicates the SPI data transmission type, can be configured by master command or software settings. o 0: Single SPI o 1: Dual SPI o 2: Quad SPI o 3: Not used • [3]: RXMSBF, indicates whether the first byte of the received RX data received is MSB. Set RXMSBF to 1 to define the first byte as MSB, otherwise set it to 0. • [2]: TXMSBF, indicates the first byte of the transmitted TX data is MSB. Set TXMSBF to 1 to define the first byte as MSB, otherwise set it to 0. • [1]: CPOL, control bit of the SCK polarity. o 0: CPOL = 0 o 1: CPOL = 1 • [0]: CPHA, control bit of the SCK sample data phase o 0: CPHA = 0 o 1: CPHA = 1

A00B0004 SPISLV_TRIG SPI Slave Trigger Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								**SPIS_RXDMA_SW_RDY**								**SPIS_TXDMA_SW_RDY**
Type								WO								WO

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Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**SPIS_SW_RST**								**SPIS_SW_ON**
Type								WO								WO
Reset								0								0

Bit(s)	Name	Description
24	SPIS_RXDMA_SW_RDY	**Software ready to receive data** Write 1 to this bit to indicate the SPI slave can receive RX data. TXRX_FIFO_RDY of the status of STA register will be set. And master can query the status to check whether the slave is ready to receive data.
16	SPIS_TXDMA_SW_RDY	**Software ready to transmit data** Write 1 to this bit to indicate the SPI slave can transmit TX data. TXRX_FIFO_RDY of STA register status will be set. And the master can query the status to check whether the slave is ready to transmit data.
8	SPIS_SW_RST	**Software reset** Software reset bit; resets the state machine and data FIFO of SPI slave controller (not the register define). When this bit is 1, software reset is active high, and hardware can automatically recover to 0. The default value is 0.
0	SPIS_SW_ON	**Software ON** The SPI slave controller is enabled by software, the slave software can set SR_SLV_ON by SPIS_SW_ON control.

A00B0008 SPISLV_IE **SPI Slave Interrupt Enable** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**SPIS_IE**								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	SPIS_IE	**SPI slave interrupt source enable** [8]: TMOUT_ERR_IE, interrupt enable bit of timeout error [7]: WR_DATA_ERR_IE, interrupt enable bit of SPI master write data error [6]: RD_DATA_ERR_IE, interrupt enable bit of SPI master read data error [5]: POWER_ON_IE, interrupt enable bit of SPI slave receive power-on command [4]: POWER_OFF_IE, interrupt enable bit of SPI slave receive power-off [3]: WR_TRANS_FINISH_IE, interrupt enable bit of SPI master write data finish [2]: RD_TRANS_FINISH_IE, interrupt enable bit of SPI master read data finish [1]: WR_CFG_FINISH_IE, interrupt enable bit of SPI master configure write finish [0]: RD_CFG_FINISH_IE, interrupt enable bit of SPI master configure read finish

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A00B000C SPISLV_INT **SPI Slave Interrupt** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SPIS_INT								
Type								RC								
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
8:0	SPIS_INT	**SPI slave interrupt source** [8]: TMOUT_ERR_INT, timeout error interrupt [7]: WR_DATA_ERR_INT, SPI master write data error interrupt [6]: RD_DATA_ERR_INT, SPI master read data error interrupt [5]: POWER_ON_INT, SPI slave receive power-on command interrupt [4]: POWER_OFF_INT, SPI slave receive power-off command interrupt [3]: WR_TRANS_FINISH_INT, SPI master write data finish interrupt [2]: RD_TRANS_FINISH_INT, SPI master read data finish interrupt [1]: WR_CFG_FINISH_INT, SPI master configure write finish interrupt [0]: RD_CFG_FINISH_INT, SPI master configure read finish interrupt

A00B0010 SPISLV_STA **SPI Slave Status** **00040000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														SPIS_AHB_STA		
Type														RO		
Reset														1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			SPIS_STA													
Type			RO													
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18:16	SPIS_AHB_STA	**SPI slave AHB status** [18:17]: AHB_STATUS 0: BUST transfer 1: SINGLE WORD transfer 2: IDLE 3: SINGLE BYTE transfer [16]: AHB_DIR 0: DMA read memory 1: DMA write memory

13:0	SPIS_STA	**SPI slave status**
		• SPIS_STA[7:0] is the feedback data when SPI master sends read status command
		  o [13]: SR_POWER_ON
		  SPI slave receives power-on command.

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Cleared after SPIS_SW_ON is set to 1.

- [12]: SR_POWER_OFF
  SPI slave receives power-off command.
  Cleared after SPIS_SW_ON is set to 0.
- [11]: SR_WR_FINISH
  SPI master write data finish.
  Cleared after the next configure write or read (CW/CR) command.
- [10]: SR_RD_FINISH
  SPI master read data finish.
  Cleared after the next CW/CR command.
- [9]: SR_CFG_WRITE_FINISH
  SPI slave receive CW command is complete.
  Cleared after the next CW/CR command.
- [8]: SR_CFG_READ_FINISH
  SPI slave receive CR command is finished.
  Cleared after the next CW/CR command.
- [7]: SR_CMD_ERROR
  Used for SPI master to debug.
  Cleared after SPI master sends a correct command.
- [6]: SR_TIMOUT_ERR

- The time out error occurs in the following condition : 1. After the previous configure command success, the SPI slave did not receive RD/WR command. 2. The period exceeds the timeout threshold value.If there is an error, master must send WS command to clear this bit and poll this bit until it is 0.
  - [5]: SR_RDWR_FINISH
    The bit is set to 1 when SPI slave receives or sends all data.
    Cleared after SPI slave receives CR/CW command.
  - [4]: SR_WR_ERR
    After a WR command, master can read this bit to check for an error in the write transfer through RS command.
    If there is an error, master must send WS command to clear this bit and poll this bit until it is 0.
  - [3]: SR_RD_ERR
    After an RD command, master can read this bit to check for an error in the read transfer through RS.
    If there is timeout error, master must send WS command to clear this bit and poll this bit until it is 0.
  - [2]: SR_TXRX_FIFO_RDY
    When CR, this bit indicates whether TX FIFO is ready. Master polls this bit to know if the slave is ready to send data, then master can send the RD command.
- When CW, this bit indicates whether RX FIFO is ready. Master polls this bit to know if the slave is ready to send data, then master can send WD command.
  This bit will be cleared after SPI slave receives CR/CW command.
  - [1]: SR_CFG_SUCESS
    SPI master configure package address/length successfully.
  - [0]: SR_SLV_ON
- Enable SPI slave controller by setting SPIS_SW_ON = 1. After SPI slave receives POWER-ON command, slave software can set this bit by controlling SPIS_SW_ON.

A00B0014 SPISLV_TRANS_LENGTH SPI Slave Transfer Length Register 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIS_TRANS_LENGTH															

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Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPIS_TRANS_LENGTH**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	SPIS_TRANS_LENGTH	**Transfer length** Defines the SPI master transfer package length in bytes.

A00B0018 SPISLV_TRANS_ADDR SPI Slave Transfer Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPIS_TRANS_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPIS_TRANS_ADDR**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIS_TRANS_ADDR	**Transfer address** Defines the SPI master transfer package start address.

A00B001C SPISLV_TMOUT_THR SPI Slave Timeout Threshold Register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SPIS_TMOUT_THR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SPIS_TMOUT_THR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	SPIS_TMOUT_THR	**Timeout threshold time** The time out error occurs in the following condition : 1. After the previous configure command success, the SPI slave did not receive RD/WR command. 2. The period exceeds the timeout threshold value. The timeout counter unit is 3.05μs.

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A00B0020 SPISLV_BUFFER_BASE_ADDR SPI Slave Buffer Base Address Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIS_BUFFER_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIS_BUFFER_BASE_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIS_BUFFER_BASE_ADDR	**Buffer base address** Configurable DMA address to access memory. The address must be aligned with the word boundary. If trying to access from unaligned memory address, the request will cause RAM to do two operations. As a result, the relatively slow memory access will become even slower.

A00B0024 SPISLV_BUFFER_SIZE SPI Slave Buffer Size Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIS_BUFFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIS_BUFFER_SIZE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SPIS_BUFFER_SIZE	**Buffer base size** Configurable buffer size indicating whether SPI master is configured successfully.

A00B0028 SPISLV_CMD_RECEIVED SPI Slave CMD Received 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Nam									SPIS_CMD_RECEIVED							

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e																
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SPIS_CMD_RECEIVED	**Command received** SPI slave received a command.

A20E0000 SPISLV_PAD_DUMMY_CNT SPI Slave Pad Dummy Count 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SPIS_PAD_DUMMY_CNT			
Type													RW			
Reset													0	0	0	0

Bit(s)	Name	Description
3:0	SPIS_PAD_DUMMY_CNT	**Dummy count** The number of dummy bits in one packet. Dummy phase is the second transmission of packet between command phase and data phase. Dummy phase cannot transmit/receive data, it is only used in Dual/Quad SPI (SPIS_TYPE = 1 or 2).

A20E0004 SPISLV_PAD_CMD_DEF0 SPI Slave Pad Command Define 0 08060402

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIS_PAD_CMD_WS								SPIS_PAD_CMD_RS							
Type	RW								RW							
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIS_PAD_CMD_PWON								SPIS_PAD_CMD_PWOFF							
Type	RW								RW							
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit(s)	Name	Description
31:24	SPIS_PAD_CMD_WS	**Defines Write Status (WS) command value**

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Bit(s)	Name	Description
23:16	SPIS_PAD_CMD_RS	**Defines Read Status (RS) command value**
15:8	SPIS_PAD_CMD_PWON	**Defines Power-ON (PWON) command value**
7:0	SPIS_PAD_CMD_PWOFF	**Defines Power-OFF (PWOFF) command value**

A20E0008 SPISLV_PAD_CMD_DEF1 SPI Slave Pad Command Define 1 0E810C0A

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SPIS_PAD_CMD_WR								SPIS_PAD_CMD_RD							
Type	RW								RW							
Reset	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SPIS_PAD_CMD_CW								SPIS_PAD_CMD_CR							
Type	RW								RW							
Reset	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	0

Bit(s)	Name	Description
31:24	SPIS_PAD_CMD_WR	**Defines Write Data (WR) command value**
23:16	SPIS_PAD_CMD_RD	**Defines Read Data (RD) command value**
15:8	SPIS_PAD_CMD_CW	**Defines Configure Write (CW) command value**
7:0	SPIS_PAD_CMD_CR	**Defines Configure Read (CR) command value**

A20E000C SPISLV_PAD_CMD_DEF2 SPI Slave Pad Command Define 2 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SPIS_PAD_CMD_CT							
Type									RW							
Reset									0	0	0	1	0	0	0	0

Bit(s)	Name	Description
7:0	SPIS_PAD_CMD_CT	**Defines Configure Type (CT) command value**

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Bit(s)	Name	Description

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22. Auxiliary ADC Unit

22.1. Overview

MT2625 features an auxiliary ADC (AUXADC) unit with five external channels and two internal channels to measure a 12-bit successive approximation register (SAR) ADC. The reference voltage is 1.4V. The SAR ADC waveform is shown in Figure 13.1-1.

Figure 22.1-1. SAR ADC waveform

22.2. Abbreviations

Table 2.1-1 lists the abbreviations used in this chapter.

Table 22.2-1. Abbreviations

Abbreviation	Definition
AUXADC	Auxiliary ADC
SAR ADC	Successive approximation ADC
VBATSNS	Voltage battery sensor
TS	Temperature sensor
LSLP	Light sleep
LDO	Low dropout

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22.3. Features

1) Immediate mode.

There are five channels for external and two channels for internal channel use in immediate mode. The AUXADC measures values only once when the flag of the channel in the AUXADC_CON1 register is set. The value sampled for channel 0 is stored in register AUXADC_DATA0, the value for channel 1 is stored in register AUXADC_DATA1, and so on.

2) Zero-consumption-voltage (ZCV) mode.

There is only one channel for internal channel use in ZCV mode. This channel measures voltage automatically to monitor battery power during power up and wake up.

22.4. Block diagram

The block diagram for the AUXADC is shown in Figure 7.3-1.

Figure 22.4-1. AUXADC block diagram

22.5. Functions

1) Immediate mode.

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The AUXADC measures values only once when the flag of the channel in the AUXADC_CON1 register is set. For example, if the value in AUXADC_CON1 is set, the AUXADC will sample the data for channel 0. Without configuring AUXADC_CON4, AUXADC_CON1 must be cleared and set again to initialize another sampling.

If the AUTOSET flag in register AUXADC_CON4 is set, the auto-sampling function will be enabled. The A/D converter then samples the data for the specified channel. When the data register AUXADC_DATA0 is read, the A/D converter immediately samples the next value for channel 0.

If multiple channels are selected at the same time, the task will be performed sequentially on every selected channel. For example, if AUXADC_CON1 is set to 0xf, if 4 channels are selected, the state machine in the unit will start sampling from channel 3 to channel 0 and save the values of each input channel in respective registers.

2) Zero-consumption-voltage (ZCV) mode

There is only one channel for internal channels in ZCV mode. This channel only measures voltage automatically during power up and wake up. Set AUXADC_ZCV_BYPASS to 1, to prevent default automatic measurements after wake up. The ZCV data will be saved into AUXADC_DATA_ZCV.

Table 22.5-1. AUXADC channel description

AUXADC Channel ID	Description
Channel 0	External (immediate mode)
Channel 1	External (immediate mode)
Channel 2	External (immediate mode)
Channel 3	External (immediate mode)
Channel 4	External (immediate mode)
Channel 5	Internal – TS (immediate mode)
Channel 6	Internal – VBATSNS (immediate mode)
Channel ZCV	Internal – VBATSNS (ZCV mode)

22.6. Programming sequence

There are external and internal channels measured by the AUXADC. When using an external channel to sample data, GPIO register settings must be correct. For more details, see section, “General Purpose Inputs/Outputs”. If the correct GPIO settings are not turned on, the AUXADC will not sample correct data. When using an internal channel to sample data, some registers must be set correctly to turn on the internal channel.

The following guidelines are about setting the TS and VBATSNS.

1) TS

- TS control
  - In the MT2625 PMU, PMU temperature could be sensed by TS output to AUXADC
- Control flow
  - To enable TS output to AUXADC, set 0xA207_0A60[4]-RG_ADC_TS_EN high, wait for 200µs, and then enable AUXADC measurement. After that, set 0xA207_0A60[4]-RG_ADC_TS_EN low to save the current.
  - The current consumption is around 10µA and will not be disabled automatically in LSLP mode, so the bit must be set low when the detection is done or before entering LSLP mode.

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2) VBATSNS

- VBATSNS control
  - In the MT2625 PMU, the VBAT sensing output is default-on for ZCV detection. The divider circuit's current consumption is about 200µA
- Control flow
  - In normal mode, the detection circuits could be disabled, if the current consumption is a major concern.
  - Set `0xA207_0A60[3]-RG_EN_VABTSNS_ROUT` low to disable detection circuits.
  - To measure VBAT voltage, set `0xA207_0A60[3]-RG_EN_VABTSNS_ROUT=1'b1` and wait for 200µs, then enable AUXADC channel. After the measurement, set `0xA207_0A60[3]-RG_EN_VABTSNS_ROUT=1'b0` to save the current.
  - Before entering LSLP mode, this bit needs to be set high for ZCV detection when chip returns to normal mode.
  - The internal control is disabled automatically in LSLP mode so it will not consume power in LSLP mode.

The following guidelines are about setting different modes.

1) Immediate mode

Immediate mode sampling is accomplished by programming `AUXADC_CON1` with the channels to be sampled.

- Sample data after selecting the channel.
- Wait for `AUXADC_CON3 [0]: ADC_STAT` to change from 1 (busy) to 0 (idle).

It is required to program `AUXADC_CON1` back to 0 before sampling again. The immediate mode programming sequence is summarized in Figure 22.6-1.

Figure 22.6-1. Immediate mode programming sequence

Note: to disable the AUXADC, turn off the digital clock (`ANA_EN_CON[0] = 0`) first and then turn off the analog power (`MACRO_CON2[0]=0`).

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2) Zero-consumption-voltage (ZCV) mode:

There is only one internal channel (VBATSNS) in ZCV mode (see Table 22.5-1). This channel measures voltage automatically during power up and wake up. There is no need to control the ZCV programming sequence. However, it is possible to control the measurement of next wake up by programming AUXADC_ZCV_BYPASS.

Note: To use the ZCV feature, do not disable the clock gate of AUXADC (XO_PDN_COND0[21], default is active), otherwise the ZCV feature will not function at next wakeup.

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22.7. Register mapping

Module name: AUXADC Base address: (+a0140000h)

Address	Name	Width (bits)	Register Function
A0140004	AUXADC_CON1	16	Configure channel in immediate mode
A0140008	AUXADC_CON3	16	Configure reset and read status
A014000C	AUXADC_CON4	16	Configure auto-set
A0140010	AUXADC_DATA0	16	channel 0 data
A0140014	AUXADC_DATA1	16	channel 1 data
A0140018	AUXADC_DATA2	16	channel 2 data
A014001C	AUXADC_DATA3	16	channel 3 data
A0140020	AUXADC_DATA4	16	channel 4 data
A0140024	AUXADC_DATA5	16	channel 5 data
A0140028	AUXADC_DATA6	16	channel 6 data
A0140050	AUXADC_DATA_ZCV	16	ZCV channel data
A0140074	MACRO_CON2	16	Configure analog control
A0140078	ANA_EN_CON	16	Configure digital clock

A0140004 AUXADC_CON1 Configure channel in immediate mode 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										AUXADC_CON1						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	AUXADC_CON1	**Bit 0 : Channel 0 immediate mode** 0: The channel is not selected. 1: The channel is selected. **Bit 1 : Channel 1 immediate mode** 0: The channel is not selected. 1: The channel is selected. **Bit 2 : Channel 2 immediate mode** 0: The channel is not selected. 1: The channel is selected. **Bit 3 : Channel 3 immediate mode** 0: The channel is not selected. 1: The channel is selected. **Bit 4 : Channel 4 immediate mode** 0: The channel is not selected. 1: The channel is selected. **Bit 5 : Channel 5 immediate mode** 0: The channel is not selected. 1: The channel is selected. **Bit 6 : Channel 6 immediate mode** 0: The channel is not selected. 1: The channel is selected.

A0140008 AUXADC_CON3 Configure reset and read status 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name								**SOFT_RST**								**ADC_STAT**
Type								RW								RO
Reset								0								0

Bit(s)	Name	Description
8	SOFT_RST	**Software reset AUXADC state machine** 0: Default value 1: Reset the AUXADC state machine
0	ADC_STAT	**Defines the state of the module** 0: Idle. 1: Busy.

A014000C AUXADC_CON4 Configure auto-set 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**AUTOSET**
Type																RW
Reset																0

Bit(s)	Name	Description
0	AUTOSET	**Defines the auto-sampling mode of the module. In this mode, each channel starts sampling immediately without configuring the control register AUXADC_CON1 again.**

A0140010 AUXADC_DATA0 channel 0 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**AUXADC_DATA0**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA0	**Sampled data for channel0**

A0140014 AUXADC_DATA1 channel 1 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					**AUXADC_DATA1**											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA1	**Sampled data for channel1**

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A0140018 AUXADC_DATA2 channel 2 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_DATA2											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA2	Sampled data for channel2

A014001C AUXADC_DATA3 channel 3 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_DATA3											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA3	Sampled data for channel3

A0140020 AUXADC_DATA4 channel 4 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_DATA4											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA4	Sampled data for channel4

A0140024 AUXADC_DATA5 channel 5 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_DATA5											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA5	Sampled data for channel5

A0140028 AUXADC_DATA6 channel 6 data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_DATA6											
Type					RO											
Rese					0	0	0	0	0	0	0	0	0	0	0	0

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t																

Bit(s)	Name	Description
11:0	AUXADC_DATA6	**Sampled data for channel6**

A0140050 AUXADC_DATA_ZCV ZCV channel data 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					AUXADC_DATA_ZCV											
Type					RO											
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
11:0	AUXADC_DATA_ZCV	**Sampled data for ZCV channel**

A0140074 MACRO_CON2 Configure analog control 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																RG_AUXADC_LDO_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	RG_AUXADC_LDO_EN	**Enables the AUXADC analog power.**

A0140078 ANA_EN_CON Configure digital clock 00000000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																AUXADC_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	AUXADC_EN	**Enables the AUXADC clock.**

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23. General Purpose Timer

23.1. Overview

The general purpose timer (GPT) includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes, ONE-SHOT, REPEAT, freerun with interrupt (FREERUN_I), and FREERUN, and can operate on either system clock (13MHz) or real-time clock (RTC). The GPT is an always-on IP, which means it retains the previous configuration and runs even if the system enters sleep mode. Note that in sleep mode, the clock source should be set to RTC since there is no system clock.

23.2. Features

23.2.1. Timer mode

Each GPT has four modes, ONE-SHOT, REPEAT, FREERUN_I and FREERUN.

1) ONE-SHOT mode. An interrupt occurs and the timer stops once GPT is timed out.
2) REPEAT mode. An interrupt occurs and the timer resets once GPT is timed out.
3) FREERUN_I mode. An interrupt occurs and the timer continues once the GPT is timed out.
4) FREERUN mode. The GPT continues counting with no limit.

23.2.2. Timer clock source

Each GPT can operate on either system clock (13MHz) or RTC. There is also a 4-bit clock divider, which divides the clock by 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 16, 32, or 64. Note, that in sleep mode, only RTC is available.

23.2.3. Timer interrupt source

All GPTs share a single interrupt source. The user can get the interrupt status by reading `GPT_IRQSTA[5:0]` and `GPTx_IRQ_STA`. To clear the interrupt, write 1 to `GPTx_IRQ_ACK`.

23.2.4. System wakeup source

The interrupt signal is also connected to System Power Management (SPM) as a wakeup source.

23.3. Limitations

1) The following operations take two cycles of bus clock (26MHz) plus two cycles of system or RTC clock to take effect.
   - Start GPT
   - Stop GPT
   - Clear GPT
   - Set comparison value
2) Every two clear commands need to be separated by 5 cycles of bus clock and 4 cycles of system or RTC clock. GPT_CLRSTA indicates the clear status of each GPT.

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3) Every two set comparison value commands need to be separated by 5 cycles of bus clock and 4 cycles of system or RTC clock. GPT_WCOMPSTA indicates the set comparison value status of each GPT.

4) While reading the counter value of GPT5, the lower word must be read first.

23.4. Block diagram

The block diagram of the GPT is shown in Figure 23.4-1Figure 7.3-1.

Figure 23.4-1. GPT block diagram

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23.5. Functions

The function of each mode is described in Table 23.5-1.

Table 23.5-1. GPT operation modes

Mode	Interrupt	Reached limit	Example: set GPTx_COMPARE to 2 **Bold means interrupt*
ONE-SHOT	Yes	Stop	0,1,**2**,2,2,2,2,2,2,2,2,2,...
REPEAT	Yes	Restart from 0	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**...
FREERUN_I	Yes	Keep counting	0,1,**2**,3,4,5,6,7,8,9,10,...
FREERUN	No	Keep counting	0,1,2,3,4,5,6,7,8,9,10,...

23.6. Programming sequence

The following configuration is required to initialize the GPT settings:

1) Disable GPT clock (`GPTx_CON[16]`).
2) Set the clock frequency (`GPTx_CLK`).
   - Do not change the clock frequency while clock is enabled.
3) Enable the clock (`GPTx_CON[16]`).
4) Clear the counter (`GPTx_CLR`).
5) Set operation mode (`GPTx_CON[9:8]`).
   - Do not modify operation mode while GPT is enabled.
6) Enable interrupt (`GPTx_IRQ_EN`).
7) Set comparison value (`GPTx_COMPAREx`).
8) Enable the GPT (`GPTx_CON[0]`).

23.7. Register mapping

Module name: APXGPT Base address: (+a2130000h)

Address	Name	Width (bits)	Register Function
A2130000	GPT_IRQSTA	32	GPT IRQ status
A2130004	GPT_CLRSTA	32	GPT clear status
A2130008	GPT_WCOMPSTA	32	GPT write comparison value status
A2130010	GPT0_CON	32	GPT0 control
A2130014	GPT0_CLR	32	Clear GPT0
A2130018	GPT0_CLK	32	GPT0 clock setting
A213001C	GPT0_IRQ_EN	32	GPT0 IRQ enable
A2130020	GPT0_IRQ_STA	32	GPT0 IRQ status
A2130024	GPT0_IRQ_ACK	32	GPT0 IRQ acknowledgement

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Address	Name	Width (bits)	Register Function
A2130028	GPT0_COUNT	32	GPT0 counter value
A213002C	GPT0_COMPARE	32	GPT0 comparison value
A2130040	GPT1_CON	32	GPT1 control
A2130044	GPT1_CLR	32	Clear GPT1
A2130048	GPT1_CLK	32	GPT1 clock setting
A213004C	GPT1_IRQ_EN	32	GPT1 IRQ enable
A2130050	GPT1_IRQ_STA	32	GPT1 IRQ status
A2130054	GPT1_IRQ_ACK	32	GPT1 IRQ acknowledgement
A2130058	GPT1_COUNT	32	GPT1 counter value
A213005C	GPT1_COMPARE	32	GPT1 comparison value
A2130070	GPT2_CON	32	GPT2 control
A2130074	GPT2_CLR	32	Clear GPT2
A2130078	GPT2_CLK	32	GPT2 clock setting
A213007C	GPT2_IRQ_EN	32	GPT2 IRQ enable
A2130080	GPT2_IRQ_STA	32	GPT2 IRQ status
A2130084	GPT2_IRQ_ACK	32	GPT2 IRQ acknowledgement
A2130088	GPT2_COUNT	32	GPT2 counter value
A213008C	GPT2_COMPARE	32	GPT2 comparison value
A21300A0	GPT3_CON	32	GPT3 control
A21300A4	GPT3_CLR	32	Clear GPT3
A21300A8	GPT3_CLK	32	GPT3 clock setting
A21300AC	GPT3_IRQ_EN	32	GPT3 IRQ enable
A21300B0	GPT3_IRQ_STA	32	GPT3 IRQ status
A21300B4	GPT3_IRQ_ACK	32	GPT3 IRQ acknowledgement
A21300B8	GPT3_COUNT	32	GPT3 counter value
A21300BC	GPT3_COMPARE	32	GPT3 comparison value
A21300D0	GPT4_CON	32	GPT4 control
A21300D4	GPT4_CLR	32	Clear GPT4
A21300D8	GPT4_CLK	32	GPT4 clock setting
A21300DC	GPT4_IRQ_EN	32	GPT4 IRQ enable
A21300E0	GPT4_IRQ_STA	32	GPT4 IRQ status
A21300E4	GPT4_IRQ_ACK	32	GPT4 IRQ acknowledgement
A21300E8	GPT4_COUNT	32	GPT4 counter value
A21300EC	GPT4_COMPARE	32	GPT4 comparison value
A2130100	GPT5_CON	32	GPT5 control
A2130104	GPT5_CLR	32	Clear GPT5
A2130108	GPT5_CLK	32	GPT5 clock setting
A213010C	GPT5_IRQ_EN	32	GPT5 IRQ enable
A2130110	GPT5_IRQ_STA	32	GPT5 IRQ status
A2130114	GPT5_IRQ_ACK	32	GPT5 IRQ acknowledgement
A2130118	GPT5_COUNTL	32	GPT5 lower word counter value
A213011C	GPT5_COMPAREL	32	GPT5 lower word comparison value
A2130120	GPT5_COUNTH	32	GPT5 higher word counter value
A2130124	GPT5_COMPAREH	32	GPT5 higher word comparison value

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A2130000 GPT_IRQSTA GPT IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											IRQSTA					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	IRQSTA	**Interrupt status of each GPT** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A2130004 GPT_CLRSTA GPT clear status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											CLRSTA					
Type											RU					
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5:0	CLRSTA	**Clear status of each GPT** 0: Clear is done 1: Clear is in progress

A2130008 GPT_WCOMPSTA GPT write comparison value status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										WCOMPSTA						
Type										RU						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6:0	WCOMPSTA	**Write comparison value status of each GPT** 0: Write comparison value is done 1: Write comparison value is in progress

A2130010 GPT0_CON GPT0 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																**SW_CG0**
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MODE0**									**EN0**
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG0	**Enable clock for GPT0** 0: Enable 1: Disable
9:8	MODE0	**Operation mode of GPT0** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN0	**Enable GPT0** 0: Disable 1: Enable

A2130014 GPT0_CLR Clear GPT0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CLR0**
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR0	**Clear GPT0** 0: No effect 1: Clear

A2130018 GPT0_CLK GPT0 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CLK0**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK0	**Clock source & clock divider for GPT0** Bit[4] - Clock source:

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Bit(s)	Name	Description
		0: System clock (13MHz) 1: RTC clock (32KHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A213001C GPT0_IRQ_EN GPT0 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN0
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN0	**Enable interrupt of GPT0** 0: Disable 1: Enable

A2130020 GPT0_IRQ_STA GPT0 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA0
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA0	**Interrupt status of GPT0** 0: No interrupt is generated

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Bit(s)	Name	Description
		1: Interrupt is pending and waiting for service

A2130024 GPT0_IRQ_ACK GPT0 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK0
Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK0	**Interrupt acknowledgement for GPT0** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A2130028 GPT0_COUNT GPT0 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER0															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER0	**Counter value of GPT0**

A213002C GPT0_COMPARE GPT0 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE0															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE0	**Comparison value of GPT0**

A2130040 GPT1_CON GPT1 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SW_CG1

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Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MODE1**									**EN1**
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG1	**Enable clock for GPT1** 0: Enable 1: Disable
9:8	MODE1	**Operation mode of GPT1** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN1	**Enable GPT1** 0: Disable 1: Enable

A2130044 GPT1_CLR Clear GPT1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CLR1**
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR1	**Clear GPT1** 0: No effect 1: Clear

A2130048 GPT1_CLK GPT1 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CLK1**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK1	**Clock source & clock divider for GPT1** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32KHz)

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Bit(s)	Name	Description
		Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A213004C GPT1_IRQ_EN GPT1 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN1
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN1	**Enable interrupt of GPT1** 0: Disable 1: Enable

A2130050 GPT1_IRQ_STA GPT1 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA1
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA1	**Interrupt status of GPT1** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

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A2130054 GPT1_IRQ_ACK GPT1 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK1
Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK1	**Interrupt acknowledgement for GPT1** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A2130058 GPT1_COUNT GPT1 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER1	**Counter value of GPT1**

A213005C GPT1_COMPARE GPT1 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE1	**Comparison value of GPT1**

A2130070 GPT2_CON GPT2 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SW_CG2
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name							MODE2									EN2
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG2	**Enable clock for GPT2** 0: Enable 1: Disable
9:8	MODE2	**Operation mode of GPT2** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN2	**Enable GPT2** 0: Disable 1: Enable

A2130074 GPT2_CLR Clear GPT2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLR2
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR2	**Clear GPT2** 0: No effect 1: Clear

A2130078 GPT2_CLK GPT2 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK2				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK2	**Clock source & clock divider for GPT2** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32KHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2

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Bit(s)	Name	Description
		0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A213007C GPT2_IRQ_EN GPT2 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN2
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN2	**Enable interrupt of GPT2** 0: Disable 1: Enable

A2130080 GPT2_IRQ_STA GPT2 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA2
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA2	**Interrupt status of GPT2** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A2130084 GPT2_IRQ_ACK GPT2 IRQ acknowledgement 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK2
Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK2	**Interrupt acknowledgement for GPT2** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A2130088 GPT2_COUNT GPT2 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER2															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER2	**Counter value of GPT2**

A213008C GPT2_COMPARE GPT2 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE2															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE2															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE2	**Comparison value of GPT2**

A21300A0 GPT3_CON GPT3 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SW_CG3
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MODE3									EN3
Type							RW									RW

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Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG3	**Enable clock for GPT3** 0: Enable 1: Disable
9:8	MODE3	**Operation mode of GPT3** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN3	**Enable GPT3** 0: Disable 1: Enable

A21300A4 GPT3_CLR Clear GPT3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**CLR3**
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR3	**Clear GPT3** 0: No effect 1: Clear

A21300A8 GPT3_CLK GPT3 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**CLK3**				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK3	**Clock source & clock divider for GPT3** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32KHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4

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Bit(s)	Name	Description
		0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A21300AC GPT3_IRQ_EN GPT3 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN3
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN3	**Enable interrupt of GPT3** 0: Disable 1: Enable

A21300B0 GPT3_IRQ_STA GPT3 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA3
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA3	**Interrupt status of GPT3** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A21300B4 GPT3_IRQ_ACK GPT3 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**IRQACK3**
Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK3	**Interrupt acknowledgement for GPT3** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A21300B8 GPT3_COUNT GPT3 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**COUNTER3**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**COUNTER3**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER3	**Counter value of GPT3**

A21300BC GPT3_COMPARE GPT3 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**COMPARE3**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**COMPARE3**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE3	**Comparison value of GPT3**

A21300D0 GPT4_CON GPT4 control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**SW_CG4**
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MODE4**									**EN4**
Type							RW									RW
Reset							0	0								0

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Bit(s)	Name	Description
16	SW_CG4	**Enable clock for GPT4** 0: Enable 1: Disable
9:8	MODE4	**Operation mode of GPT4** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN4	**Enable GPT4** 0: Disable 1: Enable

A21300D4 GPT4_CLR Clear GPT4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLR4
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR4	**Clear GPT4** 0: No effect 1: Clear

A21300D8 GPT4_CLK GPT4 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK4				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK4	**Clock source & clock divider for GPT4** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32KHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6

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Bit(s)	Name	Description
		0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A21300DC GPT4_IRQ_EN GPT4 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN4
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN4	**Enable interrupt of GPT4** 0: Disable 1: Enable

A21300E0 GPT4_IRQ_STA GPT4 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA4
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA4	**Interrupt status of GPT4** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A21300E4 GPT4_IRQ_ACK GPT4 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK4
Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK4	**Interrupt acknowledgement for GPT4** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A21300E8 GPT4_COUNT GPT4 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER4															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER4	**Counter value of GPT4**

A21300EC GPT4_COMPARE GPT4 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE4															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE4															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE4	**Comparison value of GPT4**

A2130100 GPT5_CON GPT5 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SW_CG5
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MODE5									EN5
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG5	**Enable clock for GPT5** 0: Enable

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Bit(s)	Name	Description
		1: Disable
9:8	MODE5	**Operation mode of GPT5** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN5	**Enable GPT5** 0: Disable 1: Enable

A2130104 GPT5_CLR Clear GPT5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLR5
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR5	**Clear GPT5** 0: No effect 1: Clear

A2130108 GPT5_CLK GPT5 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK5				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK5	**Clock source & clock divider for GPT5** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32KHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8

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Bit(s)	Name	Description
		1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A213010C GPT5_IRQ_EN GPT5 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN5
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN5	**Enable interrupt of GPT5** 0: Disable 1: Enable

A2130110 GPT5_IRQ_STA GPT5 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA5
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA5	**Interrupt status of GPT5** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A2130114 GPT5_IRQ_ACK GPT5 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK5

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Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK5	**Interrupt acknowledgement for GPT5** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A2130118 GPT5_COUNTL GPT5 lower word counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER5L															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER5L															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER5L	**Lower word counter value of GPT5**

A213011C GPT5_COMPAREL GPT5 lower word comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE5L															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE5L															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE5L	**Lower word comparison value of GPT5**

A2130120 GPT5_COUNTH GPT5 higher word counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER5H															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER5H															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER5H	**Higher word counter value of GPT5**

A2130124 GPT5_COMPAREH GPT5 higher word comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	COMPARE5H															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE5H															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE5H	**Higher word comparison value of GPT5**

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24. Operating System Timer

24.1. Overview

The operating system timer (OST) includes two 32-bit timers. Each timer has four operation modes, ONE-SHOT, REPEAT, freerun with interrupt (FREERUN_I) and FREERUN, and can operate on either system clock (13MHz) or real-time clock (RTC). The OST is an always-on IP, which means it retains the previous configuration and runs even if the system enters sleep mode. Note, that in sleep mode, the clock source should be set to RTC since there is no system clock.

24.2. Features

24.2.1. Timer mode

Each OST has four modes, ONE-SHOT, REPEAT, FREERUN_I, and FREERUN.

1) ONE-SHOT mode. An interrupt occurs and the timer stops once OST is timed out.
2) REPEAT mode. An interrupt occurs and the timer resets once OST is timed out.
3) FREERUN_I mode. An interrupt occurs and the timer continues once the OST is timed out.
4) FREERUN mode. The OST continues counting with no limit.

24.2.2. Timer clock source

Each OST can operate on either system clock (13MHz) or RTC. There is also a 4-bit clock divider, which divides the clock by 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 16, 32 or 64. Note, that in sleep mode, only RTC is available.

24.2.3. Timer interrupt source

All OSTs share a single interrupt source. The user can get the interrupt status by reading `OST_IRQSTA[1:0]` and `OSTx_IRQ_STA`. To clear the interrupt, write 1 to `OSTx_IRQ_ACK`.

24.2.4. System wakeup source

The interrupt signal is also connected to System Power Management (SPM) as a wakeup source.

24.3. Limitations

1) The following operations take two cycles of bus clock (26MHz) plus two cycles of system or RTC clock to take effect.

   甲、 Start OST

   乙、 Stop OST

   丙、 Clear OST

   丁、 Set comparison value

2) Every two clear commands need to be separated by 5 cycles of bus clock and 4 cycles of system or RTC clock. OST_CLRSTA indicates the clear status of each OST.

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3) Every two set comparison value commands need to be separated by 5 cycles of bus clock and 4 cycles of system or RTC clock. OST_WCOMPSTA indicates the status of set comparison value of each OST.

24.4. Block diagram

The block diagram of the OST is shown in Figure 7.3-1.

Figure 24.4-1. OST block diagram

24.5. Functions

The function of each mode is described in Table 24.5-1.

Table 24.5-1. OST operation modes

Mode	Interrupt	Reached limit	Example: set `OSTx_COMPARE` to 2 **Bold means interrupt*
ONE-SHOT	Yes	Stop	0,1,**2**,2,2,2,2,2,2,2,2,2,...
REPEAT	Yes	Restart from 0	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**...
FREERUN_I	Yes	Keep counting	0,1,**2**,3,4,5,6,7,8,9,10,...
FREERUN	No	Keep counting	0,1,2,3,4,5,6,7,8,9,10,...

24.6. Programming sequence

The following configuration is required to initialize the OST settings:

1) Disable OST clock (`OSTx_CON[16]`).
2) Set the clock frequency (`OSTx_CLK`).
   - Do not change the clock frequency while clock is enabled.

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3) Enable the clock (OSTx_CON[16]).
4) Clear the counter (OSTx_CLR).
5) Set operation mode (OSTx_CON[9:8]).
   - Do not modify operation mode while OST is enabled.
6) Enable interrupt (OSTx_IRQ_EN).
7) Set comparison value (OSTx_COMPAREx).
8) Enable the OST (OSTx_CON[0]).

24.7. Register mapping

Module name: OSGPT Base address: (+a21b0000h)

Address	Name	Width (bits)	Register Function
A21B0000	OST_IRQSTA	32	OST IRQ status
A21B0004	OST_CLRSTA	32	OST clear status
A21B0008	OST_WCOMPSTA	32	OST write comparison value status
A21B0010	OST0_CON	32	OST0 control
A21B0014	OST0_CLR	32	Clear OST0
A21B0018	OST0_CLK	32	OST0 clock setting
A21B001C	OST0_IRQ_EN	32	OST0 IRQ enable
A21B0020	OST0_IRQ_STA	32	OST0 IRQ status
A21B0024	OST0_IRQ_ACK	32	OST0 IRQ acknowledgement
A21B0028	OST0_COUNT	32	OST0 counter value
A21B002C	OST0_COMPARE	32	OST0 comparison value
A21B0040	OST1_CON	32	OST1 control
A21B0044	OST1_CLR	32	Clear OST1
A21B0048	OST1_CLK	32	OST1 clock setting
A21B004C	OST1_IRQ_EN	32	OST1 IRQ enable
A21B0050	OST1_IRQ_STA	32	OST1 IRQ status
A21B0054	OST1_IRQ_ACK	32	OST1 IRQ acknowledgement
A21B0058	OST1_COUNT	32	OST1 counter value
A21B005C	OST1_COMPARE	32	OST1 comparison value

A21B0000 OST_IRQSTA OST IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															IRQSTA	
Type															RU	
Reset															0	0

Bit(s)	Name	Description
1:0	IRQSTA	Interrupt status of each OST

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Bit(s)	Name	Description
		0: No interrupt is generated 1: Interrupt is pending and waiting for service

A21B0004 OST_CLRSTA OST clear status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															CLRSTA	
Type															RU	
Reset															0	0

Bit(s)	Name	Description
1:0	CLRSTA	**Clear status of each OST** 0: Clear is complete 1: Clear is in progress

A21B0008 OST_WCOMPSTA OST write comparison value status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															WCOMPSTA	
Type															RU	
Reset															0	0

Bit(s)	Name	Description
1:0	WCOMPSTA	**Write comparison value status of each OST** 0: Write comparison value is ready 1: Write comparison value is in progress

A21B0010 OST0_CON OST0 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SW_CG0
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							MODE0									EN0
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG0	**Enable clock for OST0** 0: Enable

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Bit(s)	Name	Description
		1: Disable
9:8	MODE0	**Operation mode of OST0** 00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN0	**Enable OST0** 0: Disable 1: Enable

A21B0014 OST0_CLR Clear OST0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLR0
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR0	**Clear OST0** 0: No effect 1: Clear

A21B0018 OST0_CLK OST0 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK0				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK0	**Clock source & clock divider for OST0** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32kHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8

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Bit(s)	Name	Description
		1000: Clock source divided by 9 1001: Clock source divided by 10 1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A21B001C OST0_IRQ_EN OST0 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN0
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN0	**Enable interrupt of OST0** 0: Disable 1: Enable

A21B0020 OST0_IRQ_STA OST0 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA0
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA0	**Interrupt status of OST0** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A21B0024 OST0_IRQ_ACK OST0 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK0

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Type																WO
Reset																0

Bit(s)	Name	Description
0	IRQACK0	**Interrupt acknowledgement for OST0** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A21B0028 OST0_COUNT OST0 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**COUNTER0**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**COUNTER0**															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER0	**Counter value of OST0**

A21B002C OST0_COMPARE OST0 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**COMPARE0**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**COMPARE0**															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE0	**Comparison value of OST0**

A21B0040 OST1_CON OST1 control 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**SW_CG1**
Type																RW
Reset																1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**MODE1**									**EN1**
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
16	SW_CG1	**Enable clock for OST1** 0: Enable 1: Disable
9:8	MODE1	**Operation mode of OST1**

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Bit(s)	Name	Description
		00: ONE-SHOT 01: REPEAT 10: FREERUN_I 11: FREERUN
0	EN1	**Enable OST1** 0: Disable 1: Enable

A21B0044 OST1_CLR Clear OST1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLR1
Type																WO
Reset																0

Bit(s)	Name	Description
0	CLR1	**Clear OST1** 0: No effect 1: Clear

A21B0048 OST1_CLK OST1 clock setting 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												CLK1				
Type												RW				
Reset												0	0	0	0	0

Bit(s)	Name	Description
4:0	CLK1	**Clock source & clock divider for OST1** Bit[4] - Clock source: 0: System clock (13MHz) 1: RTC clock (32kHz) Bit[3:0] - Clock divider: 0000: Clock source divided by 1 0001: Clock source divided by 2 0010: Clock source divided by 3 0011: Clock source divided by 4 0100: Clock source divided by 5 0101: Clock source divided by 6 0110: Clock source divided by 7 0111: Clock source divided by 8 1000: Clock source divided by 9 1001: Clock source divided by 10

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Bit(s)	Name	Description
		1010: Clock source divided by 11 1011: Clock source divided by 12 1100: Clock source divided by 13 1101: Clock source divided by 16 1110: Clock source divided by 32 1111: Clock source divided by 64

A21B004C OST1_IRQ_EN OST1 IRQ enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQEN1
Type																RW
Reset																0

Bit(s)	Name	Description
0	IRQEN1	**Enable interrupt of OST1** 0: Disable 1: Enable

A21B0050 OST1_IRQ_STA OST1 IRQ status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQSTA1
Type																RU
Reset																0

Bit(s)	Name	Description
0	IRQSTA1	**Interrupt status of OST1** 0: No interrupt is generated 1: Interrupt is pending and waiting for service

A21B0054 OST1_IRQ_ACK OST1 IRQ acknowledgement 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																IRQACK1
Type																WO

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Reset																0

Bit(s)	Name	Description
0	IRQACK1	**Interrupt acknowledgement for OST1** 0: No effect 1: Interrupt is acknowledged and should be relinquished

A21B0058 OST1_COUNT OST1 counter value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COUNTER1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COUNTER1															
Type	RU															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	COUNTER1	**Counter value of OST1**

A21B005C OST1_COMPARE OST1 comparison value FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COMPARE1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COMPARE1															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	COMPARE1	**Comparison value of OST1**

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25. Sensor Controller

25.1. Overview

The sensor controller controls peripherals to capture sensor data with a programmable microprocessor. The purpose is to capture small blocks of sensor data in a single period using a much smaller programmable microprocessor without consuming the Cortex-M4 MCU's power. The sensor controller includes two major designs: `sensor_ctrl_ao` in always-on power domain and `sensor_ctrl_pd` in INFRASYS power domain.

25.2. Abbreviations

Table 25.2-1 lists the abbreviations used in this section.

Table 25.2-1. Abbreviations

Abbreviation	Definition
EOI	End of instruction
SPM	System power manager
MTCMOS	Multi-threshold CMOS power gating (power domain)

25.3. Features

The sensor controller module provides two timers with 32kHz counter, one microcontroller and a FIFO register group. The SYSRAM can be used as FIFO.

The timer provides two output signals:

1) `timer_wakeup_event`
2) `timer_expire_flag`

The `timer_wakeup_event` is used to notify the SPM to turn on INFRASYS MTCMOS. The `timer_expire_flag` triggers the sensor microprocessor to capture data by configuring the I2C register. The timing interval between `timer_wakeup_event` and `timer_expire_flag` is register `*SENSOR_TIMER_WAKEUP_LATENCY`, which is the preparation time for SPM to turn on INFRA. The timing interval for `timer_expire_flag` is register `*SENSOR_TIMER_EXPIRING_PERIOD`, which is the sensor data capturing period.

Figure 25.3-1. Sensor timer sequence

The microprocessor can be programmed in assembly and access I2C and SPI registers through the bus.

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The FIFO register group is for Cortex-M4 and sensor microprocessor to exchange FIFO information, such as empty, full, write pointer and read pointer.

25.4. Block diagram

The block diagram for the sensor controller is shown in Figure 7.3-1.

Figure 25.4-1. Sensor controller block diagram

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25.5. Functions

The sensor controller operation flow is shown in Figure 25.5-1. First, software configures the sensor timer, then it starts the sensor microprocessor after instruction set is loaded. The timer provides `SESNOR_TIMER_0_WAKEUP_EVENT` and `SENSOR_TIMER_0_EXPIRE_FLAG`. `INFRASYS MTCMOS (INFRA_PD)` turns on, if `SESNOR_TIMER_0_WAKEUP_EVENT` or SPM are received. Once INFRASYS is on, I2C and SPI are ready for data communication.

The `SENSOR_TIMER_0_EXPIRE_FLAG` is the actual capture time. The sensor microprocessor waits for the `SENSOR_TIMER_0_EXPIRE_FLAG` signal to configure the I2C register to capture data. `I2C_0_IRQ` shows that the data is transmitted. The data may be transmitted in chunks depending on the sensor data size. The sensor microprocessor may update write pointer after transfer is complete. After all data is transferred, the microprocessor jumps to EOI and sends "`sensor_ctrl_pd_irq`". The SPM finds it and turns off `INFRA_PD`, if the capture occurred while CMSYS is asleep.

Figure 25.5-1. Sensor controller operation flow

25.6. Register mapping

The base names and addresses are shown in the table below.

Base name	Base address
SENSOR_FIFO	0xA2180000

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Base name	Base address
SENSOR_TIMER	0xA2190000
SENSOR_UP	0xA0160000

25.6.1. SENSOR_FIFO register map

Module name: SENSOR_FIFO Base address: (+a2180000h)

Address	Name	Width (bits)	Register Function
A2180000	SENSOR_IRQ_flag	32	SENSOR_IRQ_flag
A2180004	SENSOR_IRQ_set	32	SENSOR_IRQ_set
A2180008	SENSOR_IRQ_clr	32	SENSOR_IRQ_clr
A2180010	SENSOR_IRQ_WAKEUP_AP_EN	32	SENSOR_IRQ_WAKEUP_AP_EN
A2180120	SENSOR_CH_0_REG_0	32	SENSOR_REG_0
A2180124	SENSOR_CH_0_REG_1	32	SENSOR_REG_1
A2180128	SENSOR_CH_0_REG_2	32	SENSOR_REG_2
A218012C	SENSOR_CH_0_REG_3	32	SENSOR_REG_3
A2180220	SENSOR_CH_1_REG_0	32	SENSOR_REG_0
A2180224	SENSOR_CH_1_REG_1	32	SENSOR_REG_1
A2180228	SENSOR_CH_1_REG_2	32	SENSOR_REG_2
A218022C	SENSOR_CH_1_REG_3	32	SENSOR_REG_3
A2180320	SENSOR_CH_2_REG_0	32	SENSOR_REG_0
A2180324	SENSOR_CH_2_REG_1	32	SENSOR_REG_1
A2180328	SENSOR_CH_2_REG_2	32	SENSOR_REG_2
A218032C	SENSOR_CH_2_REG_3	32	SENSOR_REG_3
A2180420	SENSOR_CH_3_REG_0	32	SENSOR_REG_0
A2180424	SENSOR_CH_3_REG_1	32	SENSOR_REG_1
A2180428	SENSOR_CH_3_REG_2	32	SENSOR_REG_2
A218042C	SENSOR_CH_3_REG_3	32	SENSOR_REG_3
A2180600	SENSOR_AO_DEBUG_CON	32	SENSOR_AO_DEBUG_CON
A2180604	SENSOR_AO_DEBUG_SELECT	32	SENSOR_AO_DEBUG_SELECT
A2180800	SENSOR_RESERVED_0	32	SENSOR_RESERVED_0
A2180804	SENSOR_RESERVED_1	32	SENSOR_RESERVED_1

A2180000 SENSOR_IRQ_flag SENSOR_IRQ_flag 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SENSOR_IRQ_flag**							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSOR_IRQ_flag	**IRQ flag: IRQ is reserved for software usage as an interrupt to Cortex-M4**

A2180004 SENSOR_IRQ_set SENSOR_IRQ_set 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SENSOR_IRQ_set**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSOR_IRQ_set	**set IRQ flag: set by sensor microprocessor**

A2180008 SENSOR_IRQ_clr SENSOR_IRQ_clr 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SENSOR_IRQ_clr**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSOR_IRQ_clr	**clear IRQ flag: clear by Cortex-M4**

A2180010 SENSOR_IRQ_WAKEUP_AP_EN SENSOR_IRQ_WAKEUP_AP_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**SENSOR_IRQ_WAKEUP_AP_EN**							
Type									RW							
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:0	SENSOR_IRQ_WAKEUP_AP_EN	**1: enable corresponding SENSOR_IRQ_flag to wake up the Cortex-M4**

A2180120 SENSOR_CH_0_REG_0 SENSOR_REG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH0_W_POINTER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH0_W_POINTER	**write pointer: write by sensor controller, read by Cortex-M4**

A2180124 SENSOR_CH_0_REG_1 SENSOR_REG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH0_R_POINTER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH0_R_POINTER	**read pointer: write by Cortex-M4, read by sensor controller**

A2180128 SENSOR_CH_0_REG_2 SENSOR_REG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH0_THRESHOLD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH0_THRESHOLD	**threshold filled by Cortex-M4, when threshold is reached, send SENSOR_FIFO_IRQ**

A218012C SENSOR_CH_0_REG_ SENSOR_REG_3 00000000

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3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH0_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH0_START_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CH0_END_ADDR	**end address for storing data**
15:0	CH0_START_ADDR	**start address for storing data**

A2180220 SENSOR_CH_1_REG_0 SENSOR_REG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH1_W_POINTER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH1_W_POINTER	**write pointer: write by sensor controller, read by Cortex-M4**

A2180224 SENSOR_CH_1_REG_1 SENSOR_REG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH1_R_POINTER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH1_R_POINTER	**read pointer: write by Cortex-M4, read by sensor controller**

A2180228 SENSOR_CH_1_REG_2 SENSOR_REG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH1_THRESHOLD															

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Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH1_THRESHOLD	**threshold filled by Cortex-M4, when threshold is reached, send SENSOR_FIFO_IRQ**

A218022C **SENSOR_CH_1_REG_3** **SENSOR_REG_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CH1_END_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH1_START_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CH1_END_ADDR	**end address for storing data**
15:0	CH1_START_ADDR	**start address for storing data**

A2180320 **SENSOR_CH_2_REG_0** **SENSOR_REG_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH2_W_POINTER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH2_W_POINTER	**write pointer: write by sensor controller, read by Cortex-M4**

A2180324 **SENSOR_CH_2_REG_1** **SENSOR_REG_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH2_R_POINTER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH2_R_POINTER	**read pointer: write by Cortex-M4, read by sensor controller**

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A2180328 SENSOR_CH_2_REG_2 SENSOR_REG_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH2_THRESHOLD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH2_THRESHOLD	**threshold filled by Cortex-M4, when threshold is reached, send SENSOR_FIFO_IRQ**

A218032C SENSOR_CH_2_REG_3 SENSOR_REG_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CH2_END_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH2_START_ADDR															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CH2_END_ADDR	**end address for storing data**
15:0	CH2_START_ADDR	**start address for storing data**

A2180420 SENSOR_CH_3_REG_0 SENSOR_REG_0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CH3_W_POINTER															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH3_W_POINTER	**write pointer: write by sensor controller, read by Cortex-M4**

A2180424 SENSOR_CH_3_REG_1 SENSOR_REG_1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

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Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH3_R_POINTER**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH3_R_POINTER	**read pointer: write by Cortex-M4, read by sensor controller**

A2180428 **SENSOR_CH_3_REG_2** **SENSOR_REG_2** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH3_THRESHOLD**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	CH3_THRESHOLD	**configurable option for Cortex-M4. SENSOR_FIFO_IRQ is issued when write pointer - read pointer >= threshold**

A218042C **SENSOR_CH_3_REG_3** **SENSOR_REG_3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**CH3_END_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**CH3_START_ADDR**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	CH3_END_ADDR	**end address for storing data**
15:0	CH3_START_ADDR	**start address for storing data**

A2180600 **SENSOR_AO_DEBUG_CON** **SENSOR_AO_DEBUG_CON** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**DEBUG_EN**
Type																RW

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Reset																0

Bit(s)	Name	Description
0	DEBUG_EN	**enable debug output**

A2180604 SENSOR_AO_DEBUG_SELECT **SENSOR_AO_DEBUG_SELECT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSOR_AO_DEBUG_SELECT_GOURP_0**								**SENSOR_AO_DEBUG_SELECT_GOURP_1**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSOR_AO_DEBUG_SELECT_GOURP_2**								**SENSOR_AO_DEBUG_SELECT_GOURP_3**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	SENSOR_AO_DEBUG_SELECT_GOURP_0	**select group_0**
23:16	SENSOR_AO_DEBUG_SELECT_GOURP_1	**select group_1**
15:8	SENSOR_AO_DEBUG_SELECT_GOURP_2	**select group_2**
7:0	SENSOR_AO_DEBUG_SELECT_GOURP_3	**select group_3**

A2180800 SENSOR_RESERVED_0 **SENSOR_RESERVED_0** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSOR_RESERVED_REG_0**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SENSOR_RESERVED_REG_0	**reserved register**

A2180804 SENSOR_RESERVED_1 **SENSOR_RESERVED_1** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSOR_RESERVED_REG_1**															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
15:0	SENSOR_RESERVED_REG_1	reserved register

25.6.2. SENSOR_TIMER register map

Module name: SENSOR_TIMER Base address: (+a2190000h)

Address	Name	Width (bits)	Register Function
A2190000	SENSOR_TIMER_0_ENABLE	32	TIMER_0_ENABLE
A2190004	SENSOR_TIMER_0_EXPIRING_PERIOD	32	TIMER_0_EXPIRING_PERIOD
A2190008	SENSOR_TIMER_0_EXPIRING_FLAG_B	32	TIMER_0_EXPIRING_FLAG_B
A219000C	SENSOR_TIMER_0_CLEAR_EXPIRING_FLAG	32	TIMER_0_CLEAR_EXPIRING_FLAG
A2190010	SENSOR_TIMER_0_IRQ_MASK	32	TIMER_0_IRQ_MASK
A2190020	SENSOR_TIMER_0_WAKEUP_LATENCY	32	TIMER_0_WAKEUP_LATENC\CY
A2190028	SENSOR_TIMER_0_WAKEUP_EVENT_B	32	TIMER_0_WAKEUP_EVENT_B
A219002C	SENSOR_TIMER_0_CLEAR_WAKEUP_EVENT	32	TIMER_0_CLEAR_WAKEUP_EVENT
A2190030	SENSOR_TIMER_0_TIMER_CNT	32	TIMER_0_TIMER_CNT
A2190040	SENSOR_TIMER_0_WAKEUP_EN	32	TIMER_0_WAKEUP_EN
A2190100	SENSOR_TIMER_1_ENABLE	32	TIMER_1_ENABLE
A2190104	SENSOR_TIMER_1_EXPIRING_PERIOD	32	TIMER_1_EXPIRING_PERIOD
A2190108	SENSOR_TIMER_1_EXPIRING_FLAG_B	32	TIMER_1_EXPIRING_FLAG
A219010C	SENSOR_TIMER_1_CLEAR_EXPIRING_FLAG	32	TIMER_1_CLEAR_EXPIRING_FLAG_B
A2190110	SENSOR_TIMER_1_IRQ_MASK	32	TIMER_1_IRQ_MASK
A2190120	SENSOR_TIMER_1_WAKEUP_LATENCY	32	TIMER_1_WAKEUP_LATENCY
A2190128	SENSOR_TIMER_1_WAKEUP_EVENT_B	32	TIMER_1_WAKEUP_EVENT_B
A219012C	SENSOR_TIMER_1_CLEAR_WAKEUP_EVENT	32	TIMER_1_CLEAR_WAKEUP_EVENT
A2190130	SENSOR_TIMER_1_TIMER_CNT	32	TIMER_1_TIMER_CNT
A2190140	SENSOR_TIMER_1_WAKEUP_EN	32	TIMER_1_WAKEUP_EN

A2190000 SENSOR_TIMER_0_ENABLE TIMER_0_ENABLE 00000000

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TIMER_0_RUN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TIMER_0_LOAD								TIMER_0_ENABLE
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
16	TIMER_0_RUN	**1: start sensor timer; 0:stop sensor timer**
8	TIMER_0_LOAD	**set timer value as an expiring period**
0	TIMER_0_ENABLE	**1: enable timer: 0: disable timer**

A2190004 SENSOR_TIMER_0_EXPIRING_PERIOD TIMER_0_EXPIRING_PERIOD 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMER_0_EXPIRING_PERIOD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TIMER_0_EXPIRING_PERIOD	**load value, down count,** maximum: (16 bits): 65535*30.5 us = 1.998s (20 bits): 31.981s (24 bits): 511.697s=8.52mins (28 bits): 2.274hours (32 bits): 36.387hours

A2190008 SENSOR_TIMER_0_EXPIRING_FLAG_B TIMER_0_EXPIRING_FLAG_B 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_0_EXPIRING_FLAG_B
Type																RO
Reset																1

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Bit(s)	Name	Description
0	TIMER_0_EXPIRING_FLAG_B	**0: timer_irq**

A219000C **SENSOR_TIMER_0_CLEAR_EXPIRING_FLAG** **TIMER_0_CLEAR_EXPIRING_FLAG** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_0_CLEAR_EXPIRING_FLAG
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_0_CLEAR_EXPIRING_FLAG	**clear timer IRQ**

A2190010 **SENSOR_TIMER_0_IRQ_MASK** **TIMER_0_IRQ_MASK** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_0_IRQ_MASK
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_0_IRQ_MASK	**mask sensor timer 0 IRQ**

A2190020 **SENSOR_TIMER_0_WAKEUP_LATENCY** **TIMER_0_WAKEUP_LATENC\CY** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TIMER_0_WAKEUP_LATENCY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

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Bit(s)	Name	Description
7:0	TIMER_0_WAKEUP_LATENCY	**latency from expiring flag rising to sample data, maximum 7.777ms** valid when wakeup_event=expiry_irq is enabled

A2190028 **SENSOR_TIMER_0_WAKEUP_EVENT_B** **TIMER_0_WAKEUP_EVENT_B** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_0_WAKEUP_EVENT_B
Type																RO
Reset																1

Bit(s)	Name	Description
0	TIMER_0_WAKEUP_EVENT_B	**0: wakeup event**

A219002C **SENSOR_TIMER_0_CLEAR_WAKEUP_EVENT** **TIMER_0_CLEAR_WAKEUP_EVENT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_0_CLEAR_WAKEUP_EVENT
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_0_CLEAR_WAKEUP_EVENT	**clear wakeup event**

A2190030 **SENSOR_TIMER_0_TIMER_CNT** **TIMER_0_TIMER_CNT** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name	TIMER_0_TIMER_CNT															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	TIMER_0_TIMER_CNT	**timer value**

A2190040 SENSOR_TIMER_0_WAKEUP_EN TIMER_0_WAKEUP_EN 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_0_WAKEUP_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_0_WAKEUP_EN	**enable wakeup** 0: wakeup_event=expiry_flag 1: wakeup_event occurred before expiry_flag by *SENSOR_TIMER_0_WAKEUP_LATENCY

A2190100 SENSOR_TIMER_1_ENABLE TIMER_1_ENABLE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																TIMER_1_RUN
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TIMER_1_LOAD								TIMER_1_ENABLE
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
16	TIMER_1_RUN	**1: timer down count; 0: timer kept current value** **1: start sensor timer; 0:stop sensor timer**
8	TIMER_1_LOAD	**timer load from an expiring period** **set timer value as an expiring period**
0	TIMER_1_ENABLE	**enable timer** **1: enable timer: 0: disable timer**

A2190104 SENSOR_TIMER_1_EX TIMER_1_EXPIRING_PERIOD 00000000

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PIRING_PERIOD

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMER_1_EXPIRING_PERIOD															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	TIMER_1_EXPIRING_PERIOD	**load value, down count,** maximum: (16 bits): 65535*30.5 us = 1.998s (20 bits): 31.981s (24 bits): 511.697s=8.52mins (28 bits): 2.274hours (32 bits): 36.387hours

A2190108 **SENSOR_TIMER_1_EXPIRING_FLAG_B** **TIMER_1_EXPIRING_FLAG** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_1_EXPIRING_FLAG_B
Type																RO
Reset																1

Bit(s)	Name	Description
0	TIMER_1_EXPIRING_FLAG_B	**0: timer_irq**

A219010C **SENSOR_TIMER_1_CLEAR_EXPIRING_FLAG** **TIMER_1_CLEAR_EXPIRING_FLAG_B** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_1_CLEAR_EXPIRING_FLAG
Type																RW
Reset																0

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Bit(s)	Name	Description
0	TIMER_1_CLEAR_EXPIRING_FLAG	**clear timer IRQ**

A2190110 SENSOR_TIMER_1_IRQ_MASK TIMER_1_IRQ_MASK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_1_IRQ_MASK
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_1_IRQ_MASK	**mask sensor timer 1 IRQ**

A2190120 SENSOR_TIMER_1_WAKEUP_LATENCY TIMER_1_WAKEUP_LATENCY 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TIMER_1_WAKEUP_LATENCY							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	TIMER_1_WAKEUP_LATENCY	**latency from expiring flag rising to sample data, maximum 7.777ms** valid when wakeup_event=expiry_irq is enabled

A2190128 SENSOR_TIMER_1_WAKEUP_EVENT_B TIMER_1_WAKEUP_EVENT_B 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_1_WAKEUP_EVENT_B
Type																RO
Reset																1

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Bit(s)	Name	Description
0	TIMER_1_WAKEUP_EVENT_B	**0: wakeup event**

A219012C **SENSOR_TIMER_1_CLEAR_WAKEUP_EVENT** **TIMER_1_CLEAR_WAKEUP_EVENT** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_1_CLEAR_WAKEUP_EVENT
Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_1_CLEAR_WAKEUP_EVENT	**clear wakeup event**

A2190130 **SENSOR_TIMER_1_TIMER_CNT** **TIMER_1_TIMER_CNT** **0000FFFF**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TIMER_1_TIMER_CNT															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	TIMER_1_TIMER_CNT	**timer count value**

A2190140 **SENSOR_TIMER_1_WAKEUP_EN** **TIMER_1_WAKEUP_EN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																TIMER_1_WAKEUP_EN

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Type																RW
Reset																0

Bit(s)	Name	Description
0	TIMER_1_WAKEUP_EN	**enable wakeup** 0: wakeup_event=expiry_flag 1: wakeup_event occurred before expiry_flag by *SENSOR_TIMER_1_WAKEUP_LATENCY

25.6.3. Sensor microprocessor (SENSOR_UP) register map

Module name: sensor_up Base address: (+a0160000h)

Address	Name	Width (bits)	Register Function
A0160080	SENSORUP_SPIMST_IRQ_MASK	32	**mask SPIMST IRQ to Cortex-M4**
A0160084	SENSORUP_I2C_IRQ_MASK	32	**mask I2C IRQ to Cortex-M4**
A0160300	SENSORUP_CON0	32	**Microprocessor control register 0**
A0160304	SENSORUP_CON1	32	**Microprocessor control register 1**
A0160308	STOP_SENSOR_CATCH	32	**STOP_SENSOR_CATCH**
A0160330	SENSORUP_IM_HOST_RW_PTR	32	**Microprocessor IM read write pointer register**
A0160334	SENSORUP_IM_HOST_RW_DAT	32	**Microprocessor IM read/write data**
A0160340	SENSORUP_EVENT_VECTOR0	32	**Microprocessor event vector register**
A0160344	SENSORUP_EVENT_VECTOR1	32	**Microprocessor event vector register**
A0160348	SENSORUP_EVENT_VECTOR2	32	**Microprocessor event vector register**
A016034C	SENSORUP_EVENT_VECTOR3	32	**Microprocessor event vector register**
A0160350	SENSORUP_EVENT_VECTOR4	32	**Microprocessor event vector register**
A0160354	SENSORUP_EVENT_VECTOR5	32	**Microprocessor event vector register**
A0160358	SENSORUP_EVENT_VECTOR6	32	**Microprocessor event vector register**
A016035C	SENSORUP_EVENT_VECTOR7	32	**Microprocessor event vector register**
A0160380	SENSORUP_SLEEP_WAKEUP_EVENT_MASK	32	**AP sleep wakeup event mask**
A0160390	SENSORUP_SLEEP_ISR_MASK	32	**AP sleep ISR mask**
A01603D0	SENSORUP_DEBUG_SELECT	32	**SENSOR_DEBUG_SELECT**
A01603D4	SENSORUP_DEBUG_CON	32	**SENSOR_DEBUG_OUT_EN**
A01603E0	SENSORUP_ERROR_FLAG	32	**error flag**
A0160810	SENSORUP_STATE_STATUS	32	**STATE_STATUS**

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Address	Name	Width (bits)	Register Function
A0160820	SENSORUP_SLEEP_ISR_STATUS	32	AP sleep ISR status
A0160900	SENSORUP_REG0_DATA	32	Microprocessor general RF data
A0160904	SENSORUP_REG1_DATA	32	Microprocessor general RF data
A0160908	SENSORUP_REG2_DATA	32	Microprocessor general RF data
A016090C	SENSORUP_REG3_DATA	32	Microprocessor general RF data
A0160910	SENSORUP_REG4_DATA	32	Microprocessor general RF data
A0160914	SENSORUP_REG5_DATA	32	Microprocessor general RF data
A0160918	SENSORUP_REG6_DATA	32	Microprocessor general RF data
A016091C	SENSORUP_REG7_DATA	32	Microprocessor general RF data
A0160920	SENSORUP_REG8_DATA	32	Microprocessor general RF data
A0160924	SENSORUP_REG9_DATA	32	Microprocessor general RF data
A0160928	SENSORUP_REG10_DATA	32	Microprocessor general RF data
A016092C	SENSORUP_REG11_DATA	32	Microprocessor general RF data
A0160930	SENSORUP_REG12_DATA	32	Microprocessor general RF data
A0160934	SENSORUP_REG13_DATA	32	Microprocessor general RF data
A0160938	SENSORUP_REG14_DATA	32	Microprocessor general RF data
A016093C	SENSORUP_REG15_DATA	32	Microprocessor general RF data
A0160980	SENSORUP_TIMER_OUT	32	SENSOR_uP_TIMER
A01609E0	SENSORUP_EVENT_REG_STA	32	Event register status
A01609E4	SENSORUP_FSM_STA	32	SENSOR FSM status
A0160B00	SENSORUP_RESERVE	32	uP_RESERVE
A0160B04	SENSORUP_RESERVE2	32	uP_RESERVE2
A0160B10	SENSORUP_FLAGS	32	uP_FLAGS
A0160B90	SENSORUP_SW_INT	32	SENSOR_uP_SW_INT
A0160B94	SENSORUP_SW_INT_MASK	32	SENSOR_uP_SW_INT_MASK
A0160B98	SENSORUP_SW_INT_SET	32	SENSOR_uP_SW_INT_SET
A0160B9C	SENSORUP_SW_INT_CLEAR	32	SENSOR_uP_SW_INT_CLEAR

A0160080 SENSORUP_SPIMST_IRQ_MASK mask SPIMST IRQ to Cortex-M4 **00000000**

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Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPIMST_IRQ_MASK	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPIMST_IRQ_MASK	**mask SPIMST IRQ to Cortex-M4 when sensor controller is using SPI**

A0160084 SENSORUP_I2C_IRQ_MASK mask I2C IRQ to Cortex-M4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														I2C_IRQ_MASK		
Type														RW		
Reset														0	0	0

Bit(s)	Name	Description
2:0	I2C_IRQ_MASK	**mask I2C IRQ to Cortex-M4 while sensor controller is using I2C**

A0160300 SENSORUP_CON0 uP control register 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EVENT_VEC_EN											SENSORUP_CON0_group_0				
Type	RO											RO				
Reset	0	0	0	0	0	0	0	0				0	0	0	0	0

Bit(s)	Name	Description
15:8	EVENT_VEC_EN	**Enables event vector**
4:0	SENSORUP_CON0_group_0	**[0]: Level Trigger – Kick Start microprocessor process** [1]: Level Trigger - Kick IM process [2]: kick sequencer [4]: Resets the **microprocessor**

A0160304 SENSORUP_CON1 uP control register 1 00002C00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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Name			SENSORUP_CON1_group_0													
Type			RO													
Reset			1	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:0	SENSORUP_CON1_group_0	**[0]: Enables IM slave mode** [1]: IM sleep control signal [3]: Enables master I/F access APB [4]: IM power down control signal [5]: Enables **microprocessor** timer [6]: Enables non-replace mode

A0160308 STOP_SENSOR_CATCH STOP_SENSOR_CATCH 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STOP_SENSOR_CATCH_AFTER_FINISH
Type																RW
Reset																0

Bit(s)	Name	Description
0	STOP_SENSOR_CATCH_AFTER_FINISH	**1: stop sensor microprocessor after current data capture is finished**

A0160330 SENSORUP_IM_HOST_RW_PTR uP IM read write pointer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								SENSORUP_IM_HOST_EN								SENSORUP_IM_HOST_W_EN
Type								RW								RW
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							SENSORUP_IM_HOST_RW_PTR									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
24	SENSORUP_IM_HOST_EN	**Enables sensor microprocessor IM Host pointer register**
16	SENSORUP_IM_HOST_W_EN	**Enables sensor microprocessor IM write pointer register**
9:0	SENSORUP_IM_HOST_RW_PTR	**Microprocessor IM read/write pointer register**

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A0160334 SENSORUP_IM_HOST_RW_DAT uP IM read/write data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IM_RD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IM_RD															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	IM_RD	**microprocessor IM read/write data register** Note that this register bit is not a read/write type. When writing into this register, it writes data of internal SRAM. When reading this register, it will read data of internal SRAM.

A0160340 SENSORUP_EVENT_VECTOR0 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC0_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC0						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC0_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC0	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

A0160344 SENSORUP_EVENT_VECTOR1 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC1_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC1						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC1_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC1	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

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A0160348 SENSORUP_EVENT_VECTOR2 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC2_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC2						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC2_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC2	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

A016034C SENSORUP_EVENT_VECTOR3 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC3_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC3						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC3_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC3	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

A0160350 SENSORUP_EVENT_VECTOR4 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC4_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC4						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC4_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC4	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

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A0160354 SENSORUP_EVENT_VECTOR5 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC5_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC5						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC5_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC5	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

A0160358 SENSORUP_EVENT_VECTOR6 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC6_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC6						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC6_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC6	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

A016035C SENSORUP_EVENT_VECTOR7 uP event vector register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								EVENT_VEC7_PC								
Type								RW								
Reset								0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										EVENT_VEC7						
Type										RW						
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
24:16	EVENT_VEC7_PC	**microprocessor event vector program counter**
6:0	EVENT_VEC7	**[4:0]: microprocessor event vector (WID)** [5]: **microprocessor** event vector resume [6]: **microprocessor** event vector immediate mode

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A0160380 SENSORUP_SLEEP_WAKEUP_EVENT_MASK AP Sleep Wakeup Event Mask FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_EVENT_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WAKEUP_EVENT_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	WAKEUP_EVENT_MASK	**AP wakeup event mask: r12 mask** 0: No mask 1: Mask the wakeup event and this event will not wake up the sleep procedure

A0160390 SENSORUP_SLEEP_ISR_MASK AP Sleep ISR Mask 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																SENSORUP_IRQ_B_MASK
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SENSORUP_IRQ_MASK
Type																RW
Reset																0

Bit(s)	Name	Description
16	SENSORUP_IRQ_B_MASK	**Mask microprocessor IRQB**
0	SENSORUP_IRQ_MASK	**Mask microprocessor IRQ**

A01603D0 SENSORUP_DEBUG_SELECT SENSOR_DEBUG_SELECT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SENSORUP_DEBUG_SELECT_GROUP_3								SENSORUP_DEBUG_SELECT_GROUP_2						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		SENSORUP_DEBUG_SELECT_GROUP_1								SENSORUP_DEBUG_SELECT_GROUP_0						
Type		RW								RW						
Reset		0	0	0	0	0	0	0		0	0	0	0	0	0	0

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Bit(s)	Name	Description
30:24	SENSORUP_DEBUG_SELECT_GROUP_3	**select group_3**
22:16	SENSORUP_DEBUG_SELECT_GROUP_2	**select group_2**
14:8	SENSORUP_DEBUG_SELECT_GROUP_1	**select group_1**
6:0	SENSORUP_DEBUG_SELECT_GROUP_0	**select group_0**

A01603D4 **SENSORUP_DEBUG_CON** **SENSOR_DEBUG_OUT_EN** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SENSORUP_DEBUG_OUT_EN
Type																RW
Reset																0

Bit(s)	Name	Description
0	SENSORUP_DEBUG_OUT_EN	**Enables debug monitor output** 0: Disable **microprocessor** debug monitor 1: Enable **microprocessor** debug monitor

A01603E0 **SENSORUP_ERROR_FLAG** **error flag** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_ERROR_FLAG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_ERROR_FLAG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_ERROR_FLAG	**error flag to indicate abnormal behavior**

A0160810 **SENSORUP_STATE_STATUS** **STATE_STATUS** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									STATE_STATUS							

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Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	STATE_STATUS	**Sensor state for debugging purposes.**

A0160820 **SENSORUP_SLEEP_ISR_STATUS** **AP Sleep ISR Status** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SENSORUP_SLEEP_ISR_STATUS**
Type																RO
Reset																0

Bit(s)	Name	Description
0	SENSORUP_SLEEP_ISR_STATUS	**For SPM to clear** Write 1 to clear IRQ

A0160900 **SENSORUP_REG0_DATA** **uP general RF data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG0_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG0_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG0_RF	**microprocessor data**

A0160904 **SENSORUP_REG1_DATA** **uP general RF data** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG1_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG1_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

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Bit(s)	Name	Description
31:0	SENSORUP_REG1_RF	microprocessor data

A0160908 SENSORUP_REG2_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG2_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG2_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG2_RF	microprocessor data

A016090C SENSORUP_REG3_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG3_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG3_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG3_RF	microprocessor data

A0160910 SENSORUP_REG4_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG4_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG4_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG4_RF	microprocessor data

A0160914 SENSORUP_REG5_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG5_RF															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG5_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG5_RF	**microprocessor data**

A0160918 SENSORUP_REG6_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG6_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG6_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG6_RF	**microprocessor data**

A016091C SENSORUP_REG7_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG7_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG7_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG7_RF	**microprocessor data**

A0160920 SENSORUP_REG8_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG8_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG8_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG8_RF	**microprocessor data**

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A0160924 SENSORUP_REG9_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG9_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG9_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG9_RF	**microprocessor data**

A0160928 SENSORUP_REG10_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG10_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG10_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG10_RF	**microprocessor data**

A016092C SENSORUP_REG11_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG11_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG11_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG11_RF	**microprocessor data**

A0160930 SENSORUP_REG12_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_REG12_RF															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_REG12_RF															
Type	RO															

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Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG12_RF	**microprocessor data**

A0160934 SENSORUP_REG13_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG13_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG13_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG13_RF	**microprocessor data**

A0160938 SENSORUP_REG14_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG14_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG14_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG14_RF	**microprocessor data**

A016093C SENSORUP_REG15_DATA uP general RF data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**SENSORUP_REG15_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**SENSORUP_REG15_RF**															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_REG15_RF	**microprocessor data**

A0160980 SENSORUP_TIMER_OUT SENSOR_uP_TIMER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name	SENSORUP_TIMER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_TIMER															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_TIMER	**Timer output**

A01609E0 SENSORUP_EVENT_REG_STA event register status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EVET_CNTER_STA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EVET_CNTER_STA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	EVET_CNTER_STA	**SENSOR microprocessor event register status** [31:28] CFG [27:0] Counter

A01609E4 SENSORUP_FSM_STA SENSOR FSM status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							SENSORUP_FSM_STA_group									
Type							RO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_FSM_STA_group															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
25:0	SENSORUP_FSM_STA_group	**[3:0]: EXEC_INST_OP, instruction op code** [6:4]: PC_STATE, program counter state [9:7]: IM_STATE, instruction memory state [14:10]: MASTER_STATE, master interface state [17:15]: EVENT_FSM, event state status [21:21]: UP_KICK Level Trigger: Kick-start **microprocessor** process [22:22]: IM_KICK Level Trigger: Kick-start IM process

A0160B00 SENSORUP_RESERVE uP_RESERVE 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_RESERVE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_RESERVE															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_RESERVE	**Reserved**

A0160B04 SENSORUP_RESERVE2 uP_RESERVE2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_RESERVE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_RESERVE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_RESERVE2	**Reserved**

A0160B10 SENSORUP_FLAGS uP_FLAGS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SENSORUP_FLAGS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SENSORUP_FLAGS															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SENSORUP_FLAGS	**Reserved**

A0160B90 SENSORUP_SW_INT SENSOR_uP_SW_INT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENSORUP_SW_INT							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSORUP_SW_INT	**read SENSOR software interrupt** Write 1 to clear

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A0160B94 SENSORUP_SW_INT_MASK SENSOR_uP_SW_INT_MASK 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENSORUP_SW_INT_MASK							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSORUP_SW_INT_MASK	**mask software interrupt to sensor_irq**

A0160B98 SENSORUP_SW_INT_SET SENSOR_uP_SW_INT_SET 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENSORUP_SW_INT_SET							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSORUP_SW_INT_SET	**Set SENSOR software interrupt** Write 1 to set

A0160B9C SENSORUP_SW_INT_CLEAR SENSOR_uP_SW_INT_CLEAR 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SENSORUP_SW_INT_CLEAR							
Type									RO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SENSORUP_SW_INT_CLEAR	**Clear SENSOR software interrupt** Write 1 to clear

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26. Universal Asynchronous Receiver/Transmitter

26.1. Overview

The universal asynchronous receiver transmitter (UART) provides full duplex serial communication channels between the baseband chipset and external devices.

The UART has both M16C450 and M16550A modes of operation that are compatible with a range of standard software drivers. The extensions are designed to be broadly software compatible with M16550A variants, but certain areas offer no consensus.

The UART supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits and is fully programmable by an 8-bit CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included together with separate transmit and receive FIFOs. Two modem control lines and a diagnostic loop-back mode are provided. The UART also includes two DMA handshake lines, indicating when the FIFOs are ready to transfer data to the CPU.

Note, that the UART is designed so that all internal operation is synchronized by the clock signal. This synchronization results in minor timing differences between the UART and industry standard M16550A device, which means that the core is not clocked for clock identical to the original device.

After hardware reset, the UART will be in M16C450 mode. Its FIFOs can then be enabled and the UART can enter M16550A mode. The UART also has further additional functions beyond the M16550A mode. Each of the extended functions can be selected individually under software control.

26.2. Features

- There are four UART channels supporting software flow control. Two of them support hardware flow control. Each UART has an individual interrupt source.
- For transmission, the UART supports word lengths from 5 to 8 bits with an optional parity bit and 1 or 2 stop bits.
- The UART supports standard baud rates of 110bps, 300bps, 1200bps, 2400bps, 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps, 921600bps and non-standard baud rates from 110bps to 3Mbps.
- There are dedicated DMA channels for both transmit (TX) and receive (RX) for each UART.
- The UART supports automatic baud rate detection in RX mode. The recommended baud rate range is from 110bps to 115,200bps.

26.3. Block diagram

Figure 26.3-1 shows the detailed UART block diagram.

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Figure 26.3-1. UART block diagram

26.4. Functions

26.4.1. Baud rate generation

The UART contains a programmable baud generator. The baud rate generator divides the input clock by a divisor to generate a baud clock for data sampling. The baud clock is n times the baud rate where n is a positive integer. The formula to calculate the baud rate is:

$$\text{Baud Rate} = (\text{Input Clock Frequency}) \ / \ \text{Divisor} \ / \ \text{n}$$

The input clock frequency can be either F_FXO_CK or F_FXO_CK/2, the frequency of F_FXO_CK is 26MHz. The divisor is stored in two 8-bit register fields in the Divisor Latch (DL) register, Divisor Latch High (DLH) and Divisor Latch Low (DLL). The positive integer n is controlled by HIGHSPEED.SPEED.

- When HIGHSPEED.SPEED = 0, n = 16 and the data is sampled in the eighth baud clock cycle. When HIGHSPEED.SPEED = 1, n = 8 and the data is sampled in the fourth baud clock cycle.
- When HIGHSPEED.SPEED = 2, n = 4 and the data is sampled in the second baud clock cycle.
- When HIGHSPEED.SPEED = 3, n = SAMPLE_REG.SAMPLE_COUNT+1 and the data is sampled in the (SAMPLE_REG.SAMPLE_POINT)th baud clock cycle.

26.4.2. Data format

The data format of the UART is shown in Figure 26.4-1. One transmission includes 1 start bit; 5, 6, 7 or 8 data bits; 1 optional parity bit; and 1 or 2 stop bits. The start bit is always low, the parity bit can be either odd or even parity, and the end bit is always high.

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Figure 26.4-1 UART data format

26.4.3. Transmission

Transmission of the UART includes a TX holding register (THR) and TX shift register (TSR). THR receives data from Advanced Peripheral Bus (APB) and shifts to TSR. The data in TSR will then be serialized and sent to General-Purpose Input/Output (GPIO). In FIFO mode, the THR becomes a 16-byte FIFO.

26.4.4. Reception

Reception of the UART includes an RX buffer register (RBR) and RX shift register (RSR). RSR receives and concatenates the serial data bits from GPIO. The data will then be moved from RSR to RBR and ready to be read by APB. In FIFO mode, the RBR becomes a 32-byte FIFO.

26.4.5. Direct Memory Access (DMA) mode

The UART supports DMA mode operation only when the FIFOs are enabled (FCR.FIFOE == 1). Set DMA_CON.TX_DMA_EN and DMA_CON.RX_DMA_EN to 1 to enable DMA mode of transmission and reception, respectively.

26.4.6. Hardware flow control

Two of the four UART channels support RTS/CTS hardware flow control. In transmission mode, the UART will pause transmission if CTS is asserted, and will resume transmission after CTS is de-asserted. In reception mode, the UART will assert RTS if one of the following conditions is met:

1) RBR is occupied in non-FIFO mode.
2) The amount of data in RBR is above threshold in FIFO mode or DMA mode.
3) The amount of data in virtual FIFO DMA is above threshold in DMA mode.
4) The system is entering sleep mode.

The UART will de-assert RTS when all of the above conditions are no longer met.

26.4.7. Software flow control

The UART supports XON/XOFF flow control. In transmission mode, the UART will pause transmission if an XOFF character is received and will resume transmission after receiving an XON character. In reception mode, the UART will send an XOFF character if one of the following conditions is met:

1) RBR is occupied in non-FIFO mode.
2) The amount of data in RBR is above threshold in FIFO mode or DMA mode.
3) The amount of data in virtual FIFO DMA is above threshold in DMA mode.
4) The system is entering sleep mode.

The UART will send an XON character when conditions 1, 2, and 3 are no longer valid. However, if the UART sends an XOFF character due to condition 4, the user should send an XON character manually after wake-up since the UART is powered down and all settings are cleared in sleep mode.

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26.5. Register mapping

There are four UART interfaces supported in this chipset. The registers below are the same for all UARTs. However, for UART0 and UART3, hardware flow control related functions are useless.

UART number	Base address	Feature
UART0	0xA00C0000	Supports DMA
UART1	0xA00D0000	Supports DMA, hardware flow control
UART2	0xA00E0000	Supports DMA, hardware flow control
UART3	0xA00F0000	Supports DMA

Module name: UART_0 Base address: (+a00c0000h)

Address	Name	Width (bits)	Register Function
A00C0000	RBR	32	RX buffer register
A00C0004	THR	32	TX holding register
A00C0008	DL	32	Divisor latch
A00C000C	IER	32	Interrupt enable register
A00C0010	IIR	32	Interrupt identification register
A00C0014	FCR	32	FIFO control register
A00C0018	EFR	32	Enhanced feature register
A00C001C	LCR	32	Line control register
A00C0020	MCR	32	Modem control register
A00C0024	XON_XOFF	32	XON & XOFF character
A00C0028	LSR	32	Line status register
A00C002C	SCR	32	Scratch register
A00C0030	AUTOBAUD_CON	32	Auto-baud control register
A00C0034	HIGHSPEED	32	High speed mode register
A00C0038	SAMPLE_REG	32	Sample counter & sample point register
A00C003C	AUTOBAUD_REG	32	Auto-baud monitor register
A00C0040	RATEFIX	32	Clock rate fix register
A00C0044	GUARD	32	Guard interval register
A00C0048	ESCAPE_REG	32	Escape character register
A00C004C	SLEEP_REG	32	Sleep mode control register
A00C0050	DMA_CON	32	DMA mode control register
A00C0054	RXTRIG	32	RX FIFO trigger threshold
A00C0058	FRACDIV	32	Fractional divisor
A00C005C	RX_TO_CON	32	RX timeout mode control
A00C0060	RX_TOC_DEST	32	RX timeout counter destination value
A00C0070	DEBUG_0_ADDR	32	
A00C0074	DEBUG_1_ADDR	32	
A00C0078	DEBUG_2_ADDR	32	
A00C007C	DEBUG_SEL	32	

A00C0000 RBR RX buffer register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**RBR**							
Type									RU							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	RBR	**RX buffer register**

A00C0004 THR **TX holding register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**THR**							
Type									WO							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	THR	**TX holding register**

A00C0008 DL **Divisor latch** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**DLM**								**DLL**							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15:8	DLM	**Divisor latch [15:8]**
7:0	DLL	**Divisor latch [7:0]**

A00C000C IER **Interrupt enable register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name							**CTSI_RTSI**									**XOFFI**
Type							RW									RW
Reset							0	0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							**ELSI_ERBFI**									**ETBEI**
Type							RW									RW
Reset							0	0								0

Bit(s)	Name	Description
25:24	CTSI_RTSI	**CTS & RTS interrupt** Note: This interrupt is only enabled when hardware flow control is enabled Bit[1] - When a rising edge is detected on the CTS modem control line: 0: No effect 1: Interrupt is generated Bit[0] - When a rising edge is detected on the RTS modem control line: 0: No effect 1: Interrupt is generated
16	XOFFI	**XOFF interrupt** Note: This interrupt is only enabled when software flow control is enabled When an XOFF character is received: 0: No effect 1: Interrupt is generated
9:8	ELSI_ERBFI	**RX interrupt** Bit[1] - When BI, FE, PE, or OE becomes set: 0: No effect 1: Interrupt is generated Bit[0] - When RX buffer register is full or RX FIFO threshold is reached: 0: No effect 1: Interrupt is generated
0	ETBEI	**TX interrupt** When TX holding register is empty or TX FIFO threshold is reached: 0: No effect 1: Interrupt is generated

A00C0010 IIR **Interrupt identification register** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**ID**					
Type											RU					
Rese											0	0	0	0	0	1

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Bit(s)	Name	Description
5:0	ID	**IIR[5:0] Priority Interrupt source** 000001 - No interrupt pending 000110 1 Line Status Interrupt: BI, FE, PE, or OE set in LSR 001100 2 RX data timeout 000100 3 RX data received or RX trigger level reached 000010 4 TX holding register empty or TX trigger level reached 010000 5 Software flow control: receive XOFF 100000 6 Hardware flow control: CTS or RTS rising edge Line status interrupt: RX line status interrupt is generated, if IER[9] and any of BI, FE, PE or OE (LSR[4:1]) are set. The interrupt is cleared by reading the LSR register. RX data timeout interrupt: (RX_TO_MODE = 0) When RX DMA mode is disabled, RX data timeout interrupt is generated, if the following conditions apply: 1. FIFO is not empty. 2. No data is received for four transmission periods. 3. FIFO is not read by the CPU for four transmission periods. The timeout timer restarts upon receipt of a new byte from the RX shift register or upon a CPU read from the RX FIFO. The RX data timeout interrupt is enabled by setting IER[8] to 1 and RX_TO_MODE to 0, and is cleared by reading RX FIFO. When RX DMA mode is enabled, RX data timeout interrupt is generated, if the following conditions apply: 1. FIFO is empty. 2. No data is received for four transmission periods. The timeout timer restarts upon receipt of a new byte from the RX shift register or upon reading the DMA_CON register. The RX data timeout interrupt is enabled by setting IER[8] to 1 and RX_TO_MODE to 0, and is cleared by reading the DMA_CON register. (RX_TO_MODE = 1) When RX DMA mode is disabled, RX data timeout interrupt is generated, if the following conditions apply: 1. FIFO is not empty. 2. No data is received for a certain period (defined by RX_TOC_DEST). 3. FIFO is not read by the CPU for a certain period (defined by RX_TOC_DEST). The timeout timer restarts upon receipt of a new byte from the RX shift register or upon a CPU read from the RX FIFO. The RX data timeout interrupt is enabled by setting IER[8] to 1 and RX_TO_MODE to 1, and is cleared by reading RX FIFO. When RX DMA mode is enabled, RX data timeout interrupt is generated, if the following conditions apply: 1. FIFO is empty. 2. No data is received for a certain period (defined by

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Bit(s)	Name	Description
		RX_TOC_DEST). The timeout timer restarts upon receipt of a new byte from the RX shift register or upon reading the DMA_CON register. The RX data timeout interrupt is enabled by setting IER[8] to 1 and RX_TO_MODE to 1, and is cleared by reading the DMA_CON register. RX-data-received interrupt: A RX-data-received interrupt is generated if IER[8] is set and either RX data are placed in the RX buffer register or the RX trigger level is reached. The interrupt is cleared by reading the RX buffer register or the RX FIFO (if enabled). TX-holding-register-empty interrupt: A TX-holding-register-empty interrupt is generated if IER[0] is set and either the TX holding register is empty or the contents of the TX FIFO are reduced to its trigger level. The interrupt is cleared by writing data to the TX holding register or TX FIFO (if enabled). Software flow control interrupt: A software flow control interrupt is generated if the software flow control is enabled and XOFFI (IER[16]) is set, indicating that an XOFF character has been received. The interrupt is cleared by reading the IIR register. Hardware flow control interrupt: A hardware flow control interrupt is generated if the hardware flow control is enabled and either IER[24] or IER[25] is set, indicating that a rising edge has been detected on RTS or CTS modem control line. The interrupt is cleared by reading the IIR register.

A00C0014 FCR **FIFO control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								CLRT								CLRR
Type								WO								WO
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					RFTL_TFTL											FIFOE
Type					RW											RW
Reset					0	0	0	0								0

Bit(s)	Name	Description
24	CLRT	**Clear TX FIFO** 0: No effect 1: Clear
16	CLRR	**Clear RX FIFO** 0: No effect 1: Clear
11:8	RFTL_TFTL	**RX & TX FIFO trigger threshold** Bit[3:2] - RX FIFO threshold (total 32 bytes): 00: 1

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Bit(s)	Name	Description
		01: 6 10: 12 11: Use RXTRIG register value Bit[1:0] - TX FIFO threshold (total 16 bytes): 00: 1 01: 4 10: 8 11: 14
0	FIFOE	**Enable RX & TX FIFOs** 0: Disable 1: Enable

A00C0018 EFR **Enhanced feature register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name								SEND_XON								SEND_XOFF
Type								WO								WO
Reset								0								0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							HW_FLOW_CONT								SW_FLOW_CONT	
Type							RW								RW	
Reset							0	0							0	0

Bit(s)	Name	Description
24	SEND_XON	**Send XON** Note: effective only when TX software flow control is disabled 0: No effect 1: Auto send one XON character
16	SEND_XOFF	**Send XOFF** Note: effective only when TX software flow control is disabled 0: No effect 1: Auto send one XOFF character
9:8	HW_FLOW_CONT	**Hardware flow control** Bit[1] - TX hardware flow control: 0: Disable TX flow control 1: Enable TX to receive CTS Bit[0] - RX hardware flow control: 0: Disable RX flow control 1: Enable RX to send RTS
1:0	SW_FLOW_CONT	**Software flow control** Bit[1] - TX software flow control: 0: Disable TX flow control 1: Transmit XON/XOFF as flow control byte Bit[0] - RX software flow control: 0: Disable RX flow control 1: Receive XON/XOFF as flow control byte

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A00C001C LCR **Line control register** **00000020**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**SB**			**PAR_STB_WLS**					
Type								RW			RW					
Reset								0			1	0	0	0	0	0

Bit(s)	Name	Description
8	SB	**Set break** 0: No effect 1: TX signal is forced to 0
5:0	PAR_STB_WLS	**Parity, stop bits, & word length setting** Bit[5:3] - Parity type: 000: Even parity 001: Odd parity 010: Parity is forced to 0 011: Parity is forced to 1 100: No parity Bit[2] - Number of stop bits: 0: 1 stop bit 1: 2 stop bits (effective only when word length > 5 bits) Bit[1:0] - Word length: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

A00C0020 MCR **Modem control register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																**XOFF_STATUS**
Type																RU
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**LOOP**								**RTS**
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
16	XOFF_STATUS	**XOFF status**

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Bit(s)	Name	Description
		0: No XOFF character is received 1: An XOFF character is received
8	LOOP	**Enable loop-back mode, i.e. connect TX to RX** Note: hardware flow control will be disabled in loop-back mode 0: Disable 1: Enable
0	RTS	**RTS state** 0: RTS is always 1 1: RTS value will be decided by hardware flow control

A00C0024 XON_XOFF XON & XOFF character 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	XON_CHAR								XOFF_CHAR							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	XON_CHAR	**XON character for software flow control**
7:0	XOFF_CHAR	**XOFF character for software flow control**

A00C0028 LSR Line status register 00000060

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									LSR							
Type									RU							
Reset									0	1	1	0	0	0	0	0

Bit(s)	Name	Description
7:0	LSR	**Line status register** Bit[7] - RX FIFO error: 0: No PE, FE, and BI in the RX FIFO 1: At least one of PE, FE, or BI in the RX FIFO Bit[6] - TX holding register/TX FIFO and TX shift register are empty: 0: Empty conditions below are not met. 1: Set whenever the TX FIFO and the TX shift register are empty (FIFOs are enabled), or TX holding register and TX shift register

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Bit(s)	Name	Description
		are empty (FIFOs are disabled). Bit[5] - TX holding register is empty or TX FIFO is below threshold: 0: Reset whenever the contents of the TX FIFO are above threshold (FIFOs are enabled), or TX holding register is not empty (FIFOs are disabled). 1: Set whenever the contents of the TX FIFO are below threshold (FIFOs are enabled), or TX holding register is empty and ready to accept new data (FIFOs are disabled). Bit[4] - Break interrupt (BI): 0: Reset by letting the CPU read this register. 1: Set if the RX is held in 0 state for more than one transmission period (START bit + DATA bits + PARITY + STOP bits). Bit[3] - Framing error (FE): 0: Reset by letting the CPU read this register. 1: Set if received data do not have a valid STOP bit. Bit[2] - Parity error (PE): 0: Reset by letting the CPU read this register. 1: Set if received data do not have a valid parity bit. Bit[1] - Overrun error (OE): 0: Reset by letting the CPU read this register. 1: Set if the RX buffer register is overwritten (FIFOs are disabled), or both RX FIFO and RX shift register is full (FIFOs are enabled). Note that if OE occurs and UART is still receiving data in FIFO mode, the data in the FIFO will be kept but the RX shift register will be overwritten. Bit[0] - Data ready (DR): 0: Reset by letting the CPU read the RX buffer or by reading all the FIFO bytes. 1: Set if the RX buffer register or FIFO is not empty.

A00C002C SCR **Scratch register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SCR							
Type									RW							
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7:0	SCR	**General purpose read/write register** Note: This register will not be reset

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A00C0030 AUTOBAUD_CON Auto-baud control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																AUTOBAUD_SLEEP_ACK
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AUTOBAUD_SEL								AUTOBAUD_EN
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
16	AUTOBAUD_SLEEP_ACK	**Enable auto-baud sleep acknowledgement** Note: effective only when auto-baud is enabled 0: Enable 1: Disable
8	AUTOBAUD_SEL	**Auto-baud mode** 0: Support standard baud rate 1: Support non-standard baud rate
0	AUTOBAUD_EN	**Enable auto-baud** 0: Disable 1: Enable

A00C0034 HIGHSPEED High speed mode register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															SPEED	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	SPEED	**Sample counter period** 0: 16*(baud pulse) 1: 8*(baud pulse) 2: 4*(baud pulse) 3: (SAMPLE_REG.SAMPLE_COUNT+1)*(baud pulse)

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Bit(s)	Name	Description
		Note: Baud rate = system clock frequency/speed/DL

A00C0038 SAMPLE_REG **Sample counter & sample point register** **0000FF00**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SAMPLE_POINT								SAMPLE_COUNT							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	SAMPLE_POINT	**Sample point** Note: Usually (SAMPLE_COUNT-1)/2 without decimal. Effective only when SPEED = 3
7:0	SAMPLE_COUNT	**Sample counter** Note: Effective only when SPEED = 3

A00C003C AUTOBAUD_REG **Auto-baud monitor register** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					BAUD_STAT								BAUD_RATE			
Type					RU								RU			
Reset					0	0	0	0					0	0	0	0

Bit(s)	Name	Description
11:8	BAUD_STAT	**Auto-baud state** 0: Detecting 1: AT_7N1 2: AT_7O1 3: AT_7E1 4: AT_8N1 5: AT_8O1 6: AT_8E1 7: at_7N1 8: at_7E1 9: at_7O1 10: at_8N1 11: at_8E1

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Bit(s)	Name	Description
		12: at_8O1 13: Detection fail
3:0	BAUD_RATE	**Auto-baud rate** 0: 115,200 1: 57,600 2: 38,400 3: 19,200 4: 9,600 5: 4,800 6: 2,400 7: 1,200 8: 300

A00C0040 RATEFIX **Clock rate fix register** **0000000D**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																RATEFIX
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								AUTOBAUD_RATEFIX			AUTOBAUD_SAMPLE					
Type								RW			RW					
Reset								0			0	0	1	1	0	1

Bit(s)	Name	Description
16	RATEFIX	**System clock rate for TX/RX** 0: 26MHz 1: 13MHz
8	AUTOBAUD_RATEFIX	**System clock rate for auto-baud detection** 0: 26MHz 1: 13MHz
5:0	AUTOBAUD_SAMPLE	**Clock division for auto-baud detection** If AUTOBAUD_CON.AUTOBAUD_SEL = 0 AUTOBAUD_RATE_FIX = 0: 0xd AUTOBAUD_RATE_FIX = 1: 0x6 If AUTOBAUD_CON.AUTOBAUD_SEL = 1 { RATE_FIX, AUTOBAUD_RATEFIX } = { 0, 0 }: 0xf { RATE_FIX, AUTOBAUD_RATEFIX } = { 0, 1 }: 0x7 { RATE_FIX, AUTOBAUD_RATEFIX } = { 1, 0 }: 0x1f { RATE_FIX, AUTOBAUD_RATEFIX } = { 1, 1 }: 0xf

A00C0044 GUARD **Guard interval register** **0000000F**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												**GUARD**				
Type												RW				
Reset												0	1	1	1	1

Bit(s)	Name	Description
4:0	GUARD	**Guard interval setting** Bit[4] - Enable guard interval: 0: No guard interval 1: Add guard interval after stop bit Bit[3:0] - Guard interval count value

A00C0048 ESCAPE_REG Escape character register 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**ESC_EN**	**ESC_CHAR**							
Type								RW	RW							
Reset								0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	ESC_EN	**Enable escape character** 0: Disable 1: Enable
7:0	ESC_CHAR	**Escape character setting**

A00C004C SLEEP_REG Sleep mode control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																**SLEEP_EN**
Type																RW
Rese																0

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Bit(s)	Name	Description
0	SLEEP_EN	**sleep mode flow control** 0: No active flow control when the chip enters sleep mode. 1: Active hardware flow control (assert RTS) or software flow control (send XOFF) when the chip enters sleep mode. Release hardware flow control (de-assert RTS) when the chip wakes up. However, for software control, XON should be sent manually when awakened (can use the SEND_XON register).

A00C0050 DMA_CON DMA mode control register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																FIFO_LSR_SEL
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TX_DMA_EN								RX_DMA_EN
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
16	FIFO_LSR_SEL	**FIFO LSR mode** 0: LSR holds the 1st line status error state until you read the LSR register 1: LSR updates automatically
8	TX_DMA_EN	**Enable TX DMA mode** 0: Disable 1: Enable
0	RX_DMA_EN	**Enable RX DMA mode** 0: Disable 1: Enable

A00C0054 RXTRIG RX FIFO trigger threshold 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RXTRIG			
Type													RW			
Rese													0	0	0	0

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Bit(s)	Name	Description
3:0	RXTRIG	**RX FIFO trigger threshold** Note: effective only when RFTL = 3

A00C0058 FRACDIV Fractional divisor 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FRACDIV									
Type							RW									
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	FRACDIV	**Fractional divisor** Note: effective only when SPEED = 3. Add sampling count (+1) for corresponding data bit

A00C005C RX_TO_CON RX timeout mode control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								TO_CNT_AUTORST								RX_TO_MODE
Type								RW								RW
Reset								0								0

Bit(s)	Name	Description
8	TO_CNT_AUTORST	**Time-out counter auto reset** 0: Reset the RX timeout interrupt manually (see IIR for more details) 1: RX timeout counter is reset automatically
0	RX_TO_MODE	**RX timeout mode** 0: Timeout when RX is idle for 4 characters 1: Timeout when RX is idle for a certain period of time (defined by RX_TOC_DEST)

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A00C0060 RX_TOC_DEST RX timeout counter destination value 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_TOC_DEST															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	RX_TOC_DEST	**RX timeout counter destination value** Note: effective only when RX_TO_CON[0] = 1

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27. Real Time Clock (RTC)

27.1. Introduction

The Real-Time Clock (RTC) module provides time and data information and 32.768kHz (32K) clock source. The clock is selected between three clock sources: one external (XOSC32) and two internal (DCXO32, EOSC32). A strapping bit, SLOW_SRC_B, is added for the 32K crystal existence information. The clock source is from the external oscillator when SLOW_SRC_B is 0.

The RTC block has an independent power supply. When the chip is in OFF mode or DEEPSLEEP mode, a dedicated regulator supplies power to the RTC block. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core. Regular interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches the maximum, such as 59 for seconds and minutes, 23 for hours, etc. The year span is supported up until 2127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

27.2. Abbreviations

Table 11.2-1 lists the abbreviations used in this chapter.

Table 27.2-1. Abbreviations

Abbreviation	Full Name
OSC32	32768 Hz oscillator
XOSC32	32768 Hz crystal oscillator
DCXO32	32768 Hz digitally controlled crystal oscillator
EOSC32	32768 Hz embedded oscillator
EINT	External interrupt
GPIO	General purpose input-output

27.3. Features

- There is one real time timer, two alarm timers and a dedicated EINT channel in the RTC.
- The RTC can generate wake up events to the Cortex M4, SPM and PMU to wake up the system.
- There are three 32K clock sources, external 32K crystal (XOSC32), internal oscillator (EOSC32) and divided 32K from 26MHz crystal (DCXO32).

27.4. Block diagram

The block diagram for the RTC is shown in Figure 27.4-1.

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Figure 27.4-1. RTC block diagram

27.5. Functions

Function	Description
32K clock source	• Internal 32K clock: o There are two internal 32k clock sources. One is from internal oscillator (EOSC) , the other is a divided 32k clock from DCXO 26MHz clock (DCXO) • External 32K clock: o The external 32K clock can be provided by an external 32K crystal.
Wake-up event	• Note, all wake-up events can only be used after enabling the corresponding wake-up events at the first boot up. • Alarm: RTC can generate wake-up events or interrupts when the real-time timer is the same as the alarm setting. • Tick: RTC can generate wake-up events or interrupts when the timer reaches the maximum timeout value. • EINT: An external interrupt can be input from RTC_EINT.
Peripheral	• RTC_EINT: This port defaults in input mode and will be pulled down. An external interrupt can be input to wake-up the system. Several configurations are provided to detect the external signal. User can define to trigger the EINT at rising or falling edge, disable/enable de-bounce feature (takes 4 32k clock cycles), and disable/enable synchronization feature (takes 2 32k clock cycles). • RTC_GPIO_0: This port defaults in output mode and will output low. This port can be selected to output user-defined values or the wake-up event value.

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28. Power Management Unit and Low Power Control System

28.1. Overview

The power management unit (PMU) controls the power supply of the chip, including the baseband, processor, memory, PA, SIM and more. There are two power input source for MT2625:

- For RTC timer control and PMU control (AVDD33_LDO, AVDD33_CORE, and AVDD33_VRF):

It's operated by wider input voltage range (2.1V to 3.63V), to support real time clock control and alarm logic, and to provide AP low power system control. The PMU contains Under-Voltage Lockout (UVLO) circuit, several low drop-out regulators (LDOs), efficiency buck converters and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection and low output noise.

- For PA and SIM control (AVDD33_VPA, AVDD33_VSIM):

A single regulated 3.3V power supply is required for the MT2625. It could be from external DC-DC converter to convert higher voltage supply to 3.3V or boost from a lower voltage supply to 3.3V. The low drop-out voltage output LDOs support 1.8V and 2.9V two types of SIM applications. The efficiency PA buck converters with efficient line/load regulation, high ripple rejection support wider range (0.5 to 2.8V) of power amplifiers.

Due to ultra-low input voltage and low current consumption, the battery lifetime is enhanced by using portable batteries.

28.2. Low-power operating mode

The MT2625 power state diagram is illustrated in Figure 28.2-1. In **ACTIVE** mode, the frequency of CM4 can be configured as 104 MHz or 26 MHz. When the system is in the idle condition, it can enter **IDLE** or **LIGHTSLEEP** mode. In **IDLE** mode, the PMU keeps current voltage and all CM4 and peripherals are in the idle state, which can be returned to **ACTIVE** state by any interrupt event. But if the system goes to **LIGHTSLEEP** mode, the PMU can be changed to the low power mode to further lower the current consumption with 32K clock only. The **DEEPSLEEP** mode provides a lower current consumption than **LIGHTSLEEP** mode with the ability for 8K SRAM retention. It is suitable for the applications which could be idle in a long period but also need to keep data in SRAM. It is controlled by SW to enter the **DEEPSLEEP** mode and exited by RTC or PWRKEY event. The **PSM** mode (Power Save Mode, also called **OFF)** is similar with **DEEPSLEEP** mode but no data can keep in SRAM. In **SHIPPING** mode, there are only some logics to detect the power on condition and lowest power consumption in this mode.

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Figure 28.2-1. MT2625 power states

28.3. Power performance summary

Table 28.3-1 list the current consumption of some basic scenarios at VBAT domain. Note that the current measurement condition is under the typical condition of process, voltage, and temperature.

Table 28.3-1. Current consumption in different power modes

Operation Mode		Test Conditions[1]	Current Consumptions [2]	Unit
Power Mode	Scenario			
SHIP	SHIP	• Shipping mode	< 0.3	uA
PSM (OFF)	PSM (OFF)	• RTC Timer • XTAL 32Khz	2.6	uA
DEEPSLEEP	DEEPSLEEP	• RTC Timer • 8KB SRAM data retention	3.4	uA

[1] No SYSRAM data is retained in these scenarios.

[2] Conditions: VBAT @3.3V, VDDIO @3.3V, 25°C, Typical corner IC, XTAL@26Mhz.

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Operation Mode		Test Conditions[1]	Current	Unit
		• XTAL 32Khz		
LIGHTSLEEP	**LIGHTSLEEP**	• CM4 in sleep state • TCM 96KByte SRAM is retained • XTAL 32Khz	50uA[3]	uA
ACTIVE[4]	**RX**	• RX	15	mA
	TX	• MB Band1 • TX 23dBm	291	mA
		• MB Band1 • TX 10dBm	64	mA
		• MB Band1 • TX 0dBm	31	mA
		• LB Band8 • TX 23dBm	333	mA
		• LB Band8 • TX 10dBm	60	mA
		• LB Band8 • TX 0dBm	34	mA

28.4. PMU architecture for low power system

The 3.3V power source is directly supplied to the switching regulator, digital IOs and RF-related circuit. It is converted from 3.3V by the PMU for low voltage circuits. The built-in CORE and RF buck convert to 1.1V and 1.3V for digital core, RF circuits. The four LDOs are VIO18, VSIM, VSRAM_RTC and VFEM. VCORE buck converter and VSRAM stands for digital core 1.3V to 0.7V low power mode control. VRF, VPA buck converter and VFEM stands for RF, PA and front-end module control, and VIO18 stands for IOs, PLL, and internal/external memory LDO.

In **ACTIVE/ IDLE** mode, the buck converter converts 1.1V output in MT2625. It can operate in PFM mode for optimize the power consumption. With an external on-board LC filter (2.2uH inductor and 10uF cap), it outputs a low ripple 1.1V to core system. In **ACTIVE/ IDLE** mode, VIO18 outputs 1.8V for whole chip digital IOs, memory, PLL used.

In **LIGHTSLEEP** mode back to **ACTIVE** mode, VCORE buck output voltage will converts to 1.1V from 0.7V to core system by DVFS (Dynamic Voltage Frequency Scale) control. While MT2625 is in **LIGHTSLEEP** mode, VSRAM will reduce its output level from 1.1V to 0.775V for internal retention SRAM power. VIO18 keeps outputs 1.8V for whole chip digital IOs, memory, PLL used.

In **DEEPSLEEP** mode (Deep Sleep Mode), VCORE, VRF, VPA, VFEM and VIO18 will be shut down. During this mode, only some PMU logics, RTC timer controller and retention LDO VSRAM_RTC are alive 0.775V to keep lower current consumption. During this mode, only some PMU logics, RTC timer controller and retention SRAM are alive to keep lower current consumption.

[3] The current includes SIM card current 25uA.

[4] The current includes PA SKY68018-11.

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In **OFF** mode, it's similar with **DEEPSLEEP** mode but turn off the VSRAM_RTC regulator and SRAM application.

In **SHIPPING** mode, all regulator and VSRAM_RTC will be shut down to efficiently enhance the battery life.

The MT2625 PMU power grid is illustrated in Figure 28.4-1.

Figure 28.4-1. MT2625 PMU power grid

Table 28.4-1. BUCK / LDO characteristiclists the internal BUCK/ LDO output range, default voltage setting and the output current capabilities.

Table 28.4-1. BUCK / LDO characteristic

Regulator Type	Name	Output Voltage Range(V)	Default ON Voltage(V)	IOUT (mA)
BUCK	VCORE	0.7 ~ 1.3	1.2	150
	VRF	1.3	Default off	35
	VPA	0.5 ~ 2.8	Default off	500
LDO	VIO18	1.8	1.8	180
	VFEM	1.8	Default off	35
	VSRAM_RTC	0.775 / 1.1	Default off	5

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Regulator Type	Name	Output Voltage Range(V)	Default ON Voltage(V)	IOUT (mA)
	VSIM	1.8 / 2.8 / 2.9	Default off	60 / 100/ 60

28.5. PMU functional description

28.5.1. UVLO

28.5.1.1. Under-voltage lockout (UVLO)

The UVLO state in PMU prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by AVDD33_LDO. It ensures that the device is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator that ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMU will be turned off by itself, except for RTC macro and PMU always on domain, it will draw low quiescent current. In order to optimize the low power performance, there is no UVLO in DEEPSLEEP and LIGHTSLEEP mode.

Parameter	Min.	Typical	Max.	Unit
Under voltage falling threshold	1.80	1.85	1.90	V
Under voltage rising threshold	2.05	2.10	2.15	V

28.5.2. PWRKEY

Pulling PWRKEY low is a typical method to turn on the device. The system reset ends when all default-on regulators are sequentially turned on. After that, the SOC will send the power ready signal back to PMU for acknowledgement. To successfully power on the device, PWRKEY should be kept low until PMU receives power ready from the AP.

Parameter	Conditions	Min.	Typical	Max.	Unit
PWRKEY					
High voltage		0.7*AVDD33_LDO			V
Low voltage				0.3* AVDD33_LDO	V
De-bounce time	OFF/DEEPSLEEP to ACTIVE	16	32	48	msec
	SHIPPING to ACTIVE	1	2	3	sec

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28.5.3. Long press shutdown

Long press shutdown is default feature to provide a reliable hardware reset to force shutdown PMU without removing the battery, which detects negative pulse width on PWRKEY.

28.5.3.1. Long-Press Shutdown Timer:

When negative pulse width is greater than the timer setting, the PMU will force shutdown to OFF mode.

There are four types of Long-press shutdown key-pressed timing select timer options:

- 5s
- 8s **(DEFAULT)**
- 11s
- 25s

Note: The timing variation is +/-50% for this feature.

28.5.3.2. Long-Press Shutdown Function Type:

For default setting, after long press shutdown, if PWRKEY not released, enters re-power on by sequence and long-press shutdown periodically.

There are three options for PWRKEY Long Press Function for users:

- Disabled. No long press shutdown function.
- Enabled. The power on sequence will start after the PWRKEY is released and then pressed again.
- Enabled. The power on sequence will start after the PWRKEY de-bounce time, if PWRKEY is kept low. **(DEFAULT)**

28.5.4. Thermal shutdown

This is the hardware thermal protection function and PMU will shut down immediately when the function is triggered.

If the chip reaches 150°C (±15°C), the PMU enters OFF mode by immediate power-off sequence. It will auto recover by power-on sequence, if the chip temperature is cooled down below 110 °C. (Register option for 120 °C recovery).

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28.5.5. Shipping mode

User can enter SHIPPING mode by setting register, and PMU will power-off. When in SHIPPPING mode, please note that if PWRKEY is pressed over 2 seconds, the PMU will re-power-on to normal mode by normal power-on sequence.

28.5.6. SYSRSTB cold-reset application

SYSRSTB is used to reset the PMU when system hangs. This function is default ON by hardware.

Cold reset function can be triggered by pressing SYSRSTB for over 32ms de-bounce time. When cold reset is triggered, the system is shut down immediately with immediate-off sequence. The shutdown time is 20ms to make sure analog circuits discharge completely. Then the PMU will do the normal power on. Note that the cold reset cannot be triggered in SHIPPING mode.

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