rand

simple loop

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	8326	3002	235	2717	11328	73.4993	26.5007
100	8555	2773	64	2609	11328	75.5208	24.4792
150	8608	2715	12	2503	11328	76.0328	23.9672
200	8613	2715	12	2503	11328	76.0328	23.9672

blocked

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	3513864	8496	6046	2400	3522360	99.7588	0.2412
100	3517054	5306	3483	1723	3522360	99.8494	0.1506
150	3517997	4363	2750	1463	3522360	99.8761	0.1239
200	3518531	3829	2269	1360	3522360	99.8913	0.1087

matmul

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	2054243	995053	974547	20456	3049296	67.3678	32.6322
100	2725929	323367	318911	4356	3049296	89.3954	10.6046
150	2952926	96370	94457	1763	3049296	96.8396	3.1604
200	2993130	56166	54550	1416	3049296	98.1581	1.8419

stack

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	7350	434	191	193	7784	94.4245	5.5755
100	7557	227	20	107	7784	97.0838	2.9162
150	7597	187	0	37	7784	97.5976	2.4024
200	7606	178	0	0	7784	97.7133	2.2867

fifo

simple loop

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	8383	2945	183	2712	11328	74.0025	25.9975
100	8566	2762	46	2616	11328	75.6179	24.3821
150	8609	2719	17	2552	11328	75.9975	24.0025
200	8618	2710	12	2498	11328	76.077	23.923

blocked

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	3515847	6513	4305	2158	3522360	99.8151	0.1849
100	3518018	4342	2776	1466	3522360	99.8767	0.1233
150	3518127	4233	2666	1417	3522360	99.8798	0.1202
200	3519196	3164	1862	1102	3522360	99.9102	0.0898

matmul

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	1922048	1127248	1104630	22568	3049296	63.0325	36.9675
100	1965746	1083550	1071756	11694	3049296	64.4656	35.5344
150	3014895	34401	33085	1166	3049296	98.8718	1.1282
200	3015427	33869	32514	1155	3049296	98.8893	1.1107

stack

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate

50	7417	367	132	185	7784	95.2852	4.7148
100	7568	216	3	113	7784	97.2251	2.7749
150	7592	192	0	42	7784	97.5334	2.4666
200	7606	178	0	0	7784	97.7133	2.2867

clock

simple loop

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	8544	2784	89	2645	11328	75.4237	24.5763
100	8631	2697	10	2587	11328	76.1917	23.8083
150	8643	2685	1	2534	11328	76.2977	23.7023
200	8643	2685	0	2485	11328	76.2977	23.7023

blocked

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	3516737	5623	3155	2418	3522360	99.8404	0.1596
100	3518012	4348	2591	1657	3522360	99.8766	0.1234
150	3518588	3772	2547	1075	3522360	99.8929	0.1071
200	3519154	3206	1918	1088	3522360	99.909	0.091

matmul

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	2008106	1041190	1040025	1115	3049296	65.8547	34.1453
100	2047515	1001781	1000583	1098	3049296	67.1471	32.8529
150	3014663	34633	33386	1097	3049296	98.8642	1.1358
200	3016433	32863	31568	1095	3049296	98.9223	1.0777

stack

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	7488	296	82	164	7784	96.1973	3.8027
100	7587	197	5	92	7784	97.4692	2.5308
150	7594	190	0	40	7784	97.5591	2.4409
200	7606	178	0	0	7784	97.7133	2.2867

lru

simple loop

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	8549	2779	86	2643	11328	75.4679	24.5321
100	8639	2689	3	2586	11328	76.2624	23.7376
150	8644	2684	0	2534	11328	76.3065	23.6935
200	8644	2684	0	2484	11328	76.3065	23.6935

blocked

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	3517236	5124	2716	2358	3522360	99.8545	0.1455
100	3518583	3777	2583	1094	3522360	99.8928	0.1072
150	3518594	3766	2542	1074	3522360	99.8931	0.1069
200	3518692	3668	2395	1073	3522360	99.8959	0.1041

matmul

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	2008108	1041188	1040021	1117	3049296	65.8548	34.1452

100	2042860	1006436	1005238	1098	3049296	66.9945	33.0055
150	3016435	32861	31616	1095	3049296	98.9223	1.0777
200	3016450	32846	31551	1095	3049296	98.9228	1.0772

stack

mem size	Hit count	Miss count	Clean evict	Dirty evic	Total references	Hit rate	Miss rate
50	7492	292	85	157	7784	96.2487	3.7513
100	7594	190	2	88	7784	97.5591	2.4409
150	7604	180	0	30	7784	97.6876	2.3124
200	7606	178	0	0	7784	97.7133	2.2867

The fourth program of my choice

The program I choose is stack loop(tr-stack.ref), although it has a similar implementation of heap loop, but produces a constant and high hit rate for all page replacement algorithms due to its stack implementation.

Comparison of four page replacements algorithms

From data we can observe the ranking of overall hit rates for these four algorithms is rand < fifo <= clock <= lru
and in theory arc should have the best performance of hit rates. We can find rand overall has poor performance due
to its implementation, but in one exception - tr-matmul because the data in matmul is randomly generated. ARC have
the best performance in theory, since arc combines LRU and LFU. Fifo overall perform worse then clock, lru and arc
because rather than take the first to replace for fifo, others algo have a higher chance to keep better canadiantes.

How LRU and ARC behave as the size of memory increases.

From data we can observe that the hit rate of lru increases as the size of memory increases. In theory as the
size of memory increases, the algo can use a bigger recent use tables, more precise predictions will be made,
that generates lru to perform better with a bigger memory. ARC combines LRU and LFU, a bigger memory also
generates arc to perform better.