ICM-42688-P Datasheet

High Precision 6-Axis MEMS MotionTracking™ Device

ICM-42688-P HIGHLIGHTS

The ICM-42688-P is a 6-axis MEMS MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer. It has a configurable host interface that supports I3C℠, I²C and SPI serial communication, features a 2 kB FIFO and 2 programmable interrupts with ultra-low-power wake-on-motion support to minimize system power consumption.

ICM-42688-P supports highly accurate external clock input, that helps to reduce system level sensitivity error, improve orientation measurement from gyroscope data, reduce ODR sensitivity to temperature and device to device variation.

The device includes industry first 20-bits data format support in FIFO for high-data resolution. This FIFO format encapsulates 19-bits of gyroscope data and 18-bits of accelerometer data.

Other industry-leading features include InvenSense on-chip APEX Motion Processing engine for gesture recognition, activity classification, and pedometer, along with programmable digital filters, and an embedded temperature sensor.

The device supports a VDD operating range of 1.71V to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

ICM-42688-P FEATURES

- Gyroscope Noise: 2.8 mdps/√Hz & Accelerometer Noise: 70 µg/√Hz
  - Low-Noise mode 6-axis current consumption of 0.88 mA
- User selectable Gyro Full-scale range (dps): ± 15.6/31.2/62.5/125/250/500/1000/2000
- User selectable Accelerometer Full-scale range (g): ± 2/4/8/16
- User-programmable digital filters for gyro, accel, and temp sensor
- APEX Motion Functions:
  - Pedometer, Tilt Detection, Tap Detection
  - Wake on Motion, Raise to Wake/Sleep, Significant Motion Detection
- Host interface: 12.5 MHz I3C℠, 1 MHz I²C, 24 MHz SPI

APPLICATIONS

- AR/VR Controllers
- Head Mounted Displays
- Wearables
- Sports
- Robotics
- IoT Applications

BLOCK DIAGRAM

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-42688-P†	–40°C to +85°C	2.5x3mm 14-Pin LGA

†Denotes RoHS and Green-Compliant Package

TDK-INVENSENSE SENSORS FOR SMARTPHONE, MOBILE & IOT APPLICATIONS

Parameter	ICM-40607 Sensorhub	ICM-42605 Sensorhub	ICM-42686-P Handheld Action	ICM-42688-P HMD & Robotics
GYRO Noise (mdps/rt-Hz)	7	3.8	5.3	2.8
GYRO Offset Temp Stability (mdps/°C)	±30	±20	±10	±5
GYRO Range & Resolution	±2000dps; 16-bits	±2000dps; 16-bits	±4000dps; 16/19-bits	±2000dps; 16/19-bits
ACCEL Noise (µg/rt-Hz)	110	70	70	AXY: 65; AZ: 70
ACCEL Range & Resolution	±16g; 16-bits	±16g; 16-bits	±32g; 16/18-bits	±16g; 16/18-bits
ODR & Sample Synch	8kHz; No RTC	8kHz; No RTC	32kHz; RTC	32kHz; RTC

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ICM-42688-P 数据手册

高精度6轴MEMS运动追踪™ 设备

ICM-42688-P亮点

ICM-42688-P是一款六轴MEMS运动追踪设备，集成了三轴陀螺仪和三轴加速度计。它具有可配置主机接口，支持I3C℠、I²C和SPI串行通信，配备2 kB FIFO和2个可编程中断，并具有超低功耗运动唤醒功能，以最小化系统功耗。

ICM-42688-P支持高精度外部时钟输入，有助于降低系统级灵敏度误差，提升基于陀螺仪数据的方向测量精度，减少输出数据速率对温度和设备间差异的敏感性。

该设备在FIFO中首次实现行业领先的20位数据格式支持，以实现高数据分辨率。此FIFO格式封装了19位陀螺仪数据和18位加速度计数据。

其他行业领先特性包括应美盛片上APEX运动处理引擎，支持手势识别、活动分类和计步器功能，同时配备可编程数字滤波器和嵌入式温度传感器。

该设备支持1.71V至3.6V的VDD工作电压范围，以及独立的1.71V至3.6V数字IO电源VDDIO。

ICM-42688-P 特性

- 陀螺仪噪声：2.8 mdps/√Hz & 加速度计噪声：70 µg/√Hz
  - 低噪声模式六轴电流消耗为0.88 毫安
- 用户可选陀螺仪满量程范围（度每秒）：± 15.6/31.2/62.5/125/250/500/1000/2000
- 用户可选加速度计满量程
  量程(重力加速度): ± 2/4/8/16
- 用户可编程数字滤波器（适用于陀螺仪、加速度计及温度传感器）
- APEX运动功能:
  - 计步器、倾斜检测、敲击检测
  - 运动唤醒、抬手唤醒/睡眠、大幅运动检测
- 主机接口: 12.5 兆赫 I3C℠, 1 兆赫 I²C, 24 MHz SPI

应用

- AR/VR控制器
- 头戴式显示器
- 可穿戴设备
- 体育
- 机器人技术
- 物联网应用

框图

订购信息

PART	温度范围	封装
ICM-42688-P †	–40摄氏度 至 +85摄氏度	2.5x3毫米 14针脚 LGA

†表示符合有害物质限制指令和环保合规封装

TDK-INVENSENSE传感器 适用于智能手机、移动设备及物联网应用

参数	ICM-40607 传感器中心	ICM-42605 传感器中心	ICM-42686-P 手持动作	ICM-42688-P 头
陀螺仪噪声（毫度每秒每平方根赫兹）	7	3.8	5.3	2.8
陀螺仪偏移温度稳定性（毫度每秒每摄氏度）	±30	±20	±10	±5
陀螺仪范围与分辨率	±2000度每秒；16位	±2000度每秒；16位	±4000度每秒；16/19位	±2000度每秒；16/19位
加速度计噪声（微克每平方根赫兹）	110	70	70	AXY: 65; AZ: 70
加速度计范围与分辨率	±16重力加速度; 16位	±16重力加速度; 16位	±32重力加速度; 16/18位	±16重力加速度; 16/18位
输出数据速率与采样同步	8千赫；无实时时钟	8千赫；无实时时钟	32千赫；实时时钟	32千赫；实时时钟

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-42688-P Single-Interface MotionTracking device. The device is housed in a small 2.5x3x0.91 mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-42688-P is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.91 mm (14-pin LGA) package. It also features a 2K-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-42688-P, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports eight programmable full-scale range settings from ±15.625dps to ±2000dps, and the accelerometer supports four programmable full-scale range settings from ±2g to ±16g.

ICM-42688-P also supports external clock input for highly accurate 31kHz to 50kHz clock, that helps to reduce system level sensitivity error, improve orientation measurement from gyroscope data, reduce ODR sensitivity to temperature and device to device variation.

The device includes industry first 20-bits data format support in FIFO for high-data resolution. This FIFO format encapsulates 19-bits of gyroscope data and 18-bits of accelerometer data for high precision applications. Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3C^{SM}, I^{2}C and SPI serial interfaces, a VDD operating range of 1.71 V to 3.6 V, and a separate VDDIO operating range of 1.71 V to 3.6 V.

The host interface can be configured to support I3C^{SM} slave, I^{2}C slave, or SPI slave modes. The I3C^{SM} interface supports speeds up to 12.5MHz (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode), the I^{2}C interface supports speeds up to 1 MHz, and the SPI interface supports speeds up to 24 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.91 mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- AR/VR Controllers
- Head Mounted Displays
- Wearables
- Sports
- Robotics

1 简介

1.1 目的与范围

本文档为产品规格，提供关于ICM-42688-P单接口运动追踪设备的描述、规格及设计相关信息。该设备采用小型2.5x3x0.91毫米14引脚LGA封装。

1.2 产品概述

ICM-42688-P是一款六轴运动追踪设备，集成了三轴陀螺仪和三轴加速度计，采用2.5x3x0.91毫米（14引脚LGA）小型封装。该设备还配备2K字节FIFO，可减少串行总线接口的数据流量，并通过让系统处理器突发读取传感器数据后进入低功耗模式来降低功耗。ICM-42688-P凭借其六轴集成技术，使制造商无需进行昂贵且复杂的分立器件选择、认证和系统级集成，从而确保为消费者提供最佳运动性能。

该陀螺仪支持八种可编程全量程范围设置，从±15.625度每秒至±2000度每秒；加速度计支持四种可编程全量程范围设置，从±2重力加速度至±16重力加速度。

ICM-42688-P还支持外部时钟输入，可提供31千赫至50千赫的高精度时钟，有助于降低系统级灵敏度误差，提升基于陀螺仪数据的方向测量精度，并减少输出数据速率对温度及设备间差异的敏感性。

该设备在FIFO中首次实现了行业领先的20位数据格式支持，以实现高数据分辨率。此FIFO格式封装了19位陀螺仪数据和18位加速度计数据，适用于高精度应用。其他行业领先特性包括片上16位模数转换器、可编程数字滤波器、嵌入式温度传感器及可编程中断。设备具备I3C^{SM}、I^{2}C与SPI串行接口，VDD工作电压范围为1.71伏至3.6伏，独立的VDDIO工作电压范围同样为1.71伏至3.6伏。

主机接口可配置为支持I3C^{SM} 从模式、I^{2}C从模式或SPI从模式。I3C^{SM} 接口支持最高12.5兆赫速率（SDR模式下数据速率达12.5兆比特每秒，DDR模式下为25兆比特每秒），I^{2}C接口支持最高1兆赫速率，而SPI接口支持最高24兆赫速率。

通过利用其专利且经过量产验证的CMOS-MEMS制造平台（该平台通过晶圆级键合将MEMS晶圆与配套CMOS电子器件集成），应美盛已将封装尺寸缩小至2.5x3x0.91毫米（14引脚LGA）的占位面积和厚度，从而提供了一种非常小巧、高性能且低成本的封装。该设备通过支持20,000*g*冲击的可靠性，展现出高鲁棒性。

1.3 应用

- AR/VR控制器
- 头戴式显示器
- 可穿戴设备
- 体育
- 机器人技术

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-42688-P includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with programmable full-scale range of ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees/sec
- Low Noise (LN) power mode support
- Digitally-programmable low-pass filters
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-42688-P includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with programmable full-scale range of ±2*g*, ±4*g* ±8*g* and ±16*g*
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 MOTION FEATURES

ICM-42688-P includes the following motion features, also known as APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen)

- Pedometer: Tracks Step Count, also issues Step Detect interrupt
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35° for more than a programmable time
- Raise to Wake/Sleep: Gesture detection for wake and sleep events. Interrupt is issued when either of these two events are detected
- Tap Detection: Issues an interrupt when a tap is detected, along with the tap count
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold
- Significant Motion Detection: Detects Significant Motion if Wake on Motion events are detected during a programmable time window

2.4 ADDITIONAL FEATURES

ICM-42688-P includes the following additional features:

- External clock input supports highly accurate clock input from 31kHz to 50kHz, helps to reduce system level sensitivity error, improve orientation measurement from gyroscope data, reduce ODR sensitivity to temperature and device to device variation
- 2K byte FIFO buffer enables the applications processor to read the data in bursts
- 20-bits data format support in FIFO for high-data resolution
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- 12.5MHz I3C^{SM} (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode) / 1 MHz I^{2}C / 24 MHz SPI slave host interface
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.91 mm (14-pin LGA)
- 20,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

2 特性

2.1 陀螺仪特性

ICM-42688-P中的三轴MEMS陀螺仪包含广泛特性：

- 数字输出X、Y、Z轴角速率传感器（陀螺仪），具有可编程全量程范围，可选±15.625、 ±31.25、±62.5、 ±125、 ±250、 ±500、 ±1000和±2000 度/秒
- 低噪声（LN）电源模式支持
- 数字可编程低通滤波器
- 出厂校准灵敏度比例因子
- 自检

2.2 加速度计特性

ICM-42688-P中的三轴MEMS加速度计包含广泛特性：

- 数字输出X、Y和Z轴加速度计，可编程全量程范围为±2重力加速度、±4重力加速度 ±8重力加速度 和±16重力加速度
- 支持低噪声(LN)和低功耗(LP)电源模式
- 用户可编程中断
- 运动唤醒中断功能，用于应用处理器的低功耗操作
- 自检

2.3 运动特性

ICM-42688-P包含以下运动特性，也称为顶点（**高级计步器**与**事件检测—新一代**）

- 计步器：追踪步数计数，同时触发步进检测中断
- 倾斜检测：当倾斜角度超过35° 并持续超过可编程时间时触发中断
- 抬手唤醒/睡眠：用于唤醒和睡眠事件的手势检测。检测到任一事件时触发中断
- 敲击检测：检测到轻敲时触发中断，并记录轻触计数
- 运动唤醒：当加速度计数据超过可编程阈值时检测运动
- 大幅运动检测：如果在可编程时间窗口内检测到运动唤醒事件，则判定为大幅运动

2.4 附加特性

ICM-42688-P包含以下附加特性：

- 外部时钟输入支持31千赫至50千赫的高精度时钟信号，有助于降低系统级灵敏度误差，提升基于陀螺仪数据的方向测量精度，减少输出数据速率对温度及设备间差异的敏感性
- 2K字节FIFO缓冲区支持应用处理器以突发模式读取数据
- 先进先出（FIFO）支持20位数据格式，实现高数据分辨率
- 用户可编程数字滤波器，适用于陀螺仪、加速度计和温度传感器
- 12.5兆赫I3C^{SM} （SDR模式下数据速率高达12.5兆比特每秒，DDR模式下25兆比特每秒）/1兆赫I^{2}C/24兆赫SPI从机接口
- 数字输出温度传感器
- 便携设备用最小最薄LGA封装：2.5x3x0.91毫米（14引脚LGA）
- 可承受20,000 *g*冲击
- 微机电系统结构采用晶圆级气密封装与键合
- 符合有害物质限制指令与环保合规要求

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_FS_SEL=0		±2000		º/s	2
	GYRO_FS_SEL =1		±1000		º/s	2
	GYRO_FS_SEL =2		±500		º/s	2
	GYRO_FS_SEL =3		±250		º/s	2
	GYRO_FS_SEL =4		±125		º/s	2
	GYRO_FS_SEL =5		±62.5		º/s	2
	GYRO_FS_SEL =6		±31.25		º/s	2
	GYRO_FS_SEL =7		±15.625		º/s	2
Gyroscope ADC Word Length	Output in two's complement format		16		bits	2, 5
Sensitivity Scale Factor	GYRO_FS_SEL=0		16.4		LSB/(º/s)	2
	GYRO_FS_SEL =1		32.8		LSB/(º/s)	2
	GYRO_FS_SEL =2		65.5		LSB/(º/s)	2
	GYRO_FS_SEL =3		131		LSB/(º/s)	2
	GYRO_FS_SEL =4		262		LSB/(º/s)	2
	GYRO_FS_SEL =5		524.3		LSB/(º/s)	2
	GYRO_FS_SEL =6		1048.6		LSB/(º/s)	2
	GYRO_FS_SEL =7		2097.2		LSB/(º/s)	2
Sensitivity Scale Factor Initial Tolerance	Component and Board-level, 25°C		±0.5		%	1
Sensitivity Scale Factor Variation Over Temperature	0°C to +70°C		±0.005		%/ºC	3
Nonlinearity	Best fit straight line; 25°C		±0.1		%	3
Cross-Axis Sensitivity	Board-level		±1.25		%	3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Board-level, 25°C		±0.5		º/s	3
ZRO Variation vs. Temperature	0°C to +70°C		±0.005		º/s/ºC	3
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz		0.0028		º/s /√Hz	1
Total RMS Noise	Bandwidth = 100 Hz		0.028		º/s-rms	4
Gyroscope Mechanical Frequencies		25	27	29	KHz	1
Low Pass Filter Response	ODR < 1kHz	5		500	Hz	2
	ODR ≥ 1kHz	42		3979	Hz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		30		ms	3
Output Data Rate		12.5		32000	Hz	2

Table 1. Gyroscope Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not tested in production.
4. Calculated from Rate Noise Spectral Density.
5. 20-bits data format supported in FIFO, see section 6.1.

3 电气特性

3.1 陀螺仪规格

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	MIN	TYP	MAX	单位	注释
陀螺仪灵敏度						
全量程范围	陀螺仪满量程选择=0_ _		±2000		º/s	2
	陀螺仪_满量程_选择 =1		±1000		º/s	2
	陀螺仪_满量程_选择 =2		±500		º/s	2
	陀螺仪_满量程_选择 =3		±250		º/s	2
	陀螺仪_满量程_选择 =4		±125		º/s	2
	陀螺仪_满量程_选择 =5		±62.5		º/s	2
	陀螺仪_满量程_选择 =6		±31.25		º/s	2
	陀螺仪_满量程_选择 =7		±15.625		º/s	2
陀螺仪ADC字长	二进制补码格式输出		16		bits	2, 5
灵敏度比例因子	陀螺仪满量程选择=0_ _		16.4		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择 =1		32.8		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择=2		65.5		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择=3		131		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择=4		262		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择 =5		524.3		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择 =6		1048.6		最小有效位/(度/秒)	2
	陀螺仪_满量程_选择 =7		2097.2		最小有效位/(度/秒)	2
灵敏度比例因子初始容差	元件和板级，25摄氏度		±0.5		%	1
灵敏度比例因子随温度	0摄氏度至+70摄氏度		±0.005		%/ºC	3
非线性	最佳拟合直线；25摄氏度		±0.1		%	3
交叉轴灵敏度	板级		±1.25		%	3
零速率输出（ZRO）						
初始零速率输出容差	板级，25摄氏度		±0.5		º/s	3
零速率输出随温度变化	0摄氏度至+70摄氏度		±0.005		度/秒/摄氏度	3
其他参数						
速率噪声谱密度	@ 10赫兹		0.0028		o/s /√赫兹	1
总均方根噪声	带宽 = 100 赫兹		0.028		度/秒-均方根	4
陀螺仪机械频率		25	27	29	KHz	1
低通滤波器响应	输出数据速率 < 1千赫	5		500	Hz	2
	输出数据速率 ≥ 1千赫	42		3979	Hz	2
陀螺仪启动时间	从陀螺仪启用到陀螺仪驱动就绪的时间		30		ms	3
输出数据速率		12.5		32000	Hz	2

表1. 陀螺仪规格

注释：

1. 在生产中测试。
2. 设计保证。
3. 源自部件验证或特性分析，未在生产中测试。
4. 根据速率噪声谱密度计算。
5. 先进先出支持20位数据格式，详见第6.1节。

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	ACCEL_FS_SEL =0			±16		*g*	2
	ACCEL_FS_SEL =1			±8		*g*	2
	ACCEL_FS_SEL =2			±4		*g*	2
	ACCEL_FS_SEL =3			±2		*g*	2
ADC Word Length	Output in two's complement format			16		bits	2, 5
Sensitivity Scale Factor	ACCEL_FS_SEL =0			2,048		LSB/*g*	2
	ACCEL_FS_SEL =1			4,096		LSB/*g*	2
	ACCEL_FS_SEL =2			8,192		LSB/*g*	2
	ACCEL_FS_SEL =3			16,384		LSB/*g*	2
Sensitivity Scale Factor Initial Tolerance	Component and Board-level, 25°C			±0.5		%	1
Sensitivity Change vs. Temperature	-40°C to +85°C			±0.005		%/ºC	3
Nonlinearity	Best Fit Straight Line, ±2g			±0.1		%	3
Cross-Axis Sensitivity	Board-level			±1		%	3
ZERO-G OUTPUT							
Initial Tolerance	Board-level, all axes			±20		m*g*	3
Zero-G Level Change vs. Temperature	-40°C to +85°C			±0.15		m*g*/ºC	3
OTHER PARAMETERS							
Power Spectral Density	@ 10 Hz	X and Y-axis		65		µ*g*/√Hz	1
		Z-axis		70		µ*g*/√Hz	1
RMS Noise	Bandwidth = 100 Hz	X and Y-axis		0.65		mg-rms	4
		Z-axis		0.70		mg-rms	4
Low-Pass Filter Response	ODR < 1kHz		5		500	Hz	2
	ODR ≥ 1kHz		42		3979	Hz	2
Accelerometer Startup Time	From sleep mode to valid data			10		ms	3
Output Data Rate			1.5625		32000	Hz	2

Table 2. Accelerometer Specifications

Notes:

1. Tested in production.
2. Guaranteed by design.
3. Derived from validation or characterization of parts, not tested in production.
4. Calculated from Power Spectral Density.
5. 20-bits data format supported in FIFO, see section 6.1.

3.2 加速度计规格

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件		MIN	TYP	MAX	单位	注释
加速度计灵敏度							
全量程范围	加速度计_FS_选择 =0			±16		*g*	2
	加速度计满量程选择 =1			±8		*g*	2
	加速度计满量程选择 =2			±4		*g*	2
	加速度计满量程选择 =3			±2		*g*	2
ADC字长	二进制补码格式输出			16		bits	2, 5
灵敏度比例因子	加速度计满量程选择 =0			2,048		最低有效位/*g*	2
	加速度计满量程选择 =1			4,096		最低有效位/重力加速度	2
	加速度计_FS_选择 =2			8,192		最低有效位/重力加速度	2
	加速度计_FS_选择 =3			16384		最低有效位/*g*	2
灵敏度比例因子初始容差	元件和板级，25摄氏度			±0.5		%	1
灵敏度随温度变化	-40摄氏度至+85摄氏度			±0.005		%/ºC	3
非线性	最佳拟合直线, ±2重力加速度			±0.1		%	3
交叉轴灵敏度	板级			±1		%	3
零重力输出							
初始容差	板级, 所有轴			±20		m*g*	3
零重力水平随温度变化	-40摄氏度 至 +85摄氏度			±0.15		米重力加速度/ºC	3
其他参数							
功率谱密度	@ 10赫兹	X和Y轴		65		µ重力加速度/√赫兹	1
		Z轴		70		µ*g*/√赫兹	1
均方根噪声	带宽 = 100 赫兹	X和Y轴		0.65		毫克-均方根	4
		Z轴		0.70		毫克-均方根	4
低通滤波器响应	输出数据速率 < 1千赫		5		500	Hz	2
	输出数据速率 ≥ 1千赫		42		3979	Hz	2
加速度计启动时间	从睡眠模式到有效数据			10		ms	3
输出数据率			1.5625		32000	Hz	2

表2. 加速度计规格

注释：

1. 在生产中测试。
2. 设计保证。
3. 源自部件验证或特性分析，未在生产中测试。
4. 根据功率谱密度计算。
5. 先进先出支持20位数据格式，详见第6.1节。

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		0.88		mA	2
	3-Axis Accelerometer		0.28		mA	2
	3-Axis Gyroscope		0.73		mA	2
Full-Chip Sleep Mode	At 25ºC		7.5		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

3.3 电气规格

3.3.1 直流电气特性

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	MIN	TYP	MAX	单位	注释
电源电压						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
电源电流						
低噪声模式	6轴陀螺仪+ 加速度计		0.88		mA	2
	三轴加速度计		0.28		mA	2
	三轴陀螺仪		0.73		mA	2
全芯片睡眠模式	在25摄氏度		7.5		µA	2
温度范围						
指定温度范围	性能参数不适用 超出指定温度范围	-40		+85	°C	1

表3. 直流电气特性

注释：

1. Guaranteed by design.
2. 源自部件验证或特性分析，未在生产中测试。

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		3	ms	1
Power Supply Noise			10		mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output			0		LSB	3
ADC Resolution	Output in two's complement format		16		bits	2
ODR	With Filter	25		8000	Hz	2
Room Temperature Offset	25°C	-5		5	°C	3
Stabilization Time				14000	µs	2
Sensitivity	Untrimmed		132.48		LSB/°C	1
Sensitivity for FIFO data			2.07		LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	int_tpulse_duration= 0 , 1 (100us, 8us) ;	8		100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage		-0.5 V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5 V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4 V V_{OL}=0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	CLKSEL=`2b00 or gyro inactive; 25°C	-3		+3	%	1
	CLK_SEL=`2b01 and gyro active; 25°C	-1.5		+1.5	%	1
Frequency Variation over Temperature	CLK_SEL=`2b00 or gyro inactive; -40°C to +85°C			±3	%	1
	CLK_SEL=`2b01 and gyro active; -40°C to +85°C			±2	%	1
EXTERNAL CLOCK SOURCE						
Clock Frequency		31	32	50	kHz	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Based on characterization. Not tested in production.
2. Guaranteed by design.
3. Production tested.

3.3.2 交流电气特性

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	MIN	TYP	MAX	单位	注释
电源						
电源斜坡时间	单调斜坡。斜坡速率为10百分比至90百分比终值	0.01		3	ms	1
电源噪声			10		mV 峰峰值	1
温度传感器						
工作范围	环境温度	-40		85	°C	1
25°C输出			0		LSB	3
ADC分辨率	二进制补码格式输出		16		bits	2
ODR	带滤波器	25		8000	Hz	2
室温偏移	25°C	-5		5	°C	3
稳定时间				14000	µs	2
灵敏度	未修剪		132.48		LSB/°C	1
FIFO数据灵敏度			2.07		LSB/°C	1
上电复位						
寄存器读/写启动时间	从上电开始			1	ms	1
输入²C 地址						
输入²C 地址	安培 地址0 = 0_ AP_地址0 = 1		1101000 1101001			
数字输入(FSYNC, SCLK, SDI, CS)						
V_{IH}, 高电平输入电压		0.7*VDDIO			V	1
V_{IL}, 低电平输入电压				0.3*VDDIO	V	
C_I, 输入电容			< 10		pF	
数字输出 (串行数据输出, INT1, INT2)						
V_{OH}, 高电平输出电压	R_{LOAD}=1 兆欧姆;	0.9*VDDIO			V	1
V_{OL1}, 低电平输出电压	R_{LOAD}=1 兆欧姆;			0.1倍VDDIO	V	
$V_{OL.INT}$, 内部低电平输出电压	OPEN=1, 0.3毫安吸收电流			0.1	V	
输出漏电流	OPEN=1		100		nA	
t_{INT}, 内部脉冲宽度	中断_脉冲时间_持续时间= 0 , 1 (100微秒, 8微秒) ;	8		100	µs	
输入²C 输入/输出 (3CL, SDA)						
伏特$_{IL}$, 低电平输入电压		-0.5 伏特		0.3*VDDIO	V	1
伏特$_{IH}$, 高电平输入电压		0.7倍VDDIO		VDDIO + 0.5 伏特	V	
V_{hys}, 滞后			0.1倍VDDIO		V	
V_{OL}, 低电平输出电压	3 毫安灌电流	0		0.4	V	
输入$_{OL}$, 低电平输出电流	伏特$_{OL}$=0.4 伏特 伏特$_{OL}$=0.6 伏特		3 6		mA mA	
输出漏电流			100		nA	
技术$_{of}$, 输出从伏特$_{IHmax}$ 到伏特$_{ILmax}$的下降时间	C_b 总线电容（单位：皮法）	20+0.1C_b		300	ns	
内部时钟源						
时钟频率初始容差	CLKSEL=`2b00或陀螺仪未激活；25摄氏度	-3		+3	%	1
	CLK_SEL=`2b01且陀螺仪激活；25摄氏度	-1.5		+1.5	%	1
温度变化引起的频率变化	CLK_SEL=`2b00 或陀螺仪未激活；-40°C 至 +85°C			±3	%	1
	CLK_SEL=`2b01 且陀螺仪激活；-40°°C 至 +85°°C			±2	%	1
外部时钟源						
时钟频率		31	32	50	kHz	1

表4. 交流电气特性

注释：

1. 基于特征描述。未在生产中测试。
2. 设计保证。
3. 生产测试。

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.26			µs	1
t_{LOW}, SCL Low Period		0.5			µs	1
t_{HIGH}, SCL High Period		0.26			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.26			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		50			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF			120	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF			120	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.5			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		0.5			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.45	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.45	µs	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

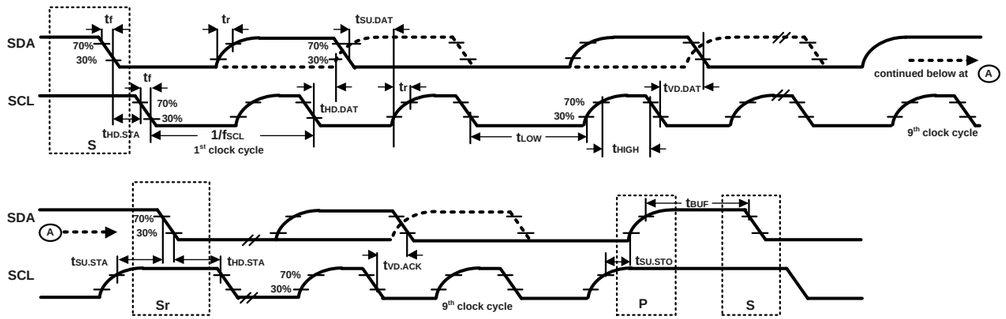


Figure 1. I²C Bus Timing Diagram

3.4 输入²电容时序特性分析

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	Min	典型值	Max	单位	注释
I²C 时序	**I²C 快速模式增强版**					
f_{SCL}, SCL 时钟频率				1	MHz	1
$t_{HD.STA}$, (重复)起始条件保持时间		0.26			µs	1
t_{LOW}, SCL 低电平周期		0.5			µs	1
t_{HIGH}, SCL高电平周期		0.26			µs	1
$t_{SU.STA}$, 重复起始条件建立时间		0.26			µs	1
$t_{HD.DAT}$, SDA数据保持时间		0			µs	1
$t_{SU.DAT}$, SDA数据建立时间		50			ns	1
t_r, SDA和SCL上升时间	C_b 总线电容从10到400皮法			120	ns	1
t_f, SDA和SCL下降时间	C_b 总线电容从10到400皮法			120	ns	1
$t_{SU.STO}$, 停止条件建立时间		0.5			µs	1
t_{BUF}, 停止与起始之间的总线空闲时间 条件		0.5			µs	1
C_b, 每条总线线路的容性负载			< 400		pF	1
$t_{VD.DAT}$, 数据有效时间				0.45	µs	1
$t_{VD.ACK}$, 数据有效确认时间				0.45	µs	1

表5. I²C 时序特性

注释:

1. 基于5个部件在评估板或插座上安装后，在不同温度和电压下的表征结果

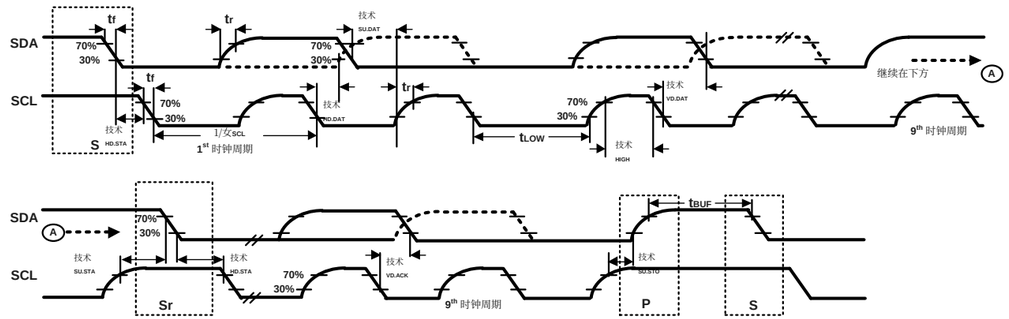


图1. I²C 总线时序图

3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			24	MHz	1
t_{LOW}, SCLK Low Period		17			ns	1
t_{HIGH}, SCLK High Period		17			ns	1
$t_{SU.CS}$, CS Setup Time		39			ns	1
$t_{HD.CS}$, CS Hold Time		18			ns	1
$t_{SU.SDI}$, SDI Setup Time		13			ns	1
$t_{HD.SDI}$, SDI Hold Time		8			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF			21.5	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	3.5			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				28	ns	1
t_{Fall}, SCLK Fall Time				16	ns	2
t_{Rise}, SCLK Rise Time				16	ns	2

Table 6. 4-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on design and device characterization

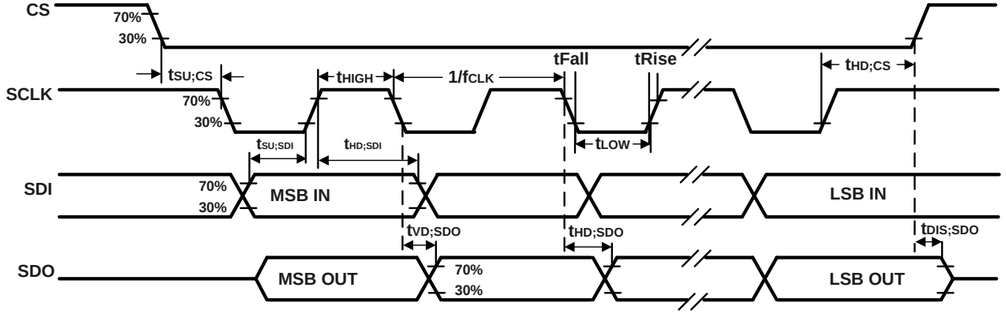


Figure 2. 4-Wire SPI Bus Timing Diagram

3.5 SPI时序特性分析 - 4线SPI模式

第4.2节的典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	MIN	TYP	MAX	单位	注释
SPI时序						
f_{SPC}, SCLK 时钟频率	默认			24	MHz	1
t_{LOW}, SCLK 低电平周期		17			ns	1
t_{HIGH}, SCLK 高电平周期		17			ns	1
$t_{SU.CS}$, CS 建立时间		39			ns	1
$t_{HD.CS}$, CS保持时间		18			ns	1
$t_{SU.SDI}$, SDI建立时间		13			ns	1
$t_{HD.SDI}$, SDI保持时间		8			ns	1
$t_{VD.SDO}$, SDO有效时间	C_{load} = 20 皮法			21.5	ns	1
$t_{HD.SDO}$, SDO保持时间	C_{load} = 20 皮法	3.5			ns	1
$t_{DIS.SDO}$, SDO输出禁用时间				28	ns	1
t_{Fall}, SCLK下降时间				16	ns	2
t_{Rise}, SCLK上升时间				16	ns	2

表6. 4线SPI时序特性（24MHz操作）

注释：

1. 基于5个部件在评估板或插座上安装后，在不同温度和电压下的表征数据
2. 基于设计和设备特性

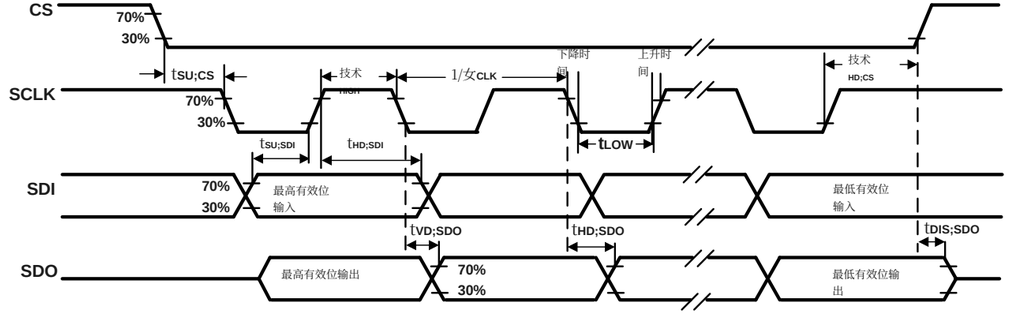


图2. 4线SPI总线时序图

3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SPC}, SCLK Clock Frequency	Default			24	MHz	1
t_{LOW}, SCLK Low Period		17			ns	1
t_{HIGH}, SCLK High Period		17			ns	1
$t_{SU.CS}$, CS Setup Time		39			ns	1
$t_{HD.CS}$, CS Hold Time		5			ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		13			ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		8			ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 20 pF			18.5	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 20 pF	3.5			ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time				28	ns	1
t_{Fall}, SCLK Fall Time				16	ns	2
t_{Rise}, SCLK Rise Time				16	ns	2

Table 7. 3-Wire SPI Timing Characteristics (24-MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on design and device characterization

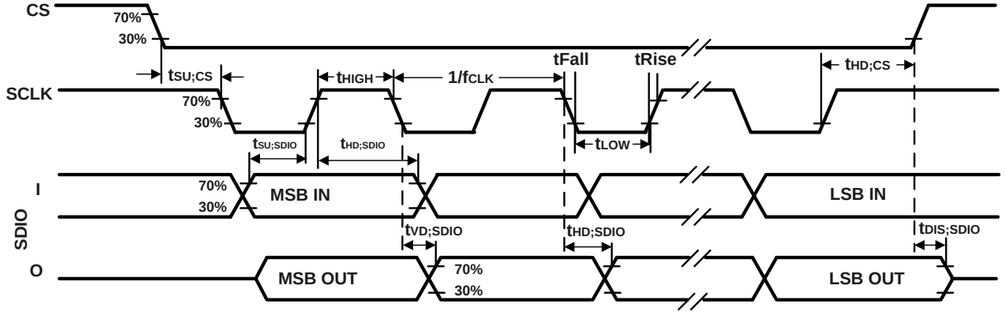


Figure 3. 3-Wire SPI Bus Timing Diagram

3.6 SPI时序特性分析 - 3线SPI模式

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	MIN	TYP	MAX	单位	注释
SPI时序						
f_{SPC}, SCLK时钟频率	默认			24	MHz	1
t_{LOW}, SCLK低电平周期		17			ns	1
t_{HIGH}, SCLK高电平周期		17			ns	1
$t_{SU.CS}$, 片选信号建立时间		39			ns	1
$t_{HD.CS}$, CS保持时间		5			ns	1
$t_{SU.SDIO}$, SDIO输入建立时间		13			ns	1
$t_{HD.SDIO}$, SDIO输入保持时间		8			ns	1
$t_{VD.SDIO}$, SDIO输出有效时间	C_{load} = 20 皮法			18.5	ns	1
$t_{HD.SDIO}$, SDIO输出保持时间	C_{load} = 20 皮法	3.5			ns	1
$t_{DIS.SDIO}$, SDIO输出禁用时间				28	ns	1
t_{Fall}, SCLK下降时间				16	ns	2
t_{Rise}, SCLK上升时间				16	ns	2

表7. 3线SPI时序特性（24MHz操作）

注释:

1. 基于5个部件在评估板或插座中安装时的温度和电压表征
2. 基于设计和设备特性

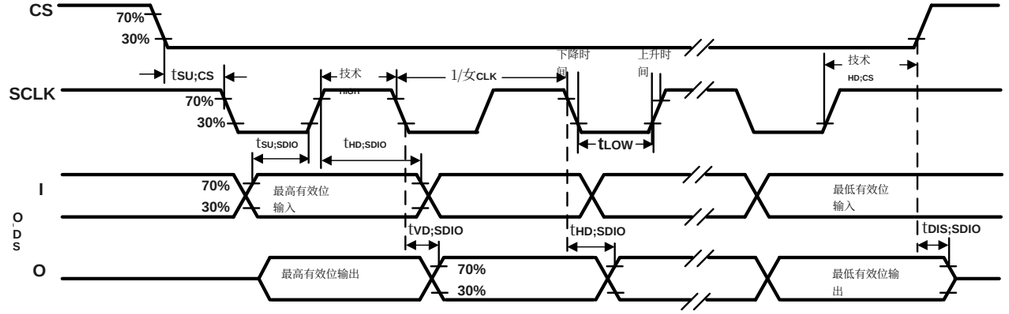


图3. 3线SPI总线时序图

3.7 RTC (CLKIN) TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8 V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
RTC (CLKIN) TIMING						
F_{RTC}, RTC Clock Frequency	Default	31	32	50	kHz	
$t_{HIGHRTC}$, RTC Clock High Period		1			µs	
$t_{RiseRTC}$, RTC Clock Rise Time		5		500	ns	
$t_{FallRTC}$, RTC Clock Fall Time		5		500	ns	

Table 8. RTC Timing Characteristics

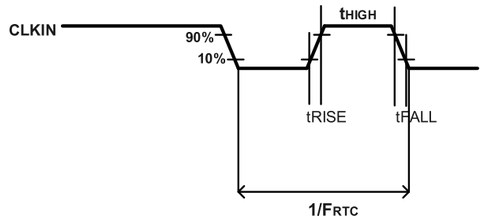


Figure 4. RTC Timing Diagram

3.7 实时时钟 (CLKIN) 时序特性

第4.2节典型工作电路，VDD = 1.8 伏特，VDDIO = 1.8 伏特，温度$_A$=25摄氏度，除非另有说明。

参数	条件	MIN	TYP	MAX	单位	注释
实时时钟 (CLKIN) 时序						
女$_{RTC}$, RTC时钟频率	默认	31	32	50	kHz	
技术$_{HIGHRTC}$, RTC时钟高电平周期		1			µs	
$t_{RiseRTC}$, RTC时钟上升时间		5		500	ns	
$t_{FallRTC}$, RTC时钟下降时间		5		500	ns	

表8. RTC时序特性

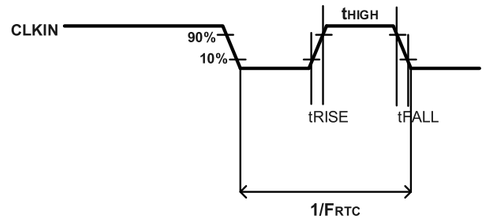


图4. RTC时序图

3.8 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
Input Voltage Level (FSYNC, SCL, SDA)	-0.5 V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 500 V (CDM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

Table 9. Absolute Maximum Ratings

3.8 绝对最大额定值

超过“绝对最大额定值”所列的应力可能会对设备造成永久性损坏。这些仅为应力额定值，并不意味着设备在这些条件下能进行功能操作。长时间暴露于绝对最大额定值条件下可能会影响设备可靠性。

参数	额定值
电源电压, VDD	-0.5 伏特 至 +4 伏特
电源电压, VDDIO	-0.5 伏特 至 +4 伏特
输入电压电平 (帧同步, SCL, SDA)	-0.5 伏特 至 VDDIO + 0.5 伏特
加速度（任意轴，无动力）	20000g持续0.2毫秒
工作温度范围	-40摄氏度至+85摄氏度
存储温度范围	-40摄氏度至+125摄氏度
静电放电（ESD）保护	2千伏（人体模型）； 500伏（充电器件模型）
闩锁	JEDEC II级（2），125°C ±100 毫安

表9. 绝对最大额定值

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

Pin Number	Pin Name	Pin Description
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I^{2}C slave address LSB
2	RESV	No Connect or Connect to GND
3	RESV	No Connect or Connect to GND
4	INT1 / INT	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain) INT: All interrupts mapped to pin 4
5	VDDIO	IO power supply voltage
6	GND	Power supply ground
7	RESV	Connect to GND
8	VDD	Power supply voltage
9	INT2 / FSYNC / CLKIN	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain) FSYNC: Frame sync input; Connect to GND if FSYNC not used CLKIN: External clock input
10	RESV	No Connect or Connect to GND
11	RESV	No Connect or Connect to GND
12	AP_CS	AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface
13	AP_SCL / AP_SCLK	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)

Table 10. Signal Descriptions

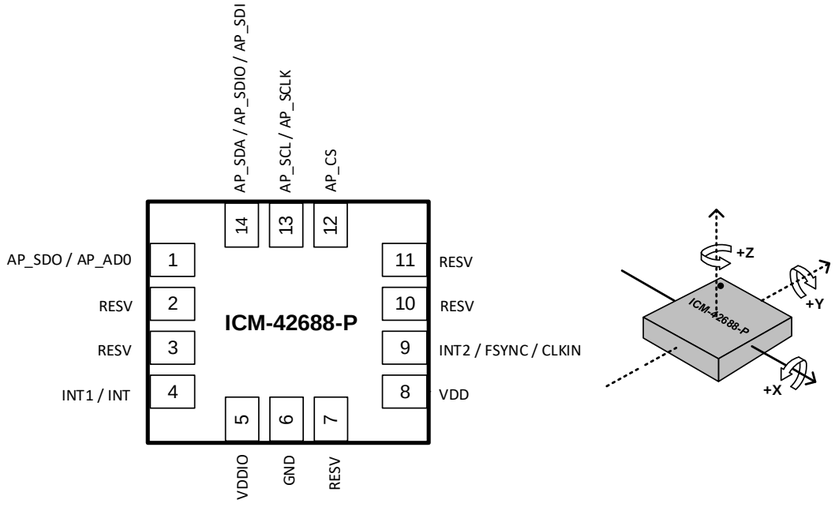


Figure 5. Pin Out Diagram for ICM-42688-P 2.5x3.0x0.91 mm LGA

4 应用信息

4.1 引脚分布图与信号描述

引脚编号	引脚名称	引脚描述
1	安培磷_串行数据输出 / 安培磷_安培数据0	AP_SDO: AP SPI串行数据输出（四线制模式）； AP_AD0: AP I3C^{SM} / I^{2}C 从设备地址最低有效位
2	RESV	不连接或接地
3	RESV	不连接或接地
4	INT1 / INT	INT1: 中断1 (注: INT1可配置为推挽或开漏) INT: 所有中断映射至引脚4
5	VDDIO	IO电源电压
6	GND	电源地
7	RESV	连接到地
8	VDD	电源电压
9	INT2 / FSYNC / CLKIN	INT2: 中断2 (注: INT2可配置为推挽或开漏) FSYNC: 帧同步输入; 若未使用FSYNC则连接到地 CLKIN: 外部时钟输入
10	RESV	不连接或接地
11	RESV	不连接或接地
12	AP片选_	AP SPI片选（AP SPI接口）；若使用AP I3C^{SM} / I^{2}C接口，则连接至VDDIO
13	AP_SCL / AP _SCLK	AP_SCL：AP I3C^{SM} / I^{2}C串行时钟；AP_SCLK：AP SPI串行时钟
14	AP_SDA / AP_ SDIO / AP SDI_	AP_SDA: AP I3C^{SM} /I^{2}C串行数据；AP_SDIO: AP SPI串行数据输入输出（三线制模式）；AP_SDI: AP SPI串行数据输入（四线制模式）

表10. 信号描述

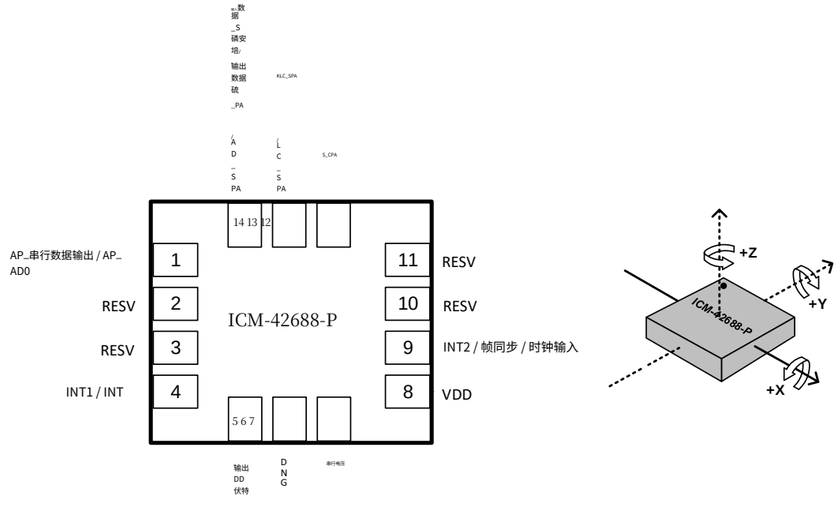


图5. ICM-42688-P 2.5x3.0x0.91毫米LGA封装引脚图

4.2 TYPICAL OPERATING CIRCUIT

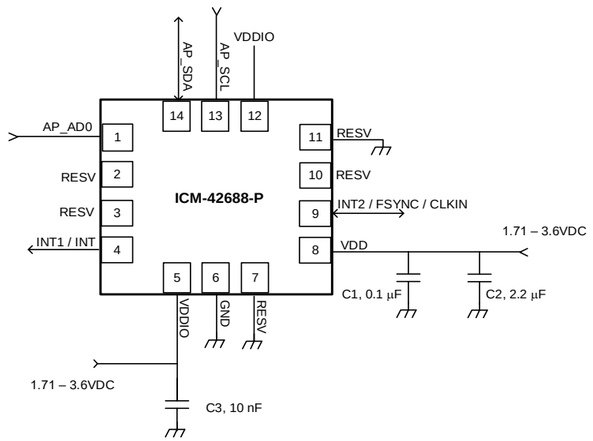


Figure 6. ICM-42688-P Application Schematic (I3C^{SM} / I^{2}C Interface to Host)

Note: I^{2}C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

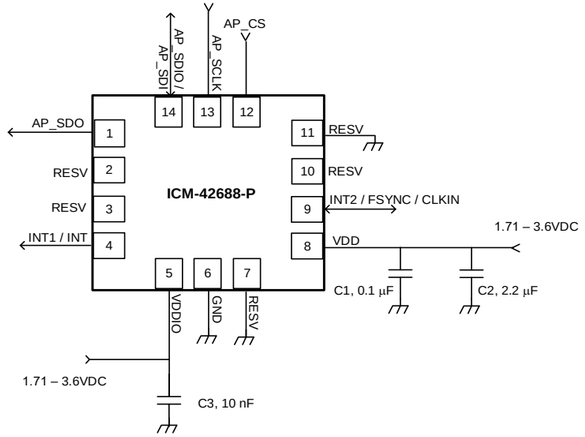


Figure 7. ICM-42688-P Application Schematic (SPI Interface to Host)

4.2 典型工作电路

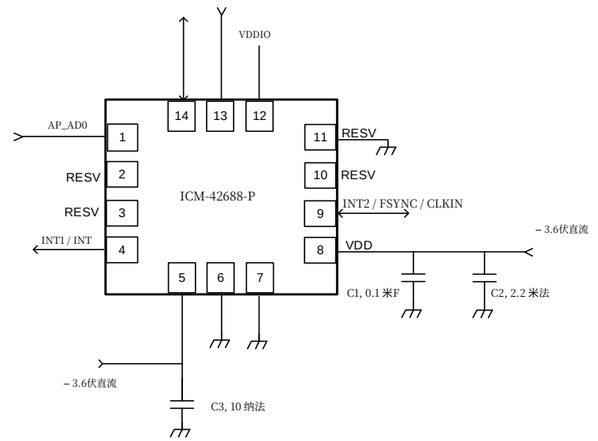


图6. ICM-42688-P应用示意图（I3C^{SM} / I^{2}C接口至主机）

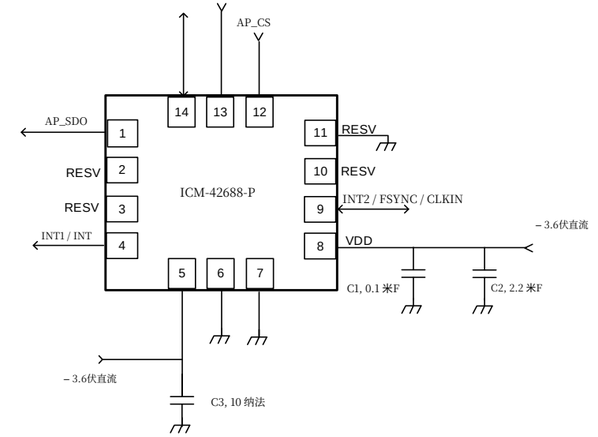


图7. ICM-42688-P应用示意图（SPI接口至主机）

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
VDD Bypass Capacitors	C1 C2	X7R, 0.1µF ±10% X7R, 2.2µF ±10%	1 1
VDDIO Bypass Capacitor	C3	X7R, 10nF ±10%	1

Table 11. Bill of Materials

4.3 外部组件物料清单

组件	标签	规格	数量
VDD旁路电容器	C1 C2	X7R, 0.1µF ±10百分比 X7R, 2.2µF ±10百分比	1 1
VDDIO 旁路电容器	C3	X7R, 10nF ±10百分比	1

表11. 物料清单

4.4 SYSTEM BLOCK DIAGRAM

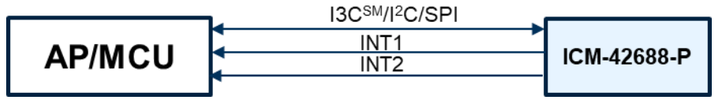


Figure 8. ICM-42688-P System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.5 OVERVIEW

The ICM-42688-P is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
  - 20-bits data format support in FIFO for high-data resolution (see section 6 for details)
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
  - 20-bits data format support in FIFO for high-data resolution (see section 6 for details)
- I3C^{SM}, I^{2}C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-42688-P includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees per second (dps).

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-42688-P includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-42688-P architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g* and ±16*g*.

4.8 I3C^{SM}, I^{2}C AND SPI HOST INTERFACE

The ICM-42688-P communicates to the application processor using an I3C^{SM}, I^{2}C, or SPI serial interface. The ICM-42688-P always acts as a slave when communicating to the application processor.

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

4.4 系统框图

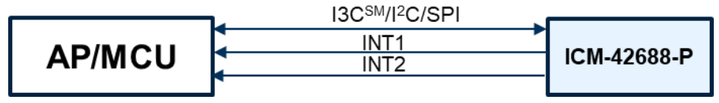


图8. ICM-42688-P系统框图

注：上述框图仅为示例。其他配置选项请参阅引脚输出（章节4.1）。

4.5 概述

ICM-42688-P由以下关键模块和功能组成：

- 三轴MEMS速率陀螺仪传感器，配备16位模数转换器及信号调理功能
  - FIFO中支持20位数据格式以实现高数据分辨率（详情见章节6）
- 三轴MEMS加速度计传感器，配备16位模数转换器及信号调理功能
  - FIFO中支持20位数据格式以实现高数据分辨率（详情见章节6）
- I3C^{SM}, I^{2}C和SPI串行通信接口
- 自检
- 时钟
- 传感器数据寄存器
- FIFO
- 中断
- 数字输出温度传感器
- 偏置和低压差稳压器
- 电荷泵
- 标准电源模式

4.6 三轴MEMS陀螺仪，带16位模数转换器和信号调理

ICM-42688-P包含一个振动式MEMS速率陀螺仪，可检测绕X、Y和Z轴的旋转。当陀螺仪绕任一感应轴旋转时，科里奥利效应会引起振动，该振动由电容拾取检测。产生的信号经过放大、解调和滤波，产生与角速率成比例的电压。该电压通过片上模数转换器（ADC）对每个轴进行采样。陀螺传感器的全量程范围可通过数字编程设置为±15.625、 ±31.25、 ±62.5、 ±125、 ±250、 ±500、 ±1000和±2000 度每秒（dps）。

4.7 三轴MEMS加速度计，配备16位模数转换器及信号调理

ICM-42688-P集成了一款3轴MEMS加速度计。沿特定轴向的加速度会引发微机电系统结构中检测质量的位移，并由电容传感器检测该位移。ICM-42688-P的架构设计降低了加速度计对制造工艺差异及热漂移的敏感性。当设备水平放置时，X轴和Y轴将测得0*g*，Z轴测得+1*g*。加速度计的比例因子已在出厂时校准，且在标称状态下与电源电压无关。数字输出的全量程范围可调整为±2*g*、 ±4*g*、 ±8*g* 及±16*g*。

4.8 I3C^{SM}、I^{2}C与SPI主机接口

ICM-42688-P通过I3C^{SM}、I^{2}C或SPI串行接口与应用处理器通信。在与应用处理器通信时，ICM-42688-P始终作为从设备运行。

4.9 自检

自检功能可测试传感器的机械和电气部分。通过陀螺仪和加速度计自检寄存器，可激活各测量轴的自检功能。

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 CLOCKING

The ICM-42688-P has a flexible clocking scheme, allowing external or internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers.

The CLKIN pin on ICM-42688-P provides the ability to input an external clock. A highly accurate external clock may be used rather than the internal clocks sources, if greater clock accuracy is desired. External clock input supports highly accurate clock input from 31kHz to 50kHz, resulting in improvement of the following:

a) ODR uncertainty due to process, temperature, operating mode (PLL vs. RCOSC), and design limitations. This uncertainty can be as high as ±8% in RCOSC mode and ±1% in PLL mode. The CLKIN, assuming a 50ppm or better 32.768kHz source, will improve the ODR accuracy from ±80,000ppm to ±50ppm in RCOSC mode, or from ±10,000ppm to ±50ppm in PLL mode.
b) System level sensitivity error. Any clock uncertainty directly impacts gyroscope sensitivity at the system level. Sophisticated systems can estimate ODR inaccuracy to some extent, but not to the extent improved by using CLKIN.
c) System-level clock/sensor synchronization. When using CLKIN, the accelerometer and gyroscope are on the same clock as the host. There is no need to continually re-synchronize the sensor data as the sensor sample points and period are known to be in exact alignment with the common system clock.
d) CLKIN helps EIS (Electronic Image Stabilization) performance by providing:
    - Very accurate gyroscope sample points for use during integration to find true angular displacement.
    - Automatic time alignment between the motion sensor and the host and potentially the camera system.
e) Other applications that benefit from CLKIN include navigation, gaming, robotics.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

For internal sources, the only setting supporting specified performance in all modes is option b). It is recommended that option b) be used when using internal clock source.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

当自检激活时，电子元件会驱动传感器动作并产生输出信号。该输出信号用于观测自检响应。

自检响应定义如下：

自检响应 = 启用自检时的传感器输出 – 禁用自检时的传感器输出

当自检响应值处于产品规格规定的最小/最大限制范围内时，该部件即通过自检。若自检响应超出最小/最大值，则判定该部件自检失败。

4.10 时钟

ICM-42688-P采用灵活时钟方案，允许使用外部或内部时钟源为内部同步电路提供时钟。该同步电路包括信号调理和模数转换器，以及各种控制电路和寄存器。

ICM-42688-P的CLKIN引脚支持输入外部时钟。若需更高时钟精度，可采用高精度外部时钟替代内部时钟源。外部时钟输入支持31千赫至50千赫的高精度时钟信号，从而改善以下方面：

a) 因工艺、温度、操作模式（锁相环 vs RC振荡器）及设计限制导致的ODR不确定性。该不确定性在RC振荡器模式下可能高达±8百分比，在锁相环模式下可达±1百分比。若采用50ppm或更高精度的32.768kHz源作为CLKIN输入，可将RC振荡器模式的ODR精度从±80,000ppm提升至±50 ppm，或将锁相环模式的精度从±10,000ppm提升至±50ppm。
b) 系统级灵敏度误差。任何时钟不确定性都会直接影响系统级的陀螺仪灵敏度。复杂系统可以在一定程度上估计ODR不准确性，但无法达到使用时钟输入（CLKIN）带来的改进程度。
c) 系统级时钟/传感器同步。使用时钟输入（CLKIN）时，加速度计和陀螺仪与主机共用一个时钟。由于传感器采样点和周期已知与公共系统时钟完全对齐，因此无需持续重新同步传感器数据。
d) 时钟输入（CLKIN）通过以下方式提升电子图像稳定（EIS）性能：
    - 提供非常精确的陀螺仪采样点，用于积分计算真实角位移。
    - 实现运动传感器与主机（可能还包括摄像系统）之间的自动时间对齐。
e) 其他受益于时钟输入的应用包括导航、游戏、机器人技术。

允许用于生成内部时钟的内部源包括：

a) 内部弛张振荡器
b) 在内部弛张振荡器与陀螺仪MEMS振荡器之间自动选择，以使用最佳可用源

对于内部源，唯一支持所有模式下指定性能的设置是选项b)。建议在使用内部时钟源时采用选项b)。

4.11 传感器数据寄存器

传感器数据寄存器包含最新的陀螺仪、加速度计和温度测量数据。这些是只读寄存器，通过串行接口访问。可随时读取这些寄存器中的数据。

4.12 中断

中断功能通过中断配置寄存器进行配置。可配置的项目包括中断引脚配置、中断锁存和清除方法以及中断触发条件。能够触发中断的项目包括：(1) 时钟发生器锁定到新的参考振荡器（在切换时钟源时使用）；(2) 新数据可用（来自FIFO和数据寄存器）；(3) 加速度计事件中断；(4) FIFO水位标记；(5) FIFO溢出。中断状态可从中断状态寄存器中读取。

4.13 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-42688-P die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature sensor register data TEMP_DATA is updated with new data at max(Accelerometer ODR, Gyroscope ODR).

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 132.48) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA / 2.07) + 25

4.14 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-42688-P.

4.15 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.16 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-42688-P.

Mode	Name	Gyro	Accel
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Power Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Low-Noise Mode	On	Off
6	6-Axis Low-Noise Mode	On	On

Table 12. Standard Power Modes for ICM-42688-P

4.13 数字输出温度传感器

使用片上温度传感器和模数转换器来测量ICM-42688-P芯片温度。模数转换器的读数可从FIFO或传感器数据寄存器中读取。

温度传感器寄存器数据 TEMP_DATA 会在加速度计输出数据速率和陀螺仪输出数据速率的最大值处更新为新数据。

来自传感器数据寄存器的温度数据值可通过以下公式转换为摄氏度：

摄氏度温度= (温度_数据 / 132.48) + 25

存储在先进先出中的温度数据为8位数量，先进先出_温度_数据。可通过以下公式转换为摄氏度：

摄氏度温度= (先进先出_温度_数据 / 2.07) + 25

4.14 偏置与LDO

偏置与LDO部分为ICM-42688-P生成所需的内部电源及参考电压和电流。

4.15 电荷泵

片上电荷泵为MEMS振荡器生成所需的高压。

4.16 标准电源模式

下表列出了ICM-42688-P的用户可访问电源模式。

Mode	Name	Gyro	加速度计
1	睡眠模式	Off	Off
2	待机模式	驱动开启	Off
3	加速度计低功耗模式	Off	循环工作
4	加速度计低噪音模式	Off	On
5	陀螺仪低噪音模式	On	Off
6	六轴低噪音模式	On	On

表12. ICM-42688-P标准电源模式

5 SIGNAL PATH

The following figure shows a block diagram of the signal path for ICM-42688-P.

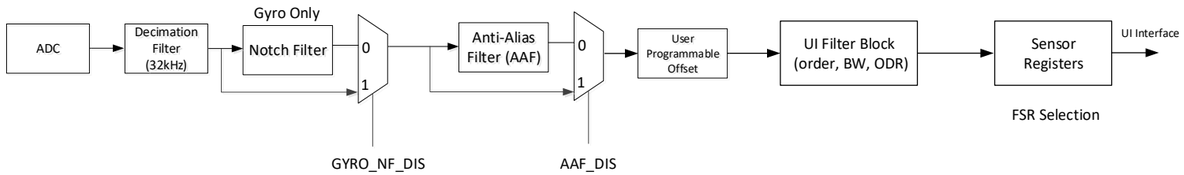


Figure 9. ICM-42688-P Signal Path

The signal path starts with ADCs for the gyroscope and accelerometer. Other components of the signal path are described below in further detail.

5.1 SUMMARY OF PARAMETERS USED TO CONFIGURE THE SIGNAL PATH

The following table shows the parameters that can control the signal path.

Parameter Name	Description
GYRO_AAF_DIS	Disables the Gyroscope Anti Alias Filter (AAF)
GYRO_AAF_DELT GYRO_AAF_DELTSQR GYRO_AAF_BITSHIFT	Three parameters required to program the gyroscope AAF. This is a 2nd order filter with programmable low pass filter. This is a user programmable filter which can be used to select the desired BW. This filter allows trading off RMS noise vs. latency for a given ODR.
ACCEL_AAF_DIS	Disables the Accelerometer Anti Alias Filter
ACCEL_AAF_DEL ACCEL_AAF_DELTSQR ACCEL_AAF_BITSHIFT	Three parameters required to program the accelerometer AAF. This is a 2nd order filter with programmable low pass filter. This is a user programmable filter which can be used to select the desired BW. This filter allows trading off RMS noise vs. latency for a given ODR.
GYRO_NF_DIS	Disables the gyro Notch Filter
GYRO_X/Y/Z_NF_COSWZ GYRO_X/Y/Z_NF_COSWZ_SEL	Factory trimmed parameters, designed to position a Notch at or near the sense peak frequency of Gyro. This allows the user to suppress only sense peak contribution to noise, while still maintaining a low latency high BW/ODR interface from the Sensor. This filter is available only in Gyro, and the parameters for X, Y, and Z are chosen independently.
GYRO_NF_BW_SEL	Factory trimmed parameter to cancel noise created by sense peak from Gyro. This parameter is common to all three axes

5.2 NOTCH FILTER

The Notch Filter is supported only for the gyroscope signal path. The following steps can be used to program the notch filter. Note that the notch filter is specific to each axis in the gyroscope, so the X, Y and Z axis can be programmed independently.

Frequency of Notch Filter (each axis)

To operate the Notch filter, two parameters NF_COSWZ, and NF_COSWZ_SEL must be programmed for each gyroscope axis.

Parameters NF_COSWZ are defined for each axis of the gyroscope as GYRO_X_NF_COSWZ (register bank 1, register 0x0Fh & register 0x12h), GYRO_Y_NF_COSWZ (register bank 1, register 0x10h & register 0x12h), GYRO_Z_NF_COSWZ (register bank 1, register 0x11h & register 0x12h). Note that the parameters have 9-bit values across two different registers.

5 信号路径

下图展示了ICM-42688-P信号路径的框图。

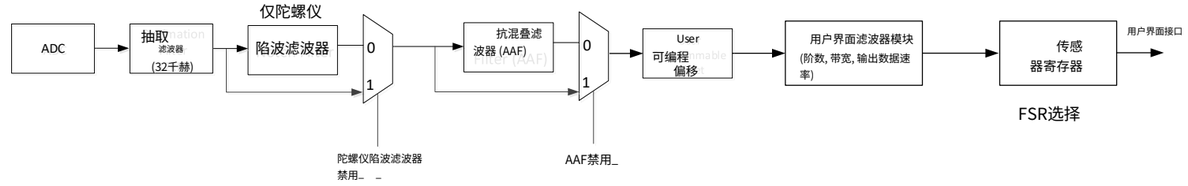


图9. ICM-42688-P信号路径

信号路径始于陀螺仪和加速度计的模数转换器。信号路径的其他组件将在下文进一步详细描述。

5.1 用于配置信号路径的参数摘要

以下表格显示了可控制信号路径的参数。

参数名称	描述
陀螺仪抗混叠滤波器禁用_ _	禁用陀螺仪抗混叠滤波器
陀螺抗混叠滤波器DELT_ _陀螺仪_抗混叠滤波器_DELTSQR 陀螺AAF位偏移_ _	配置陀螺仪抗混叠滤波器所需的三个参数。这是一个2nd 阶滤波器，具有可编程低通滤波器特性。此为用户可编程滤波器，可用于选择所需带宽。该滤波器可在给定输出数据速率下权衡均方根噪声与延迟。
加速度AAF禁用_ _	禁用加速度计抗混叠滤波器
加速度AAF增量_ _ 加速度_抗混叠滤波器_增量平方 加速度AAF位移位_ _	配置加速度计AAF需要三个参数。这是一个2nd 阶滤波器，带有可编程低通滤波器。这是一种用户可编程滤波器，可用于选择所需带宽。该滤波器允许在给定输出数据速率下权衡均方根噪声与延迟。
陀螺仪陷波滤波器禁用_ _ 陀螺仪_X/Y/Z_陷波滤波器_COSWZ 陀螺仪_X/Y/Z_陷波滤波器_COSWZ_选择	禁用陀螺仪陷波滤波器 出厂微调参数，设计用于在陀螺仪的感应峰值频率处或附近定位陷波，使用户仅抑制感应峰值对噪声的贡献，同时仍保持来自传感器的低延迟高带宽/输出数据速率接口。此滤波器仅适用于陀螺仪，且X、Y和Z轴的参数可独立选择。
GYRO NF BW SEL _ _ _	用于消除陀螺仪感应峰值所产生噪声的出厂微调参数。该参数在三轴中通用。

5.2 陷波滤波器

陷波滤波器仅支持陀螺仪信号路径。可通过以下步骤配置该滤波器。需注意陷波滤波器针对陀螺仪各轴独立设置，因此X、Y和Z轴可分别编程。

陷波滤波器频率（各轴）

启用陷波滤波器时，需为陀螺仪每个轴配置两个参数NF_COSWZ和NF_COSWZ_SEL。

参数NF_COSWZ为陀螺仪的每个轴定义如下：GYRO_X_NF_COSWZ（寄存器组1，寄存器0x0Fh与寄存器0x12h）、GYRO_Y_NF_COSWZ（寄存器组1，寄存器0x10h与寄存器0x12h）、GYRO_Z_NF_COSWZ（寄存器组1，寄存器0x11h与寄存器0x12h）。需注意，这些参数以9位值形式分布于两个不同的寄存器中。

Parameters NF_COSWZ_SEL are defined for each axis of the gyroscope as GYRO_X_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 3), GYRO_Y_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 4), GYRO_Z_NF_COSWZ_SEL (register bank 1, register 0x12h, bit 5).

Each value must be calculated using the steps described below, and programmed into the corresponding register locations mentioned above.

fdesired is the desired frequency of the Notch Filter in kHz. The lower bound for fdesired is 1kHz, and the upper bound is 3kHz. Operating the notch filter outside this range is not supported.

Step1: Fdrv = 19.2MHz/(CLKDIV*10); See Bank 3 register 0x2A for CLKDIV
Step2: COSWZ = cos(2*pi*fdesired/Fdrv)
Step3:

```
If abs(COSWZ)≤0.875
        NF_COSWZ = round[COSWZ*256]
        NF_COSWZ_SEL = 0
else
        NF_COSWZ_SEL = 1
        if COSWZ > 0.875
                NF_COSWZ = round [8*(1-COSWZ)*256]
        else if COSWZ < -0.875
                NF_COSWZ = round [-8*(1+COSWZ)*256]
        end
End
```

Bandwidth of Notch Filter (common to all axes)

The notch filter allows the user to control the width of the notch from eight possible values using a 3-bit parameter GYRO_NF_BW_SEL in register bank 1, register 0x13h, bits 6:4. This parameter is common to all three axes.

GYRO_NF_BW_SEL	Notch Filter Bandwidth (Hz)
0	1449
1	680
2	329
3	162
4	80
5	40
6	20
7	10

The notch filter can be selected or bypassed by using the parameter GYRO_NF_DIS in register bank 1, register 0x0Bh, bit 0 as shown below.

GYRO_NF_DIS	Function
0	Enable notch filter
1	Disable notch filter

参数NF_COSWZ_SEL为陀螺仪的每个轴定义如下：GYRO_X_NF_COSWZ_SEL（寄存器组1，寄存器0x12h，位3）、GYRO_Y_NF_COSWZ_SEL（寄存器组1，寄存器0x12h，位4）、GYRO_Z_NF_COSWZ_SEL（寄存器组1，寄存器0x12h，位5）。

每个数值必须按照以下描述的步骤计算，并编程写入上述对应的寄存器位置。

fdesired 是陷波滤波器的期望频率，单位为千赫。fdesired 的下限为1千赫兹，上限为3千赫。不支持在此范围之外操作陷波滤波器。

步骤1: Fdrv = 19.2兆赫/(时钟分频器*10); 时钟分频器参见存储区3寄存器0x2A
Step2: COSWZ = cos(2*pi*fdesired/Fdrv)
Step3:

```
If abs(COSWZ)≤0.875
        NF_COSWZ = round[COSWZ*256]
        NF_COSWZ_SEL = 0
else
        NF_COSWZ_SEL = 1
        if COSWZ > 0.875
                NF_COSWZ = round [8*(1-COSWZ)*256]
        else if COSWZ < -0.875
                NF_COSWZ = round [-8*(1+COSWZ)*256]
        end
End
```

陷波滤波器带宽（三轴共用）

陷波滤波器允许用户通过寄存器组1中寄存器0x13h的6:4位（3位参数GYRO_NF_BW_SEL）从八个可选值中控制陷波宽度。该参数为三轴共用。

GYRO NF BW SEL	陷波滤波器带宽（赫兹）
0	1449
1	680
2	329
3	162
4	80
5	40
6	20
7	10

可通过寄存器组1中的寄存器0x0Bh位0参数GYRO_NF_DIS选择或旁路陷波滤波器，如下所示。

GYRO NF DIS	功能
0	启用陷波滤波器
1	禁用陷波滤波器

5.3 ANTI-ALIAS FILTER

Anti-alias filters for gyroscope and accelerometer can be independently programmed to have bandwidths ranging from 42 Hz to 3979 Hz. To program the anti-alias filter for a required bandwidth, use the table below to map the bandwidth to register values as shown:

a. Register bank 2, register 0x03h, bits 6:1, ACCEL_AAF_DELT: Code from 1 to 63 that allows programming the bandwidth for accelerometer anti-alias filter
b. Register bank 2, register 0x04h, bits 7:0 and Bank 2, register 0x05h, bits 3:0, ACCEL_AAF_DELTSQR: Square of the delt value for accelerometer
c. Register bank 2, register 0x05h, bits 7:4, ACCEL_AAF_BITSHIFT: Bitshift value for accelerometer used in hardware implementation
d. Register bank 1, register 0x0Ch, bits 5:0, GYRO_AAF_DELT: Code from 1 to 63 that allows programming the bandwidth for gyroscope anti-alias filter
e. Register bank 1, register 0x0Dh, bits 7:0 and Bank 1, register 0x0Eh, bits 3:0, GYRO_AAF_DELTSQR: Square of the delt value for gyroscope
f. Register bank 1, register 0x0Eh, bits 7:4, GYRO_AAF_BITSHIFT: Bitshift value for gyroscope used in hardware implementation

3dB Bandwidth (Hz)	ACCEL_AAF_DELT; GYRO_AAF_DELT	ACCEL_AAF_DELTSQR; GYRO_AAF_DELTSQR	ACCEL_AAF_BITSHIFT; GYRO_AAF_BITSHIFT
42	1	1	15
84	2	4	13
126	3	9	12
170	4	16	11
213	5	25	10
258	6	36	10
303	7	49	9
348	8	64	9
394	9	81	9
441	10	100	8
488	11	122	8
536	12	144	8
585	13	170	8
634	14	196	7
684	15	224	7
734	16	256	7
785	17	288	7
837	18	324	7
890	19	360	6
943	20	400	6
997	21	440	6
1051	22	488	6
1107	23	528	6
1163	24	576	6
1220	25	624	6
1277	26	680	6
1336	27	736	5

5.3 抗混叠滤波器

陀螺仪和加速度计的抗锯齿滤波器可独立编程，带宽范围从42赫兹至3979赫兹。如需为特定带宽编程抗锯齿滤波器，请使用下方表格将带宽映射至寄存器值，如图所示：

a. 寄存器组2，寄存器0x03h，位6:1，加速度计_抗混叠滤波器_增量：代码从1到63，允许编程加速度计抗混叠滤波器的带宽
b. 寄存器组2，寄存器0x04h，位7:0和存储区2，寄存器0x05h，位3:0，加速度计_抗混叠滤波器_增量平方：加速度计的增量值平方
c. 寄存器组2，寄存器0x05h，位7:4，加速度计_抗混叠滤波器_位移位：硬件中使用的加速度计位移位值实现
d. 寄存器组1，寄存器0x0Ch，位5:0，陀螺仪_抗混叠滤波器_增量：1至63的代码，用于编程陀螺仪抗混滤波器的带宽
e. 寄存器组1，寄存器0x0Dh，位7:0和组1，寄存器0x0Eh，位3:0，陀螺仪_抗混叠滤波器_增量平方：陀螺仪的增量值
f. 寄存器组1，寄存器0x0Eh，位7:4，GYRO_AAF_BITSHIFT：用于硬件实现的陀螺仪位移位值

3dB带宽（赫兹）	ACCEL_AAF_DELT; GYRO_AAF_DELT	ACCEL_AAF_DELTSQR; GYRO_AAF_DELTSQR	加速度计_抗混叠滤波器_位移位; GYRO_抗混叠滤波器 位移位
42	1	1	15
84	2	4	13
126	3	9	12
170	4	16	11
213	5	25	10
258	6	36	10
303	7	49	9
348	8	64	9
394	9	81	9
441	10	100	8
488	11	122	8
536	12	144	8
585	13	170	8
634	14	196	7
684	15	224	7
734	16	256	7
785	17	288	7
837	18	324	7
890	19	360	6
943	20	400	6
997	21	440	6
1051	22	488	6
1107	23	528	6
1163	24	576	6
1220	25	624	6
1277	26	680	6
1336	27	736	5

1395	28	784	5
1454	29	848	5
1515	30	896	5
1577	31	960	5
1639	32	1024	5
1702	33	1088	5
1766	34	1152	5
1830	35	1232	5
1896	36	1296	5
1962	37	1376	4
2029	38	1440	4
2097	39	1536	4
2166	40	1600	4
2235	41	1696	4
2306	42	1760	4
2377	43	1856	4
2449	44	1952	4
2522	45	2016	4
2596	46	2112	4
2671	47	2208	4
2746	48	2304	4
2823	49	2400	4
2900	50	2496	4
2978	51	2592	4
3057	52	2720	4
3137	53	2816	3
3217	54	2944	3
3299	55	3008	3
3381	56	3136	3
3464	57	3264	3
3548	58	3392	3
3633	59	3456	3
3718	60	3584	3
3805	61	3712	3
3892	62	3840	3
3979	63	3968	3

The anti-alias filter can be selected or bypassed for the gyroscope by using the parameter GYRO_AAF_DIS in register bank 1, register 0x0Bh, bit 1 as shown below.

GYRO_AAF_DIS	Function
0	Enable gyroscope anti-aliasing filter
1	Disable gyroscope anti-aliasing filter

1395	28	784	5
1454	29	848	5
1515	30	896	5
1577	31	960	5
1639	32	1024	5
1702	33	1088	5
1766	34	1152	5
1830	35	1232	5
1896	36	1296	5
1962	37	1376	4
2029	38	1440	4
2097	39	1536	4
2166	40	1600	4
2235	41	1696	4
2306	42	1760	4
2377	43	1856	4
2449	44	1952	4
2522	45	2016	4
2596	46	2112	4
2671	47	2208	4
2746	48	2304	4
2823	49	2400	4
2900	50	2496	4
2978	51	2592	4
3057	52	2720	4
3137	53	2816	3
3217	54	2944	3
3299	55	3008	3
3381	56	3136	3
3464	57	3264	3
3548	58	3392	3
3633	59	3456	3
3718	60	3584	3
3805	61	3712	3
3892	62	3840	3
3979	63	3968	3

通过使用寄存器组1中寄存器0x0Bh的位1参数GYRO_AAF_DIS，可以选择或旁路陀螺仪的抗混叠滤波器，如下所示。

GYRO AAF DIS_ _	功能
0	启用陀螺仪抗混叠滤波器
1	禁用陀螺仪抗混叠滤波器

The anti-alias filter can be selected or bypassed for the accelerometer by using the parameter ACCEL_AAF_DIS in register bank 2, register 0x03h, bit 0 as shown below.

ACCEL_AAF_DIS	Function
0	Enable accelerometer anti-aliasing filter
1	Disable accelerometer anti-aliasing filter

5.4 USER PROGRAMMABLE OFFSET

Gyroscope and accelerometer offsets can be programmed by the user by using registers OFFSET_USER0, through OFFSET_USER8, in bank 0, registers 0x77h through 0x7Fh (bank 4) as shown below.

Register Address	Register Name	Bits	Function
0x77h	OFFSET_USER0	7:0	Lower bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x78h	OFFSET_USER1	3:0	Upper bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
		7:4	Upper bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x79h	OFFSET_USER2	7:0	Lower bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x7Ah	OFFSET_USER3	7:0	Lower bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
0x7Bh	OFFSET_USER4	3:0	Upper bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
		7:4	Upper bits of X-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Ch	OFFSET_USER5	7:0	Lower bits of X-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Dh	OFFSET_USER6	7:0	Lower bits of Y-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Eh	OFFSET_USER7	3:0	Upper bits of Y-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
		7:4	Upper bits of Z-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.
0x7Fh	OFFSET_USER8	7:0	Lower bits of Z-accel offset programmed by user. Max value is ±1 g, resolution is 0.5 g.

5.5 UI FILTER BLOCK

The UI filter block can be programmed to select filter order and bandwidth independently for gyroscope and accelerometer.

Gyroscope filter order can be selected by programming the parameter GYRO_UI_FILT_ORD in register bank 0, register 0x51h, bits 3:2, as shown below.

可通过寄存器组2中的寄存器0x03h位0参数ACCEL_AAF_DIS选择或旁路加速度计的抗混叠滤波器，如下所示。

加速度AAF禁用_ –	功能
0	启用加速度计抗混叠滤波器
1	禁用加速度计抗混叠滤波器

5.4 用户可编程偏移

用户可通过使用存储区0中的寄存器OFFSET_USER0至OFFSET_USER8，对陀螺仪和加速度计偏移进行编程设置，如存储区0的寄存器0x77h至0x7Fh（存储区4）所示。

寄存器地址	寄存器名称	Bits	功能
0x77h	用户0偏移量_	7:0	用户编程的X陀螺仪偏移量的低位。最大值为±64 度每秒，分辨率为1/32度/秒。
0x78h	用户1偏移量_	3:0	用户编程的X陀螺仪偏移量的高位。最大值为±64 度每秒，分辨率为1/32度/秒。
		7:4	用户编程的Y陀螺仪偏移量的高位。最大值为±64 度每秒，分辨率为1/32度/秒。
0x79h	用户2偏移量_	7:0	用户编程的Y陀螺偏移低位。最大值为±64 度每秒，分辨率为1/32度/秒。
0x7Ah	用户3偏移量_	7:0	用户编程的Z陀螺偏移低位。最大值为±64 度每秒，分辨率为1/32度/秒。
0x7Bh	偏移量 用户4_	3:0	Z轴陀螺仪偏移的高位由用户编程。最大值为±64 度每秒，分辨率为1/32度/秒。
		7:4	X轴加速度计偏移的高位由用户编程。最大值为±1 重力加速度，分辨率为0.5g。
0x7Ch	偏移量 用户5_	7:0	X轴加速度计偏移的低位由用户编程。最大值为±1 重力加速度，分辨率为0.5g。
0x7Dh	偏移量 用户6_	7:0	Y轴加速度偏移的低位由用户编程。最大值为±1 重力加速度，分辨率为0.5g。
0x7Eh	偏移量 USER7_	3:0	用户编程的Y轴加速度偏移高位。最大值为±1 重力加速度，分辨率为0.5g。
		7:4	用户编程的Z轴加速度偏移高位。最大值为±1 重力加速度，分辨率为0.5g。
0x7Fh	偏移量 USER8_	7:0	用户编程的Z轴加速度偏移低位。最大值为±1 重力加速度，分辨率为0.5g。

5.5 用户界面滤波器模块

用户界面滤波器模块可编程为陀螺仪和加速度计独立选择滤波器阶数和带宽。

陀螺仪滤波器阶数可通过编程寄存器组0中的寄存器0x51h位3:2的参数GYRO_UI_FILT_ORD进行选择，如下所示。

GYRO_UI_FILT_ORD	Filter Order
00	1st order
01	2nd order
10	3rd order
11	Reserved

Accelerometer filter order can be selected by programming the parameter ACCEL_UI_FILT_ORD in register bank 0, register 0x53h, bits 4:3, as shown below.

ACCEL_UI_FILT_ORD	Filter Order
00	1st order
01	2nd order
10	3rd order
11	Reserved

Gyroscope and accelerometer filter 3dB bandwidth can be selected by programming the parameter GYRO_UI_FILT_BW in register bank 0, register 0x52h, bits 3:0, and the parameter ACCEL_UI_FILT_BW in register bank 0, register 0x52h, bits 7:4, as shown below. The values shown in bold correspond to low noise and the values shown in italics correspond to low latency. User can select the appropriate setting based on the application requirements for power and latency. Corresponding Noise Bandwidth (NBW) and Group Delay values are also shown.

1st Order Filter 3dB Bandwidth, Noise Bandwidth (NBW), Group Delay

		3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*8400.0*									
2	16000	*4194.1*									
3	8000	*2096.3*									
4	4000	*1048.1*									
5	2000	*524.0*									
6	1000	**498.3**	**227.2**	**188.9**	**111.0**	**92.4**	**59.6**	**48.8**	**23.9**	**262.0**	*2096.3*
15	500	**249.1**	**113.6**	**94.4**	**55.5**	**46.2**	**29.8**	**24.4**	**11.9**	**131.0**	*1048.1*
7	200	**99.6**	**90.9**	**75.5**	**44.4**	**37.0**	**23.8**	**19.5**	**9.6**	*104.8*	*419.2*
8	100	**49.8**	*90.9*	*75.5*	**44.4**	**37.0**	**23.8**	**19.5**	**9.6**	*104.8*	*209.6*
9	50	**24.9**	*90.9*	*75.5*	*44.4*	*37.0*	**23.8**	**19.5**	**9.6**	*104.8*	*104.8*
10	25	**12.5**	*90.9*	*75.5*	*44.4*	*37.0*	*23.8*	*19.5*	**9.6**	*104.8*	*52.4*
11	12.5	*12.5*	*90.9*	*75.5*	*44.4*	*37.0*	*23.8*	*19.5*	*9.6*	*104.8*	*52.4*

		NBW Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)									
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*8831.7*									
2	16000	*4410.6*									
3	8000	*2204.6*									

陀螺仪 用户界面 滤波器 阶数	滤波器阶数
00	1st 阶数
01	2nd 阶数
10	3rd 阶数
11	保留

加速度计滤波器阶数可通过编程寄存器组0中寄存器0x53h的位4:3参数ACCEL_UI_FILT_ORD进行选择，如下所示。

ACCEL UI FILT ORD	滤波器阶数
00	1st 阶数
01	2nd 阶数
10	3rd 阶数
11	保留

陀螺仪和加速度计滤波器3分贝带宽可通过编程寄存器组0中的寄存器0x52h位3:0的参数GYRO_UI_FILT_BW，以及寄存器0x52h位7:4的参数ACCEL_UI_FILT_BW进行选择，如下所示。粗体显示的数值对应低噪声，斜体显示的数值对应低延迟。用户可根据应用对功耗和延迟的需求选择合适的设置。同时列出了相应的噪声带宽（NBW）和群延迟值。

1st 阶数滤波器3dB带宽，噪声带宽（NBW），群延迟

		陀螺仪/加速度计_用户界面_滤波器_输出数据速率=0 (一阶滤波器)的3dB带宽（赫兹）									
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*8400.0*									
2	16000	*4194.1*									
3	8000	*2096.3*									
4	4000	*1048.1*									
5	2000	*524.0*									
6	1000	**498.3**	**227.2**	**188.9**	**111.0**	**92.4**	**59.6**	**48.8**	**23.9**	**262.0**	*2096.3*
15	500	**249.1**	**113.6**	**94.4**	**55.5**	**46.2**	**29.8**	**24.4**	**11.9**	**131.0**	*1048.1*
7	200	**99.6**	**90.9**	**75.5**	**44.4**	**37.0**	**23.8**	**19.5**	**9.6**	*104.8*	*419.2*
8	100	**49.8**	*90.9*	*75.5*	**44.4**	**37.0**	**23.8**	**19.5**	**9.6**	*104.8*	*209.6*
9	50	**24.9**	*90.9*	*75.5*	*44.4*	*37.0*	**23.8**	**19.5**	**9.6**	*104.8*	*104.8*
10	25	**12.5**	*90.9*	*75.5*	*44.4*	*37.0*	*23.8*	*19.5*	**9.6**	*104.8*	*52.4*
11	12.5	*12.5*	*90.9*	*75.5*	*44.4*	*37.0*	*23.8*	*19.5*	*9.6*	*104.8*	*52.4*

		陀螺仪/加速度计_用户界面_滤波器_输出数据速率=0 (一阶滤波器)的NBW带宽（赫兹）									
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*8831.7*									
2	16000	*4410.6*									
3	8000	*2204.6*									

4	4000	*1102.2*									
5	2000	*551.1*									
6	1000	**551.1**	**230.8**	**196.3**	**126.5**	**108.9**	**75.8**	**64.1**	**34.1**	**275.6**	*2204.6*
15	500	**280.5**	**115.4**	**98.2**	**63.3**	**54.5**	**37.9**	**32.1**	**17.1**	**137.8**	*1102.2*
7	200	**112.2**	**92.4**	**78.5**	**50.6**	**43.6**	**30.3**	**25.7**	**13.7**	*110.3*	*440.9*
8	100	**56.1**	*92.4*	*78.5*	**50.6**	**43.6**	**30.3**	**25.7**	**13.7**	*110.3*	*220.5*
9	50	**28.1**	*92.4*	*78.5*	*50.6*	*43.6*	**30.3**	**25.7**	**13.7**	*110.3*	*110.3*
10	25	**14.1**	*92.4*	*78.5*	*50.6*	*43.6*	*30.3*	*25.7*	**13.7**	*110.3*	*55.2*
11	12.5	*14.1*	*92.4*	*78.5*	*50.6*	*43.6*	*30.3*	*25.7*	*13.7*	*110.3*	*55.2*

	Group Delay @DC (ms) for GYRO/ACCEL_UI_FILT_ORD=0 (1st order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*0.1*									
2	16000	*0.1*									
3	8000	*0.2*									
4	4000	*0.4*									
5	2000	*0.8*									
6	1000	**0.6**	**1.8**	**2.0**	**2.8**	**3.1**	**4.1**	**4.7**	**8.1**	**1.5**	*0.2*
15	500	**1.1**	**3.6**	**4.0**	**5.5**	**6.1**	**8.1**	**9.3**	**16.2**	**3.0**	*0.4*
7	200	**2.7**	**4.4**	**5.0**	**6.8**	**7.6**	**10.2**	**11.7**	**20.3**	*3.8*	*1.0*
8	100	**5.3**	*4.4*	*5.0*	**6.8**	**7.6**	**10.2**	**11.7**	**20.3**	*3.8*	*1.9*
9	50	**10.5**	*4.4*	*5.0*	*6.8*	*7.6*	**10.2**	**11.7**	**20.3**	*3.8*	*3.8*
10	25	**21.0**	*4.4*	*5.0*	*6.8*	*7.6*	*10.2*	*11.7*	**20.3**	*3.8*	*7.5*
11	12.5	*21.0*	*4.4*	*5.0*	*6.8*	*7.6*	*10.2*	*11.7*	*20.3*	*3.8*	*7.5*

2nd Order Filter 3dB Bandwidth, Noise Bandwidth (NBW), Group Delay

	3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=1 (2nd order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*8400.0*									
2	16000	*4194.1*									
3	8000	*2096.3*									
4	4000	*1048.1*									
5	2000	*524.0*									
6	1000	**493.3**	**230.7**	**191.6**	**117.5**	**97.1**	**59.6**	**48.0**	**21.3**	**262.0**	*2096.3*
15	500	**246.7**	**115.3**	**95.8**	**58.8**	**48.5**	**29.8**	**24.0**	**10.6**	**131.0**	*1048.1*
7	200	**98.7**	**92.3**	**76.6**	**47.0**	**38.8**	**23.8**	**19.2**	**8.5**	*104.8*	*419.2*
8	100	**49.3**	*92.3*	*76.6*	**47.0**	**38.8**	**23.8**	**19.2**	**8.5**	*104.8*	*209.6*
9	50	**24.7**	*92.3*	*76.6*	*47.0*	*38.8*	**23.8**	**19.2**	**8.5**	*104.8*	*104.8*
10	25	**12.3**	*92.3*	*76.6*	*47.0*	*38.8*	*23.8*	*19.2*	**8.5**	*104.8*	*52.4*
11	12.5	*12.3*	*92.3*	*76.6*	*47.0*	*38.8*	*23.8*	*19.2*	*8.5*	*104.8*	*52.4*

4	4000	*1102.2*									
5	2000	*551.1*									
6	1000	**551.1**	**230.8**	**196.3**	**126.5**	**108.9**	**75.8**	**64.1**	**34.1**	**275.6**	*2204.6*
15	500	**280.5**	**115.4**	**98.2**	**63.3**	**54.5**	**37.9**	**32.1**	**17.1**	**137.8**	*1102.2*
7	200	**112.2**	**92.4**	**78.5**	**50.6**	**43.6**	**30.3**	**25.7**	**13.7**	*110.3*	*440.9*
8	100	**56.1**	*92.4*	*78.5*	**50.6**	**43.6**	**30.3**	**25.7**	**13.7**	*110.3*	*220.5*
9	50	**28.1**	*92.4*	*78.5*	*50.6*	*43.6*	**30.3**	**25.7**	**13.7**	*110.3*	*110.3*
10	25	**14.1**	*92.4*	*78.5*	*50.6*	*43.6*	*30.3*	*25.7*	**13.7**	*110.3*	*55.2*
11	12.5	*14.1*	*92.4*	*78.5*	*50.6*	*43.6*	*30.3*	*25.7*	*13.7*	*110.3*	*55.2*

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=0 （一阶滤波器）的直流群延迟（毫秒）										
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*0.1*									
2	16000	*0.1*									
3	8000	*0.2*									
4	4000	*0.4*									
5	2000	*0.8*									
6	1000	**0.6**	**1.8**	**2.0**	**2.8**	**3.1**	**4.1**	**4.7**	**8.1**	**1.5**	*0.2*
15	500	**1.1**	**3.6**	**4.0**	**5.5**	**6.1**	**8.1**	**9.3**	**16.2**	**3.0**	*0.4*
7	200	**2.7**	**4.4**	**5.0**	**6.8**	**7.6**	**10.2**	**11.7**	**20.3**	*3.8*	*1.0*
8	100	**5.3**	*4.4*	*5.0*	**6.8**	**7.6**	**10.2**	**11.7**	**20.3**	*3.8*	*1.9*
9	50	**10.5**	*4.4*	*5.0*	*6.8*	*7.6*	**10.2**	**11.7**	**20.3**	*3.8*	*3.8*
10	25	**21.0**	*4.4*	*5.0*	*6.8*	*7.6*	*10.2*	*11.7*	**20.3**	*3.8*	*7.5*
11	12.5	*21.0*	*4.4*	*5.0*	*6.8*	*7.6*	*10.2*	*11.7*	*20.3*	*3.8*	*7.5*

2nd 阶滤波器3dB带宽、噪声带宽（NBW）、群延迟

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=1 （二阶滤波器）的3dB带宽（赫兹）										
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*8400.0*									
2	16000	*4194.1*									
3	8000	*2096.3*									
4	4000	*1048.1*									
5	2000	*524.0*									
6	1000	**493.3**	**230.7**	**191.6**	**117.5**	**97.1**	**59.6**	**48.0**	**21.3**	**262.0**	*2096.3*
15	500	**246.7**	**115.3**	**95.8**	**58.8**	**48.5**	**29.8**	**24.0**	**10.6**	**131.0**	*1048.1*
7	200	**98.7**	**92.3**	**76.6**	**47.0**	**38.8**	**23.8**	**19.2**	**8.5**	*104.8*	*419.2*
8	100	**49.3**	*92.3*	*76.6*	**47.0**	**38.8**	**23.8**	**19.2**	**8.5**	*104.8*	*209.6*
9	50	**24.7**	*92.3*	*76.6*	*47.0*	*38.8*	**23.8**	**19.2**	**8.5**	*104.8*	*104.8*
10	25	**12.3**	*92.3*	*76.6*	*47.0*	*38.8*	*23.8*	*19.2*	**8.5**	*104.8*	*52.4*
11	12.5	*12.3*	*92.3*	*76.6*	*47.0*	*38.8*	*23.8*	*19.2*	*8.5*	*104.8*	*52.4*

	NBW Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=1 (2nd order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*8831.7*									
2	16000	*4410.6*									
3	8000	*2204.6*									
4	4000	*1102.2*									
5	2000	*551.1*									
6	1000	**551.1**	**223.7**	**189.9**	**122.7**	**102.8**	**64.7**	**52.5**	**23.7**	**275.6**	*2204.6*
15	500	**259.6**	**111.9**	**95.0**	**61.4**	**51.4**	**32.4**	**26.3**	**11.9**	**137.8**	*1102.2*
7	200	**103.9**	**89.5**	**76.0**	**49.1**	**41.2**	**25.9**	**21.0**	**9.5**	*110.3*	*440.9*
8	100	**52.0**	*89.5*	*76.0*	**49.1**	**41.2**	**25.9**	**21.0**	**9.5**	*110.3*	*220.5*
9	50	**26.0**	*89.5*	*76.0*	*49.1*	*41.2*	**25.9**	**21.0**	**9.5**	*110.3*	*110.3*
10	25	**13.0**	*89.5*	*76.0*	*49.1*	*41.2*	*25.9*	*21.0*	**9.5**	*110.3*	*55.2*
11	12.5	*13.0*	*89.5*	*76.0*	*49.1*	*41.2*	*25.9*	*21.0*	*9.5*	*110.3*	*55.2*

	Group Delay @DC (ms) for GYRO/ACCEL_UI_FILT_ORD=1 (2nd order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*0.1*									
2	16000	*0.1*									
3	8000	*0.2*									
4	4000	*0.4*									
5	2000	*0.8*									
6	1000	**0.7**	**2.1**	**2.4**	**3.2**	**3.7**	**5.2**	**6.1**	**12.0**	**1.5**	*0.2*
15	500	**1.3**	**4.1**	**4.7**	**6.4**	**7.3**	**10.4**	**12.2**	**24.0**	**3.0**	*0.4*
7	200	**3.3**	**5.1**	**5.8**	**8.0**	**9.1**	**12.9**	**15.3**	**30.0**	*3.8*	*1.0*
8	100	**6.5**	*5.1*	*5.8*	**8.0**	**9.1**	**12.9**	**15.3**	**30.0**	*3.8*	*1.9*
9	50	**12.9**	*5.1*	*5.8*	*8.0*	*9.1*	**12.9**	**15.3**	**30.0**	*3.8*	*3.8*
10	25	**25.7**	*5.1*	*5.8*	*8.0*	*9.1*	*12.9*	*15.3*	**30.0**	*3.8*	*7.5*
11	12.5	*25.7*	*5.1*	*5.8*	*8.0*	*9.1*	*12.9*	*15.3*	*30.0*	*3.8*	*7.5*

3rd Order Filter 3dB Bandwidth, Noise Bandwidth (NBW), Group Delay

	3dB Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=2 (3rd order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*8400.0*									
2	16000	*4194.1*									
3	8000	*2096.3*									
4	4000	*1048.1*									
5	2000	*524.0*									
6	1000	**492.9**	**234.7**	**195.8**	**118.9**	**97.9**	**60.8**	**46.8**	**25.2**	**262.0**	*2096.3*
15	500	**246.4**	**117.4**	**97.9**	**59.5**	**48.9**	**30.4**	**23.4**	**12.6**	**131.0**	*1048.1*
7	200	**98.6**	**93.9**	**78.3**	**47.6**	**39.2**	**24.3**	**18.7**	**10.1**	*104.8*	*419.2*

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=1 的NBW带宽（赫兹）（二阶滤波器）										
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*8831.7*									
2	16000	*4410.6*									
3	8000	*2204.6*									
4	4000	*1102.2*									
5	2000	*551.1*									
6	1000	**551.1**	**223.7**	**189.9**	**122.7**	**102.8**	**64.7**	**52.5**	**23.7**	**275.6**	*2204.6*
15	500	**259.6**	**111.9**	**95.0**	**61.4**	**51.4**	**32.4**	**26.3**	**11.9**	**137.8**	*1102.2*
7	200	**103.9**	**89.5**	**76.0**	**49.1**	**41.2**	**25.9**	**21.0**	**9.5**	*110.3*	*440.9*
8	100	**52.0**	*89.5*	*76.0*	**49.1**	**41.2**	**25.9**	**21.0**	**9.5**	*110.3*	*220.5*
9	50	**26.0**	*89.5*	*76.0*	*49.1*	*41.2*	**25.9**	**21.0**	**9.5**	*110.3*	*110.3*
10	25	**13.0**	*89.5*	*76.0*	*49.1*	*41.2*	*25.9*	*21.0*	**9.5**	*110.3*	*55.2*
11	12.5	*13.0*	*89.5*	*76.0*	*49.1*	*41.2*	*25.9*	*21.0*	*9.5*	*110.3*	*55.2*

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=1 的直流群延迟（毫秒）（二阶滤波器）										
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*0.1*									
2	16000	*0.1*									
3	8000	*0.2*									
4	4000	*0.4*									
5	2000	*0.8*									
6	1000	**0.7**	**2.1**	**2.4**	**3.2**	**3.7**	**5.2**	**6.1**	**12.0**	**1.5**	*0.2*
15	500	**1.3**	**4.1**	**4.7**	**6.4**	**7.3**	**10.4**	**12.2**	**24.0**	**3.0**	*0.4*
7	200	**3.3**	**5.1**	**5.8**	**8.0**	**9.1**	**12.9**	**15.3**	**30.0**	*3.8*	*1.0*
8	100	**6.5**	*5.1*	*5.8*	**8.0**	**9.1**	**12.9**	**15.3**	**30.0**	*3.8*	*1.9*
9	50	**12.9**	*5.1*	*5.8*	*8.0*	*9.1*	**12.9**	**15.3**	**30.0**	*3.8*	*3.8*
10	25	**25.7**	*5.1*	*5.8*	*8.0*	*9.1*	*12.9*	*15.3*	**30.0**	*3.8*	*7.5*
11	12.5	*25.7*	*5.1*	*5.8*	*8.0*	*9.1*	*12.9*	*15.3*	*30.0*	*3.8*	*7.5*

3rd 阶数滤波器3分贝带宽、噪声带宽（NBW）、群延迟

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=2 （三阶滤波器）的3dB带宽（赫兹）										
		陀螺仪/加速度计_UI_FILT_BW									
陀螺仪/加速度计_ODR	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*8400.0*									
2	16000	*4194.1*									
3	8000	*2096.3*									
4	4000	*1048.1*									
5	2000	*524.0*									
6	1000	**492.9**	**234.7**	**195.8**	**118.9**	**97.9**	**60.8**	**46.8**	**25.2**	**262.0**	*2096.3*
15	500	**246.4**	**117.4**	**97.9**	**59.5**	**48.9**	**30.4**	**23.4**	**12.6**	**131.0**	*1048.1*
7	200	**98.6**	**93.9**	**78.3**	**47.6**	**39.2**	**24.3**	**18.7**	**10.1**	*104.8*	*419.2*

8	100	**49.3**	*93.9*	*78.3*	**47.6**	**39.2**	**24.3**	**18.7**	**10.1**	*104.8*	*209.6*
9	50	**24.6**	*93.9*	*78.3*	*47.6*	*39.2*	**24.3**	**18.7**	**10.1**	*104.8*	*104.8*
10	25	**12.3**	*93.9*	*78.3*	*47.6*	*39.2*	*24.3*	*18.7*	**10.1**	*104.8*	*52.4*
11	12.5	*12.3*	*93.9*	*78.3*	*47.6*	*39.2*	*24.3*	*18.7*	*10.1*	*104.8*	*52.4*

	NBW Bandwidth (Hz) for GYRO/ACCEL_UI_FILT_ORD=2 (3rd order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*8831.7*									
2	16000	*4410.6*									
3	8000	*2204.6*									
4	4000	*1102.2*									
5	2000	*551.1*									
6	1000	**551.1**	**221.3**	**188.5**	**120.1**	**100.0**	**62.9**	**48.6**	**26.4**	**275.6**	*2204.6*
15	500	**252.0**	**110.7**	**94.3**	**60.1**	**50.0**	**31.5**	**24.3**	**13.2**	**137.8**	*1102.2*
7	200	**100.8**	**88.6**	**75.4**	**48.1**	**40.0**	**25.2**	**19.5**	**10.6**	*110.3*	*440.9*
8	100	**50.4**	*88.6*	*75.4*	**48.1**	**40.0**	**25.2**	**19.5**	**10.6**	*110.3*	*220.5*
9	50	**25.2**	*88.6*	*75.4*	*48.1*	*40.0*	**25.2**	**19.5**	**10.6**	*110.3*	*110.3*
10	25	**12.6**	*88.6*	*75.4*	*48.1*	*40.0*	*25.2*	*19.5*	**10.6**	*110.3*	*55.2*
11	12.5	*12.6*	*88.6*	*75.4*	*48.1*	*40.0*	*25.2*	*19.5*	*10.6*	*110.3*	*55.2*

	Group Delay @DC (ms) for GYRO/ACCEL_UI_FILT_ORD=2 (3rd order filter)										
		GYRO/ACCEL_UI_FILT_BW									
GYRO/ACCEL_ODR	ODR(Hz)	0	1	2	3	4	5	6	7	14	15
1	32000	*0.1*									
2	16000	*0.1*									
3	8000	*0.2*									
4	4000	*0.4*									
5	2000	*0.8*									
6	1000	**0.8**	**2.3**	**2.7**	**4.0**	**4.6**	**6.6**	**8.2**	**14.1**	**1.5**	*0.2*
15	500	**1.6**	**4.6**	**5.4**	**7.9**	**9.2**	**13.2**	**16.3**	**28.1**	**3.0**	*0.4*
7	200	**4.0**	**5.8**	**6.8**	**9.8**	**11.4**	**16.5**	**20.4**	**35.2**	*3.8*	*1.0*
8	100	**8.0**	*5.8*	*6.8*	**9.8**	**11.4**	**16.5**	**20.4**	**35.2**	*3.8*	*1.9*
9	50	**15.9**	*5.8*	*6.8*	*9.8*	*11.4*	**16.5**	**20.4**	**35.2**	*3.8*	*3.8*
10	25	**31.8**	*5.8*	*6.8*	*9.8*	*11.4*	*16.5*	*20.4*	**35.2**	*3.8*	*7.5*
11	12.5	*31.8*	*5.8*	*6.8*	*9.8*	*11.4*	*16.5*	*20.4*	*35.2*	*3.8*	*7.5*

5.6 UI PATH ODR AND FSR SELECTION

Gyroscope ODR can be selected by programming the parameter GYRO_ODR in register bank 0, register 0x4Fh, bits 3:0 as shown below.

GYRO_ODR	Gyroscope ODR Value
0000	Reserved
0001	32kHz

8	100	**49.3**	*93.9*	*78.3*	**47.6**	**39.2**	**24.3**	**18.7**	**10.1**	*104.8*	*209.6*
9	50	**24.6**	*93.9*	*78.3*	*47.6*	*39.2*	**24.3**	**18.7**	**10.1**	*104.8*	*104.8*
10	25	**12.3**	*93.9*	*78.3*	*47.6*	*39.2*	*24.3*	*18.7*	**10.1**	*104.8*	*52.4*
11	12.5	*12.3*	*93.9*	*78.3*	*47.6*	*39.2*	*24.3*	*18.7*	*10.1*	*104.8*	*52.4*

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=2 (三阶滤波器)的NBW带宽（赫兹）										
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*8831.7*									
2	16000	*4410.6*									
3	8000	*2204.6*									
4	4000	*1102.2*									
5	2000	*551.1*									
6	1000	**551.1**	**221.3**	**188.5**	**120.1**	**100.0**	**62.9**	**48.6**	**26.4**	**275.6**	*2204.6*
15	500	**252.0**	**110.7**	**94.3**	**60.1**	**50.0**	**31.5**	**24.3**	**13.2**	**137.8**	*1102.2*
7	200	**100.8**	**88.6**	**75.4**	**48.1**	**40.0**	**25.2**	**19.5**	**10.6**	*110.3*	*440.9*
8	100	**50.4**	*88.6*	*75.4*	**48.1**	**40.0**	**25.2**	**19.5**	**10.6**	*110.3*	*220.5*
9	50	**25.2**	*88.6*	*75.4*	*48.1*	*40.0*	**25.2**	**19.5**	**10.6**	*110.3*	*110.3*
10	25	**12.6**	*88.6*	*75.4*	*48.1*	*40.0*	*25.2*	*19.5*	**10.6**	*110.3*	*55.2*
11	12.5	*12.6*	*88.6*	*75.4*	*48.1*	*40.0*	*25.2*	*19.5*	*10.6*	*110.3*	*55.2*

	陀螺仪/加速度计_用户界面_滤波器_输出数据速率=2 直流群延迟（毫秒）（三阶滤波器）										
		陀螺仪/加速度计_用户界面_滤波器_带宽									
陀螺仪/加速度计_输出数据速率	输出数据速率（赫兹）	0	1	2	3	4	5	6	7	14	15
1	32000	*0.1*									
2	16000	*0.1*									
3	8000	*0.2*									
4	4000	*0.4*									
5	2000	*0.8*									
6	1000	**0.8**	**2.3**	**2.7**	**4.0**	**4.6**	**6.6**	**8.2**	**14.1**	**1.5**	*0.2*
15	500	**1.6**	**4.6**	**5.4**	**7.9**	**9.2**	**13.2**	**16.3**	**28.1**	**3.0**	*0.4*
7	200	**4.0**	**5.8**	**6.8**	**9.8**	**11.4**	**16.5**	**20.4**	**35.2**	*3.8*	*1.0*
8	100	**8.0**	*5.8*	*6.8*	**9.8**	**11.4**	**16.5**	**20.4**	**35.2**	*3.8*	*1.9*
9	50	**15.9**	*5.8*	*6.8*	*9.8*	*11.4*	**16.5**	**20.4**	**35.2**	*3.8*	*3.8*
10	25	**31.8**	*5.8*	*6.8*	*9.8*	*11.4*	*16.5*	*20.4*	**35.2**	*3.8*	*7.5*
11	12.5	*31.8*	*5.8*	*6.8*	*9.8*	*11.4*	*16.5*	*20.4*	*35.2*	*3.8*	*7.5*

5.6 用户界面路径 输出数据速率与FSR选择

陀螺仪输出数据速率可通过编程寄存器组0中寄存器0x4Fh的位3:0参数GYRO_ODR来选择，如下所示。

GYRO_ODR	陀螺仪输出数据速率值
0000	保留
0001	32千赫

0010	16kHz
0011	8kHz
0100	4kHz
0101	2kHz
0110	1kHz (default)
0111	200Hz
1000	100Hz
1001	50Hz
1010	25Hz
1011	12.5Hz
1100	Reserved
1101	Reserved
1110	Reserved
1111	500Hz

Gyroscope FSR can be selected by programming the parameter GYRO_UI_FS_SEL in register bank 0, register 0x4Fh, bits 7:5 as shown below.

GYRO_UI_FS_SEL	Gyroscope FSR Value
000	2000dps
001	1000dps
010	500dps
011	250dps
100	125dps
101	62.5dps
110	31.25dps
111	15.625dps

Accelerometer ODR can be selected by programming the parameter ACCEL_ODR in register bank 0, register 0x50h, bits 3:0 as shown below.

ACCEL_ODR	Accelerometer ODR Value
0000	Reserved
0001	32kHz (LN mode)
0010	16kHz (LN mode)
0011	8kHz (LN mode)
0100	4kHz (LN mode)
0101	2kHz (LN mode)
0110	1kHz (LN mode) (default)
0111	200Hz (LP or LN mode)
1000	100Hz (LP or LN mode)
1001	50Hz (LP or LN mode)
1010	25Hz (LP or LN mode)

0010	16千赫
0011	8kHz
0100	4kHz
0101	2kHz
0110	1千赫（默认）
0111	200赫兹
1000	100赫兹
1001	50Hz
1010	25Hz
1011	12.5赫兹
1100	保留
1101	保留
1110	保留
1111	500赫兹

陀螺仪满量程范围可通过编程寄存器组0中寄存器0x4Fh的位7:5参数GYRO_UI_FS_SEL进行选择，如下所示。

GYRO UI FS SEL_ _ _	陀螺仪满量程范围值
000	2000度每秒
001	1000度每秒
010	500度每秒
011	250度每秒
100	125度每秒
101	62.5度每秒
110	31.25度/秒
111	15.625度/秒

加速度计输出数据速率可通过编程寄存器组0中寄存器0x50h的位3:0参数ACCEL_ODR来选择，如下所示。

加速度计输出数据速率_	加速度计输出数据速率值
0000	保留
0001	32千赫（低噪声模式）
0010	16千赫（低噪声模式）
0011	8千赫（低噪声模式）
0100	4千赫（低噪声模式）
0101	2千赫（低噪声模式）
0110	1千赫（低噪声模式）（默认）
0111	200赫兹（低功耗或低噪声模式）
1000	100赫兹（低功耗或低噪声模式）
1001	50赫兹（低功耗或低噪声模式）
1010	25赫兹（LP或LN模式）

1011	12.5Hz (LP or LN mode)
1100	6.25Hz (LP mode)
1101	3.125Hz (LP mode)
1110	1.5625Hz (LP mode)
1111	500Hz (LP or LN mode)

Accelerometer FSR can be selected by programming the parameter ACCEL_UI_FS_SEL in register bank 0, register 0x50h, bits 7:5 as shown below.

ACCEL_UI_FS_SEL	Accelerometer FSR Value
000	16g
001	8g
010	4g
011	2g
100	Reserved
101	Reserved
110	Reserved
111	Reserved

1011	12.5赫兹 (低通模式或线性模式)
1100	6.25赫兹 (低通模式)
1101	3.125赫兹 (低通模式)
1110	1.5625赫兹（低通模式）
1111	500赫兹（低通或线性模式）

可通过编程寄存器组0中的寄存器0x50h的位7:5参数ACCEL_UI_FS_SEL来选择加速度计满量程范围，如下所示。

ACCEL UI FS SEL	加速度计满量程范围值
000	16g
001	8g
010	4g
011	2g
100	保留
101	保留
110	保留
111	保留

6 FIFO

The ICM-42688-P contains a 2K byte FIFO register that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO.

6.1 PACKET STRUCTURE

The following figure shows the FIFO packet structures supported in ICM-42688-P. Base data format for gyroscope and accelerometer is 16-bits per element. 20-bits data format support is included in one of the packet structures. When 20-bits data format is used, gyroscope data consists of 19-bits of actual data and the LSB is always set to 0, accelerometer data consists of 18-bits of actual data and the two lowest order bits are always set to 0. When 20-bits data format is used, the only FSR settings that are operational are ±2000dps for gyroscope and ±16g for accelerometer, even if the FSR selection register settings are configured for other FSR values. The corresponding sensitivity scale factor values are 131 LSB/dps for gyroscope and 8192 LSB/g for accelerometer.

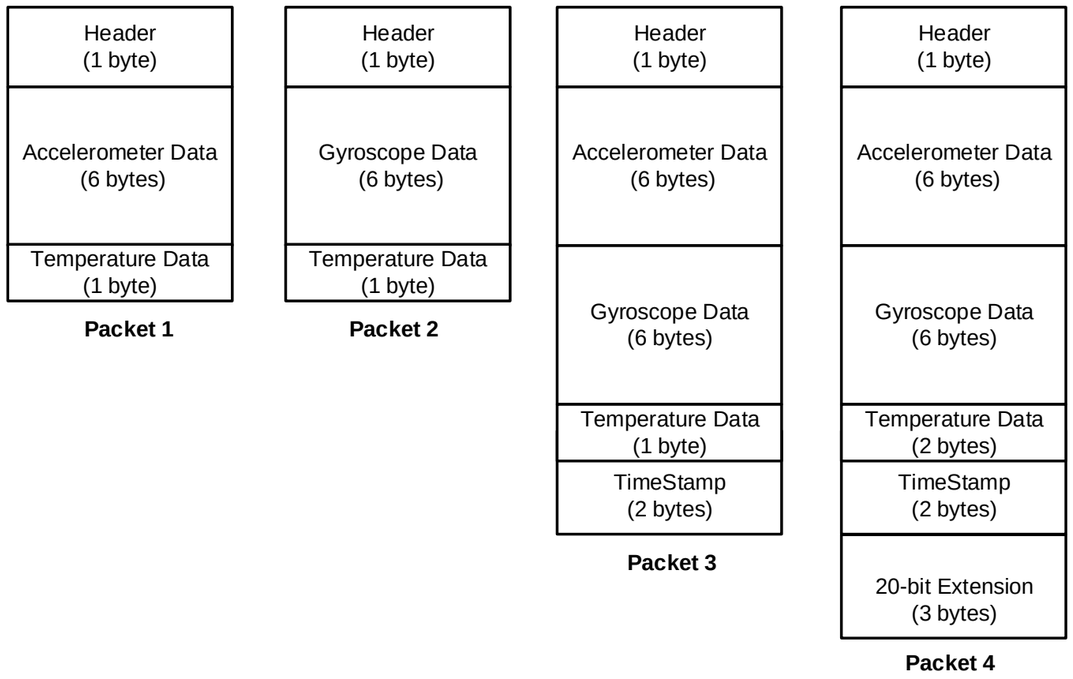


Figure 10. FIFO Packet Structure

The rest of this sub-section describes how individual data is packaged in the different FIFO packet structures.

6 FIFO

ICM-42688-P包含一个可通过串行接口访问的2K字节FIFO寄存器。FIFO配置寄存器决定哪些数据被写入FIFO。可选数据包括陀螺仪数据、加速度计数据、温度读数及FSYNC输入。FIFO计数器用于追踪FIFO中有效数据的字节数。

6.1 数据包结构

下图展示了ICM-42688-P支持的FIFO数据包结构。陀螺仪和加速度计的基础数据格式为每元素16位。其中一种数据包结构包含20位数据格式支持。当使用20位数据格式时，陀螺仪数据由19位实际数据组成且最低有效位恒置0，加速度计数据由18位实际数据组成且最低两个阶数位恒置0。使用20位数据格式时，唯一可操作的FSR设置为陀螺仪±2000度/秒和加速度计±16g，即使FSR选择寄存器配置了其他FSR值。对应的灵敏度比例因子值为陀螺仪131 LSB/度/秒和加速度计8192 LSB/g。

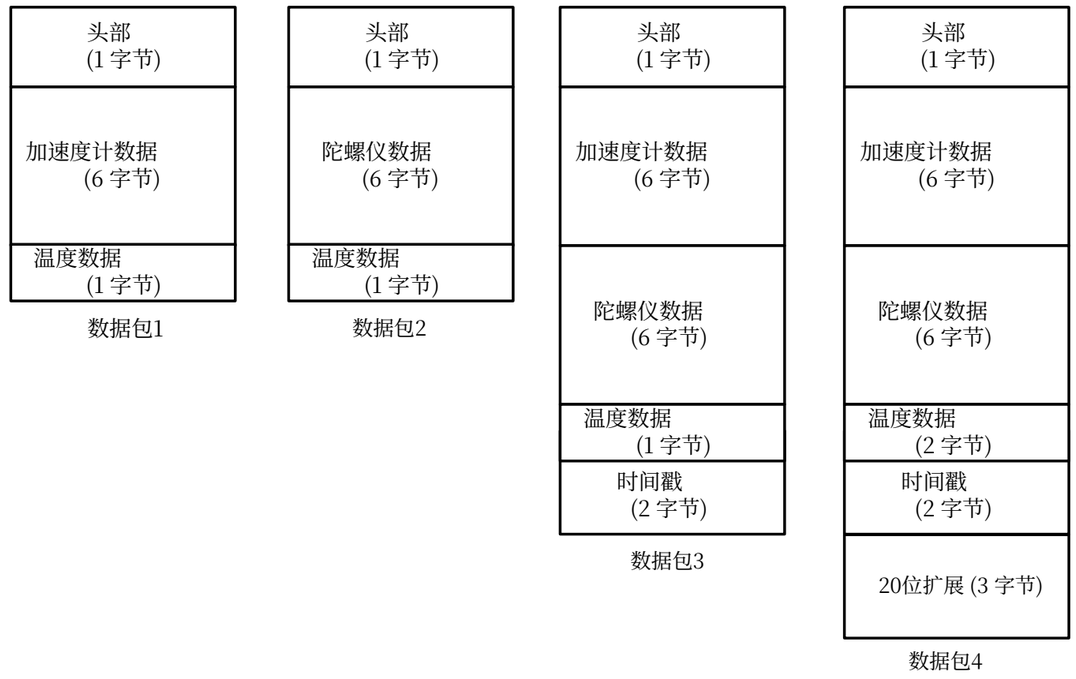


图10. FIFO数据包结构

本小节剩余部分将描述个体数据如何在不同FIFO数据包结构中封装。

Packet 1: Individual data is packaged in Packet 1 as shown below.

Byte	Content
0x00	FIFO Header
0x01	Accel X [15:8]
0x02	Accel X [7:0]
0x03	Accel Y [15:8]
0x04	Accel Y [7:0]
0x05	Accel Z [15:8]
0x06	Accel Z [7:0]
0x07	Temperature[7:0]

Packet 2: Individual data is packaged in Packet 2 as shown below.

Byte	Content
0x00	FIFO Header
0x01	Gyro X [15:8]
0x02	Gyro X [7:0]
0x03	Gyro Y [15:8]
0x04	Gyro Y [7:0]
0x05	Gyro Z [15:8]
0x06	Gyro Z [7:0]
0x07	Temperature[7:0]

Packet 3: Individual data is packaged in Packet 3 as shown below.

Byte	Content
0x00	FIFO Header
0x01	Accel X [15:8]
0x02	Accel X [7:0]
0x03	Accel Y [15:8]
0x04	Accel Y [7:0]
0x05	Accel Z [15:8]
0x06	Accel Z [7:0]
0x07	Gyro X [15:8]
0x08	Gyro X [7:0]
0x09	Gyro Y [15:8]
0x0A	Gyro Y [7:0]
0x0B	Gyro Z [15:8]
0x0C	Gyro Z [7:0]
0x0D	Temperature[7:0]
0x0E	TimeStamp[15:8]
0x0F	TimeStamp[7:0]

数据包1: 个体数据封装在数据包1中，如下所示。

Byte	内容
0x00	FIFO头
0x01	加速度X轴 [15:8]
0x02	加速度X轴 [7:0]
0x03	加速度Y轴 [15:8]
0x04	加速度Y轴 [7:0]
0x05	加速度Z轴 [15:8]
0x06	加速度Z轴 [7:0]
0x07	温度[7:0]

数据包2: 个体数据封装在数据包2中，如下所示。

Byte	内容
0x00	FIFO头
0x01	陀螺仪X轴 [15:8]
0x02	陀螺仪X轴 [7:0]
0x03	陀螺仪Y轴 [15:8]
0x04	陀螺仪Y轴 [7:0]
0x05	陀螺仪Z轴 [15:8]
0x06	陀螺仪Z轴 [7:0]
0x07	温度[7:0]

数据包3: 个体数据封装在数据包3中，如下所示。

Byte	内容
0x00	FIFO头
0x01	加速度X轴 [15:8]
0x02	加速度X轴 [7:0]
0x03	加速度Y轴 [15:8]
0x04	加速度Y轴 [7:0]
0x05	加速度Z轴 [15:8]
0x06	加速度Z轴 [7:0]
0x07	陀螺仪X轴 [15:8]
0x08	陀螺仪X轴 [7:0]
0x09	陀螺仪Y轴 [15:8]
0x0A	陀螺仪Y轴 [7:0]
0x0B	陀螺仪Z轴[15:8]
0x0C	陀螺仪Z轴[7:0]
0x0D	温度[7:0]
0x0E	时间戳[15:8]
0x0F	时间戳[7:0]

Packet 4: Individual data is packaged in Packet 4 as shown below.

Byte	Content	
0x00	FIFO Header	
0x01	Accel X [19:12]	
0x02	Accel X [11:4]	
0x03	Accel Y [19:12]	
0x04	Accel Y [11:4]	
0x05	Accel Z [19:12]	
0x06	Accel Z [11:4]	
0x07	Gyro X [19:12]	
0x08	Gyro X [11:4]	
0x09	Gyro Y [19:12]	
0x0A	Gyro Y [11:4]	
0x0B	Gyro Z [19:12]	
0x0C	Gyro Z [11:4]	
0x0D	Temperature[15:8]	
0x0E	Temperature[7:0]	
0x0F	TimeStamp[15:8]	
0x10	TimeStamp[7:0]	
0x11	Accel X [3:0]	Gyro X [3:0]
0x12	Accel Y [3:0]	Gyro Y [3:0]
0x13	Accel Z [3:0]	Gyro Z [3:0]

6.2 FIFO HEADER

The following table shows the structure of the 1byte FIFO header.

Bit Field	Item	Description
7	HEADER_MSG	1: FIFO is empty 0: Packet contains sensor data
6	HEADER_ACCEL	1: Packet is sized so that accel data have location in the packet, FIFO_ACCEL_EN must be 1 0: Packet does not contain accel sample
5	HEADER_GYRO	1: Packet is sized so that gyro data have location in the packet, FIFO_GYRO_EN must be 1 0: Packet does not contain gyro sample
4	HEADER_20	1 : Packet has a new and valid sample of extended 20-bit data for gyro and/or accel 0 : Packet does not contain a new and valid extended 20-bit data
3:2	HEADER_TIMESTAMP_FSYNC	00: Packet does not contain timestamp or FSYNC time data 01: Reserved 10: Packet contains ODR Timestamp 11: Packet contains FSYNC time, and this packet is flagged as first ODR after FSYNC (only if FIFO_TMST_FSYNC_EN is 1)
1	HEADER_ODR_ACCEL	1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel
0	HEADER_ODR_GYRO	1: The ODR for gyro is different for this gyro data packet compared to the previous gyro packet 0: The ODR for gyro is the same as the previous packet with gyro

Note at least HEADER_ACCEL or HEADER_GYRO must be set for a sensor data packet to be set.

数据包4: 个体数据按如下所示封装在数据包4中。

Byte	内容	
0x00	FIFO头	
0x01	加速度X轴 [19:12]	
0x02	加速度X轴 [11:4]	
0x03	加速度Y轴 [19:12]	
0x04	加速度Y轴 [11:4]	
0x05	加速度Z轴 [19:12]	
0x06	加速度Z轴 [11:4]	
0x07	陀螺仪X轴 [19:12]	
0x08	陀螺仪X轴 [11:4]	
0x09	陀螺仪Y轴 [19:12]	
0x0A	陀螺仪Y轴 [11:4]	
0x0B	陀螺仪Z轴 [19:12]	
0x0C	陀螺仪Z轴 [11:4]	
0x0D	温度[15:8]	
0x0E	温度[7:0]	
0x0F	时间戳[15:8]	
0x10	时间戳[7:0]	
0x11	加速度计X轴[3:0]	陀螺仪X轴[3:0]
0x12	加速度Y轴 [3:0]	陀螺仪Y轴 [3:0]
0x13	加速度Z轴 [3:0]	陀螺仪Z轴 [3:0]

6.2 FIFO头

以下表格展示了1字节FIFO头的结构。

位域	Item	描述
7	头部信息_	1: 先进先出队列为空 0: 数据包包含传感器数据
6	头部加速度计_	1: 数据包大小确保加速度数据在数据包中有固定位置，先进先出 加速度计使能_ _ 必须为1 0: 数据包不包含加速度样本
5	头部陀螺仪_	1: 数据包大小确保陀螺仪数据在数据包中有固定位置，先进先出_陀螺仪_使能必须为1 0: 数据包不包含陀螺仪样本
4	头部 20_	1 : 数据包包含陀螺仪和/或加速度计的新有效扩展20位数据样本 0 : 数据包不包含新的有效扩展20位数据
3:2	头部 _时间戳 _帧同步	00: 数据包不包含时间戳或帧同步时间数据 01: 保留 10: 数据包包含ODR时间戳 11: 数据包包含帧同步时间，且此数据包标记为帧同步后的首个ODR (仅当FIFO_TMST_FSYNC_EN为1时)
1	头部ODR加速度_ _	1: 此加速度数据包的ODR与前一包不同 加速度计数据包 0: 加速度计的输出数据速率与前一加速度计数据包相同
0	头部 _ODR_GYRO	1: 陀螺仪的输出数据速率与前一陀螺仪数据包不同 陀螺仪数据包 0: 陀螺仪的输出数据速率与前一陀螺仪数据包相同

注意：传感器数据包中必须至少设置HEADER_加速度计或HEADER_陀螺仪。

6.3 MAXIMUM FIFO STORAGE

The maximum number of packets that can be stored in FIFO is a variable quantity depending on the use case. As shown in the figure below, the physical FIFO size is 2048 bytes. A number of bytes equal to the packet size selected (see section 6.1) is reserved to prevent reading a packet during write operation. Additionally, a read cache 2 packets wide is available.

When there is no serial interface operation, the read cache is not available for storing packets, being fed by the serial interface clock.

When serial interface operation happens, depending on the operation length and the packet size chosen, either 1 or 2 of the packet entries in read cache may become available for storing packets. In that case the total storage available is up to the maximum number of packets that can be accommodated in 2048 (2040 in case of 20 bytes packets) bytes + 1 packet size, depending on the packet size used.

Due to the non-deterministic nature of system operation, driver memory allocation should always be the largest size of 2080 bytes.

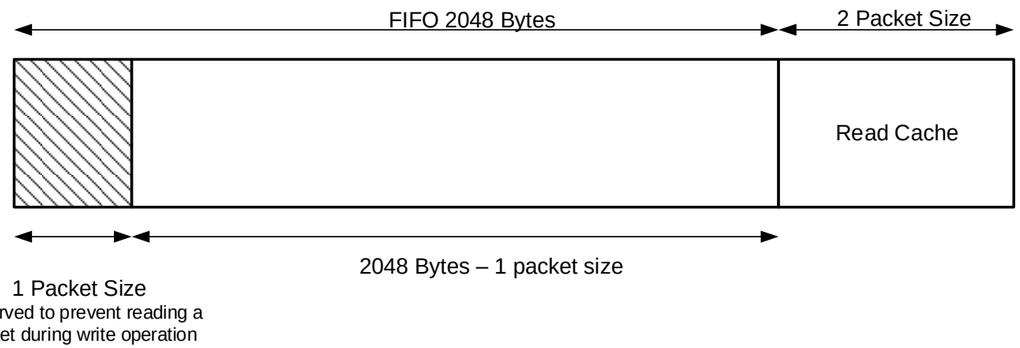


Figure 11. Maximum FIFO Storage

6.4 FIFO CONFIGURATION REGISTERS

The following control bits in bank 0, register 0x5Fh determine what data is placed into the FIFO. The values of these bits may change while the FIFO is being filled without corruption of the FIFO.

BIT	NAME	FUNCTION
4	FIFO_HIRES_EN	0: Default setting; Sensor data have regular resolution 1: Sensor data in FIFO will have extended resolution enabling the 20 Bytes packet with priority on other setting below
3	FIFO_TMST_FSYNC_EN	0: FIFO will only contain ODR timestamp information 1: FIFO can also contain FSYNC time and FSYNC flag for one ODR after an FSYNC event
1	FIFO_GYRO_EN	0: Default setting; Gyroscope data not placed into FIFO 1: Enables gyroscope data packets of 6-bytes to be placed in FIFO
0	FIFO_ACCEL_EN	0: Default setting; Accelerometer data not placed into FIFO 1: Enables accelerometer data packets of 6-bytes to be placed in FIFO

Configuration register settings above impact FIFO header and FIFO packet size as follows:

6.3 最大FIFO存储

FIFO中可存储的数据包最大数量是一个根据使用场景而定的变量。如下图所示，物理FIFO大小为2048字节。为防止在写入操作期间读取数据包，会预留等于所选数据包大小的字节数（参见第6.1节）。此外，还提供一个2个数据包宽度的读取缓存。

当没有串行接口操作时，读取缓存不可用于存储数据包，因为它由串行接口时钟驱动。

当串行接口操作发生时，根据操作长度和所选的数据包大小，读取缓存中可能有1或2个数据包条目可用于存储数据包。此时，可用存储总量最多可达2048字节（若使用20字节数据包则为2040字节）+ 1 数据包大小所能容纳的最大数据包数量，具体取决于所使用的数据包大小。

由于系统操作的非确定性，驱动程序内存分配应始终保持最大2080字节的容量。

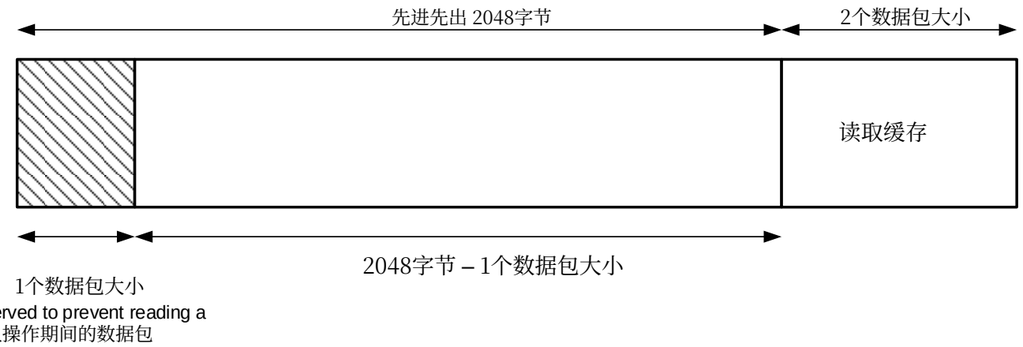


图11. 最大FIFO存储

6.4 FIFO配置寄存器

存储区0中的寄存器0x5Fh内的以下控制位决定了哪些数据会被存入FIFO。在FIFO填充过程中，这些位的值可能会发生变化，但不会导致FIFO数据损坏。

BIT	NAME	功能
4	FIFO 高分辨率_EN	0: 默认设置；传感器数据采用常规分辨率 1: FIFO中的传感器数据将采用扩展分辨率，启用20字节数据包，优先于下方其他设置
3	FIFO TMST FSY使能	0: FIFO将仅包含ODR时间戳信息 1: 先进先出队列在帧同步事件后还可包含一个输出数据速率周期的帧同步时间及帧同步标志
1	先进先出队列 陀螺仪使能	0: 默认设置；陀螺仪数据不存入先进先出队列 1: 启用将6字节的陀螺仪数据包存入先进先出队列
0	先进先出队列 加速度计 使能	0: 默认设置；加速度计数据不存入先进先出队列 1：使能6字节的加速度计数据包放入先进先出队列

上述配置寄存器设置会影响FIFO头部和先进先出包大小如下：

FIFO_HIRES_EN	FIFO_ACCEL_EN	FIFO_GYRO_EN	FIFO_TMST_FSYNC_EN	Header	Packet size
1	X	X	0	8’b_0111_10xx	20 Bytes
1	X	X	1	8’b_0111_11xx	20 Bytes
0	1	1	0	8’b_0110_10xx	16 Bytes
0	1	1	1	8’b_0110_11xx	16 Bytes
0	1	0	X	8’b_0100_00xx	8 Bytes
0	0	1	X	8’b_0010_00xx	8 Bytes
0	0	0	X	No FIFO writes	No FIFO writes

FIFO高分辨率使能 _ _	FIFO加速度计使能 _ _	FIFO陀螺仪使能 _ _	先进先出 时间戳_ _ 帧同步 _EN	头部	数据包大小
1	X	X	0	8位二进制_0111_10xx	20字节
1	X	X	1	8位二进制_0111_11xx	20字节
0	1	1	0	8位二进制_0110_10xx	16字节
0	1	1	1	8位二进制_0110_11xx	16字节
0	1	0	X	8位二进制_0100_00xx	8字节
0	0	1	X	8位二进制0010_00xx	8字节
0	0	0	X	无FIFO写入	无FIFO写入

7 PROGRAMMABLE INTERRUPTS

The ICM-42688-P has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, ICM-42688-P includes In-band Interrupt (IBI) support for the I3C^{SM} interface.

7 可编程中断

ICM-42688-P拥有一个可编程中断系统，可在INT引脚上生成中断信号。状态标志指示中断源。中断源可单独启用或禁用。有两个中断输出。如寄存器部分所述，任何中断均可映射至任一中断引脚。中断提供以下配置选项

- INT1和INT2可配置为推挽或开漏
- 电平或脉冲模式
- 高电平有效或低电平有效

此外，ICM-42688-P还包含针对I3C^{SM} 接口的带内中断(IBI)支持。

8 APEX MOTION FUNCTIONS

The APEX (**A**dvanced **P**edometer and **E**vent Detection – ne**X**t gen) features ICM-42688-P consist of:

- Pedometer: Tracks Step count and issues a Step Detect Interrupt
- Tilt Detection: Issues an interrupt when the Tilt angle exceeds 35 degrees for more than a programmable time.
- Raise to Wake/Sleep: Gesture detection for wake and sleep events. Interrupt is issued when either of these two events are detected.
- Tap Detection: Issues an interrupt when Tap is detected, along with a register containing the Tap Count.
- Wake on Motion (WoM): Detects motion when accelerometer samples exceed a programmable threshold. This motion event can be used to enable chip operation from sleep mode.
- Significant Motion Detector (SMD): Detects motion if WoM events are detected during a programmable time window (2s or 4s).

8.1 APEX ODR SUPPORT

APEX algorithms are designed to work with the accelerometer, for a variety of ODR settings. However, there is a minimum ODR required for each algorithm. The following table shows the relationship between the available accelerometer ODRs and the operation of the APEX algorithms. In order to allow more flexible operation where we can control the ODR of the APEX algorithms independent of the accelerometer ODR, we allow for an additional selection determined by the field DMP_ODR. The tables below shows how DMP_ODR should be configured in relation to the accelerometer ODR and the expected performance.

Accel ODR	DMP_ODR	Tap Detection	Pedometer	Tilt Detection	Raise to Wake/Sleep
< 25Hz	X	Disabled	Disabled	Disabled	Disabled
≥ 25Hz	0 (25Hz)	Disabled	Low Power	Low Power	Enabled
≥ 50Hz	2 (50Hz)	Disabled	Normal	Normal	Enabled

Accel ODR	Tap Detection
200Hz	Low Power
500Hz	Normal
1kHz	High Performance
> 1kHz	Disabled

If the accelerometer ODR is set below the minimum DMP ODR (25 Hz), the APEX features cannot be enabled.

When the accelerometer ODR needs to be set differently from the DMP ODR, only the integer multiple of DMP ODR for accelerometer sensor ODR is suitable to use with DMP. For example, when the accelerometer ODR is set as 200 Hz, the APEX features can be enabled with choices of 25 Hz, or 50 Hz, depending on the DMP_ODR register setting.

DMP ODR should not be changed on the fly. The following sequence should be followed for changing the DMP ODR:

8 APEX运动功能

顶点(**高级计步器**与**事件**检测–**次**世代)特性ICM-42688-P包含以下功能：

- 计步器：追踪步数计数并触发步进检测中断
- 倾斜检测：当倾斜角度超过35度并持续超过可编程时间时，触发中断。
- 抬手唤醒/睡眠：用于唤醒和睡眠事件的手势检测。当检测到这两个事件中的任意一个时，触发中断。

- 轻敲检测：检测到轻敲时触发中断，同时寄存器中记录轻触计数。
- 动作唤醒(WoM)：当加速度计采样超过可编程阈值时检测运动。该运动事件可用于从睡眠模式启用芯片操作。

- 显著动作检测器(SMD)：如果在可编程时间窗口（2秒或4秒）内检测到WoM事件，则判定为运动。

8.1 APEX ODR支持

APEX算法设计用于与加速度计协同工作，支持多种输出数据速率设置。但每种算法均有其最低输出数据速率要求。下表展示了可用加速度计输出数据速率与APEX算法运行状态之间的对应关系。为实现更灵活的控制——使APEX算法的输出数据速率可独立于加速度计输出数据速率进行调节——我们通过DMP_ODR字段提供了额外选择项。下方表格说明了DMP_ODR应如何根据加速度计输出数据速率进行配置及其预期性能表现。

加速度计输出数据速率	数字运动处理器输出数据速率	敲击检测	计步器	倾斜检测	抬手唤醒/睡眠
< 25赫兹	X	禁用	禁用	禁用	禁用
≥ 25赫兹	0 (25赫兹)	禁用	低功耗	低功耗	启用
≥ 50赫兹	2 (50赫兹)	禁用	正常	正常	启用

加速度计输出数据速率	敲击检测
200赫兹	低功耗
500赫兹	正常
1kHz	高性能
> 1千赫	禁用

若加速度计输出数据速率设置低于数字运动处理器输出数据速率最小值（25赫兹），则无法启用APEX功能。

当需要将加速度计输出数据速率与数字运动处理器输出数据速率设为不同值时，仅采用数字运动处理器输出数据速率的整数倍作为加速度传感器输出数据速率方可与数字运动处理器兼容。例如，当加速度计输出数据速率设为200赫兹时，根据DMP_输出数据速率寄存器设置，可选择25赫兹或50赫兹以启用APEX功能。

数字运动处理器输出数据速率不应在运行时更改。更改数字运动处理器输出数据速率时应遵循以下步骤：

1. Disable Pedometer, and Tilt Detection if they are enabled
2. Change DMP ODR
3. Set DMP_INIT_EN for one cycle (Register 0x4Bh in Bank 0)
4. Unset DMP_INIT_EN (Register 0x4Bh in Bank 0)
5. Enable APEX features of interest

8.2 DMP POWER SAVE MODE

DMP Power Save Mode can be enabled or disabled by DMP_POWER_SAVE (Register 0x56h in Bank 0). When the DMP Power Save Mode is enabled, APEX features are enabled only when WOM is detected. WOM must be explicitly enabled for the DMP to work in this mode. When WOM is not detected the APEX features are on pause. If the user does not want to use DMP Power Save Mode they may set DMP_POWER_SAVE = 0, and use APEX functions without WOM detection.

8.3 PEDOMETER PROGRAMMING

- Pedometer configuration parameters
  1. LOW_ENERGY_AMP_TH_SEL (Register 0x40h in Bank 4)
  2. PED_AMP_TH_SEL (Register 0x41h in Bank 4)
  3. PED_STEP_CNT_TH_SEL (Register 0x41h in Bank 4)
  4. PED_HI_EN_TH_SEL (Register 0x42h in Bank 4)
  5. PED_SB_TIMER_TH_SEL (Register 0x42h in Bank 4)
  6. PED_STEP_DET_TH_SEL (Register 0x42h in Bank 4)
  7. SENSITIVITY_MODE (Register 0x48h in Bank 4)
  8. There are 2 ODR and 2 sensitivity modes

Accel ODR (DMP_ODR)	normal	slow walk
25 Hz (0)	low power	low power and slow walk
50 Hz (2)	high performance	slow walk

- Initialize Sensor in a typical configuration
  1. Set accelerometer ODR to 50 Hz (Register 0x50h in Bank 0)
  2. Set accelerometer to Low Power mode (Register 0x4Eh in Bank 0)
     ACCEL_MODE = 2 and (Register 0x4Eh in Bank 0), ACCEL_LP_CLK_SEL = 0, for low power mode
  3. Set DMP ODR = 50 Hz and turn on Pedometer feature (Register 0x56h in Bank 0)
  4. Wait 1 millisecond

- Initialize APEX hardware
  1. Set DMP_MEM_RESET_EN to 1 (Register 0x4Bh in Bank 0)
  2. Wait 1 millisecond
  3. Set LOW_ENERGY_AMP_TH_SEL to 10 (Register 0x40h in Bank 4)
  4. Set PED_AMP_TH_SEL to 8 (Register 0x41h in Bank 4)
  5. Set PED_STEP_CNT_TH_SEL to 5 (Register 0x41h in Bank 4)
  6. Set PED_HI_EN_TH_SEL to 1 (Register 0x42h in Bank 4)
  7. Set PED_SB_TIMER_TH_SEL to 4 (Register 0x42h in Bank 4)
  8. Set PED_STEP_DET_TH_SEL to 2 (Register 0x42h in Bank 4)
  9. Set SENSITIVITY_MODE to 0 (Register 0x48h in Bank 4)
  10. Set DMP_INIT_EN to 1 (Register 0x4Bh in Bank 0)
  11. Wait 50 milliseconds
  12. Enable STEP detection, source for INT1 by setting bit 5 in register INT_SOURCE6 (Register 0x4Dh in Bank 4) to 1. Or if INT2 is selected for STEP detection, enable STEP detection source by setting bit 5 in register INT_SOURCE7 (Register 0x4Eh in Bank 4) to 1.
  13. Turn on Pedometer feature by setting PED_ENABLE to 1 (Register 0x56h in Bank 0)

1. 若计步器与倾斜检测功能处于启用状态，则将其禁用
2. 更改数字运动处理器输出数据速率
3. 设置DMP_INIT_EN为一个周期（Bank 0中的寄存器0x4B）
4. 取消设置DMP_初始化_使能 (Bank 0中的寄存器0x4B)
5. 启用感兴趣的APEX功能

8.2 DMP省电模式

DMP省电模式可通过DMP_POWER_SAVE（Bank 0中的寄存器0x56h）启用或禁用。当DMP省电模式启用时，APEX功能仅在检测到WOM时启用。必须显式启用WOM才能使DMP在此模式下工作。当未检测到WOM时，APEX功能处于暂停状态。如果用户不想使用DMP省电模式，可以设置DMP_POWER_SAVE= 0，并在无需WOM检测的情况下使用APEX功能。

8.3 计步器编程

- 计步器配置参数
  1. 低_能量_放大器_阈值_选择 (Bank 4中的寄存器0x40)
  2. PED_放大器_阈值_选择 (Bank 4中的寄存器0x41)
  3. PED_步进_计数_阈值_选择 (Bank 4中的寄存器0x41)
  4. PED_高_使能_阈值_选择 (Bank 4 中的寄存器 0x42h)
  5. PED_SB_定时器_阈值_选择 (Bank 4 中的寄存器 0x42h)
  6. PED_步进_检测_阈值_选择 (Bank 4 中的寄存器 0x42h)
  7. 灵敏度_模式 (Bank 4 中的寄存器 0x48h)
  8. 有2种输出数据速率和2种灵敏度模式

加速度计输出数据速率 (DMP_ODR)	正常	慢走
25赫兹 (0)	低功耗	低功耗与慢走
50赫兹 (2)	高性能	慢走

- 以典型配置初始化传感器
  1. 设置加速度计输出数据速率为50赫兹 (寄存器0x50h在Bank 0)
  2. 将加速度计设置为低功耗模式（Bank 0中的寄存器0x4Eh）
     加速度计_模式 = 2 和（Bank 0中的寄存器0x4Eh），加速度计_低通_时钟_选择 = 0，用于低功耗模式
  3. 设置DMP输出数据速率 = 50 赫兹并开启计步器功能（Bank 0中的寄存器0x56h）
  4. 等待1毫秒

- 初始化APEX硬件件
  1. 设置DMP内存_ _重置_使能为1 (Bank 0中的寄存器0x4B)
  2. 等待1毫秒
  3. 设置LOW_能量_放大器_阈值_选择为10 (Bank 4中的寄存器0x40)
  4. 设置PED_放大器_阈值_选择为8 (Bank 4中的寄存器0x41)
  5. 设置PED_步进_计数_阈值_选择为5 (Bank 4中的寄存器0x41)
  6. 设置PED _HI_EN_TH_将SEL设置为1 (Bank 4 中的寄存器 0x42h)
  7. 设置PED_SB_TIMER_TH_SEL为4 (Bank 4 中的寄存器 0x42h)
  8. 设置PED_STEP_DET_TH_SEL为2 (Bank 4 中的寄存器 0x42h)
  9. 设置SENSITIVITY_MODE为0 (Bank 4 中的寄存器 0x48h)
  10. 设置DMP_INIT_EN为1 (Bank 0中的寄存器0x4B)
  11. 等待50毫秒
  12. 通过将寄存器INT_SOURCE6（Bank 4中的寄存器0x4Dh）的第5位设置为1，启用步数检测功能，并作为INT1的中断源。若选择INT2进行步数检测，则通过将寄存器INT_SOURCE7（Bank 4中的寄存器0x4Eh）的第5位设置为1来启用步数检测源。
  13. 通过将PED_ENABLE设置为1（Bank 0中的寄存器0x56h）来开启计步器功能。

- Output registers
  1. Read interrupt register (Register 0x38h in Bank 0) for STEP_DET_INT
  2. If the step count is equal to or greater than 65535 (uint16), the STEP_CNT_OVF_INT (Register 0x38h in Bank 0) will be set to 1. Example:
     - Take 1 step =>output step count = 65533 (real step count is 65533)
     - Take 1 step => output step count = 65534 (real step count is 65534)
     - Take 1 step => output step count = 0 and interrupt is fired (real step count is 65535+0= 65535)
     - Take 1 step => output step count = 1 (real step count is 65535+1=65536)
  3. Read the step count in STEP_CNT (Register 0x31h and 0x32h in Bank 0)
  4. Read the step cadence in STEP_CADENCE (Register 0x33h in Bank 0)
  5. Read the activity class in ACTIVITY_CLASS (Register 0x34h in Bank 0)

8.4 TILT DETECTION PROGRAMMING

- Tilt Detection configuration parameters
  1. TILT_WAIT_TIME (Register 0x43h in Bank 4)
     This parameter configures how long of a delay after tilt is detected before interrupt is triggered
     Default is 2 (4 s).
     Range is 0 = 0 s, 1 = 2 s, 2 = 4 s, 3 = 6 s
     For example, setting TILT_WAIT_TIME = 2 is equivalent to 4 seconds for all ODRs

- Initialize Sensor in a typical configuration
  1. Set accelerometer ODR (Register 0x50h in Bank 0)
     ACCEL_ODR = 9 for 50 Hz or 10 for 25 Hz
  2. Set Accel to Low Power mode (Register 0x4Eh in Bank 0)
     ACCEL_MODE = 2 and (Register 0x4Dh in Bank 0), ACCEL_LP_CLK_SEL = 0, for low power mode
  3. Set DMP ODR (Register 0x56h in Bank 0)
     DMP_ODR = 0 for 25 Hz, 2 for 50 Hz
  4. Wait 1 millisecond

- Initialize APEX hardware
  1. Set DMP_MEM_RESET_EN to 1 (Register 0x4Bh in Bank 0)
  2. Wait 1 millisecond
  3. Set TILT_WAIT_TIME (Register 0x43h in Bank 4) if default value does not meet needs
  4. Wait 1 millisecond
  5. Set DMP_INIT_EN to 1 (Register 0x4Bh in Bank 0)
  6. Enable Tilt Detection, source for INT1 by setting bit 3 in register INT_SOURCE6 (Register 0x4Dh in Bank 4) to 1. Or if INT2 is selected for Tilt Detection, enable Tilt Detection source by setting bit 3 in register INT_SOURCE7 (Register 0x4Eh in Bank 4) to 1.
  7. Wait 50 milliseconds
  8. Turn on Tilt Detection feature by setting TILT_ENABLE to 1 (Register 0x56h in Bank 0)

- Output registers
  1. Read interrupt register (Register 0x38h in Bank 0) for TILT_DET_INT

8.5 RAISE TO WAKE/SLEEP PROGRAMMING

- Raise to Wake/Sleep configuration parameters
  1. SLEEP_TIME_OUT (Register 0x43h in Bank 4)
  2. MOUNTING_MATRIX (Register 0x44h in Bank 4)
  3. SLEEP_GESTURE_DELAY (Register 0x45h in Bank 4)

- Initialize Sensor in a typical configuration
  1. Set accelerometer ODR (Register 0x50h in Bank 0)
     ACCEL_ODR = 10 for 25 Hz

- 输出寄存器
  1. 读取中断寄存器 (Bank 0 中的寄存器 0x38h) 以获取STEP_DET_INT
  2. 如果步数计数等于或超过65535 (无符号16位整数)，STEP_CNT_OVF_INT (Bank 0 中的寄存器 0x38h) 将被设置为1。示例:
     - 迈出1步=>输出步数计数= 65533 (实际步数计数为65533)
     - 迈出1步=> 输出步数计数= 65534 (实际步数计数为65534)
     - 迈出1步=> 输出步数计数= 0 并触发中断(实际步数计数为65535+0= 65535)
     - 迈出1步=> 输出步数计数= 1 (实际步数计数为65535+1=65536)
  3. 读取STEP_CNT中的步数计数(Bank 0中的寄存器0x31h和0x32h)
  4. 读取STEP_CADENCE中的步频(Bank 0中的寄存器0x33h)
  5. 读取活动类别ACTIVITY_CLASS（Bank 0中的寄存器0x34h）

8.4 倾斜检测编程

- 倾斜检测配置参数
  1. TILT_WAIT_TIME（Bank 4 中的寄存器 0x43h）
     此参数配置检测到倾斜后延迟多长时间触发中断，默认值为2（4秒）。

     范围为0 = 0 秒、1 = 2 秒、2 = 4 秒、3 = 6 秒
     例如，设置TILT_WAIT_TIME = 2 相当于所有输出数据速率下的4秒

- 以典型配置初始化传感器
  1. 设置加速度计输出数据速率（Bank 0中的寄存器0x50h）
     加速度计_输出数据速率= 9 为50赫兹或10为25赫兹
  2. 设置加速度计为低功耗模式（Bank 0中的寄存器0x4Eh）
     加速度计_模式 = 2 和（Bank 0中的寄存器0x4Dh），加速度计_低通_时钟_选择 = 0，用于低功耗模式
  3. 设置数字运动处理器输出数据速率（Bank 0中的寄存器0x56h）
     DMP_输出数据速率 = 0 对应25赫兹，2对应50赫兹
  4. 等待1毫秒

- 初始化APEX硬件
  1. 设置DMP_MEM_将_使能设为1（Bank 0中的寄存器0x4B）
  2. 等待1毫秒
  3. 设置TILT_若默认值不满足需求，则等待_时间（Bank 4 中的寄存器 0x43h）
  4. 等待1毫秒
  5. 设置DMP_INIT_EN为1（Bank 0中的寄存器0x4B）
  6. 启用倾斜检测，通过将寄存器INT_SOURCE6（Bank 4中的寄存器0x4D）的位3设为1来设置INT1的来源。或者如果选择INT2进行倾斜检测，通过将寄存器INT_SOURCE7（Bank 4中的寄存器0x4E）的位3设为1来启用倾斜检测来源。
  7. 等待50毫秒
  8. 通过将TILT_ENABLE设为1（Bank 0中的寄存器0x56h）来开启倾斜检测功能

- 输出寄存器
  1. 读取中断寄存器 (Bank 0 中的寄存器 0x38h) 以获取倾斜_检测_中断

8.5 抬手唤醒/睡眠编程

- 抬起唤醒/睡眠配置参数
  1. 睡眠_时间_输出 (Bank 4 中的寄存器 0x43h)
  2. 安装_矩阵 (Bank 4 中的寄存器 0x44h)
  3. 睡眠_手势_延迟 (Bank 4 中的寄存器 0x45h)

- 初始化传感器在 t yp ical confi guration
  1. 设置加速度计输出数据速率（寄存器0x50h在Bank 0）
     加速度计_输出数据速率= 10 为25赫兹

2. Set Accel to Low Power mode (Register 0x4Eh in Bank 0)
   ACCEL_MODE = 2 and (Register 0x4Dh in Bank 0), ACCEL_LP_CLK_SEL = 0, for low power mode
3. Set DMP ODR (Register 0x56h in Bank 0)
   DMP_ODR = 0 for 25 Hz, 2 for 50 Hz
4. Wait 1 millisecond

- Initialize APEX hardware
  1. Set DMP_MEM_RESET_EN to 1 (Register 0x4Bh in Bank 0)
  2. Wait 1 millisecond
  3. Set SLEEP_TIME_OUT (Register 0x43h in Bank 4) if default value does not meet needs
  4. Wait 1 millisecond
  5. Set MOUNTING_MATRIX (Register 0x44h in Bank 4) if default value does not meet needs
  6. Wait 1 millisecond
  7. Set SLEEP_GESTURE_DELAY (Register 0x45h in Bank 4) if default value does not meet needs
  8. Wait 1 millisecond
  9. Set DMP_INIT_EN to 1 (Register 0x4Bh in Bank 0)
  10. Enable Raise to Wake/Sleep, source for INT1 by setting bit 2,1 in register INT_SOURCE6 (Register 0x4Dh in Bank 4) to 1. Or if INT2 is selected for Raise to Wake/Sleep, enable Raise to Wake/Sleep source by setting bit 2,1 in register INT_SOURCE7 (Register 0x4Eh in Bank 4) to 1.
  11. Wait 50 milliseconds
  12. Turn on Raise to Wake/Sleep feature by setting R2W_EN to 1 (Register 0x56h in Bank 0)

- Output registers
  1. Read interrupt register (Register 0x38h in Bank 0) for WAKE_INT, SLEEP_INT

8.6 TAP DETECTION PROGRAMMING

- Tap Detection configuration parameters
  1. TAP_TMAX (Register 0x47h in Bank 4)
  2. TAP_TMIN (Register 0x47h in Bank 4)
  3. TAP_TAVG (Register 0x47h in Bank 4)
  4. TAP_MIN_JERK_THR (Register 0x46h in Bank 4)
  5. TAP_MAX_PEAK_TOL (Register 0x46h in Bank 4)
  6. TAP_ENABLE (Register 0x56h in Bank 0)

- Initialize Sensor in a typical configuration
  1. Set accelerometer ODR (Register 0x50h in Bank 0)
     ACCEL_ODR = 15 for 500 Hz (ODR of 200Hz or 1kHz may also be used)
  2. Set power modes and filter configurations as shown below
     - For ODR up to 500Hz, set Accel to Low Power mode (Register 0x4Eh in Bank 0)
       ACCEL_MODE = 2 and ACCEL_LP_CLK_SEL = 0, (Register 0x4Dh in Bank 0) for low power mode
       Set filter settings as follows: ACCEL_DEC2_M2_ORD = 2 (Register 0x53h in Bank 0); ACCEL_UI_FILT_BW = 4 (Register 0x52h in Bank 0)
     - For ODR of 1kHz, set Accel to Low Noise mode (Register 0x4Eh in Bank 0) ACCEL_MODE = 1
       Set filter settings as follows: ACCEL_UI_FILT_ORD = 2 (Register 0x53h in Bank 0); ACCEL_UI_FILT_BW = 0 (Register 0x52h in Bank 0)
  3. Wait 1 millisecond

- Initialize APEX hardware
  1. Set TAP_TMAX to 2 (Register 0x47h in Bank 4)
  2. Set TAP_TMIN to 3 (Register 0x47h in Bank 4)
  3. Set TAP_TAVG to 3 (Register 0x47h in Bank 4)
  4. Set TAP_MIN_JERK_THR to 17 (Register 0x46h in Bank 4)
  5. Set TAP_MAX_PEAK_TOL to 2 (Register 0x46h in Bank 4)

2. 设置加速度计为低功耗模式 (Bank 0中的寄存器0x4Eh)
   加速度计_模式 = 2 及 (Bank 0中的寄存器0x4Dh), 加速度计_低通_时钟_选择 = 0, 用于低功耗模式
3. 设置DMP ODR（Bank 0中的寄存器0x56h）
   DMP ODR = 0 对应25赫兹_ , 2对应50 Hz
4. 等待1毫秒

- 初始化APEX硬件
  1. 设置DMP _MEM_重置_使能为1（Bank 0中的寄存器0x4B）
  2. 等待1毫秒
  3. 若默认值不满足需求，设置睡眠_时间_输出（Bank 4 中的寄存器 0x43h）
  4. 等待1毫秒
  5. 设置安装 _矩阵（Bank 4 中的寄存器 0x44h）若默认值不满足需求
  6. 等待1毫秒
  7. 如果默认值不满足需求，设置睡眠_手势_延迟（Bank 4 中的寄存器 0x45h）
  8. 等待1毫秒
  9. 将DMP_初始化_使能设置为1（Bank 0中的寄存器0x4B）
  10. 通过将寄存器INT_来源6（Bank 4中的寄存器0x4Dh）的位2,1设置为1，启用抬手唤醒/睡眠，并将INT1作为来源。或者如果选择INT2用于抬手唤醒/睡眠，则通过将寄存器INT_来源7（Bank 4中的寄存器0x4Eh）的位2,1设置为1来启用抬手唤醒/睡眠来源。
  11. 等待50毫秒
  12. 通过将R2W_EN设为1（Bank 0中的寄存器0x56h）来开启抬手唤醒/睡眠功能

- 输出寄存器
  1. 读取中断寄存器 (Bank 0 中的寄存器 0x38h) 以获取唤醒_中断、睡眠_中断

8.6 轻敲检测编程

- 轻敲检测配置参数
  1. TAP_TMAX（Bank 4中的寄存器0x47h）
  2. TAP_TMIN（Bank 4中的寄存器0x47h）
  3. 轻敲_平均温度 (Bank 4中的寄存器0x47h)
  4. 轻敲_最小_抖动_推力 (Bank 4中的寄存器0x46h)
  5. 轻敲_最大_峰值_容差 (Bank 4中的寄存器0x46h)
  6. 轻敲_使能 (Bank 0中的寄存器0x56h)

- 初始化传感器在技术 yp配置中 guration
  1. 设置加速度计输出数据速率（Bank 0中的寄存器0x50h）
     加速度计_输出数据速率 = 15 设为500赫兹（也可使用200赫兹或1千赫兹的输出数据速率）
  2. 按如下所示设置电源模式及滤波器配置
     - 对于输出数据速率最高至500赫兹的情况，设置加速度计为低功耗模式（Bank 0中的寄存器0x4Eh）加速度计_模式 = 2 及加速度计_低通_时钟_选择 = 0（Bank 0中的寄存器0x4Dh）以启用低功耗模式。滤波器设置如下：加速度计_抽取2_模式2_输出数据速率 = 2 （Bank 0中的寄存器0x53h）；加速度计_用户界面_滤波器_带宽 = 4（Bank 0中的寄存器0x52h）
       - 对于1千赫兹的输出数据速率，设置加速度计为低噪声模式（Bank 0中的寄存器0x4Eh）加速度计_模式 = 1。滤波器设置如下：加速度计_用户界面_滤波器_输出数据速率 = 2 （Bank 0中的寄存器0x53h）；加速度计_用户界面_滤波器_带宽 =0（Bank 0中的寄存器0x52h）
  3. 等待1毫秒

- 初始化APEX硬件
  1. 将TAP_TMAX设为2（Bank 4中的寄存器0x47h）
  2. 将TAP_TMIN设为3（Bank 4中的寄存器0x47h）
  3. 将TAP_TAVG设为3（Bank 4中的寄存器0x47h）
  4. 将TAP_MIN_JERK_THR设为17（Bank 4中的寄存器0x46h）
  5. 将轻敲_最大值_峰值_容差设置为2（Bank 4中的寄存器0x46h）

6. Wait 1 millisecond
7. Enable TAP source for INT1 by setting bit 0 in register INT_SOURCE6 (Register 0x4Dh in Bank 4) to 1. Or if INT2 is selected for TAP, enable TAP source by setting bit 0 in register INT_SOURCE7 (Register 0x4Eh in Bank 4) to 1.
8. Wait 50 milliseconds
9. Turn on TAP feature by setting TAP_ENABLE to 1 (Register 0x56h in Bank 0)

- Output registers
  1. Read interrupt register (Register 0x38h in Bank 0) for TAP_DET_INT
  2. Read the tap count in TAP_NUM (Register 0x35h in Bank 0)
  3. Read the tap axis in TAP_AXIS (Register 0x35h in Bank 0)
  4. Read the polarity of tap pulse in TAP_DIR (Register 0x35h in Bank 0)

8.7 WAKE ON MOTION PROGRAMMING

- Wake on Motion configuration parameters
  1. WOM_X_TH (Register 0x4Ah in Bank 4)
  2. WOM_Y_TH (Register 0x4Bh in Bank 4)
  3. WOM_Z_TH (Register 0x4Ch in Bank 4)
  4. WOM_INT_MODE (Register 0x57h in Bank 0)
  5. WOM_MODE (Register 0x57h in Bank 0)

- Initialize Sensor in a typical configuration
  1. Set accelerometer ODR (Register 0x50h in Bank 0)
     ACCEL_ODR = 9 for 50 Hz
  2. Set Accel to Low Power mode (Register 0x4Eh in Bank 0)
     ACCEL_MODE = 2 and (Register 0x4Dh in Bank 0), ACCEL_LP_CLK_SEL = 0, for low power mode
  3. Wait 1 millisecond

- Initialize APEX hardware
  1. Set WOM_X_TH to 98 (Register 0x4Ah in Bank 4)
  2. Set WOM_Y_TH to 98 (Register 0x4Bh in Bank 4)
  3. Set WOM_Z_TH to 98 (Register 0x4Ch in Bank 4)
  4. Wait 1 millisecond
  5. Enable all 3 axes as WOM sources for INT1 by setting bits 2:0 in register INT_SOURCE1 (Register 0x66h in Bank 0) to 1. Or if INT2 is selected for WOM, enable all 3 axes as WOM sources by setting bits 2:0 in register INT_SOURCE4 (Register 0x69h in Bank 0) to 1.
  6. Wait 50 milliseconds
  7. Turn on WOM feature by setting WOM_INT_MODE to 0, WOM_MODE to 1, SMD_MODE to 1 (Register 0x56h in Bank 0)

- Output registers
  1. Read interrupt register (Register 0x7Dh in Bank 0) for WOM_X_INT
  2. Read interrupt register (Register 0x7Dh in Bank 0) for WOM_Y_INT
  3. Read interrupt register (Register 0x7Dh in Bank 0) for WOM_Z_INT

8.8 SIGNIFICANT MOTION DETECTION PROGRAMMING

- Significant Motion Detection configuration parameters
  1. WOM_X_TH (Register 0x4Ah in Bank 4)
  2. WOM_Y_TH (Register 0x4Bh in Bank 4)
  3. WOM_Z_TH (Register 0x4Ch in Bank 4)
  4. WOM_INT_MODE (Register 0x57h in Bank 0)
  5. WOM_MODE (Register 0x57h in Bank 0)
  6. SMD_MODE (Register 0x57h in Bank 0)

- Initialize Sensor in a typical configuration

6. 等待1毫秒
7. 通过将寄存器INT_SOURCE6（Bank 4中的寄存器0x4Dh）的位0设为1，为INT1启用TAP源。若选择INT2作为TAP中断，则通过将寄存器INT_SOURCE7（Bank 4中的寄存器0x4Eh）的位0设为1来启用TAP源。
8. 等待50毫秒
9. 通过将TAP_ENABLE设为1（Bank 0中的寄存器0x56h）来开启TAP功能

- 输出寄存器
  1. 读取中断寄存器（Bank 0中的寄存器0x38h）以获取TAP_DET_INT
  2. 读取TAP_NUM（Bank 0中的寄存器0x35h）中的轻触计数
  3. 读取TAP_AXIS（Bank 0中的寄存器0x35h）中的点击轴
  4. 读取TAP_DIR（Bank 0 中的寄存器 0x35h）中的轻触脉冲极性

8.7 运动唤醒编程

- 运动唤醒配置参数
  1. WOM_X_TH（Bank 4 中的寄存器 0x4Ah）
  2. WOM_Y_TH（Bank 4 中的寄存器 0x4Bh）
  3. WOM_Z_TH（Bank 4 中的寄存器 0x4Ch）
  4. WOM_INT_MODE (第0存储区寄存器0x57h)
  5. WOM _MODE (第0存储区寄存器0x57h)

- 以典型配置初始化传感器
  1. 设置加速度计输出数据速率 (寄存器0x50h在Bank 0)
     加速度计输出数据速率 = 9 为50赫兹_
  2. 设置加速度计为低功耗模式（Bank 0中的寄存器0x4Eh）
     加速度计_模式 = 2 和（Bank 0中的寄存器0x4Dh），加速度计_低通_时钟_选择 = 0，用于低功耗模式
  3. 等待1毫秒

- 初始化APEX硬件
  1. 设置WOM_X轴_阈值为98（Bank 4 中的寄存器 0x4Ah）
  2. 设置WOM_Y轴_阈值为98（Bank 4 中的寄存器 0x4Bh）
  3. 将WOM_Z_TH设置为98（Bank 4 中的寄存器 0x4Ch）
  4. 等待1毫秒
  5. 通过设置寄存器INT_SOURCE1（Bank 0寄存器0x66h）中的位2:0，启用所有3个轴作为INT1的WOM来源设置为1。或者如果选择INT2作为WOM，通过设置寄存器INT_SOURCE4（Bank 0寄存器0x69h）中的位2:0为1，启用所有3个轴作为WOM来源。
  6. 等待50毫秒
  7. 通过将WOM_INT_MODE设置为0，WOM_MODE设置为1，SMD_MODE设置为1（寄存器0x56h在存储区0)

- 输出寄存器
  1. 读取中断寄存器（存储区0中的寄存器0x7Dh）以获取WOM_X_中断
  2. 读取中断寄存器（存储区0中的寄存器0x7Dh）以获取WOM_Y_中断
  3. 读取中断寄存器（存储区0中的寄存器0x7Dh）以获取WOM_Z_中断

8.8 显著运动检测编程

- 显著运动检测配置参数
  1. WOM_X_阈值 (Bank 4 中的寄存器 0x4Ah)
  2. WOM_Y_阈值 (Bank 4 中的寄存器 0x4Bh)
  3. WOM_Z_阈值 (Bank 4 中的寄存器 0x4Ch)
  4. WOM_中断_模式 (第0存储区寄存器0x57h)
  5. WOM_模式 (第0存储区寄存器0x57h)
  6. SMD_模式 (第0存储区寄存器0x57h)

- 以典型配置初始化传感器

1. Set accelerometer ODR (Register 0x50h in Bank 0)
   ACCEL_ODR = 9 for 50 Hz
2. Set Accel to Low Power mode (Register 0x4Eh in Bank 0)
   ACCEL_MODE = 2 and (Register 0x4Dh in Bank 0), ACCEL_LP_CLK_SEL = 0, for low power mode
3. Wait 1 millisecond

- Initialize APEX hardware
  1. Set WOM_X_TH to 98 (Register 0x4Ah in Bank 4)
  2. Set WOM_Y_TH to 98 (Register 0x4Bh in Bank 4)
  3. Set WOM_Z_TH to 98 (Register 0x4Ch in Bank 4)
  4. Wait 1 millisecond
  5. Enable SMD source for INT1 by setting bit 3 in register INT_SOURCE1 (Register 0x66h in Bank 0) to 1. Or if INT2 is selected for SMD, enable SMD source by setting bit 3 in register INT_SOURCE4 (Register 0x69h in Bank 0) to 1.
  6. Wait 50 milliseconds
  7. Turn on SMD feature by setting WOM_INT_MODE to 0, WOM_MODE to 1, SMD_MODE to 3 (Register 0x56h in Bank 0)
- Output registers
  1. Read interrupt register (Register 0x7Dh in Bank 0) for SMD_INT

1. 设置加速度计输出数据速率 (寄存器0x50h在Bank 0)
   加速度计_输出数据速率 = 9 为50赫兹
2. 设置加速度计为低功耗模式 (Bank 0中的寄存器0x4Eh)
   加速度计_模式 = 2 和 （Bank 0中的寄存器0x4Dh），加速度计_低通_时钟_选择 = 0，用于低功耗模式
3. 等待1毫秒

- 初始化APEX硬件
  1. 将WOM_X轴_阈值设为98（Bank 4 中的寄存器 0x4Ah）
  2. 将WOM_Y轴_阈值设为98（Bank 4 中的寄存器 0x4Bh）
  3. 将WOM_Z轴_阈值设为98（Bank 4 中的寄存器 0x4Ch）
  4. 等待1毫秒
  5. 通过将寄存器INT_SOURCE1（Bank 0中的寄存器0x66h）的位3设为1，为INT1启用SMD源。若选择INT2作为SMD的触发源，则通过将寄存器INT_SOURCE4（Bank 0寄存器0x69h）的位3设为1来启用SMD源。
  6. 等待50毫秒
  7. 通过设置WOM_INT_MODE为0、WOM_MODE为1、SMD_MODE为3（Bank 0寄存器0x56h）来开启SMD功能
- 输出寄存器
  1. 读取中断寄存器（存储区0中的寄存器0x7Dh）以获取显著运动检测_中断

9 DIGITAL INTERFACE

9.1 I3C^{SM}, I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-42688-P can be accessed using I3C^{SM} at 12.5MHz (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode), I^{2}C at 1 MHz or SPI at 24 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in Section 4.1.

9.2 I3C^{SM} INTERFACE

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

ICM-42688-P supports the following features of I3C^{SM}:

- SDR data rate up to 12.5Mbps
- DDR data rate up to 25Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- Support for asynchronous timing control mode 0
- Error detection (CRC and/or Parity)
- Common Command Code (CCC)

The ICM-42688-P always operates as an I3C^{SM} slave device when communicating to the system processor, which thus acts as the I3C^{SM} master. I3C^{SM} master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C^{SM} master.

9.3 I^{2}C INTERFACE

I^{2}C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^{2}C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-42688-P always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-42688-P is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two ICM-42688-Ps to be connected to the same I^{2}C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

9.4 I^{2}C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions
Communication on the I^{2}C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below). Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

9 数字接口

9.1 I3C^{SM}, I^{2}C 与 SPI串行接口

ICM-42688-P的内部寄存器和内存可通过I3C^{SM} 以12.5兆赫（SDR模式下数据速率可达12.5兆比特每秒，DDR模式下为25兆比特每秒）、I^{2}C以1兆赫或SPI以24兆赫进行访问。SPI可工作于三线制或四线制模式。串行接口的引脚分配详见章节4.1。

9.2 I3C^{SM} 接口

I3C^{SM} 是一种新型的双线数字接口，由串行数据(SDA)和串行时钟(SCLK)信号组成。I3C^{SM} 旨在改进I^{2}C接口，同时保持向后兼容性。

I3C^{SM} 继承了I2C在简单性、低引脚数、简易电路板设计和多点连接（相对于点对点）方面的优势，同时提供了SPI的更高数据速率、更简单的焊盘和更低功耗。I3C^{SM} 增加了特定频率下的更高吞吐量、带内中断（从从设备到主设备）以及动态寻址功能。

ICM-42688-P支持I3C^{SM}的以下特性：

- 单倍数据速率最高达12.5兆比特每秒
- 双倍数据速率最高达25兆比特每秒
- 动态地址分配
- 带内中断(IBI)支持
- 支持异步时序控制模式0
- 错误检测(CRC和/或奇偶校验)
- 通用命令码(CCC)

ICM-42688-P在与系统处理器通信时始终作为I3C^{SM} 从设备运行，因此系统处理器充当I3C^{SM} 主设备。I3C^{SM} 主设备控制SDA上的主动上拉电阻，可启用或禁用该电阻。上拉电阻可能是由引脚控制的板级电阻，也可能是I3C^{SM} 主设备内部的电阻。

9.3 I^{2}C接口

I^{2}C是一种由串行数据(SDA)和串行时钟(SCL)信号组成的双线接口。通常，这些线路采用开漏且双向的设计。在通用的I^{2}C接口实现中，连接的设备可以是主设备或从设备。主设备将从设备地址置于总线上，而匹配地址的从设备会向主设备发送确认信号。

当与系统处理器通信时，ICM-42688-P始终作为从设备运行，此时系统处理器充当主设备。SDA和SCL线通常需要连接至VDDIO的上拉电阻。最大总线速度为1兆赫。

ICM-42688-P的从设备地址为b110100X，长度为7位。该7位地址的最低有效位由引脚AP_AD0的逻辑电平决定。这使得两个ICM-42688-P可连接至同一I^{2}C总线。在此配置下，其中一个设备的地址应为b1101000（引脚AP_AD0为逻辑低电平），另一个设备的地址应为b1101001（引脚AP_AD0为逻辑高电平）。

9.4 输入^{2}通信协议

起始条件(S)与停止条件(P)
I^{2}C总线上的通信始于主设备在总线上放置起始条件(S)，其定义为当SCL线为高电平时SDA线发生高到低转换（参见下图）。总线被视为繁忙状态，直到主设备在总线上放置停止条件(P)，即当SCL为高电平时SDA线发生低到高转换（参见下图）。此外，如果生成的是重复起始条件(Sr)而非停止条件，总线仍保持繁忙状态。

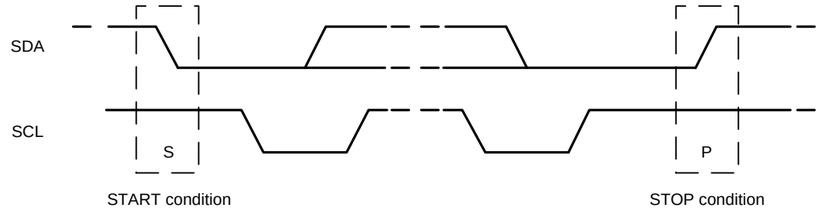


Figure 12. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

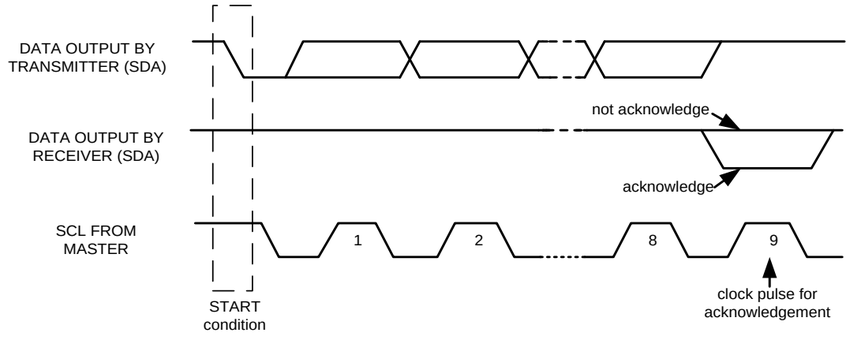


Figure 13. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

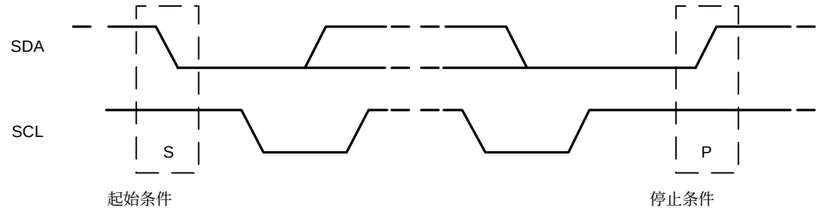


图12. 启动和停止条件

数据格式/确认

I²C数据字节定义为8位长度。每次数据传输中传输的字节数量没有限制。每个传输的字节后必须跟随一个确认(ACK)信号。确认信号的时钟由主设备生成，而接收器通过拉低SDA并在确认时钟脉冲的高电平期间保持其低电平来生成实际的确认信号。

若从设备处于忙碌状态且需完成其他任务后才能继续传输或接收数据字节，可通过保持SCL为低电平强制主设备进入等待状态。当从设备准备就绪并释放时钟线时，正常数据传输将恢复（参见下图）。

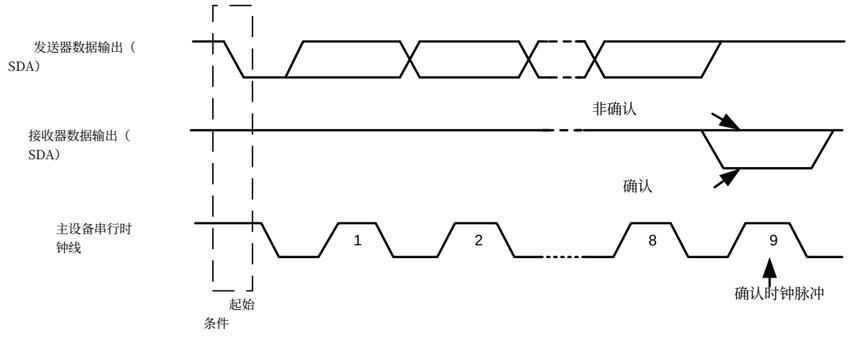


图13. I²C总线上的确认

通信

在通过起始条件(S)启动通信后，主设备发送一个7位从设备地址，后跟一个8th 位（即读/写位）。该读/写位指示主设备是从从设备接收数据还是向其写入数据。随后，主设备释放SDA线并等待从设备发回的确认信号(ACK)。每个传输的字节后必须跟随一个确认位。为确认接收，从设备会将SDA线拉低并在SCL线高电平期间保持低电平。数据传输总是由主设备通过停止条件(P)终止，从而释放通信线路。但主设备也可生成重复启动条件(Sr)，在不先产生停止条件(P)的情况下寻址另一个从设备。当SCL为高电平时，SDA线从低到高的跳变即定义为停止条件。除起始和停止条件外，所有SDA线变化都应发生在SCL为低电平期间。

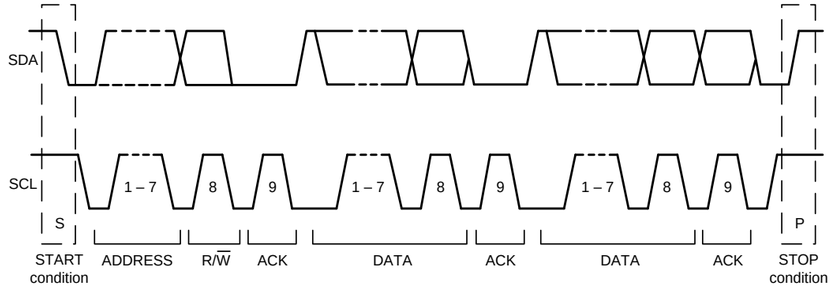


Figure 14. Complete I²C Data Transfer

To write the internal ICM-42688-P registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-42688-P acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-42688-P acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-42688-P automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-42688-P registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-42688-P, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-42688-P sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

9.5 I²C TERMS

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address

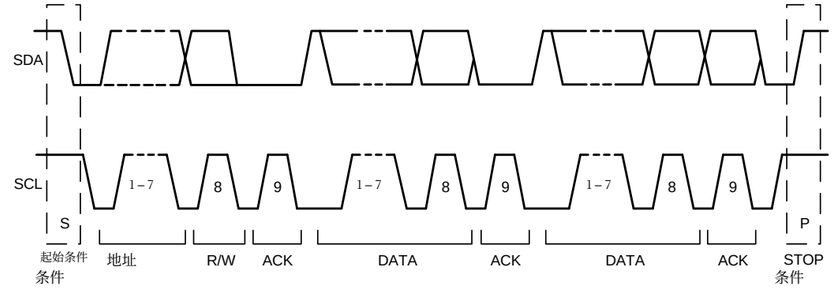


图14. 完整I²C数据传输

要写入ICM-42688-P内部寄存器，主设备需先传输起始条件(S)，接着发送I²C地址和写位(0)。在第9th 个时钟周期（时钟为高电平时），ICM-42688-P会确认传输。然后主设备将寄存器地址(RA)置于总线上。在ICM-42688-P确认收到寄存器地址后，主设备将寄存器数据送上总线。随后是ACK信号，数据传输可通过停止条件(P)结束。若要在最后ACK信号后写入多字节，主设备可继续输出数据而非发送停止信号。此时ICM-42688-P会自动递增寄存器地址并将数据载入相应寄存器。下图展示了单字节和双字节写入序列。

单字节写入序列

主设备	S	AD+W		RA		DATA		P
从设备			ACK		ACK		ACK	

突发写入序列

主设备	S	AD+W		RA		DATA		DATA		P
从设备			ACK		ACK		ACK		ACK	

要读取ICM-42688-P内部寄存器，主设备首先发送起始条件，接着发送I²C地址和写位，然后是待读取的寄存器地址。接收到来自ICM-42688-P的ACK信号后，主设备发送起始信号、从设备地址及读位。随后ICM-42688-P返回ACK信号和数据。通信以非确认(NACK)信号和主设备的停止位结束。NACK条件定义为SDA线在第9th 个时钟周期保持高电平。下图展示了单字节和双字节读取序列。

单字节读取序列

主设备	S	AD+W		RA		S	AD+R			NACK	P
从设备			ACK		ACK			ACK	DATA		

突发读取序列

主设备	S	AD+W		RA		S	AD+R			ACK		NACK	P
从设备			ACK		ACK			ACK	DATA		DATA		

9.5 I²C条款

信号	描述
S	起始条件：当SCL为高电平时，SDA从高电平变为低电平
AD	从设备I²C地址

W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-42688-P internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 13. I²C Terms

W	写位 (0)
R	读位 (1)
ACK	确认: 在9th 时钟周期内，当SCL线为高电平时，SDA线保持低电平
NACK	非确认：SDA 线在9th 时钟周期保持高电平
RA	ICM-42688-P 内部寄存器地址
DATA	发送或接收数据
P	停止条件：当SCL为高电平时，SDA从低电平变为高电平

表13. I²C条款

9.6 SPI INTERFACE

The ICM-42688-P supports 3-wire or 4-wire SPI for the host interface. The ICM-42688-P always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 24 MHz
5. SPI read operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. SPI write operations are completed in 16 clock cycles (two bytes). The first byte contains the SPI Address, and the second byte contains the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Write (0) operation. The following 7 bits contain the Register Address.
7. Supports Single or Burst Reads and Single Writes.

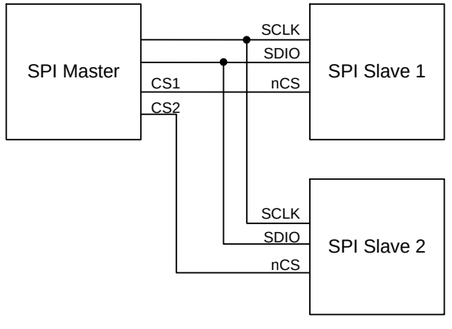


Figure 15. Typical SPI Master/Slave Configuration

9.6 SPI接口

ICM-42688-P支持三线制或四线制SPI作为主机接口。在标准主从SPI操作中，ICM-42688-P始终作为从设备运行。

对于主设备而言，串行时钟输出(SCLK)、串行数据输出(SDO)、串行数据输入(SDI)和串行数据输入输出(SDIO)由所有从设备共享。每个SPI从模式设备需要主设备提供独立的片选(CS)信号线。

CS信号在传输开始时拉低(有效)，在传输结束时恢复高电平(无效)。同一时间只有一条CS信号线处于有效状态，确保任一时刻仅选择一个从设备。未被选中的从设备其CS信号线保持高电平，使得它们的SDO线路维持高阻抗状态，从而不会干扰任何处于活动状态的设备。

SPI操作特性

1. 数据以最高有效位（MSB）优先、最低有效位（LSB）最后的方式传输
2. 数据在SCLK的上升沿被锁存
3. 数据应在SCLK的下降沿进行转换
4. SCLK的最高频率为24兆赫
5. SPI读取操作需16个或更多时钟周期（两个或更多字节）完成。首字节包含SPI地址，后续字节包含SPI数据。首字节的第一位为读/写位，表示读取（1）操作。随后的7位为寄存器地址。在多字节读取情况下，数据为两个或更多字节：

SPI地址格式

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI数据格式

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. SPI写入操作在16个时钟周期（两个字节）内完成。第一个字节包含SPI地址，第二个字节包含SPI数据。第一个字节的第一位包含读/写位，表示写入(0)操作。随后的7位包含寄存器地址。
7. 支持单次或突发读取和单次写入。

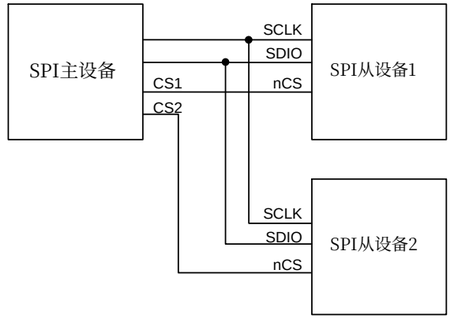


图15. 典型的SPI主从配置

10 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

10.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

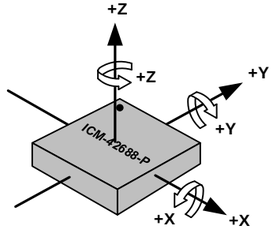


Figure 16. Orientation of Axes of Sensitivity and Polarity of Rotation

10 组装

本节提供应美盛微机电系统（MEMS）设备采用LGA封装组装的一般准则。

10.1 轴方向

下图展示了敏感轴方向及旋转极性的示意图。请注意图中的引脚1标识(•)。

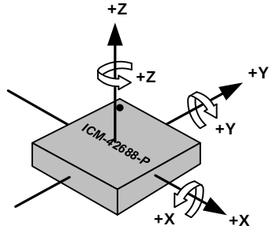
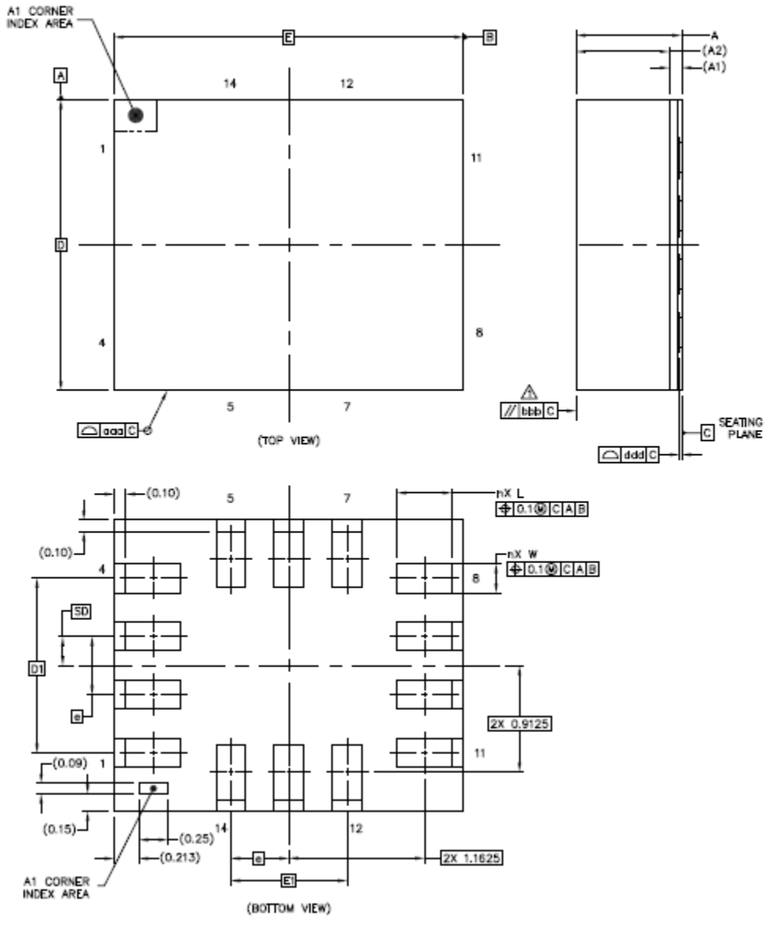


图16. 敏感轴方向和旋转极性

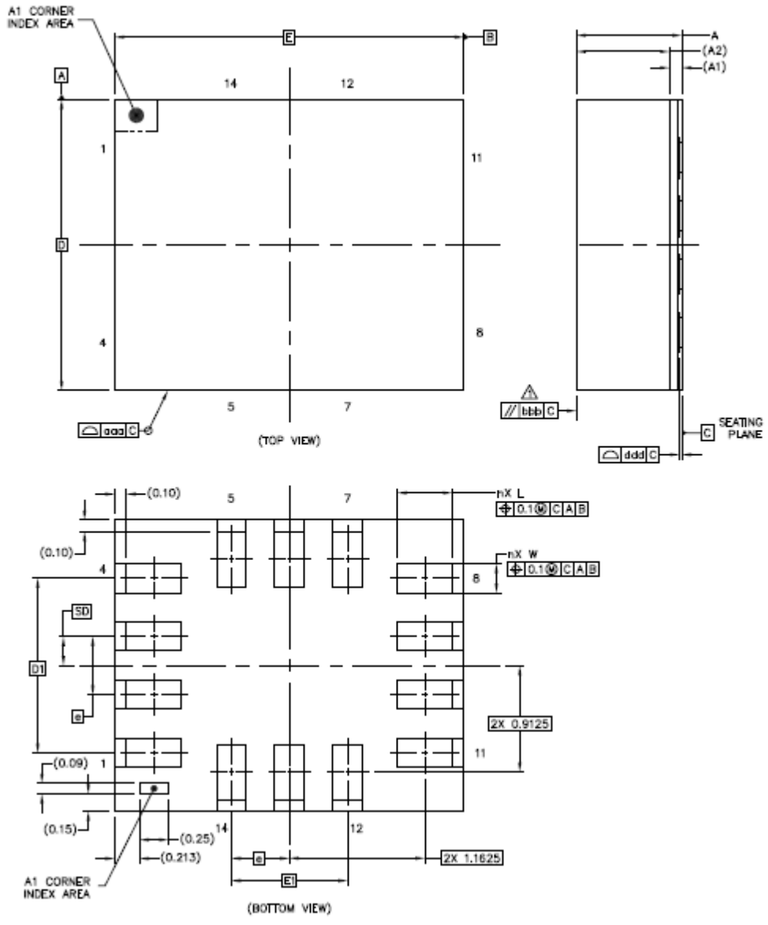
10.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.91) mm NiAu pad finish



10.2 封装尺寸

14引脚LGA (2.5x3x0.91) 毫米 镍金焊盘处理



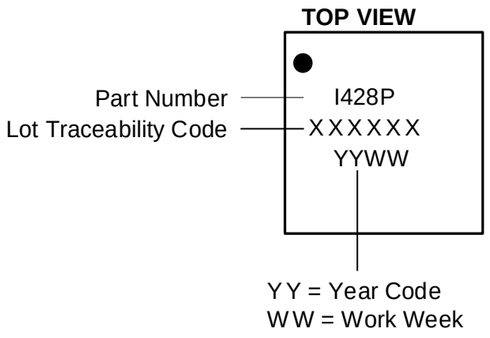
	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.85	0.91	0.97
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.8	REF
Body Size	D		2.5	BSC
	E		3	BSC
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.425	0.475	0.525
Lead Pitch	e		0.5	BSC
Lead Count	n		14	
Edge Pin Center to Center	D1		1.5	BSC
	E1		1	BSC
Body Center to Contact Pin	SD		0.25	BSC
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	

	符号	尺寸（毫米）		
		MIN	NOM	MAX
总厚度	A	0.85	0.91	0.97
基板厚度	A1		0.105 参考	
模具厚度	A2		0.8 参考	
主体尺寸	D		2.5	BSC
	E		3	BSC
引脚宽度	W	0.2	0.25	0.3
引脚长度	L	0.425	0.475	0.525
引脚间距	e		0.5 基本尺寸	
引脚数	n		14	
边缘引脚中心距	D1		1.5 基本尺寸	
	E1		1 基本尺寸	
本体中心至接触引脚	SD		0.25 基本尺寸	
封装边缘公差	aaa		0.1	
模具平整度	bbb		0.2	
共面性	ddd		0.08	

11 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-42688-P devices is summarized below:

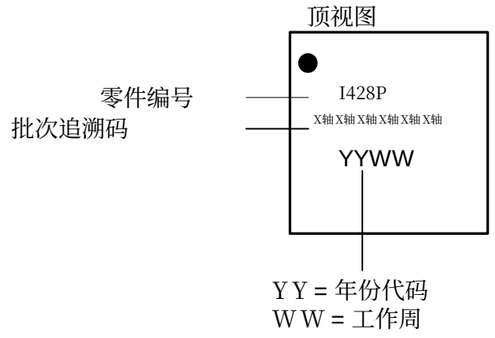
Part Number	Part Number Package Marking
ICM-42688-P	I428P



11 零件编号包装标记

ICM-42688-P 设备的零件编号包装标记总结如下：

零件编号	零件编号包装标记
ICM-42688-P	I428P



12 USE NOTES

12.1 ACCELEROMETER MODE TRANSITIONS

When transitioning from accelerometer Low Power (LP) mode to accelerometer Low Noise (LN) mode, if ODR is 6.25Hz or lower, software should change ODR to a value of 12.5Hz or higher, because accelerometer LN mode does not support ODR values below 12.5Hz.

When transitioning from accelerometer LN mode to accelerometer LP mode, if ODR is greater than 500Hz, software should change ODR to a value of 500Hz or lower, because accelerometer LP mode does not support ODR values above 500Hz.

12.2 ACCELEROMETER LOW POWER (LP) MODE AVERAGING FILTER SETTING

Software drivers provided with the device use Averaging Filter setting of 16x. This setting is recommended for meeting Android noise requirements in LP mode, and to minimize accelerometer offset variation when transitioning from LP to Low Noise (LN) mode. 1x averaging filter can be used by following the setting configuration shown in section 14.38.

12.3 SETTINGS FOR I²C, I3C^{SM}, AND SPI OPERATION

Upon bootup the device comes up in SPI mode. The following settings should be used for I²C, I3C^{SM}, and SPI operation.

Scenario 1: INT1/INT2 pins are used for interrupt assertion in I3C^{SM} mode.

Register Field	I²C Driver Setting	I3C^{SM} Driver Setting	SPI Driver Setting
I3C_EN (bit 4, register INTF_CONFIG6, address 0x7C, bank 1)	1	1	1
I3C_SDR_EN (bit 0, register INTF_CONFIG6, address 0x7C, bank 1)	0	1	1
I3C_DDR_EN (bit 1, register INTF_CONFIG6, address 0x7C, bank 1)	0	0	1
I3C_BUS_MODE (bit 6, register INTF_CONFIG4, address 0x7A, bank 1)	0	0	0
I2C_SLEW_RATE (bits 5:3, register DRIVE_CONFIG, address 0x13, bank 0)	1	0	0
SPI_SLEW_RATE (bits 2:0, register DRIVE_CONFIG, address 0x13, bank 0)	1	5	5

Scenario 2: IBI is used for interrupt assertion in I3C^{SM} mode.

Register Field	I²C Driver Setting	I3C^{SM} Driver Setting	SPI Driver Setting
I3C_EN (bit 4, register INTF_CONFIG6, address 0x7C, bank 1)	1	1	1
I3C_SDR_EN (bit 0, register INTF_CONFIG6, address 0x7C, bank 1)	0	1	1
I3C_DDR_EN (bit 1, register INTF_CONFIG6, address 0x7C, bank 1)	0	1	1
I3C_BUS_MODE (bit 6, register INTF_CONFIG4, address 0x7A, bank 1)	0	0	0
I2C_SLEW_RATE (bits 5:3, register DRIVE_CONFIG, address 0x13, bank 0)	1	0	0
SPI_SLEW_RATE (bits 2:0, register DRIVE_CONFIG, address 0x13, bank 0)	1	5	5

12.4 NOTCH FILTER AND ANTI-ALIAS FILTER OPERATION

Use of Notch Filter and Anti-Alias Filter is supported only for Low Noise (LN) mode operation. The host is responsible for keeping the UI path in LN mode while Notch Filter and Anti-Alias Filter are turned on.

12.5 EXTERNAL CLOCK INPUT EFFECT ON ODR

ODR values supported by the device scale with external clock frequency, if external clock input is used. The ODR values shown in the datasheet are supported with external clock input frequency of 32kHz. For any other external clock input frequency, these ODR values will scale by a factor of (External clock value in kHz / 32). For example, if an external clock frequency of 32.768kHz is used, instead of ODR value of 500Hz, it will be 500 * (32.768 / 32) = 512Hz.

12 使用说明

12.1 加速度计模式切换

当加速度计从低功耗（LP）模式切换至低噪声（LN）模式时，若输出数据速率为6.25赫兹或更低，软件应将输出数据速率调整为12.5赫兹或更高值，因为加速度计低噪声(LN)模式不支持低于12.5赫兹的输出数据速率。

当从加速度计低噪声(LN)模式切换到加速度计低功耗(LP)模式时，若输出数据速率(ODR)超过500赫兹，软件应将ODR调整为500赫兹或更低值，因为加速度计低功耗(LP)模式不支持高于500赫兹的ODR值。

12.2 加速度计低功耗 (LP) 模式平均滤波器设置

设备随附的软件驱动程序采用16倍平均滤波器设置。该设置推荐用于满足低功耗(LP)模式下的Android噪声要求，并最小化从低功耗(LP)模式切换到低噪声(LN)模式时的加速度计偏移变化。1倍平均滤波器可通过遵循14.38节所示的配置设置来使用。

12.3 I²C、I3C^{SM}及SPI操作设置

设备启动时默认进入SPI模式。以下设置适用于I²C、I3C^{SM}和SPI操作。

场景1: INT1/INT2引脚用于I3C^{SM} 模式下的中断断言。

寄存器字段	I²C驱动设置	I3C^{SM} 驱动设置	SPI驱动设置
I3C_使能 (位4, 寄存器INTF_CONFIG6, 地址0x7C, 存储区1)	1	1	1
I3C_单倍数据速率_使能 (位0, 寄存器INTF_CONFIG6, 地址0x7C, 存储区1)	0	1	1
I3C_DDR_EN (位1, 寄存器 INTF_CONFIG6, 地址0x7C, 存储区1)	0	0	1
I3C_BUS_MODE (位6, 寄存器 INTF_CONFIG4, 地址0x7A, 存储区1) I2C_	0	0	0
SLEW_RATE (位5:3, 寄存器 DRIVE_CONFIG, 地址0x13, 存储区0) SPI_	1	0	0
SLEW_RATE (位2:0, 寄存器 DRIVE_CONFIG, 地址0x13, 存储区0)	1	5	5

场景2: IBI用于I3C^{SM} 模式下的中断断言。

寄存器字段	I²C驱动设置	I3C^{SM} 驱动设置	SPI驱动设置
I3C_使能 (位4, 寄存器 INTF_CONFIG6, 地址0x7C, 存储区1)	1	1	1
I3C_单倍数据速率_使能 (位0, 寄存器 INTF_CONFIG6, 地址0x7C, 存储区1)	0	1	1
I3C_双倍数据速率_使能 (位1, 寄存器 INTF_CONFIG6, 地址0x7C, 存储区1)	0	1	1
I3C_BUS_模式 (位6, 寄存器 INTF_CONFIG4, 地址0x7A, 存储区1)	0	0	0
I2C_斜率_速率 (位5:3, 寄存器 DRIVE_配置, 地址0x13, 存储区0)	1	0	0
SPI_SLEW_速率 (位2:0, 寄存器 DRIVE_配置, 地址0x13, 存储区0)	1	5	5

12.4 陷波滤波器与抗锯齿滤波器操作

陷波滤波器和抗锯齿滤波器的使用仅支持在低噪声(LN)模式下运行。主机需确保在开启陷波滤波器和抗锯齿滤波器时，用户界面路径保持低噪声(LN)模式。

12.5 外部时钟输入对输出数据速率的影响

设备支持的输出数据速率值会随外部时钟频率变化（若使用外部时钟输入）。数据手册中标明的输出数据速率值基于32千赫的外部时钟输入频率。对于其他外部时钟输入频率，这些输出数据速率值将按比例缩放，缩放系数为（外部时钟频率值（千赫）/32）。例如，若使用32.768千赫的外部时钟频率，原本500赫兹的输出数据速率值将变为500*(32.768/32)= 512赫兹。

12.6 INT_ASYNC_RESET CONFIGURATION

For register INT_CONFIG1 (bank 0 register 0x64) bit 4 INT_ASYNC_RESET, user should change setting to 0 from default setting of 1, for proper INT1 and INT2 pin operation.

12.7 FIFO TIMESTAMP INTERVAL SCALING

When RTC_MODE =1 (bank 0 register 0x4D bit2) and register INTF_CONFIG5 (bank 1 register 0x7B) bit 2:1 (PIN9_FUNCTION) is set to 10 for CLKIN input;

THEN

If TMST_RES = 0 (corresponding to timestamp resolution of 1µs), timestamp interval reported in FIFO requires scaling by a factor of 32.768/RTC Frequency.
For example when ODR = 1kHz, RTC Frequency 32kHz, the true timestamp interval should be 1000µs. But the value in FIFO toggles between 976 and 977. After scaling 976.5 * 32.768/32 = 1000µs.

If TMST_RES = 1 (corresponding to timestamp resolution of 1 RTC clock period), timestamp interval reported in FIFO requires scaling by a factor of RTC clock period.
For example when ODR = 1kHz, RTC Frequency 32kHz, the true timestamp interval should be 1000µs. But the value in FIFO is 32. After scaling 1/32kHz*32 = 1000µs.

ELSE

If TMST_RES = 0 (corresponding to timestamp resolution of 1µs), timestamp interval reported in FIFO requires scaling by a factor of 32/30.
For example when ODR = 1kHz, the true timestamp interval should be 1000µs. But the value in FIFO toggles between 937 and 938. After scaling 937.5 * 32/30 = 1000µs.

If TMST_RES = 1 (corresponding to timestamp resolution of 16µs), timestamp interval reported in FIFO requires scaling by a factor of 16*32/30.
For example when ODR = 1kHz, the true timestamp interval should be 1000µs. But the value in FIFO toggles between 58 and 59. After scaling 58.5 * 16* 32/30 = 1000µs.

12.8 SUPPLEMENTARY INFORMATION FOR FIFO_HOLD_LAST_DATA_EN

This section contains supplementary information for using register field FIFO_HOLD_LAST_DATA_EN (bit 7) of register INTF_CONFIG0 (address 0x4C, bank 0) .

The following table shows the values in FIFO:

FIFO_HOLD_LAST_DATA_EN		16-bit FIFO Packet	20-bit FIFO Packet
0 (Insert Invalid code)	Valid sample	All values in: {-32766 to +32767}	Gyro: All Even numbers in {-524256 to +524286} Example: {-524256, -524254, -524252, -524250 .....+524284, +524286}
			Accel: Every Other Even number in {-524256 to +524284} Example: {-524256, -524252, -524248, -524244 .....+524280, +524284}
	Invalid sample	-32768	-524288
1 ("copy last valid" mode: No invalid code insertion)	Valid sample	All values in: {-32768 to +32767}	Gyro: All Even numbers in {-524288 to +524286} Example: {-524288, -524286, -524284, -524282 .....+524284, +524286 }
			Accel: Every Other Even number in {-524288 to +524284 } Example: {-524288, -524284, -524280 .....+524280, +524284}
	Invalid sample	Copy last valid sample	

12.6 INT异步复位配置_ _

对于寄存器INT_配置1（存储区0寄存器0x64）的位4 INT_异步_重置，用户应将默认设置从1改为0，以确保INT1和INT2引脚正常工作。

12.7 FIFO时间戳间隔缩放

当RTC_模式=1 (bank 0寄存器0x4D bit2)和寄存器INTF_配置5(bank 1寄存器0x7B)位2:1(PIN9_功能)设置为10用于CLKIN输入时；

THEN

若TMST_分辨率= 0 (对应时间戳分辨率为1微秒)，FIFO中报告的时间戳间隔需按32.768/RTC频率的比例因子进行缩放。

例如当输出数据速率= 1千赫、RTC频率32千赫时，真实时间戳间隔应为1000µ秒。但FIFO中的值会在976和977之间切换。缩放后为976.5 * 32.768/32 = 1000µ秒。

若TMST_分辨率= 1 (对应时间戳分辨率为1个RTC时钟周期)，FIFO中报告的时间戳间隔需按RTC时钟周期的比例因子进行缩放。
例如当输出数据速率= 1千赫、RTC频率32千赫时，真实时间戳间隔应为1000µ秒。但FIFO中的值为32。缩放后为1/32千赫*32 = 1000µ秒。

ELSE

如果时间戳 分辨率 = 0 (对应于时间戳分辨率为1微秒），先进先出队列中报告的时间戳间隔需要按32/30的比例进行缩放。例如当输出数据速率 = 1千赫时，真实时间戳间隔应为1000µ秒。但先进先出队列中的数值在937与938之间切换。经缩放后为937.5 * 32/30 = 1000µ秒。

如果时间戳 分辨率= 1 (对应时间戳分辨率为16微秒），FIFO中报告的时间戳间隔需要按16*32/30的比例进行缩放。例如当开漏读= 1千赫时，真实时间戳间隔应为1000µ秒。但FIFO中的值在58和59之间切换。缩放后为58.5 * 16 * 32/30 = 1000µ秒。

12.8 FIFO保持最后数据输入的补充信息_ _ _ _

本节包含关于使用寄存器INTF_CONFIG0（地址0x4C，存储区0）中寄存器字段先进先出_保持_最后_数据_使能（位7）的补充信息。

下表显示FIFO中的值：

FIFO保持最后数据输入 _ _ _ _		16位FIFO数据包	20位FIFO数据包
0（插入无效代码）	有效样本	所有值在：{-32766 至+32767}	陀螺仪：{-524256 至+524286}范围内的所有偶数 示例：{-524256, -524254, -524252, -524250 ..... +524284, +524286}
			加速度计：{-524256 至+524284}范围内每隔一个偶数 示例：{-524256, -524252, -524248, -524244 .....+524280, +524284}
	无效样本	-32768	-524288
1（"复制最后有效值"模式：否无效代码插入)	有效样本	所有值在：{-32768 至+32767}	陀螺仪：{-524288 至+524286}范围内的所有偶数 示例：{-524288, -524286, -524284, -524282 ..... +524284, +524286 }
			加速度计：{-524288 至+524284 }范围内每隔一个偶数 示例：{-524288, -524284, -524280 .....+524280, +524284}
	无效样本	复制最后一个有效样本	

The following table shows the values in sense registers on reset:

	FIFO_HOLD_LAST_DATA_EN = 0	FIFO_HOLD_LAST_DATA_EN = 1
Power On Reset till First Sample	Accel/Gyro/Temperature Sensor = -32768	Accel/Gyro/Temperature Sensor = 0

The following table shows the values in sense registers after first sample is received. As shown in table, the combination of FIFO_HOLD_LAST_DATA_EN and FSYNC Tag determine the range of values read for valid samples and invalid samples.

FIFO_HOLD_LAST_DATA_EN		**FSYNC tag disabled**	**FSYNC Enabled on one Sensor**		
			Sensor selected for FSYNC Tag		Other Sensor Not selected for FSYNC tagging
			FSYNC tagged	FSYNC not tagged	
0 (Insert Invalid code)	Valid sample	All values in: {-32766 to +32767}	All ODD values in: {-32765 to +32767}	All EVEN values in: {-32766 to +32766}	All values in: {-32766 to +32767}
	Invalid sample	Registers do not receive invalid samples. Registers hold last valid sample until new one arrives			
1 ("copy last valid" mode: No invalid code insertion)	Valid sample	All values in: {-32768 to +32767}	All ODD values in: {-32767 to +32767}	All EVEN values in: {-32768 to +32766}	All values in: {-32768 to +32767}
	Invalid sample	Registers do not receive invalid samples. Registers hold last valid sample until new one arrives			

12.9 REGISTER VALUES MODIFICATION

The only register settings that user can modify during sensor operation are for ODR selection, FSR selection, and sensor mode changes (register parameters GYRO_ODR, ACCEL_ODR, GYRO_FS_SEL, ACCEL_FS_SEL, GYRO_MODE, ACCEL_MODE). User must not modify any other register values during sensor operation. The following procedure must be used for other register values modification.

- Turn Accel and Gyro Off
- Modify register values
- Turn Accel and/or Gyro On

以下表格显示重置时感应寄存器中的值：

	FIFO保持最后数据输入 = 0	FIFO保持最后数据输入 = 1
上电复位至首次采样	加速度计/陀螺仪/温度传感器 = -32768	加速度计/陀螺仪/温度传感器 = 0

下表显示首次采样后感应寄存器中的值。如表所示，先进先出_保持_最后_数据_使能与FSYNC标签的组合决定了读取有效样本和无效样本时的数值范围。

FIFO保持最后数据输入		**帧同步标记禁用**	**在一个传感器上启用FSYNC**		
			选择用于FSYNC标签的传感器		其他传感器未被选择用于FSYNC标记
			已标记FSYNC	未标记FSYNC	
0 (插入无效代码)	有效样本	所有值在: {-32766 to +32767}	所有奇数数值范围: {-32765 to +32767}	所有偶数数值范围: {-32766 to +32766}	所有值在: {-32766 to +32767}
	无效样本	寄存器不接收无效样本。寄存器会保持最后有效样本直至新样本到达			
1 ("复制最后有效"模式: 无无效code插入)	有效样本	所有值在: {-32768 至 +32767}	所有奇数数值范围: {-32767 至 +32767}	所有偶数数值范围: {-32768 至 +32766}	所有值在: {-32768 至 +32767}
	无效样本	寄存器不会接收无效样本。寄存器将保留最后有效样本直至新样本到达			

12.9 寄存器值修改

用户在传感器运行期间可修改的寄存器设置仅限于输出数据速率选择、满量程选择及传感器模式变更（寄存器参数GYRO_ODR、ACCEL_ODR、GYRO_FS_SEL、ACCEL_FS_SEL、GYRO_MODE、ACCEL_MODE）。传感器运行期间严禁修改其他寄存器值。其他寄存器值修改必须遵循以下流程。

- 关闭加速度计和陀螺仪
- 修改寄存器值
- 开启加速度计和/或陀螺仪

13 REGISTER MAP

This section lists the register map for the ICM-42688-P, for user banks 0, 1, 2, 3, 4.

13.1 USER BANK 0 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11	17	DEVICE_CONFIG	R/W	-			SPI_MODE	-			SOFT_RESET_CONFIG
13	19	DRIVE_CONFIG	R/W	-		I2C_SLEW_RATE			SPI_SLEW_RATE		
14	20	INT_CONFIG		-		INT2_MODE	INT2_DRIVE_CIRCUIT	INT2_POLARITY	INT1_MODE	INT1_DRIVE_CIRCUIT	INT1_POLARITY
16	22	FIFO_CONFIG	R/W	FIFO_MODE		-					
1D	29	TEMP_DATA1	SYNCR	TEMP_DATA[15:8]							
1E	30	TEMP_DATA0	SYNCR	TEMP_DATA[7:0]							
1F	31	ACCEL_DATA_X1	SYNCR	ACCEL_DATA_X[15:8]							
20	32	ACCEL_DATA_X0	SYNCR	ACCEL_DATA_X[7:0]							
21	33	ACCEL_DATA_Y1	SYNCR	ACCEL_DATA_Y[15:8]							
22	34	ACCEL_DATA_Y0	SYNCR	ACCEL_DATA_Y[7:0]							
23	35	ACCEL_DATA_Z1	SYNCR	ACCEL_DATA_Z[15:8]							
24	36	ACCEL_DATA_Z0	SYNCR	ACCEL_DATA_Z[7:0]							
25	37	GYRO_DATA_X1	SYNCR	GYRO _DATA_X[15:8]							
26	38	GYRO _DATA_X0	SYNCR	GYRO _DATA_X[7:0]							
27	39	GYRO _DATA_Y1	SYNCR	GYRO _DATA_Y[15:8]							
28	40	GYRO _DATA_Y0	SYNCR	GYRO _DATA_Y[7:0]							
29	41	GYRO _DATA_Z1	SYNCR	GYRO_DATA_Z[15:8]							
2A	42	GYRO _DATA_Z0	SYNCR	GYRO_DATA_Z[7:0]							
2B	43	TMST_FSYNCH	SYNCR	TMST_FSYNC_DATA[15:8]							
2C	44	TMST_FSYNCL	SYNCR	TMST_FSYNC_DATA[7:0]							
2D	45	INT_STATUS	R/C	-	UI_FSYNC_INT	PLL_RDY_INT	RESET_DONE_INT	DATA_RDY_INT	FIFO_THS_INT	FIFO_FULL_INT	AGC_RDY_INT
2E	46	FIFO_COUNTH	R	FIFO_COUNT[15:8]							
2F	47	FIFO_COUNTL	R	FIFO_COUNT[7:0]							
30	48	FIFO_DATA	R	FIFO_DATA							
31	49	APEX_DATA0	SYNCR	STEP_CNT[7:0]							
32	50	APEX_DATA1	SYNCR	STEP_CNT[15:8]							
33	51	APEX_DATA2	R	STEP_CADENCE							
34	52	APEX_DATA3	R	-					DMP_IDLE	ACTIVITY_CLASS	
35	53	APEX_DATA4	R	-			TAP_NUM		TAP_AXIS		TAP_DIR
36	54	APEX_DATA5	R	-		DOUBLE_TAP_TIMING					
37	55	INT_STATUS2	R/C	-				SMD_INT	WOM_Z_INT	WOM_Y_INT	WOM_X_INT
38	56	INT_STATUS3	R/C	-		STEP_DET_INT	STEP_CNT_OVF_INT	TILT_DET_INT	WAKE_INT	SLEEP_INT	TAP_DET_INT
4B	75	SIGNAL_PATH_RESET	W/C	-	DMP_INIT_EN	DMP_MEM_RESET_EN	-	ABORT_AND_RESET	TMST_STROBE	FIFO_FLUSH	-
4C	76	INTF_CONFIG0	R/W	FIFO_HOLD_LAST_DATA_EN	FIFO_COUNT_REC	FIFO_COUNT_ENDIAN	SENSOR_DATA_ENDIAN	-		UI_SIFS_CFG	
4D	77	INTF_CONFIG1	R/W	-				ACCEL_LP_CLK_SEL	RTC_MODE	CLKSEL	
4E	78	PWR_MGMT0	R/W	-		TEMP_DIS	IDLE	GYRO_MODE		ACCEL_MODE	
4F	79	GYRO_CONFIG0	R/W	GYRO_FS_SEL			-	GYRO_ODR			
50	80	ACCEL_CONFIG0	R/W	ACCEL_FS_SEL			-	ACCEL_ODR			
51	81	GYRO_CONFIG1	R/W	TEMP_FILT_BW			-	GYRO_UI_FILT_ORD		GYRO_DEC2_M2_ORD	
52	82	GYRO_ACCEL_CONFIG0	R/W	ACCEL_UI_FILT_BW				GYRO_UI_FILT_BW			
53	83	ACCEL_CONFIG1	R/W	-			ACCEL_UI_FILT_ORD		ACCEL_DEC2_M2_ORD		-

13 注册映射

本节列出了ICM-42688-P的寄存器映射，涵盖用户存储区0、1、2、3、4。

13.1 用户库0寄存器映射

Addr (十六	Addr (十进	寄存器名称	串行 I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11	17	设备配置_	R/W	-			SPI 模式_	-			软重置_ 配置
13	19	驱动器配置_	R/W	-		I2C_SLEW_RATE			SPI_SLEW_RATE		
14	20	中断配置_		-		INT2模式_	中断2_驱动器_电路	INT2极性_	INT1 模式_	INT1 驱动	INT1 极性_
16	22	先进先出 配置_	R/W	先进先出 模式_		-					
1D	29	温度 数据1_	SYNCR	温度_数据[15:8]							
1E	30	温度 数据0_	SYNCR	温度_数据[7:0]							
1F	31	加速度数据 X1_	SYNCR	加速度计_数据_X轴[15:8]							
20	32	加速度数据 X0_	SYNCR	加速度计_数据_X轴[7:0]							
21	33	加速度数据 Y1_	SYNCR	加速度计_数据_Y轴[15:8]							
22	34	加速度数据 Y0_	SYNCR	加速度计_数据_Y轴[7:0]							
23	35	加速度数据 Z1轴1_	SYNCR	加速度计_数据_Z轴[15:8]							
24	36	加速度数据 Z0_	SYNCR	加速度计_数据_Z轴[7:0]							
25	37	陀螺仪数据 X1_	SYNCR	陀螺仪 _数据_X轴[15:8]							
26	38	陀螺仪数据 X0_	SYNCR	陀螺仪 _数据_X轴[7:0]							
27	39	陀螺仪数据 Y1_	SYNCR	陀螺仪 _数据_Y轴[15:8]							
28	40	陀螺仪数据 Y0_	SYNCR	陀螺仪 _数据_Y轴[7:0]							
29	41	陀螺仪数据 Z1_	SYNCR	陀螺仪_数据_Z[15:8]							
2A	42	陀螺数据Z0_	SYNCR	陀螺仪_数据_Z[7:0]							
2B	43	时间戳帧同步高_	SYNCR	时间戳_帧同步_数据[15:8]							
2C	44	时间戳帧同步低_	SYNCR	时间戳_帧同步_数据[7:0]							
2D	45	中断STATUS_	R/C	-	用户界面 帧同步 国际新闻_ 技术		锁相环就绪 中断	重置 完成_中断_	数据 就绪 输入 NT		先进先出 满 输入 NT	先进先出 阈值 国际新闻_ 技术	AGC RDY 国际新闻_ 技术
2E	46	FIFO COUNTH_	R	FIFO_计数[15:8]							
2F	47	FIFO计数低字节_	R	FIFO_计数[7:0]							
30	48	FIFO数据_	R	FIFO数据_							
31	49	APEX 数据0_	SYNCR	步进_CNT[7:0]							
32	50	APEX 数据1_	SYNCR	步进_CNT[15:8]							
33	51	APEX 数据2_	R	步频_							
34	52	顶点数据3_	R	-					DMP空闲_	活动类别_	
35	53	顶点数据4_	R	-			点击次数_		点击轴_		点击方向_
36	54	顶点数据5_	R	-		双击计时_					
37	55	中断状态2_	R/C	-				表面贴装器件中断_	陀螺仪Z轴中断_	陀螺仪Y轴中断_	陀螺仪X轴中断_
38	56	INT STATUS3_	R/C	-		步进检测输入 技术	步进计数输出_ _伏特女 _INT	倾斜检测输入 技术	唤醒中断_	睡眠中断_	点击检测中断
4B	75	信号路径重置_	W/C	-	DMP初始化EN	数字运动处理器_内存_重置 _EN	-	中止并_重置_	时间戳选通_E	FIFO刷新_	-
4C	76	接口配置0_	R/W	FIFO保持 L_ASTDATA E N	FIFO计数_记录_	FIFO计数 传感器数据_ 安培 字节序	字节序_	-		用户界面SIFS 配置_	
4D	77	接口配置1_	R/W	-				加速度低通滤波 选择器_	实时时钟模式_	时钟选择	
4E	78	电源管理0_	R/W	-		温度显示_	IDLE	陀螺仪模式_		加速度计模式_	
4F	79	陀螺仪配置0_	R/W	陀螺仪满量程选择			-	陀螺仪输出数据速率_			
50	80	加速度计配置0_	R/W	加速度计满量程选择			-	加速度计输出数据速率_			
51	81	陀螺仪配置1_	R/W	温度滤波器带宽_			-	GYRO_UI_FILT_ORD		陀螺仪 DEC2 M2 输出数据速率	
52	82	陀螺仪加速度计配置0_	R/W	加速度计用户界面滤波器带宽				GYRO_UI_FILT_BW			
53	83	加速度计配置1_	R/W	-			加速度计用户界面滤波器阶数_		加速度计DEC2 M2输出数据速率		-

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54	84	TMST_CONFIG	R/W	-			TMST_TO_REGS_EN	TMST_RES	TMST_DELTA_EN	TMST_FSYNC_EN	TMST_EN
56	86	APEX_CONFIG0	R/W	DMP_POWER_SAVE	TAP_ENABLE	PED_ENABLE	TILT_ENABLE	R2W_EN	-	DMP_ODR	
57	87	SMD_CONFIG	R/W	-				WOM_INT_MODE	WOM_MODE	SMD_MODE	
5F	95	FIFO_CONFIG1	R/W	-	FIFO_RESUME_PARTIAL_RD	FIFO_WM_GT_TH	FIFO_HIRES_EN	FIFO_TMST_FSYNC_EN	FIFO_TEMP_EN	FIFO_GYRO_EN	FIFO_ACCEL_EN
60	96	FIFO_CONFIG2	R/W	FIFO_WM[7:0]							
61	97	FIFO_CONFIG3	R/W	-				FIFO_WM[11:8]			
62	98	FSYNC_CONFIG	R/W	-	FSYNC_UI_SEL			-		FSYNC_UI_FLAG_CLEAR_SEL	FSYNC_POLARITY
63	99	INT_CONFIG0	R/W	-		UI_DRDY_INT_CLEAR		FIFO_THS_INT_CLEAR		FIFO_FULL_INT_CLEAR	
64	100	INT_CONFIG1	R/W	-	INT_TPULSE_DURATION	INT_TDEASSERT_DISABLE	INT_ASYNC_RESET	-			
65	101	INT_SOURCE0	R/W	-	UI_FSYNC_INT1_EN	PLL_RDY_INT1_EN	RESET_DONE_INT1_EN	UI_DRDY_INT1_EN	FIFO_THS_INT1_EN	FIFO_FULL_INT1_EN	UI_AGC_RDY_INT1_EN
66	102	INT_SOURCE1	R/W	-	I3C_PROTOCOL_ERROR_INT1_EN	-		SMD_INT1_EN	WOM_Z_INT1_EN	WOM_Y_INT1_EN	WOM_X_INT1_EN
68	104	INT_SOURCE3	R/W	-	UI_FSYNC_INT2_EN	PLL_RDY_INT2_EN	RESET_DONE_INT2_EN	UI_DRDY_INT2_EN	FIFO_THS_INT2_EN	FIFO_FULL_INT2_EN	UI_AGC_RDY_INT2_EN
69	105	INT_SOURCE4	R/W	-	I3C_PROTOCOL_ERROR_INT2_EN	-		SMD_INT2_EN	WOM_Z_INT2_EN	WOM_Y_INT2_EN	WOM_X_INT2_EN
6C	108	FIFO_LOST_PKT0	R	FIFO_LOST_PKT_CNT[15:8]							
6D	109	FIFO_LOST_PKT1	R	FIFO_LOST_PKT_CNT[7:0]							
70	112	SELF_TEST_CONFIG	R/W		ACCEL_ST_POWER	EN_AZ_ST	EN_AY_ST	EN_AX_ST	EN_GZ_ST	EN_GY_ST	EN_GX_ST
75	117	WHO_AM_I	R	WHOAMI							
76	118	REG_BANK_SEL	R/W	-					BANK_SEL		

13.2 USER BANK 1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03	03	SENSOR_CONFIG0	R/W	-		ZG_DISABLE	YG_DISABLE	XG_DISABLE	ZA_DISABLE	YA_DISABLE	XA_DISABLE
0B	11	GYRO_CONFIG_STATIC2	R/W	-						GYRO_AAF_DIS	GYRO_NF_DIS
0C	12	GYRO_CONFIG_STATIC3	R/W	-	GYRO_AAF_DELT						
0D	13	GYRO_CONFIG_STATIC4	R/W	GYRO_AAF_DELTSQR[7:0]							
0E	14	GYRO_CONFIG_STATIC5	R/W	GYRO_AAF_BITSHIFT				GYRO_AAF_DELTSQR[11:8]			
0F	15	GYRO_CONFIG_STATIC6	R/W	GYRO_X_NF_COSWZ[7:0]							
10	16	GYRO_CONFIG_STATIC7	R/W	GYRO_Y_NF_COSWZ[7:0]							
11	17	GYRO_CONFIG_STATIC8	R/W	GYRO_Z_NF_COSWZ[7:0]							
12	18	GYRO_CONFIG_STATIC9	R/W	-		GYRO_Z_NF_COSWZ_SEL[0]	GYRO_Y_NF_COSWZ_SEL[0]	GYRO_X_NF_COSWZ_SEL[0]	GYRO_Z_NF_COSWZ[8]	GYRO_Y_NF_COSWZ[8]	GYRO_X_NF_COSWZ[8]
13	19	GYRO_CONFIG_STATIC10	R/W	-	GYRO_NF_BW_SEL			-			
5F	95	XG_ST_DATA	R/W	XG_ST_DATA							
60	96	YG_ST_DATA	R/W	YG_ST_DATA							
61	97	ZG_ST_DATA	R/W	ZG_ST_DATA							
62	98	TMSTVAL0	R	TMST_VALUE[7:0]							
63	99	TMSTVAL1	R	TMST_VALUE[15:8]							
64	100	TMSTVAL2	R	-				TMST_VALUE[19:16]			
7A	122	INTF_CONFIG4	R/W	-	I3C_BUS_MODE	-				SPI_AP_4WIRE	-
7B	123	INTF_CONFIG5	R/W	-					PIN9_FUNCTION		-
7C	124	INTF_CONFIG6	R/W	ASYNCTIME0_DIS	-		I3C_EN	I3C_IBI_BYTE_EN	I3C_IBI_EN	I3C_DDR_EN	I3C_SDR_EN

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地址	地址	寄存器名称	串行 I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54	84	时间戳配置_	R/W	-			时间戳_至_读GS_EN	时间戳分辨率_	时间戳_增量_EN	时间戳帧同步_使能_	TMST启用_
56	86	APEX配置0_	R/W	DMP_POWER_SAVE	轻敲启用_	计步启用_	倾斜启用_	R2W启用_	-	数字运动处理器输出数据速率_	
57	87	显著运动检测配置_	R/W	-				WOM_中断_MODE	女性模式_	SMD模式_	
5F	95	先进先出配置1_	R/W	-	先进先出 RESUME 部件 读_	先进先出_水位标记_G技术阈值_	先进先出 高分辨率使能_	先进先出 时间戳故障同步 使能_	先进先出 温度使能_	FIFO 陀螺仪使能_	FIFO_加速度计_EN
60	96	FIFO 配置2_	R/W	FIFO_水位标记[7:0]							
61	97	FIFO 配置3_	R/W	-				FIFO_水位标记[11:8]			
62	98	帧同步 配置_	R/W	-	帧同步 用户界面 选择_			-		帧同步_UI_FLAG 清除 硫 E	帧同步 POLA_RITY
63	99	中断 配置0_	R/W	-		UI数据就绪 中断 清除_		FIFO_THS_INT_清除		FIFO满 中断 清除_	
64	100	中断 配置1_	R/W	-	INT_脉冲时间_持续时间	中断_TDE轴实时 禁用_	INT_异步_重置	-			
65	101	中断 来源0_	R/W	-	用户界面_帧同步_国际新闻T1_EN	锁相环_RDY_INT 1 使能	重置 _DONE_INT1 _EN	用户界面_数据就绪_中断 1 使能	FIFO_阈值_国际新闻T1_EN	FIFO_满_输入NT1 使能_	用户界面_AGC_RDY INT1 使能_
66	102	中断 来源1_	R/W	-	I3C_协议OL_ERROR_输入NT1_EN	-		加速度计低功耗_中断_EN	WOM_Z轴_中断 1 使能_	WOM_Y轴_中断 1 使能_	WOM_X_中断 1 使能_
68	104	INT SOURCE3_	R/W	-	用户界面_帧同步_国际新闻T2使能_	锁相环_RDY_中断 2使能	重置_完成 INT2使能_	用户界面_数据就绪_中断 2使能	先进先出_阈值_国际新闻T2使能_	先进先出_满_输入NT2使能_	用户界面_AGC_RDY INT2使能_
69	105	中断来源4_	R/W	-	I3C_协议OL_ERROR_输入NT2_EN	-		加速度计低功耗_中断_EN	WOM_Z轴_中断 2 使能_	WOM_Y轴_中断 2 使能_	WOM_X轴_中断 2 使能_
6C	108	FIFO丢失数据包0_	R	先进先出_丢失_数据包_计数[15:8]							
6D	109	FIFO丢失数据包1	R	先进先出_丢失_数据包_计数[7:0]							
70	112	自检配置_	R/W		加速度计_ST_POWER	使能 Z轴 自检_	使能 Y轴 自检_	使能 X轴 自检_	使能 GZ 自检_	使能 GY 自检_	使能 GX 自检_
75	117	我是谁_	R	我是谁							
76	118	寄存器组选择_	R/W	-					存储区选择_		

13.2 用户银行1寄存器映射

Addr (十六进制)	Addr (十进制)	寄存器名称	串行 I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03	03	传感器 配置0_	R/W	-		Z轴陀螺仪 禁用_	Y轴陀螺仪 禁用_	XG 禁用_	ZA 禁用_	YA 禁用_	XA禁用_
0B	11	陀螺配置静态2_	R/W	-						陀螺_抗混叠滤波器_数据IS	陀螺噪声滤波器DI_ 硫
0C	12	陀螺配置静态3_	R/W	-	陀螺抗混叠滤波器DELT_						
0D	13	陀螺配置静态4_	R/W	陀螺_抗混叠滤波器_增量平方[7:0]							
0E	14	陀螺仪配置静态5_	R/W	陀螺AAF位偏移_				陀螺_抗混叠滤波器_增量平方[11:8]			
0F	15	陀螺仪配置静态6_	R/W	陀螺仪_X轴_NF_COSWZ[7:0]							
10	16	陀螺仪配置静态7_	R/W	陀螺仪_Y轴_NF_COSWZ[7:0]							
11	17	陀螺仪配置静态8_	R/W	陀螺仪_Z轴_NF_COSWZ[7:0]							
12	18	陀螺配置静态9_	R/W	-		陀螺仪Z轴 NF_C OSWZ_[选择0]	陀螺仪Y轴 NF_C OSWZ_[选择0]	陀螺仪X轴 NF_C OSWZ_[选择0]	陀螺仪Z轴 NF COSWZ[8]	陀螺仪Y轴 NF COSWZ[8]	陀螺仪X轴 NF COSWZ[8]
13	19	陀螺仪配置 STATIC10_	R/W	-	陀螺仪 NF 带宽 选择			-			
5F	95	XG ST 数据_	R/W	XG ST 数据_							
60	96	YG ST 数据_	R/W	YG ST 数据_							
61	97	Z轴陀螺仪 自检 数据	R/W	Z轴陀螺仪 自检 数据							
62	98	时间戳值0	R	时间戳_值[7:0]							
63	99	时间戳值1	R	时间戳_值[15:8]							
64	100	时间戳值2	R	-				时间戳_值[19:16]			
7A	122	INTF 配置4_	R/W	-	I3C_总线_MODE	-				SPI_安培隔_4读输入E	-
7B	123	INTF CONFIG5_	R/W	-					引脚9功能_		-
7C	124	接口配置6_	R/W	异步时间0禁用_	-		I3C使能_	I3C_IBI_字节_EN	I3C IBI使能_	I3C 双倍数据速率使能_	I3C SDR 使能_

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13.3 USER BANK 2 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03	03	ACCEL_CONFIG_STATIC2	R/W	-	ACCEL_AAF_DELT						ACCEL_AAF_DIS
04	04	ACCEL_CONFIG_STATIC3	R/W	ACCEL_AAF_DELTSQR[7:0]							
05	05	ACCEL_CONFIG_STATIC4	R/W	ACCEL_AAF_BITSHIFT				ACCEL_AAF_DELTSQR[11:8]			
3B	59	XA_ST_DATA	R/W	XA_ST_DATA							
3C	60	YA_ST_DATA	R/W	YA_ST_DATA							
3D	61	ZA_ST_DATA	R/W	ZA_ST_DATA							

13.4 USER BANK 3 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2A	42	CLKDIV	R	-	CLKDIV						

13.5 USER BANK 4 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40	64	APEX_CONFIG1	R/W	LOW_ENERGY_AMP_TH_SEL				DMP_POWER_SAVE_TIME_SEL			
41	65	APEX_CONFIG2	R/W	PED_AMP_TH_SEL				PED_STEP_CNT_TH_SEL			
42	66	APEX_CONFIG3	R/W	PED_STEP_DET_TH_SEL			PED_SB_TIMER_TH_SEL			PED_HI_EN_TH_SEL	
43	67	APEX_CONFIG4	R/W	TILT_WAIT_TIME_SEL		SLEEP_TIME_OUT			-		
44	68	APEX_CONFIG5	R/W	-					MOUNTING_MATRIX		
45	69	APEX_CONFIG6	R/W	-					SLEEP_GESTURE_DELAY		
46	70	APEX_CONFIG7	R/W	TAP_MIN_JERK_THR						TAP_MAX_PEAK_TOL	
47	71	APEX_CONFIG8	R/W	-	TAP_TMAX		TAP_TAVG		TAP_TMIN		
48	72	APEX_CONFIG9	R/W	-							SENSITIVITY_MODE
4A	74	ACCEL_WOM_X_THR	R/W	WOM_X_TH							
4B	75	ACCEL_WOM_Y_THR	R/W	WOM_Y_TH							
4C	76	ACCEL_WOM_Z_THR	R/W	WOM_Z_TH							
4D	77	INT_SOURCE6	R/W	-		STEP_DET_INT1_EN	STEP_CNT_OFL_INT1_EN	TILT_DET_INT1_EN	WAKE_DET_INT1_EN	SLEEP_DET_INT1_EN	TAP_DET_INT1_EN
4E	78	INT_SOURCE7	R/W	-		STEP_DET_INT2_EN	STEP_CNT_OFL_INT2_EN	TILT_DET_INT2_EN	WAKE_DET_INT2_EN	SLEEP_DET_INT2_EN	TAP_DET_INT2_EN
4F	79	INT_SOURCE8	R/W	-		FSYNC_IBI_EN	PLL_RDY_IBI_EN	UI_DRDY_IBI_EN	FIFO_THS_IBI_EN	FIFO_FULL_IBI_EN	AGC_RDY_IBI_EN
50	80	INT_SOURCE9	R/W	I3C_PROTOCOL_ERROR_IBI_EN	-		SMD_IBI_EN	WOM_Z_IBI_EN	WOM_Y_IBI_EN	WOM_X_IBI_EN	-
51	81	INT_SOURCE10	R/W	-		STEP_DET_IBI_EN	STEP_CNT_OFL_IBI_EN	TILT_DET_IBI_EN	WAKE_DET_IBI_EN	SLEEP_DET_IBI_EN	TAP_DET_IBI_EN
77	119	OFFSET_USER0	R/W	GYRO_X_OFFUSER[7:0]							
78	120	OFFSET_USER1	R/W	GYRO_Y_OFFUSER[11:8]				GYRO_X_OFFUSER[11:8]			
79	121	OFFSET_USER2	R/W	GYRO_Y_OFFUSER[7:0]							
7A	122	OFFSET_USER3	R/W	GYRO_Z_OFFUSER[7:0]							
7B	123	OFFSET_USER4	R/W	ACCEL_X_OFFUSER[11:8]				GYRO_Z_OFFUSER[11:8]			
7C	124	OFFSET_USER5	R/W	ACCEL_X_OFFUSER[7:0]							
7D	125	OFFSET_USER6	R/W	ACCEL_Y_OFFUSER[7:0]							
7E	126	OFFSET_USER7	R/W	ACCEL_Z_OFFUSER[11:8]				ACCEL_Y_OFFUSER[11:8]			
7F	127	OFFSET_USER8	R/W	ACCEL_Z_OFFUSER[7:0]							

Detailed register descriptions are provided in the sections that follow. Please note the following regarding Clock Domain for each register:

13.3 用户库2寄存器映射

地址	地址	寄存器名称	串行 I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03	03	加速度配置静态2_ _	R/W	-	加速度AAF增量_ _						加速度抗混叠滤波器_ _ DIS
04	04	加速度配置静态3_ _	R/W	加速度计_抗混叠滤波器_增量平方[7:0]							
05	05	加速度计_配置 _静态4	R/W	加速度 _AAF_位移位				加速度计_抗混叠滤波器_增量平方[11:8]			
3B	59	X轴加速度自检数据 _ _	R/W	X轴加速度自检数据 _ _							
3C	60	Y轴加速度自检数据 _ _	R/W	Y轴加速度自检数据 _ _							
3D	61	Z轴加速度自检数据_ _	R/W	Z轴加速度自检数据_ _							

13.4 用户组3寄存器映射

地址	地址	寄存器名称	串行 I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2A	42	时钟分频器	R	-	时钟分频器						

13.5 用户库4寄存器映射

Addr (十六进制)	Addr (十进制)	寄存器名称	串行 I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40	64	APEX 配置1_	R/W	低能耗放大器阈值选择_ _ _ _				DMP省电模式时间选择_ _ _ _			
41	65	APEX 配置2_	R/W	PED_AMP_阈值选择_				计步器步数检测窗口_ _ _ _			
42	66	APEX配置3_	R/W	计步器步数检测阈值选择 _ _ _ _			PED_SB_定时器_TH_SEL			PED高使能阈值选择 _ _ _ _	
43	67	APEX配置4_	R/W	倾斜等待时间选择 _ _ _		睡眠超时_ _			-		
44	68	APEX配置5_	R/W	-					安装矩阵_		
45	69	顶点配置6_	R/W	-					睡眠手势延迟_ _		
46	70	顶点配置7_	R/W	轻敲最小抖动阈值 _ _ _ _						轻敲_最大值_峰值 _TOL	
47	71	顶点配置8_	R/W	-	轻敲技术最大值		轻敲技术平均值		轻敲技术最小值		
48	72	APEX配置9_	R/W	-							灵敏度_ 模式
4A	74	加速度计 _WOM_X_THR	R/W	WOM X轴 阈值_ _							
4B	75	加速度计 WOM Y轴 推力 _ _ _	R/W	WOM Y轴 阈值_ _							
4C	76	加速度计 WOM Z轴 推力	R/W	WOM Z轴 阈值_ _							
4D	77	中断 来源6_	R/W	-		步进 检测IN _ _ 定时器1 使能_	步进_计数_输出 FL INT1 使能	倾斜检测输入 唤醒 1 使能 _ _	检测输入_ _ NT1 使能_	定时器 _ _ _	睡眠 检测输入 _ _ NT1 使能_	点击检测中断 1 使能_
4E	78	中断源7_	R/W	-		步进 检测输入 _ _ T2 使能_	步骤计数器 _ _ 标志中断 2 使能_ _	倾斜检测输入 唤醒 能_ _ NT2使能	检测输入_ _ T2使能_		睡眠_检测_输入 NT2使能_	点击检测中断 2 使能_
4F	79	中断源8_	R/W	-		帧同步IBI使能 _ _ N	锁相环就绪 IBI _ _ _ 使能	用户首发_数据就绪_IBI _EN	先进先出_阈值_IBI _EN	先进先出_满_输入输入 使能_	AGC_读取Y_IBI _EN	
50	80	INT SOURCE9_	R/W	I3C 协议_开漏 ERROR_IBI 使能_ _	-		SMD IBI使能_ _	WOM_Z轴_IBI_ EN	WOM_Y轴_IBI_ EN	WOM_X轴_IBI_ EN	-	
51	81	中断 来源10_	R/W	-		步进 检测IB _ _ 输入 使能_	步进_计数_输出 FL IBI 使能	倾斜检测IBI 唤醒 _ _ BI 使能 _	检测输入_ _ 使能 _	睡眠 检测输入 _ _ BI 使能_	点击检测间隔 _ _ 使能_	
77	119	用户0偏移量_	R/W	陀螺仪_X轴_用户偏移[7:0]							
78	120	用户1偏移量_	R/W	陀螺仪_Y轴_用户偏移[11:8]				陀螺仪_X轴_用户偏移[11:8]			
79	121	用户2偏移量_	R/W	陀螺仪_Y轴_用户偏移[7:0]							
7A	122	用户3偏移量_	R/W	陀螺仪_Z轴_用户偏移[7:0]							
7B	123	用户4偏移量_	R/W	加速度计_X轴_用户偏移[11:8]				陀螺仪_Z轴_关闭用户[11:8]			
7C	124	偏移量 用户5_	R/W	加速度计_X轴_关闭用户[7:0]							
7D	125	偏移量 用户6_	R/W	加速度计_Y轴_关闭用户[7:0]							
7E	126	偏移量 用户7_	R/W	加速度计_Z轴_关闭用户[11:8]				加速度计_Y轴_关闭用户[11:8]			
7F	127	偏移 用户8_	R/W	加速度计_Z轴_关闭用户[7:0]							

详细寄存器描述将在后续章节中提供。请注意以下关于每个寄存器的时钟域说明：

- Clock Domain: SCLK_UI means that the register is controlled from the UI interface

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

- 时钟域：SCLK_用户界面表示该寄存器由用户界面接口控制

标记为保留的寄存器字段不得被用户修改。该寄存器的复位值可用于确定保留寄存器字段的默认值，除非另有说明，即使其他寄存器字段的值被用户修改，也必须保持此默认值。

14 USER BANK 0 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 0.

Note: The device powers up in sleep mode.

14.1 DEVICE_CONFIG

Name: DEVICE_CONFIG
Address: 17 (11h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	-	Reserved
4	SPI_MODE	SPI mode selection 0: Mode 0 and Mode 3 (default) 1: Mode 1 and Mode 2
3:1	-	Reserved
0	SOFT_RESET_CONFIG	Software reset configuration 0: Normal (default) 1: Enable reset After writing 1 to this bitfield, wait 1ms for soft reset to be effective, before attempting any other register access

14.2 DRIVE_CONFIG

Name: DRIVE_CONFIG
Address: 19 (13h)
Serial IF: R/W
Reset value: 0x05
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	I2C_SLEW_RATE	Controls slew rate for output pin 14 in I^2C mode only 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved
2:0	SPI_SLEW_RATE	Controls slew rate for output pin 14 in SPI or $I3C^{SM}$ mode, and for all other output pins 000: 20ns-60ns 001: 12ns-36ns 010: 6ns-18ns 011: 4ns-12ns 100: 2ns-6ns 101: < 2ns 110: Reserved 111: Reserved

14 用户库0寄存器映射 – 描述

本节描述USR存储区0中每个寄存器的功能和内容。**注意：**设备上电时处于睡眠模式。

14.1 设备配置_

名称: 设备配置_地址:
17 (11h)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:5	-	保留
4	SPI_MODE	SPI模式选择 0：模式0和模式3（默认） 1: 模式1和模式2
3:1	-	保留
0	软重置配置_ _	软件复位配置 0: 正常（默认） 1: 启用复位 向此位域写入1后，等待1毫秒使软重置生效，然后再尝试其他寄存器访问

14.2 驱动器配置_

Name: DRIVE_CONFIG
_地址：19 (13h)
串行接口：读/写
复位值：0x05
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5:3	I2C 转换速率_ _	仅控制I^2C模式下输出引脚14的转换速率 000: 20纳秒-60纳秒 001: 12纳秒-36纳秒 010: 6纳秒-18纳秒 011: 4纳秒-12纳秒 100: 2纳秒-6纳秒 101: < 2纳秒 110: 保留 111: 保留
2:0	SPI转换速率_ _	控制SPI或$I3C^{SM}$ 模式下引脚14及其他所有输出引脚的信号斜率 000: 20纳秒-60纳秒 001: 12纳秒-36纳秒 010: 6纳秒-18纳秒 011: 4纳秒-12纳秒 100: 2纳秒-6纳秒 101: < 2纳秒 110: 保留 111: 保留

14.3 INT_CONFIG

Name: INT_CONFIG
Address: 20 (14h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT2_MODE	INT2 interrupt mode 0: Pulsed mode 1: Latched mode
4	INT2_DRIVE_CIRCUIT	INT2 drive circuit 0: Open drain 1: Push pull
3	INT2_POLARITY	INT2 interrupt polarity 0: Active low (default) 1: Active high
2	INT1_MODE	INT1 interrupt mode 0: Pulsed mode 1: Latched mode
1	INT1_DRIVE_CIRCUIT	INT1 drive circuit 0: Open drain 1: Push pull
0	INT1_POLARITY	INT1 interrupt polarity 0: Active low (default) 1: Active high

14.4 FIFO_CONFIG

Name: FIFO_CONFIG
Address: 22 (16h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	FIFO_MODE	00: Bypass Mode (default) 01: Stream-to-FIFO Mode 10: STOP-on-FULL Mode 11: STOP-on-FULL Mode
5:0	-	Reserved

14.5 TEMP_DATA1

Name: TEMP_DATA1
Address: 29 (1Dh)
Serial IF: SYNCR
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	TEMP_DATA[15:8]	Upper byte of temperature data

14.3 中断配置_

名称: 中断配置_地址:
20 (14h) 串行接口:
读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	INT2_MODE	INT2中断模式 0: 脉冲模式 1: 锁存模式
4	INT2驱动电路_ _	INT2驱动电路 0: 开漏 1: 推挽
3	INT2中断极性_	INT2中断极性 0: 低电平有效（默认） 1: 高电平有效
2	INT1_MODE	INT1中断模式 0: 脉冲模式 1: 锁存模式
1	INT1驱动电路_ _	INT1驱动电路 0: 开漏 1: 推挽
0	INT1极性_	INT1中断极性 0: 低电平有效（默认） 1: 高电平有效

14.4 先进先出 配置_

名称：先进先出 配置_
地址：22 (16h) 串行接
口：读/写 复位值：
0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	先进先 MODE 出_	00: 旁路模式（默认） 01: 流到FIFO模式 10: 满量程停止模式 11: 满量程停止模式
5:0	-	保留

14.5 温度数据1_

名称：温度数据1_地址：
29 (1维) 串行接口：
SYNCR 复位值：0x80

时钟域：SCLK _UI

BIT	NAME	功能
7:0	温度_数据[15:8]	温度数据的高字节

14.6 TEMP_DATA0

Name: TEMP_DATA0 Address: 30 (1Eh) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:0	TEMP_DATA[7:0]	Lower byte of temperature data

Temperature sensor register data TEMP_DATA is updated with new data at max(Accelerometer ODR, Gyroscope ODR).

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 132.48) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA / 2.07) + 25

14.7 ACCEL_DATA_X1

Name: ACCEL_DATA_X1 Address: 31 (1Fh) Serial IF: SYNCR Reset value: 0x80 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_DATA_X[15:8]	Upper byte of Accel X-axis data

14.8 ACCEL_DATA_X0

Name: ACCEL_DATA_X0 Address: 32 (20h) Serial IF: SYNCR Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_DATA_X[7:0]	Lower byte of Accel X-axis data

14.9 ACCEL_DATA_Y1

Name: ACCEL_DATA_Y1 Address: 33 (21h) Serial IF: SYNCR Reset value: 0x80 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_DATA_Y[15:8]	Upper byte of Accel Y-axis data

14.6 温度 数据0_

名称: 温度 _数据0 地址：30 (1Eh) 串行接口：SYNCR 复位值：0x00 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7:0	温度_数据[7:0]	温度数据低字节

温度传感器寄存器数据 TEMP_DATA 会在加速度计输出数据速率和陀螺仪输出数据速率的最大值更新时获取新数据。

传感器数据寄存器中的温度数据值可通过以下公式转换为摄氏度：

摄氏度温度 = (TEMP_DATA / 132.48) + 25

存储在先进先出队列中的温度数据是一个8位数值，FIFO_TEMP_DATA。可通过以下公式转换为摄氏度：

摄氏度温度 = (FIFO_TEMP_DATA / 2.07) + 25

14.7 加速度数据 X1_ _

名称：加速度数据 X1_ _ 地址：31 (1Fh) 串行接口：SYNCR 复位值：0x80 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7:0	加速度计_数据_X轴[15:8]	加速度计X轴数据的高字节

14.8 加速度数据 X0_ _

名称：加速度数据 X0 _ _地址：32 (20h) 串 行接口：SYNCR 复位值：0x00 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7:0	加速度计_数据_X轴[7:0]	加速度X轴数据低字节

14.9 加速度数据 Y1_ _

名称：加速度数据 Y1 _ _地址：33 (21h) 串 行接口：SYNCR 复位值：0x80 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7:0	加速度计_数据_Y轴[15:8]	加速度Y轴数据高字节

14.10 ACCEL_DATA_Y0

Name: ACCEL_DATA_Y0
Address: 34 (22h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y[7:0]	Lower byte of Accel Y-axis data

14.11 ACCEL_DATA_Z1

Name: ACCEL_DATA_Z1
Address: 35 (23h)
Serial IF: SYNCR
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[15:8]	Upper byte of Accel Z-axis data

14.12 ACCEL_DATA_Z0

Name: ACCEL_DATA_Z0
Address: 36 (24h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z[7:0]	Lower byte of Accel Z-axis data

14.13 GYRO_DATA_X1

Name: GYRO_DATA_X1
Address: 37 (25h)
Serial IF: SYNCR
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_X[15:8]	Upper byte of Gyro X-axis data

14.14 GYRO_DATA_X0

Name: GYRO_DATA_X0
Address: 38 (26h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_X[7:0]	Lower byte of Gyro X-axis data

14.10 加速度数据 Y0_ _

名称: 加速度数据 Y0
_ _地址: 34 (22h)
串行接口：SYNCR 复
位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	加速度计_数据_Y轴[7:0]	加速度计Y轴数据低字节

14.11 加速度数据Z轴_ _

名称：加速度数据Z轴
_ _地址：35 (23h)
串行接口：SYNCR 复
位值：0x80
时钟域：SCLK _UI

BIT	NAME	功能
7:0	加速度计_数据_Z轴[15:8]	加速度计Z轴数据高字节

14.12 加速度计数据Z轴0_ _

名称：加速度数据 Z0_ _
地址：36 (24h) 串
行接口：SYNCR
复位值：0x00
时钟域：SCLK 用户界面_

BIT	NAME	功能
7:0	加速度_数据_Z[7:0]	加速度计Z轴数据的低字节

14.13 陀螺仪数据 X1_ _

名称：陀螺仪数据 X1
_ _地址：37 (25h)
串行接口：SYNCR
复位值：0x80
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_数据_X[15:8]	陀螺仪X轴数据高字节

14.14 陀螺仪数据 X0_ _

名称: 陀螺仪数据 X0
_ _地址: 38 (26h) 串
行接口：SYNCR
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_数据_X轴[7:0]	陀螺仪X轴数据的低字节

14.15 GYRO_DATA_Y1

Name: GYRO_DATA_Y1
Address: 39 (27h)
Serial IF: SYNCR
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Y[15:8]	Upper byte of Gyro Y-axis data

14.16 GYRO_DATA_Y0

Name: GYRO_DATA_Y0
Address: 40 (28h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Y[7:0]	Lower byte of Gyro Y-axis data

14.17 GYRO_DATA_Z1

Name: GYRO_DATA_Z1
Address: 41 (29h)
Serial IF: SYNCR
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Z[15:8]	Upper byte of Gyro Z-axis data

14.18 GYRO_DATA_Z0

Name: GYRO_DATA_Z0
Address: 42 (2Ah)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Z[7:0]	Lower byte of Gyro Z-axis data

14.19 TMST_FSYNCH

Name: TMST_FSYNCH
Address: 43 (2Bh)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_UI[15:8]	Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

14.15 陀螺仪数据 Y1_ _

名称: 陀螺仪 _数据 Y1_
地址：39 (27h) 串
行接口：SYNCR
复位值：0x80
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_数据_Y轴[15:8]	陀螺Y轴数据的高字节

14.16 陀螺仪数据 Y0_ _

名称：陀螺仪数据 Y0_ _
地址：40 (28h) 串
行接口：SYNCR
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_数据_Y[7:0]	陀螺Y轴数据的低字节

14.17 陀螺仪数据 Z1_ _

名称：陀螺仪数据 Z1
_ _地址：41 (29h) 串
行接口：SYNCR 复位值：
0x80
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_数据_Z[15:8]	陀螺Z轴数据高字节

14.18 陀螺仪 _DATA_Z0

名称：陀螺仪 _陀螺数据Z0_
地址：42 (2Ah)
串行接口：SYNCR 复
位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_数据_Z轴[7:0]	陀螺仪Z轴数据的低字节

14.19 时间戳帧同步高_

名称: 时间戳帧同步高_
地址: 43 (2Bh) 串行接
口: SYNCR
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	时间戳_帧同步_数据_用户界面[15:8]	存储从FSYNC上升沿到用户界面接口读取状态寄存器中FSYNC标签时最新输出数据速率之间的时间增量的高字节寄存器

14.20 TMST_FSYNCL

Name: TMST_FSYNCL
Address: 44 (2Ch)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_UI[7:0]	Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

14.21 INT_STATUS

Name: INT_STATUS
Address: 45 (2Dh)
Serial IF: R/C
Reset value: 0x10
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	UI_FSYNC_INT	This bit automatically sets to 1 when a UI FSYNC interrupt is generated. The bit clears to 0 after the register has been read.
5	PLL_RDY_INT	This bit automatically sets to 1 when a PLL Ready interrupt is generated. The bit clears to 0 after the register has been read.
4	RESET_DONE_INT	This bit automatically sets to 1 when software reset is complete. The bit clears to 0 after the register has been read.
3	DATA_RDY_INT	This bit automatically sets to 1 when a Data Ready interrupt is generated. The bit clears to 0 after the register has been read.
2	FIFO_THS_INT	This bit automatically sets to 1 when the FIFO buffer reaches the threshold value. The bit clears to 0 after the register has been read.
1	FIFO_FULL_INT	This bit automatically sets to 1 when the FIFO buffer is full. The bit clears to 0 after the register has been read.
0	AGC_RDY_INT	This bit automatically sets to 1 when an AGC Ready interrupt is generated. The bit clears to 0 after the register has been read.

14.22 FIFO_COUNTH

Name: FIFO_COUNTH
Address: 46 (2Eh)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	FIFO_COUNT[15:8]	High Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_REC setting. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

14.20 时间戳帧同步低_

名称: TMST FSYNCL_
地址: 44 (2Ch) 串行接
口：SYNCR
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	时间戳_帧同步_数据_用户界面[7:0]	存储从帧同步上升沿到用户界面接口读取状态寄存器中FSYNC标签前最新输出数据速率之间的时间增量低字节 寄存器

14.21 中断状态_

名称：INT STAT
US_地址：45 (2
Dh) 串行接口：R/C
复位值：0x10
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	用户界面 FSYNC 中断_ _	当产生UI帧同步中断时，该位自动置1。读取寄存器后该位清零为0。
5	PLL就绪中断 _ _	当产生PLL就绪中断时，该位自动置1。读取寄存器后该位清零为0。
4	复位完成中断_ _	当软件复位完成时，该位自动置1。读取寄存器后该位清零为0。
3	数据就绪中断_ _	当生成数据就绪中断时，该位自动置1。读取寄存器后该位清零。
2	FIFO阈值中断_ _	当FIFO缓冲区达到阈值时，该位自动置1。读取寄存器后该位清零。
1	FIFO满中断_ _	当FIFO缓冲区满时，该位自动置1。读取寄存器后该位清零。
0	AGC就绪中断_ _	当产生AGC就绪中断时，此位自动置1。读取寄存器后该位清零为0。

14.22 FIFO COUNTH_

名称：FIFO COUNTH_
地址：46 (2Eh) 串行接
口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	FIFO_计数[15:8]	高比特位，计数表示根据FIFO_计数_记录设置，FIFO中可用的记录或字节数。 读取此字节将锁存FIFO_计数高字节和FIFO计数低字节的数据。 _

14.23 FIFO_COUNTL

Name: FIFO_COUNTL
Address: 47 (2Fh)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	FIFO_COUNT[7:0]	Low Bits, count indicates the number of records or bytes available in FIFO according to FIFO_COUNT_REC setting. Note: Must read FIFO_COUNTH to latch new data for both FIFO_COUNTH and FIFO_COUNTL.

14.24 FIFO_DATA

Name: FIFO_DATA
Address: 48 (30h)
Serial IF: R
Reset value: 0xFF
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	FIFO_DATA	FIFO data port

14.25 APEX_DATA0

Name: APEX_DATA0
Address: 49 (31h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	STEP_CNT[7:0]	Pedometer Output: Lower byte of Step Count measured by pedometer

14.26 APEX_DATA1

Name: APEX_DATA1
Address: 50 (32h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	STEP_CNT[15:8]	Pedometer Output: Upper byte of Step Count measured by pedometer

14.23 FIFO计数低字节_

名称: FIFO _计数低位
地址：47 (2Fh)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	先进先出_计数[7:0]	低位计数表示根据FIFO_COUNT_REC设置，FIFO中可用的记录或字节数。 注意：必须读取FIFO_COUNTH以锁存FIFO_COUNTH和FIFO COUNTL的新数据。_

14.24 FIFO数据_

名称：FIFO _DATA
地址：48 (30h)
串行接口：R
复位值：0xFF
时钟域：SCLK _UI

BIT	NAME	功能
7:0	FIFO_DATA	FIFO数据端口

14.25 APEX 数据0_

名称：APEX 数据
0_地址：49 (31h)
串行接口：SYNCR
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	步进_计数[7:0]	计步器输出：计步器测量的步数计数低字节

14.26 APEX 数据1_

名称：APEX 数据1_地址：50
(32h)
串行接口：SYNCR
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	步进_计数[15:8]	计步器输出: 由计步器测量的步数的高位字节

14.27 APEX_DATA2

Name: APEX_DATA2
Address: 51 (33h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	STEP_CADENCE	Pedometer Output: Walk/run cadency in number of samples. Format is u6.2. e.g. At 50Hz ODR and 2Hz walk frequency, the cadency is 25 samples. The register will output 100.

14.28 APEX_DATA3

Name: APEX_DATA3
Address: 52 (34h)
Serial IF: R
Reset value: 0x04
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:3	-	Reserved
2	DMP_IDLE	0: Indicates DMP is running 1: Indicates DMP is idle
1:0	ACTIVITY_CLASS	Pedometer Output: Detected activity 00: Unknown 01: Walk 10: Run 11: Reserved

14.27 APEX 数据2_

Name: APEX_DATA2
_地址: 51 (33h)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	步频_	计步器输出：步行/跑步步频的样本数量。格式为 u6.2。例如，在50Hz输出数据速率和2Hz步行频率下，步频为25样本。该寄存器将输出100。

14.28 顶点数据3_

名称：顶点 _数据3
地址：52 (34h)
串行接口：R
复位值：0x04
时钟域：SCLK _UI

BIT	NAME	功能
7:3	-	保留
2	DMP空闲_	0：表示DMP正在运行 1: 表示DMP空闲
1:0	活动类别_	计步器输出：检测到的活动 00：未知 01：步行 10: 运行 11: 保留

14.29 APEX_DATA4

Name: APEX_DATA4
Address: 53 (35h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	-	Reserved
4:3	TAP_NUM	Tap Detection Output: Number of taps in the current Tap event 00: No tap 01: Single tap 10: Double tap 11: Reserved
2:1	TAP_AXIS	Tap Detection Output: Represents the accelerometer axis on which tap energy is concentrated 00: X-axis 01: Y-axis 10: Z-axis 11: Reserved
0	TAP_DIR	Tap Detection Output: Polarity of tap pulse 0: Current accelerometer value – Previous accelerometer value is a positive value 1: Current accelerometer value – Previous accelerometer value is a negative value or zero

14.30 APEX_DATA5

Name: APEX_DATA5
Address: 54 (36h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	DOUBLE_TAP_TIMING	DOUBLE_TAP_TIMING measures the time interval between the two taps when double tap is detected. It counts every 16 accelerometer samples as one unit between the 2 tap pulses. Therefore, the value is related to the accelerometer ODR. Time in seconds = DOUBLE_TAP_TIMING * 16 / ODR For example, if the accelerometer ODR is 500 Hz, and the DOUBLE_TAP_TIMING register reading is 6, the time interval value is 6*16/500 = 0.192 seconds.

14.29 顶点数据4_

名称: 顶点数据4_
地址: 53 (35h)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:5	-	保留
4:3	TAP_NUM	轻敲检测输出：当前轻敲事件中的轻敲次数 00：无轻敲 01：单次轻敲 10：双击 11: 保留
2:1	点击轴_	轻敲检测输出: 表示轻敲能量集中的加速度计轴 00：X轴 01：Y轴 10：Z轴 11: 保留
0	点击方向_	轻敲检测输出：轻触脉冲极性 0：当前加速度计值 – 先前加速度计值为正值 1：当前加速度计值 – 先前加速度计值为负值或零

14.30 顶点数据5_

名称：顶点 _DATA5
地址：54 (36h)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5:0	双击计时_ –	DOUBLE_TAP_TIMING用于测量检测到双击时两次轻敲之间的时间间隔。它以每16个加速度计采样为一个单位，计算两次轻敲脉冲之间的间隔。因此，该数值与加速度计输出数据速率相关。 时间（秒） = DOUBLE_TAP_TIMING * 16 / 输出数据速率 例如，若加速度计输出数据速率为500赫兹，且DOUBLE_TAP_TIMING寄存器读数为6，则时间间隔值为6*16/500 = 0.192秒。

14.31 INT_STATUS2

Name: INT_STATUS2
Address: 55 (37h)
Serial IF: R/C
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	-	Reserved
3	SMD_INT	Significant Motion Detection Interrupt, clears on read
2	WOM_Z_INT	Wake on Motion Interrupt on Z-axis, clears on read
1	WOM_Y_INT	Wake on Motion Interrupt on Y-axis, clears on read
0	WOM_X_INT	Wake on Motion Interrupt on X-axis, clears on read

14.32 INT_STATUS3

Name: INT_STATUS3
Address: 56 (38h)
Serial IF: R/C
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_INT	Step Detection Interrupt, clears on read
4	STEP_CNT_OVF_INT	Step Count Overflow Interrupt, clears on read
3	TILT_DET_INT	Tilt Detection Interrupt, clears on read
2	WAKE_INT	Wake Event Interrupt, clears on read
1	SLEEP_INT	Sleep Event Interrupt, clears on read
0	TAP_DET_INT	Tap Detection Interrupt, clears on read

14.33 SIGNAL_PATH_RESET

Name: SIGNAL_PATH_RESET
Address: 75 (4Bh)
Serial IF: W/C
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	DMP_INIT_EN	When this bit is set to 1, the DMP is enabled
5	DMP_MEM_RESET_EN	When this bit is set to 1, the DMP memory is reset
4	-	Reserved
3	ABORT_AND_RESET	When this bit is set to 1, the signal path is reset by restarting the ODR counter and signal path controls
2	TMST_STROBE	When this bit is set to 1, the time stamp counter is latched into the time stamp register. This is a write on clear bit.
1	FIFO_FLUSH	When set to 1, FIFO will get flushed.
0	-	Reserved

14.31 中断状态2_

名称: 中断状态2_地址:
55 (37h) 串行接口 :
R/C
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:4	-	保留
3	SMD_INT	显著运动检测中断，读取后清除
2	WOM_Z_INT	Z轴运动唤醒中断，读取后清除
1	WOM_Y_INT	Y轴运动唤醒中断，读取后清除
0	WOM_X_INT	X轴运动唤醒中断，读取后清除

14.32 中断状态3_

名称：中断状态3_地
址：56 (38h) 串行接
口：R/C
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	STEP_DET_INT	步进检测中断，读取时清除
4	步进计数溢出_ _ _INT	步进计数溢出中断，读取时清除
3	倾斜检测中断_ _	倾斜检测中断，读取时清除
2	WAKE_INT	唤醒事件中断，读取时清除
1	睡眠中断_	睡眠事件中断，读取时清除
0	点击检测中断 _ _	轻击检测中断，读取时清除

14.33 信号路径重置_ _

名称：信号路径重置_ _
地址：75 (4Bh) 串行接口：
写/清除 复位值：0x00 时钟
域：SCLK
_UI

BIT	NAME	功能
7	-	保留
6	DMP初始化使能_ _	当此位设置为1时 , DMP将被启用
5	数字运动处理器 内存 重置 使能 _ _ _	当此位设为1时，数字运动处理器内存将被重置
4	-	保留
3	中止并重置_ _	当此位设为1时，信号路径将通过重启输出数据速率计数器和信号路径控制进行重置
2	时间戳选通_	当此位设置为1时，时间戳计数器将被锁存至时间戳寄存器。此为写入清除位。
1	FIFO刷新_	设置为1时，先进先出队列将被刷新。
0	-	保留

14.34 INTF_CONFIG0

Name: INTF_CONFIG0
Address: 76 (4Ch)
Serial IF: R/W
Reset value: 0x30
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	FIFO_HOLD_LAST_DATA_EN	This bit selects the treatment of invalid samples. See **Invalid Data Generation** note below this register description. **Setting this bit to 0:** In order to signal an invalid sample, and to differentiate it from a valid sample based on values only: Sense Registers: • Do not receive invalid samples. They hold the last valid sample. Repeated reading before new sample received will yield copies of the last valid sample. • Valid samples of values -32768, -32767 are replaced with -32766 • FSYNC Tagging can modify the least significant bit and further limit values (see section 12.8). FIFO: • 16-bit FIFO packet: Same as Sense Registers, except: ○ FSYNC tagging is not applied to data in FIFO. • 20-bit FIFO packet: ○ Invalid samples are indicated with the value -524288 ○ Valid samples in {-524288 to -524258} are replaced by -524256 ○ Valid Gyro samples: All Even numbers in { -524256 to +524286} ○ Valid Accel samples: All numbers divisible by 4 in {-524256 to +524284} ○ FSYNC tagging is not applied to data in FIFO. **Setting this bit to 1:** Sense registers: • Do not receive invalid samples. They hold the last valid sample. Repeated reading before new sample received will yield copies of the last valid sample. • FSYNC Tagging can modify the least significant bit and further limit values (see section 12.8). FIFO: • Invalid sample will get copy of last valid sample • 16-bit FIFO packet: Same as Sense Registers, except: ○ FSYNC tagging is not applied to data in FIFO. • 20-bit FIFO packet: ○ Valid Gyro samples: All Even numbers in {-524288 to +524286} ○ - Valid Accel samples: All numbers divisible by 4 in {-524288 to +524284} ○ FSYNC tagging is not applied to data in FIFO.

14.34 接口配置0_

名称: 接口配置0_
地址: 76 (4Ch)
串行接口：读/写
复位值：0x30
时钟域：SCLK _UI

BIT	NAME	功能
7	FIFO保持最后数据E_ _ _ _ N	该位选择无效样本的处理方式。参见**无效数据生成**此寄存器描述下方的注释。 **将此位设为0：** 为了标记一个无效样本，并将其与仅基于值的有效样本区分开来： 感应寄存器： • 不接收无效样本。它们保留最后有效样本。在新样本接收前重复读取将得到最后有效样本的副本。 • 值为-32768、-32767的有效样本将被替换为-32766 • FSYNC标记可修改最低有效位并进一步限制数值（参见第12.8节）。 先进先出： • 16位FIFO数据包：与感应寄存器相同，但存在以下例外： ○ FSYNC标记不适用于先进先出队列中的数据。 • 20位FIFO数据包： ○ 无效样本用值-524288表示 ○ 有效样本在{-524288至-524258}范围内将被替换为-524256 ○ 有效陀螺仪样本：{ -524256至+524286}范围内的所有偶数 ○ 有效加速度计样本：{-524256至...范围内所有能被4整除的数字+524284} ○ FSYNC标记不适用于FIFO中的数据。 **将此位设置为1：** 感应寄存器： • 不接收无效样本。它们保留最后有效样本。在新样本接收前重复读取将得到最后有效样本的副本。 • FSYNC标记可修改最低有效位并进一步限制值（参见第12.8节）。 先进先出： • 无效样本将获取最后有效样本的副本 • 16位FIFO数据包：与感应寄存器相同，但有以下例外： ○ FSYNC标记不适用于FIFO中的数据。 • 20位FIFO数据包： ○ 有效陀螺仪样本：{-524288至+524286}范围内的所有偶数 ○ - 有效加速度样本：{-524288至+524284}范围内所有能被4整除的数字。 FSYNC标记不适用于FIFO中的数据。

6	FIFO_COUNT_REC	0: FIFO count is reported in bytes 1: FIFO count is reported in records (1 record = 16 bytes for header + gyro + accel + temp sensor data + time stamp, or 8 bytes for header + gyro/accel + temp sensor data, or 20 bytes for header + gyro + accel + temp sensor data + time stamp + 20-bit extension data)
5	FIFO_COUNT_ENDIAN	0: FIFO count is reported in Little Endian format 1: FIFO count is reported in Big Endian format (default)
4	SENSOR_DATA_ENDIAN	0: Sensor data is reported in Little Endian format 1: Sensor data is reported in Big Endian format (default)
3:2	-	Reserved
1:0	UI_SIFS_CFG	0x: Reserved 10: Disable SPI 11: Disable I2C

Invalid Data Generation: FIFO/Sense Registers may contain invalid data under the following conditions:

a) From power on reset to first ODR sample of any sensor (accel, gyro, temp sensor)
b) When any sensor is disabled (accel, gyro, temp sensor)
c) When accel and gyro are enabled with different ODRs. In this case, the sensor with lower ODR will generate invalid samples when it has no new data.

Invalid data can take special values or can hold last valid sample received. For -32768 to be used as a flag for invalid accel/gyro samples, the valid accel/gyro sample range is limited in such case as well. Bit 7 of INTF_CONFIG0 controls what values invalid (and valid) samples can take as shown above.

14.35 INTF_CONFIG1

Name: INTF_CONFIG1
Address: 77 (4Dh)
Serial IF: R/W
Reset value: 0x91
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	-	Reserved
3	ACCEL_LP_CLK_SEL	0: Accelerometer LP mode uses Wake Up oscillator clock 1: Accelerometer LP mode uses RC oscillator clock
2	RTC_MODE	0: No input RTC clock is required 1: RTC clock input is required
1:0	CLKSEL	00: Always select internal RC oscillator 01: Select PLL when available, else select RC oscillator (default) 10: Reserved 11: Disable all clocks

6	FIFO计数 记录_ _	0: FIFO计数以字节为单位报告 1: FIFO计数以记录为单位报告（1条记录= 16 字节用于头部+ 陀螺仪+ 加速度计 + 温度传感器数据 + 时间戳，或8字节头部 + 陀螺仪/加速度计 + 温度传感器数据，或20字节头部 + 陀螺仪 + 加速度计 + 温度传感器数据 + 时间戳 + 20-位扩展数据)
5	FIFO计数字节序_ _	0：FIFO计数以小端格式报告 1：FIFO计数以大端格式报告（默认）
4	传感器数据字节序_ _	0: 传感器数据以小端格式报告 1: 传感器数据以大端格式报告（默认）
3:2	-	保留
1:0	用户界面SIFS配置_ _	0x: 保留 10: 禁用SPI 11: 禁用I2C

无效数据生成：FIFO/感应寄存器在以下条件下可能包含无效数据：

a) 从上电复位到任何传感器（加速度计、陀螺仪、温度传感器）的首个ODR采样期间
b) 当任何传感器被禁用时（加速度计、陀螺仪、温度传感器）
c) 当加速度计和陀螺仪以不同输出数据速率启用时。此时，输出数据速率较低的传感器在没有新数据时将生成无效样本。

无效数据可以采用特殊值或保留最后接收的有效样本。若要将-32768用作无效加速度计/陀螺仪样本的标记，则在此情况下有效加速度计/陀螺仪样本范围也会受到限制。如上方所示，INTF_CONFIG0的位7控制着无效（及有效）样本可采用的数值范围。

14.35 接口配置1_

名称：接口配置1_地址：
77（4Dh）串行接口：
读/写复位值：0x91

时钟域：SCLK _UI

BIT	NAME	功能
7:4	-	保留
3	加速度低通滤波 CLK 选择 _ _ _	0: 加速度计低功耗模式使用唤醒振荡器时钟 1: 加速度计低功耗模式使用RC振荡器时钟
2	实时时钟模式_	0: 无需输入RTC时钟 1: 需要输入RTC时钟
1:0	CLKSEL	00: 始终选择内部RC振荡器 01: 有PLL时选择PLL，否则选择RC振荡器（默认） 10: 保留 11: 禁用所有时钟

14.36 PWR_MGMT0

Name: PWR_MGMT0
Address: 78 (4Eh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	TEMP_DIS	0: Temperature sensor is enabled (default) 1: Temperature sensor is disabled
4	IDLE	If this bit is set to 1, the RC oscillator is powered on even if Accel and Gyro are powered off. Nominally this bit is set to 0, so when Accel and Gyro are powered off, the chip will go to OFF state, since the RC oscillator will also be powered off
3:2	GYRO_MODE	00: Turns gyroscope off (default) 01: Places gyroscope in Standby Mode 10: Reserved 11: Places gyroscope in Low Noise (LN) Mode Gyroscope needs to be kept ON for a minimum of 45ms. When transitioning from OFF to any of the other modes, do not issue any register writes for 200µs.
1:0	ACCEL_MODE	00: Turns accelerometer off (default) 01: Turns accelerometer off 10: Places accelerometer in Low Power (LP) Mode 11: Places accelerometer in Low Noise (LN) Mode When transitioning from OFF to any of the other modes, do not issue any register writes for 200µs.

14.36 电源 管理0_

名称: 电源 管理0_
地址: 78 (4Eh)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	温度DIS_	0: 温度传感器启用（默认） 1: 温度传感器禁用
4	IDLE	若此位设为1，即使加速度计和陀螺仪关闭，RC振荡器仍保持开启。 默认此位设为0，因此当加速度计和陀螺仪关闭时，芯片将进入关闭状态，因为RC振荡器也会被关闭。
3:2	陀螺仪模式_	00: 关闭陀螺仪（默认） 01: 将陀螺仪置于待机模式 10: 保留 11: 将陀螺仪置于低噪声（LN）模式 陀螺仪需保持开启状态至少45毫秒。从关闭状态切换到其他模式时，200微秒内不得进行任何寄存器写入操作。
1:0	加速度计模式_	00: 关闭加速度计（默认） 01: 关闭加速度计 10: 将加速度计置于低功耗（LP）模式 11: 将加速度计置于低噪声(LN)模式 当从关闭状态切换到其他任何模式时，200微秒内不要进行任何寄存器写入操作。

14.37 GYRO_CONFIG0

Name: GYRO_CONFIG0
Address: 79 (4Fh)
Serial IF: R/W
Reset value: 0x06
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	GYRO_FS_SEL	Full scale select for gyroscope UI interface output 000: ±2000dps (default) 001: ±1000dps 010: ±500dps 011: ±250dps 100: ±125dps 101: ±62.5dps 110: ±31.25dps 111: ±15.625dps
4	-	Reserved
3:0	GYRO_ODR	Gyroscope ODR selection for UI interface output 0000: Reserved 0001: 32kHz 0010: 16kHz 0011: 8kHz 0100: 4kHz 0101: 2kHz 0110: 1kHz (default) 0111: 200Hz 1000: 100Hz 1001: 50Hz 1010: 25Hz 1011: 12.5Hz 1100: Reserved 1101: Reserved 1110: Reserved 1111: 500Hz

14.37 陀螺仪 配置0_

名称: 陀螺仪 配置0_
地址: 79 (4Fh)
串行接口：读/写
复位值：0x06
时钟域：SCLK _UI

BIT	NAME	功能
7:5	GYRO_FS_SEL	陀螺仪用户界面接口输出的满量程选择 000: ±2000度每秒（默认） 001: ±1000度每秒 010: ±500度每秒 011: ±250度每秒 100: ±125度每秒 101: ±62.5度每秒 110: ±31.25度每秒 111: ±15.625度每秒
4	-	保留
3:0	陀螺仪输出数据速率_	用于UI界面输出的陀螺仪输出数据速率选择 0000: 保留 0001: 32千赫 0010: 16千赫 0011: 8千赫 0100: 4千赫 0101: 2千赫 0110: 1千赫（默认） 0111: 200赫兹 1000: 100赫兹 1001: 50赫兹 1010: 25赫兹 1011: 12.5赫兹 1100: 保留 1101: 保留 1110: 保留 1111: 500赫兹

14.38 ACCEL_CONFIG0

Name: ACCEL_CONFIG0
Address: 80 (50h)
Serial IF: R/W
Reset value: 0x06
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	ACCEL_FS_SEL	Full scale select for accelerometer UI interface output 000: ±16g (default) 001: ±8g 010: ±4g 011: ±2g 100: Reserved 101: Reserved 110: Reserved 111: Reserved
4	-	Reserved
3:0	ACCEL_ODR	Accelerometer ODR selection for UI interface output 0000: Reserved 0001: 32kHz (LN mode) 0010: 16kHz (LN mode) 0011: 8kHz (LN mode) 0100: 4kHz (LN mode) 0101: 2kHz (LN mode) 0110: 1kHz (LN mode) (default) 0111: 200Hz (LP or LN mode) 1000: 100Hz (LP or LN mode) 1001: 50Hz (LP or LN mode) 1010: 25Hz (LP or LN mode) 1011: 12.5Hz (LP or LN mode) 1100: 6.25Hz (LP mode) 1101: 3.125Hz (LP mode) 1110: 1.5625Hz (LP mode) 1111: 500Hz (LP or LN mode)

14.38 加速度计配置0_

名称: 加速度计配置0_
地址: 80 (50h)
串行接口：读/写
复位值：0x06
时钟域：SCLK _UI

BIT	NAME	功能
7:5	加速度 _FS_SEL 计	加速度计用户界面输出满量程选择 000: ±16重力加速度 (默认) 001: ±8重力加速度 010: ±4重力加速度 011: ±2重力加速度 100: 保留 101: 保留 110: 保留 111: 保留
4	-	保留
3:0	加速度计输出数 据速率_	用于UI界面输出的加速度计ODR选择 0000: 保留 0001: 32千赫（低噪声模式） 0010: 16千赫（低噪声模式） 0011: 8千赫（低噪声模式） 0100: 4千赫（低噪声模式） 0101: 2千赫（低噪声模式） 0110: 1千赫（低噪声模式）（默认） 0111: 200赫兹（低功耗或低噪声模式） 1000: 100赫兹（低功耗或低噪声模式） 1001: 50赫兹（低功耗或低噪声模式） 1010: 25赫兹（低功耗或低噪声模式） 1011: 12.5赫兹（低功耗或低噪声模式） 1100: 6.25赫兹（低通模式） 1101: 3.125赫兹 (低通模式) 1110: 1.5625赫兹 (低通模式) 1111: 500赫兹 (低通或线性模式)

14.39 GYRO_CONFIG1

Name: GYRO_CONFIG1
Address: 81 (51h)
Serial IF: R/W
Reset value: 0x16
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	TEMP_FILT_BW	Sets the bandwidth of the temperature signal DLPF 000: DLPF BW = 4000Hz; DLPF Latency = 0.125ms (default) 001: DLPF BW = 170Hz; DLPF Latency = 1ms 010: DLPF BW = 82Hz; DLPF Latency = 2ms 011: DLPF BW = 40Hz; DLPF Latency = 4ms 100: DLPF BW = 20Hz; DLPF Latency = 8ms 101: DLPF BW = 10Hz; DLPF Latency = 16ms 110: DLPF BW = 5Hz; DLPF Latency = 32ms 111: DLPF BW = 5Hz; DLPF Latency = 32ms
4	-	Reserved
3:2	GYRO_UI_FILT_ORD	Selects order of GYRO UI filter 00: 1st Order 01: 2nd Order 10: 3rd Order 11: Reserved
1:0	GYRO_DEC2_M2_ORD	Selects order of GYRO DEC2_M2 Filter 00: Reserved 01: Reserved 10: 3rd Order 11: Reserved

14.39 陀螺仪配置1_

名称: 陀螺仪配置1_地
址: 81 (51h)
串行接口：读/写
复位值：0x16
时钟域：SCLK _UI

BIT	NAME	功能
7:5	温度滤波器带宽_ _	设置温度信号数字低通滤波器的带宽 000：数字低通滤波器 带宽 = 4000赫兹；数字低通滤波器延迟 = 0.125毫秒（默认） 001：数字低通滤波器带宽 = 170赫兹；数字低通滤波器延迟 = 1毫秒 010：数字低通滤波器带宽 = 82赫兹；数字低通滤波器延迟 = 2毫秒 011: 数字低通滤波器 带宽 = 40赫兹; 数字低通滤波器 延迟 = 4 毫秒 100: 数字低通滤波器 带宽 = 20 赫兹 ; 数字低通滤波器 延迟 = 8毫秒 101: 数字低通滤波器 带宽 = 10赫兹; 数字低通滤波器 延迟 = 16毫秒 110: 数字低通滤波器 带宽 = 5 赫兹; 数字低通滤波器 延迟 = 32毫秒 111: 数字低通滤波器带宽 = 5 赫兹 ; 数字低通滤波器 延迟 = 32 毫秒
4	-	保留
3:2	GYRO_UI_FILT_ORD	选择陀螺仪用户界面滤波器的阶数 00: 1st 阶 01: 2nd 阶 10: 3rd 阶 11: 保留
1:0	陀螺仪 DEC2 M2 输出数据速率 _ _ _	选择陀螺仪 DEC2 M2 滤波器的阶数_00: 保留 01: 保留 10: 3rd 阶 11: 保留

14.40 GYRO_ACCEL_CONFIG0

Name: GYRO_ACCEL_CONFIG0
Address: 82 (52h)
Serial IF: R/W
Reset value: 0x11
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_UI_FILT_BW	**LN Mode:** Bandwidth for Accel LPF 0 BW=ODR/2 1 BW=max(400Hz, ODR)/4 (default) 2 BW=max(400Hz, ODR)/5 3 BW=max(400Hz, ODR)/8 4 BW=max(400Hz, ODR)/10 5 BW=max(400Hz, ODR)/16 6 BW=max(400Hz, ODR)/20 7 BW=max(400Hz, ODR)/40 8 to 13: Reserved 14 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(400Hz, ODR) 15 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(200Hz, 8*ODR) **LP Mode:** 0 Reserved 1 1x AVG filter (default) 2 to 5 Reserved 6 16x AVG filter 7 to 15 Reserved
3:0	GYRO_UI_FILT_BW	**LN Mode:** Bandwidth for Gyro LPF 0 BW=ODR/2 1 BW=max(400Hz, ODR)/4 (default) 2 BW=max(400Hz, ODR)/5 3 BW=max(400Hz, ODR)/8 4 BW=max(400Hz, ODR)/10 5 BW=max(400Hz, ODR)/16 6 BW=max(400Hz, ODR)/20 7 BW=max(400Hz, ODR)/40 8 to 13: Reserved 14 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(400Hz, ODR) 15 Low Latency option: Trivial decimation @ ODR of Dec2 filter output. Dec2 runs at max(200Hz, 8*ODR)

14.40 陀螺仪加速度计配置0_ _

名称: 陀螺仪加速度计配置0
_ _地址: 82 (52h) 串行接口:
读/写
复位值：0x11
时钟域：SCLK _UI

BIT	NAME	功能
7:4	加速度计用户界面滤波器带宽_ _ _	**线性模式：** 加速度低通滤波器带宽 0 带宽=输出数据速率/2 1 带宽=最大值(400赫兹, 输出数据速率)/4 (默认) 2 带宽=最大值(400赫兹, 输出数据速率)/5 3 带宽=最大值(400赫兹, 输出数据速率)/8 4 带宽=最大值(400赫兹, 输出数据速率)/10 5 带宽=最大值(400赫兹, 输出数据速率)/16 6 带宽=最大值(400赫兹, 输出数据速率)/20 7 带宽=最大值(400赫兹, 输出数据速率)/40 8 至 13: 保留 14 低延迟选项: Dec2滤波器输出的输出数据速率处的简单抽取。Dec2运行于max(400赫兹, 输出数据速率) 15 低延迟选项: Dec2滤波器输出的输出数据速率处的简单抽取。Dec2运行于max(200赫兹, 8倍输出数据速率) **低通模式：** 0 保留 1 1倍均值滤波器（默认） 2 至 5 保留 6 16倍均值滤波器 7 至 15 保留
3:0	陀螺仪用户界面滤波器带宽_ _ _	**线性模式：** 陀螺仪低通滤波器带宽 0 带宽=输出数据速率/2 1 带宽=最大值(400赫兹, 输出数据速率)/4 (默认) 2 带宽=最大值(400赫兹, 输出数据速率)/5 3 带宽=最大值(400赫兹, 输出数据速率)/8 4 带宽=最大值(400赫兹, 输出数据速率)/10 5 带宽=最大值(400赫兹, 输出数据速率)/16 6 带宽=最大值(400赫兹, 输出数据速率)/20 7 带宽=最大值(400赫兹, 输出数据速率)/40 8 至 13: 保留 14 低延迟选项: Dec2滤波器输出的输出数据速率处的简单抽取。Dec2运行于最大值(400赫兹, 输出数据速率) 15 低延迟选项: Dec2滤波器输出的输出数据速率处的简单抽取。Dec2运行于最大值(200赫兹, 8倍输出数据速率)

14.41 ACCEL_CONFIG1

Name: ACCEL_CONFIG1
Address: 83 (53h)
Serial IF: R/W
Reset value: 0x0D
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	-	Reserved
4:3	ACCEL_UI_FILT_ORD	Selects order of ACCEL UI filter 00: 1st Order 01: 2nd Order 10: 3rd Order 11: Reserved
2:1	ACCEL_DEC2_M2_ORD	Order of Accelerometer DEC2_M2 filter 00: Reserved 01: Reserved 10: 3rd order 11: Reserved
0	-	Reserved

14.42 TMST_CONFIG

Name: TMST_CONFIG
Address: 84 (54h)
Serial IF: R/W
Reset value: 0x23
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	-	Reserved
4	TMST_TO_REGS_EN	0: TMST_VALUE[19:0] read always returns 0s 1: TMST_VALUE[19:0] read returns timestamp value
3	TMST_RES	Time Stamp resolution: When set to 0 (default), time stamp resolution is 1 µs. When set to 1: If RTC is disabled, resolution is 16µs. If RTC is enabled, resolution is 1 RTC clock period
2	TMST_DELTA_EN	Time Stamp delta enable: When set to 1, the time stamp field contains the measurement of time since the last occurrence of ODR.
1	TMST_FSYNC_EN	Time Stamp register FSYNC enable (default). When set to 1, the contents of the Timestamp feature of FSYNC is enabled. The user also needs to select FIFO_TMST_FSYNC_EN in order to propagate the timestamp value to the FIFO.
0	TMST_EN	0: Time Stamp register disable 1: Time Stamp register enable (default)

14.41 加速度计配置1_

名称: 加速度计 _配置1
地址：83 (53h)
串行接口：读/写
复位值：0x0D
时钟域：SCLK _UI

BIT	NAME	功能
7:5	-	保留
4:3	加速度 _UI_FILT_ORD 计	选择加速度计用户界面滤波器阶数 00: 1st 阶数 01: 2nd 阶数 10: 3rd 阶数 11: 保留
2:1	加速度 _DEC2_M2_ORD 计	加速度计DEC2 M2滤波器阶数_00: 保留 01: 保留 10: 3rd 阶数 11: 保留
0	-	保留

14.42 时间戳 配置_

名称：时间戳 配置_地
址：84 (54h) 串行接口：
读/写
复位值：0x23
时钟域：SCLK _UI

BIT	NAME	功能
7:5	-	保留
4	时间戳 到 寄存器 使能 _ _ _	0: 时间戳_值[19:0] 读 总是返回 0 1: 时间戳_值[19:0] 读 返回 时间戳值
3	时间戳 分辨率 _	时间戳分辨率: 当设置为 0 (默认) 时，时间戳分辨率为 1 微秒。 设为1时：若RTC禁用，分辨率为16微秒；若RTC启用，分辨率为1个RTC时钟周期
2	时间戳增量使能_ _	时间戳增量启用：设为1时，时间戳字段记录自上次输出数据速率(ODR)触发后的时间测量值。
1	TMST FSYNC启用 _ _	时间戳寄存器FSYNC启用（默认）。设为1时，将启用FSYNC的时间戳特性功能。用户还需选择FIFO_TMST_FSYNC_EN才能将时间戳值传递至FIFO。
0	TMST启用_	0: 时间戳寄存器禁用 1: 时间戳寄存器启用（默认）

14.43 APEX_CONFIG0

Name: APEX_CONFIG0 Address: 86 (56h) Serial IF: R/W Reset value: 0x82 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7	DMP_POWER_SAVE	0: DMP power save mode not active 1: DMP power save mode active (default)
6	TAP_ENABLE	0: Tap Detection not enabled 1: Tap Detection enabled when accelerometer ODR is set to one of the ODR values supported by Tap Detection (200Hz, 500Hz, 1kHz)
5	PED_ENABLE	0: Pedometer not enabled 1: Pedometer enabled
4	TILT_ENABLE	0: Tilt Detection not enabled 1: Tilt Detection enabled
3	R2W_EN	0: Raise to Wake/Sleep not enabled 1: Raise to Wake/Sleep enabled
2	-	Reserved
1:0	DMP_ODR	00: 25Hz 01: Reserved 10: 50Hz 11: Reserved

14.44 SMD_CONFIG

Name: SMD_CONFIG Address: 87 (57h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	WOM_INT_MODE	0: Set WoM interrupt on the OR of all enabled accelerometer thresholds 1: Set WoM interrupt on the AND of all enabled accelerometer threshold
2	WOM_MODE	0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample
1:0	SMD_MODE	00: SMD disabled 01: Reserved 10: SMD short (1 sec wait) An SMD event is detected when two WOM are detected 1 sec apart 11: SMD long (3 sec wait) An SMD event is detected when two WOM are detected 3 sec apart

14.43 APEX配置0_

名称: APEX配置0_地址: 86 (56h) 串行接口：读/ 写 复位值: 0x82 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7	DMP省电模式_ _	0: DMP省电模式未激活 1: DMP省电模式激活（默认）
6	轻敲启用_	0: 敲击检测未启用 1: 当加速度计输出数据速率设置为敲击检测支持的输出数据速率之一（200赫兹、500赫兹、1千赫兹）时，敲击检测启用
5	计步启用_	0: 计步器未启用 1: 计步器启用
4	倾斜启用_	0: 倾斜检测未启用 1: 倾斜检测已启用
3	R2W启用_	0: 抬手唤醒/睡眠未启用 1: 抬手唤醒/睡眠已启用
2	-	保留
1:0	数字运动处理器输出数据速率_	00: 25赫兹 01: 保留 10: 50赫兹 11: 保留

14.44 显著运动检测配置_

名称：显著运动检测配 置_地址：87 (57h) 串行 接口：读/写 复位值： 0x00 时钟域：SCLK 用 户界面_		
BIT	**NAME**	**功能**
7:4	-	保留
3	女性中断模式_ _	0：在所有启用的加速度计阈值的或上设置女性中断 1：在所有启用的加速度计阈值的与上设置女性中断
2	女性模式_	0: 初始样本已存储。未来样本将与初始样本比较 1: 将当前样本与前一样本比较
1:0	SMD模式_	00: SMD禁用 01: 保留 10: SMD短事件（1秒等待）当检测到两个WOM间隔1秒时，即判定发生SMD事件 11: SMD长事件（3秒等待）当检测到两个WOM间隔3秒时，即判定发生SMD事件

14.45 FIFO_CONFIG1

Name: FIFO_CONFIG1
Address: 95 (5Fh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	FIFO_RESUME_PARTIAL_RD	0: Partial FIFO read disabled, requires re-reading of the entire FIFO 1: FIFO read can be partial, and resume from last read point
5	FIFO_WM_GT_TH	Trigger FIFO watermark interrupt on every ODR (DMA write) if FIFO_COUNT ≥ FIFO_WM_TH
4	FIFO_HIRES_EN	Enable 3 bytes of extended 20-bits accel, gyro data + 1 byte of extended 16-bit temperature sensor data to be placed into the FIFO
3	FIFO_TMST_FSYNC_EN	Must be set to 1 for all FIFO use cases when FSYNC is used.
2	FIFO_TEMP_EN	Enable temperature sensor packets to go to FIFO
1	FIFO_GYRO_EN	Enable gyroscope packets to go to FIFO
0	FIFO_ACCEL_EN	Enable accelerometer packets to go to FIFO

14.46 FIFO_CONFIG2

Name: FIFO_CONFIG2
Address: 96 (60h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	FIFO_WM[7:0]	Lower bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_REC setting. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source.

14.47 FIFO_CONFIG3

Name: FIFO_CONFIG3
Address: 97 (61h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	FIFO_WM[11:8]	Upper bits of FIFO watermark. Generate interrupt when the FIFO reaches or exceeds FIFO_WM size in bytes or records according to FIFO_COUNT_REC setting. Interrupt only fires once. This register should be set to non-zero value, before choosing this interrupt source.

Note: Do not set FIFO_WM to value 0.

14.45 先进先出 配置1_

名称: 先进先出 配置1_
地址: 95 (5Fh)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	先进先出 分辨率 部件 读取 _ _ _	0: 部分FIFO读取禁用，需重新读取整个FIFO 1: FIFO读取可部分进行，并从上次读取点恢复
5	FIFO水位标记大于阈值 _ _ _	在每次输出数据速率（DMA写入）时触发FIFO水位标记中断，如果FIFO计数≥ FIFO水位标记_ _TH
4	FIFO高分辨率使能 _ _	启用3字节的扩展20位加速度计、陀螺仪数据+ 1 字节的扩展待存入先进先出队列的16位温度传感器数据
3	先进先出时间戳帧同步使能_ _ _	当使用帧同步功能时，所有涉及先进先出的应用场景必须将该位设为1。
2	先进先出温度传感器使能_ _	允许温度传感器数据包进入先进先出队列
1	FIFO_GYRO_EN	允许陀螺仪数据包进入先进先出队列
0	FIFO_加速度计 _EN	使加速度计数据包进入先进先出队列

14.46 先进先出 配置2_

名称: 先进先出 _配置2
地址: 96 (60h)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	先进先出_ 水位标记[7:0]	先进先出水位标记的低位。当FIFO达到或超过根据FIFO_WM设置的字节或记录大小时触发中断。 FIFO_COUNT_REC设置。中断仅触发一次。在选择此中断源前，该寄存器应设置为非零值。

14.47 FIFO配置3_

Name: FIFO CONFIG3
_地址：97 (61h)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:4	-	保留
3:0	先进先出_ 水位标记[11:8]	先进先出水位标记的高位部分。当先进先出存储器中的数据量达到或超过先进先出_水位标记所设定的字节数或记录数时，将产生中断。 先进先出_计数_记录设置。中断仅触发一次。在选择此中断源之前，该寄存器应设置为非零值。

注意：不要将FIFO水位标记设置为0值。_

14.48 FSYNC_CONFIG

Name: FSYNC_CONFIG Address: 98 (62h) Serial IF: R/W Reset value: 0x10 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6:4	FSYNC_UI_SEL	000: Do not tag FSYNC flag 001: Tag FSYNC flag to TEMP_OUT LSB 010: Tag FSYNC flag to GYRO_XOUT LSB 011: Tag FSYNC flag to GYRO_YOUT LSB 100: Tag FSYNC flag to GYRO_ZOUT LSB 101: Tag FSYNC flag to ACCEL_XOUT LSB 110: Tag FSYNC flag to ACCEL_YOUT LSB 111: Tag FSYNC flag to ACCEL_ZOUT LSB
3:2	-	Reserved
1	FSYNC_UI_FLAG_CLEAR_SEL	0: FSYNC flag is cleared when UI sensor register is updated 1: FSYNC flag is cleared when UI interface reads the sensor register LSB of FSYNC tagged axis
0	FSYNC_POLARITY	0: Start from Rising edge of FSYNC pulse to measure FSYNC interval 1: Start from Falling edge of FSYNC pulse to measure FSYNC interval

Please also refer to Section 12.8 for supplementary information on FSYNC tag.

14.49 INT_CONFIG0

Name: INT_CONFIG0 Address: 99 (63h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5:4	UI_DRDY_INT_CLEAR	Data Ready Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on Sensor Register Read 11: Clear on Status Bit Read AND on Sensor Register read
3:2	FIFO_THS_INT_CLEAR	FIFO Threshold Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read
1:0	FIFO_FULL_INT_CLEAR	FIFO Full Interrupt Clear Option (latched mode) 00: Clear on Status Bit Read (default) 01: Clear on Status Bit Read 10: Clear on FIFO data 1Byte Read 11: Clear on Status Bit Read AND on FIFO data 1 byte read

14.48 帧同步 配置_

名称: 帧同步 配置_地 址: 98 (62h) 串行接口：读/写 复位值：0x10 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7	-	保留
6:4	帧同步 用户界面 选择_ _	000：不标记帧同步标志 001：将帧同步标志标记到温度_输出最低有效位 010：将帧同步标志标记到陀螺仪_X轴输出最低有效位 011：将帧同步标志标记到陀螺仪_Y轴输出最低有效位 100：将帧同步标志标记到陀螺仪_Z轴输出最低有效位 101：将帧同步标志标记到加速度计_X轴输出最低有效位 110：将帧同步标志标记到加速度计_Y轴输出最低有效位 111：将帧同步标志标记到加速度计_Z轴输出最低有效位
3:2	-	保留 FSYNC_用户界面_标志_清除_SE L 0: 当用户界面传感器寄存器更新时，FSYNC标志被清除
1		1: 当用户界面接口读取传感器寄存器时，FSYNC 标志被清除 已标记 FSYNC 轴的最低有效位 FSYNC_ 极性 0: 从 FSYNC 脉冲的上升沿开始测量FSYNC间隔 1: 从FSYNC脉冲的下降沿开始测量FSYNC间隔
0		

请同时参考第12.8节获取关于FSYNC标签的补充信息。

14.49 中断_配置0

名称：中断配置0_地 址：99 (63h) 串行接 口：读/写 复位值：0x00 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7:6	-	保留
5:4	UI数据就绪中断清除 _ _ _	数据就绪中断清除选项（锁存模式）00：状态位读取时清除（默认） 01：状态位读取时清除 10：传感器寄存器读取时清除 11：状态位读取时清除且传感器寄存器读取时清除
3:2	FIFO阈值中断清除_ _ _	FIFO阈值中断清除选项（锁存模式）00：状态位读取时清除（默认） 01：状态位读取时清除 10：FIFO数据1字节读取时清除 11：状态位读取和FIFO数据1字节读取时清除
1:0	FIFO满中断清除_ _ _	FIFO满中断清除选项（锁存模式）00：状态位读取时清除（默认） 01：状态位读取时清除 10：FIFO数据1字节读取时清除 11：状态位读取和FIFO数据1字节读取时清除

14.50 INT_CONFIG1

Name: INT_CONFIG1
Address: 100 (64h)
Serial IF: R/W
Reset value: 0x10
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	INT_TPULSE_DURATION	Interrupt pulse duration 0: Interrupt pulse duration is 100µs. Use only if ODR < 4kHz. (Default) 1: Interrupt pulse duration is 8 µs. Required if ODR ≥ 4kHz, optional for ODR < 4kHz.
5	INT_TDEASSERT_DISABLE	Interrupt de-assertion duration 0: The interrupt de-assertion duration is set to a minimum of 100µs. Use only if ODR < 4kHz. (Default) 1: Disables de-assert duration. Required if ODR ≥ 4kHz, optional for ODR < 4kHz.
4	INT_ASYNC_RESET	User should change setting to 0 from default setting of 1, for proper INT1 and INT2 pin operation
3:0	-	Reserved

14.51 INT_SOURCE0

Name: INT_SOURCE0
Address: 101 (65h)
Serial IF: R/W
Reset value: 0x10
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	UI_FSYNC_INT1_EN	0: UI FSYNC interrupt not routed to INT1 1: UI FSYNC interrupt routed to INT1
5	PLL_RDY_INT1_EN	0: PLL ready interrupt not routed to INT1 1: PLL ready interrupt routed to INT1
4	RESET_DONE_INT1_EN	0: Reset done interrupt not routed to INT1 1: Reset done interrupt routed to INT1
3	UI_DRDY_INT1_EN	0: UI data ready interrupt not routed to INT1 1: UI data ready interrupt routed to INT1
2	FIFO_THS_INT1_EN	0: FIFO threshold interrupt not routed to INT1 1: FIFO threshold interrupt routed to INT1
1	FIFO_FULL_INT1_EN	0: FIFO full interrupt not routed to INT1 1: FIFO full interrupt routed to INT1
0	UI_AGC_RDY_INT1_EN	0: UI AGC ready interrupt not routed to INT1 1: UI AGC ready interrupt routed to INT1

14.50 中断配置1_

名称: 中断_配置1
地址：100 (64h)
串行接口：读/写
复位值：0x10
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	中断脉冲持续时间_ _	中断脉冲持续时间 0: 中断脉冲持续时间为100微秒。仅当输出数据速率为< 4千赫时使用。（默认） 1: 中断脉冲持续时间为8微秒。当输出数据速率为≥ 4千赫时必须设置，输出数据速率为< 4千赫时可选。
5	INT_解除断言时间_禁用	中断解除断言持续时间 0: 中断解除断言持续时间设置为最小100微秒。仅当输出数据速率{v1}千赫时使用。（默认） 仅当ODR < 4千赫时使用。（默认设置） 1: 禁用解除断言持续时间。当ODR ≥ 4千赫时必须设置，对于ODR <4千赫可选。
4	INT异步复位_ _	用户应将默认设置从1更改为0，以确保INT1正常工作 和INT2引脚操作
3:0	-	保留

14.51 中断来源0_

名称：中断来源0_地址：
101（十六进制65）
串行接口：读/写
复位值：0x10
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	UI FSYNC INT1 使能 _ _ _	0: UI FSYNC中断未路由至INT1 1: UI FSYNC中断路由至INT1
5	PLL就绪中断INT1使能 _ _ _	0: PLL就绪中断未路由至INT1 1: PLL就绪中断路由至INT1
4	复位完成中断INT1使能 _ _ _	0: 复位完成中断未路由至INT1 1: 复位完成中断路由至INT1
3	UI数据就绪 INT1 使能 _ _ _	0: UI数据就绪中断未路由至INT1 1: UI数据就绪中断路由至INT1
2	FIFO阈值 INT1 使能 _ _ _	0: FIFO阈值中断未路由至INT1 1: FIFO阈值中断路由至INT1
1	FIFO满INT1使能 _ _ _	0: FIFO满中断未路由至INT1 1: FIFO满中断路由至INT1
0	UI AGC就绪INT1使能 _ _ _ _	0: UI AGC就绪中断未路由至INT1 1: UI AGC就绪中断路由至INT1

14.52 INT_SOURCE1

Name: INT_SOURCE1
Address: 102 (66h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	I3C_PROTOCOL_ERROR_INT1_EN	0: I3C^{SM} protocol error interrupt not routed to INT1 1: I3C^{SM} protocol error interrupt routed to INT1
5:4	-	Reserved
3	SMD_INT1_EN	0: SMD interrupt not routed to INT1 1: SMD interrupt routed to INT1
2	WOM_Z_INT1_EN	0: Z-axis WOM interrupt not routed to INT1 1: Z-axis WOM interrupt routed to INT1
1	WOM_Y_INT1_EN	0: Y-axis WOM interrupt not routed to INT1 1: Y-axis WOM interrupt routed to INT1
0	WOM_X_INT1_EN	0: X-axis WOM interrupt not routed to INT1 1: X-axis WOM interrupt routed to INT1

14.53 INT_SOURCE3

Name: INT_SOURCE3
Address: 104 (68h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	UI_FSYNC_INT2_EN	0: UI FSYNC interrupt not routed to INT2 1: UI FSYNC interrupt routed to INT2
5	PLL_RDY_INT2_EN	0: PLL ready interrupt not routed to INT2 1: PLL ready interrupt routed to INT2
4	RESET_DONE_INT2_EN	0: Reset done interrupt not routed to INT2 1: Reset done interrupt routed to INT2
3	UI_DRDY_INT2_EN	0: UI data ready interrupt not routed to INT2 1: UI data ready interrupt routed to INT2
2	FIFO_THS_INT2_EN	0: FIFO threshold interrupt not routed to INT2 1: FIFO threshold interrupt routed to INT2
1	FIFO_FULL_INT2_EN	0: FIFO full interrupt not routed to INT2 1: FIFO full interrupt routed to INT2
0	UI_AGC_RDY_INT2_EN	0: UI AGC ready interrupt not routed to INT2 1: UI AGC ready interrupt routed to INT2

14.52 中断 来源1_

名称: 中断 来源1_地
址: 102 (66h)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	I3C 协议错误 IN_ _ _ T1_EN	0: I3C^{SM} 协议错误中断未路由至INT1 1: I3C^{SM} 协议错误中断路由至INT1
5:4	-	保留
3	SMD INT1 使能 _ _	0: SMD中断未路由至INT1 1: SMD中断路由至INT1
2	陀螺仪Z轴中断1使能 _ _ _	0: Z轴WOM中断未路由至INT1 1: Z轴WOM中断路由至INT1
1	陀螺仪Y轴中断 使能 _ _ _	0: Y轴WOM中断未路由至INT1 1: Y轴WOM中断路由至INT1
0	陀螺仪X轴中断 使能 _ _ _	0: X轴WOM中断未路由至INT1 1: X轴WOM中断路由至INT1

14.53 INT SOURCE3_

名称：INT SOURCE3_
地址：104 (68h) 串行
接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	UI帧同步INT2使能 _ _ _	0: UI帧同步中断未路由至INT2 1: UI帧同步中断路由至INT2
5	锁相环就绪INT2使能 _ _ _	0: PLL就绪中断未路由至INT2 1: PLL就绪中断路由至INT2
4	复位完成INT2使能_ _ _	0: 复位完成中断未路由至INT2 1: 复位完成中断路由至INT2
3	UI数据就绪INT2使能 _ _ _	0: UI数据就绪中断未路由至INT2 1: UI数据就绪中断路由至INT2
2	FIFO阈值 INT2使能 _ _ _	0: FIFO阈值中断未路由至INT2 1: FIFO阈值中断路由至INT2
1	FIFO满 INT2使能 _ _ _	0: FIFO满中断未路由至INT2 1: FIFO满中断已路由至INT2
0	UI AGC就绪INT2使能 _ _ _ _	0: UI AGC就绪中断未路由至INT2 1: UI AGC就绪中断已路由至INT2

14.54 INT_SOURCE4

Name: INT_SOURCE4
Address: 105 (69h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	I3C_PROTOCOL_ERROR_INT2_EN	0: I3C^{SM} protocol error interrupt not routed to INT2 1: I3C^{SM} protocol error interrupt routed to INT2
5:4	-	Reserved
3	SMD_INT2_EN	0: SMD interrupt not routed to INT2 1: SMD interrupt routed to INT2
2	WOM_Z_INT2_EN	0: Z-axis WOM interrupt not routed to INT2 1: Z-axis WOM interrupt routed to INT2
1	WOM_Y_INT2_EN	0: Y-axis WOM interrupt not routed to INT2 1: Y-axis WOM interrupt routed to INT2
0	WOM_X_INT2_EN	0: X-axis WOM interrupt not routed to INT2 1: X-axis WOM interrupt routed to INT2

14.55 FIFO_LOST_PKT0

Name: FIFO_LOST_PKT0
Address: 108 (6Ch)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[7:0]	Low byte, number of packets lost in the FIFO

14.56 FIFO_LOST_PKT1

Name: FIFO_LOST_PKT1
Address: 109 (6Dh)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	FIFO_LOST_PKT_CNT[15:8]	High byte, number of packets lost in the FIFO

14.54 中断 来源4_

名称: 中断 来源4_
地址: 105 (69h)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6	I3C 协议错误 IN_ _ _ T2使能_	0: I3C^{SM} 协议错误中断未路由至INT2 1: I3C^{SM} 协议错误中断路由至INT2
5:4	-	保留
3	SMD INT2使能 _ _	0: SMD中断未路由至INT2 1: SMD中断路由至INT2
2	陀螺仪Z轴中断INT2使能 _ _ _	0: Z轴WOM中断未路由至INT2 1: Z轴WOM中断路由至INT2
1	陀螺仪Y轴中断INT2使能 _ _ _	0: Y轴WOM中断未路由至INT2 1: Y轴WOM中断路由至INT2
0	陀螺仪X轴中断INT2使能 _ _ _	0: X轴WOM中断未路由至INT2 1: X轴WOM中断路由至INT2

14.55 FIFO丢失数据包0_ _

名称: FIFO丢失_ _PKT0
地址：108 (6Ch)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	先进先出_丢失_数据包_计数[7:0]	低字节，FIFO中丢失的数据包数量

14.56 FIFO丢失数据包1_ _

名称：FIFO丢失数据包1_ _
地址：109 (6Dh)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	先进先出_丢失_数据包_计数[15:8]	高字节，FIFO中丢失的数据包数量

14.57 SELF_TEST_CONFIG

Name: SELF_TEST_CONFIG
Address: 112 (70h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6	ACCEL_ST_POWER	Set to 1 for accel self-test Otherwise set to 0; Set to 0 after self-test is completed
5	EN_AZ_ST	Enable Z-accel self-test
4	EN_AY_ST	Enable Y-accel self-test
3	EN_AX_ST	Enable X-accel self-test
2	EN_GZ_ST	Enable Z-gyro self-test
1	EN_GY_ST	Enable Y-gyro self-test
0	EN_GX_ST	Enable X-gyro self-test

14.58 WHO_AM_I

Name: WHO_AM_I
Address: 117 (75h)
Serial IF: R
Reset value: 0x47
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	WHOAMI	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x47. This is different from the I²C address of the device as seen on the slave I²C controller by the applications processor.

14.59 REG_BANK_SEL

Note: This register is accessible from all register banks

Name: REG_BANK_SEL
Address: 118 (76h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: ALL

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	BANK_SEL	Register bank selection 000: Bank 0 (default) 001: Bank 1 010: Bank 2 011: Bank 3 100: Bank 4 101: Reserved 110: Reserved 111: Reserved

14.57 自检配置_ _

名称: 自检配置_ _地
址: 112 (70h) 串行接口:
读/写 复位值：0x00 时
钟域：SCLK 用户界面_

BIT	NAME	功能
7	-	保留
6	加速度计自检电源_ _	设置为1以进行加速度计自检 否则设置为0；自检完成后设置为0
5	启用Z轴加速度计自检_ _	启用Z轴加速度计自检
4	使能Y轴自检_ _	启用Y轴加速度计自检
3	使能X轴自检_ _	启用X轴加速度计自检
2	使能Z轴陀螺仪自检_ _	启用Z轴陀螺仪自检
1	EN GY ST_ _	启用Y轴陀螺仪自检
0	EN GX ST_ _	启用X轴陀螺仪自检

14.58 我是谁_ _

名称：我是谁_ _地
址：117 (75h) 串行接
口：R 复位值：0x47
时钟域：SCLK
_UI

BIT	NAME	功能
7:0	我是谁	用于向用户指示当前访问设备的寄存器

描述：

该寄存器用于验证设备身份。WHOAMI的内容是一个8位设备ID。寄存器的默认值为0x47。这与应用处理器在从设备I²C控制器上看到的设备I²C地址不同。

14.59 寄存器组选择_ _

注意：该寄存器可从所有寄存器组访问

Name: REG_BANK_SEL
Address: 118 (76h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: ALL

BIT	NAME	功能
7:3	-	保留
2:0	BANK_SEL	寄存器组选择 000: 存储区0 (默认) 001: 存储区1 010: 存储区2 011: 存储区3 100: 存储区4 101: 保留 110: 保留 111: 保留

15 USER BANK 1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 1.

15.1 SENSOR_CONFIG0

Name: SENSOR_CONFIG0
Address: 03 (03h)
Serial IF: R/W
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	ZG_DISABLE	0: Z gyroscope is on 1: Z gyroscope is disabled
4	YG_DISABLE	0: Y gyroscope is on 1: Y gyroscope is disabled
3	XG_DISABLE	0: X gyroscope is on 1: X gyroscope is disabled
2	ZA_DISABLE	0: Z accelerometer is on 1: Z accelerometer is disabled
1	YA_DISABLE	0: Y accelerometer is on 1: Y accelerometer is disabled
0	XA_DISABLE	0: X accelerometer is on 1: X accelerometer is disabled

15.2 GYRO_CONFIG_STATIC2

Name: GYRO_CONFIG_STATIC2
Address: 11 (0Bh)
Serial IF: R/W
Reset value: 0xA0
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:2	-	Reserved
1	GYRO_AAF_DIS	0: Enable gyroscope anti-aliasing filter (default) 1: Disable gyroscope anti-aliasing filter
0	GYRO_NF_DIS	0: Enable Notch Filter (default) 1: Disable Notch Filter

15.3 GYRO_CONFIG_STATIC3

Name: GYRO_CONFIG_STATIC3
Address: 12 (0Ch)
Serial IF: R/W
Reset value: 0x0D
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	GYRO_AAF_DELT	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

15 用户银行1寄存器映射 – 描述

本节描述USR存储区1内每个寄存器的功能与内容。

15.1 传感器配置0_

名称: 传感器配置0_地
址: 03 (03h) 串行接口:
读/写 复位值：0x80
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	Z轴陀螺仪 禁用_	0: Z轴陀螺仪开启 1: Z轴陀螺仪禁用
4	Y轴陀螺仪 禁用_	0: Y轴陀螺仪开启 1: Y轴陀螺仪禁用
3	XG 禁用_	0: X轴陀螺仪开启 1: X轴陀螺仪禁用
2	ZA 禁用_	0: Z轴加速度计开启 1: Z轴加速度计禁用
1	YA 禁用_	0: Y轴加速度计开启 1: Y轴加速度计禁用
0	XA禁用_	0: X轴加速度计已开启 1: X轴加速度计已禁用

15.2 陀螺配置静态2_ _

名称：陀螺配置静态2_ _
地址：11 (0Bh) 串行接口：读/
写 复位值：0xA0 时钟域：
SCLK
_UI

BIT	NAME	功能
7:2	-	保留
1	陀螺仪抗混叠滤波器 禁用_ _	0: 启用陀螺仪抗混叠滤波器（默认） 1: 禁用陀螺仪抗混叠滤波器
0	陀螺仪陷波滤波器 禁用_ _	0: 启用陷波滤波器（默认） 1: 禁用陷波滤波器

15.3 陀螺配置静态3_ _

名称：陀螺配置静态3_ _地
址：12 (0Ch) 串行接口：读/写

复位值：0x0D
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5:0	陀螺抗混叠滤波器 DELT_ _	控制陀螺仪抗混滤波器的带宽 详见章节5.2

15.4 GYRO_CONFIG_STATIC4

Name: GYRO_CONFIG_STATIC4
Address: 13 (0Dh)
Serial IF: R/W
Reset value: 0xAA
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_AAF_DELTSQR[7:0]	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

15.5 GYRO_CONFIG_STATIC5

Name: GYRO_CONFIG_STATIC5
Address: 14 (0Eh)
Serial IF: R/W
Reset value: 0x80
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	GYRO_AAF_BITSHIFT	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details
3:0	GYRO_AAF_DELTSQR[11:8]	Controls bandwidth of the gyroscope anti-alias filter See section 5.2 for details

15.6 GYRO_CONFIG_STATIC6

Name: GYRO_CONFIG_STATIC6
Address: 15 (0Fh)
Serial IF: R/W
Reset value: 0xXX (Factory trimmed on an individual device basis)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_X_NF_COSWZ[7:0]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details

15.7 GYRO_CONFIG_STATIC7

Name: GYRO_CONFIG_STATIC7
Address: 16 (10h)
Serial IF: R/W
Reset value: 0xXX (Factory trimmed on an individual device basis)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_Y_NF_COSWZ[7:0]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details

15.4 陀螺配置静态4_ _

Name: GYRO_CONFIG_STATIC4
Address: 13 (0Dh)
串行接口：读/写
复位值: 0xAA
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_抗混叠滤波器_增量平方[7:0]	控制陀螺仪抗混滤波器的带宽 详见章节5.2

15.5 陀螺仪配置静态5_ _

名称：陀螺仪配置静态5_ _
地址：14（0Eh） 串行接口：读/
写
复位值：0x80
时钟域：SCLK _UI

BIT	NAME	功能
7:4	陀螺AAF位偏移_ _	控制陀螺仪抗混滤波器的带宽 详见章节5.2
3:0	陀螺_抗混_增量平方[11:8]	控制陀螺仪抗混滤波器的带宽 详见第5.2节

15.6 陀螺仪配置静态6_ _

Name: GYRO_CONFIG_STATIC6
Address: 15 (0Fh)
串行接口：读/写
复位值：0xXX (根据单个设备出厂校准)
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_X轴_陷波滤波器_COSWZ[7:0]	用于陀螺仪X轴陷波滤波器频率选择 详情参见第5.1节

15.7 陀螺仪配置静态7_ _

Name: GYRO_CONFIG_STATIC7
Address: 16 (10h)
(_串行接口：
读/写
复位值：0xXX (根据单个设备出厂校准)
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_Y_陷波滤波器_COSWZ[7:0]	用于陀螺仪Y轴陷波滤波器频率选择 详情参见第5.1节

15.8 GYRO_CONFIG_STATIC8

Name: GYRO_CONFIG_STATIC8
Address: 17 (11h)
Serial IF: R/W
Reset value: 0xXX (Factory trimmed on an individual device basis)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_Z_NF_COSWZ[7:0]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details

15.9 GYRO_CONFIG_STATIC9

Name: GYRO_CONFIG_STATIC9
Address: 18 (12h)
Serial IF: R/W
Reset value: 0xXX (Factory trimmed on an individual device basis)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	GYRO_Z_NF_COSWZ_SEL[0]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details
4	GYRO_Y_NF_COSWZ_SEL[0]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details
3	GYRO_X_NF_COSWZ_SEL[0]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details
2	GYRO_Z_NF_COSWZ[8]	Used for gyroscope Z-axis notch filter frequency selection See section 5.1 for details
1	GYRO_Y_NF_COSWZ[8]	Used for gyroscope Y-axis notch filter frequency selection See section 5.1 for details
0	GYRO_X_NF_COSWZ[8]	Used for gyroscope X-axis notch filter frequency selection See section 5.1 for details

15.10 GYRO_CONFIG_STATIC10

Name: GYRO_CONFIG_STATIC10
Address: 19 (13h)
Serial IF: R/W
Reset value: 0x11
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6:4	GYRO_NF_BW_SEL	Selects bandwidth for gyroscope notch filter See section 5.1 for details
3:0	-	Reserved

15.8 陀螺仪配置静态8_ _

名称: 陀螺仪 _配置 _静态8
地址：17 (11h)
串行接口：读/写
复位值：0xXX (根据单个设备出厂校准)
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_Z轴_陷波滤波器_COSWZ[7:0]	用于陀螺仪Z轴陷波滤波器频率选择 详见第5.1节

15.9 陀螺配置静态9_ _

名称：陀螺配置静态9_ _地
址：18 (12h) 串行接口：读/写

复位值：0xXX (根据单个设备出厂校准)
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	陀螺仪_Z轴_陷波滤波器_COSWZ_选择[0]	用于陀螺仪Z轴陷波滤波器频率选择 详情参见第5.1节
4	陀螺仪_Y轴_陷波滤波器_COSWZ_选择[0]	用于陀螺仪Y轴陷波滤波器频率选择 详情参见第5.1节
3	陀螺仪_X轴_女_一氧化碳SWZ_选择[0]	用于陀螺仪X轴陷波滤波器频率选择 详情参见第5.1节
2	陀螺仪_Z轴_女_一氧化碳SWZ轴[8]	用于陀螺仪Z轴陷波滤波器频率选择 详情参见第5.1节
1	陀螺仪_Y轴_女_一氧化碳SWZ轴[8]	用于陀螺仪Y轴陷波滤波器频率选择，详情参见第5.1节
0	陀螺仪_X轴_女_一氧化碳SWZ[8]	用于陀螺仪X轴陷波滤波器频率选择，详情参见第5.1节

15.10 陀螺仪配置 STATIC10_ _

名称：陀螺仪配置 STATIC10
_ _地址：19 (13h) 串行接口：
读/写
复位值：0x11
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6:4	陀螺仪陷波滤波器带宽选择_ _ _	选择陀螺仪陷波滤波器的带宽，详情参见第5.1节
3:0	-	保留

15.11 XG_ST_DATA

Name: XG_ST_DATA
Address: 95 (5Fh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	XG_ST_DATA	X-gyro self-test data

15.12 YG_ST_DATA

Name: YG_ST_DATA
Address: 96 (60h)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	YG_ST_DATA	Y-gyro self-test data

15.13 ZG_ST_DATA

Name: ZG_ST_DATA
Address: 97 (61h)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ZG_ST_DATA	Z-gyro self-test data

15.14 TMSTVAL0

Name: TMSTVAL0
Address: 98 (62h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	TMST_VALUE[7:0]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

15.11 XG ST 数据_ _

Name: XG_ST_DATA
Address: 95 (5Fh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
时钟域：SCLK _UI

BIT	NAME	功能
7:0	XG ST 数据_ _	X轴陀螺自检数据

15.12 YG ST 数据_ _

Name: YG_ST_DATA
Address: 96 (60h)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
(时钟域：SCLK _UI

BIT	NAME	功能
7:0	YG_ST_DATA	Y轴陀螺仪自检数据

15.13 Z轴陀螺仪 自检 数据

_ _

Name: ZG_ST_DATA
Address: 97 (61h)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
时钟域：SCLK _UI

BIT	NAME	功能
7:0	Z轴陀螺仪 自检 数据_ _	Z轴陀螺自检数据

15.14 时间戳值0

名称：TMSTVAL0
地址：98 (62h) 串行
接口：R 复位值：
0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	TMST_值[7:0]	当TMST_STROBE被编程时，内部计数器的当前值被锁存到此寄存器。允许读取时间戳的完整20位精度。

15.15 TMSTVAL1

Name: TMSTVAL1
Address: 99 (63h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	TMST_VALUE[15:8]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

15.16 TMSTVAL2

Name: TMSTVAL2
Address: 100 (64h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	TMST_VALUE[19:16]	When TMST_STROBE is programmed, the current value of the internal counter is latched to this register. Allows the full 20-bit precision of the time stamp to be read back.

15.17 INTF_CONFIG4

Name: INTF_CONFIG4
Address: 122 (7Ah)
Serial IF: R/W
Reset value: 0x83
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:2	-	Reserved
6	I3C_BUS_MODE	0: Device is on a bus with I^2C and $I3C^{SM}$ devices 1: Device is on a bus with $I3C^{SM}$ devices only
5:2	-	Reserved
1	SPI_AP_4WIRE	0: AP interface uses 3-wire SPI mode 1: AP interface uses 4-wire SPI mode (default)
0	-	Reserved

15.15 时间戳值1

名称: 时间戳值1
地址: 99 (63h)
串行接口：R
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	时间戳_值[15:8]	当TMST_STROBE被编程时，内部计数器的当前值被锁存到此寄存器中。允许读取时间戳的全部20位精度。

15.16 时间戳值2

名称：时间戳值2
地址：100 (64h)
串行接口：读
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:4	-	保留
3:0	时间戳_值[19:16]	当 TMST_STROBE 被编程时，内部计数器的当前值将被锁存到此寄存器。允许读取时间戳的完整20位精度。

15.17 INTF 配置4_

名称: INTF 配置4_
地址：122 (7Ah)
串行接口：读/写
复位值：0x83
时钟域：SCLK _UI

BIT	NAME	功能
7:2	-	保留
6	I3C总线模式_ _	0: 设备位于支持I^2C和$I3C^{SM}$ 设备的总线 1: 设备位于仅支持$I3C^{SM}$ 设备的总线
5:2	-	保留
1	SPI AP 4线_ _	0: AP接口使用3线SPI模式 1: AP接口使用4线SPI模式（默认）
0	-	保留

15.18 INTF_CONFIG5

Name: INTF_CONFIG5
Address: 123 (7Bh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:3	-	Reserved
2:1	PIN9_FUNCTION	Selects among the following functionalities for pin 9 00: INT2 01: FSYNC 10: CLKIN 11: Reserved
0	-	Reserved

15.19 INTF_CONFIG6

Name: INTF_CONFIG6
Address: 124 (7Ch)
Serial IF: R/W
Reset value: 0x5F
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	ASYNCTIME0_DIS	0: I3C^{SM}Asynchronous Mode 0 timing control is enabled 1: I3C^{SM} Asynchronous Mode 0 timing control is disabled
6:5	-	Reserved
4	I3C_EN	0: I3C^{SM} slave not enabled 1: I3C^{SM} slave enabled
3	I3C_IBI_BYTE_EN	0: I3C^{SM} IBI payload function not enabled 1: I3C^{SM} IBI payload function enabled
2	I3C_IBI_EN	0: I3C^{SM} IBI function not enabled 1: I3C^{SM} IBI function enabled
1	I3C_DDR_EN	0: I3C^{SM} DDR mode not enabled 1: I3C^{SM} DDR mode enabled
0	I3C_SDR_EN	0: I3C^{SM} SDR mode not enabled 1: I3C^{SM} SDR mode enabled

15.18 INTF 配置5_

名称: INTF _配置5
地址：123 (7Bh)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:3	-	保留
2:1	引脚9功能_	为引脚9选择以下功能之一 00: INT2 01: 帧同步 10: 时钟输入 11: 保留
0	-	保留

15.19 接口配置6_

名称：接口配置6_地
址：124 (7Ch)
串行接口：读/写
复位值：0x5F
时钟域：SCLK _UI

BIT	NAME	功能
7	异步时间0禁用_	0: I3C^{SM}异步模式0时序控制已启用 1: I3C^{SM} 异步模式0时序控制已禁用
6:5	-	保留
4	I3C使能_	0: I3C^{SM} 从设备未启用 1: I3C^{SM} 从设备已启用
3	I3C IBI 字节 使能 _ _ _	0: I3C^{SM} IBI 负载功能未启用 1: I3C^{SM} IBI 负载功能已启用
2	I3C IBI 使能 _ _	0: I3C^{SM} IBI 功能未启用 1: I3C^{SM} IBI 功能已启用
1	I3C DDR 使能 _ _	0: I3C^{SM} DDR模式未启用 1: I3C^{SM} DDR模式已启用
0	I3C SDR 使能 _ _	0: I3C^{SM} SDR模式未启用 1: I3C^{SM} SDR模式启用

16 USER BANK 2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 2.

16.1 ACCEL_CONFIG_STATIC2

Name: ACCEL_CONFIG_STATIC2
Address: 03 (03h)
Serial IF: R/W
Reset value: 0x30
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6:1	ACCEL_AAF_DELT	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details
0	ACCEL_AAF_DIS	0: Enable accelerometer anti-aliasing filter (default) 1: Disable accelerometer anti-aliasing filter

16.2 ACCEL_CONFIG_STATIC3

Name: ACCEL_CONFIG_STATIC3
Address: 04 (04h)
Serial IF: R/W
Reset value: 0x40
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_AAF_DELTSQR[7:0]	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details

16.3 ACCEL_CONFIG_STATIC4

Name: ACCEL_CONFIG_STATIC4
Address: 05 (05h)
Serial IF: R/W
Reset value: 0x62
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_AAF_BITSHIFT	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details
3:0	ACCEL_AAF_DELTSQR[11:8]	Controls bandwidth of the accelerometer anti-alias filter See section 5.2 for details

16.4 XA_ST_DATA

Name: XA_ST_DATA
Address: 59 (3Bh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	XA_ST_DATA	X-accel self-test data

16 用户库2寄存器映射 – 描述

本节描述USR Bank 2中每个寄存器的功能和内容。

16.1 加速度配置静态2_ _

名称：加速度配置静态2_ _
地址：03 (03h) 串行接口：读/写

复位值：0x30
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6:1	加速度AAF增量_ _	控制加速度计抗混叠滤波器的带宽 详见章节5.2
0	加速度AAF禁用_ _	0：启用加速度计抗混叠滤波器（默认） 1：禁用加速度计抗混叠滤波器

16.2 加速度配置静态3_ _

名称：加速度配置静态3
_ _地址：04 (04h) 串行接口：读/写 复位值：0x40 时钟域：SCLK
_UI

BIT	NAME	功能
7:0	加速度计_抗混叠滤波器_增量平方[7:0]	控制加速度计抗混叠滤波器的带宽 详见第5.2节

16.3 加速度计配置静态4_ _

名称：加速度计配置静态4
_ _地址：05 (05h) 串行接口：读/写
复位值：0x62
时钟域：SCLK _UI

BIT	NAME	功能
7:4	加速度计抗混叠滤波器位移位 _ _	控制加速度计抗混叠滤波器的带宽 详见章节5.2
3:0	加速度计_抗混叠滤波器_增量平方[11:8]	控制加速度计抗混叠滤波器的带宽 详见章节5.2

16.4 X轴加速度自检数据

_ _

Name: XA_ST_DATA
Address: 59 (3Bh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	功能
7:0	X轴加速度自检数据_ _	X轴加速度自检数据

16.5 YA_ST_DATA

Name: YA_ST_DATA
Address: 60 (3Ch)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	YA_ST_DATA	Y-accel self-test data

16.6 ZA_ST_DATA

Name: ZA_ST_DATA
Address: 61 (3Dh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ZA_ST_DATA	Z-accel self-test data

16.5 Y轴 自检 数据_ _

Name: YA_ST_DATA
Address: 60 (3Ch)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
时钟域：SCLK _UI

BIT	NAME	功能
7:0	Y轴自检数据_ _	Y轴加速度自测数据

16.6 Z轴自检数据_ _

Name: ZA_ST_DATA
Address: 61 (3Dh)
Serial IF: R/W
Reset value: 0xXX (The value in this register indicates the self-test output generated during manufacturing tests)
时钟域：SCLK_UI

BIT	NAME	功能
7:0	ZA_ST_DATA	Z轴加速度自检数据

17 USER BANK 3 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 3.

17.1 CLKDIV

Name: CLKDIV Address: 42 (2Ah) Serial IF: R Reset value: 0xXX (Factory trimmed on an individual device basis) Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7	-	Reserved
6:0	CLKDIV	Clock divider value for Notch filter operation

17 用户组3寄存器映射 – 描述

本节描述USR存储区3中每个寄存器的功能和内容。

17.1 时钟分频器

名称: 时钟分频器 地址：42 (2Ah) 串行接口：R 复位值：0xXX (根据单个设备出厂校准) 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7	-	保留
6:0	时钟分频器	陷波滤波器操作的时钟分频值

18 USER BANK 4 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within USR Bank 4.

18.1 APEX_CONFIG1

Name: APEX_CONFIG1
Address: 64 (40h)
Serial IF: R/W
Reset value: 0xA2
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	LOW_ENERGY_AMP_TH_SEL	Pedometer Low Energy mode amplitude threshold selection Use default value 1010b
3:0	DMP_POWER_SAVE_TIME_SEL	When the DMP is in power save mode, it is awakened by the WOM and will wait for a certain duration before going back to sleep. This bitfield configures this duration. 0000: 0 seconds 0001: 4 seconds 0010: 8 seconds 0011: 12 seconds 0100: 16 seconds 0101: 20 seconds 0110: 24 seconds 0111: 28 seconds 1000: 32 seconds 1001: 36 seconds 1010: 40 seconds 1011: 44 seconds 1100: 48 seconds 1101: 52 seconds 1110: 56 seconds 1111: 60 seconds

18 用户库4寄存器映射 – 描述

本节描述USR存储区4中每个寄存器的功能和内容。

18.1 APEX 配置1_

名称: APEX 配置1_地址:
64 (40h) 串行接口：读/
写
复位值：0xA2
时钟域：SCLK _UI

BIT	NAME	功能
7:4	低功耗放大器推力选择 _ _ _ _	计步器低功耗模式幅度阈值选择 使用默认值1010b
3:0	DMP省电模式时间S_ _ _ _ EL	当DMP处于省电模式时，它会被WOM唤醒，并 在返回睡眠状态前等待一定持续时间。此位域用于配置该持续时 间。 0000：0秒 0001：4秒 0010：8秒 0011: 12秒 0100: 16秒 0101: 20秒 0110: 24秒 0111: 28秒 1000: 32秒 1001: 36秒 1010: 40秒 1011: 44秒 1100: 48秒 1101: 52秒 1110: 56秒 1111: 60秒

18.2 APEX_CONFIG2

Name: APEX_CONFIG2
Address: 65 (41h)
Serial IF: R/W
Reset value: 0x85
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	PED_AMP_TH_SEL	Pedometer amplitude threshold selection Use default value 1000b
3:0	PED_STEP_CNT_TH_SEL	Pedometer step count detection window Use default value 0101b 0000: 0 steps 0001: 1 step 0010: 2 steps 0011: 3 steps 0100: 4 steps 0101: 5 steps (default) 0110: 6 steps 0111: 7 steps 1000: 8 steps 1001: 9 steps 1010: 10 steps 1011: 11 steps 1100: 12 steps 1101: 13 steps 1110: 14 steps 1111: 15 steps

18.2 APEX 配置2_

名称: APEX 配置2_
地址: 65 (41h)
串行接口：读/写
复位值：0x85
时钟域：SCLK _UI

BIT	NAME	功能
7:4	PED 放大器 阈值 选择 _ _ _	计步器幅度阈值选择 使用默认值 1000b
3:0	计步器步数检测窗口 _ _ _ _	计步器步数检测窗口 使用默认值 0101b 0000: 0步 0001: 1步 0010: 2步 0011: 3步 0100: 4步 0101: 5步 (默认) 0110: 6步 0111: 7步 1000: 8步 1001: 9步 1010: 10步 1011: 11步 1100: 12步 1101: 13步 1110: 14步 1111: 15步

18.3 APEX_CONFIG3

Name: APEX_CONFIG3
Address: 66 (42h)
Serial IF: R/W
Reset value: 0x51
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:5	PED_STEP_DET_TH_SEL	Pedometer step detection threshold selection Use default value 010b 000: 0 steps 001: 1 step 010: 2 steps (default) 011: 3 steps 100: 4 steps 101: 5 steps 110: 6 steps 111: 7 steps
4:2	PED_SB_TIMER_TH_SEL	Pedometer step buffer timer threshold selection Use default value 100b 000: 0 samples 001: 1 sample 010: 2 samples 011: 3 samples 100: 4 samples (default) 101: 5 samples 110: 6 samples 111: 7 samples
1:0	PED_HI_EN_TH_SEL	Pedometer high energy threshold selection Use default value 01b

18.3 APEX配置3_

名称: APEX配置3_
地址: 66 (42h)
串行接口：读/写
复位值：0x51
时钟域：SCLK _UI

BIT	NAME	功能
7:5	计步器步数检测阈值选择 _ _ _ _	计步器步数检测阈值选择 使用默认值010b 000: 0步 001: 1步 010: 2步 (默认) 011: 3步 100: 4步 101: 5步 110: 6步 111: 7步
4:2	PED SB TIMER TH SEL _ _ _ _	计步器步数缓冲定时器阈值选择 使用默认值100二进制 000: 0样本 001: 1样本 010: 2 样本 011: 3 样本 100: 4 样本 (默认) 101: 5 样本 110: 6 样本 111: 7 样本
1:0	PED 高 使能 阈值 选择 _ _ _ _	计步器高能量阈值选择 使用默认值01二进制

18.4 APEX_CONFIG4

Name: APEX_CONFIG4
Address: 67 (43h)
Serial IF: R/W
Reset value: 0xA4
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	TILT_WAIT_TIME_SEL	Configures duration of delay after tilt is detected before interrupt is triggered 00: 0s 01: 2s 10: 4s (default) 11: 6s
5:3	SLEEP_TIME_OUT	Configures the time out for sleep detection, for Raise to Wake/Sleep feature 000: 1.28sec 001: 2.56sec 010: 3.84sec 011: 5.12sec 100: 6.40sec 101: 7.68sec 110: 8.96sec 111: 10.24sec
2:0	-	Reserved

18.5 APEX_CONFIG5

Name: APEX_CONFIG5
Address: 68 (44h)
Serial IF: R/W
Reset value: 0x8C
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	MOUNTING_MATRIX	Defines mounting matrix, chip to device frame 000: [1 0 0; 0 1 0; 0 0 1] 001: [1 0 0; 0 -1 0; 0 0 -1] 010: [-1 0 0; 0 1 0; 0 0 -1] 011: [-1 0 0; 0 -1 0; 0 0 1] 100: [0 1 0; 1 0 0; 0 0 -1] 101: [0 1 0; -1 0 0; 0 0 1] 110: [0 -1 0; 1 0 0; 0 0 1] 111: [0 -1 0; -1 0 0; 0 0 -1]

18.4 APEX配置4_

名称: APEX配置4_
地址: 67 (43h)
串行接口：读/写
复位值：0xA4
时钟域：SCLK _UI

BIT	NAME	功能
7:6	倾斜等待时间选择 _ _ _	配置检测到倾斜后触发中断前的延迟时间 00: 0秒 01: 2秒 10: 4秒 (默认) 11: 6秒
5:3	睡眠超时_ _	配置睡眠检测的超时时间，用于抬手唤醒/睡眠功能 000: 1.28秒 001: 2.56秒 010: 3.84秒 011: 5.12秒 100: 6.40秒 101: 7.68秒 110: 8.96秒 111: 10.24秒
2:0	-	保留

18.5 APEX配置5_

Name: APEX_CONFIG5
Address: 68 (44h)
串行接口：读/写
复位值：0x8C
时钟域：SCLK _UI

BIT	NAME	功能
7:3	-	保留
2:0	安装矩阵_	定义安装矩阵，芯片到设备框架 000: [1 0 0; 0 1 0; 0 0 1] 001: [1 0 0; 0 -1 0; 0 0 -1] 010：[-1 0 0；0 1 0；0 0 -1] 011：[-1 0 0；0 -1 0；0 0 1] 100: [0 1 0; 1 0 0; 0 0 -1] 101: [0 1 0; -1 0 0; 0 0 1] 110: [0 -1 0; 1 0 0; 0 0 1] 111: [0 -1 0; -1 0 0; 0 0 -1]

18.6 APEX_CONFIG6

Name: APEX_CONFIG6
Address: 69 (45h)
Serial IF: R/W
Reset value: 0x5C
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	SLEEP_GESTURE_DELAY	Configures detection window for sleep gesture detection 000: 0.32sec 001: 0.64sec 010: 0.96sec 011: 1.28sec 100: 1.60sec 101: 1.92sec 110: 2.24sec 111: 2.56sec

18.7 APEX_CONFIG7

Name: APEX_CONFIG7
Address: 70 (46h)
Serial IF: R/W
Reset value: 0x45
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:2	TAP_MIN_JERK_THR	Tap Detection minimum jerk threshold Use default value 010001b
1:0	TAP_MAX_PEAK_TOL	Tap Detection maximum peak tolerance Use default value 01b

18.8 APEX_CONFIG8

Name: APEX_CONFIG8
Address: 71 (47h)
Serial IF: R/W
Reset value: 0x5B
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7	-	Reserved
6:5	TAP_TMAX	Tap measurement window (number of samples) Use default value 01b
4:3	TAP_TAVG	Tap energy measurement window (number of samples) Use default value 01b
2:0	TAP_TMIN	Single tap window (number of samples) Use default value 011b

18.6 顶点配置6_

名称: 顶点 _CONFIG6
地址：69 (45h)
串行接口：读/写
复位值：0x5C
时钟域：SCLK _UI

BIT	NAME	功能
7:3	-	保留
2:0	睡眠 _手势 _延迟	配置睡眠手势检测的检测窗口 000: 0.32秒 001: 0.64秒 010: 0.96秒 011: 1.28秒 100: 1.60秒 101: 1.92秒 110: 2.24秒 111: 2.56秒

18.7 顶点配置7_

名称：顶点配置7_
地址：70 (46h)
串行接口：读/写
复位值：0x45
时钟域：SCLK _UI

BIT	NAME	功能
7:2	点击最小急动阈值 _ _ _	点击检测最小急动阈值 使用默认值010001b
1:0	点击最大峰值容差 _ _ _	点击检测最大峰值容差 使用默认值01b

18.8 顶点配置8_

名称: 顶点配置8_
地址: 71 (47h)
串行接口：读/写
复位值: 0x5B
时钟域：SCLK _UI

BIT	NAME	功能
7	-	保留
6:5	轻敲 TMAX_	抽头测量窗口（样本数量）使用默认值01二进制
4:3	轻敲 TAVG_	轻触能量测量窗口（样本数量） 使用默认值01二进制
2:0	轻敲 TMIN_	单次轻触窗口（样本数量） 使用默认值011b

18.9 APEX_CONFIG9

Name: APEX_CONFIG9
Address: 72 (48h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:1	-	Reserved
0	SENSITIVITY_MODE	0: Low power mode at accelerometer ODR 25Hz; High performance mode at accelerometer ODR ≥ 50Hz 1: Low power and slow walk mode at accelerometer ODR 25Hz; Slow walk mode at accelerometer ODR ≥ 50Hz

18.10 ACCEL_WOM_X_THR

Name: ACCEL_WOM_X_THR
Address: 74 (4Ah)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	WOM_X_TH	Threshold value for the Wake on Motion Interrupt for X-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256=~3.9mg

18.11 ACCEL_WOM_Y_THR

Name: ACCEL_WOM_Y_THR
Address: 75 (4Bh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	WOM_Y_TH	Threshold value for the Wake on Motion Interrupt for Y-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256=~3.9mg

18.12 ACCEL_WOM_Z_THR

Name: ACCEL_WOM_Z_THR
Address: 76 (4Ch)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	WOM_Z_TH	Threshold value for the Wake on Motion Interrupt for Z-axis accelerometer WoM thresholds are expressed in fixed “mg” independent of the selected Range [0g : 1g]; Resolution 1g/256=~3.9mg

18.9 APEX配置9_

Name: APEX_CONFIG9
Address: 72 (48h)
Serial IF: R/W
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:1	-	保留
0	灵敏度模式_	0: 低功耗模式，加速度计输出数据率25Hz；高性能模式，加速度计输出数据率≥ 50Hz 1: 低功耗与慢走模式，加速度计输出数据率25Hz；慢走模式，加速度计输出数据率≥ 50Hz

18.10 加速度计 WOM X轴 阈值

_ _ _

名称：加速度计 WOM X轴 阈值_ _ _地址：74 (4Ah) 串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	WOM X轴 阈值_ _	X轴加速度计的运动唤醒中断阈值，WoM阈值以固定的“毫克”表示，与所选量程[0g无关：1g]；分辨率1g/256=~3.9mg

18.11 加速度计WOM Y轴阈值

_ _ _

名称：ACCEL WOM Y THR
_ _ _地址：75 (4Bh) 串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	WOM Y 阈值_ _	Y轴加速度计运动唤醒中断的阈值，唤醒运动阈值以固定的“毫克”表示，与所选范围无关 [0g：1g]；分辨率 1g/256=~3.9mg

18.12 加速度计 WOM Z 阈值_ _ _

名称：加速度计 WOM Z 阈值
_ _ _地址：76 (4Ch) 串行接口：读/写 复位值：0x00 时钟域：SCLK _UI

BIT	NAME	功能
7:0	WOM Z 阈值_ _	Z轴加速度计运动唤醒中断的阈值唤醒运动阈值以固定的“毫克”表示，与所选量程[0g无关：1g]；分辨率1g/256=~3.9毫克

18.13 INT_SOURCE6

Name: INT_SOURCE6
Address: 77 (4Dh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_INT1_EN	0: Step detect interrupt not routed to INT1 1: Step detect interrupt routed to INT1
4	STEP_CNT_OFL_INT1_EN	0: Step count overflow interrupt not routed to INT1 1: Step count overflow interrupt routed to INT1
3	TILT_DET_INT1_EN	0: Tilt detect interrupt not routed to INT1 1: Tile detect interrupt routed to INT1
2	WAKE_DET_INT1_EN	0: Wake detect interrupt not routed to INT1 1: Wake detect interrupt routed to INT1
1	SLEEP_DET_INT1_EN	0: Sleep detect interrupt not routed to INT1 1: Sleep detect interrupt routed to INT1
0	TAP_DET_INT1_EN	0: Tap detect interrupt not routed to INT1 1: Tap detect interrupt routed to INT1

18.14 INT_SOURCE7

Name: INT_SOURCE7
Address: 78 (4Eh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_INT2_EN	0: Step detect interrupt not routed to INT2 1: Step detect interrupt routed to INT2
4	STEP_CNT_OFL_INT2_EN	0: Step count overflow interrupt not routed to INT2 1: Step count overflow interrupt routed to INT2
3	TILT_DET_INT2_EN	0: Tilt detect interrupt not routed to INT2 1: Tile detect interrupt routed to INT2
2	WAKE_DET_INT2_EN	0: Wake detect interrupt not routed to INT2 1: Wake detect interrupt routed to INT2
1	SLEEP_DET_INT2_EN	0: Sleep detect interrupt not routed to INT2 1: Sleep detect interrupt routed to INT2
0	TAP_DET_INT2_EN	0: Tap detect interrupt not routed to INT2 1: Tap detect interrupt routed to INT2

18.13 中断 来源6_

名称: 中断 来源6_
地址：77（4Dh）
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	步进 检测 INT1 使能 _ _ _	0: 步进检测中断未路由至INT1 1: 步进检测中断路由至INT1
4	步进计数溢出中断1使能 _ _ _ _	0: 步进计数溢出中断未路由至INT1 1: 步进计数溢出中断路由至INT1
3	倾斜检测中断1使能 _ _ _	0: 倾斜检测中断未路由至INT1 1: 平铺检测中断已路由至INT1
2	唤醒检测INT1使能 _ _ _	0: 唤醒检测中断未路由至INT1 1: 唤醒检测中断已路由至INT1
1	睡眠检测INT1使能 _ _ _	0: 睡眠检测中断未路由至INT1 1: 睡眠检测中断路由至INT1
0	点击检测中断1使能 _ _ _	0: 轻击检测中断未路由至INT1 1: 轻击检测中断路由至INT1

18.14 中断源7_

名称：中断源7_地
址：78 (4Eh)
串行接口：读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	步进检测中断路由至INT2使能_ _ _	0: 步进检测中断未路由至INT2 1: 步进检测中断路由至INT2
4	步进计数溢出中断2使能 _ _ _ _	0: 步进计数溢出中断未路由至INT2 1: 步进计数溢出中断路由至INT2
3	倾斜检测INT2使能 _ _ _	0: 倾斜检测中断未路由至INT2 1: 平铺检测中断路由至INT2
2	唤醒检测INT2使能 _ _ _	0: 唤醒检测中断未路由至INT2 1: 唤醒检测中断路由至INT2
1	睡眠检测中断INT2使能 _ _ _	0：睡眠检测中断未路由至INT2 1：睡眠检测中断路由至INT2
0	点击检测中断INT2使能 _ _ _	0：轻击检测中断未路由至INT2 1：轻击检测中断路由至INT2

18.15 INT_SOURCE8

Name: INT_SOURCE8 Address: 79 (4Fh) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7:6	-	Reserved
5	FSYNC_IBI_EN	0: FSYNC interrupt not routed to IBI 1: FSYNC interrupt routed to IBI
4	PLL_RDY_IBI_EN	0: PLL ready interrupt not routed to IBI 1: PLL ready interrupt routed to IBI
3	UI_DRDY_IBI_EN	0: UI data ready interrupt not routed to IBI 1: UI data ready interrupt routed to IBI
2	FIFO_THS_IBI_EN	0: FIFO threshold interrupt not routed to IBI 1: FIFO threshold interrupt routed to IBI
1	FIFO_FULL_IBI_EN	0: FIFO full interrupt not routed to IBI 1: FIFO full interrupt routed to IBI
0	AGC_RDY_IBI_EN	0: AGC ready interrupt not routed to IBI 1: AGC ready interrupt routed to IBI

18.16 INT_SOURCE9

Name: INT_SOURCE9 Address: 80 (50h) Serial IF: R/W Reset value: 0x00 Clock Domain: SCLK_UI		
BIT	**NAME**	**FUNCTION**
7	I3C_PROTOCOL_ERROR_IBI_EN	0: I3C^{SM} protocol error interrupt not routed to IBI 1: I3C^{SM} protocol error interrupt routed to IBI
6:5	-	Reserved
4	SMD_IBI_EN	0: SMD interrupt not routed to IBI 1: SMD interrupt routed to IBI
3	WOM_Z_IBI_EN	0: Z-axis WOM interrupt not routed to IBI 1: Z-axis WOM interrupt routed to IBI
2	WOM_Y_IBI_EN	0: Y-axis WOM interrupt not routed to IBI 1: Y-axis WOM interrupt routed to IBI
1	WOM_X_IBI_EN	0: X-axis WOM interrupt not routed to IBI 1: X-axis WOM interrupt routed to IBI
0	-	Reserved

18.15 中断源8_

名称: 中断 _SOURCE8 地址：79 (4Fh) 串行接口：读/写 复位值：0x00 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7:6	-	保留
5	帧同步IBI使能_ _	0: 帧同步中断未路由至IBI 1: 帧同步中断路由至IBI
4	锁相环就绪IBI使能 _ _ _	0: PLL就绪中断未路由至IBI 1: PLL就绪中断路由至IBI
3	UI数据就绪IBI使能 _ _ _	0: UI数据就绪中断未路由至IBI 1: UI数据就绪中断路由至IBI
2	FIFO阈值IBI使能 _ _ _	0: FIFO阈值中断未路由至IBI 1: FIFO阈值中断路由至IBI
1	FIFO 满IBI使能 _ _ _	0: FIFO满中断未路由至IBI 1: FIFO满中断已路由至IBI
0	AGC就绪中断IBI使能 _ _ _	0: AGC就绪中断未路由至IBI 1: AGC就绪中断已路由至IBI

18.16 INT SOURCE9_

名称：INT SOURCE9_ 地址：80 (50h) 串行接口：读/写 复位值：0x00 时钟域：SCLK _UI		
BIT	**NAME**	**功能**
7	I3C 协议错误 IBI_ _ _ _EN	0: I3C^{SM} 协议错误中断未路由至IBI 1: I3C^{SM} 协议错误中断路由至IBI
6:5	-	保留
4	SMD IBI使能_ _	0: SMD中断未路由至IBI 1: SMD中断路由至IBI
3	WOM Z轴IBI 使能 _ _ _	0: Z轴WOM中断未路由至IBI 1: Z轴WOM中断路由至IBI
2	WOM Y轴IBI 使能 _ _ _	0: Y轴WOM中断未路由至IBI 1: Y轴WOM中断路由至IBI
1	WOM X IBI 使能_ _ _	0: X轴WOM中断未路由至IBI 1: X轴WOM中断已路由至IBI
0	-	保留

18.17 INT_SOURCE10

Name: INT_SOURCE10
Address: 81 (51h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:6	-	Reserved
5	STEP_DET_IBI_EN	0: Step detect interrupt not routed to IBI 1: Step detect interrupt routed to IBI
4	STEP_CNT_OFL_IBI_EN	0: Step count overflow interrupt not routed to IBI 1: Step count overflow interrupt routed to IBI
3	TILT_DET_IBI_EN	0: Tilt detect interrupt not routed to IBI 1: Tile detect interrupt routed to IBI
2	WAKE_DET_IBI_EN	0: Wake detect interrupt not routed to IBI 1: Wake detect interrupt routed to IBI
1	SLEEP_DET_IBI_EN	0: Sleep detect interrupt not routed to IBI 1: Sleep detect interrupt routed to IBI
0	TAP_DET_IBI_EN	0: Tap detect interrupt not routed to IBI 1: Tap detect interrupt routed to IBI

18.18 OFFSET_USER0

Name: OFFSET_USER0
Address: 119 (77h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_X_OFFUSER[7:0]	Lower bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

18.19 OFFSET_USER1

Name: OFFSET_USER1
Address: 120 (78h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	GYRO_Y_OFFUSER[11:8]	Upper bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.
3:0	GYRO_X_OFFUSER[11:8]	Upper bits of X-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

18.17 中断 来源10_

名称: 中断 来源10_地址:
81 (51h) 串行接口 : 读 /
写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:6	-	保留
5	步进检测IBI使能 _ _ _	0：步进检测中断未路由至IBI 1：步进检测中断路由至IBI
4	步进计数溢出IBI使能 _ _ _ _	0: 步进计数溢出中断未路由至IBI 1: 步进计数溢出中断路由至IBI
3	倾斜 检测 IBI 使能 _ _ _	0: 倾斜检测中断未路由至IBI 1: 倾斜检测中断路由至IBI
2	唤醒 检测 IBI 使能 _ _ _	0: 唤醒检测中断未路由至IBI 1: 唤醒检测中断路由至IBI
1	睡眠检测IBI使能_ _ _	0: 睡眠检测中断未路由至IBI 1: 睡眠检测中断路由至IBI
0	点击检测间隔使能 _ _ _	0: 轻触检测中断未路由至IBI 1: 轻触检测中断路由至IBI

18.18 用户0偏移量_

名称：用户0偏移量_地
址：119 (77h) 串行接口：
读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_X_用户偏移[7:0]	用户编程的X陀螺仪偏移量的低位。最大值为±64 度每秒，分辨率为1/32度/秒。

18.19 用户1偏移量_

名称: 用户1偏移量_地址:
120 (78h) 串行接口 : 读 /
写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:4	陀螺仪_Y_偏移用户[11:8]	用户编程的Y陀螺仪偏移量的高位。最大值为±64 度每秒，分辨率为1/32度每秒。
3:0	陀螺仪_X_偏移用户[11:8]	用户编程的X陀螺仪偏移量的高位。最大值为±64 度每秒，分辨率为1/32度/秒。

18.20 OFFSET_USER2

Name: OFFSET_USER2
Address: 121 (79h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_Y_OFFUSER[7:0]	Lower bits of Y-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

18.21 OFFSET_USER3

Name: OFFSET_USER3
Address: 122 (7Ah)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	GYRO_Z_OFFUSER[7:0]	Lower bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

18.22 OFFSET_USER4

Name: OFFSET_USER4
Address: 123 (7Bh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_X_OFFUSER[11:8]	Upper bits of X-accel offset programmed by user. Max value is ±1g, resolution is 0.5mg.
3:0	GYRO_Z_OFFUSER[11:8]	Upper bits of Z-gyro offset programmed by user. Max value is ±64 dps, resolution is 1/32 dps.

18.23 OFFSET_USER5

Name: OFFSET_USER5
Address: 124 (7Ch)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_X_OFFUSER[7:0]	Lower bits of X-accel offset programmed by user. Max value is ±1g, resolution is 0.5mg.

18.20 用户2偏移量_

名称：用户2偏移量_地
址：121 (79h) 串行接口：
读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_Y_用户偏移[7:0]	用户编程的Y陀螺偏移低位。最大值为±64 度每秒，分辨率为1/32度/秒。

18.21 用户3偏移量_

名称：用户3偏移量_地
址：122 (7Ah) 串行接口：
读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	陀螺仪_Z轴_用户偏移[7:0]	用户编程的Z陀螺偏移低位。最大值为±64 度每秒，分辨率为1/32度每秒。

18.22 偏移用户4_

名称：偏移用户4_地址：
123 (7Bh) 串行接口：读/
写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:4	加速度计_X_偏移用户[11:8]	用户编程的X轴加速度计偏移高位。最大值为±1g，分辨率为0.5毫克。
3:0	陀螺仪_Z_偏移用户[11:8]	用户编程的Z轴陀螺仪偏移高位。最大值为±64 度每秒，分辨率为1/32度每秒。

18.23 偏移用户5_

名称：偏移用户5_地址：
124 (7Ch) 串行接口：读/
写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	加速度计_X_偏移用户[7:0]	X轴加速度计偏移的低位由用户编程。最大值为±1g，分辨率为0.5毫克。

18.24 OFFSET_USER6

Name: OFFSET_USER6
Address: 125 (7Dh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_Y_OFFUSER[7:0]	Lower bits of Y-accel offset programmed by user. Max value is ±1g, resolution is 0.5mg.

18.25 OFFSET_USER7

Name: OFFSET_USER7
Address: 126 (7Eh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:4	ACCEL_Z_OFFUSER[11:8]	Upper bits of Z-accel offset programmed by user. Max value is ±1g, resolution is 0.5mg.
3:0	ACCEL_Y_OFFUSER[11:8]	Upper bits of Y-accel offset programmed by user. Max value is ±1g, resolution is 0.5mg.

18.26 OFFSET_USER8

Name: OFFSET_USER8
Address: 127 (7Fh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK_UI

BIT	NAME	FUNCTION
7:0	ACCEL_Z_OFFUSER[7:0]	Lower bits of Z-accel offset programmed by user. Max value is ±1g, resolution is 0.5mg.

18.24 偏移 用户6_

名称: 偏移 用户6_地址:
125 (7Dh) 串行接口: 读/
写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	加速度计_Y_偏移用户[7:0]	Y轴加速度偏移的低位由用户编程。最大值为±1重力加速度，分辨率为0.5毫克。

18.25 偏移用户7_

名称：偏移量 用户7_地
址：126 (7Eh) 串行接口：
读/写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:4	加速度计_Z_偏移用户[11:8]	用户编程的Z轴加速度偏移高位。最大值为±1重力加速度，分辨率为0.5毫克。
3:0	加速度计_Y轴_偏移用户[11:8]	用户编程的Y轴加速度偏移高位。最大值为±1重力加速度，分辨率为0.5毫克。

18.26 偏移用户8_

名称：偏移用户8_地址：
127 (7Fh) 串行接口：读/
写
复位值：0x00
时钟域：SCLK _UI

BIT	NAME	功能
7:0	加速度计_Z_偏移用户[7:0]	Z轴加速度偏移的低位由用户编程。最大值为±1g，分辨率为0.5mg。

19 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

19 参考

以下信息请参阅“应美盛微机电系统处理应用笔记(AN-IVS-0002A-00)”：

- 制造建议
  - 组装指南和建议
  - PCB设计指南和建议
  - MEMS处理说明
  - ESD注意事项
  - 回流规范
  - 存储规范
  - 包装标记规范
  - 带盘规范
  - 盘与披萨盒标签
  - 包装
  - 代表性运输纸箱标签
- 合规
  - 环境合规
  - DRC合规
  - 合规声明免责

20 DOCUMENT INFORMATION

20.1 REVISION HISTORY

Revision Date	Revision	Description
11/18/2019	1.0	Initial Release
03/02/2020	1.1	Added product overview page (Page 1); Updated Conditions in Tables 1 and 2; Updated SPI timing characteristics specs (Tables 6, 7); Updated SPI interface description (Section 9.6)
04/19/2020	1.2	Updated specification notes (Tables 1, 2, 3, 4); Updated absolute maximum ratings (Table 8)
08/28/2020	1.3	Updated Internal Clock Source and Notes (Table 4); Added SPI SCLK Fall Time/Rise Time (Tables 6, 7); Updated APEX Hardware Initialization for Pedometer Programming (Section 8.3); Updated I3C^{SM} Interface information (Section 9.2); Added Use Note 12.9 (Register Values Modification); Added ASYNCTIME0_DIS information (Sections 13.2, 15.19)
09/28/2020	1.4	Added Section 3.7 RTC (CLKIN) Timing Characterization
05/05/2021	1.5	Updated FIFO Timestamp Interval Scaling (Section 12.7); Updated TMST_RES register field description (Section 14.42)
06/20/2021	1.6	Updated FIFO_COUNTH and FIFO_COUNTL description (Section 14.22, 14.23)
12/01/2022	1.7	Updated Figure 5
07/27/2023	1.8	Updated Notch Filter (Section 5.2); Added CLKDIV (Section 13.4, 17.1)

20 文档信息

20.1 修订历史

修订日期	修订版本	描述
11/18/2019	1.0	初始发布
03/02/2020	1.1	新增产品概述页（第1页）；更新表1和2中的条件；更新SPI时序特性规格（表6、7）；更新SPI接口描述（第9.6节）
2020年4月19日	1.2	更新后的规格说明（表1、2、3、4）；更新后的绝对最大额定值（表8）
2020年8月28日	1.3	更新后的内部时钟源和说明（表4）；新增SPI SCLK下降时间/上升时间（表6、7）；更新后的计步器APEX硬件初始化编程（第8.3节）；更新后的I3C^{SM}接口信息（第9.2节）；新增使用说明12.9（寄存器值修改）；新增ASYNCTIME0_DIS信息（第13.2、15.19节）
2020年9月28日	1.4	新增第3.7节RTC (CLKIN)时序特性
2021年5月5日	1.5	更新后的FIFO时间戳间隔缩放 (第12.7节)；更新TMST_RES寄存器字段描述 (第14.42节)
2021年6月20日	1.6	更新FIFO_COUNTH和FIFO_COUNTL描述 (第14.22、14.23节)
2022年12月1日	1.7	更新后的图5
2023年7月27日	1.8	更新陷波滤波器（第5.2节）；新增时钟分频器（第13.4节、17.1节）

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