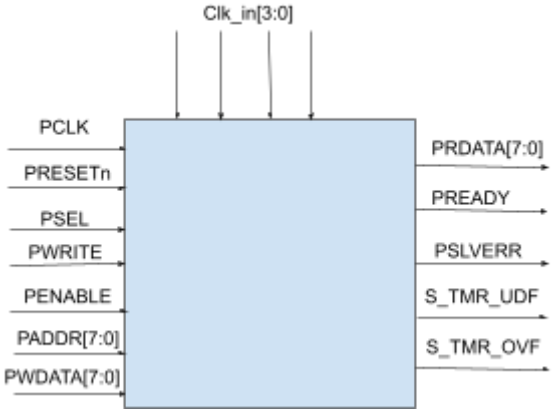
TIMER DESIGN

1. **Overview**
    a. **Feature**
        - Selection of four clock sources
          The counters can be driven by one of four internal clock signals
            - ☐ T*2
            - ☐ T*4
            - ☐ T*8
            - ☐ T*16

          or an external clock input
        - The counters can be cleared by an external reset signal (falling edge)
        - Timer output control by a combination of two signals, underflow and overflow. Underflow signal triggers when the counter counts down and overflow signal triggers when the counter counts up.

    b. **Block diagram**



    c. **Input/Outputs pin (LSI pin – CHIP PIN/PORT)**

Signal	Source	Description
Clk_in	INPUT	User Clock. The rising edge of this clock signal indicates that the counter is ready to count up or down whenever the system clock is triggered.
PCLK	INPUT	System Clock. The

		rising edge of PCLK times all transfers on the APB.
PRESETn	INPUT	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PSEL	INPUT	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PWRITE	INPUT	Direction signal. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PENABLE	INPUT	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PADDR	INPUT	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PWDATA	INPUT	Write data. This bus is driven by the peripheral bus bridge

		unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PRDATA	OUTPUT	Read data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PREADY	OUTPUT	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	OUTPUT	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.
S_TMR_UDF	OUTPUT	Underflow signal. This signal is triggered when the counter goes below 8'h00.
S_TMR_OVF	OUTPUT	Overflow signal. This signal is triggered when the counter goes above 8'hff.

d. Register specification

- **Timer Data Register (TDR):**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reg_tdr[7:0]							

Bit Description of TDR:

Bit Name	F/V	Description
reg_tdr[7:0]	R/W	This register contains the data used for updating the value of counter when this register is updated to new value

- **Timer Counter Control Register (TCR):**

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Load	Reserved	Up/Down	En	Reserved	Reserved	cks1	cks0

Bit Description of TCR

Bit name	**F/V**	**Description**
Load[7]	R/W	Manual load data from TDR to TCNT when it active High. 1: load data to TCNT 0: Normal operation.
6	Reserved	Reserved
Up/Down[5]	R/W	Control counter up or counter down 0: counter up 1: counter down
En[4]	R/W	0: disable 1: enable
3:2	Reserved	Reserved

cks[1:0]	R/W	Select internal clocks for circuit 00: T*2 01: T*4 10: T*8 11: T*16

- **Timer Status Register (TSR):**

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved						S_TMR_UDF	S_TMR_OVF

Bit Description of TSR:

Bit name	**R/W**	**Description**
7:2	R	Reserved
S_TMR_UDF	R/W*	Timer counter underflow when counter 8'h00 down to 8'hff: This bit is only set by hardware, clear by software
S_TMR_OVF	R/W*	Timer counter overflow when counter 8'hff to 8'h00: This bit is only set by hardware, clear by software

2. **Read/write register control**
   a. **Input/Outputs pin**

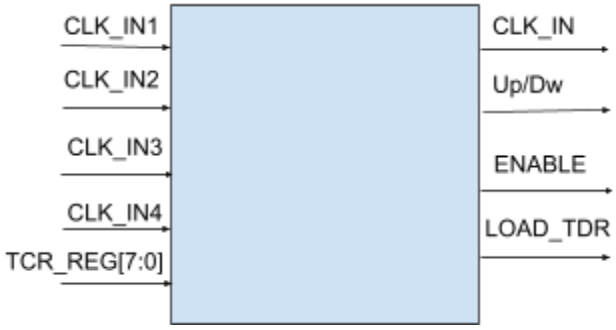
b. **Functional/Protocol**

c. **State machine control for APB protocol**

d. **Timing chart**

3. **Control logic**

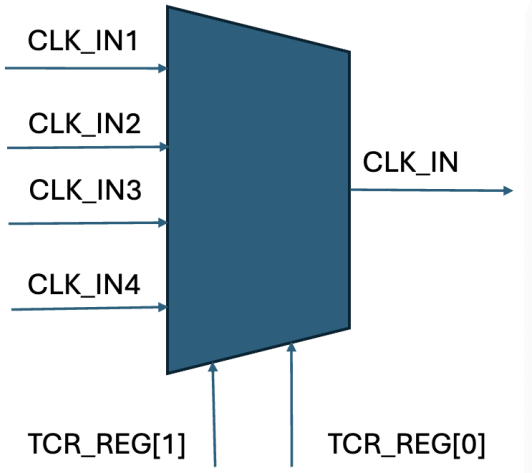
a. **Input/Outputs pin**



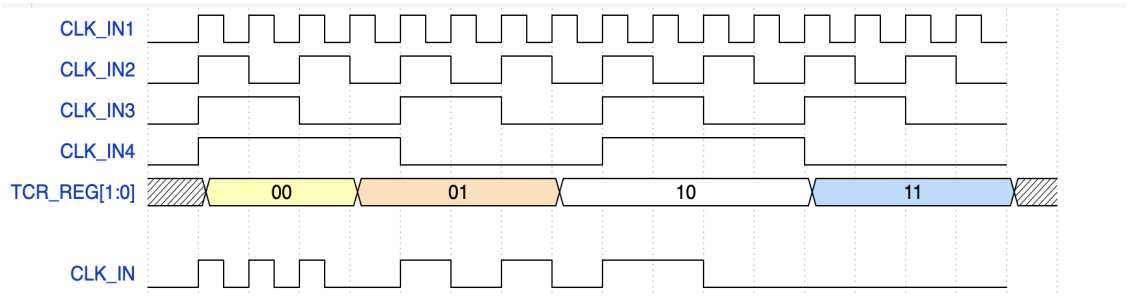
b. **Functional/Protocol**

This block is responsible for choosing the counting clock CLK_IN1, CLK_IN2, CLIK_IN3, CLK_IN4 through a 4:2 mux with the first two bits of TCR_REG as an enable signal. This clock signal and load_data, up/dw and en signals from TCR_REG are used as inputs to the timer counter (TCNT) block.

c. **Design circuit**

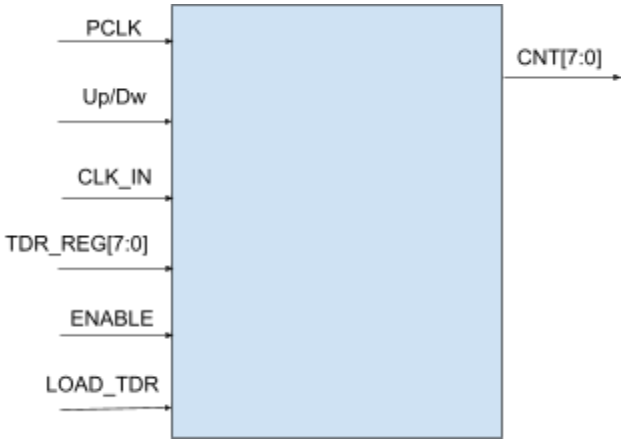


d. **Timing chart**



4. Timer counter (TCNT)

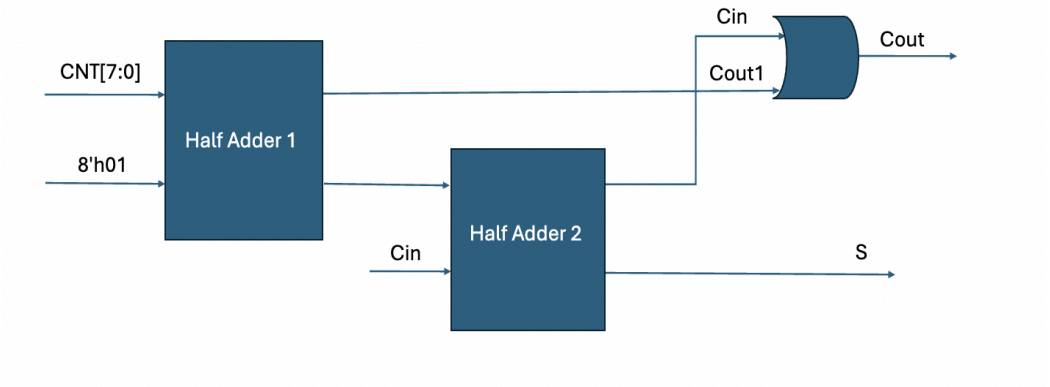
a. Input/Outputs pin



b. Functional/Protocol

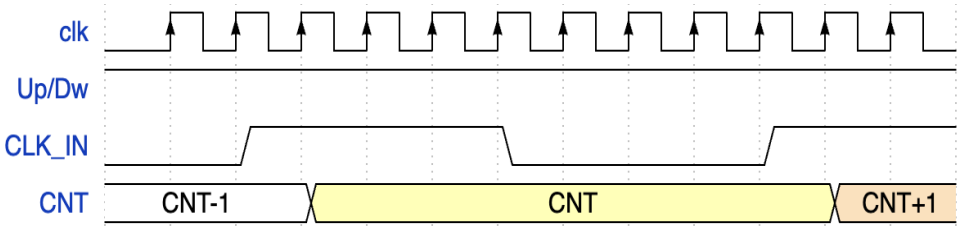
This block is responsible for counting up/down. If the rising edge of counting clock clk_in is detected, the counter is counted up or down in the next system clock cycle. If the value of LOAD_TDR is high, the value of TDR_REG[7:0] is going to be loaded into CNT and the counter starts counting from there. Otherwise the CNT signal performs normal operation.

c. Design circuit

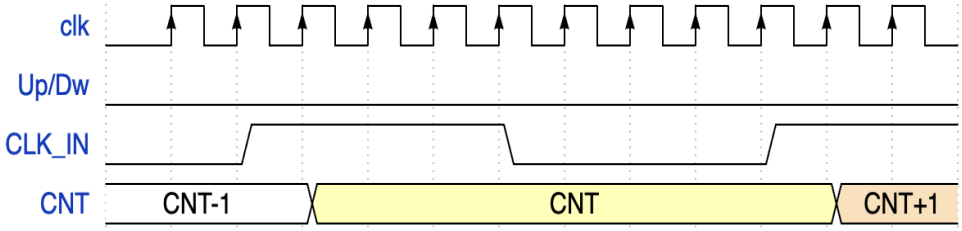


d. Timing chart

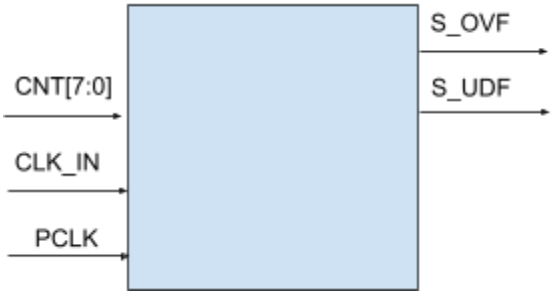
- **Counter up**



- **Counter down**



5. **Overflow/Underflow comparison**
   a. **Input/Outputs pin**

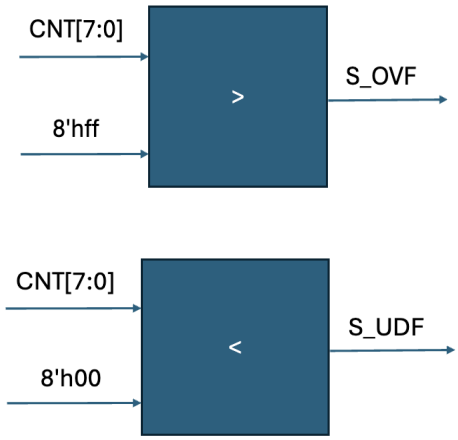


   b. **Functional/Protocol**

   This block is responsible for updating the two bits of TSR_REG[7:0], S_TMR_UDF[1] and S_TMR_OVF[0].

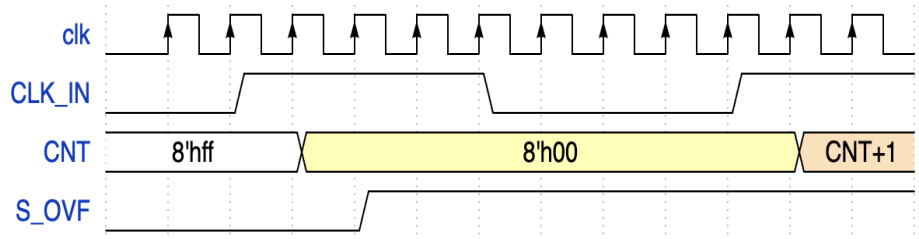
   - If the counter is counting up, it compares the value of CNT to 8'hff to determine if the counter is overflowing and S_TMR_OVF[0] is triggered. Output S_OVF is set to 1 at the next clock cycle after counter changes from 8'hff to 8'h00.
   - Otherwise it compares the value of CNT to 8'h00 to determine if the counter is underflowing and S_TMR_UDF[1] is triggered. Output S_UDF is set to 1 at the next clock cycle after counter changes from 8'h00 to 8'hff.

   c. **Design circuit**



d. Timing chart

- **Overflow**



- **Underflow**