WOLF CREEK
COMPUTE CANISTER

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wolfcreek_controller	DATE: Wed Jul 16 11:04:44 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 1OF360	

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SYSTEM BLOCK DIAGRAM

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 14:01:00 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 7OF360

CE:0 : @WOLFCREEK_CONTROLLER_LIB.WOLFCREEK_CONTROLLER:SCH,LIBPACKB

POWER BLOCK DIAGRAM

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wolfcreek_controller

wolfcreek_controller.cpm

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DATE: Wed Jul 16 14:17:03 2014	DWG NO: <DWG>	REV: A-0
DRAWNBY: <ENGINEER>	SHEET: 80F360	

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POWER BUDGET TABLE

wolfcreek_controller	DATE: Wed Jul 02 14:01:00 2014	DWG NO: <DRAWING>	REV: <REVISION>
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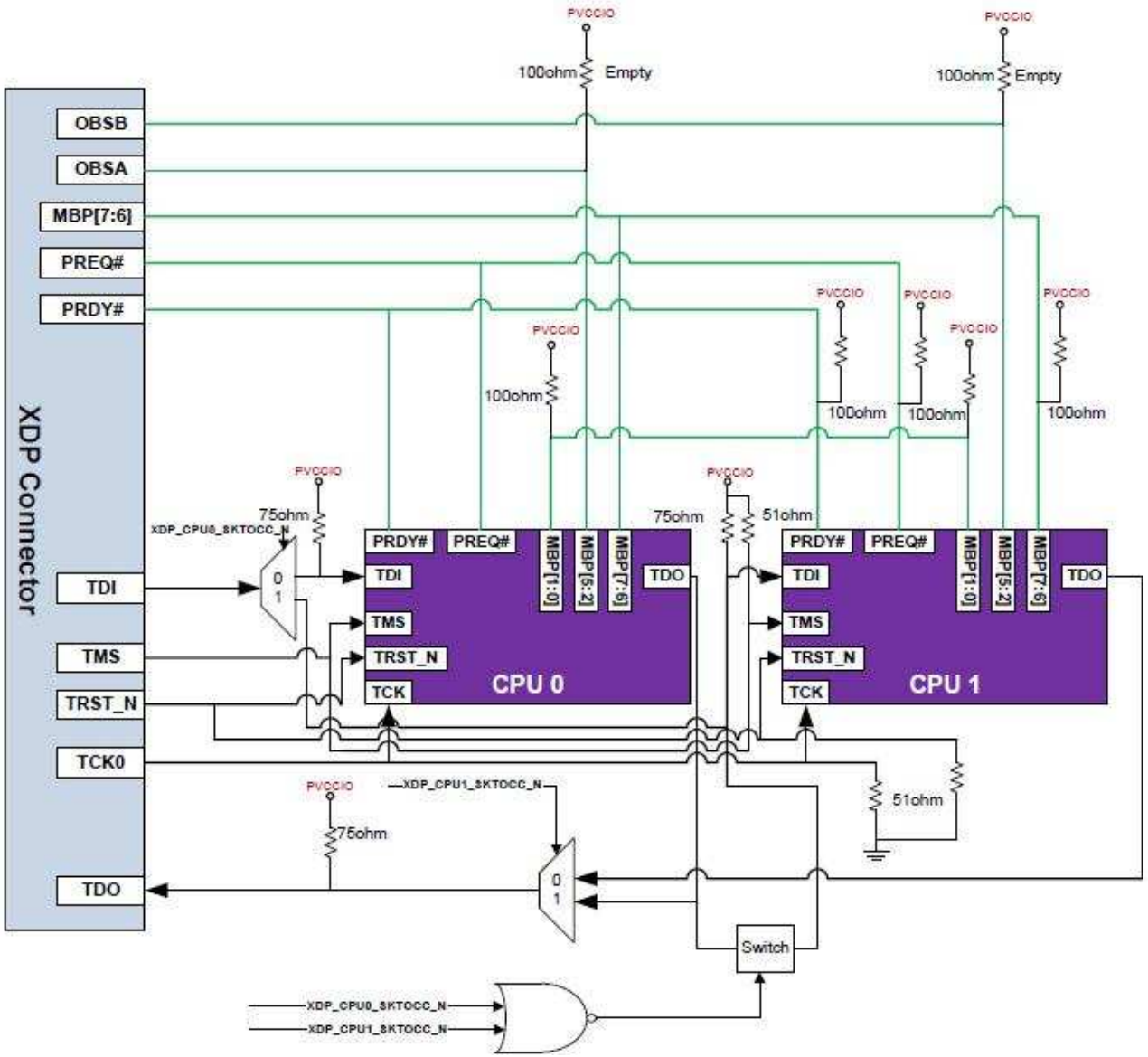

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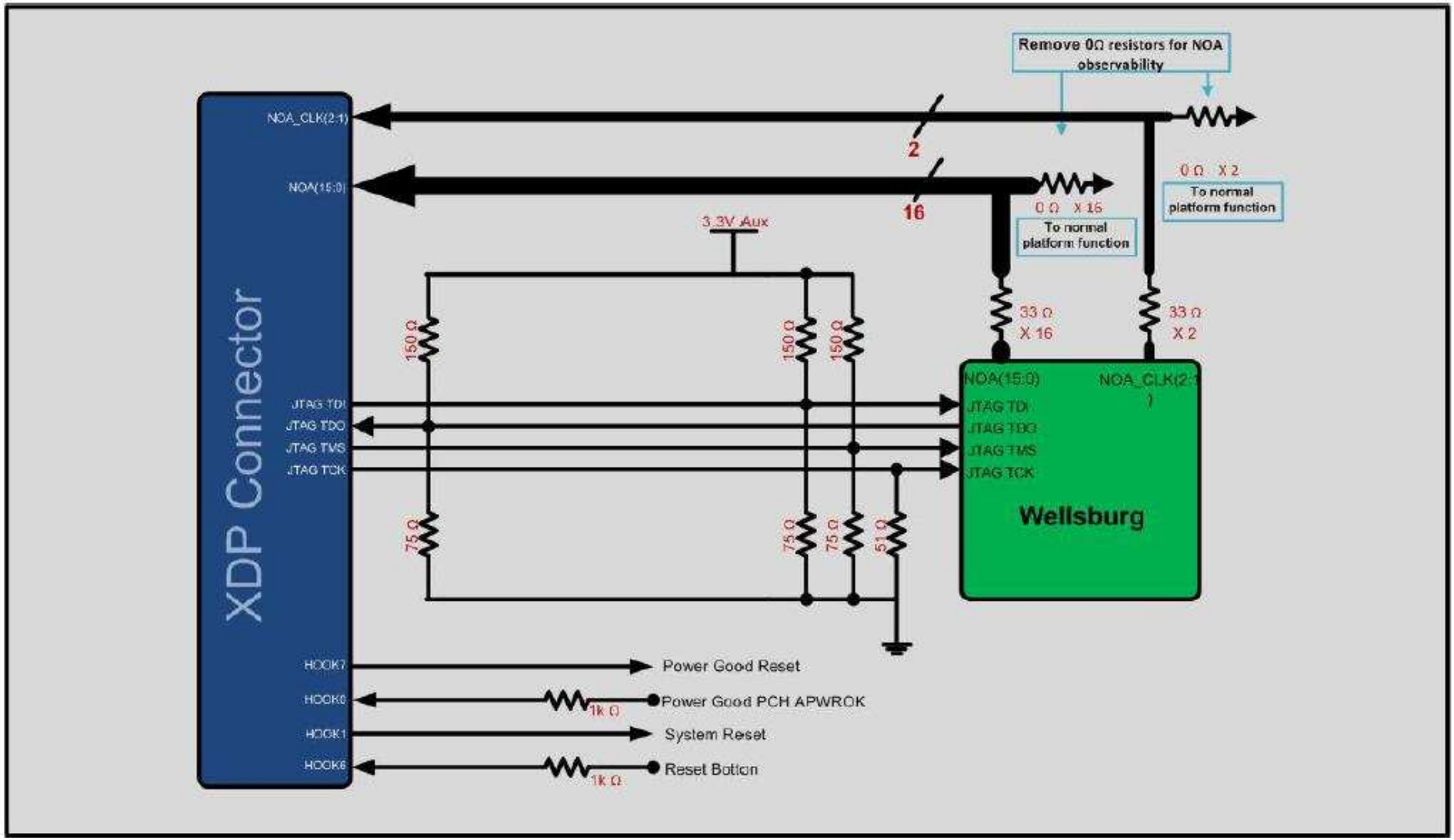
wolfcreek_controller	XDP/JTAG BLOCK DIAGRAM(CPU)	DATE: Sat Jun 28 11:00:57 2014	DWG NO: <DRAWING> / REV: <REVISION>
wolfcreek_controller.cpm		DRAWN BY: <ENGINEER>	SHEET: 10OF360



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wolfcreek_controller	XDP/JTAG BLOCK DIAGRAM(PCH)	DATE: Sat Jun 28 11:00:59 2014	DWG NO: <DRAWING> REV: <REVISION>
wolfcreek_controller.cpm		DRAWN BY: <ENGINEER>	SHEET: 11OF360

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wolfcreek_controller	CLOCK DISTRIBUTION DIAGRAM	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DATE: Wed Jul 02 14:01:00 2014	SHEET: 12OF360	
	DRAWN BY: <ENGINEER>		

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POWER SEQUENCE DIAGRAM

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 14:01:00 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

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RESET BLOCK DIAGRAM

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SMBUS DIAGRAM
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 14:01:00 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 15OF360

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UNTITLED wolfcreek_controller	DATE: Sat Jun 28 11:01:08 2014	DWG NO: <DRAWING>	REV: <REVISION>
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SPI BIOS DIAGRAM

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 14:01:01 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 17OF360

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PCIE DIAGRAM
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 14:01:01 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

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USB PORT MAPPING

wolfcreek_controller

wolfcreek_controller.cpm

DATE:	Wed Jul 02 14:01:01 2014
DRAWN BY:	<ENGINEER>
DWG NO:	<DRAWING>
REV:	<REVISION>
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UNTITLED wolfcreek_controller	DATE: Sat Jun 28 11:01:16 2014	DWG NO: <DRAWING>	REV: <REVISION>
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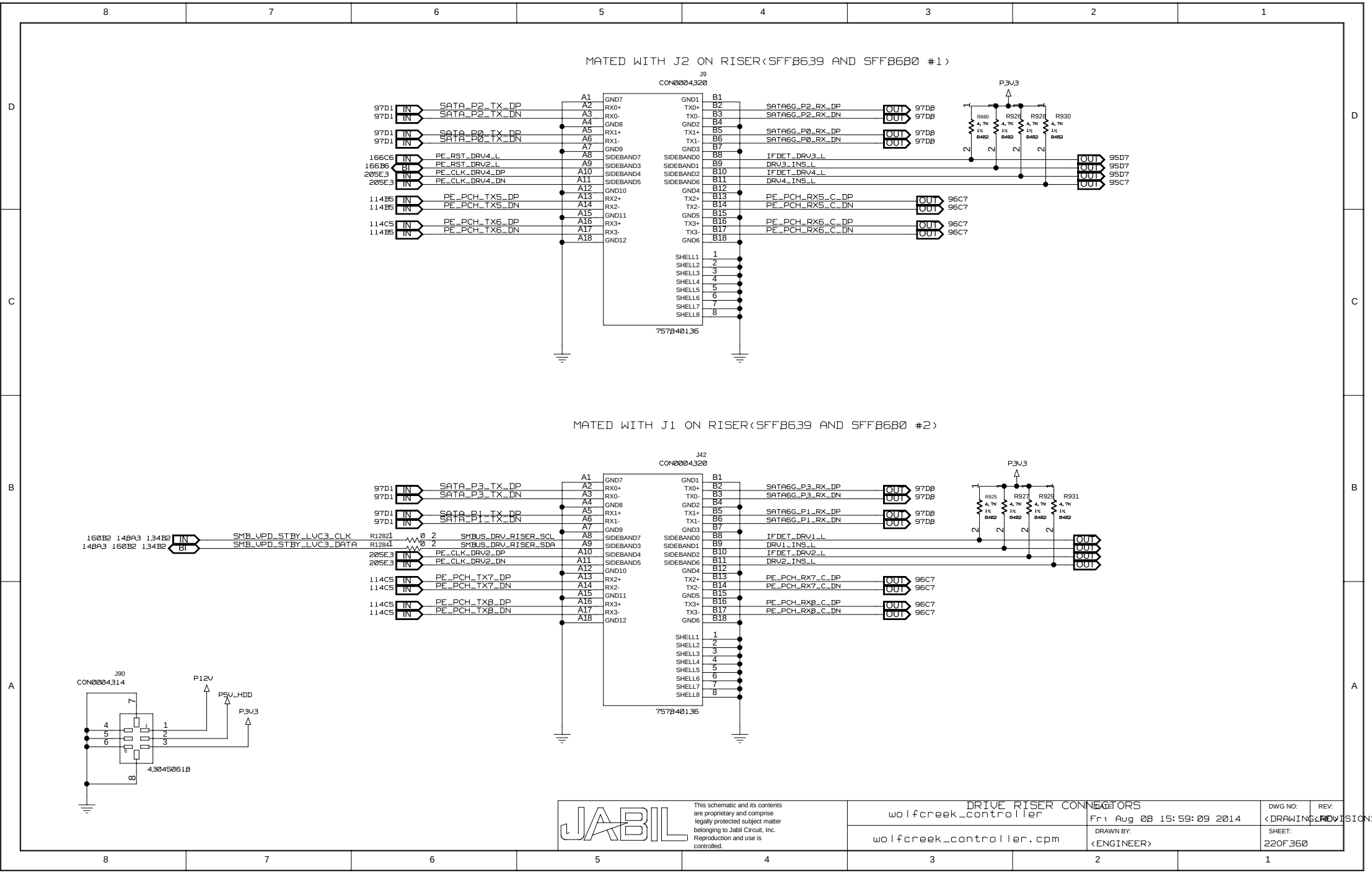
UNTITLED wolfcreek_controller	DATE: Sat Jun 28 11:01:17 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 21OF360	


MATED WITH J2 ON RISER(SFF8639 AND SFF8680 #1)
J9
CON0004320
757B401,36
SATA_P2_TX_DP
SATA_P2_TX_DN
SATA_P0_TX_DP
SATA_P0_TX_DN
PE_RST_DRV4_L
PE_RST_DRV2_L
PE_CLK_DRV4_DP
PE_CLK_DRV4_DN
PE_PCH_TX5_DP
PE_PCH_TX5_DN
PE_PCH_TX6_DP
PE_PCH_TX6_DN
SATA6G_P2_RX_DP
SATA6G_P2_RX_DN
SATA6G_P0_RX_DP
SATA6G_P0_RX_DN
IFDET_DRV3_L
DRV3_INS_L
IFDET_DRV4_L
DRV4_INS_L
PE_PCH_RX5_C_DP
PE_PCH_RX5_C_DN
PE_PCH_RX6_C_DP
PE_PCH_RX6_C_DN
P3V3
R880
R926
R928
R930
MATED WITH J1 ON RISER(SFF8639 AND SFF8680 #2)
J42
CON0004320
757B401,36
SATA_P3_TX_DP
SATA_P3_TX_DN
SATA_P1_TX_DP
SATA_P1_TX_DN
SMB_VPD_STBY_LVC3_CLK
SMB_VPD_STBY_LVC3_DATA
R1282
R1284
SMBUS_DRV_RISER_SCL
SMBUS_DRV_RISER_SDA
PE_CLK_DRV2_DP
PE_CLK_DRV2_DN
PE_PCH_TX7_DP
PE_PCH_TX7_DN
PE_PCH_TX8_DP
PE_PCH_TX8_DN
SATA6G_P3_RX_DP
SATA6G_P3_RX_DN
SATA6G_P1_RX_DP
SATA6G_P1_RX_DN
IFDET_DRV1_L
DRV1_INS_L
IFDET_DRV2_L
DRV2_INS_L
PE_PCH_RX7_C_DP
PE_PCH_RX7_C_DN
PE_PCH_RX8_C_DP
PE_PCH_RX8_C_DN
P3V3
R925
R927
R929
R931
J90
CON0004314
P12V
P5V_HDD
P3V3
4,3045061B
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DRIVE RISER CONNECTORS
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Fri Aug 08 15:59:09 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING NO>
REV:
<REVISION>
SHEET:
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PLACE R1044 CLOSED TO THE CPU.

J94
CON0003,B41

204F3 IN	CK_100M_CPU0_B0_DP	CL41	BCLK0_DP				
204E3 IN	CK_100M_CPU0_B0_DN	CN41	BCLK0_DN				
204E3 IN	CK_100M_CPU0_B1_DP	BA45	BCLK1_DP				
204E3 IN	CK_100M_CPU0_B1_DN	AW45	BCLK1_DN				
B4B8 IN	PWRGD_CPU0_AB_DRAM_G	CH16	DRAM_PWR_OK_C01				
B4A8 IN	PWRGD_CPU0_CD_DRAM_G	W29	DRAM_PWR_OK_C23				
69B3 69B4 6BB3 6BB4 OUT	M_AB_RESET_N	DC15	DDR_RESET_C01_N				
71B3 71B4 70B3 70B4 OUT	M_CD_RESET_N	C23	DDR_RESET_C23_N				
7BA8 B1B5 BI	H_CPU0_MEMAB_MEMHOT_G_N	CL33	MEM_HOT_C01_N				
7BA8 B1A5 BI	H_CPU0_MEMCD_MEMHOT_G_N	P36	MEM_HOT_C23_N				
23A7 OUT	M_AB_CPU_VREF	BY16	DDR01_VREF				
	TP_AB_VREFDQ_1	CP40	RSVD_CP40				
	TP_AB_VREFDQ_0	CF40	RSVD_CF40				
23A3 OUT	M_CD_CPU_VREF	T40	DDR23_VREF				
	TP_CD_VREFDQ_1	M40	RSVD_M40				
	TP_CD_VREFDQ_0	R41	RSVD_R41				
122D8 OUT	SMB_DDR_AB_SCL_G	CK42	DDR_SCL_C01				
122D8 BI	SMB_DDR_AB_SDA_G	CM42	DDR_SDA_C01				
122C8 OUT	SMB_DDR_CD_SCL_G	V40	DDR_SCL_C23				
122C8 BI	SMB_DDR_CD_SDA_G	Y40	DDR_SDA_C23				
23B7	SMB_PE_HP_CPU0_SCL_GTL	B46	PE_HP_SCL				
23B7	SMB_PE_HP_CPU0_SDA_GTL	D46	PE_HP_SDA				
37C7 127D6 127A8 IN	XDP_CPU_OBSFN_B_MBP7_G_N	AW43	BPM_N<7>				
127D6 127A8 IN	XDP_CPU_OBSFN_B_MBP6_G_N	BA43	BPM_N<6>				
37C7 127D6 IN	XDP_CPU0_OBSDATA_A_MBP5_G_N	BD46	BPM_N<5>				
127B7 127D6 IN	XDP_CPU0_OBSDATA_A_MBP4_G_N	BE45	BPM_N<4>				
127D6 127B7 IN	XDP_CPU0_OBSDATA_A_MBP3_G_N	BF46	BPM_N<3>				
127B7 127D6 IN	XDP_CPU0_OBSDATA_A_MBP2_G_N	BE47	BPM_N<2>				
127A7	XDP_CPU_MBP1_G_N	BB44	BPM_N<1>				
	XDP_CPU_MBP0_G_N	BC43	BPM_N<0>				
12BA8 127D6 IN	XDP_CPU0_PREQ_G_N	CW49	PREQ_N				
127D6 12BA4 OUT	XDP_CPU0_PRDY_G_N	CU49	PRDY_N				
12BD8 IN	XDP_CPU0_TDI_G	CF42	TDI				
37B7 12BB3 127C6 IN	XDP_CPU_TCK_G	CA45	TCK				
37B7 12BC3 127C3 IN	XDP_CPU_TMS_G	BY46	TMS				
37B7 12BB3 127C3 IN	XDP_CPU_TRST_G_N	CV50	TRST_N				

			PWRGOOD	BJ53	PWRGD_CPU0_G	IN	B4D7 127C8
			RESET_N	CR43	RST_CPU0_G_N	IN	B4C7 127C1
			EAR_N	CE53	PU_CPU0_EAR_G_N	IN	B5A6
			PMSYNC	K52	H_PM_SYNC_G	IN	97B2 37D2
			PECI	CG55	PECI_CPU_G	BI	37D2 15BB7
			SVIDDATA	AR43	SVID_DIO_CPU0_AR43_R R14351 0	BI	PVCCIN_CPU0_SDIO BI 227C2 229B2 231B2
			SVIDCLK	AU43	SVID_CLK_R_CPU0 1 5.11 R1044 2 1% 0402 PVCCIN_CPU0_SCLK	OUT	227B2 229B2 231B2
			SVIDALERT_N	AN43	SVID_ALERT_CPU0_R1_G R662 1 220 2 1% 0603 PVCCIN_CPU0_ALERT	IN	231B2 227C2 229B2
			CATERR_N	CC51	H_CPU0_CATERR_G_N	OUT	79D8
			ERROR<2>_N	BB52	H_CPU0_ERR2_G_N	OUT	77C8
			ERROR<1>_N	BB48	H_CPU0_ERR1_G_N	OUT	77C8
			ERROR<0>_N	BD50	H_CPU0_ERR0_G_N	OUT	77D8
			MSMI_N	H52	H_CPU0_MSMI_G_N	OUT	B5B8
			PROCHOT_N	BL51	H_CPU0_PROCHOT_G_N	BI	B1D1 B2D4 7BC8
			THERMTRIP_N	BJ47	H_CPU0_THERMTRIP_G_N	OUT	B5A4 7BC8
			SAFE_MODE_BOOT	BK56	PU_CPU0_SAFE_MODE_BOOT	IN	76C6
			FRMAGENT	Y48	PU_CPU0_FRMAGENT	IN	76D6
			BMCINIT	AM48	PU_CPU0_BMCINIT	IN	76D6
			TXT_AGENT	AH52	PU_CPU0_TXT_AGENT	IN	76D4
			TXT_PLTEN	AF52	PD_CPU0_TXT_PLTEN	IN	76D4
			BIST_ENABLE	AJ43	PD_CPU0_BIST_ENABLE	IN	76C4
			PM_FAST_WAKE_N	AV44	H_CPU0_FAST_WAKE_G_N	IN	B5D8
			SKTOCC_N	BU49	FM_CPU0_SKTOCC_LVT3_N	OUT	B5C4 12BB8 165B8 166C6
			SOCKET_ID<1>	CC53	PU_CPU0_SOCKET_ID_1	OUT	76C6
			SOCKET_ID<0>	CP52	PU_CPU0_SOCKET_ID_0	OUT	76C6
			PROC_ID	AB48	FM_CPU0_BDX_PRSNT_LVT3_N	OUT	B5C2 135B2 166C6 243C7
			RSVD_C53	C53	TP_G_CPU0_OVERCLK		
			RSVD_CR51	CR51	NC_CPU0_LGSPARE_5		
			RSVD_AV46	AV46	NC_CPU0_LGSPARE_4		
			RSVD_AY46	AY46	NC_CPU0_LGSPARE_3		
			RSVD_AJ55	AJ55	NC_CPU0_LGSPARE_1		
			RSVD_BD48	BD48	NC_CPU0_LGSPARE_0		
			TDO	CG41	XDP_CPU0_TDO_G	OUT	12BB4 12BC5

SYM 1 OF 18

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PVCCIO

R654 100 1% 0402
R655 100 1% 0402

37C8 BI
37C8 BI

PVCCIO

R1415 4.7K 1% 0402 SMB_PE_HP_CPU0_SCL_GTL 23C6
R1416 4.7K 1% 0402 SMB_PE_HP_CPU0_SDA_GTL 23C6

PVDDQ_AB

R658 1K 1% 0402

23D7 IN M_AB_CPU_VREF R656 5% 0402 M_AB_VREF OUT 52A8 53A8 54A8 55A8

C667 0.01UF 25V 0402
R657 1K 1% 0402

PVDDQ_CD

R661 1K 1% 0402

23C7 IN M_CD_CPU_VREF R659 5% 0402 M_CD_VREF OUT 56A8 57A8 58A8 59A8

C668 0.01UF 25V 0402
R660 1K 1% 0402

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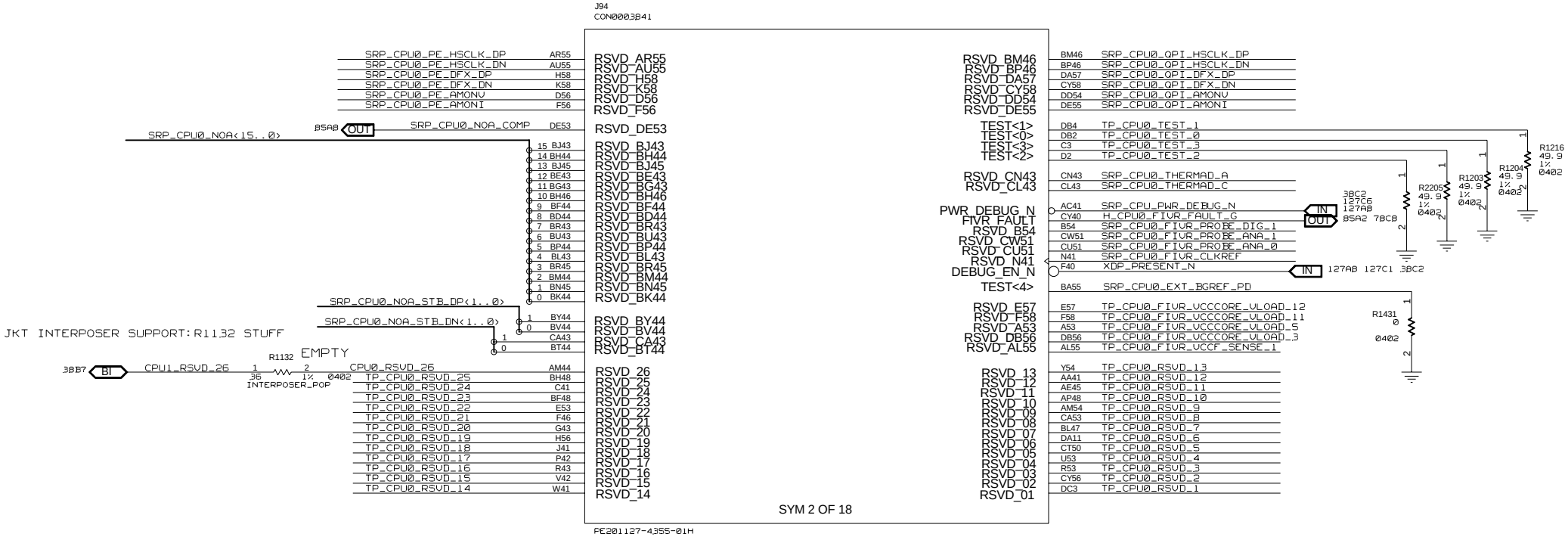
HASWELL SOCKET 0 (1 OF 14)
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Wed Jul 30 14:58:15 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 2,30F,360



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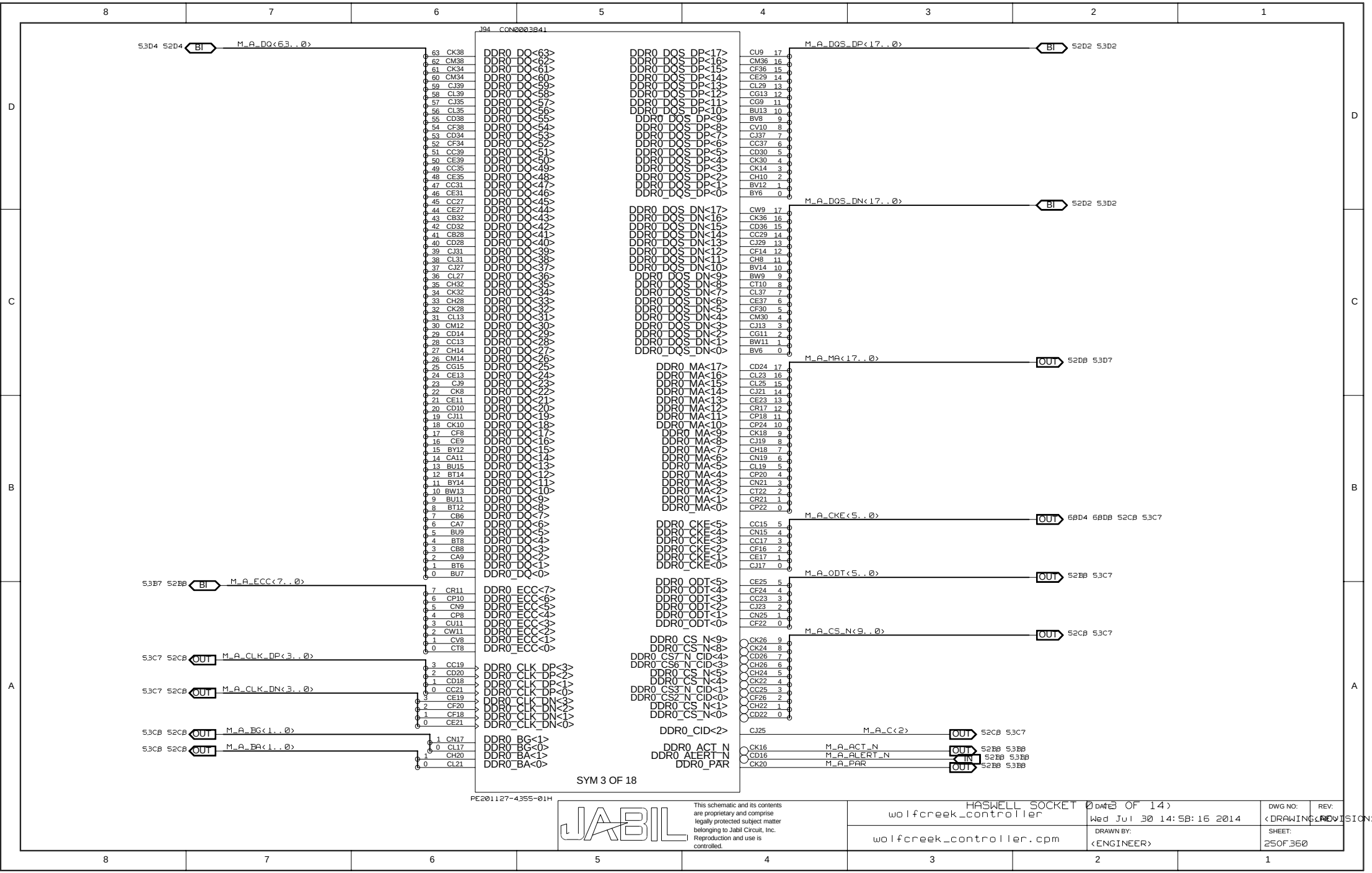
HASWELL SOCKET 0 (2 OF 14) wolfcreek_controller	DATE: Wed Jul 30 14:58:15 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 24OF36O	


J94 CON0003B41
5,3D4 52D4 BI M_A_DQ<63..0>
63 CK38 DDR0_DQ<63>
62 CM38 DDR0_DQ<62>
61 CK34 DDR0_DQ<61>
60 CM34 DDR0_DQ<60>
59 CJ39 DDR0_DQ<59>
58 CL39 DDR0_DQ<58>
57 CJ35 DDR0_DQ<57>
56 CL35 DDR0_DQ<56>
55 CD38 DDR0_DQ<55>
54 CF38 DDR0_DQ<54>
53 CD34 DDR0_DQ<53>
52 CF34 DDR0_DQ<52>
51 CC39 DDR0_DQ<51>
50 CE39 DDR0_DQ<50>
49 CC35 DDR0_DQ<49>
48 CE35 DDR0_DQ<48>
47 CC31 DDR0_DQ<47>
46 CE31 DDR0_DQ<46>
45 CC27 DDR0_DQ<45>
44 CE27 DDR0_DQ<44>
43 CB32 DDR0_DQ<43>
42 CD32 DDR0_DQ<42>
41 CB28 DDR0_DQ<41>
40 CD28 DDR0_DQ<40>
39 CJ31 DDR0_DQ<39>
38 CL31 DDR0_DQ<38>
37 CJ27 DDR0_DQ<37>
36 CL27 DDR0_DQ<36>
35 CH32 DDR0_DQ<35>
34 CK32 DDR0_DQ<34>
33 CH28 DDR0_DQ<33>
32 CK28 DDR0_DQ<32>
31 CL13 DDR0_DQ<31>
30 CM12 DDR0_DQ<30>
29 CD14 DDR0_DQ<29>
28 CC13 DDR0_DQ<28>
27 CH14 DDR0_DQ<27>
26 CM14 DDR0_DQ<26>
25 CG15 DDR0_DQ<25>
24 CE13 DDR0_DQ<24>
23 CJ9 DDR0_DQ<23>
22 CK8 DDR0_DQ<22>
21 CE11 DDR0_DQ<21>
20 CD10 DDR0_DQ<20>
19 CJ11 DDR0_DQ<19>
18 CK10 DDR0_DQ<18>
17 CF8 DDR0_DQ<17>
16 CE9 DDR0_DQ<16>
15 BY12 DDR0_DQ<15>
14 CA11 DDR0_DQ<14>
13 BU15 DDR0_DQ<13>
12 BT14 DDR0_DQ<12>
11 BY14 DDR0_DQ<11>
10 BW13 DDR0_DQ<10>
9 BU11 DDR0_DQ<9>
8 BT12 DDR0_DQ<8>
7 CB6 DDR0_DQ<7>
6 CA7 DDR0_DQ<6>
5 BU9 DDR0_DQ<5>
4 BT8 DDR0_DQ<4>
3 CB8 DDR0_DQ<3>
2 CA9 DDR0_DQ<2>
1 BT6 DDR0_DQ<1>
0 BU7 DDR0_DQ<0>
5,3B7 52B8 BI M_A_ECC<7..0>
7 CR11 DDR0_ECC<7>
6 CP10 DDR0_ECC<6>
5 CN9 DDR0_ECC<5>
4 CP8 DDR0_ECC<4>
3 CU11 DDR0_ECC<3>
2 CW11 DDR0_ECC<2>
1 CV8 DDR0_ECC<1>
0 CT8 DDR0_ECC<0>
5,3C7 52C8 OUT M_A_CLK_DP<3..0>
3 CC19 DDR0_CLK_DP<3>
2 CD20 DDR0_CLK_DP<2>
1 CD18 DDR0_CLK_DP<1>
0 CC21 DDR0_CLK_DP<0>
5,3C7 52C8 OUT M_A_CLK_DN<3..0>
3 CE19 DDR0_CLK_DN<3>
2 CF20 DDR0_CLK_DN<2>
1 CF18 DDR0_CLK_DN<1>
0 CE21 DDR0_CLK_DN<0>
5,3C8 52C8 OUT M_A_BG<1..0>
1 CN17 DDR0_BG<1>
0 CL17 DDR0_BG<0>
5,3C8 52C8 OUT M_A_BA<1..0>
1 CH20 DDR0_BA<1>
0 CL21 DDR0_BA<0>
DDR0_DQS_DP<17> CU9 17
DDR0_DQS_DP<16> CM36 16
DDR0_DQS_DP<15> CF36 15
DDR0_DQS_DP<14> CE29 14
DDR0_DQS_DP<13> CL29 13
DDR0_DQS_DP<12> CG13 12
DDR0_DQS_DP<11> CG9 11
DDR0_DQS_DP<10> BU13 10
DDR0_DQS_DP<9> BV8 9
DDR0_DQS_DP<8> CV10 8
DDR0_DQS_DP<7> CJ37 7
DDR0_DQS_DP<6> CC37 6
DDR0_DQS_DP<5> CD30 5
DDR0_DQS_DP<4> CK30 4
DDR0_DQS_DP<3> CK14 3
DDR0_DQS_DP<2> CH10 2
DDR0_DQS_DP<1> BV12 1
DDR0_DQS_DP<0> BY6 0
M_A_DQS_DP<17..0> BI 52D2 53D2
DDR0_DQS_DN<17> CW9 17
DDR0_DQS_DN<16> CK36 16
DDR0_DQS_DN<15> CD36 15
DDR0_DQS_DN<14> CC29 14
DDR0_DQS_DN<13> CJ29 13
DDR0_DQS_DN<12> CF14 12
DDR0_DQS_DN<11> CH8 11
DDR0_DQS_DN<10> BV14 10
DDR0_DQS_DN<9> BW9 9
DDR0_DQS_DN<8> CT10 8
DDR0_DQS_DN<7> CL37 7
DDR0_DQS_DN<6> CE37 6
DDR0_DQS_DN<5> CF30 5
DDR0_DQS_DN<4> CM30 4
DDR0_DQS_DN<3> CJ13 3
DDR0_DQS_DN<2> CG11 2
DDR0_DQS_DN<1> BW11 1
DDR0_DQS_DN<0> BV6 0
M_A_DQS_DN<17..0> BI 52D2 53D2
DDR0_MA<17> CD24 17
DDR0_MA<16> CL23 16
DDR0_MA<15> CL25 15
DDR0_MA<14> CJ21 14
DDR0_MA<13> CE23 13
DDR0_MA<12> CR17 12
DDR0_MA<11> CP18 11
DDR0_MA<10> CP24 10
DDR0_MA<9> CK18 9
DDR0_MA<8> CJ19 8
DDR0_MA<7> CH18 7
DDR0_MA<6> CN19 6
DDR0_MA<5> CL19 5
DDR0_MA<4> CP20 4
DDR0_MA<3> CN21 3
DDR0_MA<2> CT22 2
DDR0_MA<1> CR21 1
DDR0_MA<0> CP22 0
M_A_MA<17..0> OUT 52D8 53D7
DDR0_CKE<5> CC15 5
DDR0_CKE<4> CN15 4
DDR0_CKE<3> CC17 3
DDR0_CKE<2> CF16 2
DDR0_CKE<1> CE17 1
DDR0_CKE<0> CJ17 0
M_A_CKE<5..0> OUT 68D4 68D8 52C8 53C7
DDR0_ODT<5> CE25 5
DDR0_ODT<4> CF24 4
DDR0_ODT<3> CC23 3
DDR0_ODT<2> CJ23 2
DDR0_ODT<1> CN25 1
DDR0_ODT<0> CF22 0
M_A_ODT<5..0> OUT 52B8 53C7
DDR0_CS_N<9> CK26 9
DDR0_CS_N<8> CK24 8
DDR0_CS7_N_CID<4> CD26 7
DDR0_CS6_N_CID<3> CH26 6
DDR0_CS_N<5> CH24 5
DDR0_CS_N<4> CK22 4
DDR0_CS3_N_CID<1> CC25 3
DDR0_CS2_N_CID<0> CF26 2
DDR0_CS_N<1> CH22 1
DDR0_CS_N<0> CD22 0
M_A_CS_N<9..0> OUT 52C8 53C7
DDR0_CID<2> CJ25 M_A_C<2> OUT 52C8 53C7
DDR0_ACT_N CK16 M_A_ACT_N OUT 52B8 53B8
DDR0_ALERT_N CD16 M_A_ALERT_N IN 52B8 53B8
DDR0_PAR CK20 M_A_PAR OUT 52B8 53B8
SYM 3 OF 18
PE201127-4355-01H
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HASWELL SOCKET 0 (3 OF 14)
wolfcreek_controller
DATE: Wed Jul 30 14:58:16 2014
DWG NO: <DRAWING>
REV: <REVISION>
wolfcreek_controller.cpm
DRAWN BY: <ENGINEER>
SHEET: 25OF360

J94 CON0003B41

55D4 54D4	BI	M_B_DQ<63..0>	63 DE39	DDR1_DQ<63>	DDR1_DQS_DP<17>	CW13 17	M_B_DQS_DP<17..0> BI 54D2 55D2
			62 DF38	DDR1_DQ<62>	DDR1_DQS_DP<16>	DD36 16	
			61 DB36	DDR1_DQ<61>	DDR1_DQS_DP<15>	CV36 15	
			60 DC35	DDR1_DQ<60>	DDR1_DQS_DP<14>	DA31 14	
			59 DA39	DDR1_DQ<59>	DDR1_DQS_DP<13>	CU29 13	
			58 DC39	DDR1_DQ<58>	DDR1_DQS_DP<12>	DC7 12	
			57 DF36	DDR1_DQ<57>	DDR1_DQS_DP<11>	CW3 11	
			56 DC37	DDR1_DQ<56>	DDR1_DQS_DP<10>	CH4 10	
			55 CT38	DDR1_DQ<55>	DDR1_DQS_DP<9>	BV2 9	
			54 CV38	DDR1_DQ<54>	DDR1_DQS_DP<8>	DB14 8	
			53 CT34	DDR1_DQ<53>	DDR1_DQS_DP<7>	DB38 7	
			52 CV34	DDR1_DQ<52>	DDR1_DQS_DP<6>	CR37 6	
			51 CR39	DDR1_DQ<51>	DDR1_DQS_DP<5>	DD32 5	
			50 CU39	DDR1_DQ<50>	DDR1_DQS_DP<4>	CT30 4	
			49 CR35	DDR1_DQ<49>	DDR1_DQS_DP<3>	DB10 3	
			48 CU35	DDR1_DQ<48>	DDR1_DQS_DP<2>	CT4 2	
			47 DE33	DDR1_DQ<47>	DDR1_DQS_DP<1>	CJ5 1	
			46 DA33	DDR1_DQ<46>	DDR1_DQS_DP<0>	BY4 0	
			45 CY28	DDR1_DQ<45>			M_B_DQS_DN<17..0> BI 54D2 55D2
			44 DB28	DDR1_DQ<44>	DDR1_DQS_DN<17>	CY14 17	
			43 DF34	DDR1_DQ<43>	DDR1_DQS_DN<16>	DE37 16	
			42 DC33	DDR1_DQ<42>	DDR1_DQS_DN<15>	CT36 15	
			41 DB30	DDR1_DQ<41>	DDR1_DQS_DN<14>	CY32 14	
			40 DA29	DDR1_DQ<40>	DDR1_DQS_DN<13>	CR29 13	
			39 CR31	DDR1_DQ<39>	DDR1_DQS_DN<12>	DD8 12	
			38 CU31	DDR1_DQ<38>	DDR1_DQS_DN<11>	CU3 11	
			37 CR27	DDR1_DQ<37>	DDR1_DQS_DN<10>	CG3 10	
			36 CU27	DDR1_DQ<36>	DDR1_DQS_DN<9>	BW1 9	
			35 CP32	DDR1_DQ<35>	DDR1_DQS_DN<8>	DA13 8	
			34 CT32	DDR1_DQ<34>	DDR1_DQS_DN<7>	DA37 7	
			33 CP28	DDR1_DQ<33>	DDR1_DQS_DN<6>	CU37 6	
			32 CT28	DDR1_DQ<32>	DDR1_DQS_DN<5>	DB32 5	
			31 DF10	DDR1_DQ<31>	DDR1_DQS_DN<4>	CV30 4	
			30 DE9	DDR1_DQ<30>	DDR1_DQS_DN<3>	DC9 3	
			29 CY6	DDR1_DQ<29>	DDR1_DQS_DN<2>	CV4 2	
			28 DA5	DDR1_DQ<28>	DDR1_DQS_DN<1>	CH6 1	
			27 DC11	DDR1_DQ<27>	DDR1_DQS_DN<0>	BW3 0	
			26 DE11	DDR1_DQ<26>			M_B_MA<17..0> OUT 54D7 55D7
			25 DB8	DDR1_DQ<25>	DDR1_MA<17>	CT24 17	
			24 DA7	DDR1_DQ<24>	DDR1_MA<16>	CY24 16	
			23 CR5	DDR1_DQ<23>	DDR1_MA<15>	CV24 15	
			22 CU5	DDR1_DQ<22>	DDR1_MA<14>	CN23 14	
			21 CP2	DDR1_DQ<21>	DDR1_MA<13>	CW25 13	
			20 CR1	DDR1_DQ<20>	DDR1_MA<12>	CW17 12	
			19 CP6	DDR1_DQ<19>	DDR1_MA<11>	CV18 11	
			18 CT6	DDR1_DQ<18>	DDR1_MA<10>	CR23 10	
			17 CV2	DDR1_DQ<17>	DDR1_MA<9>	CY18 9	
			16 CR3	DDR1_DQ<16>	DDR1_MA<8>	DA19 8	
			15 CL3	DDR1_DQ<15>	DDR1_MA<7>	CT18 7	
			14 CK6	DDR1_DQ<14>	DDR1_MA<6>	CW19 6	
			13 CF6	DDR1_DQ<13>	DDR1_MA<5>	CY20 5	
			12 CE5	DDR1_DQ<12>	DDR1_MA<4>	CR19 4	
			11 CM4	DDR1_DQ<11>	DDR1_MA<3>	CW21 3	
			10 CL5	DDR1_DQ<10>	DDR1_MA<2>	CV20 2	
			9 CF4	DDR1_DQ<9>	DDR1_MA<1>	DA21 1	
			8 CE3	DDR1_DQ<8>	DDR1_MA<0>	CY22 0	
			7 BY2	DDR1_DQ<7>			M_B_CKE<5..0> OUT 69D4 69D8 54C7 55C7
			6 CA1	DDR1_DQ<6>	DDR1_CKE<5>	DA15 5	
			5 BT2	DDR1_DQ<5>	DDR1_CKE<4>	CY16 4	
			4 BT4	DDR1_DQ<4>	DDR1_CKE<3>	DF16 3	
			3 CB4	DDR1_DQ<3>	DDR1_CKE<2>	DD16 2	
			2 CA3	DDR1_DQ<2>	DDR1_CKE<1>	DC17 1	
			1 BU1	DDR1_DQ<1>	DDR1_CKE<0>	DA17 0	
			0 BV4	DDR1_DQ<0>			M_B_ODT<5..0> OUT 54C7 55B7
55B7 54B7	BI	M_B_ECC<7..0>			DDR1_ODT<5>	DD26 5	
			7 DE13	DDR1_ECC<7>	DDR1_ODT<4>	DA25 4	
			6 DC13	DDR1_ECC<6>	DDR1_ODT<3>	DC25 3	
			5 CT14	DDR1_ECC<5>	DDR1_ODT<2>	DC23 2	
			4 CR13	DDR1_ECC<4>	DDR1_ODT<1>	DE25 1	
			3 DF14	DDR1_ECC<3>	DDR1_ODT<0>	DD22 0	
			2 DD14	DDR1_ECC<2>			M_B_CS_N<9..0> OUT 54C7 55C7
			1 CV14	DDR1_ECC<1>	DDR1_CS_N<9>	DF26 9	
			0 CU13	DDR1_ECC<0>	DDR1_CS_N<8>	DF24 8	
55C7 54C7	OUT	M_B_CLK_DP<3..0>			DDR1_CS7_N_CID<4>	CV26 7	
			3 DE19	DDR1_CLK_DP<3>	DDR1_CS6_N_CID<3>	CY26 6	
			2 DF20	DDR1_CLK_DP<2>	DDR1_CS_N<5>	DD24 5	
			1 DF18	DDR1_CLK_DP<1>	DDR1_CS_N<4>	DA23 4	
55C7 54C7	OUT	M_B_CLK_DN<3..0>	0 DE21	DDR1_CLK_DP<0>	DDR1_CS3_N_CID<1>	CP26 3	
			3 DC19	DDR1_CLK_DN<3>	DDR1_CS2_N_CID<0>	CT26 2	
			2 DD20	DDR1_CLK_DN<2>	DDR1_CS_N<1>	DE23 1	
			1 DD18	DDR1_CLK_DN<1>	DDR1_CS_N<0>	DF22 0	
			0 DC21	DDR1_CLK_DN<0>			
55C8 54C8	OUT	M_B_BG<1..0>			DDR1_CID<2>	CR25	M_B_C<2> OUT 54C7 55C7
			1 CP16	DDR1_BG<1>			
			0 CV16	DDR1_BG<0>	DDR1_ACT_N	CT16	M_B_ACT_N OUT 54B8 55B8
55C8 54C8	OUT	M_B_BA<1..0>			DDR1_ALERT_N	CR15	M_B_ALERT_N IN 54B8 55B8
			1 CV22	DDR1_BA<1>	DDR1_PAR	CT20	M_B_PAR OUT 54B8 55B8
			0 CW23	DDR1_BA<0>			

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PE201127-4355-01H

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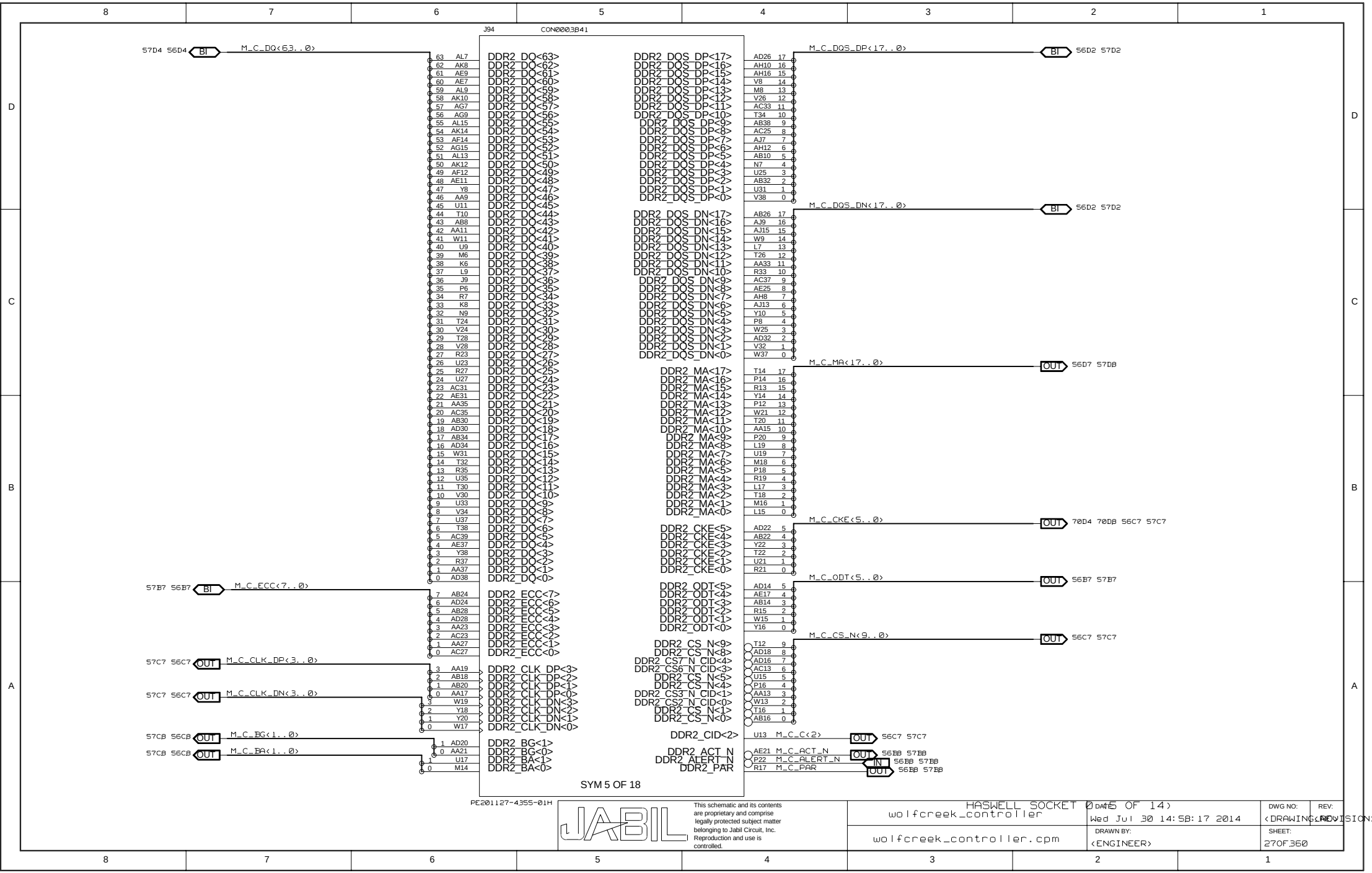
HASWELL SOCKET 0 (4 OF 14) wolfcreek_controller	DATE: Wed Jul 30 14:58:16 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 26OF360	


J94
CON00038A1
M_C_DQ<63..0>
M_C_DQS_DP<17..0>
M_C_DQS_DN<17..0>
M_C_MA<17..0>
M_C_CKE<5..0>
M_C_ODT<5..0>
M_C_CS_N<9..0>
M_C_ECC<7..0>
M_C_CLK_DP<3..0>
M_C_CLK_DN<3..0>
M_C_BG<1..0>
M_C_BA<1..0>
M_C_C<2>
M_C_ACT_N
M_C_ALERT_N
M_C_PAR
DDR2_CID<2>
DDR2_ACT_N
DDR2_ALERT_N
DDR2_PAR
SYM 5 OF 18
PE201127-4355-01H
JABIL
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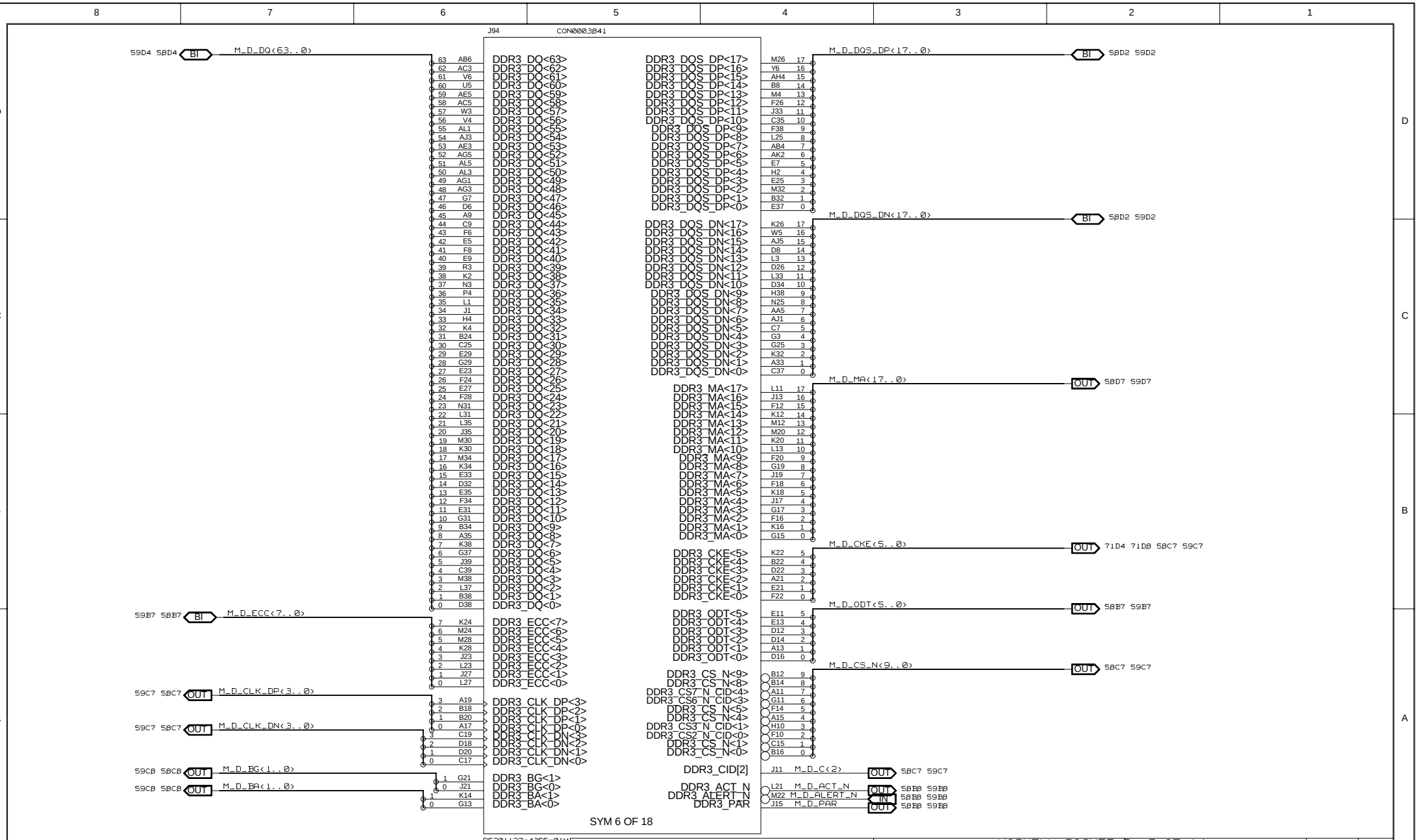
HASWELL SOCKET 0 (5 OF 14)
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Wed Jul 30 14:58:17 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 27OF360


J94
CON0003841
59D4 58D4 BI M_D_DQ<63..0>
DDR3_DQ<63> AB6
DDR3_DQ<62> AC3
DDR3_DQ<61> V6
DDR3_DQ<60> U5
DDR3_DQ<59> AE5
DDR3_DQ<58> AC5
DDR3_DQ<57> W3
DDR3_DQ<56> V4
DDR3_DQ<55> AL1
DDR3_DQ<54> AJ3
DDR3_DQ<53> AE3
DDR3_DQ<52> AG5
DDR3_DQ<51> AL5
DDR3_DQ<50> AL3
DDR3_DQ<49> AG1
DDR3_DQ<48> AG3
DDR3_DQ<47> G7
DDR3_DQ<46> D6
DDR3_DQ<45> A9
DDR3_DQ<44> C9
DDR3_DQ<43> F6
DDR3_DQ<42> E5
DDR3_DQ<41> F8
DDR3_DQ<40> E9
DDR3_DQ<39> R3
DDR3_DQ<38> K2
DDR3_DQ<37> N3
DDR3_DQ<36> P4
DDR3_DQ<35> L1
DDR3_DQ<34> J1
DDR3_DQ<33> H4
DDR3_DQ<32> K4
DDR3_DQ<31> B24
DDR3_DQ<30> C25
DDR3_DQ<29> E29
DDR3_DQ<28> G29
DDR3_DQ<27> E23
DDR3_DQ<26> F24
DDR3_DQ<25> E27
DDR3_DQ<24> F28
DDR3_DQ<23> N31
DDR3_DQ<22> L31
DDR3_DQ<21> L35
DDR3_DQ<20> J35
DDR3_DQ<19> M30
DDR3_DQ<18> K30
DDR3_DQ<17> M34
DDR3_DQ<16> K34
DDR3_DQ<15> E33
DDR3_DQ<14> D32
DDR3_DQ<13> E35
DDR3_DQ<12> F34
DDR3_DQ<11> E31
DDR3_DQ<10> G31
DDR3_DQ<9> B34
DDR3_DQ<8> A35
DDR3_DQ<7> K38
DDR3_DQ<6> G37
DDR3_DQ<5> J39
DDR3_DQ<4> C39
DDR3_DQ<3> M38
DDR3_DQ<2> L37
DDR3_DQ<1> B38
DDR3_DQ<0> D38
59B7 58B7 BI M_D_ECC<7..0>
DDR3_ECC<7> K24
DDR3_ECC<6> M24
DDR3_ECC<5> M28
DDR3_ECC<4> K28
DDR3_ECC<3> J23
DDR3_ECC<2> L23
DDR3_ECC<1> J27
DDR3_ECC<0> L27
59C7 58C7 OUT M_D_CLK_DP<3..0>
DDR3_CLK_DP<3> A19
DDR3_CLK_DP<2> B18
DDR3_CLK_DP<1> B20
DDR3_CLK_DP<0> A17
59C7 58C7 OUT M_D_CLK_DN<3..0>
DDR3_CLK_DN<3> C19
DDR3_CLK_DN<2> D18
DDR3_CLK_DN<1> D20
DDR3_CLK_DN<0> C17
59C8 58C8 OUT M_D_BG<1..0>
DDR3_BG<1> G21
DDR3_BG<0> J21
59C8 58C8 OUT M_D_BA<1..0>
DDR3_BA<1> K14
DDR3_BA<0> G13
DDR3_DQS_DP<17> M26 17
DDR3_DQS_DP<16> Y6 16
DDR3_DQS_DP<15> AH4 15
DDR3_DQS_DP<14> B8 14
DDR3_DQS_DP<13> M4 13
DDR3_DQS_DP<12> F26 12
DDR3_DQS_DP<11> J33 11
DDR3_DQS_DP<10> C35 10
DDR3_DQS_DP<9> F38 9
DDR3_DQS_DP<8> L25 8
DDR3_DQS_DP<7> AB4 7
DDR3_DQS_DP<6> AK2 6
DDR3_DQS_DP<5> E7 5
DDR3_DQS_DP<4> H2 4
DDR3_DQS_DP<3> E25 3
DDR3_DQS_DP<2> M32 2
DDR3_DQS_DP<1> B32 1
DDR3_DQS_DP<0> E37 0
M_D_DQS_DP<17..0> BI 58D2 59D2
DDR3_DQS_DN<17> K26 17
DDR3_DQS_DN<16> W5 16
DDR3_DQS_DN<15> AJ5 15
DDR3_DQS_DN<14> D8 14
DDR3_DQS_DN<13> L3 13
DDR3_DQS_DN<12> D26 12
DDR3_DQS_DN<11> L33 11
DDR3_DQS_DN<10> D34 10
DDR3_DQS_DN<9> H38 9
DDR3_DQS_DN<8> N25 8
DDR3_DQS_DN<7> AA5 7
DDR3_DQS_DN<6> AJ1 6
DDR3_DQS_DN<5> C7 5
DDR3_DQS_DN<4> G3 4
DDR3_DQS_DN<3> G25 3
DDR3_DQS_DN<2> K32 2
DDR3_DQS_DN<1> A33 1
DDR3_DQS_DN<0> C37 0
M_D_DQS_DN<17..0> BI 58D2 59D2
DDR3_MA<17> L11 17
DDR3_MA<16> J13 16
DDR3_MA<15> F12 15
DDR3_MA<14> K12 14
DDR3_MA<13> M12 13
DDR3_MA<12> M20 12
DDR3_MA<11> K20 11
DDR3_MA<10> L13 10
DDR3_MA<9> F20 9
DDR3_MA<8> G19 8
DDR3_MA<7> J19 7
DDR3_MA<6> F18 6
DDR3_MA<5> K18 5
DDR3_MA<4> J17 4
DDR3_MA<3> G17 3
DDR3_MA<2> F16 2
DDR3_MA<1> K16 1
DDR3_MA<0> G15 0
M_D_MA<17..0> OUT 58D7 59D7
DDR3_CKE<5> K22 5
DDR3_CKE<4> B22 4
DDR3_CKE<3> D22 3
DDR3_CKE<2> A21 2
DDR3_CKE<1> E21 1
DDR3_CKE<0> F22 0
M_D_CKE<5..0> OUT 71D4 71D8 58C7 59C7
DDR3_ODT<5> E11 5
DDR3_ODT<4> E13 4
DDR3_ODT<3> D12 3
DDR3_ODT<2> D14 2
DDR3_ODT<1> A13 1
DDR3_ODT<0> D16 0
M_D_ODT<5..0> OUT 58B7 59B7
DDR3_CS_N<9> B12 9
DDR3_CS_N<8> B14 8
DDR3_CS7_N_CID<4> A11 7
DDR3_CS6_N_CID<3> G11 6
DDR3_CS_N<5> F14 5
DDR3_CS_N<4> A15 4
DDR3_CS3_N_CID<1> H10 3
DDR3_CS2_N_CID<0> F10 2
DDR3_CS_N<1> C15 1
DDR3_CS_N<0> B16 0
M_D_CS_N<9..0> OUT 58C7 59C7
DDR3_CID[2] J11 M_D_C<2> OUT 58C7 59C7
DDR3_ACT_N L21 M_D_ACT_N OUT 58B8 59B8
DDR3_ALERT_N M22 M_D_ALERT_N IN 58B8 59B8
DDR3_PAR J15 M_D_PAR OUT 58B8 59B8
SYM 6 OF 18
PE201127-4355-01H
JABIL
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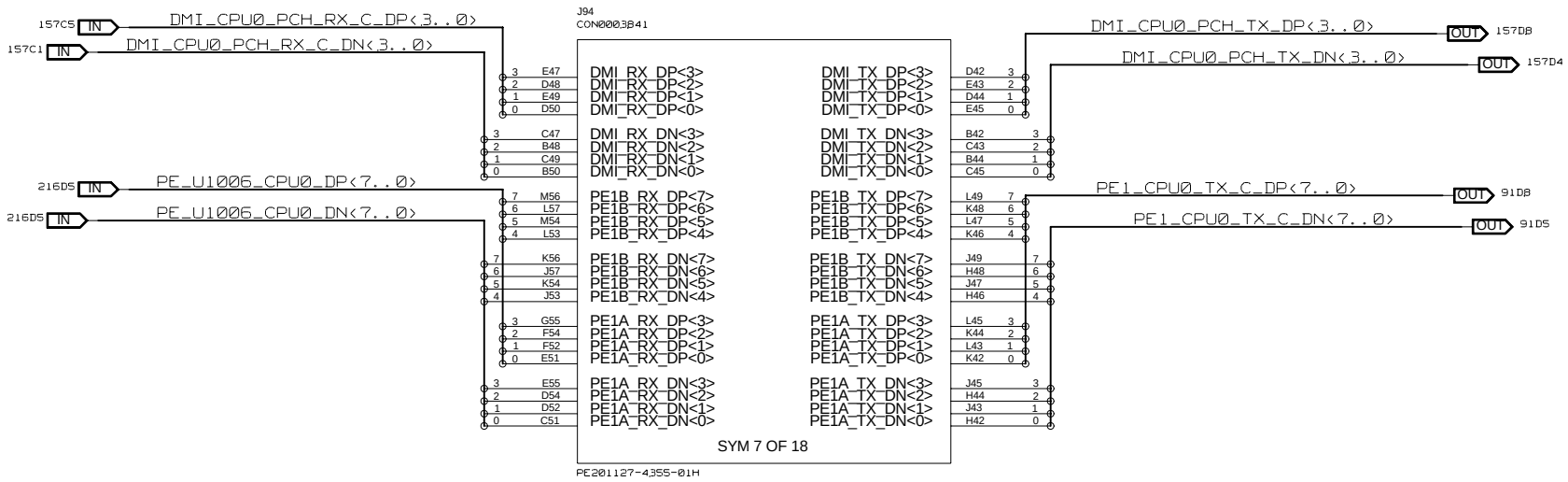
HASWELL SOCKET 0 (5 OF 14)
wolfcreek_controller
DATE: Wed Jul 30 14:58:17 2014
DWG NO: <DRAWING>
REV: <REVISION>
wolfcreek_controller.cpm
DRAWN BY: <ENGINEER>
SHEET: 28OF360



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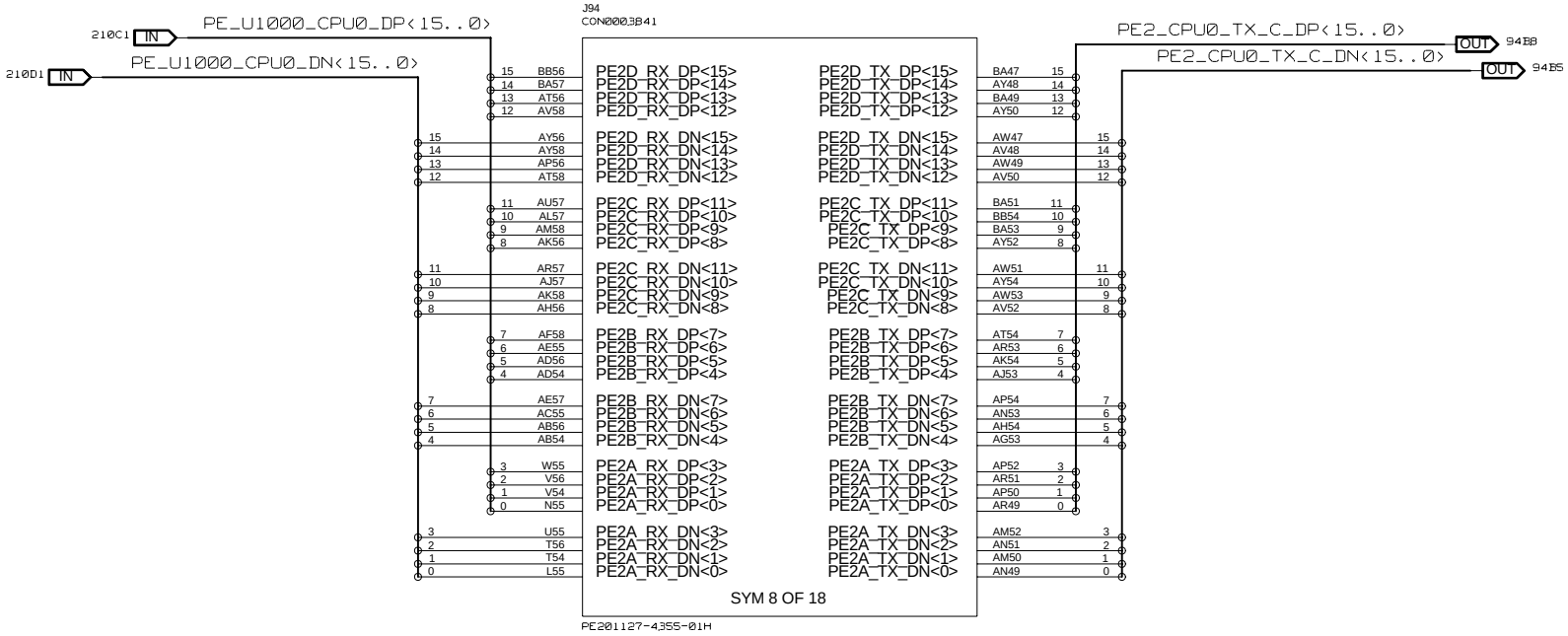
HASWELL SOCKET 0 (7 OF 14) wolfcreek_controller	DATE: Wed Jul 30 14:58:18 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 29OF360	



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HASWELL SOCKET 0 (8 OF 14)
wolfcreek_controller

DATE: Wed Jul 30 14:58:18 2014

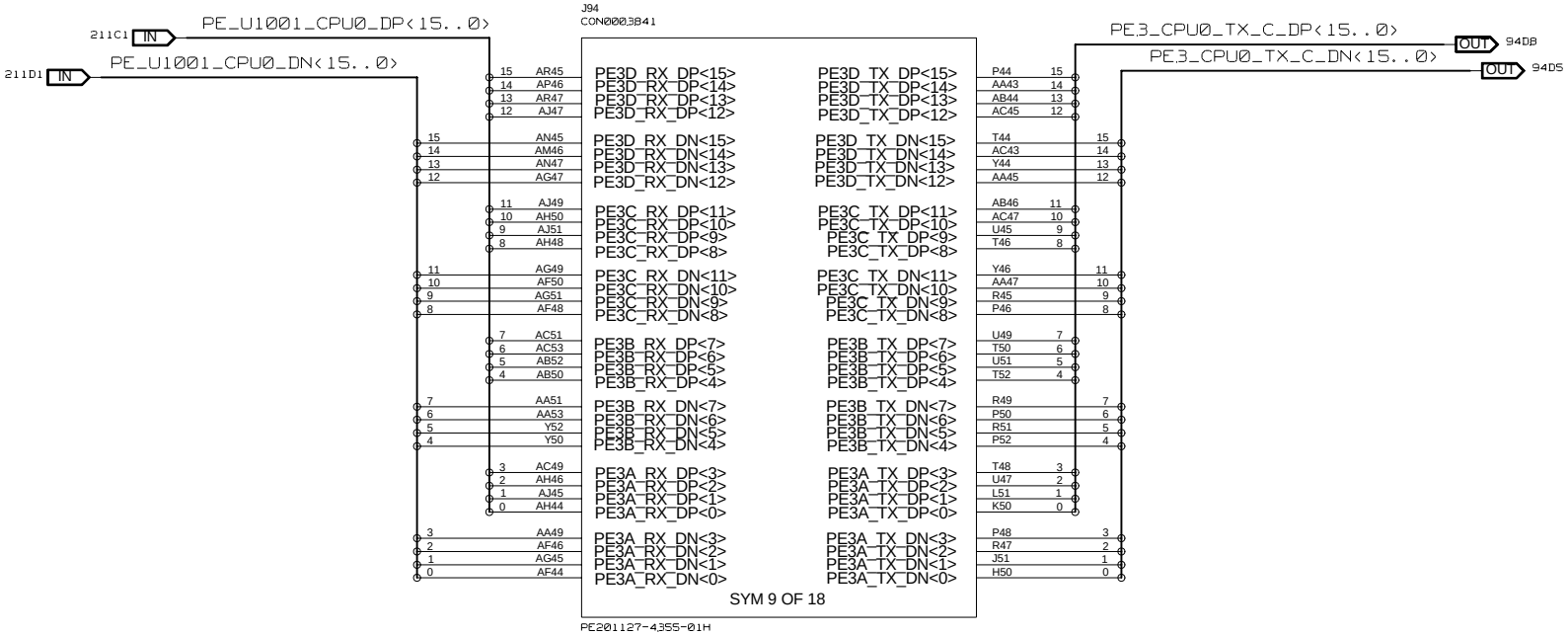
DWG NO: <DRAWING>

REV: <REVISION>

wolfcreek_controller.cpm

DRAWN BY: <ENGINEER>

SHEET: 30OF360



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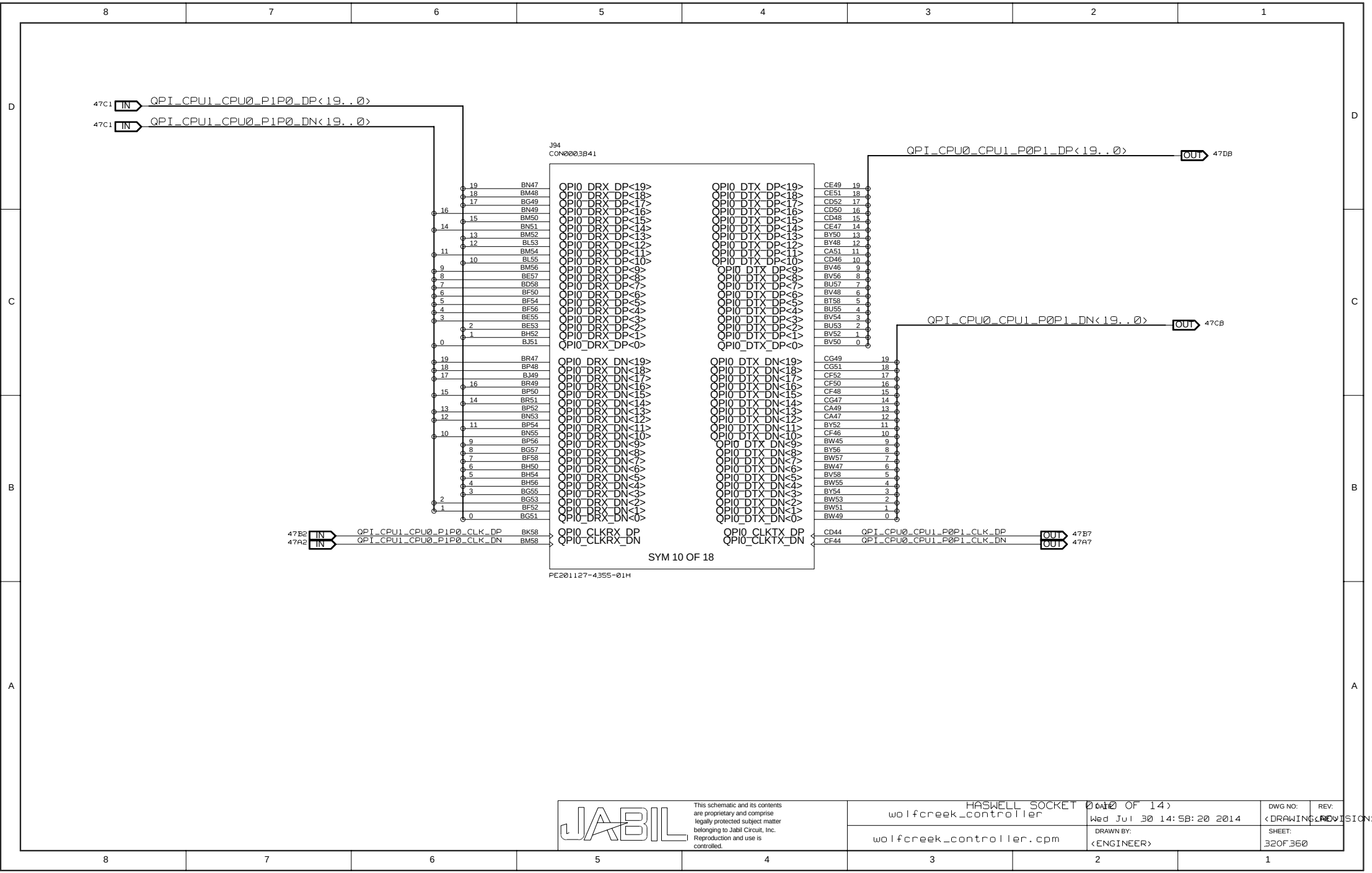
HASWELL SOCKET 0 (PAGE OF 14) wolfcreek_controller	DATE: Wed Jul 30 14:58:19 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 31 OF 360	


47C1 IN QPI_CPU1_CPU0_P1P0_DP<19..0>
47C1 IN QPI_CPU1_CPU0_P1P0_DN<19..0>
J94
CON000.3B41
QPI_CPU0_CPU1_P0P1_DP<19..0> OUT 47D8
QPI_CPU0_CPU1_P0P1_DN<19..0> OUT 47C8
QPI0_DRX_DP<19> BN47
QPI0_DRX_DP<18> BM48
QPI0_DRX_DP<17> BG49
QPI0_DRX_DP<16> BN49
QPI0_DRX_DP<15> BM50
QPI0_DRX_DP<14> BN51
QPI0_DRX_DP<13> BM52
QPI0_DRX_DP<12> BL53
QPI0_DRX_DP<11> BM54
QPI0_DRX_DP<10> BL55
QPI0_DRX_DP<9> BM56
QPI0_DRX_DP<8> BE57
QPI0_DRX_DP<7> BD58
QPI0_DRX_DP<6> BF50
QPI0_DRX_DP<5> BF54
QPI0_DRX_DP<4> BF56
QPI0_DRX_DP<3> BE55
QPI0_DRX_DP<2> BE53
QPI0_DRX_DP<1> BH52
QPI0_DRX_DP<0> BJ51
QPI0_DRX_DN<19> BR47
QPI0_DRX_DN<18> BP48
QPI0_DRX_DN<17> BJ49
QPI0_DRX_DN<16> BR49
QPI0_DRX_DN<15> BP50
QPI0_DRX_DN<14> BR51
QPI0_DRX_DN<13> BP52
QPI0_DRX_DN<12> BN53
QPI0_DRX_DN<11> BP54
QPI0_DRX_DN<10> BN55
QPI0_DRX_DN<9> BP56
QPI0_DRX_DN<8> BG57
QPI0_DRX_DN<7> BF58
QPI0_DRX_DN<6> BH50
QPI0_DRX_DN<5> BH54
QPI0_DRX_DN<4> BH56
QPI0_DRX_DN<3> BG55
QPI0_DRX_DN<2> BG53
QPI0_DRX_DN<1> BF52
QPI0_DRX_DN<0> BG51
47B2 IN QPI_CPU1_CPU0_P1P0_CLK_DP BK58
47A2 IN QPI_CPU1_CPU0_P1P0_CLK_DN BM58
QPI0_CLKRX_DP
QPI0_CLKRX_DN
QPI0_DTX_DP<19> CE49
QPI0_DTX_DP<18> CE51
QPI0_DTX_DP<17> CD52
QPI0_DTX_DP<16> CD50
QPI0_DTX_DP<15> CD48
QPI0_DTX_DP<14> CE47
QPI0_DTX_DP<13> BY50
QPI0_DTX_DP<12> BY48
QPI0_DTX_DP<11> CA51
QPI0_DTX_DP<10> CD46
QPI0_DTX_DP<9> BV46
QPI0_DTX_DP<8> BV56
QPI0_DTX_DP<7> BU57
QPI0_DTX_DP<6> BV48
QPI0_DTX_DP<5> BT58
QPI0_DTX_DP<4> BU55
QPI0_DTX_DP<3> BV54
QPI0_DTX_DP<2> BU53
QPI0_DTX_DP<1> BV52
QPI0_DTX_DP<0> BV50
QPI0_DTX_DN<19> CG49
QPI0_DTX_DN<18> CG51
QPI0_DTX_DN<17> CF52
QPI0_DTX_DN<16> CF50
QPI0_DTX_DN<15> CF48
QPI0_DTX_DN<14> CG47
QPI0_DTX_DN<13> CA49
QPI0_DTX_DN<12> CA47
QPI0_DTX_DN<11> BY52
QPI0_DTX_DN<10> CF46
QPI0_DTX_DN<9> BW45
QPI0_DTX_DN<8> BY56
QPI0_DTX_DN<7> BW57
QPI0_DTX_DN<6> BW47
QPI0_DTX_DN<5> BV58
QPI0_DTX_DN<4> BW55
QPI0_DTX_DN<3> BY54
QPI0_DTX_DN<2> BW53
QPI0_DTX_DN<1> BW51
QPI0_DTX_DN<0> BW49
QPI0_CLKTX_DP
QPI0_CLKTX_DN
CD44 QPI_CPU0_CPU1_P0P1_CLK_DP OUT 47B7
CF44 QPI_CPU0_CPU1_P0P1_CLK_DN OUT 47A7
SYM 10 OF 18
PE201127-4355-01H
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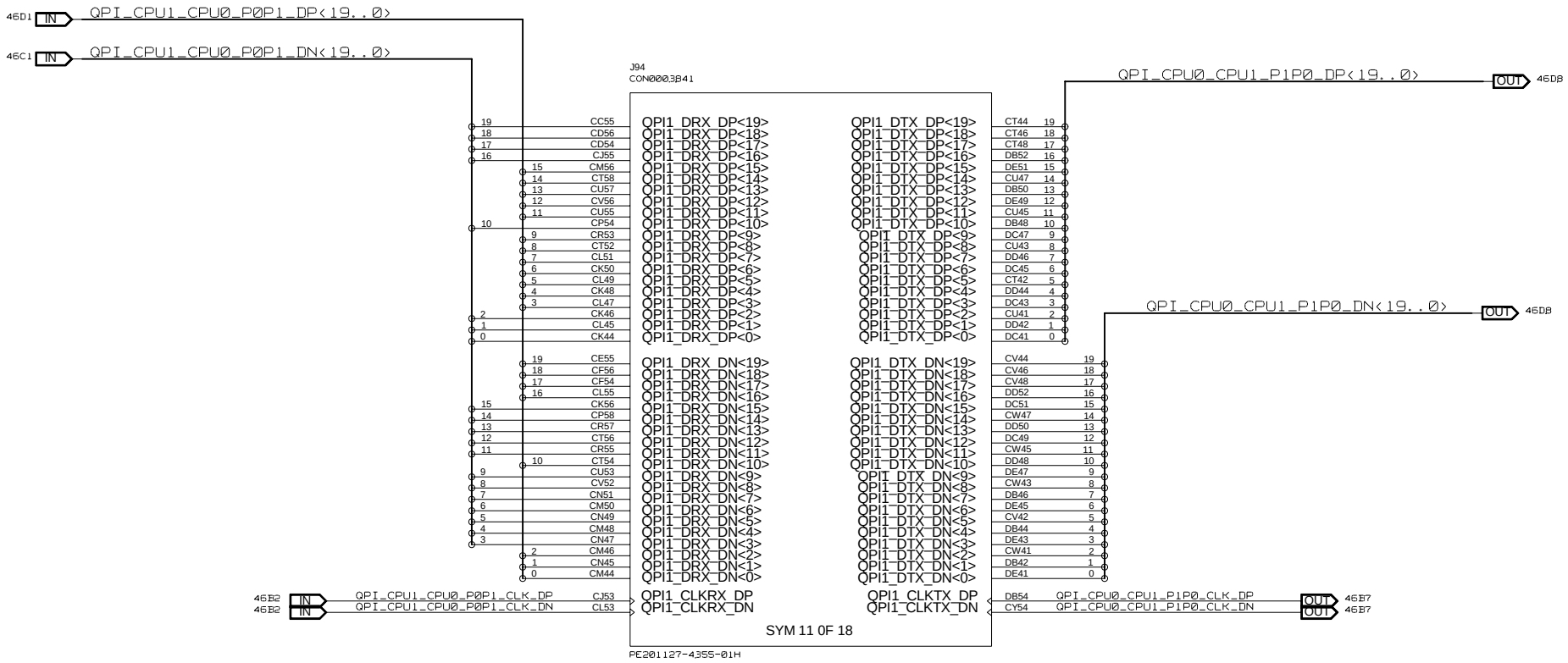
HASWELL SOCKET 0 (10 OF 14)
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Wed Jul 30 14:58:20 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING NO>
REV:
<REVISION>
SHEET:
32OF360



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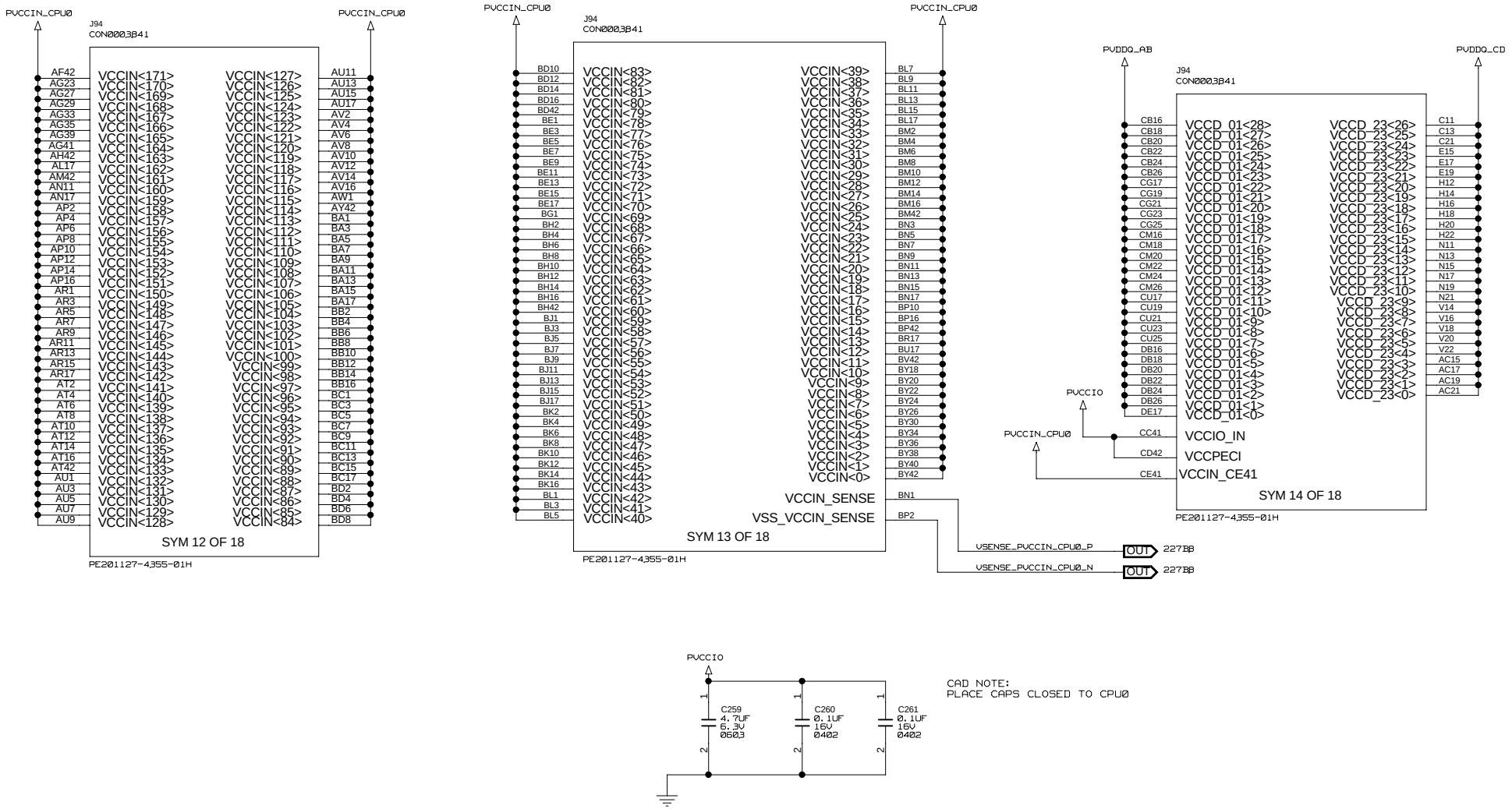
HASWELL SOCKET 0 (11 OF 14) wolfcreek_controller	DATE: Wed Jul 30 14:58:20 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 33OF360	



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HASWELL SOCKET 0 (12 OF 14)
wolfcreek_controller

DATE: Wed Jul 30 14:58:21 2014

DWG NO: <DRAWING NO>

REV: <REVISION>

wolfcreek_controller.cpm

DRAWN BY: <ENGINEER>

SHEET: 34OF36O

J94
CON0003B41

A23	VSS<630>	VSS<551>	M2
A37	VSS<629>	VSS<550>	M36
A39	VSS<628>	VSS<549>	M42
A41	VSS<627>	VSS<548>	M44
A43	VSS<626>	VSS<547>	M46
A45	VSS<625>	VSS<546>	M48
A47	VSS<624>	VSS<545>	M50
A49	VSS<623>	VSS<544>	M52
A5	VSS<622>	VSS<543>	N23
A51	VSS<621>	VSS<542>	N27
A7	VSS<620>	VSS<541>	N29
B10	VSS<619>	VSS<540>	N33
B36	VSS<618>	VSS<539>	N35
B40	VSS<617>	VSS<538>	N37
B52	VSS<616>	VSS<537>	N39
B6	VSS<615>	VSS<536>	N43
C33	VSS<614>	VSS<535>	N45
C5	VSS<613>	VSS<534>	N47
C55	VSS<612>	VSS<533>	N49
D10	VSS<611>	VSS<532>	N5
D24	VSS<610>	VSS<531>	N51
D36	VSS<609>	VSS<530>	N53
D4	VSS<608>	VSS<529>	P10
D40	VSS<607>	VSS<528>	P24
E1	VSS<606>	VSS<527>	P26
E3	VSS<605>	VSS<526>	P28
E39	VSS<604>	VSS<525>	P30
E41	VSS<603>	VSS<524>	P32
F2	VSS<602>	VSS<523>	P34
F30	VSS<601>	VSS<522>	P38
F32	VSS<600>	VSS<521>	P40
F36	VSS<599>	VSS<520>	P54
F4	VSS<598>	VSS<519>	P56
F42	VSS<597>	VSS<518>	R11
F44	VSS<596>	VSS<517>	R25
F48	VSS<595>	VSS<516>	R29
F50	VSS<594>	VSS<515>	R31
G1	VSS<593>	VSS<514>	R39
G23	VSS<592>	VSS<513>	R5
G27	VSS<591>	VSS<512>	R55
G33	VSS<590>	VSS<511>	R9
G35	VSS<589>	VSS<510>	T36
G39	VSS<588>	VSS<509>	T4
G41	VSS<587>	VSS<508>	T42
G45	VSS<586>	VSS<507>	T6
G47	VSS<585>	VSS<506>	T8
G49	VSS<584>	VSS<505>	U29
G5	VSS<583>	VSS<504>	U3
G51	VSS<582>	VSS<503>	U39
G53	VSS<581>	VSS<502>	U41
G57	VSS<580>	VSS<501>	U43
G9	VSS<579>	VSS<500>	U7
H24	VSS<578>	VSS<499>	V10
H26	VSS<577>	VSS<498>	V12
H28	VSS<576>	VSS<497>	V36
H30	VSS<575>	VSS<496>	V44
H32	VSS<574>	VSS<495>	V46
H34	VSS<573>	VSS<494>	V48
H36	VSS<572>	VSS<493>	V50
H40	VSS<571>	VSS<492>	V52
H54	VSS<570>	VSS<491>	W23
H6	VSS<569>	VSS<490>	W27
H8	VSS<568>	VSS<489>	W33
J25	VSS<567>	VSS<488>	W35
J29	VSS<566>	VSS<487>	W39
J3	VSS<565>	VSS<486>	W43
J31	VSS<564>	VSS<485>	W45
J37	VSS<563>	VSS<484>	W47
J5	VSS<562>	VSS<483>	W49
J55	VSS<561>	VSS<482>	W51
J7	VSS<560>	VSS<481>	W53
K10	VSS<559>	VSS<480>	W7
K36	VSS<558>	VSS<479>	Y12
K40	VSS<557>	VSS<478>	Y24
L29	VSS<556>	VSS<477>	Y26
L39	VSS<555>	VSS<476>	Y28
L41	VSS<554>	VSS<475>	Y30
L5	VSS<553>	VSS<474>	Y32
M10	VSS<552>	VSS<473>	Y34

SYM 15 OF 18

PE201127-4355-01H

J94
CON0003B41

Y36	VSS<472>	VSS<393>	AH6
Y4	VSS<471>	VSS<392>	AH14
Y42	VSS<470>	VSS<391>	AH58
Y56	VSS<469>	VSS<390>	AJ11
AA3	VSS<468>	VSS<389>	AJ17
AA25	VSS<467>	VSS<388>	AK4
AA29	VSS<466>	VSS<387>	AK6
AA7	VSS<465>	VSS<386>	AK16
AA31	VSS<464>	VSS<385>	AK42
AA39	VSS<463>	VSS<384>	AK44
AA55	VSS<462>	VSS<383>	AK46
AB12	VSS<461>	VSS<382>	AK48
AB36	VSS<460>	VSS<381>	AK50
AB40	VSS<459>	VSS<380>	AK52
AB42	VSS<458>	VSS<379>	AL11
AC7	VSS<457>	VSS<378>	AL43
AC9	VSS<456>	VSS<377>	AL45
AC11	VSS<455>	VSS<376>	AL47
AC29	VSS<454>	VSS<375>	AL49
AD4	VSS<453>	VSS<374>	AL51
AD8	VSS<452>	VSS<373>	AL53
AD6	VSS<451>	VSS<372>	AM2
AD10	VSS<450>	VSS<371>	AM4
AD12	VSS<449>	VSS<370>	AM6
AD36	VSS<448>	VSS<369>	AM8
AD40	VSS<447>	VSS<368>	AM10
AD42	VSS<446>	VSS<367>	AM12
AD44	VSS<445>	VSS<366>	AM14
AD46	VSS<444>	VSS<365>	AM16
AD48	VSS<443>	VSS<364>	AM56
AD50	VSS<442>	VSS<363>	AN1
AD52	VSS<441>	VSS<362>	AN3
AE13	VSS<440>	VSS<361>	AN5
AE15	VSS<439>	VSS<360>	AN7
AE19	VSS<438>	VSS<359>	AN9
AE23	VSS<437>	VSS<358>	AN13
AE27	VSS<436>	VSS<357>	AN15
AE29	VSS<435>	VSS<356>	AN55
AE33	VSS<434>	VSS<355>	AN57
AE35	VSS<433>	VSS<354>	AP42
AE39	VSS<432>	VSS<353>	AP44
AE41	VSS<431>	VSS<352>	AP58
AE43	VSS<430>	VSS<351>	AT44
AE47	VSS<429>	VSS<350>	AT46
AE49	VSS<428>	VSS<349>	AT48
AF10	VSS<427>	VSS<348>	AT50
AF16	VSS<426>	VSS<347>	AT52
AF18	VSS<425>	VSS<346>	AU45
AE51	VSS<424>	VSS<345>	AU47
AE53	VSS<423>	VSS<344>	AU49
AF2	VSS<422>	VSS<343>	AU51
AF4	VSS<421>	VSS<342>	AU53
AF6	VSS<420>	VSS<341>	AV42
AF8	VSS<419>	VSS<340>	AV54
AF20	VSS<418>	VSS<339>	AV56
AF22	VSS<417>	VSS<338>	AW11
AF24	VSS<416>	VSS<337>	AW13
AF26	VSS<415>	VSS<336>	AW15
AF28	VSS<414>	VSS<335>	AW17
AF30	VSS<413>	VSS<334>	AW3
AF32	VSS<412>	VSS<333>	AW5
AF34	VSS<411>	VSS<332>	AW7
AF36	VSS<410>	VSS<331>	AW9
AF38	VSS<409>	VSS<330>	AW55
AF40	VSS<408>	VSS<329>	AW57
AF54	VSS<407>	VSS<328>	AY2
AF56	VSS<406>	VSS<327>	AY4
AG11	VSS<405>	VSS<326>	AY6
AG13	VSS<404>	VSS<325>	AY8
AG17	VSS<403>	VSS<324>	AY10
AG19	VSS<402>	VSS<323>	AY12
AG21	VSS<401>	VSS<322>	AY14
AG25	VSS<400>	VSS<321>	AY16
AG31	VSS<399>	VSS<320>	AY44
AG37	VSS<398>	VSS<319>	BB42
AG43	VSS<397>	VSS<318>	BB46
AG55	VSS<396>	VSS<317>	BB50
AG57	VSS<395>	VSS<316>	BB58
AH2	VSS<394>	VSS<315>	BC45

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HASWELL SOCKET 0 (13 OF 14)
wolfcreek_controller

wolfcreek_controller.cpm

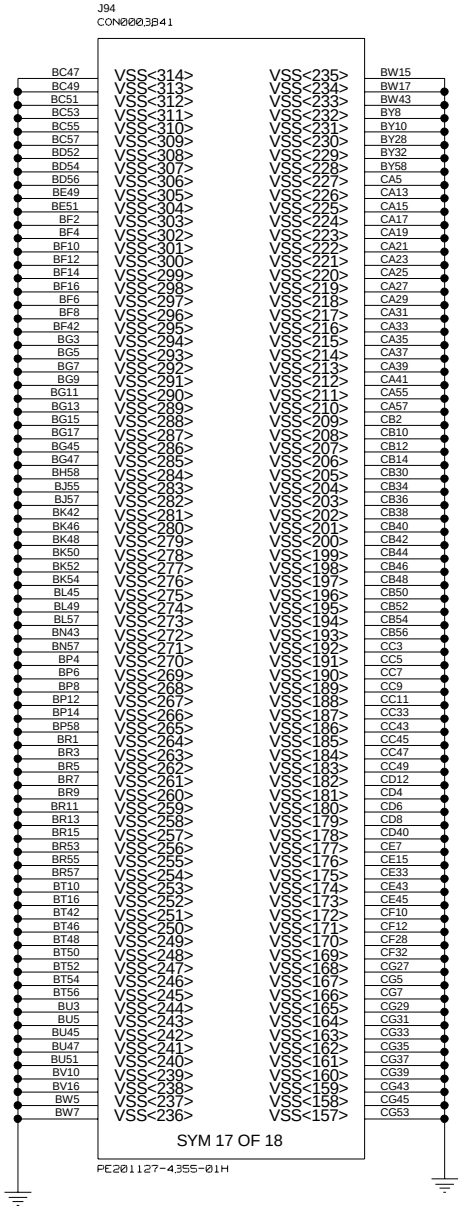
DATE: Wed Jul 30 14:58:21 2014

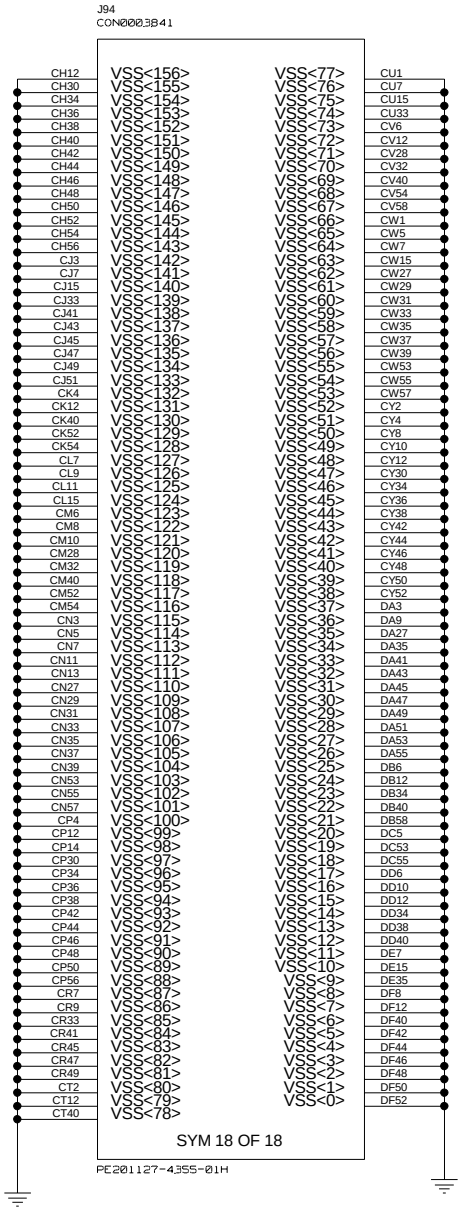
DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 35OF360





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HASWELL SOCKET (14 OF 14)	DATE: Wed Jul 30 14:58:22 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 36OF360	

PLACE R1045 CLOSED TO THE CPU.

J14
CON000,3B41

204E3 IN	CK_100M_CPU1_B0_DP	CL41	BCLK0_DP
204D3 IN	CK_100M_CPU1_B0_DN	CN41	BCLK0_DN
204D3 IN	CK_100M_CPU1_B1_DP	BA45	BCLK1_DP
204D3 IN	CK_100M_CPU1_B1_DN	AW45	BCLK1_DN
B4A8 IN	PWRGD_CPU1_EF_DRAM_G	CH16	DRAM_PWR_OK_C01
B4A8 IN	PWRGD_CPU1_GH_DRAM_G	W29	DRAM_PWR_OK_C23
7,3B8 7,3B4 72B8 72B4 63B8 62B8 61B8 60B8 OUT	M_EF_RESET_N	DC15	DDR_RESET_C01_N
75B8 75B3 74B8 74B4 67B8 66B8 65B8 64B8 OUT	M_GH_RESET_N	C23	DDR_RESET_C23_N
7BA8 B1B1 BI	H_CPU1_MEMEF_MEMHOT_G_N	CL33	MEM_HOT_C01_N
7BA8 B1A1 BI	H_CPU1_MEMGH_MEMHOT_G_N	P36	MEM_HOT_C23_N
37A7 OUT	M_EF_CPU_VREF	BY16	DDR01_VREF
	TP_EF_VREFDQ_1	CP40	RSVD_CP40
	TP_EF_VREFDQ_0	CF40	RSVD_CF40
37A4 OUT	M_GH_CPU_VREF	T40	DDR23_VREF
	TP_GH_VREFDQ_1	M40	RSVD_M40
	TP_GH_VREFDQ_0	R41	RSVD_R41
122B8 OUT	SMB_DDR_EF_SCL_G	CK42	DDR_SCL_C01
122B8 BI	SMB_DDR_EF_SDA_G	CM42	DDR_SDA_C01
122A8 OUT	SMB_DDR_GH_SCL_G	V40	DDR_SCL_C23
122A8 BI	SMB_DDR_GH_SDA_G	Y40	DDR_SDA_C23
37B7	SMB_PE_HP_CPU1_SCL_GTL	B46	PE_HP_SCL
37B7	SMB_PE_HP_CPU1_SDA_GTL	D46	PE_HP_SDA
127D6 127A8 IN	XDP_CPU_OBSFN_B_MBP7_G_N	AW43	BPM_N<7>
23C7 127A8 23C7 IN	XDP_CPU_OBSFN_B_MBP6_G_N	BA43	BPM_N<6>
127D6 127C6 127B7 IN	XDP_CPU1_OBSDATA_B_MBP5_G_N	BD46	BPM_N<5>
127C6 127B7 IN	XDP_CPU1_OBSDATA_B_MBP4_G_N	BE45	BPM_N<4>
127B7 127C6 IN	XDP_CPU1_OBSDATA_B_MBP3_G_N	BF46	BPM_N<3>
127B7 127C6 IN	XDP_CPU1_OBSDATA_B_MBP2_G_N	BE47	BPM_N<2>
23CB BI	XDP_CPU_MBP1_G_N	BB44	BPM_N<1>
23CB BI	XDP_CPU_MBP0_G_N	BC43	BPM_N<0>
12BA4 IN	XDP_CPU1_PREQ_G_N	CW49	PREQ_N
12BA8 OUT	XDP_CPU1_PRDY_G_N	CU49	PRDY_N
12BDB 12BB4 IN	XDP_CPU1_TDI_G	CF42	TDI
23B6 12BB3 127C6 IN	XDP_CPU_TCK_G	CA45	TCK
23B6 12BC3 127C3 IN	XDP_CPU_TMS_G	BY46	TMS
23B6 12BB3 127C3 IN	XDP_CPU_TRST_G_N	CV50	TRST_N

PWRGOOD	BJ53	PWRGD_CPU1_G	IN 84C7 IN 84C7
RESET_N	CR43	RST_CPU1_G_N	
EAR_N	CE53	PU_CPU1_EAR_G_N	IN 85A8
PMSYNC	K52	H_PM_SYNC_G	IN 97B2 23D2
PECI	CG55	PECI_CPU_G	BI 23D2 15BB7
SVIDDATA	AR43	PVCCIN_CPU1_SDIO	BI 23,5C2 23,7B2 23,9B2
SVIDCLK	AU43		
SVIDALERT_N	AN43	SVID_ALERT_CPU1_R1_G	1 220 R671 2 1% 0603 PVCCIN_CPU1_ALERT IN 23,9B2 23,5B2 23,7B2
CATERR_N	CC51	H_CPU1_CATERR_G_N	OUT 79C8
ERROR<2>_N	BB52	H_CPU1_ERR2_G_N	OUT 77A8
ERROR<1>_N	BB48	H_CPU1_ERR1_G_N	OUT 77A8
ERROR<0>_N	BD50	H_CPU1_ERR0_G_N	OUT 77B8
MSMI_N	H52	H_CPU1_MSMI_G_N	OUT 85B5
PROCHOT_N	BL51	H_CPU1_PROCHOT_G_N	BI 81C1 82C4 7BB8
THERMTRIP_N	BJ47	H_CPU1_THERMTRIP_G_N	OUT 85A4 7BB8
SAFE_MODE_BOOT	BK56	PU_CPU1_SAFE_MODE_BOOT	IN 76A6
FRMAGENT	Y48	PU_CPU1_FRMAGENT	IN 76B6
BMCINIT	AM48	PU_CPU1_BMCINIT	IN 76B6
TXT_AGENT	AH52	PU_CPU1_TXT_AGENT	IN 76B4
TXT_PLTEN	AF52	PD_CPU1_TXT_PLTEN	IN 76B4
BIST_ENABLE	AJ43	PD_CPU1_BIST_ENABLE	IN 76A4
PM_FAST_WAKE_N	AV44	H_CPU1_FAST_WAKE_G_N	IN 85D5
SKTOCC_N	BU49	FM_CPU1_SKTOCC_LVT3_N	OUT 85C4 12BA1 165AB 166C6
SOCKET_ID<1>	CC53	PU_CPU1_SOCKET_ID_1	OUT 76A6
SOCKET_ID<0>	CP52	PU_CPU1_SOCKET_ID_0	OUT 76A6
PROC_ID	AB48	FM_CPU1_BDX_PRSNT_LVT3_N	OUT 85C2 135B2 166C6
RSVD_C53	C53	TP_G_CPU1_OVERCLK	
RSVD_CR51	CR51	NC_CPU1_LGSPARE_5	
RSVD_AV46	AV46	NC_CPU1_LGSPARE_4	
RSVD_AY46	AY46	NC_CPU1_LGSPARE_3	
RSVD_AJ55	AJ55	NC_CPU1_LGSPARE_1	
RSVD_BD48	BD48	NC_CPU1_LGSPARE_0	
TDO	CG41	XDP_CPU1_TDO_G	OUT 12BC5

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R1045: SVID_CLK_R_CPU1 1 — 5.11 — 2 PVCCIN_CPU1_SCLK OUT 23,5B2 23,7B2 23,9B2 (1% 0402)

PVCCIO: R663 100 1% 0402; R664 100 1% 0402

PVCCIO: R1450 4.7K 1% 0402 — 1 SMB_PE_HP_CPU1_SCL_GTL 2 — 37C6; R1451 4.7K 1% 0402 — 1 SMB_PE_HP_CPU1_SDA_GTL 2 — 37C6

PVDDQ_EF: R667 1K 1% 0402; 37D7 IN M_EF_CPU_VREF 1 — R665 5% 0402 — 2 M_EF_VREF OUT 60A8 61A8 62A8 63A8; C669 0.01UF 25V 0402; R666 1K 1% 0402

PVDDQ_GH: R670 1K 1% 0402; 37C7 IN M_GH_CPU_VREF 1 — R668 5% 0402 — 2 M_GH_VREF OUT 64A8 65A8 66A8 67A8; C670 0.01UF 25V 0402; R669 1K 1% 0402

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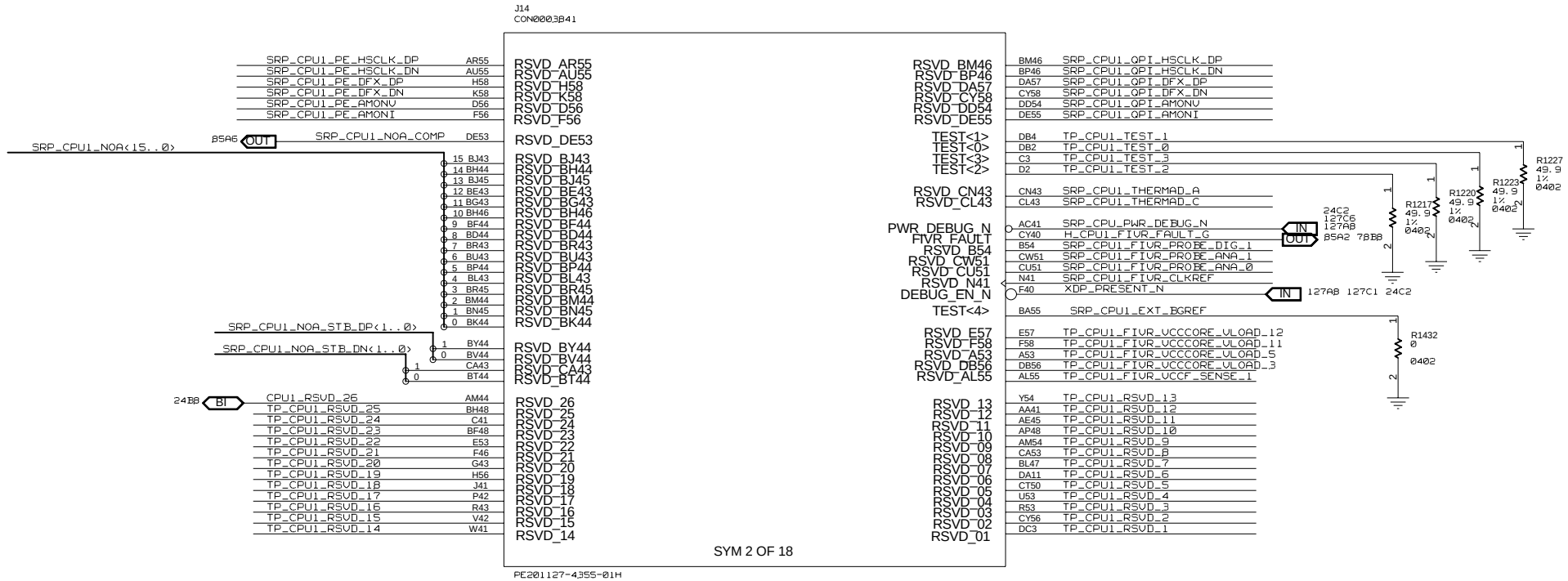
HASWELL SOCKET
wolfcreek_controller
wolfcreek_controller.cpm

PAGE (1 OF 14)
DATE: Wed Jul 30 14:58:23 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 37OF360



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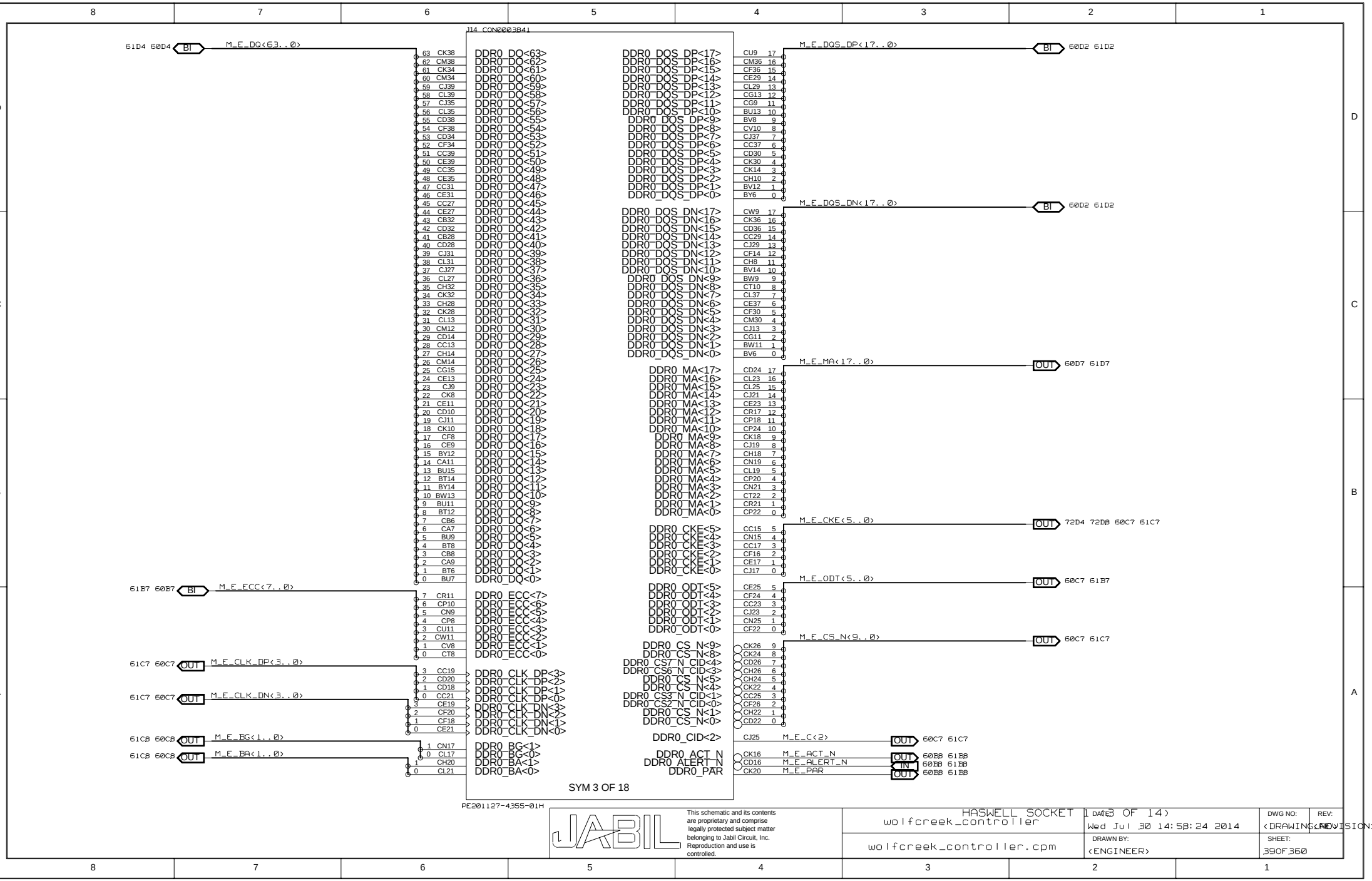
HASWELL SOCKET (2 OF 14)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:23 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 38 OF 360


J14 CON0003B41
61D4 60D4 BI M_E_DQ<63..0>
63 CK38 DDR0_DQ<63>
62 CM38 DDR0_DQ<62>
61 CK34 DDR0_DQ<61>
60 CM34 DDR0_DQ<60>
59 CJ39 DDR0_DQ<59>
58 CL39 DDR0_DQ<58>
57 CJ35 DDR0_DQ<57>
56 CL35 DDR0_DQ<56>
55 CD38 DDR0_DQ<55>
54 CF38 DDR0_DQ<54>
53 CD34 DDR0_DQ<53>
52 CF34 DDR0_DQ<52>
51 CC39 DDR0_DQ<51>
50 CE39 DDR0_DQ<50>
49 CC35 DDR0_DQ<49>
48 CE35 DDR0_DQ<48>
47 CC31 DDR0_DQ<47>
46 CE31 DDR0_DQ<46>
45 CC27 DDR0_DQ<45>
44 CE27 DDR0_DQ<44>
43 CB32 DDR0_DQ<43>
42 CD32 DDR0_DQ<42>
41 CB28 DDR0_DQ<41>
40 CD28 DDR0_DQ<40>
39 CJ31 DDR0_DQ<39>
38 CL31 DDR0_DQ<38>
37 CJ27 DDR0_DQ<37>
36 CL27 DDR0_DQ<36>
35 CH32 DDR0_DQ<35>
34 CK32 DDR0_DQ<34>
33 CH28 DDR0_DQ<33>
32 CK28 DDR0_DQ<32>
31 CL13 DDR0_DQ<31>
30 CM12 DDR0_DQ<30>
29 CD14 DDR0_DQ<29>
28 CC13 DDR0_DQ<28>
27 CH14 DDR0_DQ<27>
26 CM14 DDR0_DQ<26>
25 CG15 DDR0_DQ<25>
24 CE13 DDR0_DQ<24>
23 CJ9 DDR0_DQ<23>
22 CK8 DDR0_DQ<22>
21 CE11 DDR0_DQ<21>
20 CD10 DDR0_DQ<20>
19 CJ11 DDR0_DQ<19>
18 CK10 DDR0_DQ<18>
17 CF8 DDR0_DQ<17>
16 CE9 DDR0_DQ<16>
15 BY12 DDR0_DQ<15>
14 CA11 DDR0_DQ<14>
13 BU15 DDR0_DQ<13>
12 BT14 DDR0_DQ<12>
11 BY14 DDR0_DQ<11>
10 BW13 DDR0_DQ<10>
9 BU11 DDR0_DQ<9>
8 BT12 DDR0_DQ<8>
7 CB6 DDR0_DQ<7>
6 CA7 DDR0_DQ<6>
5 BU9 DDR0_DQ<5>
4 BT8 DDR0_DQ<4>
3 CB8 DDR0_DQ<3>
2 CA9 DDR0_DQ<2>
1 BT6 DDR0_DQ<1>
0 BU7 DDR0_DQ<0>
61B7 60B7 BI M_E_ECC<7..0>
7 CR11 DDR0_ECC<7>
6 CP10 DDR0_ECC<6>
5 CN9 DDR0_ECC<5>
4 CP8 DDR0_ECC<4>
3 CU11 DDR0_ECC<3>
2 CW11 DDR0_ECC<2>
1 CV8 DDR0_ECC<1>
0 CT8 DDR0_ECC<0>
61C7 60C7 OUT M_E_CLK_DP<3..0>
3 CC19 DDR0_CLK_DP<3>
2 CD20 DDR0_CLK_DP<2>
1 CD18 DDR0_CLK_DP<1>
0 CC21 DDR0_CLK_DP<0>
61C7 60C7 OUT M_E_CLK_DN<3..0>
3 CE19 DDR0_CLK_DN<3>
2 CF20 DDR0_CLK_DN<2>
1 CF18 DDR0_CLK_DN<1>
0 CE21 DDR0_CLK_DN<0>
61C8 60C8 OUT M_E_BG<1..0>
1 CN17 DDR0_BG<1>
0 CL17 DDR0_BG<0>
61C8 60C8 OUT M_E_BA<1..0>
1 CH20 DDR0_BA<1>
0 CL21 DDR0_BA<0>
DDR0_DQS_DP<17> CU9 17
DDR0_DQS_DP<16> CM36 16
DDR0_DQS_DP<15> CF36 15
DDR0_DQS_DP<14> CE29 14
DDR0_DQS_DP<13> CL29 13
DDR0_DQS_DP<12> CG13 12
DDR0_DQS_DP<11> CG9 11
DDR0_DQS_DP<10> BU13 10
DDR0_DQS_DP<9> BV8 9
DDR0_DQS_DP<8> CV10 8
DDR0_DQS_DP<7> CJ37 7
DDR0_DQS_DP<6> CC37 6
DDR0_DQS_DP<5> CD30 5
DDR0_DQS_DP<4> CK30 4
DDR0_DQS_DP<3> CK14 3
DDR0_DQS_DP<2> CH10 2
DDR0_DQS_DP<1> BV12 1
DDR0_DQS_DP<0> BV6 0
M_E_DQS_DP<17..0> BI 60D2 61D2
DDR0_DQS_DN<17> CW9 17
DDR0_DQS_DN<16> CK36 16
DDR0_DQS_DN<15> CD36 15
DDR0_DQS_DN<14> CC29 14
DDR0_DQS_DN<13> CJ29 13
DDR0_DQS_DN<12> CF14 12
DDR0_DQS_DN<11> CH8 11
DDR0_DQS_DN<10> BV14 10
DDR0_DQS_DN<9> BW9 9
DDR0_DQS_DN<8> CT10 8
DDR0_DQS_DN<7> CL37 7
DDR0_DQS_DN<6> CE37 6
DDR0_DQS_DN<5> CF30 5
DDR0_DQS_DN<4> CM30 4
DDR0_DQS_DN<3> CJ13 3
DDR0_DQS_DN<2> CG11 2
DDR0_DQS_DN<1> BW11 1
DDR0_DQS_DN<0> BV6 0
M_E_DQS_DN<17..0> BI 60D2 61D2
DDR0_MA<17> CD24 17
DDR0_MA<16> CL23 16
DDR0_MA<15> CL25 15
DDR0_MA<14> CJ21 14
DDR0_MA<13> CE23 13
DDR0_MA<12> CR17 12
DDR0_MA<11> CP18 11
DDR0_MA<10> CP24 10
DDR0_MA<9> CK18 9
DDR0_MA<8> CJ19 8
DDR0_MA<7> CH18 7
DDR0_MA<6> CN19 6
DDR0_MA<5> CL19 5
DDR0_MA<4> CP20 4
DDR0_MA<3> CN21 3
DDR0_MA<2> CT22 2
DDR0_MA<1> CR21 1
DDR0_MA<0> CP22 0
M_E_MA<17..0> OUT 60D7 61D7
DDR0_CKE<5> CC15 5
DDR0_CKE<4> CN15 4
DDR0_CKE<3> CC17 3
DDR0_CKE<2> CF16 2
DDR0_CKE<1> CE17 1
DDR0_CKE<0> CJ17 0
M_E_CKE<5..0> OUT 72D4 72D8 60C7 61C7
DDR0_ODT<5> CE25 5
DDR0_ODT<4> CF24 4
DDR0_ODT<3> CC23 3
DDR0_ODT<2> CJ23 2
DDR0_ODT<1> CN25 1
DDR0_ODT<0> CF22 0
M_E_ODT<5..0> OUT 60C7 61B7
DDR0_CS_N<9> CK26 9
DDR0_CS_N<8> CK24 8
DDR0_CS7_N_CID<4> CD26 7
DDR0_CS6_N_CID<3> CH26 6
DDR0_CS_N<5> CH24 5
DDR0_CS_N<4> CK22 4
DDR0_CS3_N_CID<1> CC25 3
DDR0_CS2_N_CID<0> CF26 2
DDR0_CS_N<1> CH22 1
DDR0_CS_N<0> CD22 0
M_E_CS_N<9..0> OUT 60C7 61C7
DDR0_CID<2> CJ25 M_E_C<2> OUT 60C7 61C7
DDR0_ACT_N CK16 M_E_ACT_N OUT 60B8 61B8
DDR0_ALERT_N CD16 M_E_ALERT_N IN 60B8 61B8
DDR0_PAR CK20 M_E_PAR OUT 60B8 61B8
SYM 3 OF 18
PE201127-4355-01H
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HASWELL SOCKET (3 OF 14)
wolfcreek_controller
DATE: Wed Jul 30 14:58:24 2014
DWG NO: <DRAWING>
REV: <REVISION>
wolfcreek_controller.cpm
DRAWN BY: <ENGINEER>
SHEET: 39OF360

J14 CON000384 1

63	DE39	DDR1_DQ<63>	DDR1_DQS_DP<17>	CW13	17	M_F_DQS_DP<17..0>	BI 62D2 63D2
62	DF38	DDR1_DQ<62>	DDR1_DQS_DP<16>	DD36	16		
61	DB36	DDR1_DQ<61>	DDR1_DQS_DP<15>	CV36	15		
60	DC35	DDR1_DQ<60>	DDR1_DQS_DP<14>	DA31	14		
59	DA39	DDR1_DQ<59>	DDR1_DQS_DP<13>	CU29	13		
58	DC39	DDR1_DQ<58>	DDR1_DQS_DP<12>	DC7	12		
57	DF36	DDR1_DQ<57>	DDR1_DQS_DP<11>	CW3	11		
56	DC37	DDR1_DQ<56>	DDR1_DQS_DP<10>	CH4	10		
55	CT38	DDR1_DQ<55>	DDR1_DQS_DP<9>	BV2	9		
54	CV38	DDR1_DQ<54>	DDR1_DQS_DP<8>	DB14	8		
53	CT34	DDR1_DQ<53>	DDR1_DQS_DP<7>	DB38	7		
52	CV34	DDR1_DQ<52>	DDR1_DQS_DP<6>	CR37	6		
51	CR39	DDR1_DQ<51>	DDR1_DQS_DP<5>	DD32	5		
50	CU39	DDR1_DQ<50>	DDR1_DQS_DP<4>	CT30	4		
49	CR35	DDR1_DQ<49>	DDR1_DQS_DP<3>	DB10	3		
48	CU35	DDR1_DQ<48>	DDR1_DQS_DP<2>	CT4	2		
47	DE33	DDR1_DQ<47>	DDR1_DQS_DP<1>	CJ5	1		
46	DA33	DDR1_DQ<46>	DDR1_DQS_DP<0>	BY4	0		
45	CY28	DDR1_DQ<45>				M_F_DQS_DN<17..0>	BI 62D2 63D2
44	DB28	DDR1_DQ<44>	DDR1_DQS_DN<17>	CY14	17		
43	DF34	DDR1_DQ<43>	DDR1_DQS_DN<16>	DE37	16		
42	DC33	DDR1_DQ<42>	DDR1_DQS_DN<15>	CT36	15		
41	DB30	DDR1_DQ<41>	DDR1_DQS_DN<14>	CY32	14		
40	DA29	DDR1_DQ<40>	DDR1_DQS_DN<13>	CR29	13		
39	CR31	DDR1_DQ<39>	DDR1_DQS_DN<12>	DD8	12		
38	CU31	DDR1_DQ<38>	DDR1_DQS_DN<11>	CU3	11		
37	CR27	DDR1_DQ<37>	DDR1_DQS_DN<10>	CG3	10		
36	CU27	DDR1_DQ<36>	DDR1_DQS_DN<9>	BW1	9		
35	CP32	DDR1_DQ<35>	DDR1_DQS_DN<8>	DA13	8		
34	CT32	DDR1_DQ<34>	DDR1_DQS_DN<7>	DA37	7		
33	CP28	DDR1_DQ<33>	DDR1_DQS_DN<6>	CU37	6		
32	CT28	DDR1_DQ<32>	DDR1_DQS_DN<5>	DB32	5		
31	DF10	DDR1_DQ<31>	DDR1_DQS_DN<4>	CV30	4		
30	DE9	DDR1_DQ<30>	DDR1_DQS_DN<3>	DC9	3		
29	CY6	DDR1_DQ<29>	DDR1_DQS_DN<2>	CV4	2		
28	DA5	DDR1_DQ<28>	DDR1_DQS_DN<1>	CH6	1		
27	DC11	DDR1_DQ<27>	DDR1_DQS_DN<0>	BW3	0		
26	DE11	DDR1_DQ<26>				M_F_MA<17..0>	OUT 62D7 63D7
25	DB8	DDR1_DQ<25>	DDR1_MA<17>	CT24	17		
24	DA7	DDR1_DQ<24>	DDR1_MA<16>	CY24	16		
23	CR5	DDR1_DQ<23>	DDR1_MA<15>	CV24	15		
22	CU5	DDR1_DQ<22>	DDR1_MA<14>	CN23	14		
21	CP2	DDR1_DQ<21>	DDR1_MA<13>	CW25	13		
20	CR1	DDR1_DQ<20>	DDR1_MA<12>	CW17	12		
19	CP6	DDR1_DQ<19>	DDR1_MA<11>	CV18	11		
18	CT6	DDR1_DQ<18>	DDR1_MA<10>	CR23	10		
17	CV2	DDR1_DQ<17>	DDR1_MA<9>	CY18	9		
16	CR3	DDR1_DQ<16>	DDR1_MA<8>	DA19	8		
15	CL3	DDR1_DQ<15>	DDR1_MA<7>	CT18	7		
14	CK6	DDR1_DQ<14>	DDR1_MA<6>	CW19	6		
13	CF6	DDR1_DQ<13>	DDR1_MA<5>	CY20	5		
12	CE5	DDR1_DQ<12>	DDR1_MA<4>	CR19	4		
11	CM4	DDR1_DQ<11>	DDR1_MA<3>	CW21	3		
10	CL5	DDR1_DQ<10>	DDR1_MA<2>	CV20	2		
9	CF4	DDR1_DQ<9>	DDR1_MA<1>	DA21	1		
8	CE3	DDR1_DQ<8>	DDR1_MA<0>	CY22	0		
7	BY2	DDR1_DQ<7>				M_F_CKE<5..0>	OUT 73D4 73D8 62C7 63C7
6	CA1	DDR1_DQ<6>	DDR1_CKE<5>	DA15	5		
5	BT2	DDR1_DQ<5>	DDR1_CKE<4>	CY16	4		
4	BT4	DDR1_DQ<4>	DDR1_CKE<3>	DF16	3		
3	CB4	DDR1_DQ<3>	DDR1_CKE<2>	DD16	2		
2	CA3	DDR1_DQ<2>	DDR1_CKE<1>	DC17	1		
1	BU1	DDR1_DQ<1>	DDR1_CKE<0>	DA17	0		
0	BV4	DDR1_DQ<0>				M_F_ODT<5..0>	OUT 62C7 63B7
			DDR1_ODT<5>	DD26	5		
7	DE13	DDR1_ECC<7>	DDR1_ODT<4>	DA25	4		
6	DC13	DDR1_ECC<6>	DDR1_ODT<3>	DC25	3		
5	CT14	DDR1_ECC<5>	DDR1_ODT<2>	DC23	2		
4	CR13	DDR1_ECC<4>	DDR1_ODT<1>	DE25	1		
3	DF14	DDR1_ECC<3>	DDR1_ODT<0>	DD22	0		
2	DD14	DDR1_ECC<2>				M_F_CS_N<9..0>	OUT 62C7 63C7
1	CV14	DDR1_ECC<1>	DDR1_CS_N<9>	DF26	9		
0	CU13	DDR1_ECC<0>	DDR1_CS_N<8>	DF24	8		
			DDR1_CS7_N_CID<4>	CV26	7		
3	DE19	DDR1_CLK_DP<3>	DDR1_CS6_N_CID<3>	CY26	6		
2	DF20	DDR1_CLK_DP<2>	DDR1_CS_N<5>	DD24	5		
1	DF18	DDR1_CLK_DP<1>	DDR1_CS_N<4>	DA23	4		
0	DE21	DDR1_CLK_DP<0>	DDR1_CS3_N_CID<1>	CP26	3		
3	DC19	DDR1_CLK_DN<3>	DDR1_CS2_N_CID<0>	CT26	2		
2	DD20	DDR1_CLK_DN<2>	DDR1_CS_N<1>	DE23	1		
1	DD18	DDR1_CLK_DN<1>	DDR1_CS_N<0>	DF22	0		
0	DC21	DDR1_CLK_DN<0>					
1	CP16	DDR1_BG<1>	DDR1_CID<2>	CR25		M_F_C<2>	OUT 62C7 63C7
0	CV16	DDR1_BG<0>	DDR1_ACT_N	CT16		M_F_ACT_N	OUT 62B8 63B8
1	CV22	DDR1_BA<1>	DDR1_ALERT_N	CR15		M_F_ALERT_N	IN 62B8 63B8
0	CW23	DDR1_BA<0>	DDR1_PAR	CT20		M_F_PAR	OUT 62B8 63B8

63D4 62D4 BI M_F_DQ<63..0>

63B7 62B7 BI M_F_ECC<7..0>

63C7 62C7 OUT M_F_CLK_DP<3..0>

63C7 62C7 OUT M_F_CLK_DN<3..0>

63C8 62C8 OUT M_F_BG<1..0>

63C8 62C8 OUT M_F_BA<1..0>

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HASWELL SOCKET (4 OF 14)	DATE: Wed Jul 30 14:58:24 2014	DWG NO: <DRAWING>	REV: <REVISION>
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J14 CON00038841

65D4 64D4 BI M_G_DQ<63..0>

63	AL7	DDR2_DQ<63>
62	AK8	DDR2_DQ<62>
61	AE9	DDR2_DQ<61>
60	AE7	DDR2_DQ<60>
59	AL9	DDR2_DQ<59>
58	AK10	DDR2_DQ<58>
57	AG7	DDR2_DQ<57>
56	AG9	DDR2_DQ<56>
55	AL15	DDR2_DQ<55>
54	AK14	DDR2_DQ<54>
53	AF14	DDR2_DQ<53>
52	AG15	DDR2_DQ<52>
51	AL13	DDR2_DQ<51>
50	AK12	DDR2_DQ<50>
49	AF12	DDR2_DQ<49>
48	AE11	DDR2_DQ<48>
47	Y8	DDR2_DQ<47>
46	AA9	DDR2_DQ<46>
45	U11	DDR2_DQ<45>
44	T10	DDR2_DQ<44>
43	AB8	DDR2_DQ<43>
42	AA11	DDR2_DQ<42>
41	W11	DDR2_DQ<41>
40	U9	DDR2_DQ<40>
39	M6	DDR2_DQ<39>
38	K6	DDR2_DQ<38>
37	L9	DDR2_DQ<37>
36	J9	DDR2_DQ<36>
35	P6	DDR2_DQ<35>
34	R7	DDR2_DQ<34>
33	K8	DDR2_DQ<33>
32	N9	DDR2_DQ<32>
31	T24	DDR2_DQ<31>
30	V24	DDR2_DQ<30>
29	T28	DDR2_DQ<29>
28	V28	DDR2_DQ<28>
27	R23	DDR2_DQ<27>
26	U23	DDR2_DQ<26>
25	R27	DDR2_DQ<25>
24	U27	DDR2_DQ<24>
23	AC31	DDR2_DQ<23>
22	AE31	DDR2_DQ<22>
21	AA35	DDR2_DQ<21>
20	AC35	DDR2_DQ<20>
19	AB30	DDR2_DQ<19>
18	AD30	DDR2_DQ<18>
17	AB34	DDR2_DQ<17>
16	AD34	DDR2_DQ<16>
15	W31	DDR2_DQ<15>
14	T32	DDR2_DQ<14>
13	R35	DDR2_DQ<13>
12	U35	DDR2_DQ<12>
11	T30	DDR2_DQ<11>
10	V30	DDR2_DQ<10>
9	U33	DDR2_DQ<9>
8	V34	DDR2_DQ<8>
7	U37	DDR2_DQ<7>
6	T38	DDR2_DQ<6>
5	AC39	DDR2_DQ<5>
4	AE37	DDR2_DQ<4>
3	Y38	DDR2_DQ<3>
2	R37	DDR2_DQ<2>
1	AA37	DDR2_DQ<1>
0	AD38	DDR2_DQ<0>

65B7 64B7 BI M_G_ECC<7..0>

7	AB24	DDR2_ECC<7>
6	AD24	DDR2_ECC<6>
5	AB28	DDR2_ECC<5>
4	AD28	DDR2_ECC<4>
3	AA23	DDR2_ECC<3>
2	AC23	DDR2_ECC<2>
1	AA27	DDR2_ECC<1>
0	AC27	DDR2_ECC<0>

65C7 64C7 OUT M_G_CLK_DP<3..0>

65C7 64C7 OUT M_G_CLK_DN<3..0>

3	AA19	DDR2_CLK_DP<3>
2	AB18	DDR2_CLK_DP<2>
1	AB20	DDR2_CLK_DP<1>
0	AA17	DDR2_CLK_DP<0>
3	W19	DDR2_CLK_DN<3>
2	Y18	DDR2_CLK_DN<2>
1	Y20	DDR2_CLK_DN<1>
0	W17	DDR2_CLK_DN<0>

65C8 64C8 OUT M_G_BG<1..0>

65C8 64C8 OUT M_G_BA<1..0>

1	AD20	DDR2_BG<1>
0	AA21	DDR2_BG<0>
1	U17	DDR2_BA<1>
0	M14	DDR2_BA<0>

DDR2_DQS_DP<17>	AD26	17
DDR2_DQS_DP<16>	AH10	16
DDR2_DQS_DP<15>	AH16	15
DDR2_DQS_DP<14>	V8	14
DDR2_DQS_DP<13>	M8	13
DDR2_DQS_DP<12>	V26	12
DDR2_DQS_DP<11>	AC33	11
DDR2_DQS_DP<10>	T34	10
DDR2_DQS_DP<9>	AB38	9
DDR2_DQS_DP<8>	AC25	8
DDR2_DQS_DP<7>	AJ7	7
DDR2_DQS_DP<6>	AH12	6
DDR2_DQS_DP<5>	AB10	5
DDR2_DQS_DP<4>	N7	4
DDR2_DQS_DP<3>	U25	3
DDR2_DQS_DP<2>	AB32	2
DDR2_DQS_DP<1>	U31	1
DDR2_DQS_DP<0>	V38	0
DDR2_DQS_DN<17>	AB26	17
DDR2_DQS_DN<16>	AJ9	16
DDR2_DQS_DN<15>	AJ15	15
DDR2_DQS_DN<14>	W9	14
DDR2_DQS_DN<13>	L7	13
DDR2_DQS_DN<12>	T26	12
DDR2_DQS_DN<11>	AA33	11
DDR2_DQS_DN<10>	R33	10
DDR2_DQS_DN<9>	AC37	9
DDR2_DQS_DN<8>	AE25	8
DDR2_DQS_DN<7>	AH8	7
DDR2_DQS_DN<6>	AJ13	6
DDR2_DQS_DN<5>	Y10	5
DDR2_DQS_DN<4>	P8	4
DDR2_DQS_DN<3>	W25	3
DDR2_DQS_DN<2>	AD32	2
DDR2_DQS_DN<1>	V32	1
DDR2_DQS_DN<0>	W37	0
DDR2_MA<17>	T14	17
DDR2_MA<16>	P14	16
DDR2_MA<15>	R13	15
DDR2_MA<14>	Y14	14
DDR2_MA<13>	P12	13
DDR2_MA<12>	W21	12
DDR2_MA<11>	T20	11
DDR2_MA<10>	AA15	10
DDR2_MA<9>	P20	9
DDR2_MA<8>	L19	8
DDR2_MA<7>	U19	7
DDR2_MA<6>	M18	6
DDR2_MA<5>	P18	5
DDR2_MA<4>	R19	4
DDR2_MA<3>	L17	3
DDR2_MA<2>	T18	2
DDR2_MA<1>	M16	1
DDR2_MA<0>	L15	0
DDR2_CKE<5>	AD22	5
DDR2_CKE<4>	AB22	4
DDR2_CKE<3>	Y22	3
DDR2_CKE<2>	T22	2
DDR2_CKE<1>	U21	1
DDR2_CKE<0>	R21	0
DDR2_ODT<5>	AD14	5
DDR2_ODT<4>	AE17	4
DDR2_ODT<3>	AB14	3
DDR2_ODT<2>	R15	2
DDR2_ODT<1>	W15	1
DDR2_ODT<0>	Y16	0
DDR2_CS_N<9>	T12	9
DDR2_CS_N<8>	AD18	8
DDR2_CS7_N_CID<4>	AD16	7
DDR2_CS6_N_CID<3>	AC13	6
DDR2_CS_N<5>	U15	5
DDR2_CS_N<4>	P16	4
DDR2_CS3_N_CID<1>	AA13	3
DDR2_CS2_N_CID<0>	W13	2
DDR2_CS_N<1>	T16	1
DDR2_CS_N<0>	AB16	0
DDR2_CID<2>	U13	
DDR2_ACT_N	AE21	
DDR2_ALERT_N	P22	
DDR2_PAR	R17	

M_G_DQS_DP<17..0> BI 64D2 65D2

M_G_DQS_DN<17..0> BI 64D2 65D2

M_G_MA<17..0> OUT 64D7 65D7

M_G_CKE<5..0> OUT 74D4 74DB 64C7 65C7

M_G_ODT<5..0> OUT 64B7 65B7

M_G_CS_N<9..0> OUT 64C7 65C7

M_G_C<2> OUT 64C7 65C7

M_G_ACT_N OUT 64BB 65BB

M_G_ALERT_N IN 64BB 65BB

M_G_PAR OUT 64BB 65BB

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HASWELL SOCKET 1 (5 OF 14)
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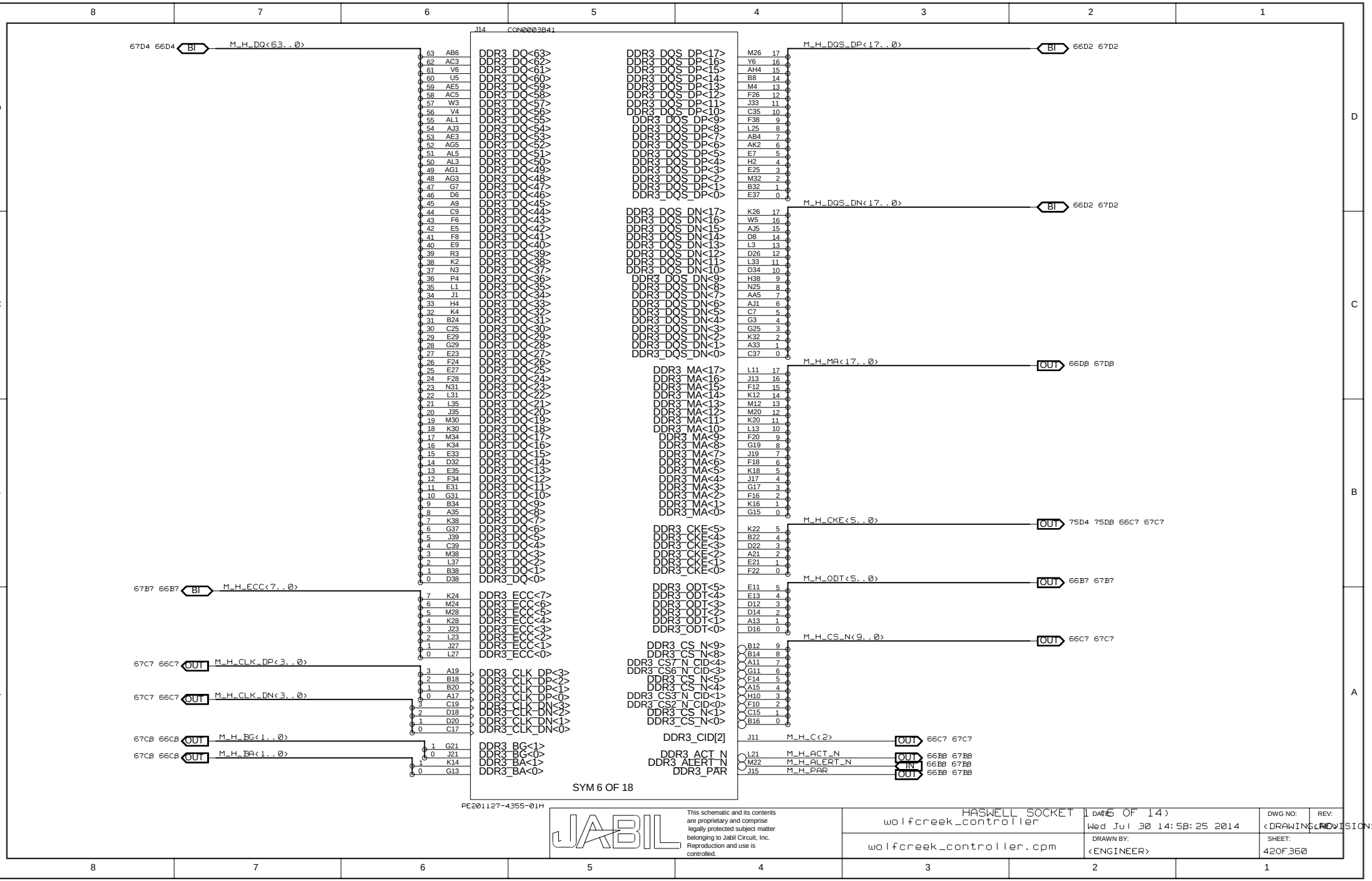
DRAWN BY: <ENGINEER>

SHEET: 41 OF 360


J14 CON0003B41
67D4 66D4 BI M_H_DQ<63..0>
63 AB6 DDR3_DQ<63>
62 AC3 DDR3_DQ<62>
61 V6 DDR3_DQ<61>
60 U5 DDR3_DQ<60>
59 AE5 DDR3_DQ<59>
58 AC5 DDR3_DQ<58>
57 W3 DDR3_DQ<57>
56 V4 DDR3_DQ<56>
55 AL1 DDR3_DQ<55>
54 AJ3 DDR3_DQ<54>
53 AE3 DDR3_DQ<53>
52 AG5 DDR3_DQ<52>
51 AL5 DDR3_DQ<51>
50 AL3 DDR3_DQ<50>
49 AG1 DDR3_DQ<49>
48 AG3 DDR3_DQ<48>
47 G7 DDR3_DQ<47>
46 D6 DDR3_DQ<46>
45 A9 DDR3_DQ<45>
44 C9 DDR3_DQ<44>
43 F6 DDR3_DQ<43>
42 E5 DDR3_DQ<42>
41 F8 DDR3_DQ<41>
40 E9 DDR3_DQ<40>
39 R3 DDR3_DQ<39>
38 K2 DDR3_DQ<38>
37 N3 DDR3_DQ<37>
36 P4 DDR3_DQ<36>
35 L1 DDR3_DQ<35>
34 J1 DDR3_DQ<34>
33 H4 DDR3_DQ<33>
32 K4 DDR3_DQ<32>
31 B24 DDR3_DQ<31>
30 C25 DDR3_DQ<30>
29 E29 DDR3_DQ<29>
28 G29 DDR3_DQ<28>
27 E23 DDR3_DQ<27>
26 F24 DDR3_DQ<26>
25 E27 DDR3_DQ<25>
24 F28 DDR3_DQ<24>
23 N31 DDR3_DQ<23>
22 L31 DDR3_DQ<22>
21 L35 DDR3_DQ<21>
20 J35 DDR3_DQ<20>
19 M30 DDR3_DQ<19>
18 K30 DDR3_DQ<18>
17 M34 DDR3_DQ<17>
16 K34 DDR3_DQ<16>
15 E33 DDR3_DQ<15>
14 D32 DDR3_DQ<14>
13 E35 DDR3_DQ<13>
12 F34 DDR3_DQ<12>
11 E31 DDR3_DQ<11>
10 G31 DDR3_DQ<10>
9 B34 DDR3_DQ<9>
8 A35 DDR3_DQ<8>
7 K38 DDR3_DQ<7>
6 G37 DDR3_DQ<6>
5 J39 DDR3_DQ<5>
4 C39 DDR3_DQ<4>
3 M38 DDR3_DQ<3>
2 L37 DDR3_DQ<2>
1 B38 DDR3_DQ<1>
0 D38 DDR3_DQ<0>
67B7 66B7 BI M_H_ECC<7..0>
7 K24 DDR3_ECC<7>
6 M24 DDR3_ECC<6>
5 M28 DDR3_ECC<5>
4 K28 DDR3_ECC<4>
3 J23 DDR3_ECC<3>
2 L23 DDR3_ECC<2>
1 J27 DDR3_ECC<1>
0 L27 DDR3_ECC<0>
67C7 66C7 OUT M_H_CLK_DP<3..0>
3 A19 DDR3_CLK_DP<3>
2 B18 DDR3_CLK_DP<2>
1 B20 DDR3_CLK_DP<1>
0 A17 DDR3_CLK_DP<0>
67C7 66C7 OUT M_H_CLK_DN<3..0>
3 C19 DDR3_CLK_DN<3>
2 D18 DDR3_CLK_DN<2>
1 D20 DDR3_CLK_DN<1>
0 C17 DDR3_CLK_DN<0>
67C8 66C8 OUT M_H_BG<1..0>
1 G21 DDR3_BG<1>
0 J21 DDR3_BG<0>
67C8 66C8 OUT M_H_BA<1..0>
1 K14 DDR3_BA<1>
0 G13 DDR3_BA<0>
DDR3_DQS_DP<17> M26 17
DDR3_DQS_DP<16> Y6 16
DDR3_DQS_DP<15> AH4 15
DDR3_DQS_DP<14> B8 14
DDR3_DQS_DP<13> M4 13
DDR3_DQS_DP<12> F26 12
DDR3_DQS_DP<11> J33 11
DDR3_DQS_DP<10> C35 10
DDR3_DQS_DP<9> F38 9
DDR3_DQS_DP<8> L25 8
DDR3_DQS_DP<7> AB4 7
DDR3_DQS_DP<6> AK2 6
DDR3_DQS_DP<5> E7 5
DDR3_DQS_DP<4> H2 4
DDR3_DQS_DP<3> E25 3
DDR3_DQS_DP<2> M32 2
DDR3_DQS_DP<1> B32 1
DDR3_DQS_DP<0> E37 0
M_H_DQS_DP<17..0> BI 66D2 67D2
DDR3_DQS_DN<17> K26 17
DDR3_DQS_DN<16> W5 16
DDR3_DQS_DN<15> AJ5 15
DDR3_DQS_DN<14> D8 14
DDR3_DQS_DN<13> L3 13
DDR3_DQS_DN<12> D26 12
DDR3_DQS_DN<11> L33 11
DDR3_DQS_DN<10> D34 10
DDR3_DQS_DN<9> H38 9
DDR3_DQS_DN<8> N25 8
DDR3_DQS_DN<7> AA5 7
DDR3_DQS_DN<6> AJ1 6
DDR3_DQS_DN<5> C7 5
DDR3_DQS_DN<4> G3 4
DDR3_DQS_DN<3> G25 3
DDR3_DQS_DN<2> K32 2
DDR3_DQS_DN<1> A33 1
DDR3_DQS_DN<0> C37 0
M_H_DQS_DN<17..0> BI 66D2 67D2
DDR3_MA<17> L11 17
DDR3_MA<16> J13 16
DDR3_MA<15> F12 15
DDR3_MA<14> K12 14
DDR3_MA<13> M12 13
DDR3_MA<12> M20 12
DDR3_MA<11> K20 11
DDR3_MA<10> L13 10
DDR3_MA<9> F20 9
DDR3_MA<8> G19 8
DDR3_MA<7> J19 7
DDR3_MA<6> F18 6
DDR3_MA<5> K18 5
DDR3_MA<4> J17 4
DDR3_MA<3> G17 3
DDR3_MA<2> F16 2
DDR3_MA<1> K16 1
DDR3_MA<0> G15 0
M_H_MA<17..0> OUT 66DB 67DB
DDR3_CKE<5> K22 5
DDR3_CKE<4> B22 4
DDR3_CKE<3> D22 3
DDR3_CKE<2> A21 2
DDR3_CKE<1> E21 1
DDR3_CKE<0> F22 0
M_H_CKE<5..0> OUT 75D4 75DB 66C7 67C7
DDR3_ODT<5> E11 5
DDR3_ODT<4> E13 4
DDR3_ODT<3> D12 3
DDR3_ODT<2> D14 2
DDR3_ODT<1> A13 1
DDR3_ODT<0> D16 0
M_H_ODT<5..0> OUT 66B7 67B7
DDR3_CS_N<9> B12 9
DDR3_CS_N<8> B14 8
DDR3_CS7_N_CID<4> A11 7
DDR3_CS6_N_CID<3> G11 6
DDR3_CS_N<5> F14 5
DDR3_CS_N<4> A15 4
DDR3_CS3_N_CID<1> H10 3
DDR3_CS2_N_CID<0> F10 2
DDR3_CS_N<1> C15 1
DDR3_CS_N<0> B16 0
M_H_CS_N<9..0> OUT 66C7 67C7
DDR3_CID[2] J11 M_H_C<2> OUT 66C7 67C7
DDR3_ACT_N L21 M_H_ACT_N OUT 66BB 67BB
DDR3_ALERT_N M22 M_H_ALERT_N IN 66BB 67BB
DDR3_PAR J15 M_H_PAR OUT 66BB 67BB
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PE201127-4355-01H
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HASWELL SOCKET (5 OF 14)
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DATE: Wed Jul 30 14:58:25 2014
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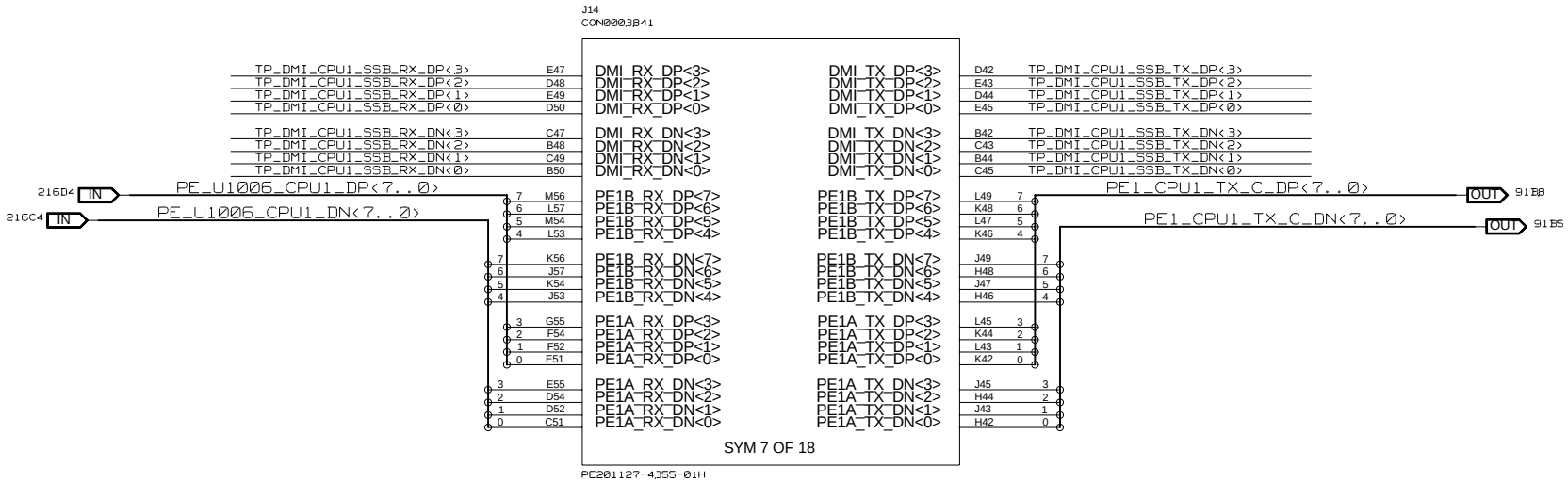
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 42OF360



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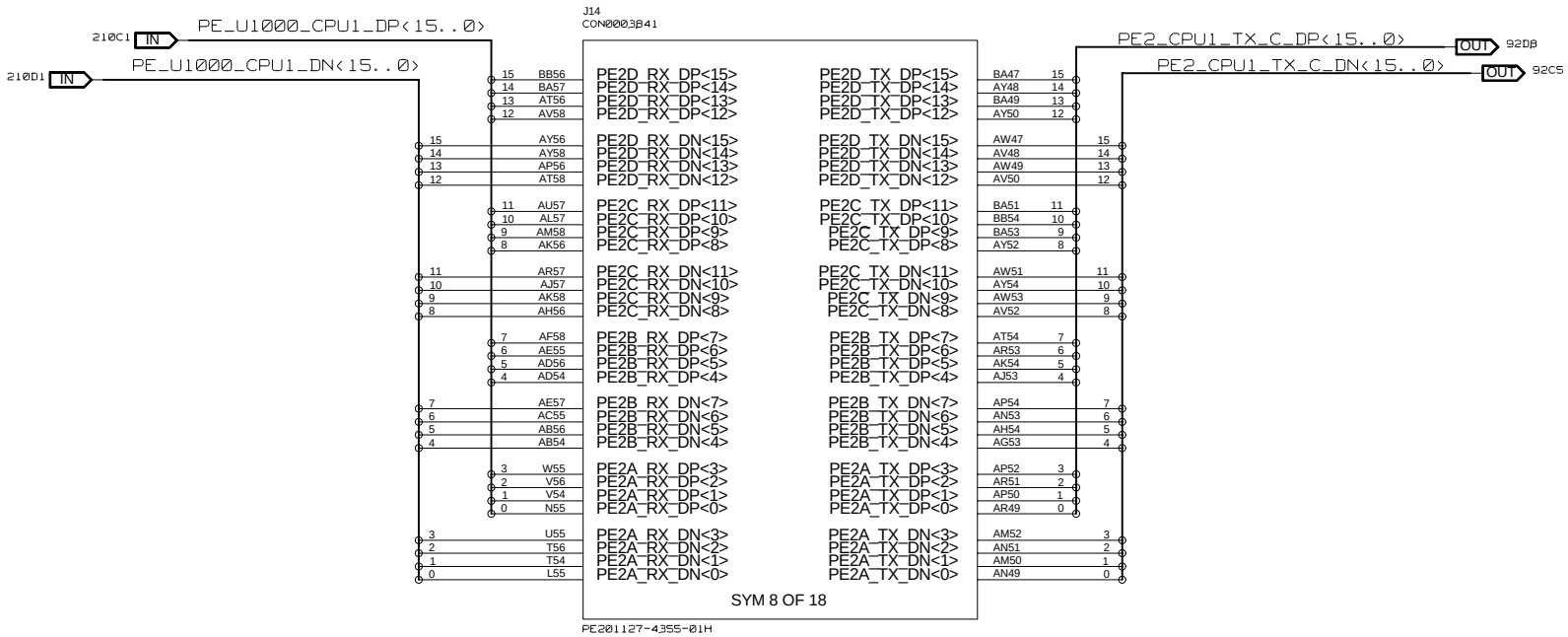
HASWELL SOCKET wolfcreek_controller	DATE: Wed Jul 30 14:58:26 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 43 OF 360	



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HASWELL SOCKET (8 OF 14)
wolfcreek_controller

DATE: Wed Jul 30 14:58:26 2014

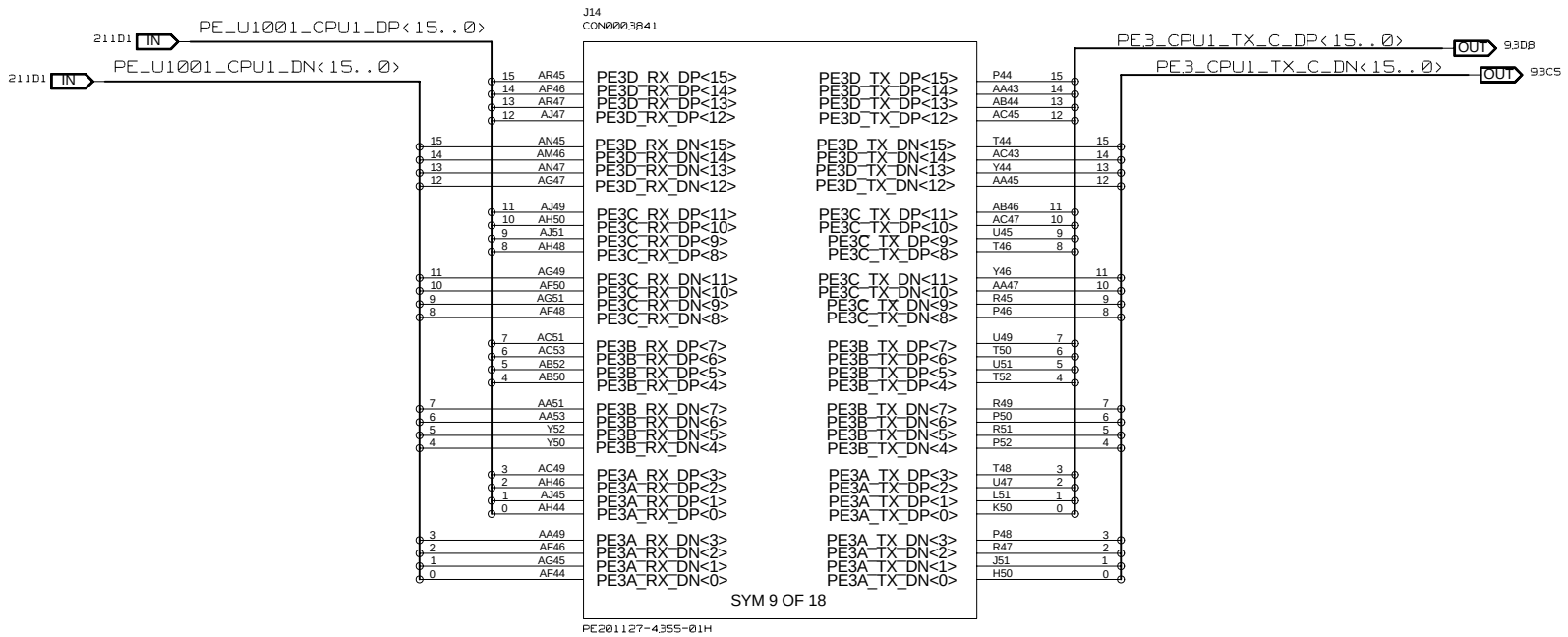
DWG NO: <DRAWING NO>

REV: <REVISION>

wolfcreek_controller.cpm

DRAWN BY: <ENGINEER>

SHEET: 44OF360



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HASWELL SOCKET (9 OF 14)
wolfcreek_controller

DATE: Wed Jul 30 14:58:27 2014

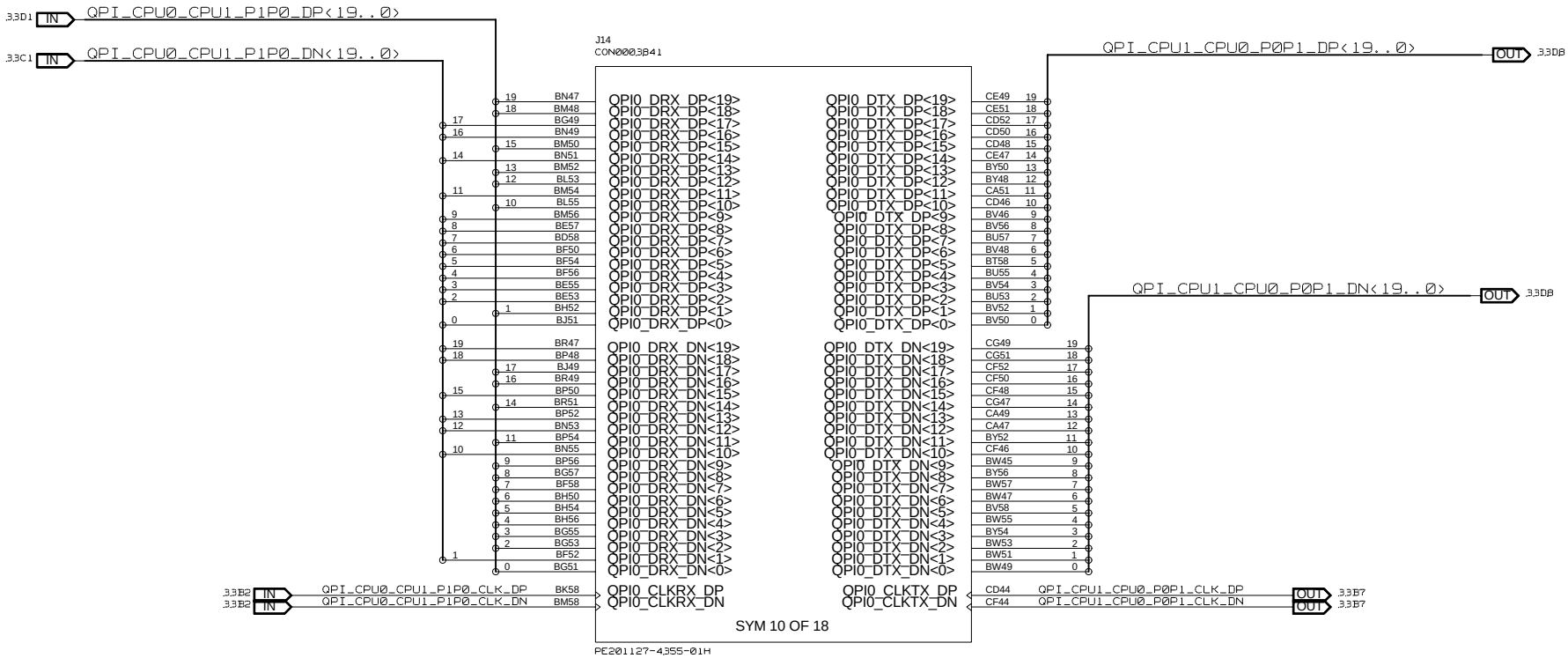
DWG NO: <DRAWING NO>

REV: <REVISION>

wolfcreek_controller.cpm

DRAWN BY: <ENGINEER>

SHEET: 45OF360



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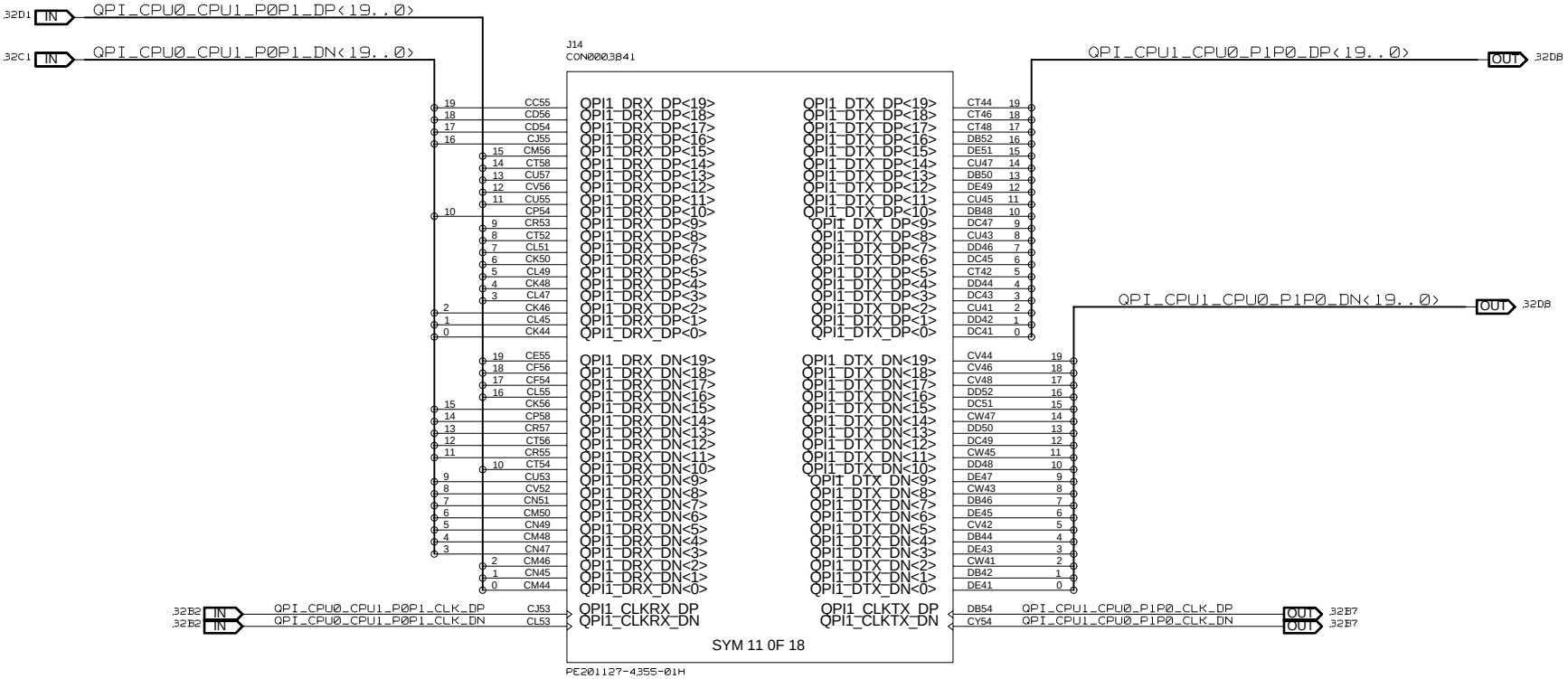
HASWELL SOCKET (10 OF 14)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:27 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 46OF360



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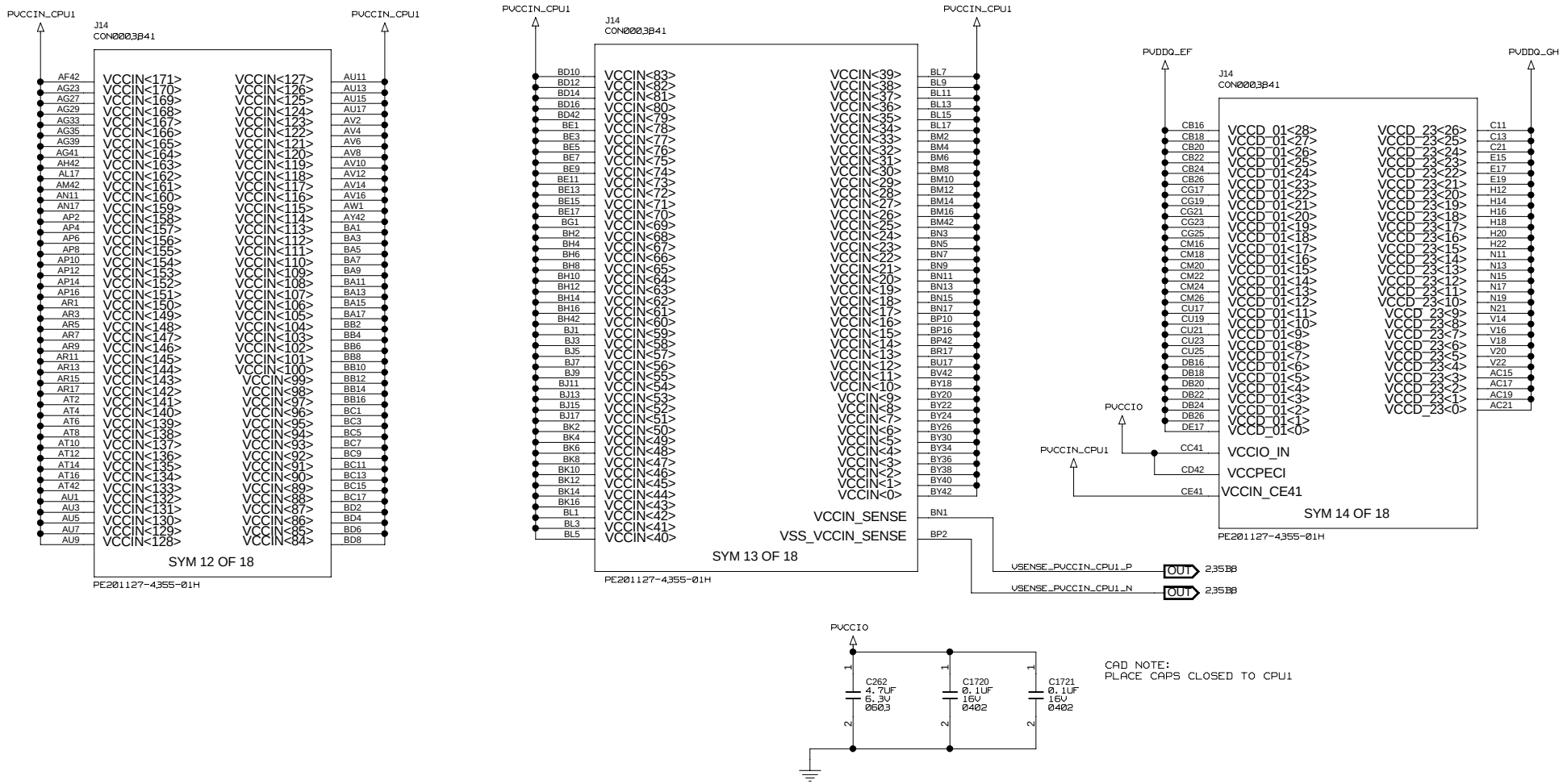
HASWELL SOCKET wolfcreek_controller	PAGE 11 OF 14 DATE: Wed Jul 30 14:58:27 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 47OF360	



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HASWELL SOCKET (12 OF 14) wolfcreek_controller	DATE: Wed Jul 30 14:58:28 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 48OF360	

J14
CON0003B41

A23	VSS<630>	VSS<551>	M2
A37	VSS<629>	VSS<550>	M36
A39	VSS<628>	VSS<549>	M42
A41	VSS<627>	VSS<548>	M44
A43	VSS<626>	VSS<547>	M46
A45	VSS<625>	VSS<546>	M48
A47	VSS<624>	VSS<545>	M50
A49	VSS<623>	VSS<544>	M52
A5	VSS<622>	VSS<543>	N23
A51	VSS<621>	VSS<542>	N27
A7	VSS<620>	VSS<541>	N29
B10	VSS<619>	VSS<540>	N33
B36	VSS<618>	VSS<539>	N35
B40	VSS<617>	VSS<538>	N37
B52	VSS<616>	VSS<537>	N39
B6	VSS<615>	VSS<536>	N43
C33	VSS<614>	VSS<535>	N45
C5	VSS<613>	VSS<534>	N47
C55	VSS<612>	VSS<533>	N49
D10	VSS<611>	VSS<532>	N5
D24	VSS<610>	VSS<531>	N51
D36	VSS<609>	VSS<530>	N53
D4	VSS<608>	VSS<529>	P10
D40	VSS<607>	VSS<528>	P24
E1	VSS<606>	VSS<527>	P26
E3	VSS<605>	VSS<526>	P28
E39	VSS<604>	VSS<525>	P30
E41	VSS<603>	VSS<524>	P32
F2	VSS<602>	VSS<523>	P34
F30	VSS<601>	VSS<522>	P38
F32	VSS<600>	VSS<521>	P40
F36	VSS<599>	VSS<520>	P54
F4	VSS<598>	VSS<519>	P56
F42	VSS<597>	VSS<518>	R11
F44	VSS<596>	VSS<517>	R25
F48	VSS<595>	VSS<516>	R29
F50	VSS<594>	VSS<515>	R31
G1	VSS<593>	VSS<514>	R39
G23	VSS<592>	VSS<513>	R5
G27	VSS<591>	VSS<512>	R55
G33	VSS<590>	VSS<511>	R9
G35	VSS<589>	VSS<510>	T36
G39	VSS<588>	VSS<509>	T4
G41	VSS<587>	VSS<508>	T42
G45	VSS<586>	VSS<507>	T6
G47	VSS<585>	VSS<506>	T8
G49	VSS<584>	VSS<505>	U29
G5	VSS<583>	VSS<504>	U3
G51	VSS<582>	VSS<503>	U39
G53	VSS<581>	VSS<502>	U41
G57	VSS<580>	VSS<501>	U43
G9	VSS<579>	VSS<500>	U7
H24	VSS<578>	VSS<499>	V10
H26	VSS<577>	VSS<498>	V12
H28	VSS<576>	VSS<497>	V36
H30	VSS<575>	VSS<496>	V44
H32	VSS<574>	VSS<495>	V46
H34	VSS<573>	VSS<494>	V48
H36	VSS<572>	VSS<493>	V50
H40	VSS<571>	VSS<492>	V52
H54	VSS<570>	VSS<491>	W23
H6	VSS<569>	VSS<490>	W27
H8	VSS<568>	VSS<489>	W33
J25	VSS<567>	VSS<488>	W35
J29	VSS<566>	VSS<487>	W39
J3	VSS<565>	VSS<486>	W43
J31	VSS<564>	VSS<485>	W45
J37	VSS<563>	VSS<484>	W47
J5	VSS<562>	VSS<483>	W49
J55	VSS<561>	VSS<482>	W51
J7	VSS<560>	VSS<481>	W53
K10	VSS<559>	VSS<480>	W7
K36	VSS<558>	VSS<479>	Y12
K40	VSS<557>	VSS<478>	Y24
L29	VSS<556>	VSS<477>	Y26
L39	VSS<555>	VSS<476>	Y28
L41	VSS<554>	VSS<475>	Y30
L5	VSS<553>	VSS<474>	Y32
M10	VSS<552>	VSS<473>	Y34

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PE201127-4355-01H

J14
CON0003B41

Y36	VSS<472>	VSS<393>	AH6
Y4	VSS<471>	VSS<392>	AH14
Y42	VSS<470>	VSS<391>	AH58
Y56	VSS<469>	VSS<390>	AJ11
AA3	VSS<468>	VSS<389>	AJ17
AA25	VSS<467>	VSS<388>	AK4
AA29	VSS<466>	VSS<387>	AK6
AA7	VSS<465>	VSS<386>	AK16
AA31	VSS<464>	VSS<385>	AK42
AA39	VSS<463>	VSS<384>	AK44
AA55	VSS<462>	VSS<383>	AK46
AB12	VSS<461>	VSS<382>	AK48
AB36	VSS<460>	VSS<381>	AK50
AB40	VSS<459>	VSS<380>	AK52
AB42	VSS<458>	VSS<379>	AL11
AC7	VSS<457>	VSS<378>	AL43
AC9	VSS<456>	VSS<377>	AL45
AC11	VSS<455>	VSS<376>	AL47
AC29	VSS<454>	VSS<375>	AL49
AD4	VSS<453>	VSS<374>	AL51
AD8	VSS<452>	VSS<373>	AL53
AD6	VSS<451>	VSS<372>	AM2
AD10	VSS<450>	VSS<371>	AM4
AD12	VSS<449>	VSS<370>	AM6
AD36	VSS<448>	VSS<369>	AM8
AD40	VSS<447>	VSS<368>	AM10
AD42	VSS<446>	VSS<367>	AM12
AD44	VSS<445>	VSS<366>	AM14
AD46	VSS<444>	VSS<365>	AM16
AD48	VSS<443>	VSS<364>	AM56
AD50	VSS<442>	VSS<363>	AN1
AD52	VSS<441>	VSS<362>	AN3
AE13	VSS<440>	VSS<361>	AN5
AE15	VSS<439>	VSS<360>	AN7
AE19	VSS<438>	VSS<359>	AN9
AE23	VSS<437>	VSS<358>	AN13
AE27	VSS<436>	VSS<357>	AN15
AE29	VSS<435>	VSS<356>	AN55
AE33	VSS<434>	VSS<355>	AN57
AE35	VSS<433>	VSS<354>	AP42
AE39	VSS<432>	VSS<353>	AP44
AE41	VSS<431>	VSS<352>	AP58
AE43	VSS<430>	VSS<351>	AT44
AE47	VSS<429>	VSS<350>	AT46
AE49	VSS<428>	VSS<349>	AT48
AF10	VSS<427>	VSS<348>	AT50
AF16	VSS<426>	VSS<347>	AT52
AF18	VSS<425>	VSS<346>	AU45
AE51	VSS<424>	VSS<345>	AU47
AE53	VSS<423>	VSS<344>	AU49
AF2	VSS<422>	VSS<343>	AU51
AF4	VSS<421>	VSS<342>	AU53
AF6	VSS<420>	VSS<341>	AV42
AF8	VSS<419>	VSS<340>	AV54
AF20	VSS<418>	VSS<339>	AV56
AF22	VSS<417>	VSS<338>	AW11
AF24	VSS<416>	VSS<337>	AW13
AF26	VSS<415>	VSS<336>	AW15
AF28	VSS<414>	VSS<335>	AW17
AF30	VSS<413>	VSS<334>	AW3
AF32	VSS<412>	VSS<333>	AW5
AF34	VSS<411>	VSS<332>	AW7
AF36	VSS<410>	VSS<331>	AW9
AF38	VSS<409>	VSS<330>	AW55
AF40	VSS<408>	VSS<329>	AW57
AF54	VSS<407>	VSS<328>	AY2
AF56	VSS<406>	VSS<327>	AY4
AG11	VSS<405>	VSS<326>	AY6
AG13	VSS<404>	VSS<325>	AY8
AG17	VSS<403>	VSS<324>	AY10
AG19	VSS<402>	VSS<323>	AY12
AG21	VSS<401>	VSS<322>	AY14
AG25	VSS<400>	VSS<321>	AY16
AG31	VSS<399>	VSS<320>	AY44
AG37	VSS<398>	VSS<319>	BB42
AG43	VSS<397>	VSS<318>	BB46
AG55	VSS<396>	VSS<317>	BB50
AG57	VSS<395>	VSS<316>	BB58
AH2	VSS<394>	VSS<315>	BC45

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PE201127-4355-01H

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HASWELL SOCKET (13 OF 14)
wolfcreek_controller

DATE: Wed Jul 30 14:58:29 2014

DWG NO: <DRAWING NO>

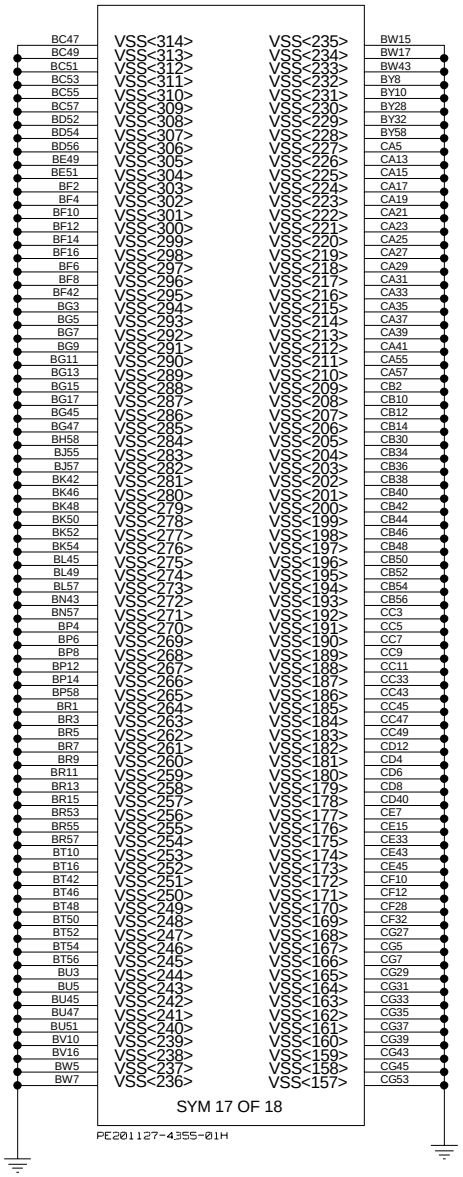
REV: <REVISION>

wolfcreek_controller.cpm

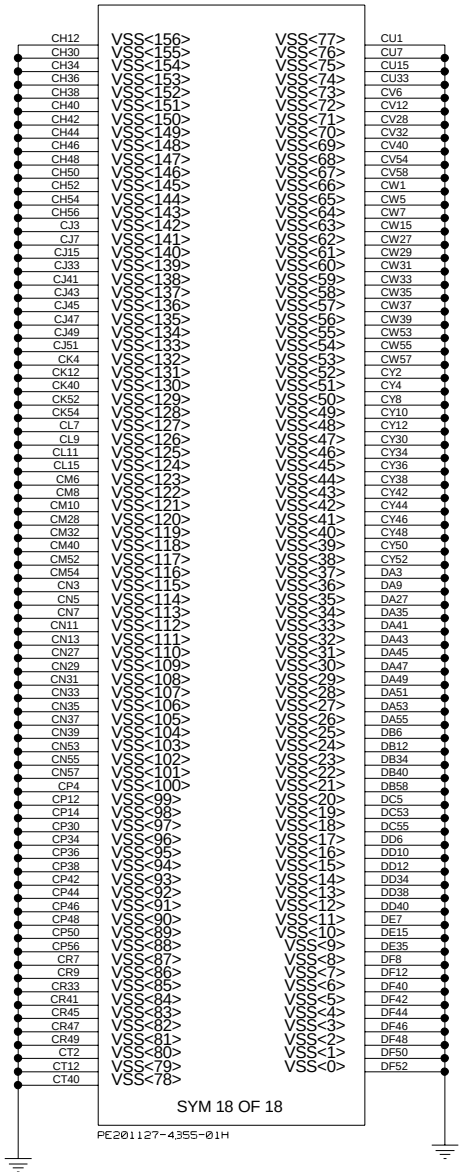
DRAWN BY: <ENGINEER>

SHEET: 49OF360

J14
CON0003B41



J14
CON0003B41



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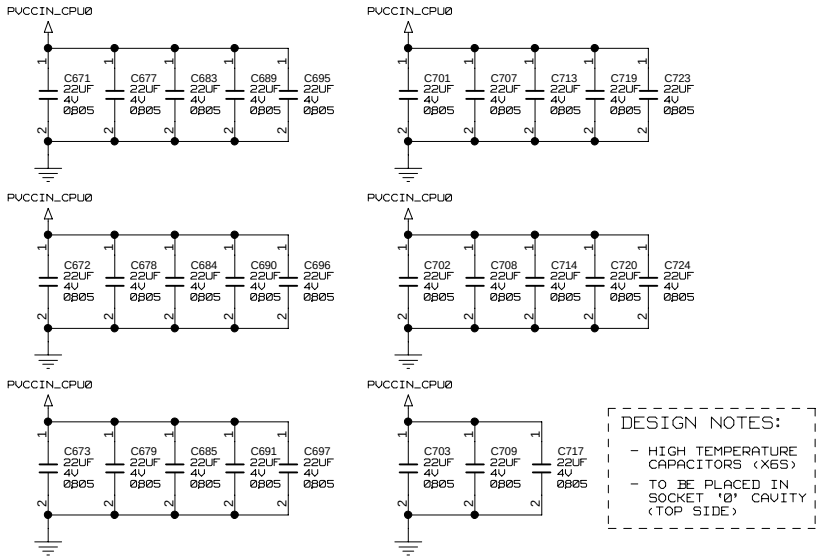
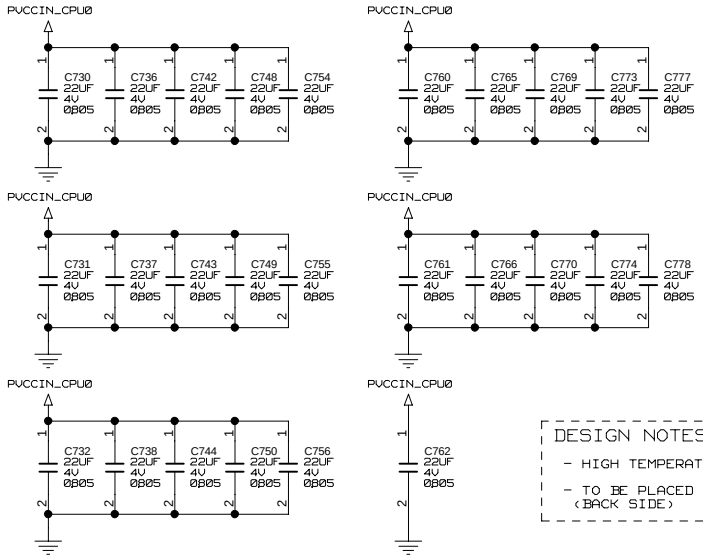
HASWELL SOCKET wolfcreek_controller	PAGE (14 OF 14) Wed Jul 30 14:58:29 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 50OF360	



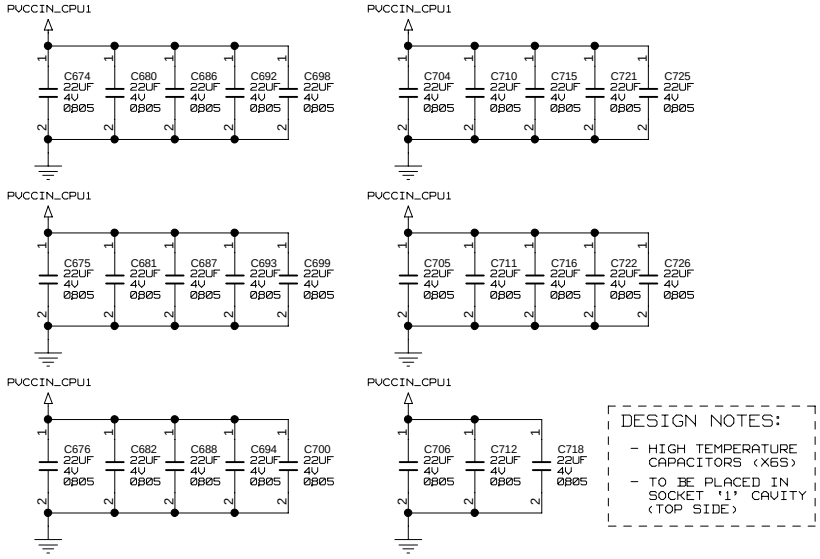
DESIGN NOTES:

- HIGH TEMPERATURE CAPACITORS (X6S)
- TO BE PLACED IN SOCKET '0' CAVITY (TOP SIDE)



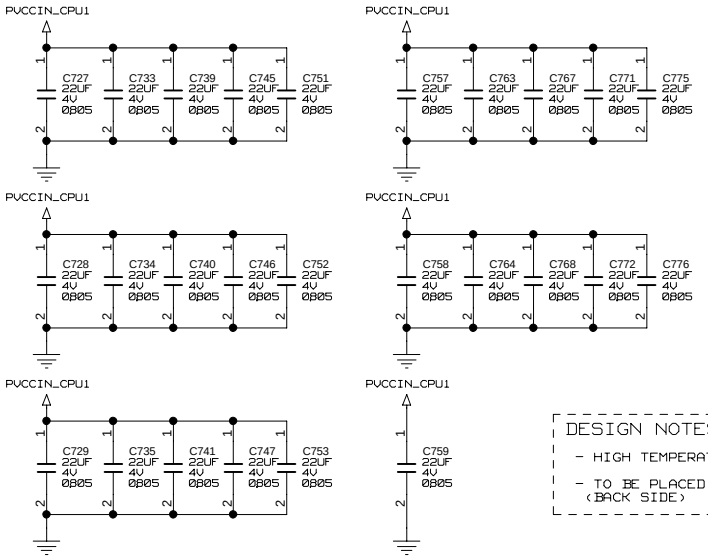
DESIGN NOTES:

- HIGH TEMPERATURE CAPACITORS (X6S)
- TO BE PLACED IN SOCKET '0' CAVITY (BACK SIDE)



DESIGN NOTES:

- HIGH TEMPERATURE CAPACITORS (X6S)
- TO BE PLACED IN SOCKET '1' CAVITY (TOP SIDE)



DESIGN NOTES:

- HIGH TEMPERATURE CAPACITORS (X6S)
- TO BE PLACED IN SOCKET '1' CAVITY (BACK SIDE)

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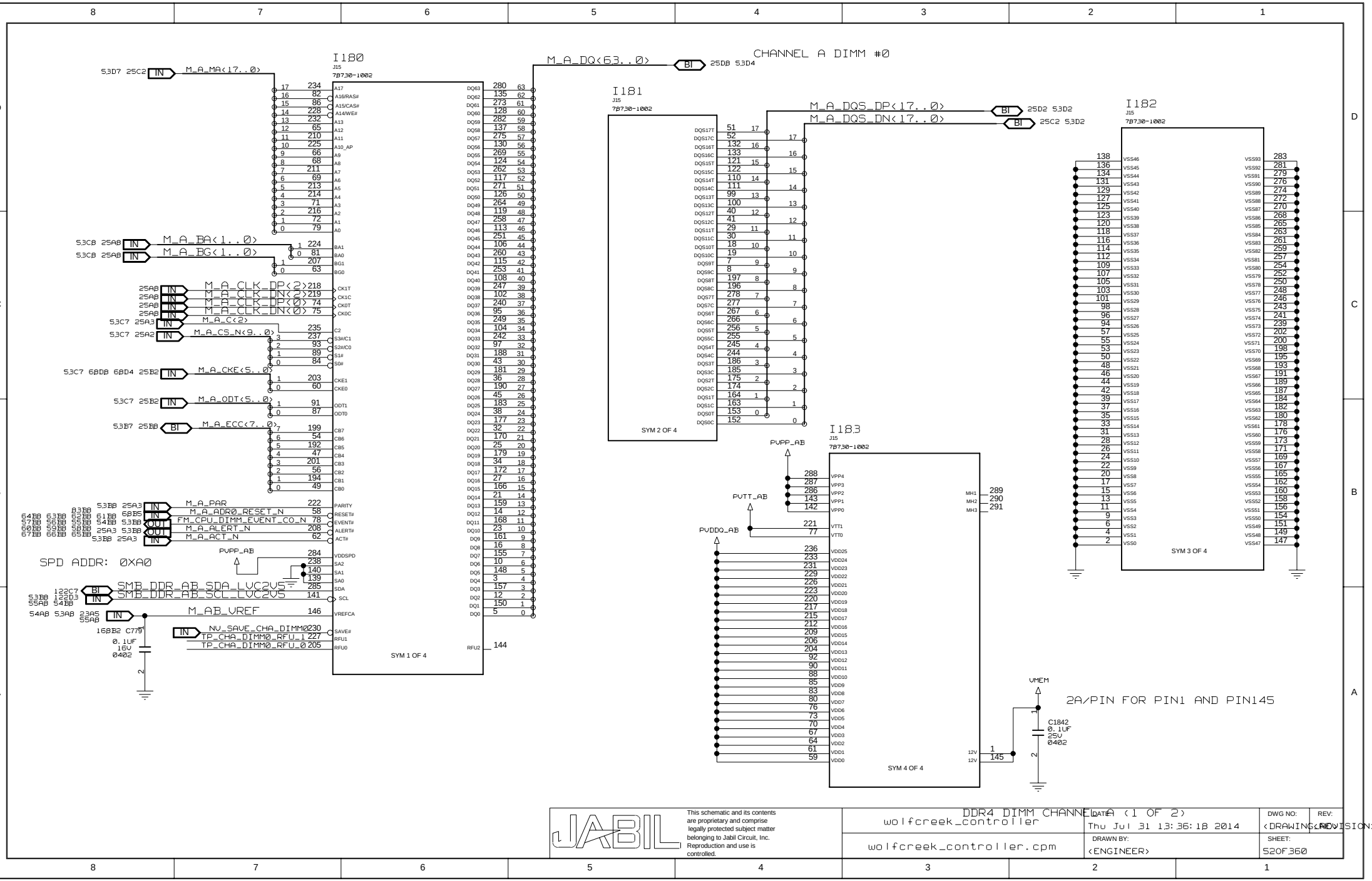
DECOUPLING CPU 0 & 1	DATE: Wed Jul 30 14:58:30 2014	DWG NO: <DRAWING NO>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 51OF360	


CHANNEL A DIMM #0
I180
J15
7B730-1002
SYM 1 OF 4
I181
J15
7B730-1002
SYM 2 OF 4
I182
J15
7B730-1002
SYM 3 OF 4
I183
J15
7B730-1002
SYM 4 OF 4
M_A_MA(17..0)
M_A_BA(1..0)
M_A_BG(1..0)
M_A_CLK_DP(2)
M_A_CLK_DN(2)
M_A_CLK_DP(0)
M_A_CLK_DN(0)
M_A_C(2)
M_A_CS_N(9..0)
M_A_CKE(5..0)
M_A_ODT(5..0)
M_A_ECC(7..0)
M_A_PAR
M_A_ADR0_RESET_N
FM_CPU_DIMM_EVENT_CO_N
M_A_ALERT_N
M_A_ACT_N
SPD ADDR: 0XA0
SMB_DDR_AB_SDA_LVC2V5
SMB_DDR_AB_SCL_LVC2V5
M_AB_VREF
NV_SAVE_CHA_DIMM0
TP_CHA_DIMM0_RFU_1
TP_CHA_DIMM0_RFU_0
M_A_DQ(63..0)
M_A_DQS_DP(17..0)
M_A_DQS_DN(17..0)
PVPP_AB
PVTT_AB
PVDDQ_AB
VMEM
C1842
0.1UF
25V
0402
2A/PIN FOR PIN1 AND PIN145
JABIL
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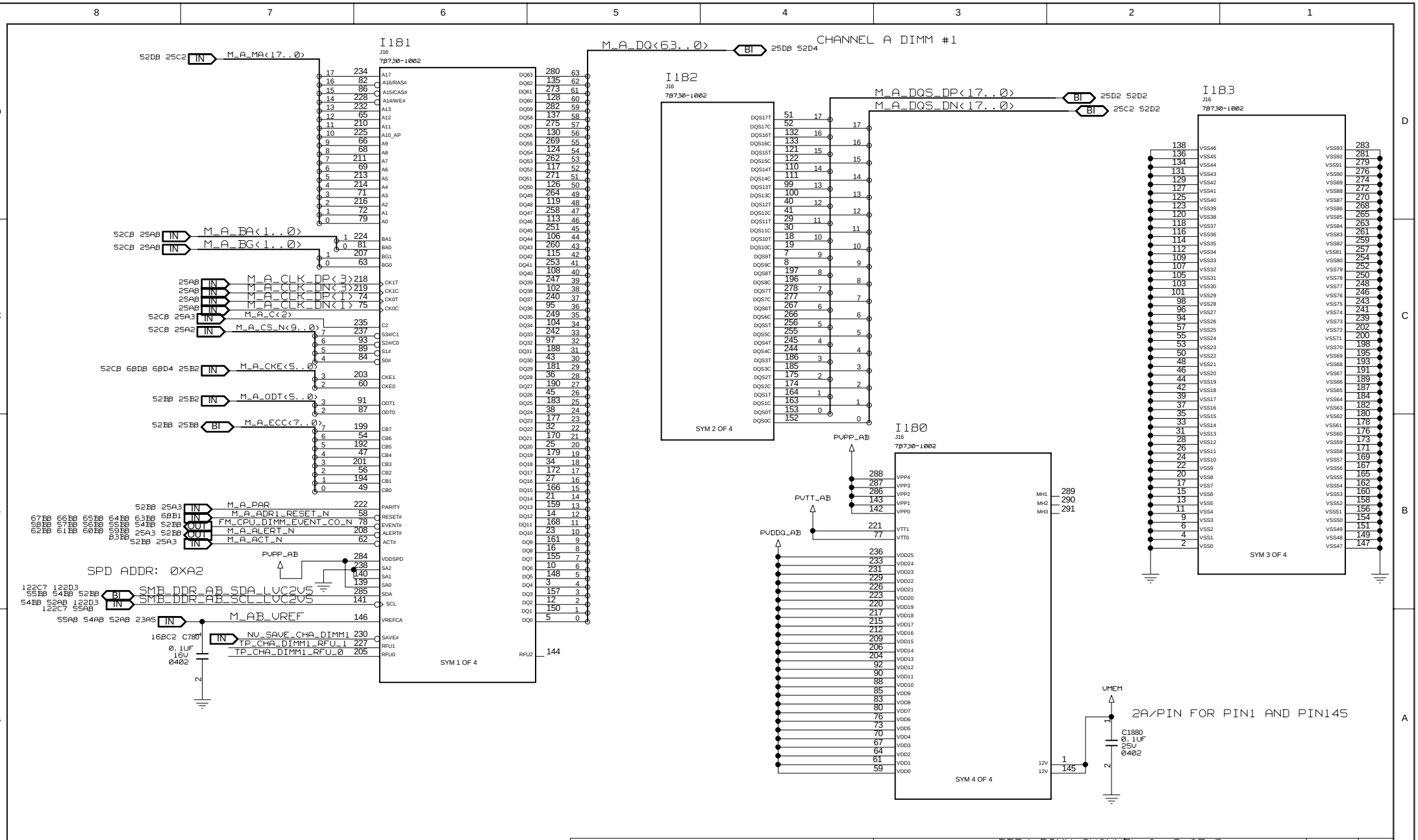
DDR4 DIMM CHANNEL A (1 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Thu Jul 31 13:36:18 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING NO>
REV:
<REVISION>
SHEET:
S2OF360



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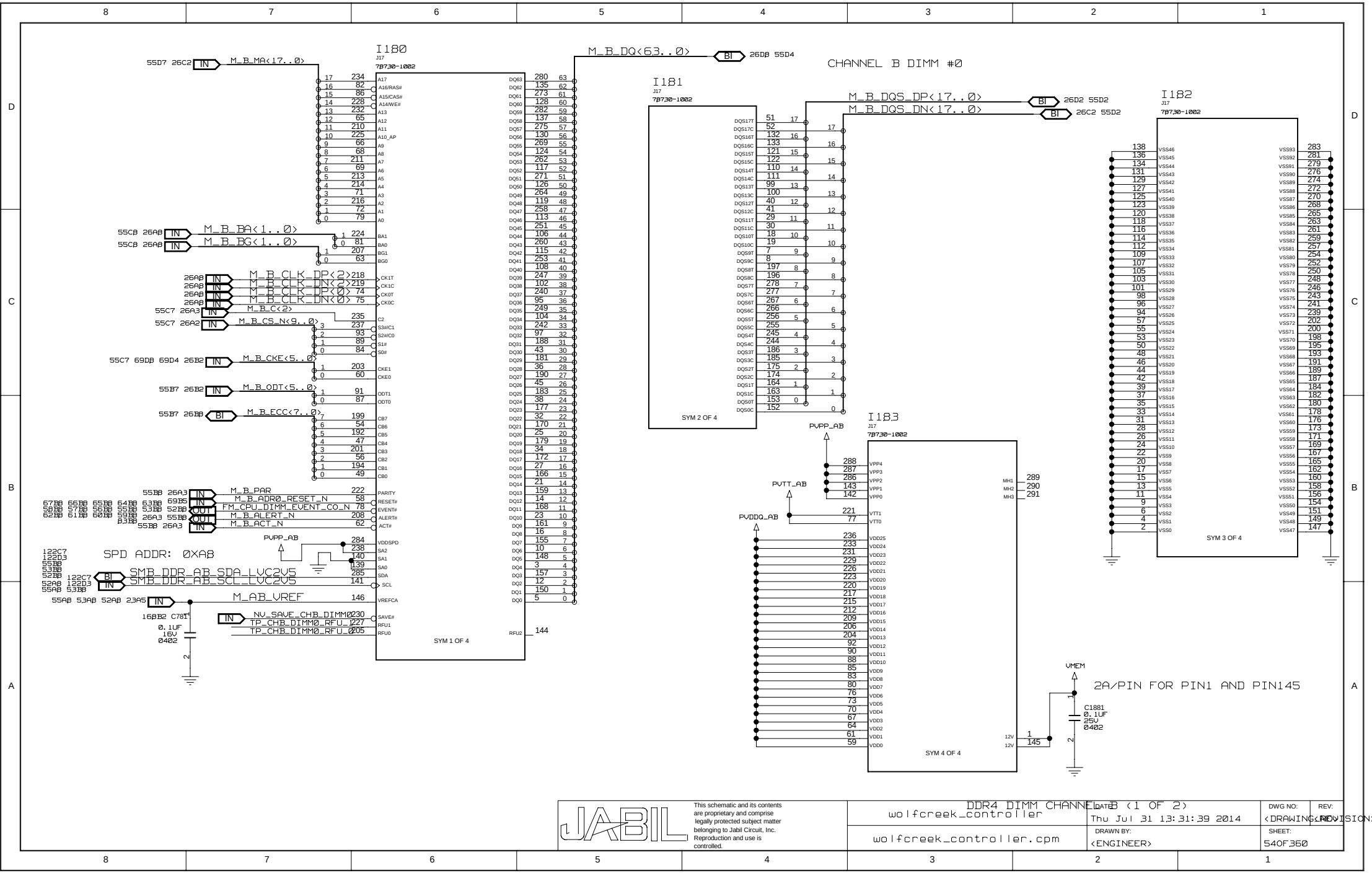
DDR4 DIMM CHANNEL A (2 OF 2)	DATE: Thu Jul 31 13:36:16 2014	DWG NO: <DRAWING NO>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 53 OF 360	


CHANNEL B DIMM #0
I180
J17
7B730-1002
SYM 1 OF 4
I181
J17
7B730-1002
SYM 2 OF 4
I182
J17
7B730-1002
SYM 3 OF 4
I183
J17
7B730-1002
SYM 4 OF 4
M_B_DQ<63..0>
M_B_DQS_DP<17..0>
M_B_DQS_DN<17..0>
M_B_MA<17..0>
M_B_BA<1..0>
M_B_BG<1..0>
M_B_CLK_DP<2>
M_B_CLK_DN<2>
M_B_CLK_DP<0>
M_B_CLK_DN<0>
M_B_C<2>
M_B_CS_N<9..0>
M_B_CKE<5..0>
M_B_ODT<5..0>
M_B_ECC<7..0>
M_B_PAR
M_B_ADR0_RESET_N
FM_CPU_DIMM_EVENT_CO_N
M_B_ALERT_N
M_B_ACT_N
SPD ADDR: 0XA8
SMB_DDR_AB_SDA_LVC2V5
SMB_DDR_AB_SCL_LVC2V5
M_AB_VREF
NV_SAVE_CHB_DIMM0
TP_CHB_DIMM0_RFU_1
TP_CHB_DIMM0_RFU_0
PVPP_AB
PVTT_AB
PVDDQ_AB
VMEM
2A/PIN FOR PIN1 AND PIN145
C1881
0.1UF
25V
0402
0.1UF
16V
0402
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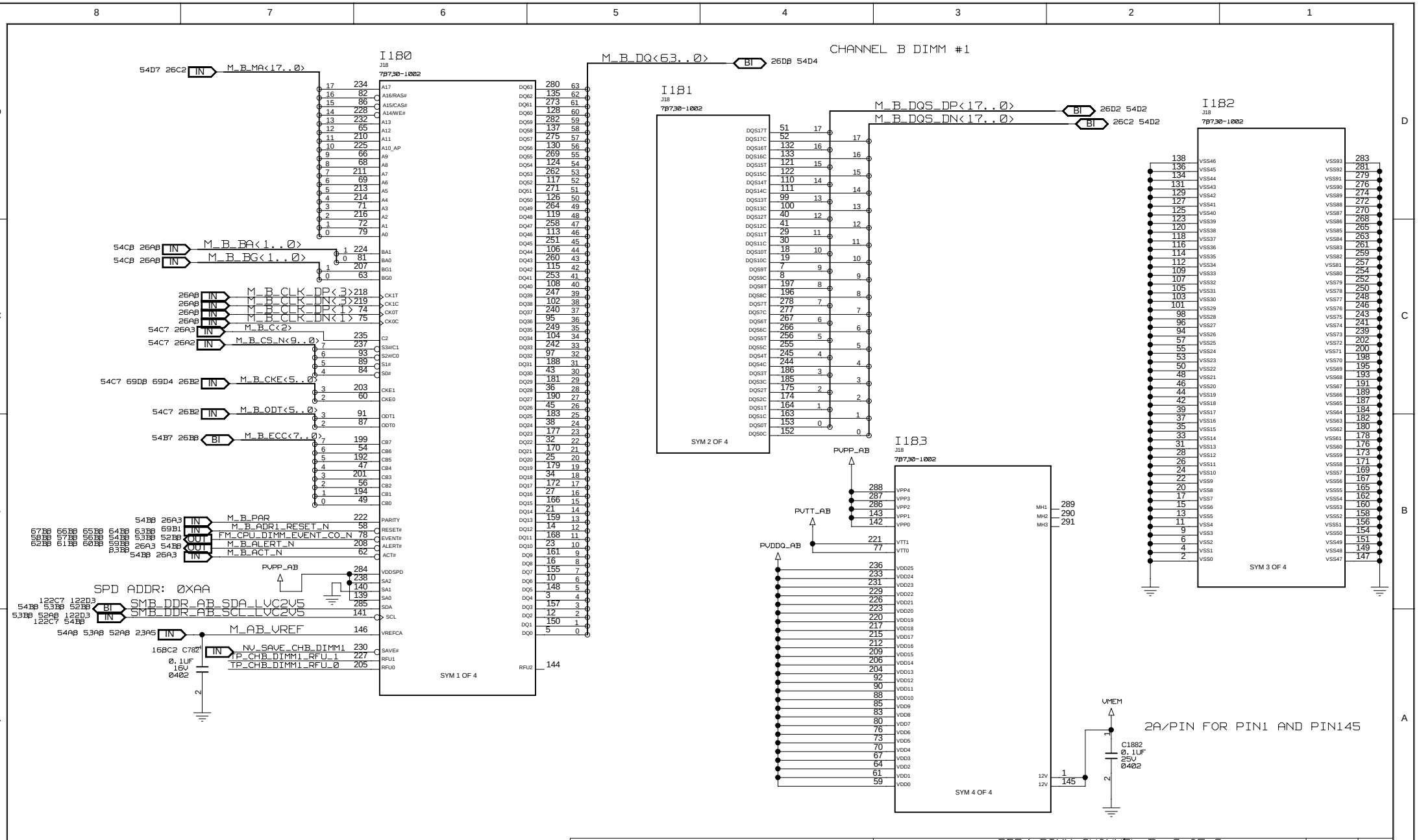
DDR4 DIMM CHANNEL B (1 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Thu Jul 31 13:31:39 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING NO>
REV:
<REVISION>
SHEET:
54OF360



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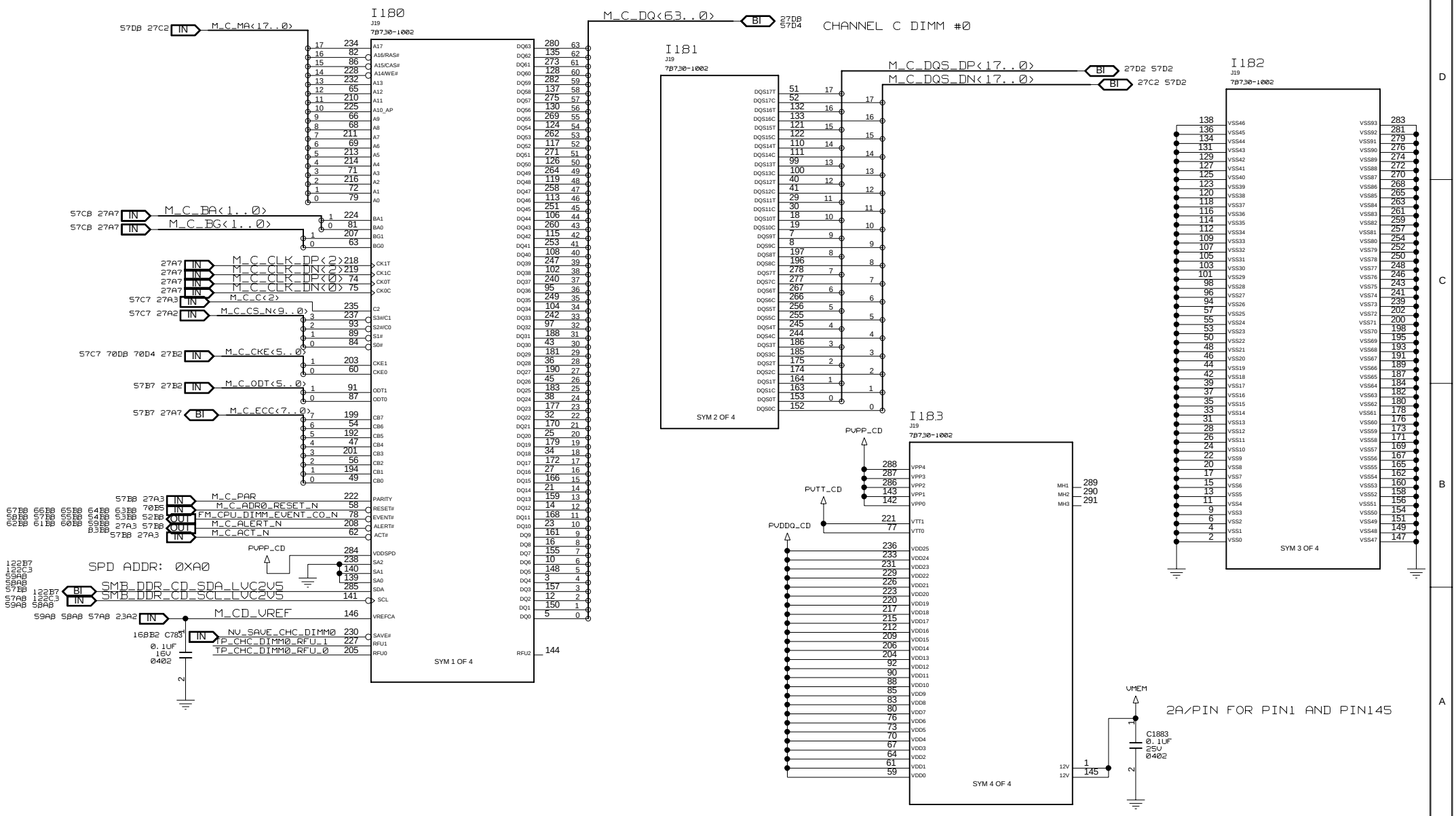
DDR4 DIMM CHANNEL B (2 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 13:31:56 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 55OF360



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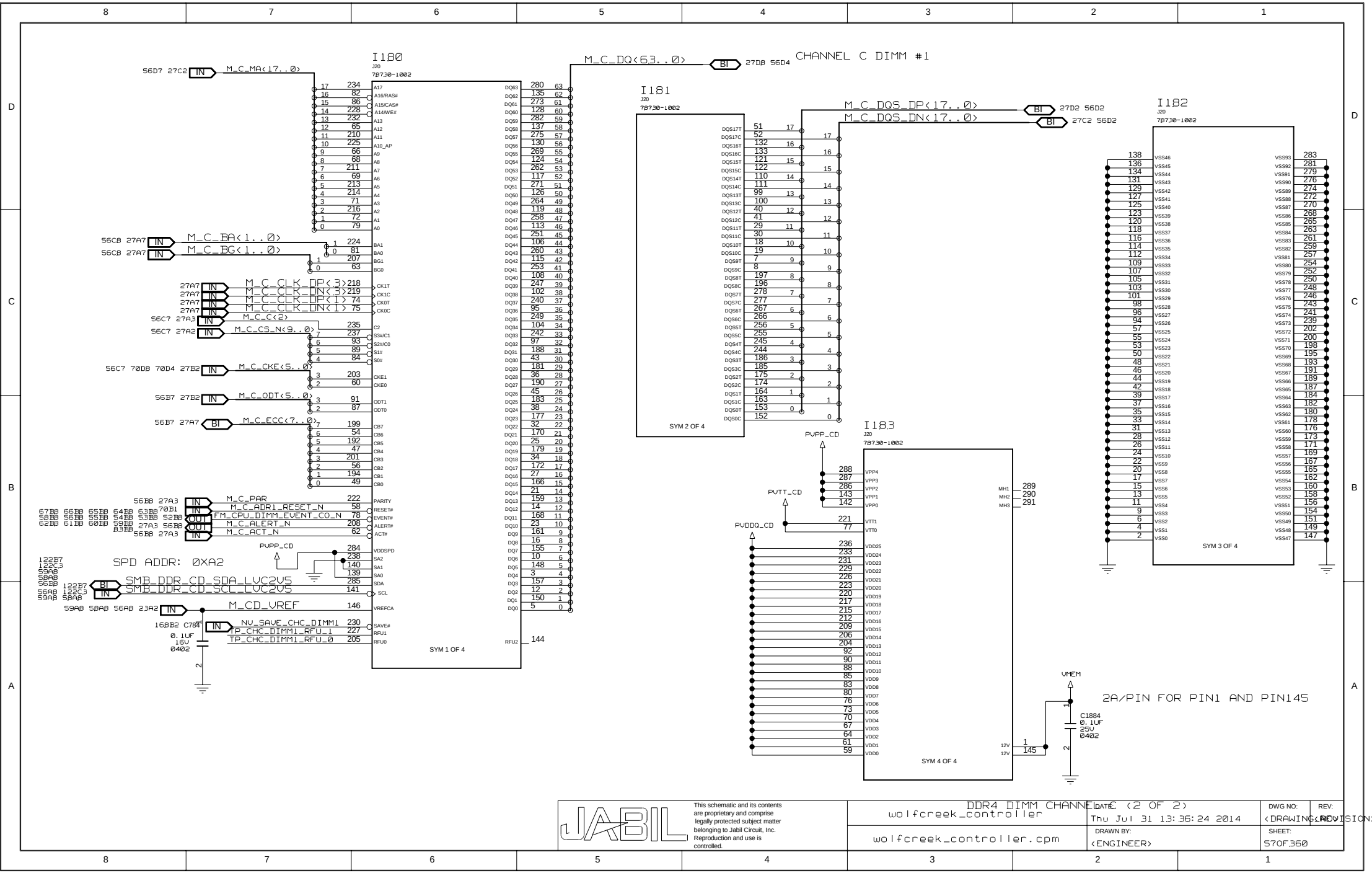
DDR4 DIMM CHANNEL C (1 OF 2)	DATE: Thu Jul 31 13:36:21 2014	DWG NO: <DRAWING NO>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 56OF360	



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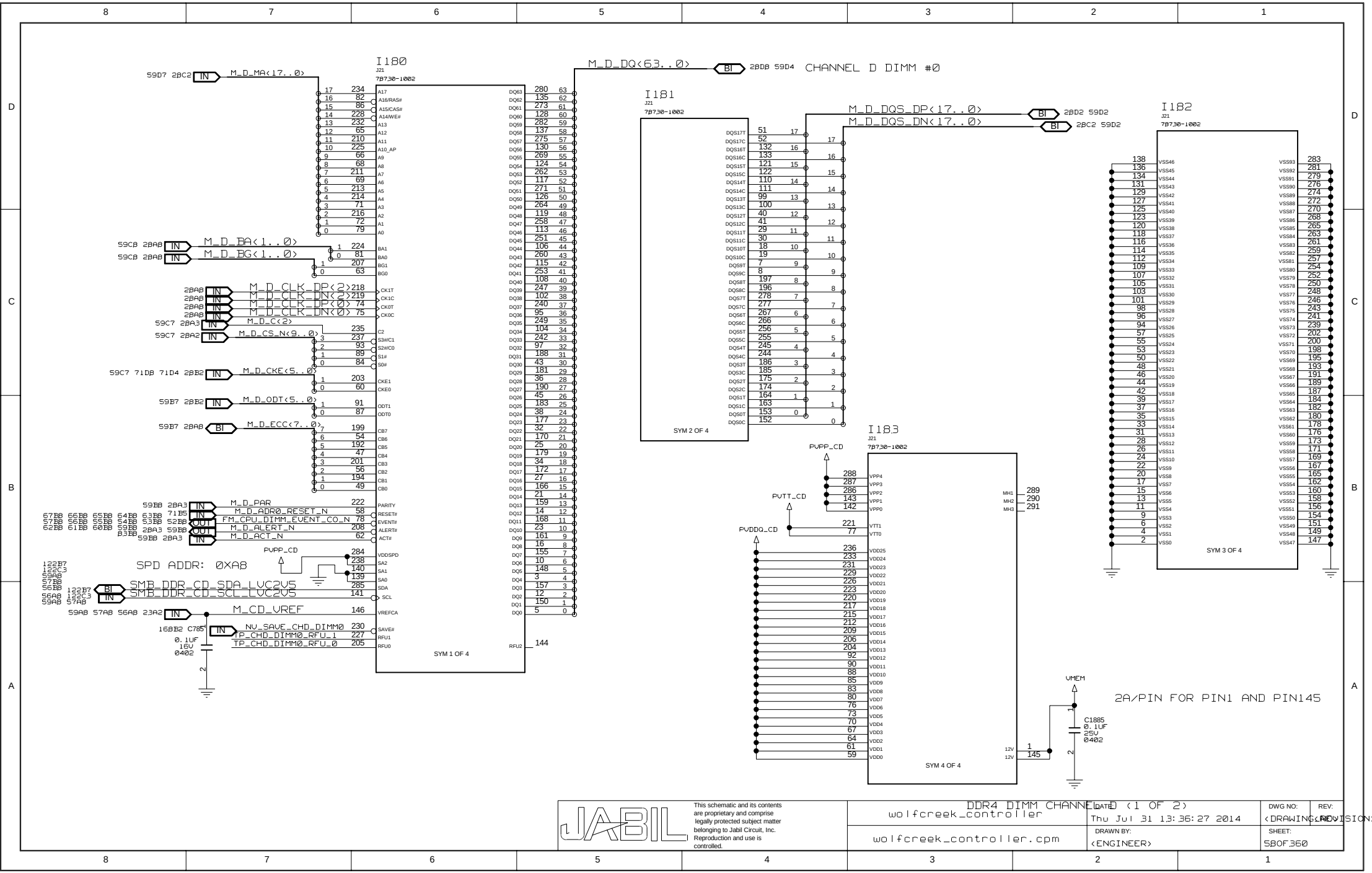
DDR4 DIMM CHANNEL C (2 OF 2)	DATE: Thu Jul 31 13:36:24 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 57OF360	



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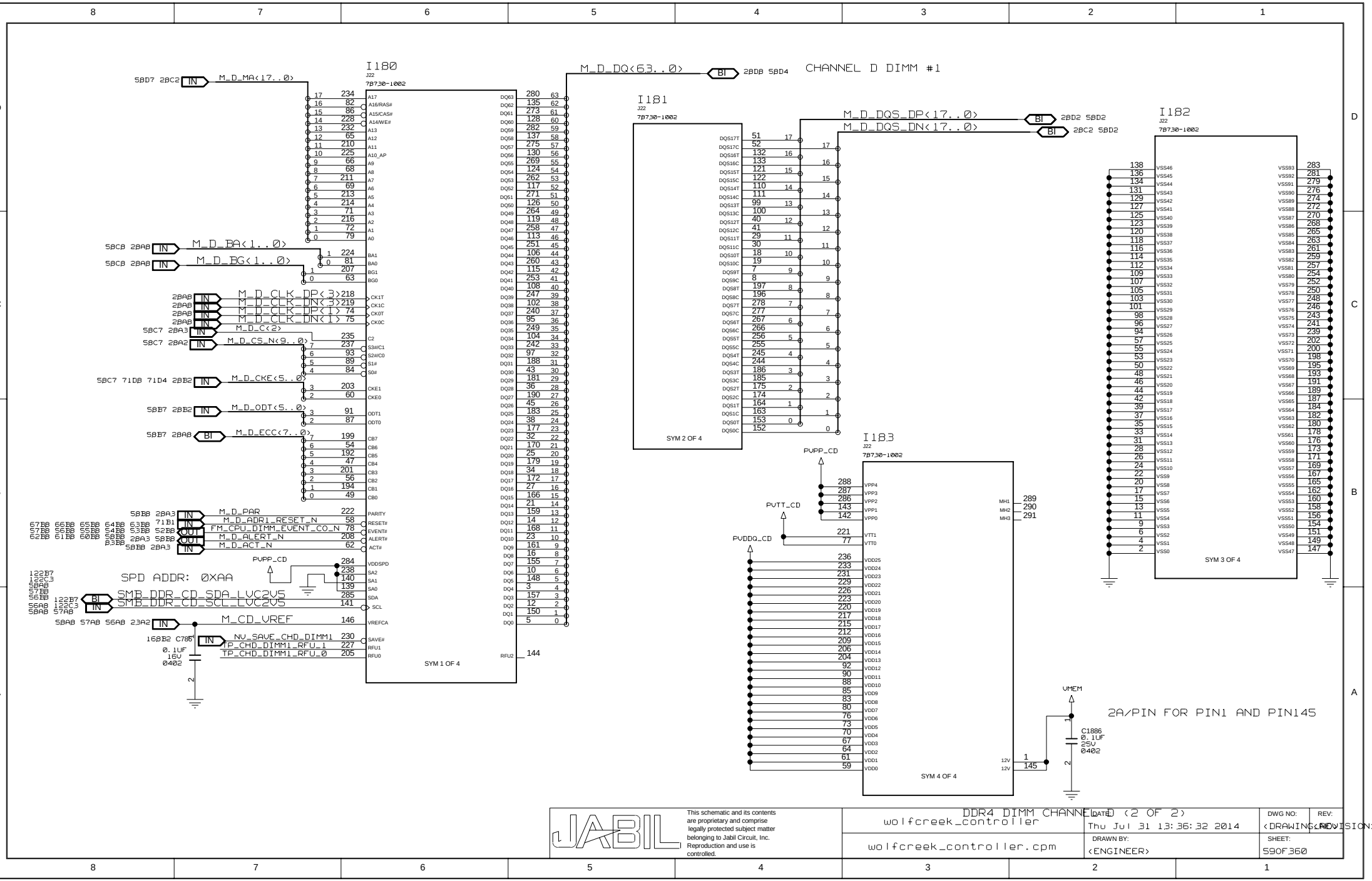
DDR4 DIMM CHANNEL D (1 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 13:36:27 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 58 OF 360


CHANNEL D DIMM #1
I180
J22
7B730-1002
SYM 1 OF 4
I181
J22
7B730-1002
SYM 2 OF 4
I182
J22
7B730-1002
SYM 3 OF 4
I183
J22
7B730-1002
SYM 4 OF 4
M_D_MA<17..0>
M_D_BA<1..0>
M_D_BG<1..0>
M_D_CLK_DP<3>
M_D_CLK_DN<3>
M_D_CLK_DP<1>
M_D_CLK_DN<1>
M_D_C<2>
M_D_CS_N<9..0>
M_D_CKE<5..0>
M_D_ODT<5..0>
M_D_ECC<7..0>
M_D_PAR
M_D_ADR1_RESET_N
FM_CPU_DIMM_EVENT_CO_N
M_D_ALERT_N
M_D_ACT_N
SPD ADDR: 0XAA
SMB_DDR_CD_SDA_LVC2V5
SMB_DDR_CD_SCL_LVC2V5
M_CD_VREF
NV_SAVE_CHD_DIMM1
TP_CHD_DIMM1_RFU_1
TP_CHD_DIMM1_RFU_0
M_D_DQ<63..0>
M_D_DQS_DP<17..0>
M_D_DQS_DN<17..0>
PVPP_CD
PVTT_CD
PVDDQ_CD
VMEM
C1886
0.1UF
25V
0402
2A/PIN FOR PIN1 AND PIN145
JABIL
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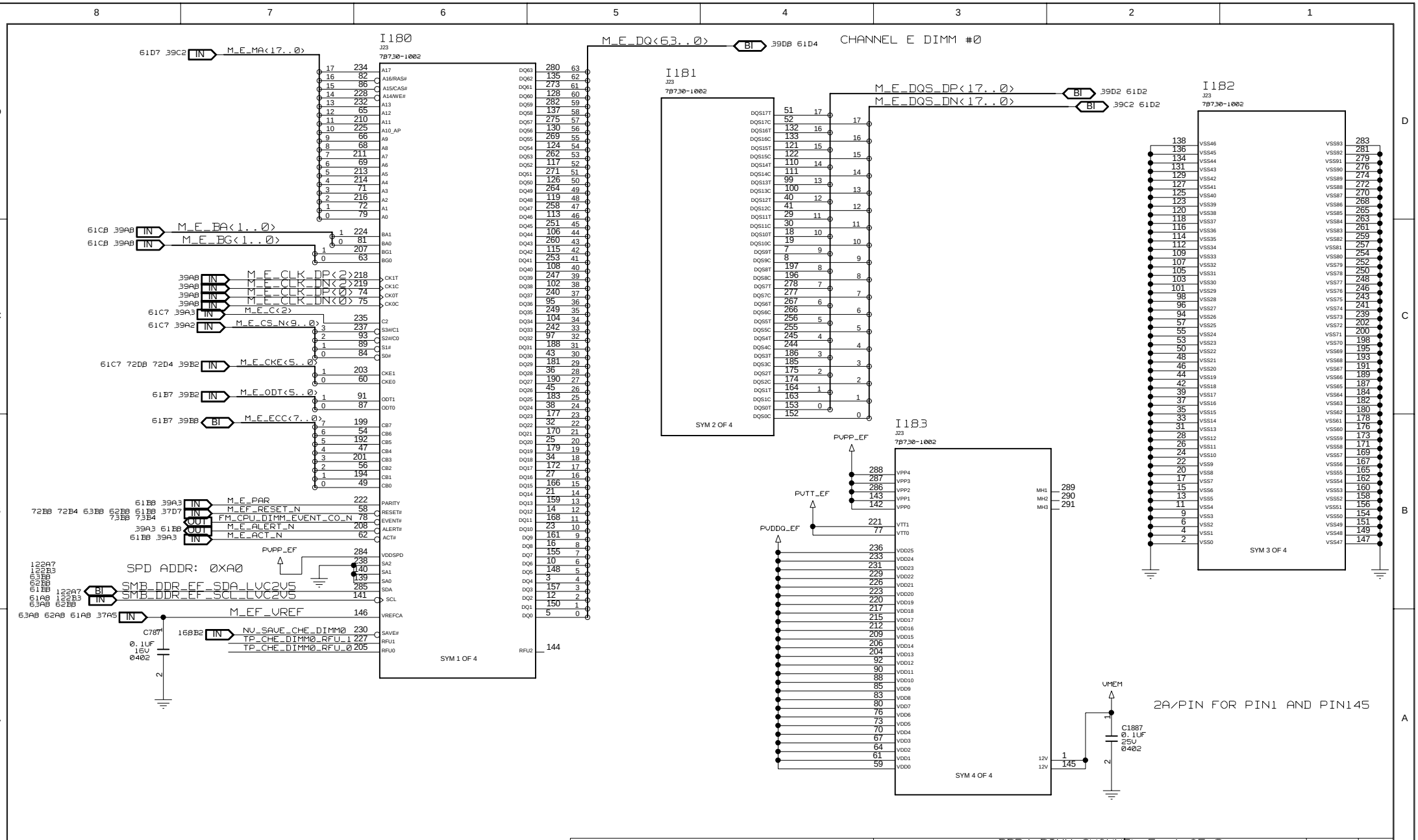
DDR4 DIMM CHANNEL D (2 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Thu Jul 31 13:36:32 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 59OF360



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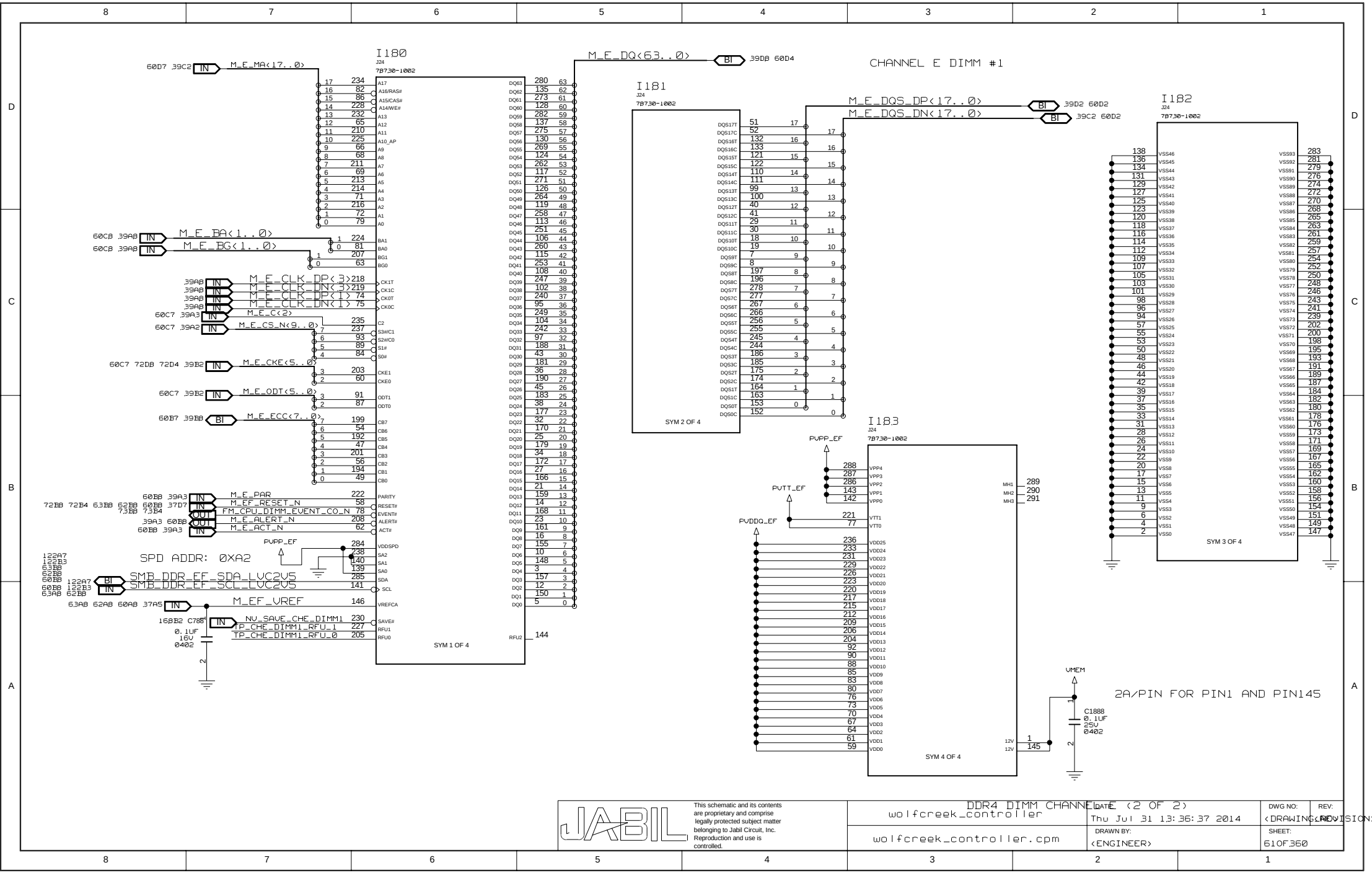
DDR4 DIMM CHANNEL E (1 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 13:36:35 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 60OF360



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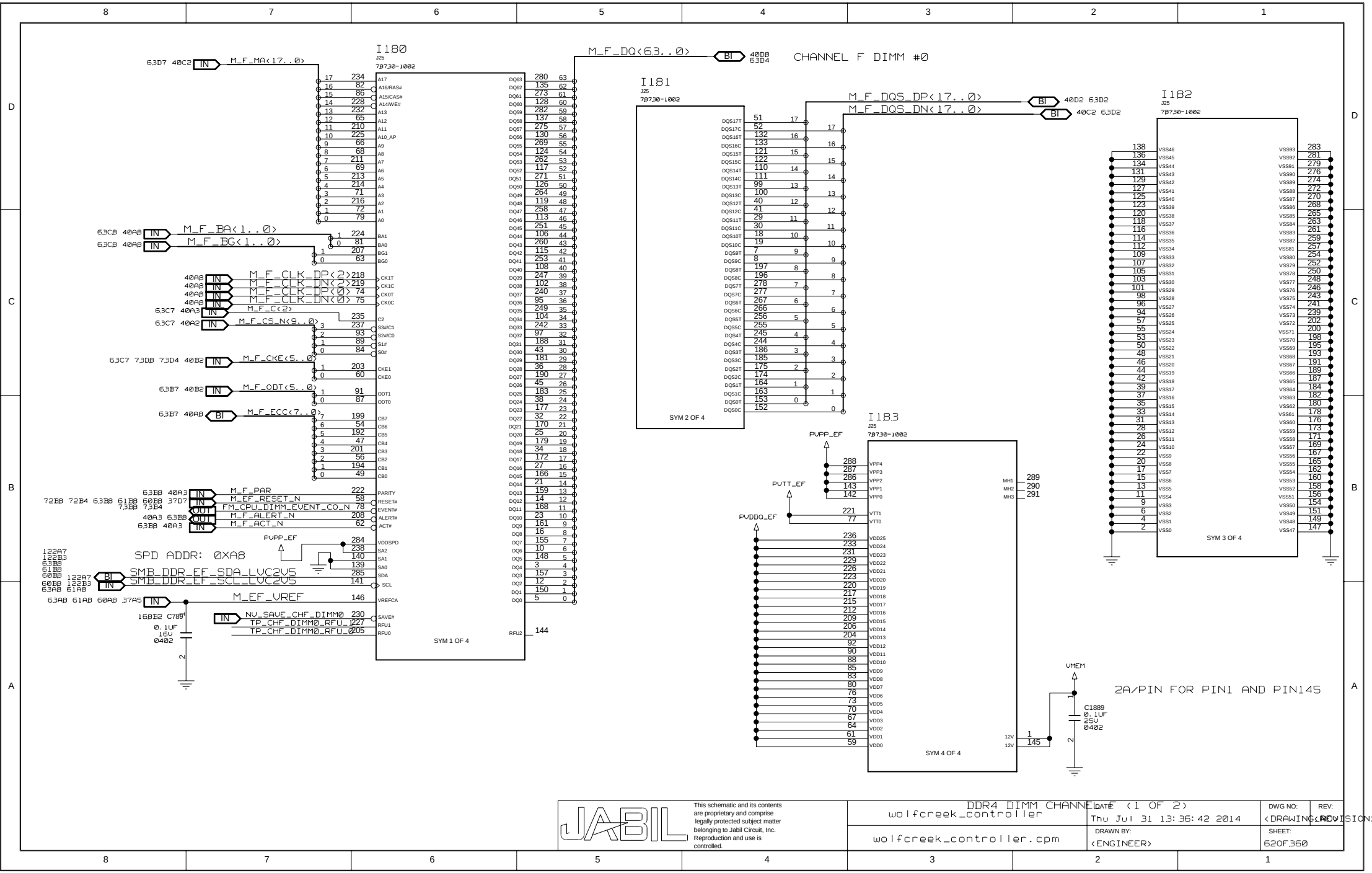
DDR4 DIMM CHANNEL E (2 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 13:36:37 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 61 OF 360



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DDR4 DIMM CHANNEL F (1 OF 2)
wolfcreek_controller

wolfcreek_controller.cpm

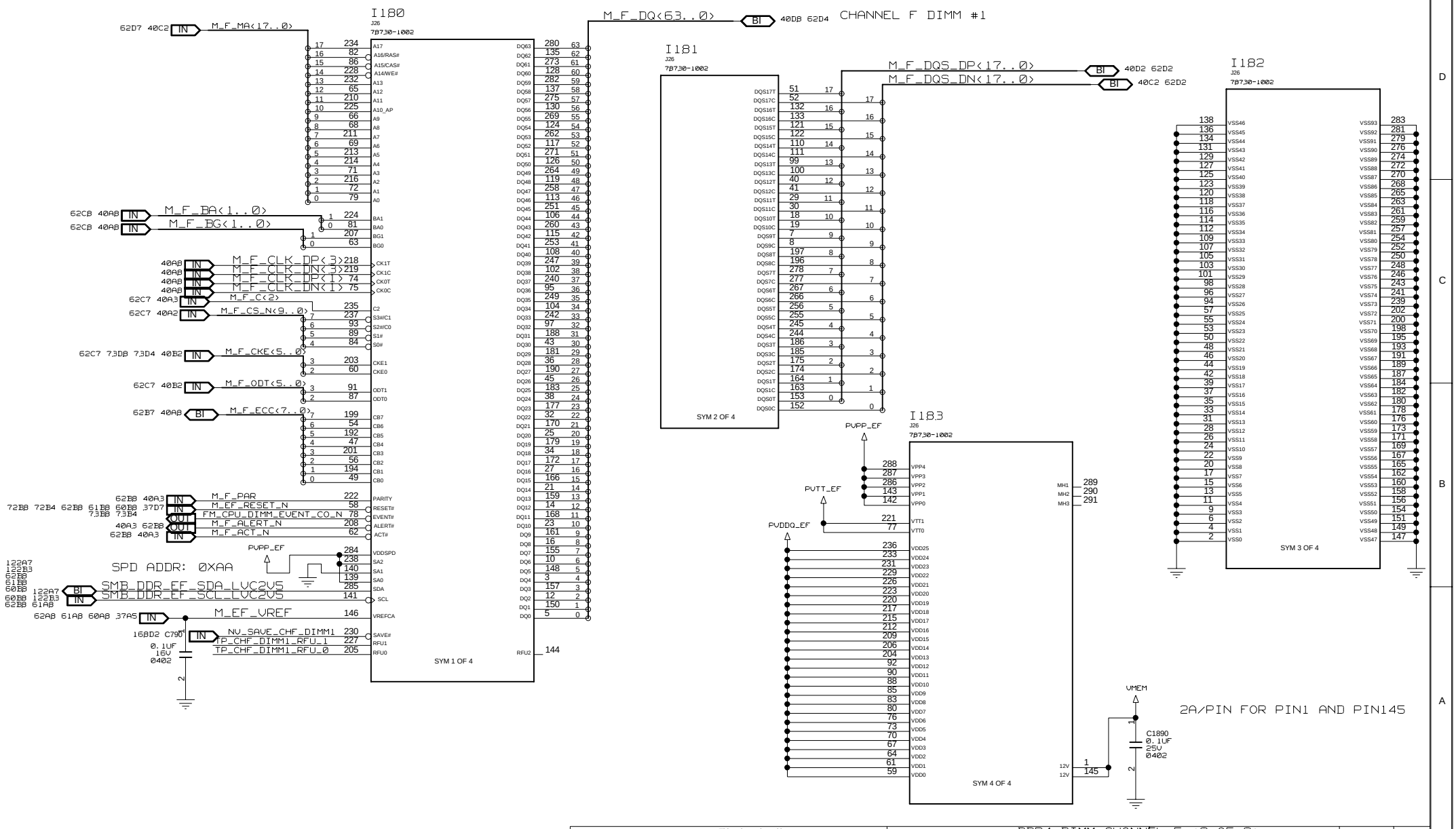
DATE: Thu Jul 31 13:36:42 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 62OF360


I180
J26
7B730-1002
SYM 1 OF 4
M_F_MA<17..0>
M_F_BA<1..0>
M_F_BG<1..0>
M_F_CLK_DP<3>
M_F_CLK_DN<3>
M_F_CLK_DP<1>
M_F_CLK_DN<1>
M_F_C<2>
M_F_CS_N<9..0>
M_F_CKE<5..0>
M_F_ODT<5..0>
M_F_ECC<7..0>
M_F_PAR
M_EF_RESET_N
FM_CPU_DIMM_EVENT_CO_N
M_F_ALERT_N
M_F_ACT_N
SPD ADDR: 0XAA
SMB_DDR_EF_SDA_LVC2V5
SMB_DDR_EF_SCL_LVC2V5
M_EF_VREF
NV_SAVE_CHF_DIMM1
TP_CHF_DIMM1_RFU_1
TP_CHF_DIMM1_RFU_0
PVPP_EF
M_F_DQ<63..0>
CHANNEL F DIMM #1
I181
J26
7B730-1002
SYM 2 OF 4
M_F_DQS_DP<17..0>
M_F_DQS_DN<17..0>
I182
J26
7B730-1002
SYM 3 OF 4
I183
J26
7B730-1002
SYM 4 OF 4
PVTT_EF
PVDDQ_EF
VMEM
C1890
0.1UF
25V
0402
2A/PIN FOR PIN1 AND PIN145
JABIL
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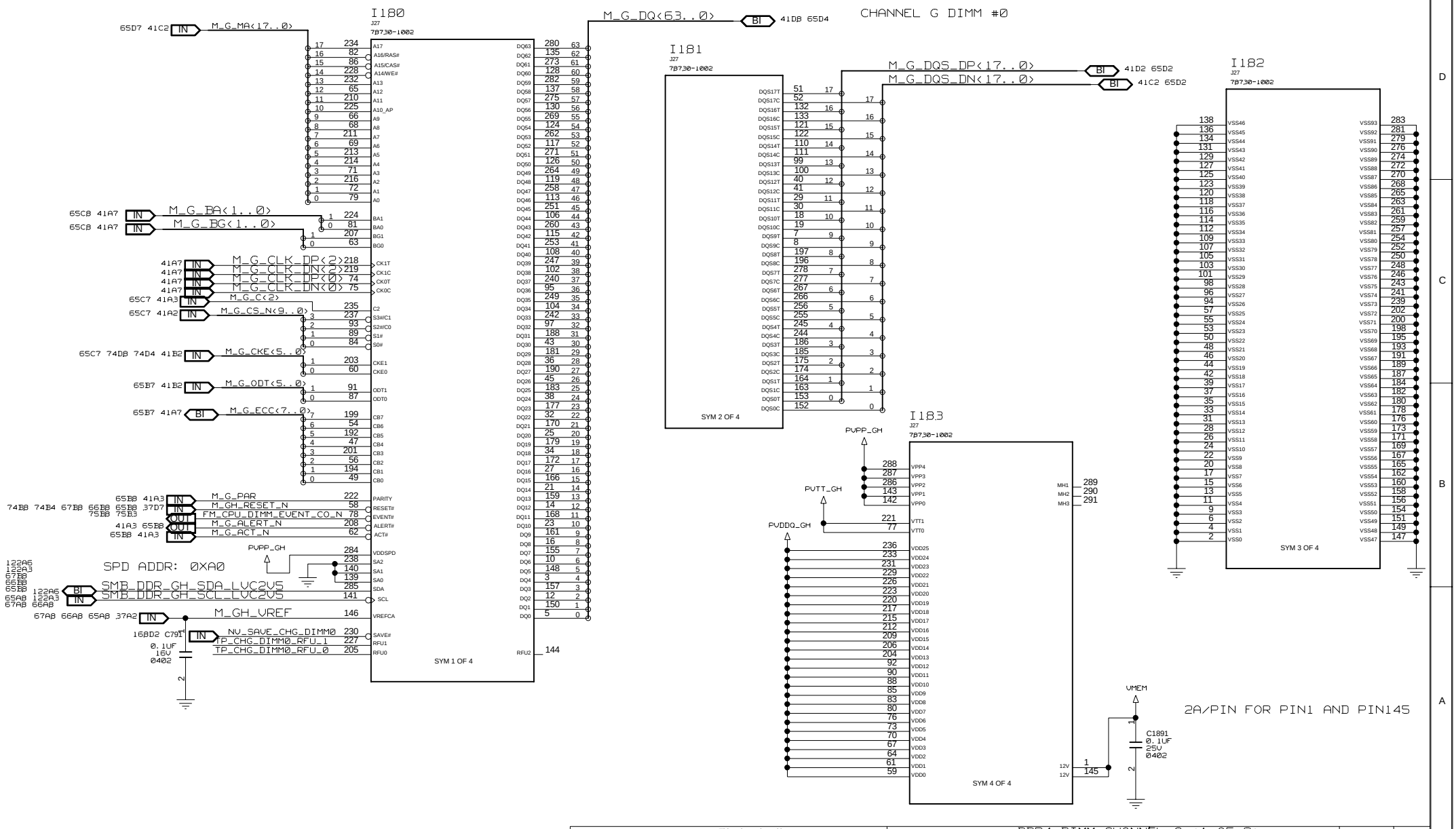
DDR4 DIMM CHANNEL F (2 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Thu Jul 31 13:36:45 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 63OF360



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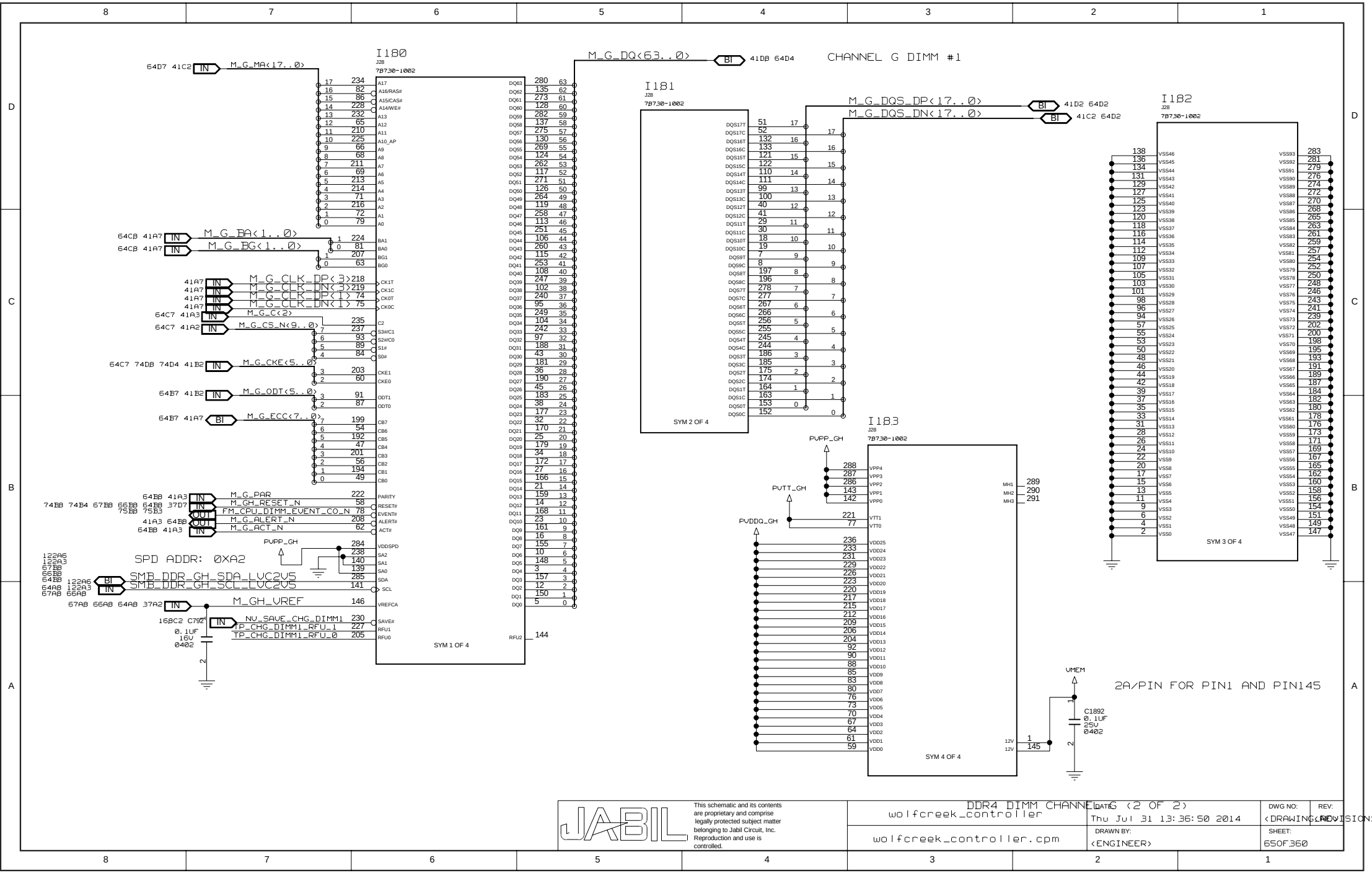
DDR4 DIMM CHANNEL G (1 OF 2)	DATE: Thu Jul 31 13:36:47 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 64OF360	



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DDR4 DIMM CHANNEL G (2 OF 2)

wolfcreek_controller

wolfcreek_controller.cpm

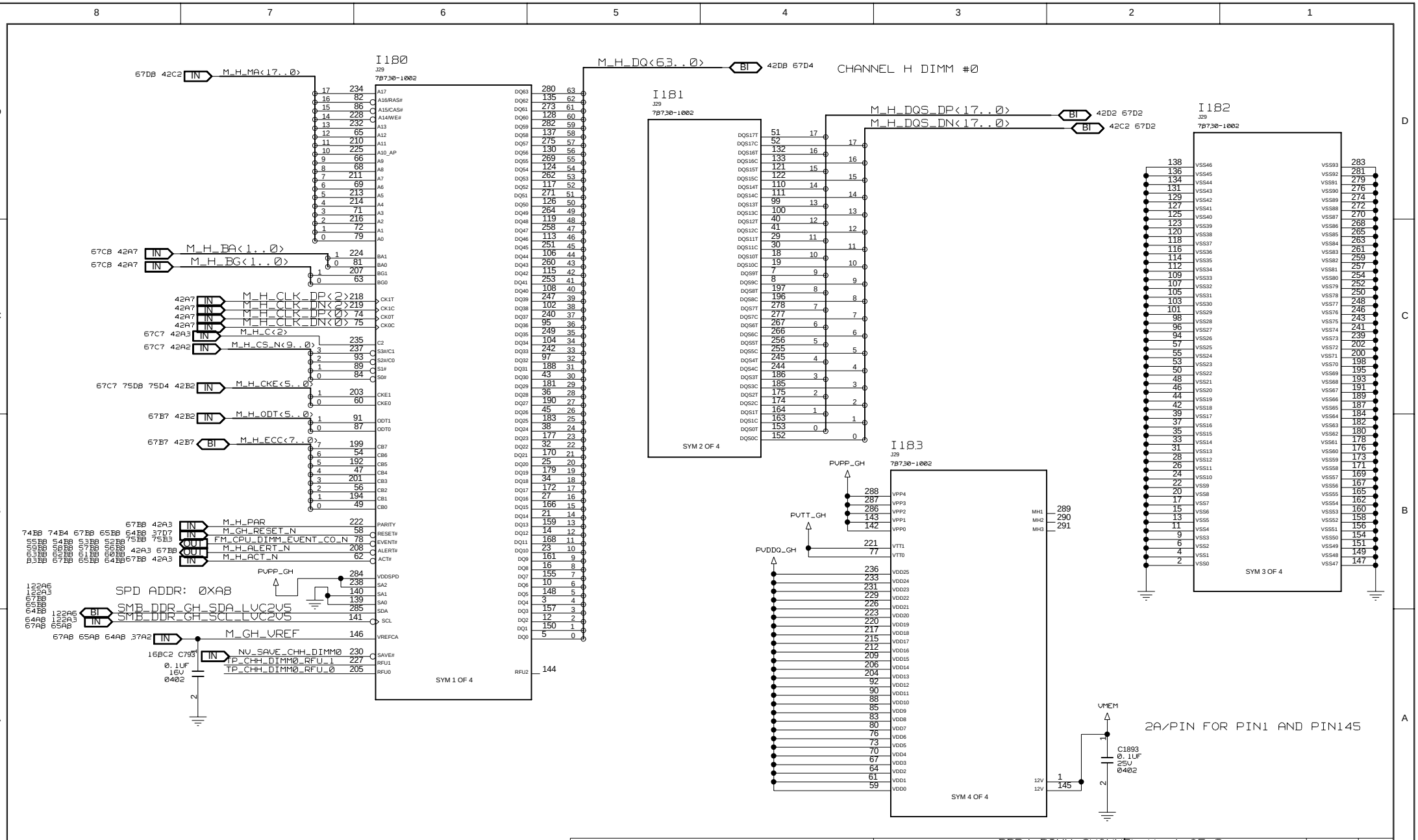
DATE: Thu Jul 31 13:36:50 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 65OF360



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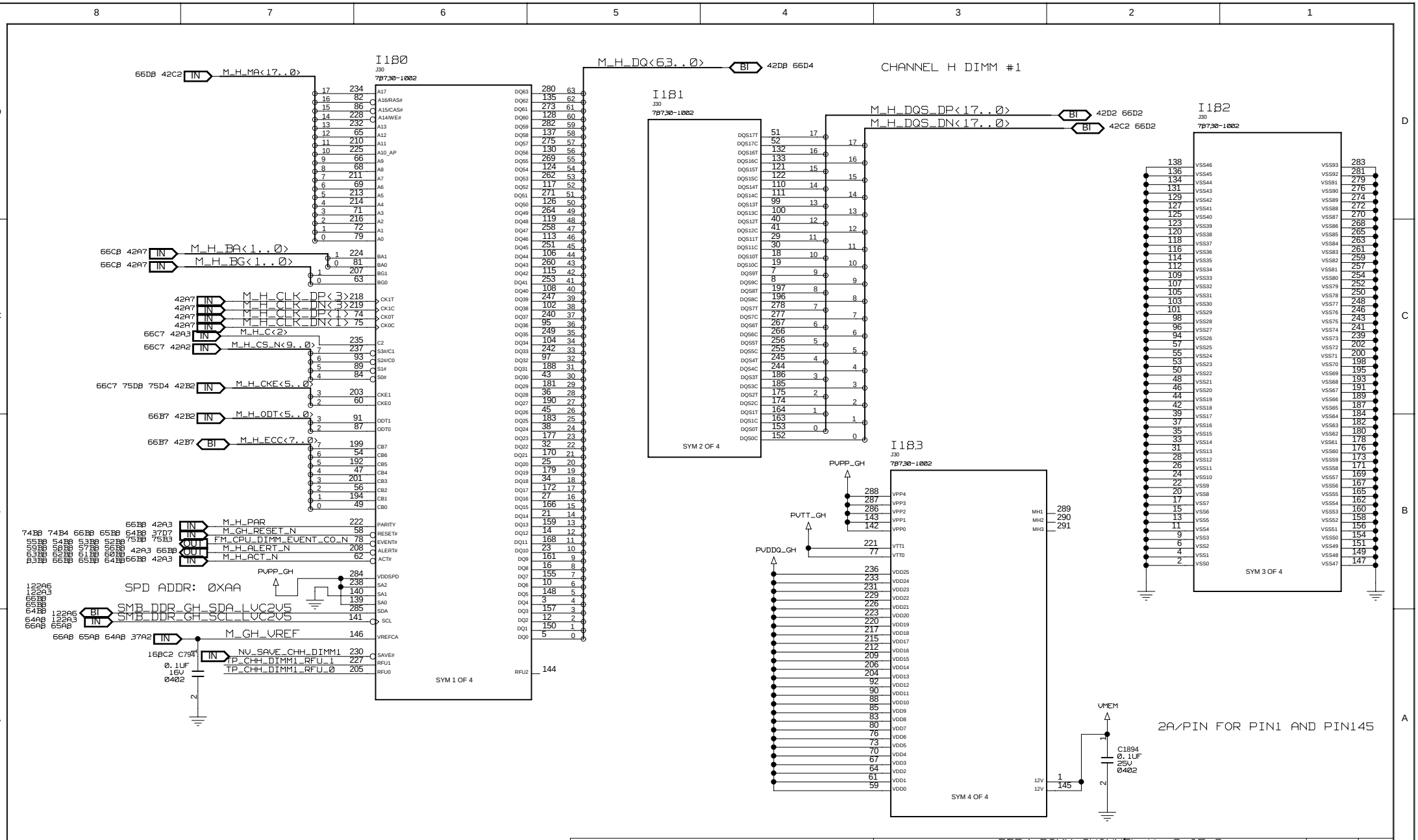
DDR4 DIMM CHANNEL H (1 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 13:36:53 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 66OF360



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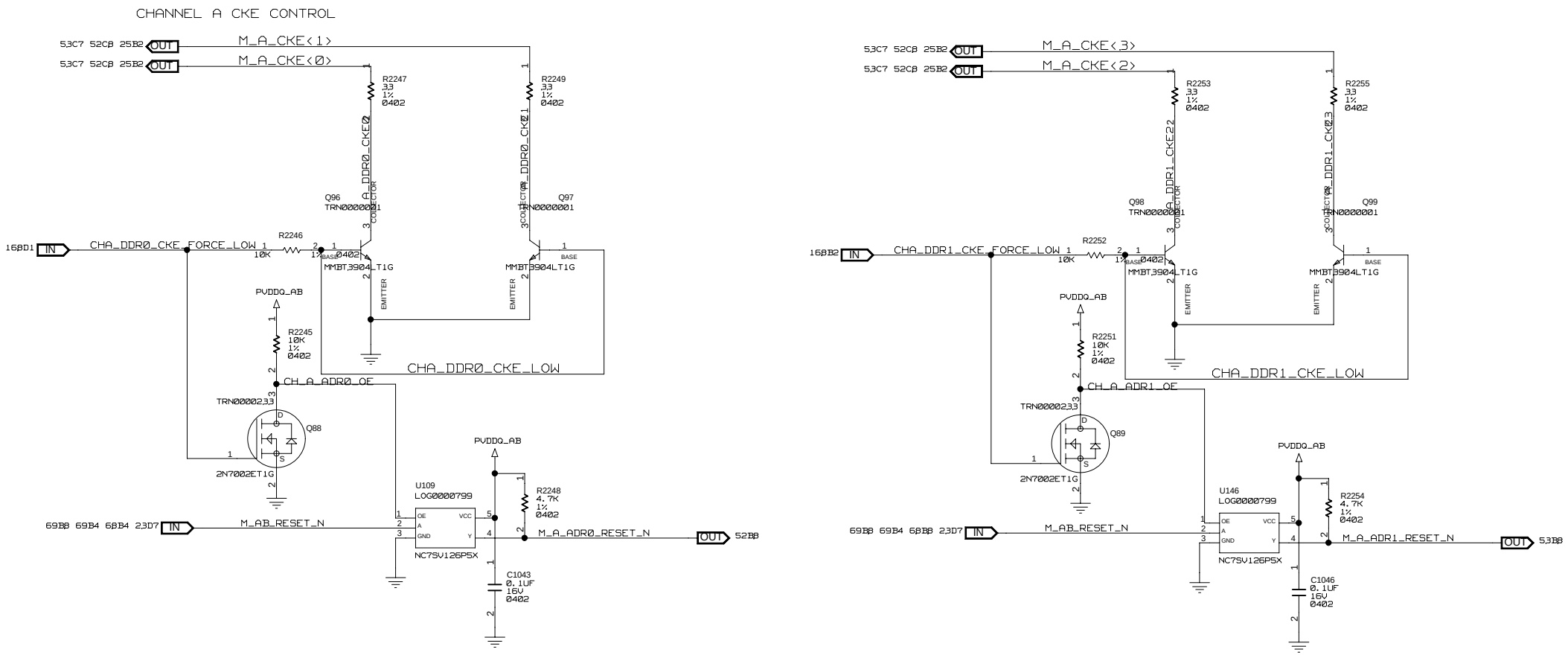
DDR4 DIMM CHANNEL H (2 OF 2)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 13:40:35 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 67OF360



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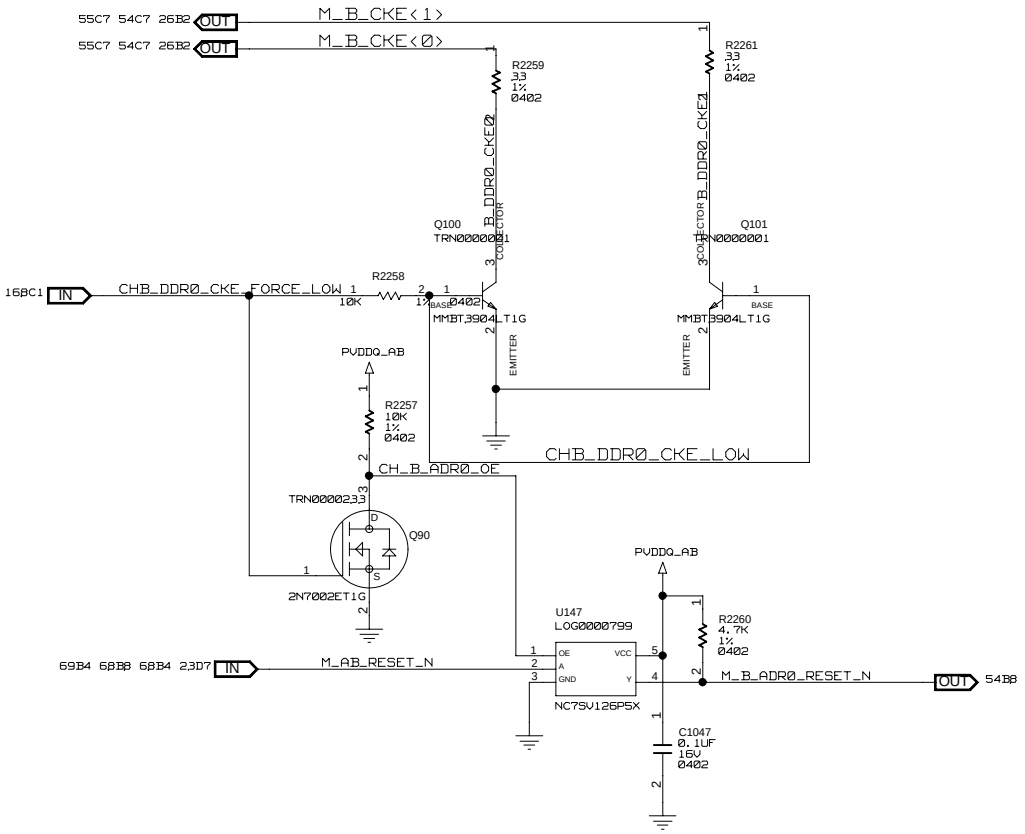
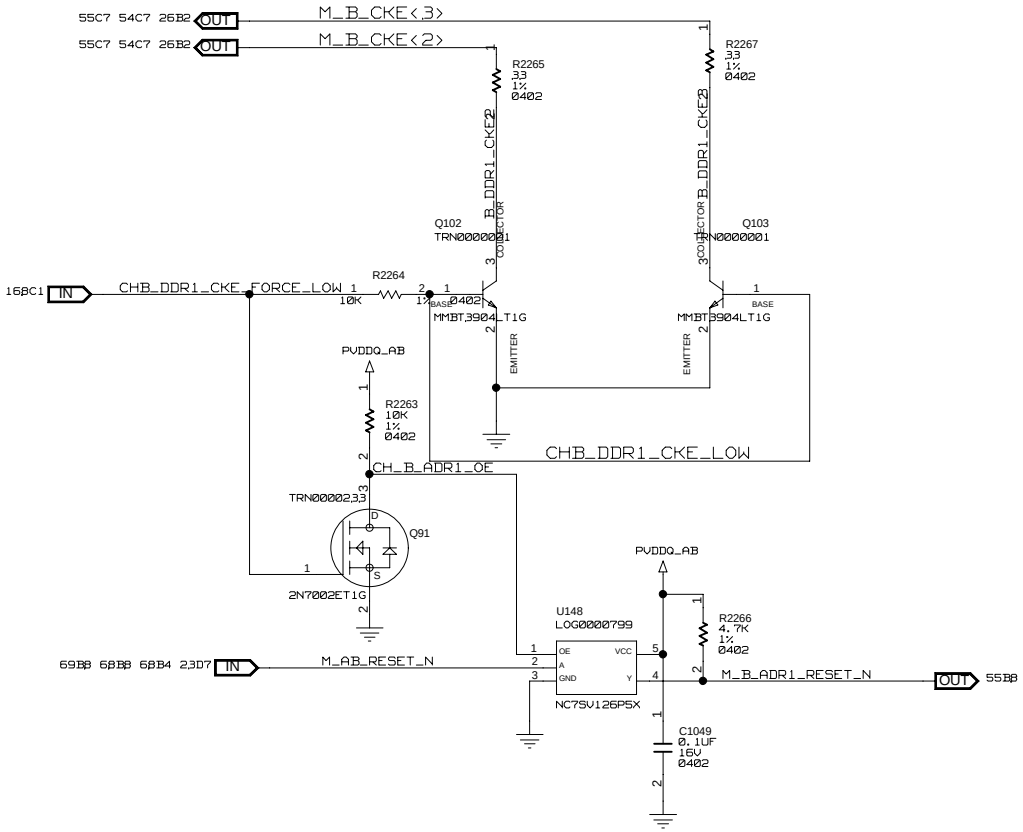
CH A ADR CKE CIRCUIT
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Thu Jul 31 11:17:44 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 60OF360

CHANNEL B CKE CONTROL





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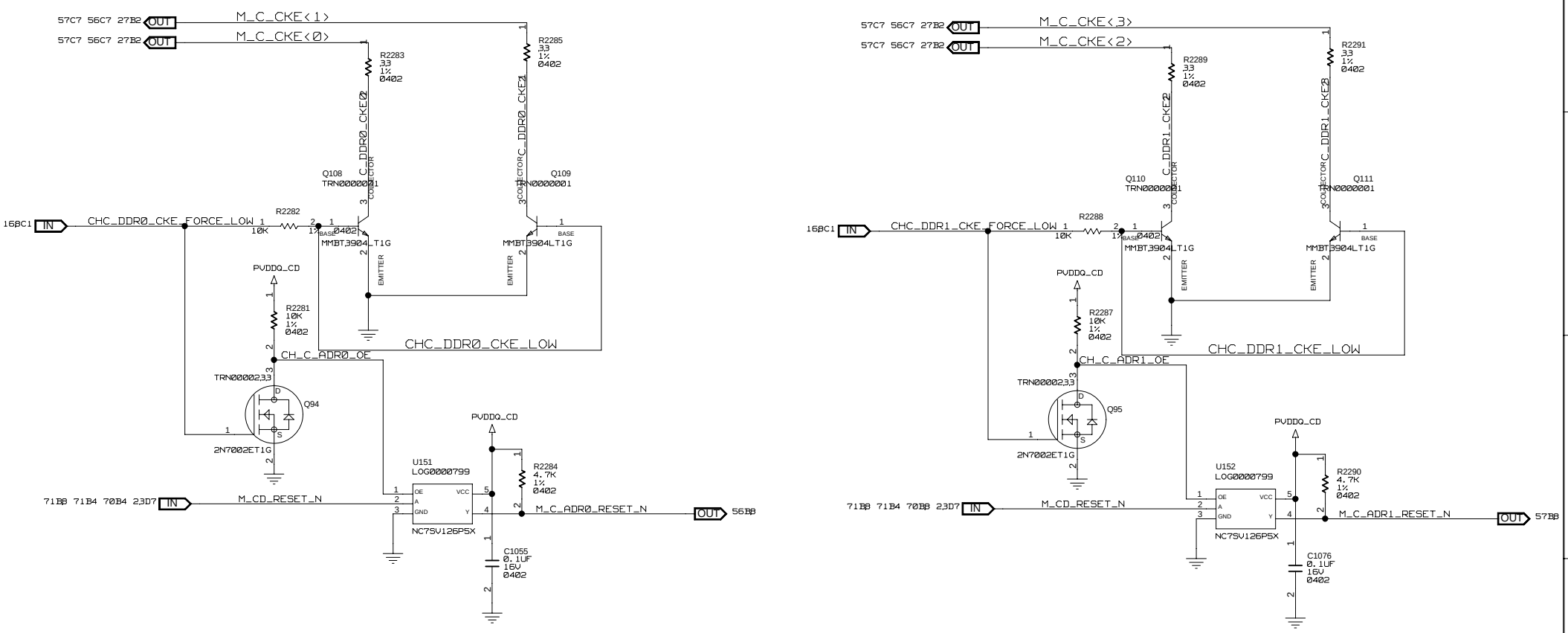
CH B ADR CKE CIRCUIT wolfcreek_controller	DATE: Thu Jul 31 11:11:24 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 69OF360	

CHANNEL C CKE CONTROL



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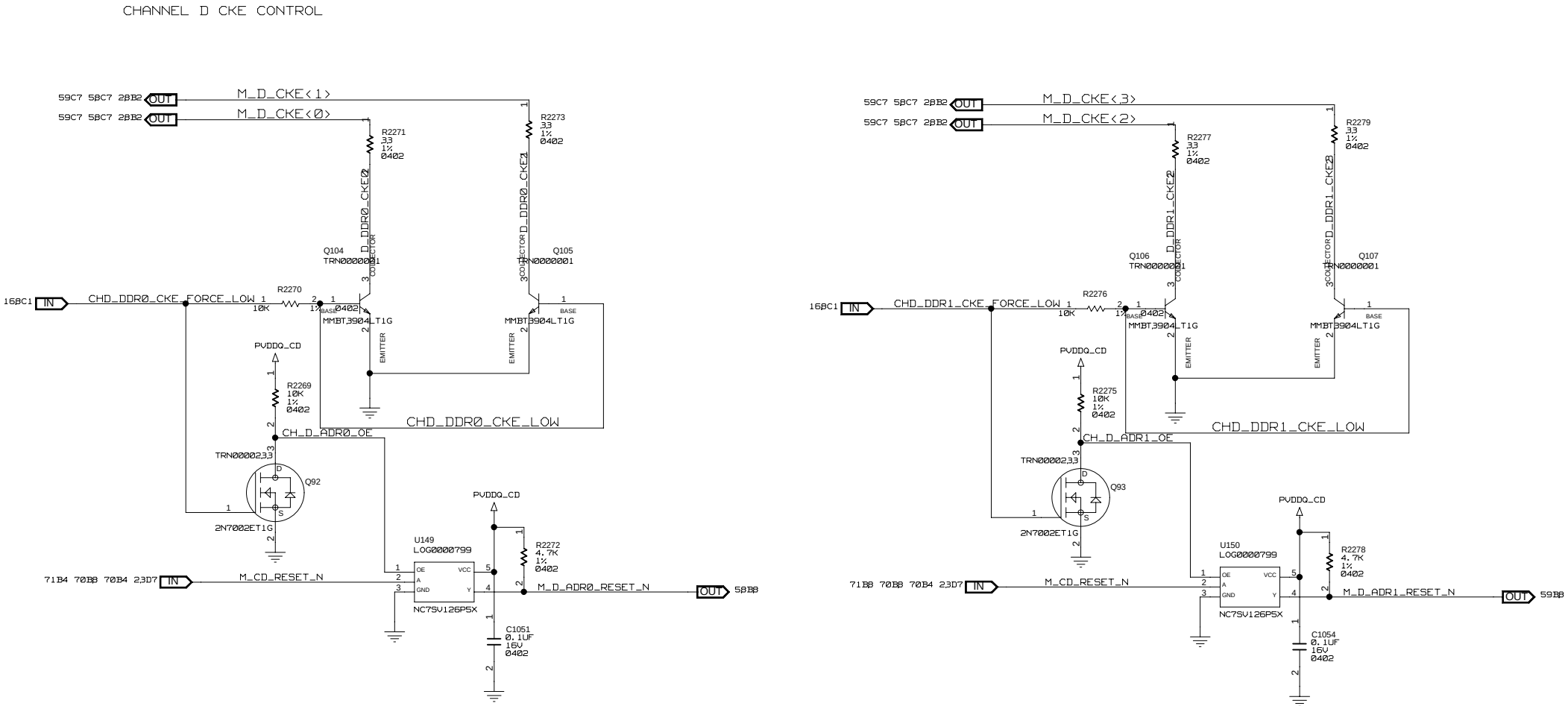
CH C ADR CKE CIRCUIT wolfcreek_controller	DATE: Thu Jul 31 11:38:13 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 70OF360	



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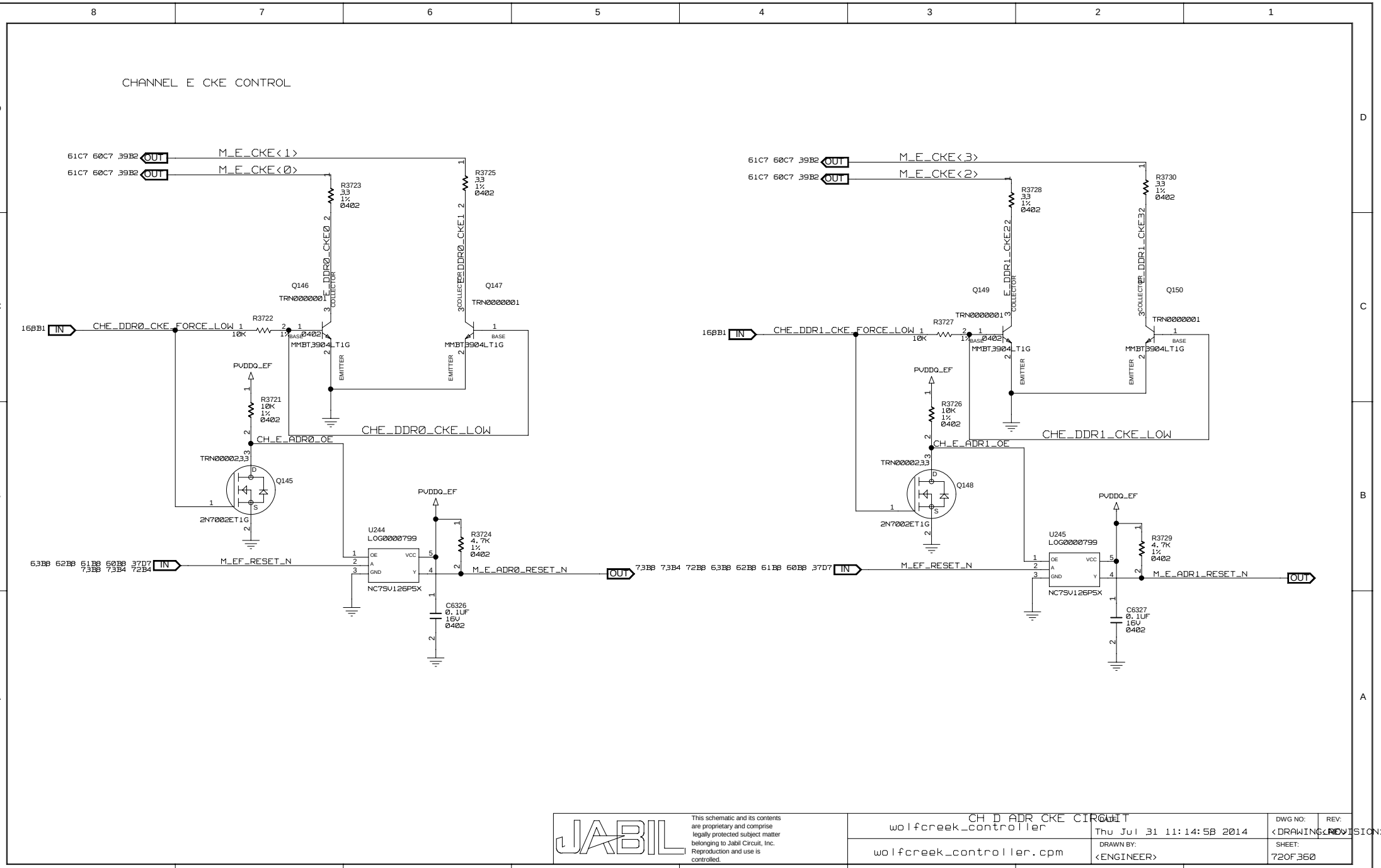
CH D ADR CKE CIRCUIT wolfcreek_controller	DATE: Thu Jul 31 11:12:32 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 71OF360	


CHANNEL E CKE CONTROL
M_E_CKE<1>
M_E_CKE<0>
M_E_CKE<3>
M_E_CKE<2>
OUT
R3723 3.3 1% 0402
R3725 3.3 1% 0402
R3728 3.3 1% 0402
R3730 3.3 1% 0402
E_DDR0_CKE0
E_DDR0_CKE1
E_DDR1_CKE2
E_DDR1_CKE3
Q146 TRN0000001
Q147 TRN0000001
Q149 TRN0000001
Q150 TRN0000001
MMBT3904LT1G
COLLECTOR
BASE
EMITTER
IN
CHE_DDR0_CKE_FORCE_LOW
CHE_DDR1_CKE_FORCE_LOW
R3722 10K 1% 0402
R3727 10K 1% 0402
PVDDQ_EF
R3721 10K 1% 0402
R3726 10K 1% 0402
CHE_DDR0_CKE_LOW
CHE_DDR1_CKE_LOW
CH_E_ADR0_OE
CH_E_ADR1_OE
TRN0000233
Q145
Q148
2N7002ET1G
U244 LOG0000799
U245 LOG0000799
OE
A
GND
VCC
Y
NC7SV126P5X
R3724 4.7K 1% 0402
R3729 4.7K 1% 0402
M_EF_RESET_N
M_E_ADR0_RESET_N
M_E_ADR1_RESET_N
C6326 0.1UF 16V 0402
C6327 0.1UF 16V 0402
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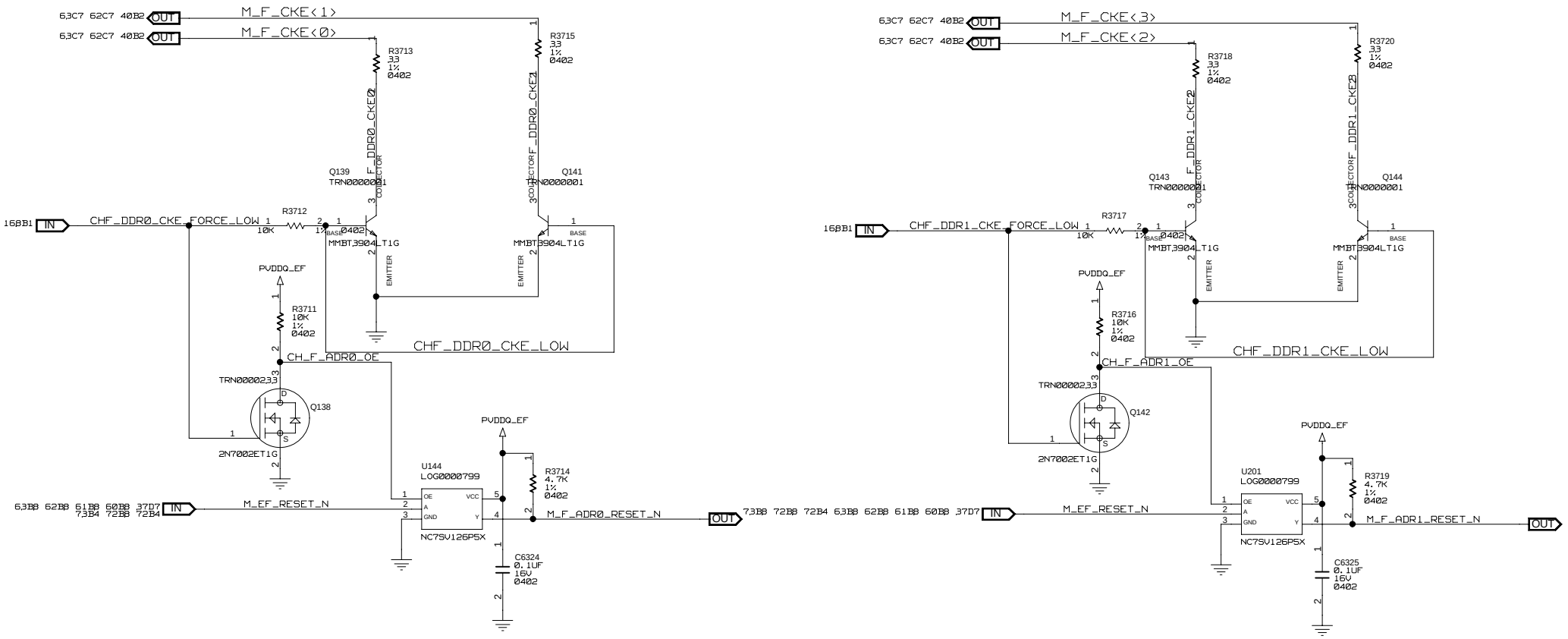
CH D ADR CKE CIRCUIT
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Thu Jul 31 11:14:58 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 72OF360

CHANNEL F CKE CONTROL



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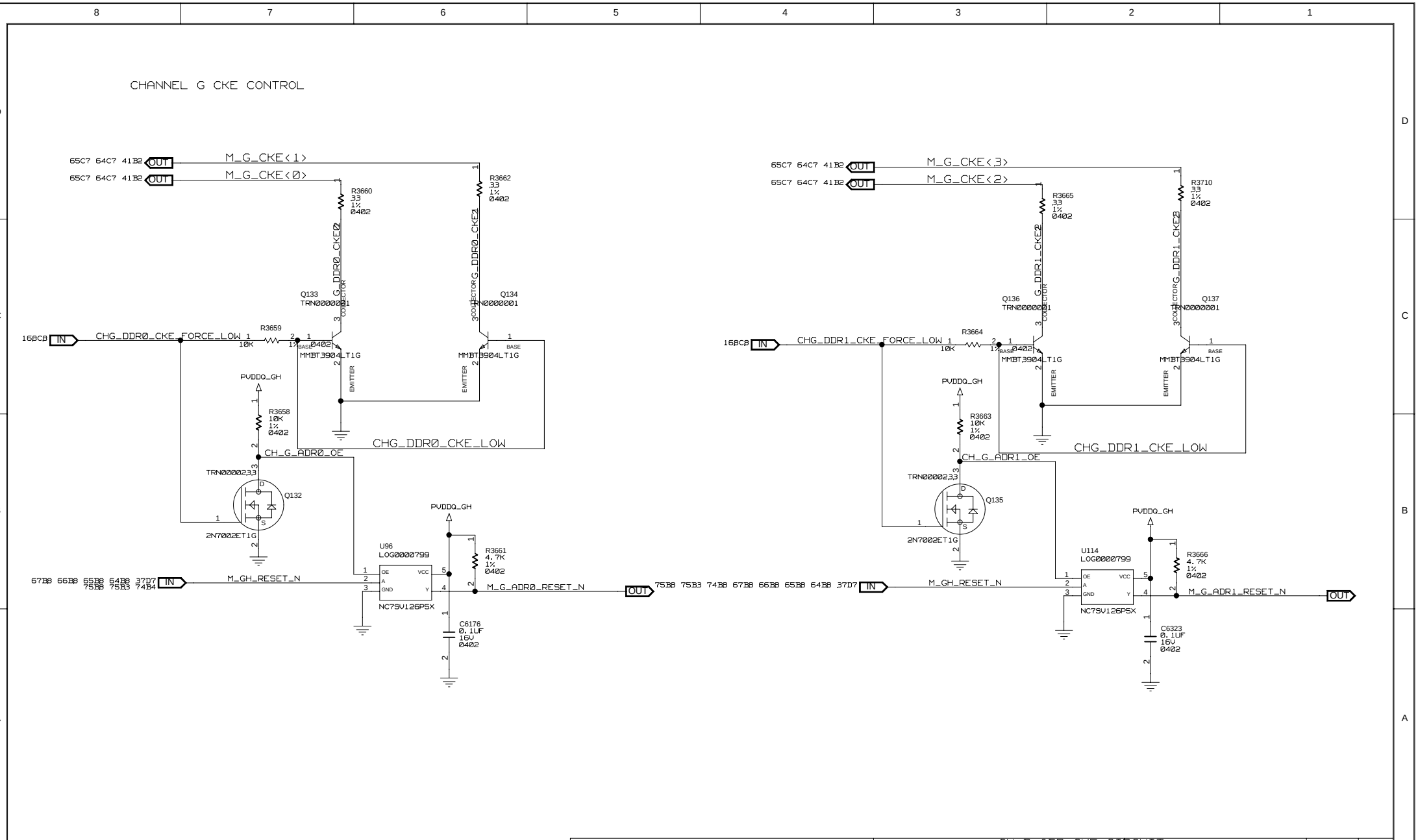
CH D ADR CKE CIRCUIT wolfcreek_controller	DATE: Thu Jul 31 11:25:35 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 7,30F,360	



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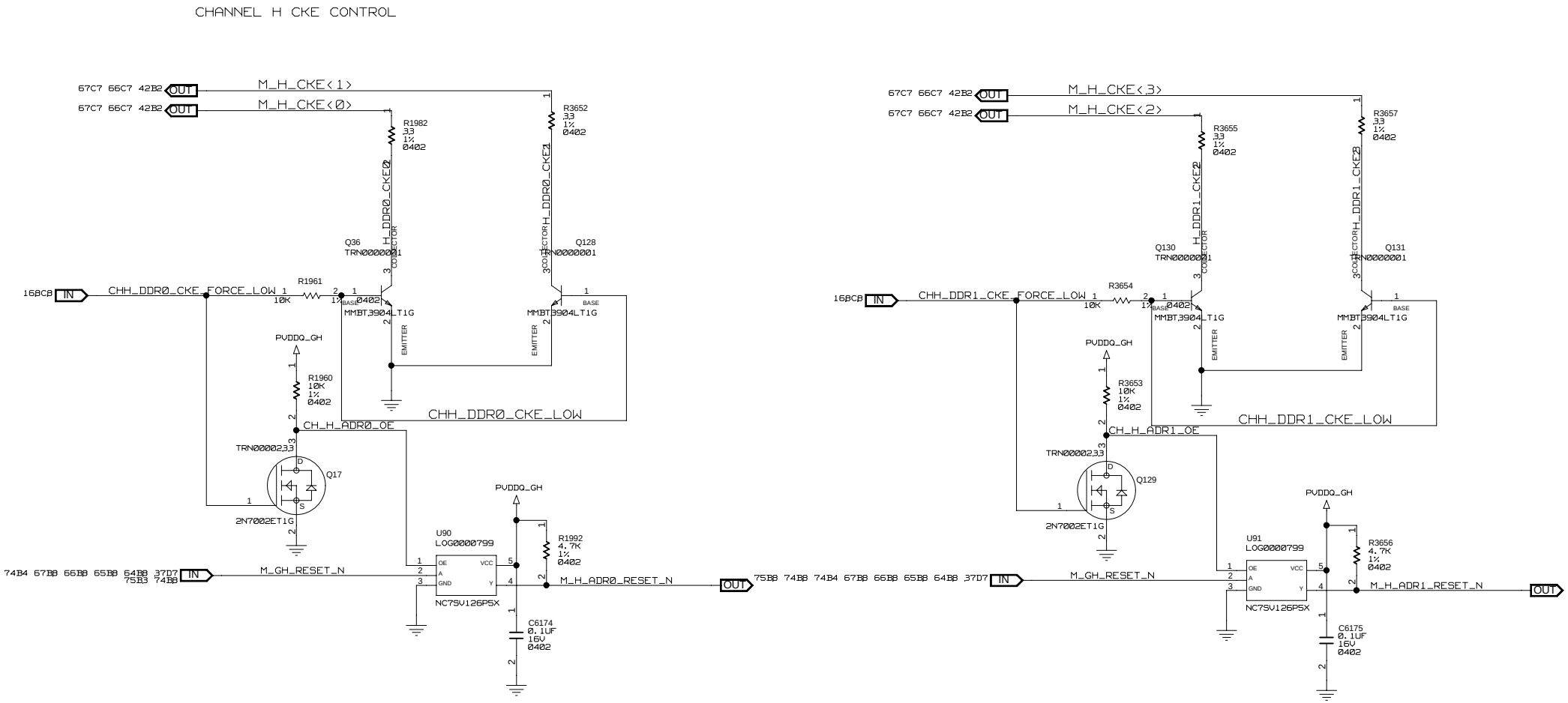
CH D ADR CKE CIRCUIT	DATE: Thu Jul 31 11:28:51 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 74OF360	



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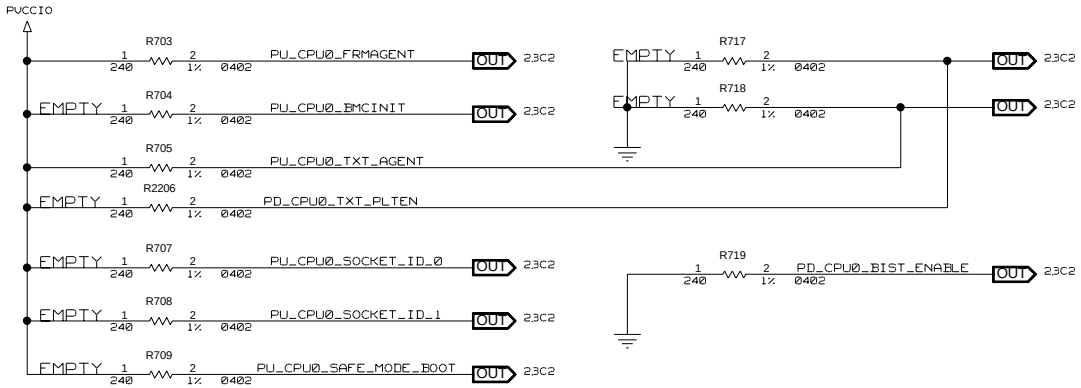
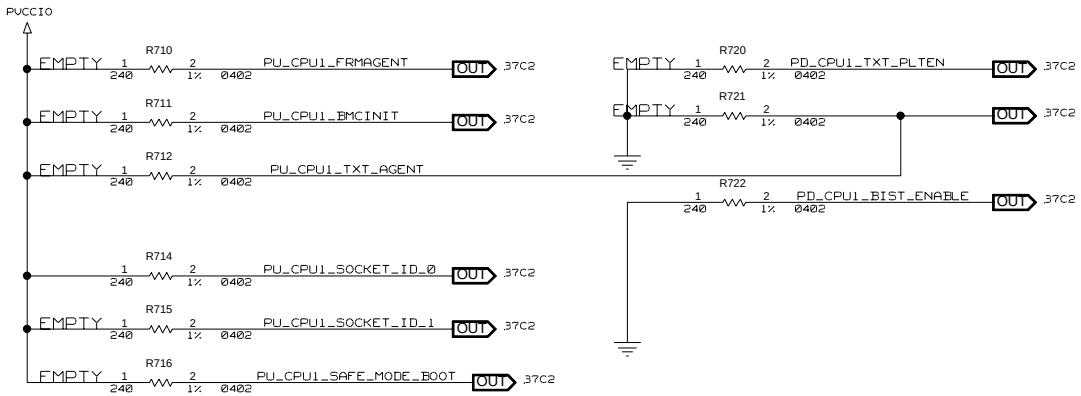
BLANK wolfcreek_controller	DATE: Thu Jul 31 18:04:14 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 75OF360	

STRAPS (CPU0)



A CONFIG TABLE WILL BE ADDED HERE

STRAPS (CPU1)



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CPU SIDE BAND: HW STRAPS

wolfcreek_controller

wolfcreek_controller.cpm

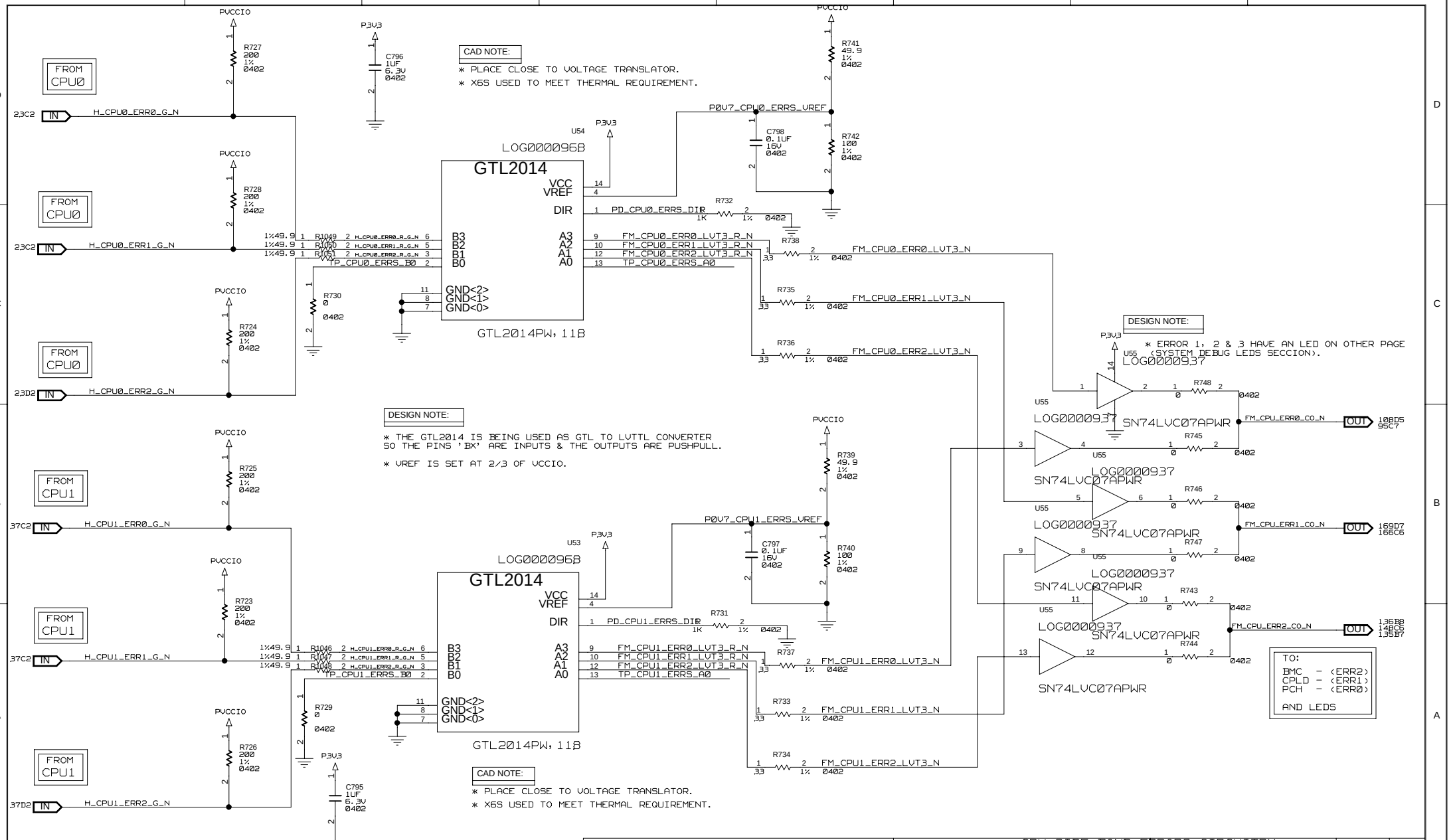
DATE: Wed Jul 30 14:58:41 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 76OF360



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CPU SIDE BAND:ERRORS CIRCUITRY

wolfcreek_controller

wolfcreek_controller.cpm

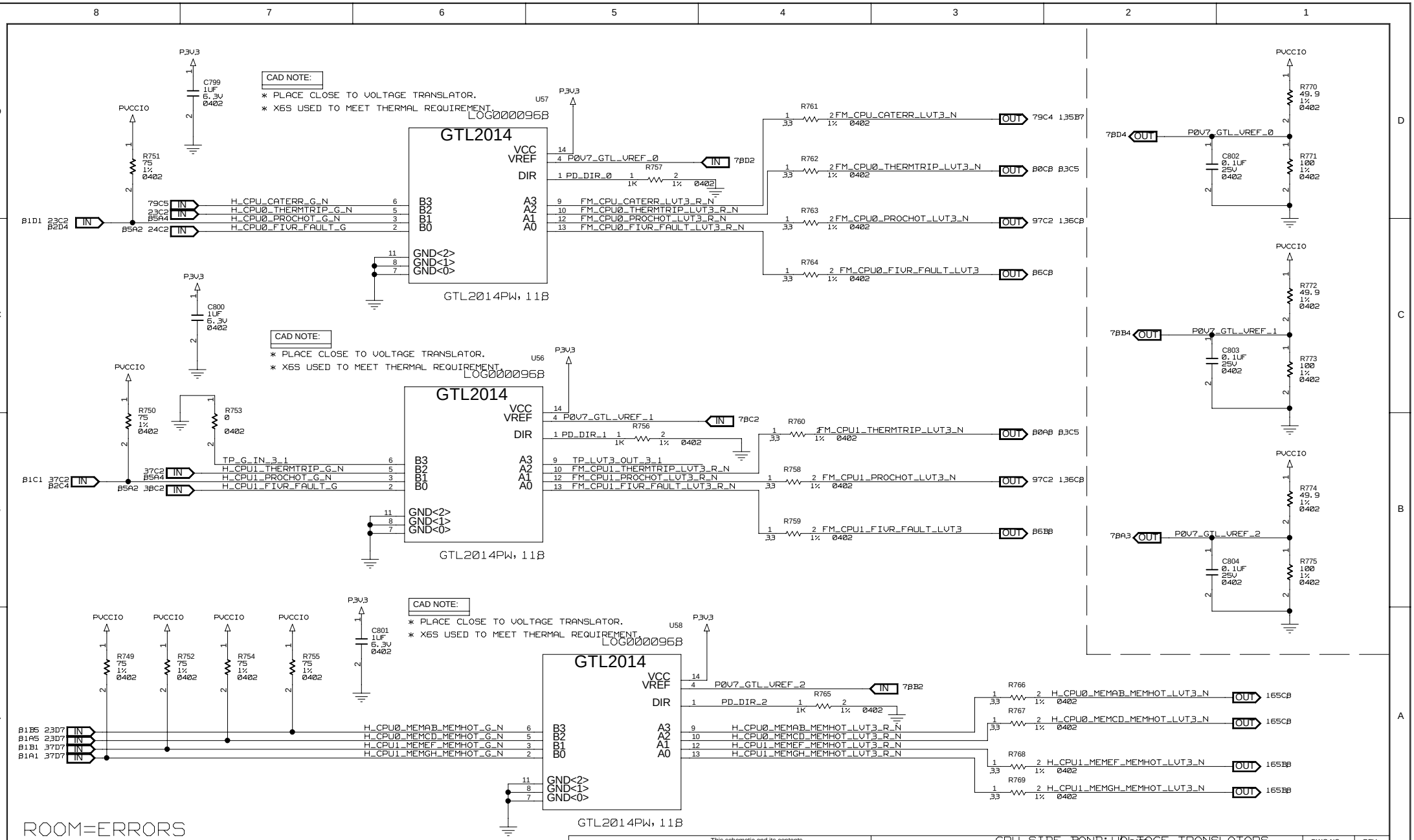
DATE: Wed Jul 30 14:58:42 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 77OF360



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CPU SIDE BAND: VOLTAGE TRANSLATORS

wolfcreek_controller

wolfcreek_controller.cpm

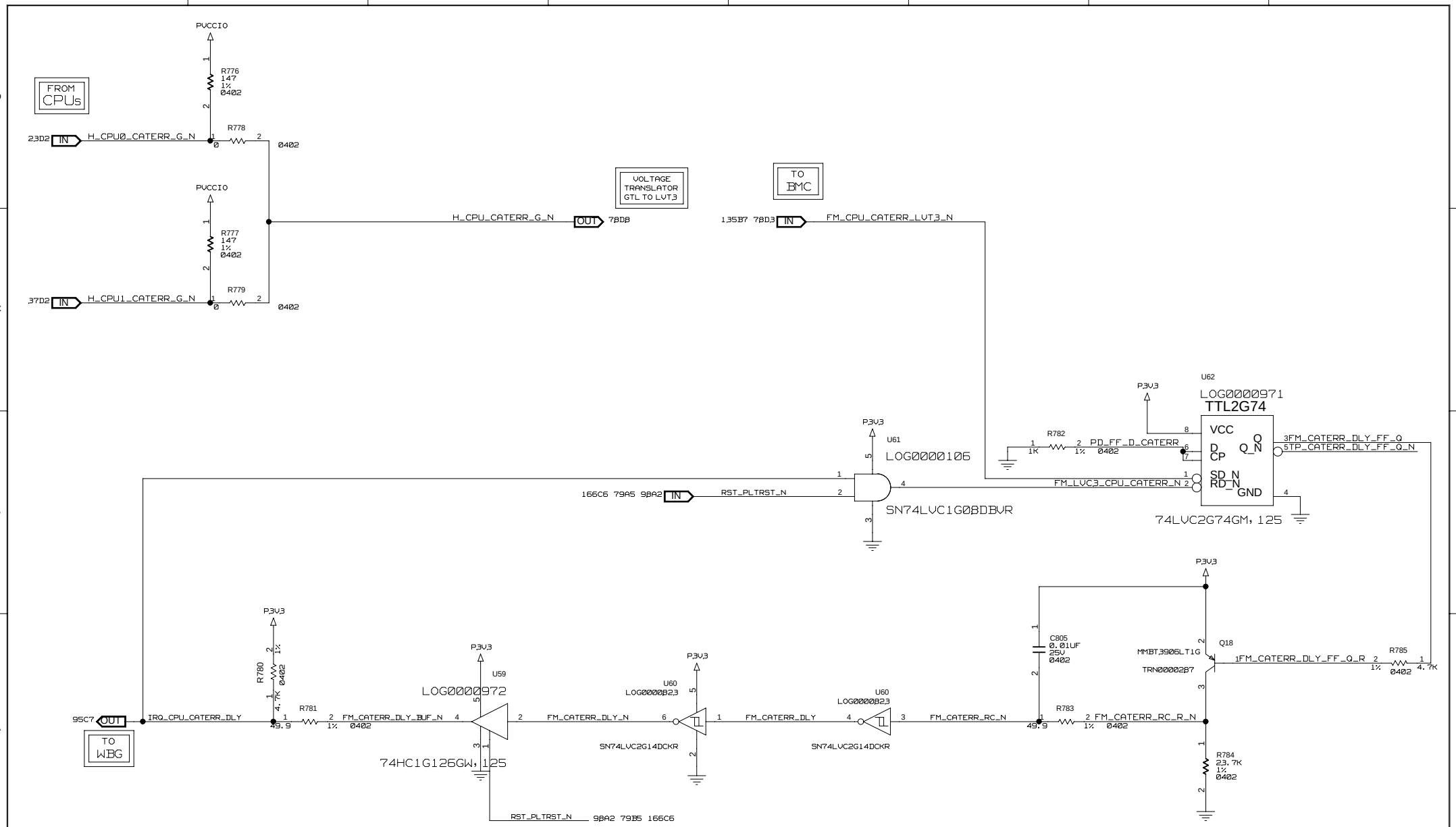
DATE: Wed Jul 30 14:58:42 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 78OF360



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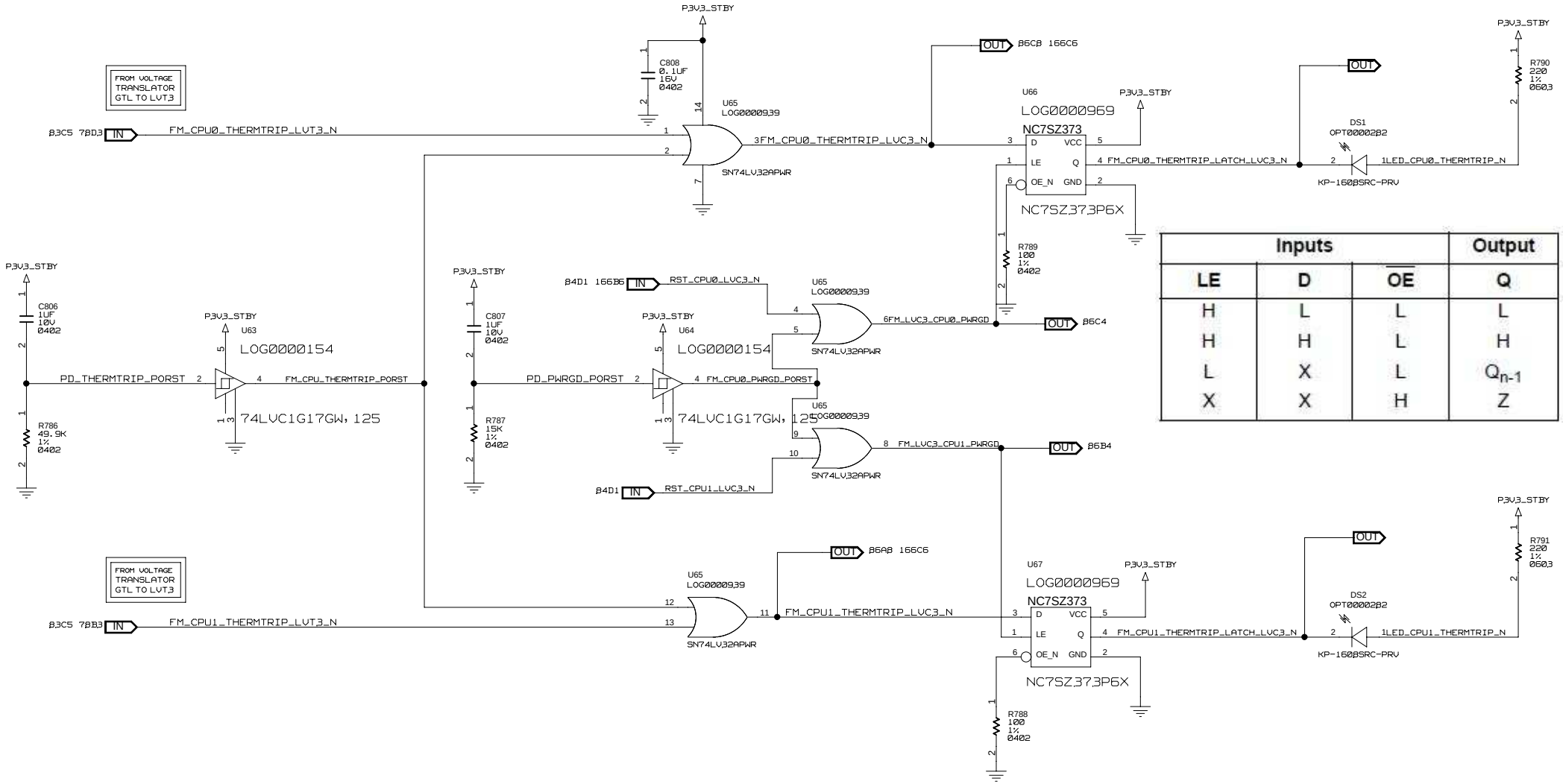
CPU SIDE BAND:CATASTROPHIC ERROR

wolfcreek_controller	DATE: Wed Jul 30 14:58:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 79OF360	



Inputs			Output
LE	D	$\overline{OE}$	Q
H	L	L	L
H	H	L	H
L	X	L	Q_{n-1}
X	X	H	Z

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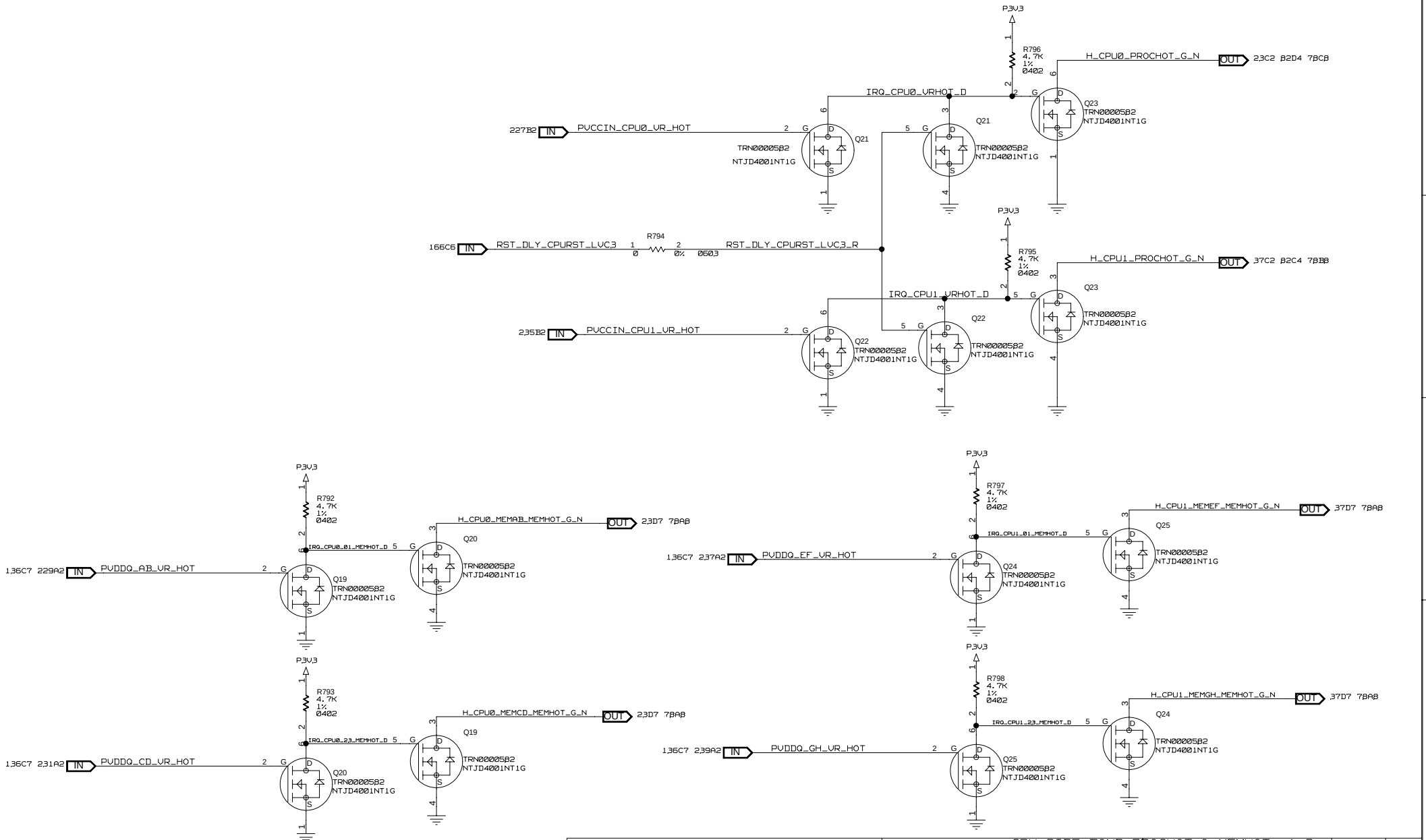
wolfcreek_controller	CPU SIDE BAND: THERMTRIP LATCHES	DWG NO: <DRAWING NO>	REV: <REVISION>
wolfcreek_controller.cpm	DATE: Wed Jul 30 14:57:35 2014	DRAWN BY: <ENGINEER>	SHEET: 80OF360



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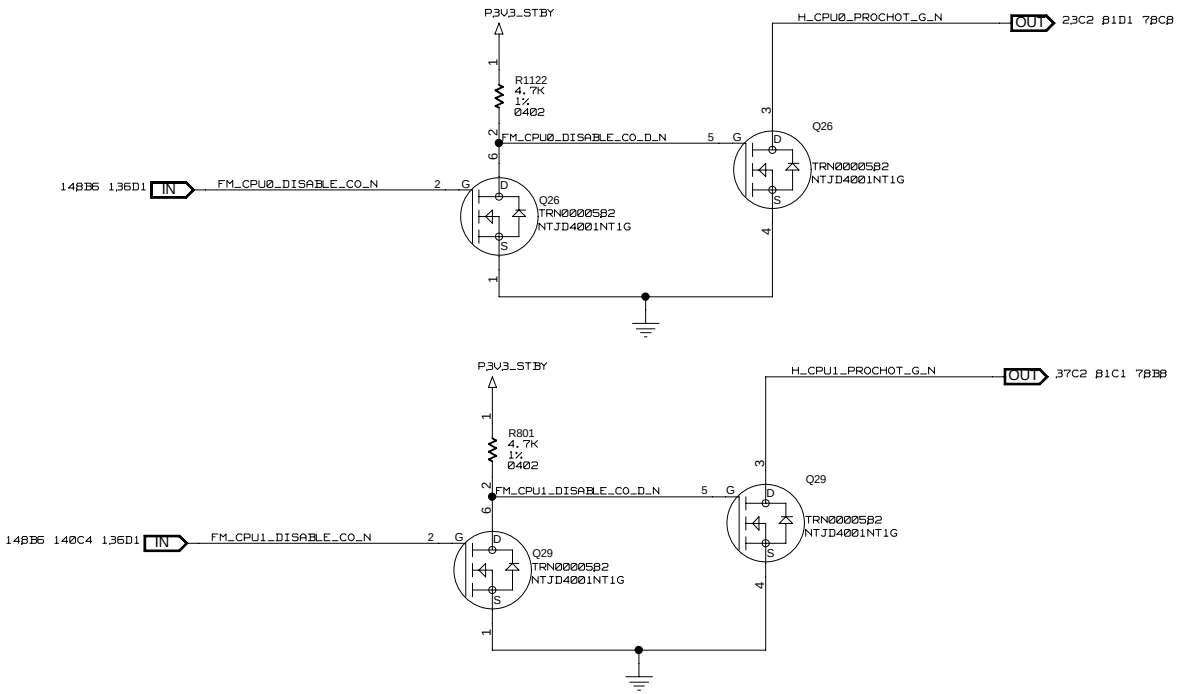
wolfcreek_controller	CPU SIDE BAND:PROCHOT & MEMHOT (1/2)	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DATE: Wed Jul 30 14:58:43 2014	DRAWN BY: <ENGINEER>	SHEET: B10F360



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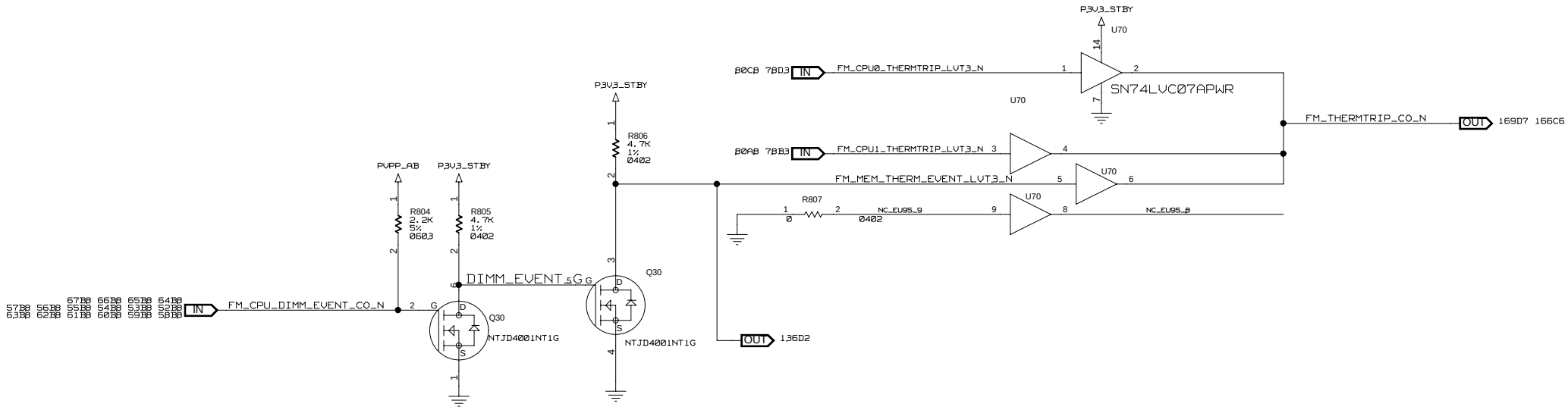
wolfcreek_controller	CPU SIDE BAND:PROCHOT & MEMHOT (2/2)	DWG NO: <DRAWING NO>	REV: <REVISION>
wolfcreek_controller.cpm	DATE: Fri Aug 08 12:05:31 2014	DRAWN BY: <ENGINEER>	SHEET: 82OF,360



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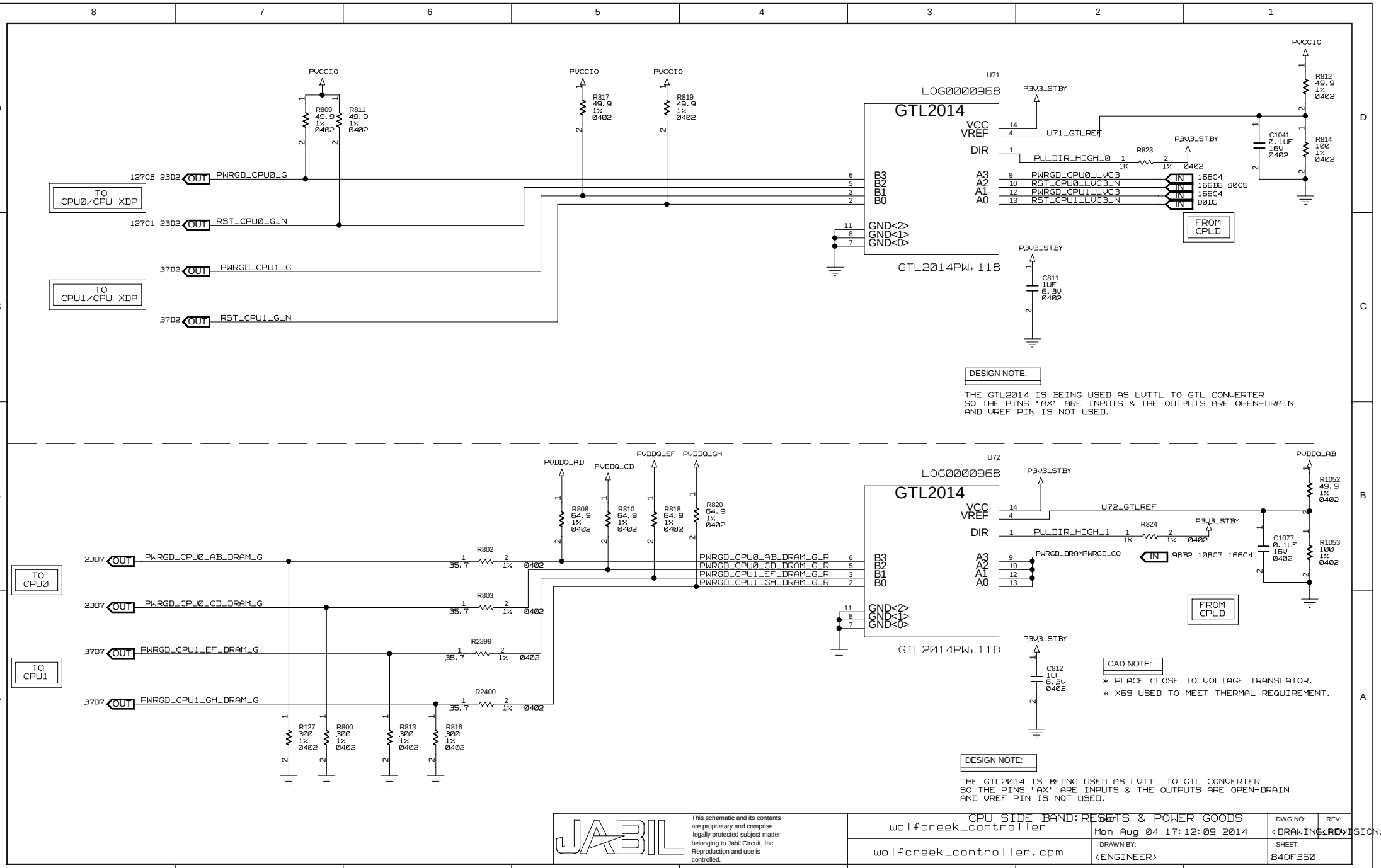
wolfcreek_controller	CPU SIDE BAND:DIMM EVENT CIRCUITRY	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DATE: Wed Jul 30 14:58:44 2014	SHEET: 030F360	
	DRAWN BY: <ENGINEER>		


PVCCIO
R809 49.9 1% 0402
R811 49.9 1% 0402
R817 49.9 1% 0402
R819 49.9 1% 0402
U71
LOG0000968
GTL2014
VCC
VREF
DIR
B3
B2
B1
B0
A3
A2
A1
A0
GND<2>
GND<1>
GND<0>
GTL2014PW,118
P3V3_STBY
U71_GTLREF
PU_DIR_HIGH_0
R823 1K 1% 0402
PWRGD_CPU0_LVC3
RST_CPU0_LVC3_N
PWRGD_CPU1_LVC3
RST_CPU1_LVC3_N
166C4
166B6 80C5
166C4
80B5
FROM CPLD
C1041 0.1UF 16V 0402
R812 49.9 1% 0402
R814 100 1% 0402
C811 1UF 6.3V 0402
127C8 23D2 OUT PWRGD_CPU0_G
127C1 23D2 OUT RST_CPU0_G_N
37D2 OUT PWRGD_CPU1_G
37D2 OUT RST_CPU1_G_N
TO CPU0/CPU XDP
TO CPU1/CPU XDP
DESIGN NOTE:
THE GTL2014 IS BEING USED AS LVTTL TO GTL CONVERTER
SO THE PINS 'AX' ARE INPUTS & THE OUTPUTS ARE OPEN-DRAIN
AND VREF PIN IS NOT USED.
PVDDQ_AB
PVDDQ_CD
PVDDQ_EF
PVDDQ_GH
R808 64.9 1% 0402
R810 64.9 1% 0402
R818 64.9 1% 0402
R820 64.9 1% 0402
U72
LOG0000968
GTL2014
U72_GTLREF
PU_DIR_HIGH_1
R824 1K 1% 0402
PWRGD_DRAMPWRGD_CO
9BB2 10BC7 166C4
FROM CPLD
R1052 49.9 1% 0402
R1053 100 1% 0402
C1077 0.1UF 16V 0402
GTL2014PW,118
C812 1UF 6.3V 0402
23D7 OUT PWRGD_CPU0_AB_DRAM_G
23D7 OUT PWRGD_CPU0_CD_DRAM_G
37D7 OUT PWRGD_CPU1_EF_DRAM_G
37D7 OUT PWRGD_CPU1_GH_DRAM_G
PWRGD_CPU0_AB_DRAM_G_R
PWRGD_CPU0_CD_DRAM_G_R
PWRGD_CPU1_EF_DRAM_G_R
PWRGD_CPU1_GH_DRAM_G_R
R802 35.7 1% 0402
R803 35.7 1% 0402
R2399 35.7 1% 0402
R2400 35.7 1% 0402
R127 300 1% 0402
R800 300 1% 0402
R813 300 1% 0402
R816 300 1% 0402
TO CPU0
TO CPU1
CAD NOTE:
* PLACE CLOSE TO VOLTAGE TRANSLATOR.
* X6S USED TO MEET THERMAL REQUIREMENT.
DESIGN NOTE:
THE GTL2014 IS BEING USED AS LVTTL TO GTL CONVERTER
SO THE PINS 'AX' ARE INPUTS & THE OUTPUTS ARE OPEN-DRAIN
AND VREF PIN IS NOT USED.
JABIL
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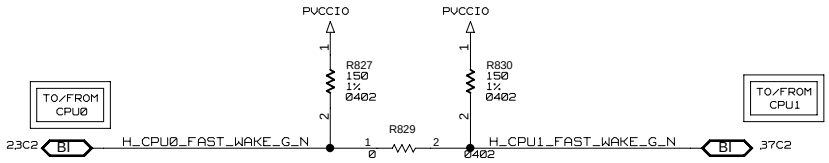
CPU SIDE BAND:RESETS & POWER GOODS
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Mon Aug 04 17:12:09 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: B4OF360

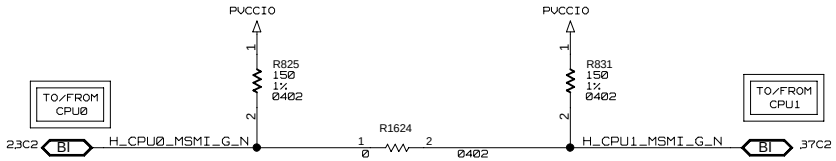
CAD NOTE:

* PLACE R827 NEAR CPU0.
* PLACE R830 NEAR CPU1.



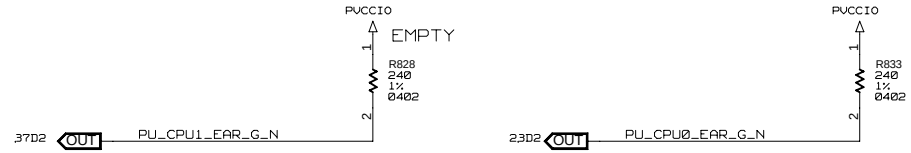
CAD NOTE:

* PLACE R825 NEAR CPU0.
* PLACE R831 NEAR CPU1.



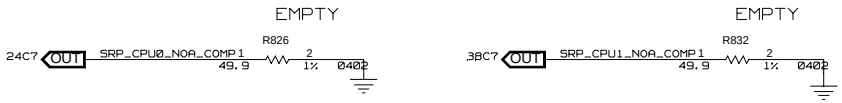
CAD NOTE:

PLACE NEAR TO RESPECTIVE CPU.



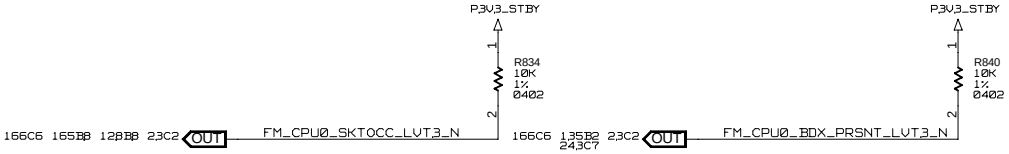
CAD NOTE:

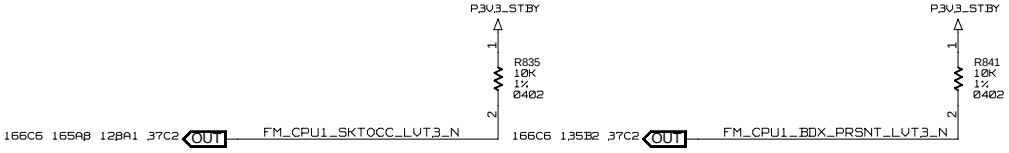
PLACE 500 MILS MAX FROM CPU0.



CAD NOTE:

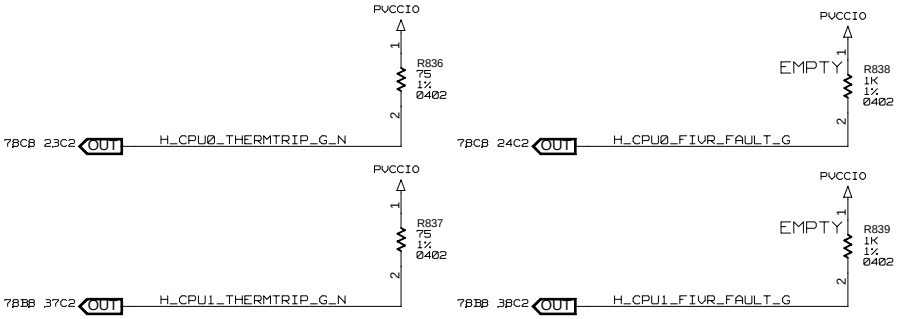
PACKAGE PINS PULL-UPS. PLACE NEAR TO CPU.





CAD NOTE:

PLACE NEAR GTL2014 VT.



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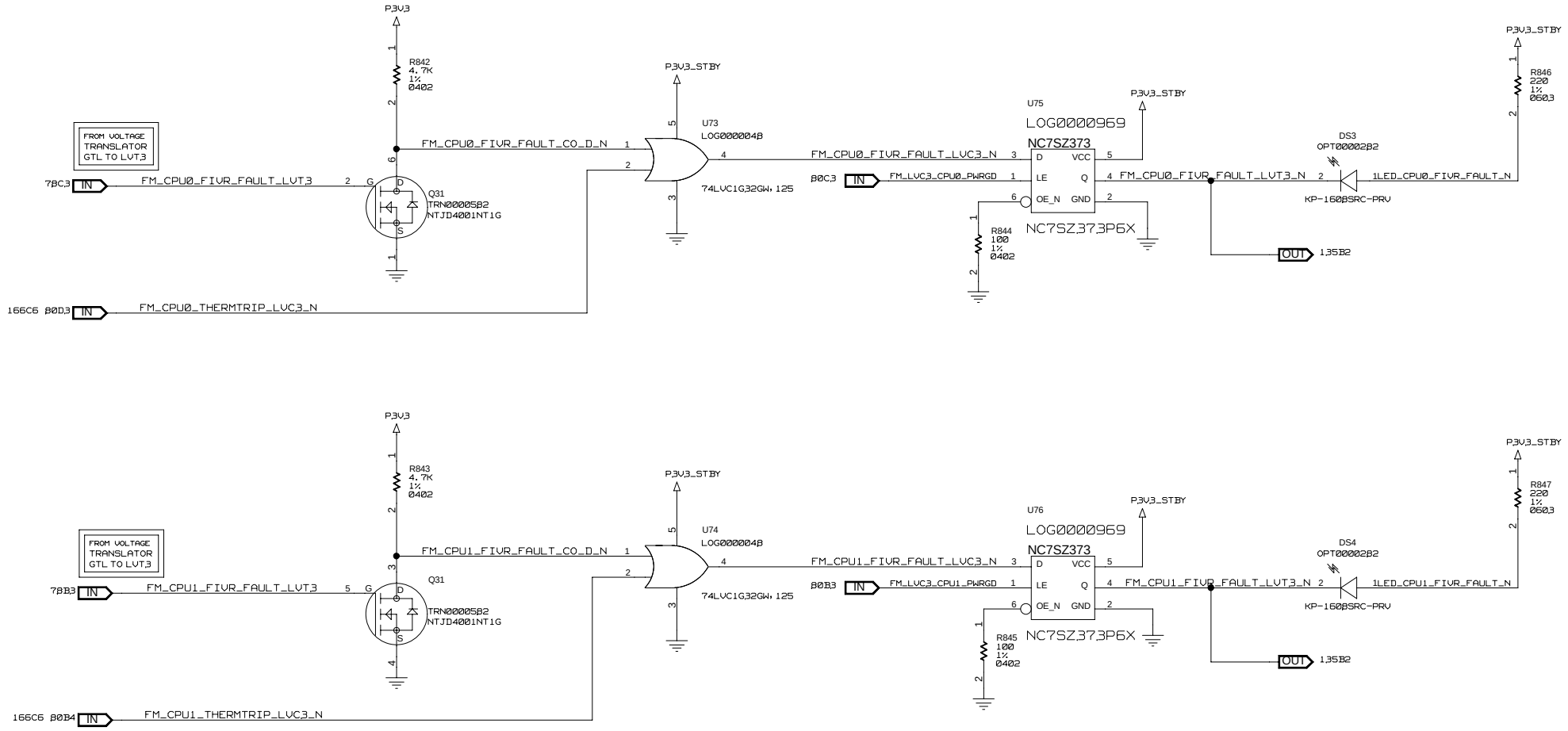
wolfcreek_controller	CPU SIDE BAND: PULL-UPS/PULL-DOWNS	DATE: Wed Jul 30 14:58:45 2014	DWG NO: <DRAWING> / REV: <REVISION>
wolfcreek_controller.cpm		DRAWN BY: <ENGINEER>	SHEET: 85OF360



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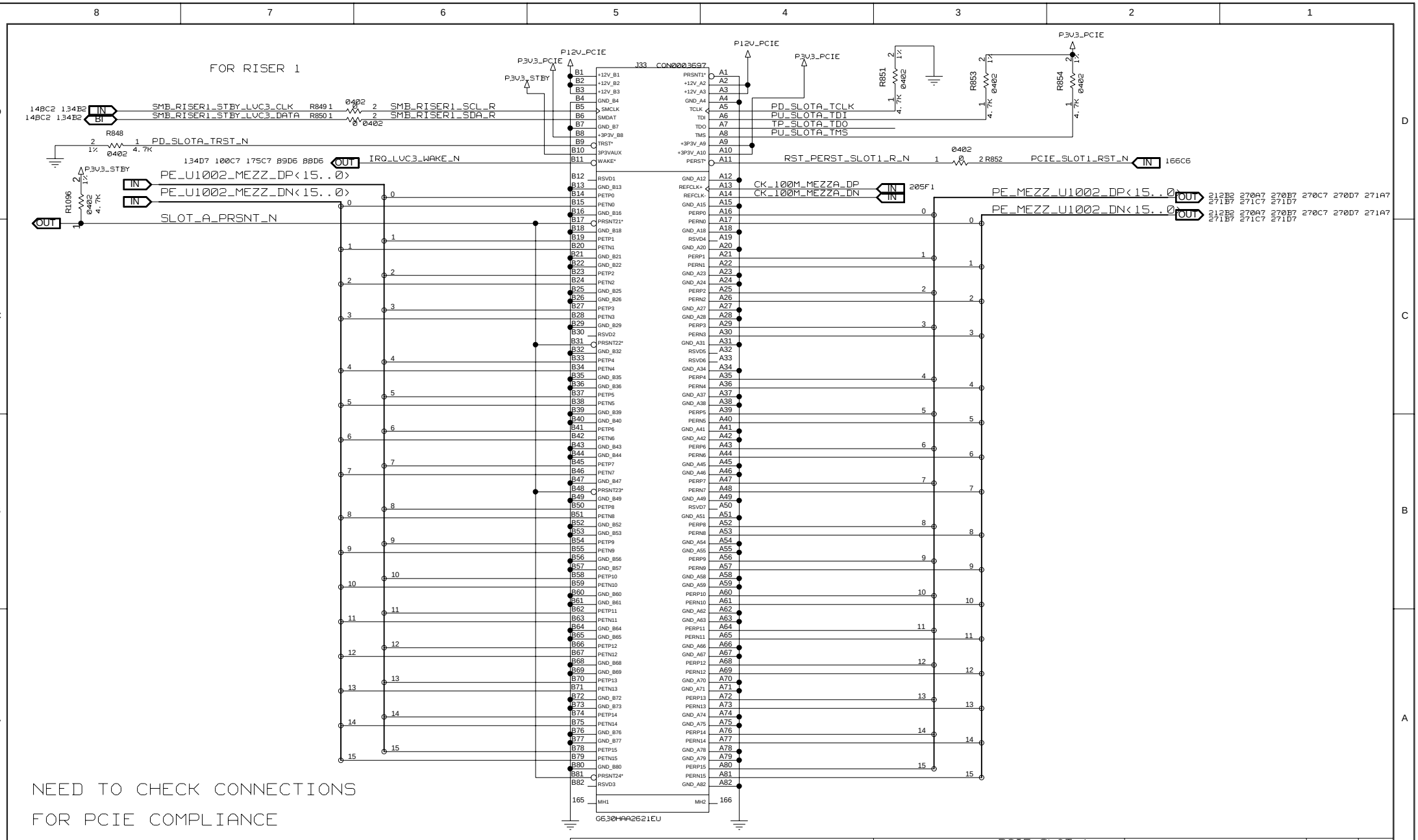
CPU SIDE BAND:FIVR FAULT

wolfcreek_controller	DATE: Wed Jul 30 14:58:47 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 86OF360	



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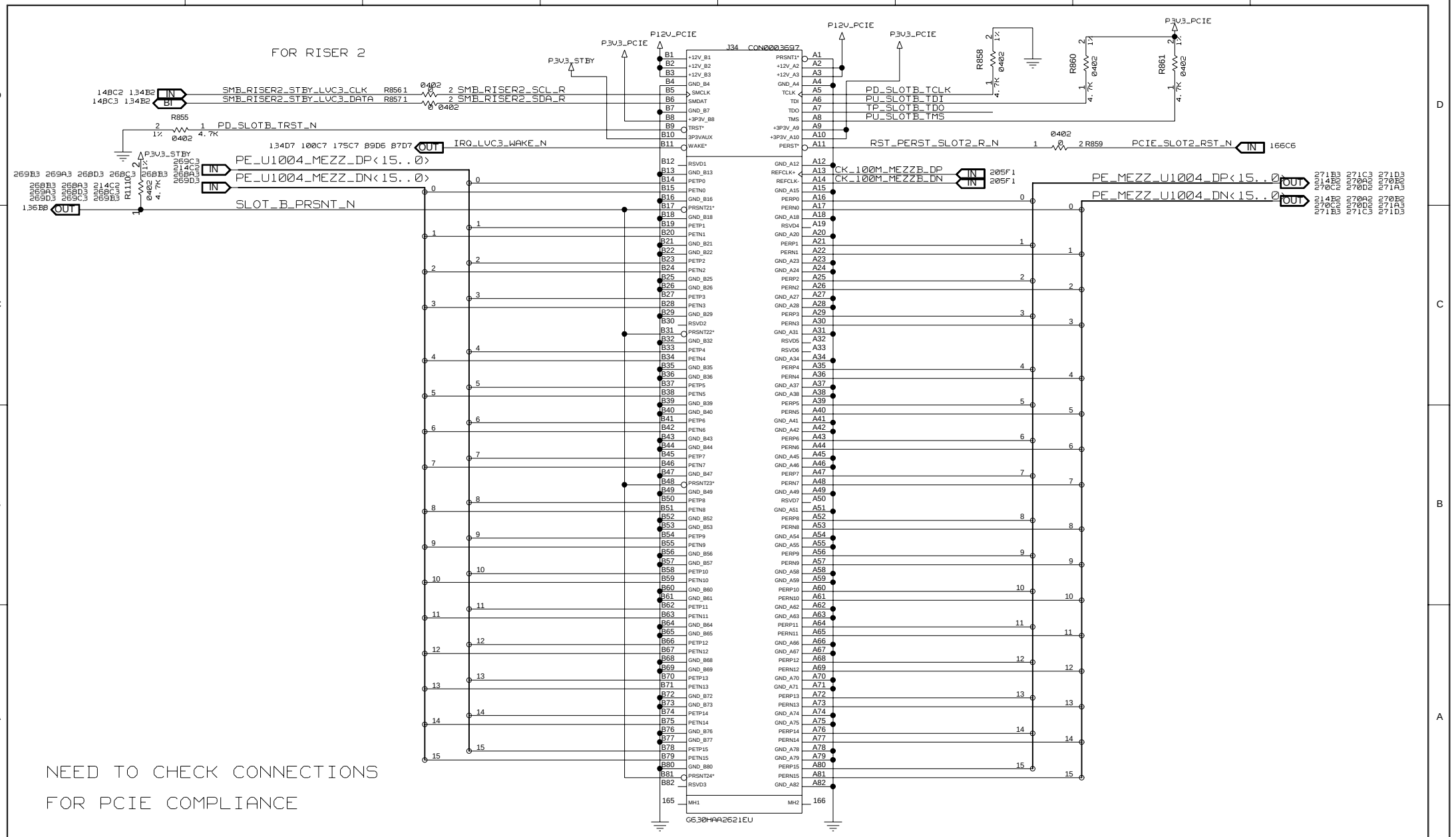
PCIE SLOT 1 wolfcreek_controller	DATE: Fri Aug 08 17:34:57 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 87OF360	



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PCIE SLOT 2
wolfcreek_controller

wolfcreek_controller.cpm

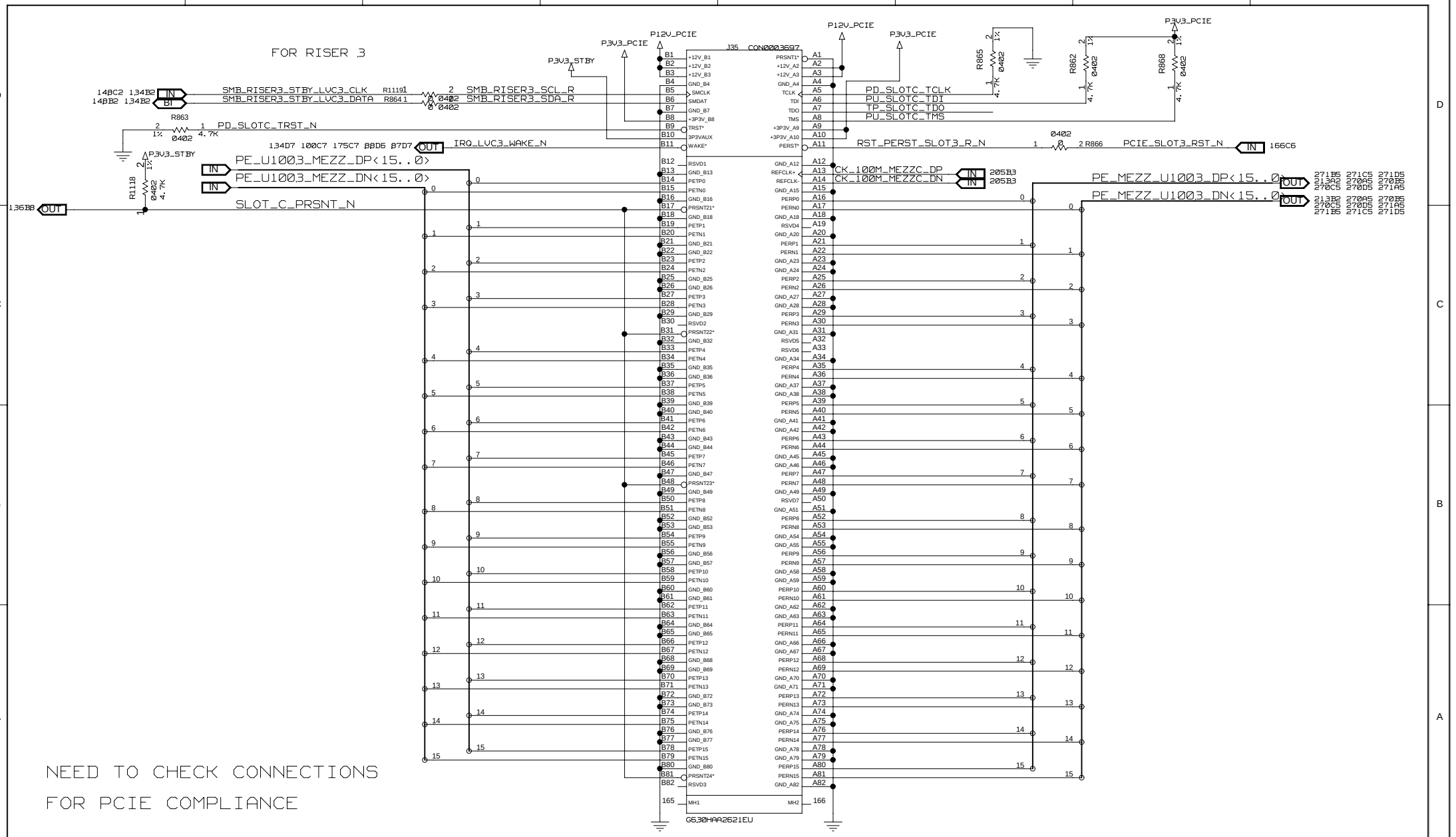
DATE: Fri Aug 08 17:35:14 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 88OF360



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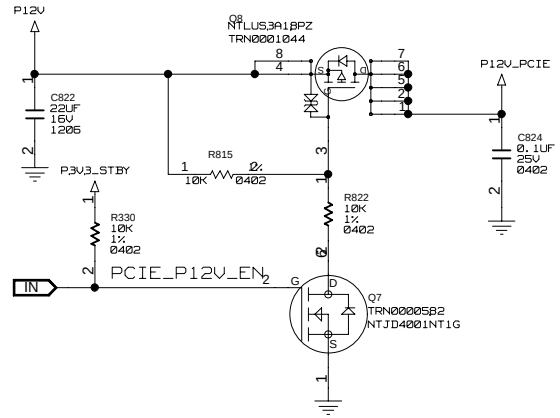
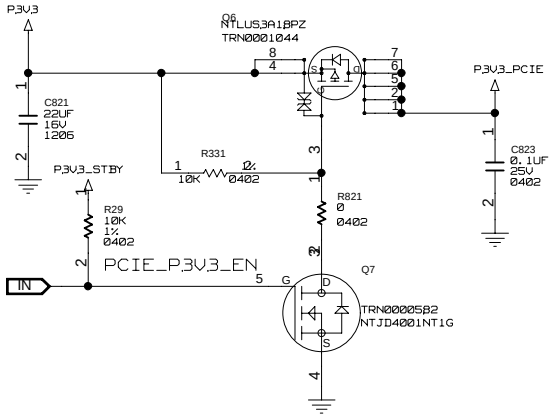
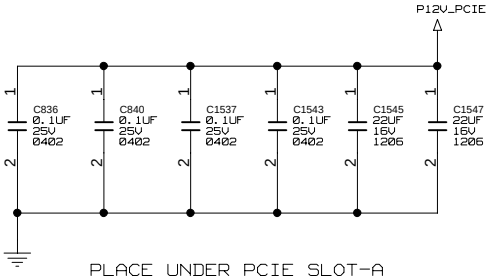
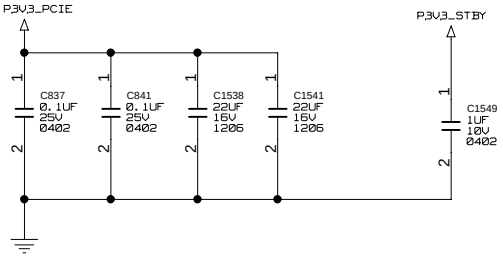
PCIE SLOT 3 wolfcreek_controller	DATE: Fri Aug 08 17:27:55 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 89OF360	

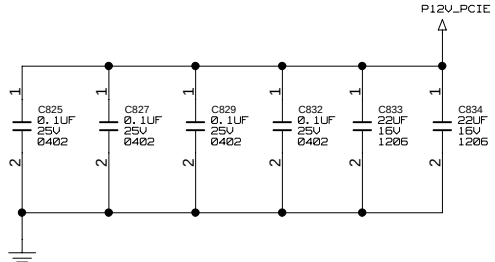




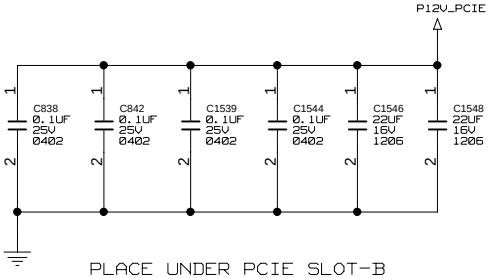


PLACE UNDER PCIE SLOT-A

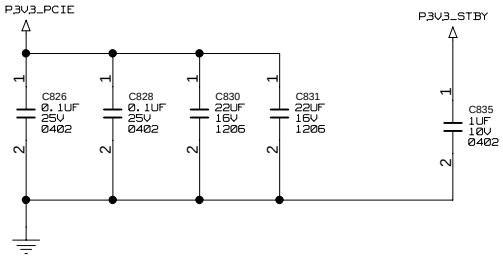


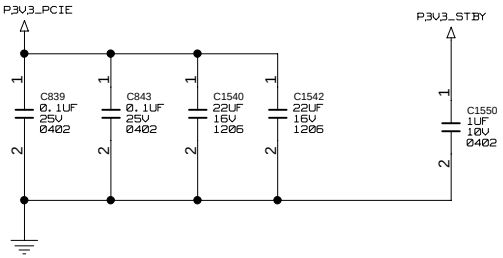


PLACE UNDER PCIE SLOT-C



PLACE UNDER PCIE SLOT-B





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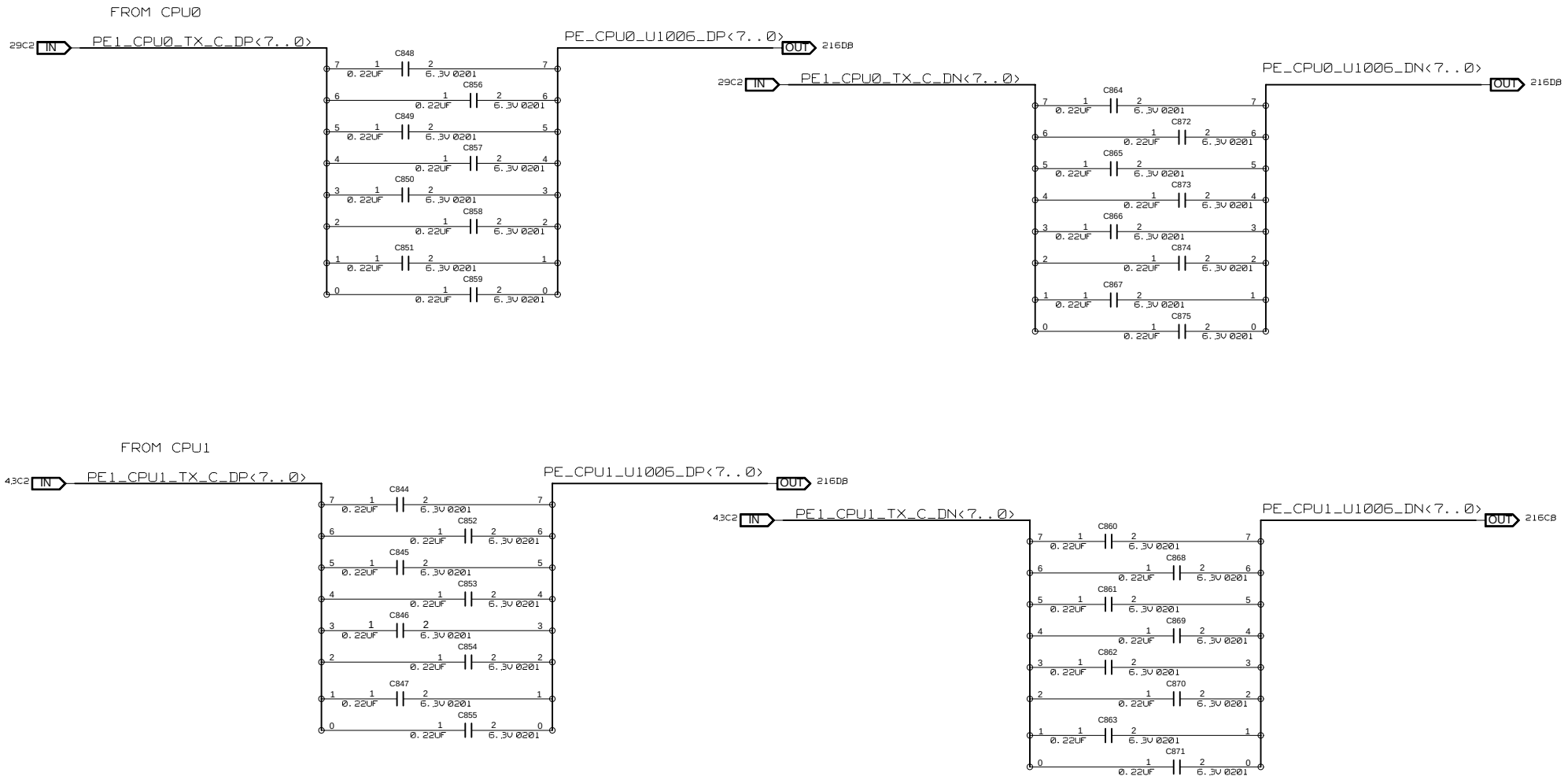
PCIE SLOT POWER wolfcreek_controller	DATE: Wed Jul 30 14:58:02 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 90OF360	



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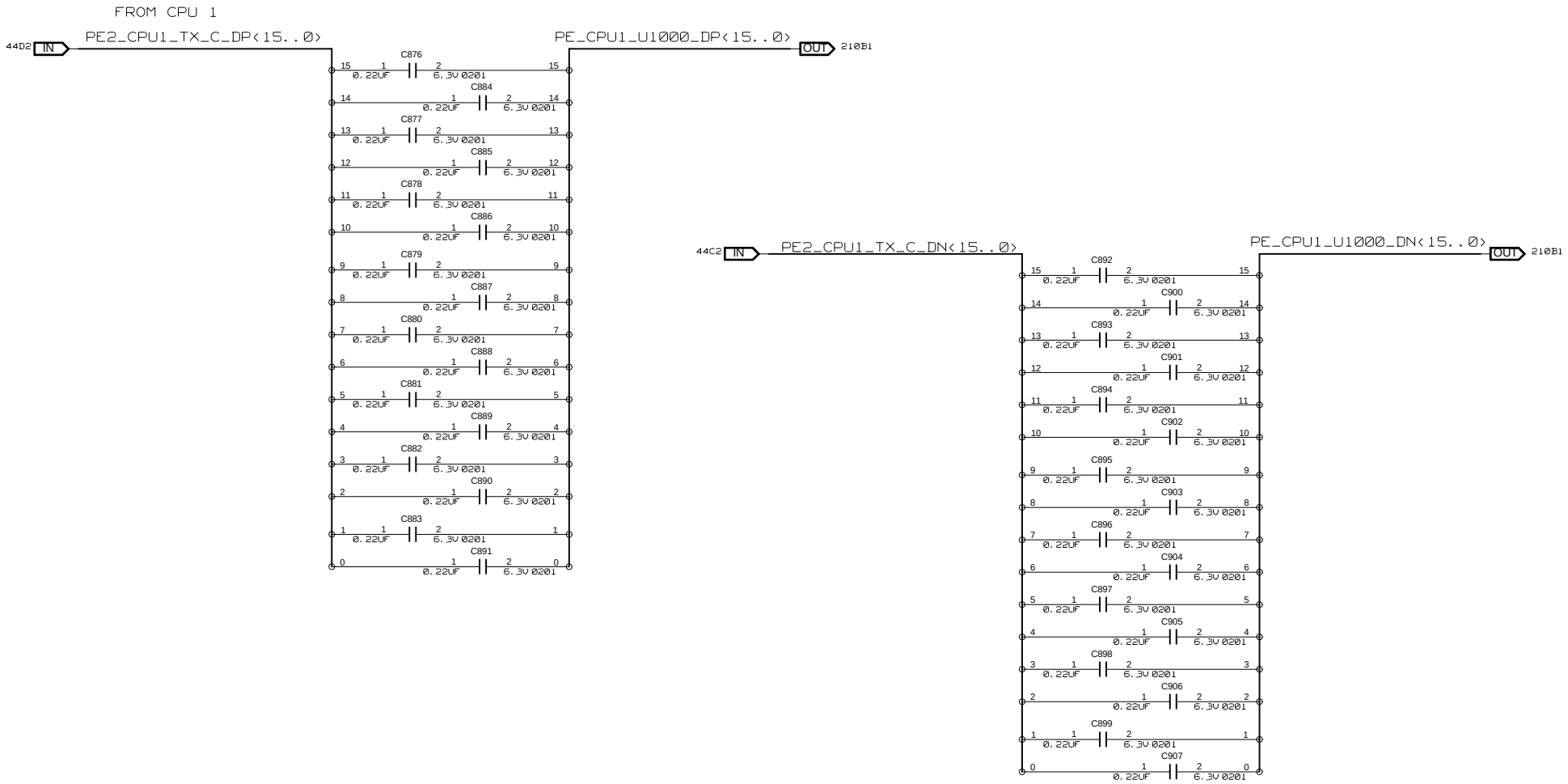
PCIE AC CAPS (1 OF 3) wolfcreek_controller	DATE: Wed Jul 30 14:58:49 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 91OF360	



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PCIE AC CAPS (2 OF 3)	DATE: Wed Jul 30 14:58:49 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 92OF360	

FROM CPU 1

45C2 IN PE3_CPU1_TX_C_DP<15..0>

PE_CPU1_U1001_DP<15..0> OUT 211B1

Pin	Net	Cap	Value	Pin
15	1	C908	0.22UF 6.3V 0201	2	15
14	1	C916	0.22UF 6.3V 0201	2	14
13	1	C909	0.22UF 6.3V 0201	2	13
12	1	C917	0.22UF 6.3V 0201	2	12
11	1	C910	0.22UF 6.3V 0201	2	11
10	1	C918	0.22UF 6.3V 0201	2	10
9	1	C911	0.22UF 6.3V 0201	2	9
8	1	C919	0.22UF 6.3V 0201	2	8
7	1	C912	0.22UF 6.3V 0201	2	7
6	1	C920	0.22UF 6.3V 0201	2	6
5	1	C913	0.22UF 6.3V 0201	2	5
4	1	C921	0.22UF 6.3V 0201	2	4
3	1	C914	0.22UF 6.3V 0201	2	3
2	1	C922	0.22UF 6.3V 0201	2	2
1	1	C915	0.22UF 6.3V 0201	2	1
0	1	C923	0.22UF 6.3V 0201	2	0

45C2 IN PE3_CPU1_TX_C_DN<15..0>

PE_CPU1_U1001_DN<15..0> OUT 211C1

Pin	Net	Cap	Value	Pin
15	1	C924	0.22UF 6.3V 0201	2	15
14	1	C932	0.22UF 6.3V 0201	2	14
13	1	C925	0.22UF 6.3V 0201	2	13
12	1	C933	0.22UF 6.3V 0201	2	12
11	1	C926	0.22UF 6.3V 0201	2	11
10	1	C934	0.22UF 6.3V 0201	2	10
9	1	C927	0.22UF 6.3V 0201	2	9
8	1	C935	0.22UF 6.3V 0201	2	8
7	1	C928	0.22UF 6.3V 0201	2	7
6	1	C936	0.22UF 6.3V 0201	2	6
5	1	C929	0.22UF 6.3V 0201	2	5
4	1	C937	0.22UF 6.3V 0201	2	4
3	1	C930	0.22UF 6.3V 0201	2	3
2	1	C938	0.22UF 6.3V 0201	2	2
1	1	C931	0.22UF 6.3V 0201	2	1
0	1	C939	0.22UF 6.3V 0201	2	0

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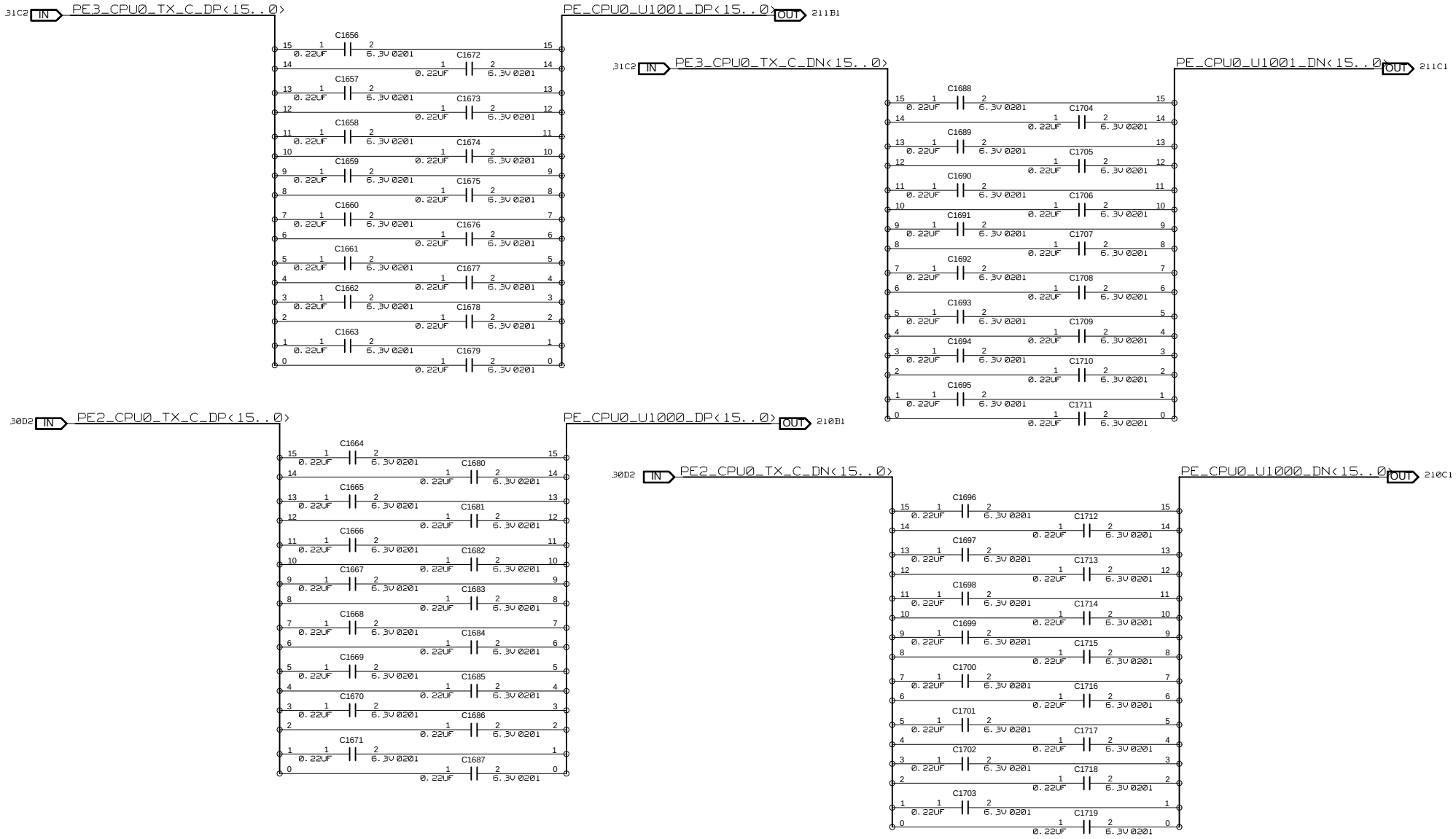
PCIE AC CAPS (3 OF 3)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:50 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 93OF360



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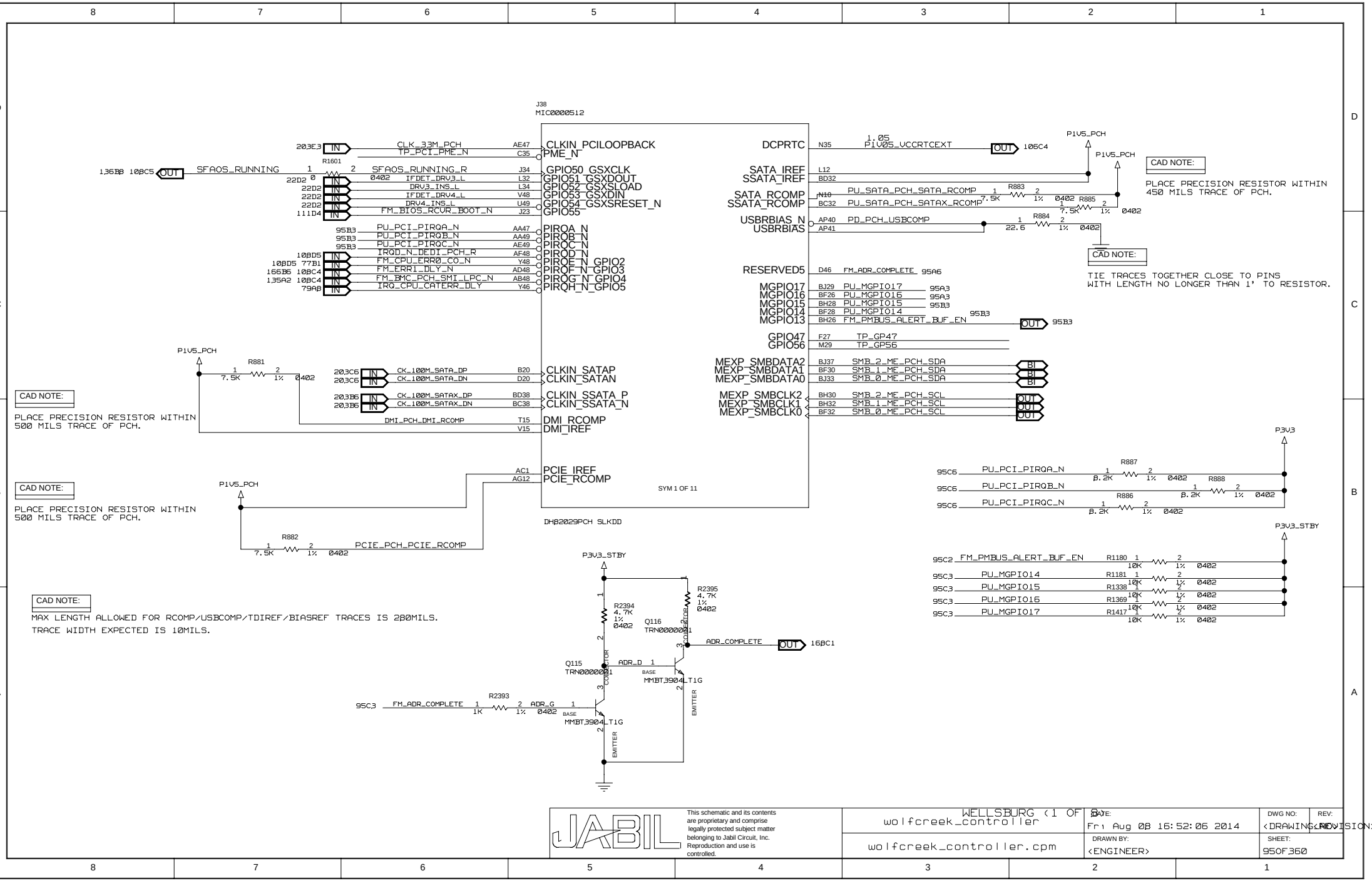
PCIE MP AC COUPLING wolfcreek_controller	DATE: Wed Jul 30 14:59:22 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 94OF360	



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WELLSBURG (1 OF 2) wolfcreek_controller	DATE: Fri Aug 08 16:52:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 95OF360	

NEED TO CHECK THIS BIFURCATION IS OK

PORTS 5-6 AND 7-8 CONFIGURED AS X2 PCIE

J38
MIC0000512

157D5	IN	DMI_CPU0_PCH_TX_C_DP<3>	L6	DMI_RXP3	DMI_TXP3	F4	DMI_CPU0_PCH_RX_DP<3>
157D1	IN	DMI_CPU0_PCH_TX_C_DN<3>	J6	DMI_RXN3	DMI_TXN3	E2	DMI_CPU0_PCH_RX_DN<3>
157D5	IN	DMI_CPU0_PCH_TX_C_DP<2>	N6	DMI_RXP2	DMI_TXP2	H4	DMI_CPU0_PCH_RX_DP<2>
157D1	IN	DMI_CPU0_PCH_TX_C_DN<2>	N7	DMI_RXN2	DMI_TXN2	H2	DMI_CPU0_PCH_RX_DN<2>
157D5	IN	DMI_CPU0_PCH_TX_C_DP<1>	T9	DMI_RXP1	DMI_TXP1	K4	DMI_CPU0_PCH_RX_DP<1>
157D1	IN	DMI_CPU0_PCH_TX_C_DN<1>	T7	DMI_RXN1	DMI_TXN1	K2	DMI_CPU0_PCH_RX_DN<1>
157D5	IN	DMI_CPU0_PCH_TX_C_DP<0>	T14	DMI_RXP0	DMI_TXP0	M4	DMI_CPU0_PCH_RX_DP<0>
157D1	IN	DMI_CPU0_PCH_TX_C_DN<0>	T12	DMI_RXN0	DMI_TXN0	M2	DMI_CPU0_PCH_RX_DN<0>
		CLKIN_DMIP	V10	RESERVED3	CLKOUT_DMIP0	BD4	TP_CLK_100M_PCH_DMIP
		CLKIN_DMIN	V12	RESERVED2	CLKOUT_DMIN0	BE2	TP_CLK_100M_PCH_DMIN
22A3	IN	PE_PCH_RX8_C_DP	AU12	PERP_8	PETP_8	AV4	PE_PCH_TX8_C_DP
22A3	IN	PE_PCH_RX8_C_DN	AU10	PERN_8	PETN_8	AV2	PE_PCH_TX8_C_DN
22B3	IN	PE_PCH_RX7_C_DP	AU7	PERP_7	PETP_7	AT2	PE_PCH_TX7_C_DP
22A3	IN	PE_PCH_RX7_C_DN	AU6	PERN_7	PETN_7	AT4	PE_PCH_TX7_C_DN
22C3	IN	PE_PCH_RX6_C_DP	AP7	PERP_6	PETP_6	AP2	PE_PCH_TX6_C_DP
22C3	IN	PE_PCH_RX6_C_DN	AP9	PERN_6	PETN_6	AP4	PE_PCH_TX6_C_DN
22D3	IN	PE_PCH_RX5_C_DP	AP12	PERP_5	PETP_5	AM2	PE_PCH_TX5_C_DN
22C3	IN	PE_PCH_RX5_C_DN	AP14	PERN_5	PETN_5	AM4	PE_PCH_TX5_C_DN
134D1	IN	PE_PCH_BMC_RX_DP	AM6	PERP_4	PETP_4	AK2	PE_PCH_BMC_TX_C_DP
134D1	IN	PE_PCH_BMC_RX_DN	AM7	PERN_4	PETN_4	AK4	PE_PCH_BMC_TX_C_DN
175C2	IN	P2E_WBG_NIC1_RX_DP<1>	AM10	PERP_3	PETP_3	AH2	P2E_WBG_NIC1_TX_C_DP<1>
175C2	IN	P2E_WBG_NIC1_RX_DN<1>	AM12	PERN_3	PETN_3	AH4	P2E_WBG_NIC1_TX_C_DN<1>
175C2	IN	P2E_WBG_NIC1_RX_DP<0>	AG15	PERP_2_USB3RP_4	PETP_2_USB3TP_4	AF2	P2E_WBG_NIC1_TX_C_DP<0>
175C2	IN	P2E_WBG_NIC1_RX_DN<0>	AG14	PERN_2_USB3RN_4	PETN_2_USB3TN_4	AF4	P2E_WBG_NIC1_TX_C_DN<0>
219C2	IN	PE_PCH_SW_RX_C_DP	AG7	PERP_1_USB3RP_3	PETP_1_USB3TP_3	AD4	PE_PCH_SW_TX_C_DP
219C2	IN	PE_PCH_SW_RX_C_DN	AG6	PERN_1_USB3RN_3	PETN_1_USB3TN_3	AD2	PE_PCH_SW_TX_C_DN
		USB3_05_RXP	AC9	USB3RP6	USB3TP6	AB4	USB3_05_TXP
		USB3_05_RXN	AC7	USB3RN6	USB3TN6	AB2	USB3_05_TXN
		USB3_04_RXP	AC12	USB3RP5	USB3TP5	Y4	USB3_04_TXP
		USB3_04_RXN	AC14	USB3RN5	USB3TN5	Y2	USB3_04_TXN
117B8	IN	USB3_01_RXP	AA15	USB3RP2	USB3TP2	V4	USB3_01_TXP
117B8	IN	USB3_01_RXN	AA14	USB3RN2	USB3TN2	V2	USB3_01_TXN
117D8	IN	USB3_00_RXP	AA6	USB3RP1	USB3TP1	T4	USB3_00_TXP
117C8	IN	USB3_00_RXN	AA7	USB3RN1	USB3TN1	T2	USB3_00_TXN
16BC1 10BC7	OUT	PBG_CPLD_CNTL0	J44	OC7_N_GPIO14	USB2P13	AC38	USB2_13_DP
136B2	IN	P12V_GD_CPLD_OUT	L43	OC6_N_GPIO10	USB2N13	AC36	USB2_13_DN
130B8	IN	FM_SMI_INT_CPLD_R_N	G43	OC5_N_GPIO9	USB2P12	AC43	USB2_12_DP
130C8	BI	NOA_4_R_FM_USB_OC_4_N	G44	OC4_N_GPIO43	USB2N12	AC44	USB2_12_DN
256D2 256A5	OUT	FORCE_STBY_ON	B42	OC3_N_GPIO42	USB2P11	AC41	USB2_11_DP
130C8	BI	NOA_2_R_FM_USB_OC_2_N	A37	OC2_N_GPIO41	USB2N11	AC40	USB2_11_DN
130D8	BI	NOA_1_R_FM_USB_OC_1_N	B38	OC1_N_GPIO40	USB2P10	AG35	USB2_10_DP
130D8	BI	NOA_0_R_FM_USB_OC_0_N	J43	OC0_N_GPIO59	USB2N10	AG36	USB2_10_DN
					USB2P9	AG41	USB2_09_DP
					USB2N9	AG40	USB2_09_DN
					USB2P8	AG44	USB2_08_DP
					USB2N8	AG43	USB2_08_DN
					USB2P7	AM43	USB2_07_DP
					USB2N7	AM44	USB2_07_DN
					USB2P6	AJ43	USB2_06_DP
					USB2N6	AJ44	USB2_06_DN
					USB2P5	AJ41	USB2_05_DP
					USB2N5	AJ40	USB2_05_DN
					USB2P4	AM40	USB2_04_DP
					USB2N4	AM41	USB2_04_DN
					USB2P3	AP43	USB2_03_DP
					USB2N3	AP44	USB2_03_DN
					USB2P2	AJ35	USB2_02_DP
					USB2N2	AJ36	USB2_02_DN
					USB2P1	AY46	USB2_01_DP
					USB2N1	AY48	USB2_01_DN
					USB2P0	AV46	USB2_00_DP
					USB2N0	AV48	USB2_00_DN
					CLKIN_DOT96P	AM36	CLK_96M_PCH_DP
					CLKIN_DOT96N	AM35	CLK_96M_PCH_DN

SYM 2 OF 11

DHB2029PCH SLKDD

DMI_CPU0_PCH_RX_DP<3>	OUT	157C8	
DMI_CPU0_PCH_RX_DN<3>	OUT	157C4	
DMI_CPU0_PCH_RX_DP<2>	OUT	157C8	
DMI_CPU0_PCH_RX_DN<2>	OUT	157C4	
DMI_CPU0_PCH_RX_DP<1>	OUT	157C8	
DMI_CPU0_PCH_RX_DN<1>	OUT	157C4	
DMI_CPU0_PCH_RX_DP<0>	OUT	157C8	
DMI_CPU0_PCH_RX_DN<0>	OUT	157C4	
PE_PCH_TX8_C_DP	OUT	114C8	
PE_PCH_TX8_C_DN	OUT	114C8	
PE_PCH_TX7_C_DP	OUT	114C8	
PE_PCH_TX7_C_DN	OUT	114C8	
PE_PCH_TX6_C_DP	OUT	114C8	
PE_PCH_TX6_C_DN	OUT	114B8	
PE_PCH_TX5_C_DN	OUT	96C2 114B8	
PE_PCH_TX5_C_DN	OUT	96C2 114B8	
PE_PCH_BMC_TX_C_DP	OUT	114B8	
PE_PCH_BMC_TX_C_DN	OUT	114B8	
P2E_WBG_NIC1_TX_C_DP<1>	OUT	114D8	
P2E_WBG_NIC1_TX_C_DN<1>	OUT	114C8	
P2E_WBG_NIC1_TX_C_DP<0>	OUT	114C8	
P2E_WBG_NIC1_TX_C_DN<0>	OUT	114C8	
PE_PCH_SW_TX_C_DP	OUT	114B8	
PE_PCH_SW_TX_C_DN	OUT	114B8	
USB3_05_TXP			
USB3_05_TXN			
USB3_04_TXP			
USB3_04_TXN			
USB3_01_TXP	OUT	117C8	
USB3_01_TXN	OUT	117C8	
USB3_00_TXP	OUT	117D8	
USB3_00_TXN	OUT	117D8	
USB2_13_DP			
USB2_13_DN			
USB2_12_DP			
USB2_12_DN			
USB2_11_DP			
USB2_11_DN			
USB2_10_DP			
USB2_10_DN			
USB2_09_DP			
USB2_09_DN			
USB2_08_DP			
USB2_08_DN			
USB2_07_DP	BI	117C4	
USB2_07_DN	BI	117B4	
USB2_06_DP			
USB2_06_DN			
USB2_05_DP			
USB2_05_DN			
USB2_04_DP			
USB2_04_DN			
USB2_03_DP			
USB2_03_DN			
USB2_02_DP			
USB2_02_DN			
USB2_01_DP	BI	117C3	
USB2_01_DN	BI	117C3	
USB2_00_DP	BI	119D5	TO BMC
USB2_00_DN	BI	119D5	
CLK_96M_PCH_DP	IN	203C6	
CLK_96M_PCH_DN	IN	203C6	

R889 10K 1% 0402
R890 10K 1% 0402

R1312 10K 1% 0402	BPM_RESERVE5	OUT	98D2 197D7
R1313 10K 1% 0402	BPM_RESERVE6	OUT	98C2 196A2
R1314 10K 1% 0402	BPM_RESERVE7	OUT	98C2 196B2
R1315 10K 1% 0402	BPM_RESERVE8	OUT	98C2 196C2

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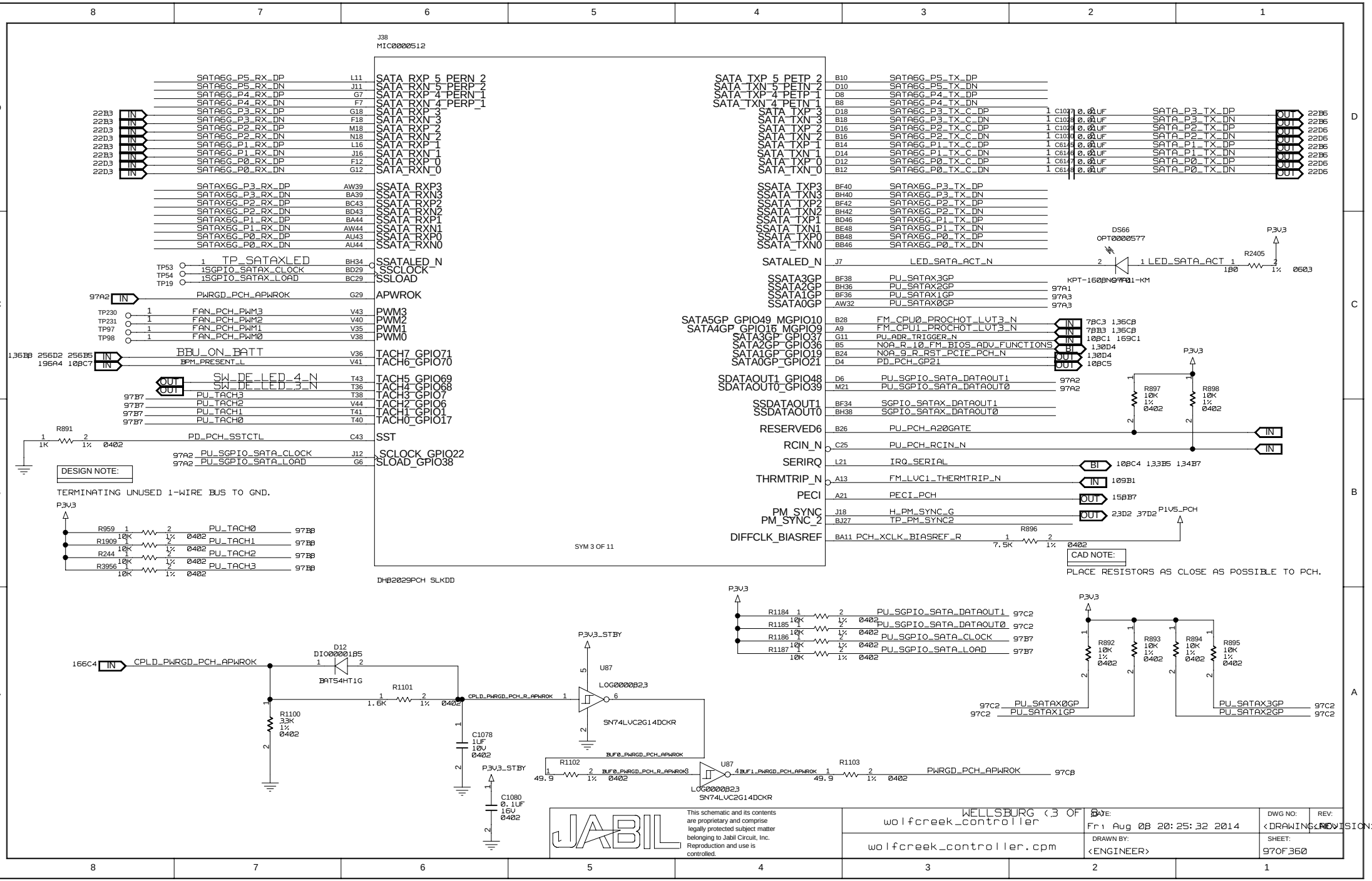
WELLSBURG (2 OF 2) wolfcreek_controller	DATE: Fri Aug 08 20:52:20 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 96OF360	


J38
MIC0000512
SATA6G_P5_RX_DP L11 SATA_RXP_5_PERN_2
SATA6G_P5_RX_DN J11 SATA_RXN_5_PERP_2
SATA6G_P4_RX_DP G7 SATA_RXP_4_PERN_1
SATA6G_P4_RX_DN F7 SATA_RXN_4_PERP_1
SATA6G_P3_RX_DP G18 SATA_RXP_3
SATA6G_P3_RX_DN F18 SATA_RXN_3
SATA6G_P2_RX_DP M18 SATA_RXP_2
SATA6G_P2_RX_DN N18 SATA_RXN_2
SATA6G_P1_RX_DP L16 SATA_RXP_1
SATA6G_P1_RX_DN J16 SATA_RXN_1
SATA6G_P0_RX_DP F12 SATA_RXP_0
SATA6G_P0_RX_DN G12 SATA_RXN_0
SATAX6G_P3_RX_DP AW39 SSATA_RXP3
SATAX6G_P3_RX_DN BA39 SSATA_RXN3
SATAX6G_P2_RX_DP BC43 SSATA_RXP2
SATAX6G_P2_RX_DN BD43 SSATA_RXN2
SATAX6G_P1_RX_DP BA44 SSATA_RXP1
SATAX6G_P1_RX_DN AW44 SSATA_RXN1
SATAX6G_P0_RX_DP AU43 SSATA_RXP0
SATAX6G_P0_RX_DN AU44 SSATA_RXN0
TP_SATAXLED BH34 SSATALED_N
SGPIO_SATAX_CLOCK BD29 SSCLOCK
SGPIO_SATAX_LOAD BC29 SSLOAD
PWRGD_PCH_APWROK G29 APWROK
FAN_PCH_PWM3 V43 PWM3
FAN_PCH_PWM2 V40 PWM2
FAN_PCH_PWM1 V35 PWM1
FAN_PCH_PWM0 V38 PWM0
BBU_ON_BATT V36 TACH7_GPIO71
BPM_PRESENT_L V41 TACH6_GPIO70
SW_DF_LED_4_N T43 TACH5_GPIO69
SW_DF_LED_3_N T36 TACH4_GPIO68
PU_TACH3 T38 TACH3_GPIO7
PU_TACH2 V44 TACH2_GPIO6
PU_TACH1 T41 TACH1_GPIO1
PU_TACH0 T40 TACH0_GPIO17
PD_PCH_SSTCTL C43 SST
PU_SGPIO_SATA_CLOCK J12 SCLOCK_GPIO22
PU_SGPIO_SATA_LOAD G6 SLOAD_GPIO38
SATA_TXP_5_PETP_2 B10 SATA6G_P5_TX_DP
SATA_TXN_5_PETN_2 D10 SATA6G_P5_TX_DN
SATA_TXP_4_PETP_1 D8 SATA6G_P4_TX_DP
SATA_TXN_4_PETN_1 B8 SATA6G_P4_TX_DN
SATA_TXP_3 D18 SATA6G_P3_TX_C_DP
SATA_TXN_3 B18 SATA6G_P3_TX_C_DN
SATA_TXP_2 D16 SATA6G_P2_TX_C_DP
SATA_TXN_2 B16 SATA6G_P2_TX_C_DN
SATA_TXP_1 B14 SATA6G_P1_TX_C_DP
SATA_TXN_1 D14 SATA6G_P1_TX_C_DN
SATA_TXP_0 D12 SATA6G_P0_TX_C_DP
SATA_TXN_0 B12 SATA6G_P0_TX_C_DN
SATA_P3_TX_DP
SATA_P3_TX_DN
SATA_P2_TX_DN
SATA_P1_TX_DP
SATA_P1_TX_DN
SATA_P0_TX_DP
SATA_P0_TX_DN
SSATA_TXP3 BF40 SATAX6G_P3_TX_DP
SSATA_TXN3 BH40 SATAX6G_P3_TX_DN
SSATA_TXP2 BF42 SATAX6G_P2_TX_DP
SSATA_TXN2 BH42 SATAX6G_P2_TX_DN
SSATA_TXP1 BD46 SATAX6G_P1_TX_DP
SSATA_TXN1 BE48 SATAX6G_P1_TX_DN
SSATA_TXP0 BB48 SATAX6G_P0_TX_DP
SSATA_TXN0 BB46 SATAX6G_P0_TX_DN
SATALED_N J7 LED_SATA_ACT_N
LED_SATA_ACT
DS66 OPT0000577
KPT-1608NG97A01-KM
R2405 1B0 1% 0603
P3V3
SSATA3GP BF38 PU_SATAX3GP
SSATA2GP BH36 PU_SATAX2GP
SSATA1GP BF36 PU_SATAX1GP
SSATA0GP AW32 PU_SATAX0GP
SATA5GP_GPIO49_MGPIO10 B28 FM_CPU0_PROCHOT_LVT3_N
SATA4GP_GPIO16_MGPIO9 A9 FM_CPU1_PROCHOT_LVT3_N
SATA3GP_GPIO37 G11 PU_ADR_TRIGGER_N
SATA2GP_GPIO36 B5 NOA_R_10_FM_BIOS_ADV_FUNCTIONS
SATA1GP_GPIO19 B24 NOA_9_R_RST_PCIE_PCH_N
SATA0GP_GPIO21 D4 PD_PCH_GP21
SDATAOUT1_GPIO48 D6 PU_SGPIO_SATA_DATAOUT1
SDATAOUT0_GPIO39 M21 PU_SGPIO_SATA_DATAOUT0
SSDATAOUT1 BF34 SGPIO_SATAX_DATAOUT1
SSDATAOUT0 BH38 SGPIO_SATAX_DATAOUT0
RESERVED6 B26 PU_PCH_A20GATE
RCIN_N C25 PU_PCH_RCIN_N
SERIRQ L21 IRQ_SERIAL
THRMTRIP_N A13 FM_LVC1_THERMTRIP_N
PECI A21 PECI_PCH
PM_SYNC J18 H_PM_SYNC_G
PM_SYNC_2 BJ27 TP_PM_SYNC2
DIFFCLK_BIASREF BA11 PCH_XCLK_BIASREF_R
R896 7.5K 1% 0402
P1V5_PCH
R897 10K 1% 0402
R898 10K 1% 0402
R891 1K 1% 0402
SYM 3 OF 11
DH82029PCH SLKDD
DESIGN NOTE:
TERMINATING UNUSED 1-WIRE BUS TO GND.
CAD NOTE:
PLACE RESISTORS AS CLOSE AS POSSIBLE TO PCH.
R959 10K 1% 0402 PU_TACH0
R1909 10K 1% 0402 PU_TACH1
R244 10K 1% 0402 PU_TACH2
R3956 10K 1% 0402 PU_TACH3
R1184 10K 1% 0402 PU_SGPIO_SATA_DATAOUT1
R1185 10K 1% 0402 PU_SGPIO_SATA_DATAOUT0
R1186 10K 1% 0402 PU_SGPIO_SATA_CLOCK
R1187 10K 1% 0402 PU_SGPIO_SATA_LOAD
R892 10K 1% 0402
R893 10K 1% 0402
R894 10K 1% 0402
R895 10K 1% 0402
PU_SATAX0GP
PU_SATAX1GP
PU_SATAX3GP
PU_SATAX2GP
CPLD_PWRGD_PCH_APWROK
D12 DI0000018B5 BAT54HT1G
R1101 1.6K 1% 0402
R1100 3.3K 1% 0402
C1078 1UF 10V 0402
CPLD_PWRGD_PCH_R_APWROK
U87 LOG0000823 SN74LVC2G14DCKR
P3V3_STBY
BUF0_PWRGD_PCH_APWROK
R1102 49.9 1% 0402
BUF0_PWRGD_PCH_R_APWROK
BUF1_PWRGD_PCH_APWROK
R1103 49.9 1% 0402
PWRGD_PCH_APWROK
C1080 0.1UF 16V 0402
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WELLSBURG (3 OF 3)
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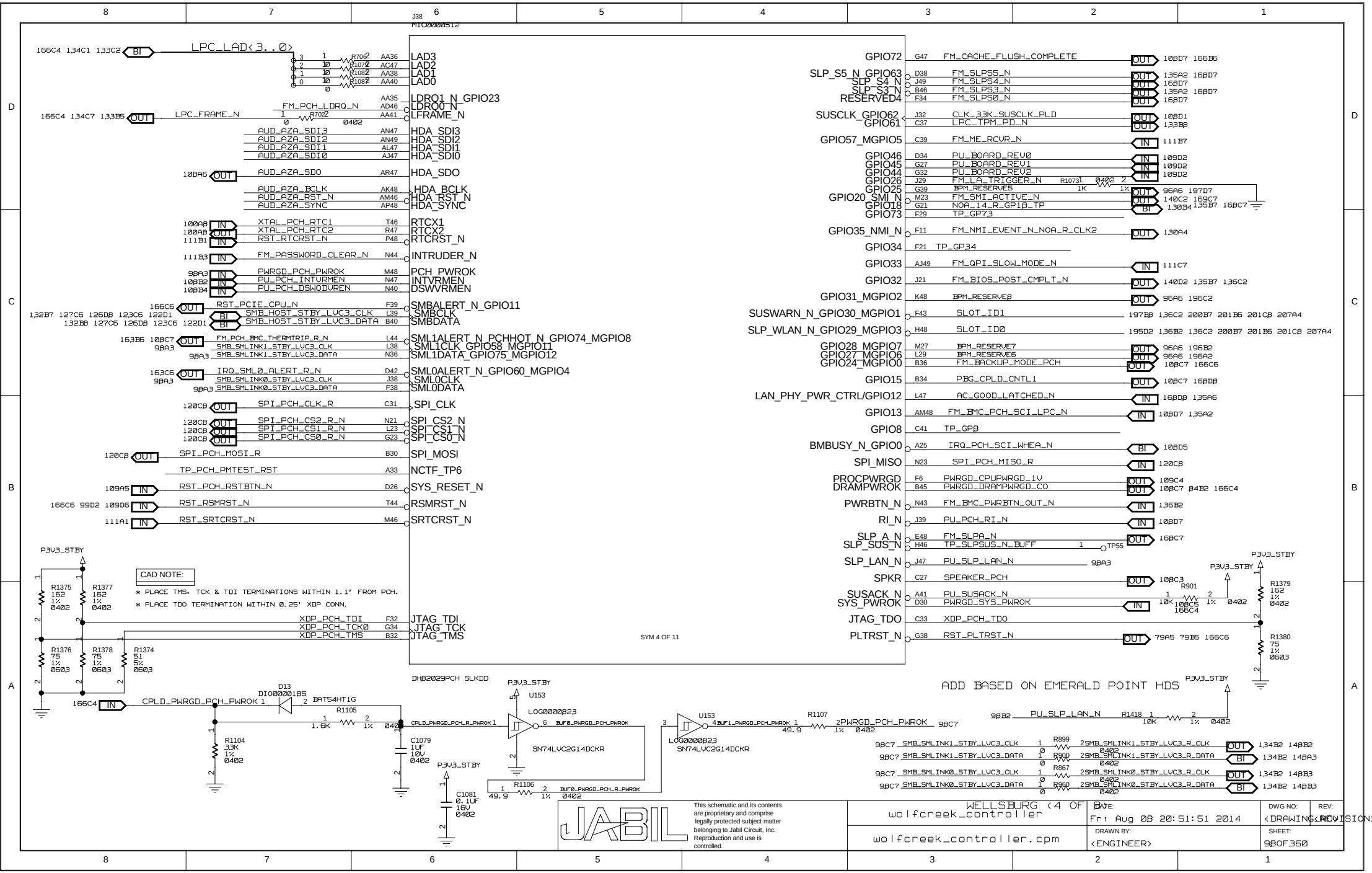
SHEET: 97OF360


J38
MIC0000512
LPC_LAD(3..0)
LAD3 AA36
LAD2 AC47
LAD1 AA38
LAD0 AA40
LDRQ1_N_GPIO23 AA35
LDRQ0_N AD46
LFRAME_N AA41
HDA_SDI3 AN47
HDA_SDI2 AN49
HDA_SDI1 AL47
HDA_SDI0 AJ47
HDA_SDO AR47
HDA_BCLK AK48
HDA_RST_N AM46
HDA_SYNC AP48
RTCX1 T46
RTCX2 R47
RTCRST_N P48
INTRUDER_N N44
PCH_PWROK M48
INTVRMEN N47
DSWVRMEN N40
SMBALERT_N_GPIO11 F39
SMBCLK L39
SMBDATA B40
SML1ALERT_N_PCHHOT_N_GPIO74_MGPIO8 L44
SML1CLK_GPIO58_MGPIO11 L38
SML1DATA_GPIO75_MGPIO12 N36
SML0ALERT_N_GPIO60_MGPIO4 D42
SML0CLK J38
SML0DATA F38
SPI_CLK C31
SPI_CS2_N N21
SPI_CS1_N L23
SPI_CS0_N G23
SPI_MOSI B30
NCTF_TP6 A33
SYS_RESET_N D26
RSMRST_N T44
SRTCRST_N M46
JTAG_TDI F32
JTAG_TCK G34
JTAG_TMS B32
SYM 4 OF 11
GPIO72 G47 FM_CACHE_FLUSH_COMPLETE
SLP_S5_N_GPIO63 D38 FM_SLPS5_N
SLP_S4_N J49 FM_SLPS4_N
SLP_S3_N B46 FM_SLPS3_N
RESERVED4 F34 FM_SLPS0_N
SUSCLK_GPIO62 J32 CLK_33K_SUSCLK_PLD
GPIO61 C37 LPC_TPM_PD_N
GPIO57_MGPIO5 C39 FM_ME_RCVR_N
GPIO46 D34 PU_BOARD_REV0
GPIO45 G27 PU_BOARD_REV1
GPIO44 G32 PU_BOARD_REV2
GPIO26 J29 FM_LA_TRIGGER_N
GPIO25 G39 BPM_RESERVE5
GPIO20_SMI_N M23 FM_SMI_ACTIVE_N
GPIO18 G21 NOA_14_R_GP18_TP
GPIO73 F29 TP_GP73
GPIO35_NMI_N F11 FM_NMI_EVENT_N_NOA_R_CLK2
GPIO34 F21 TP_GP34
GPIO33 AJ49 FM_QPI_SLOW_MODE_N
GPIO32 J21 FM_BIOS_POST_CMPLT_N
GPIO31_MGPIO2 K48 BPM_RESERVE8
SUSWARN_N_GPIO30_MGPIO1 F43 SLOT_ID1
SLP_WLAN_N_GPIO29_MGPIO3 H48 SLOT_ID0
GPIO28_MGPIO7 M27 BPM_RESERVE7
GPIO27_MGPIO6 L29 BPM_RESERVE6
GPIO24_MGPIO0 B36 FM_BACKUP_MODE_PCH
GPIO15 B34 PBG_CPLD_CNTL1
LAN_PHY_PWR_CTRL/GPIO12 L47 AC_GOOD_LATCHED_N
GPIO13 AM48 FM_BMC_PCH_SCI_LPC_N
GPIO8 C41 TP_GP8
BMBUSY_N_GPIO0 A25 IRQ_PCH_SCI_WHEA_N
SPI_MISO N23 SPI_PCH_MISO_R
PROCPWRGD F6 PWRGD_CPUPWRGD_1V
DRAMPWROK B45 PWRGD_DRAMPWRGD_CO
PWRBTN_N N43 FM_BMC_PWRBTN_OUT_N
RI_N J39 PU_PCH_RI_N
SLP_A_N E48 FM_SLPA_N
SLP_SUS_N H46 TP_SLPSUS_N_BUFF
SLP_LAN_N J47 PU_SLP_LAN_N
SPKR C27 SPEAKER_PCH
SUSACK_N A41 PU_SUSACK_N
SYS_PWROK D30 PWRGD_SYS_PWROK
JTAG_TDO C33 XDP_PCH_TDO
PLTRST_N G38 RST_PLTRST_N
CAD NOTE:
* PLACE TMS, TCK & TDI TERMINATIONS WITHIN 1.1' FROM PCH.
* PLACE TDO TERMINATION WITHIN 0.25' XDP CONN.
ADD BASED ON EMERALD POINT HDS
DH82029PCH SLKDD
U153
LOG0000823
SN74LVC2G14DCKR
CPLD_PWRGD_PCH_PWROK
BAT54HT1G
D13
DI0000018B5
R1105 1.6K
R1104 33K
C1079 1UF 16V
C1081 0.1UF 16V
R1106 49.9
R1107 49.9
2PWRGD_PCH_PWROK
PU_SLP_LAN_N
R1418 10K
R901 10K
R899
R900
R867
R860
2SMB_SMLINK1_STBY_LUVC3_R_CLK
2SMB_SMLINK1_STBY_LUVC3_R_DATA
2SMB_SMLINK0_STBY_LUVC3_R_CLK
2SMB_SMLINK0_STBY_LUVC3_R_DATA
R1375 162
R1377 162
R1376 75
R1378 75
R1374 51
R1379 162
R1380 75
P3V3_STBY
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WELLSBURG (4 OF 8)
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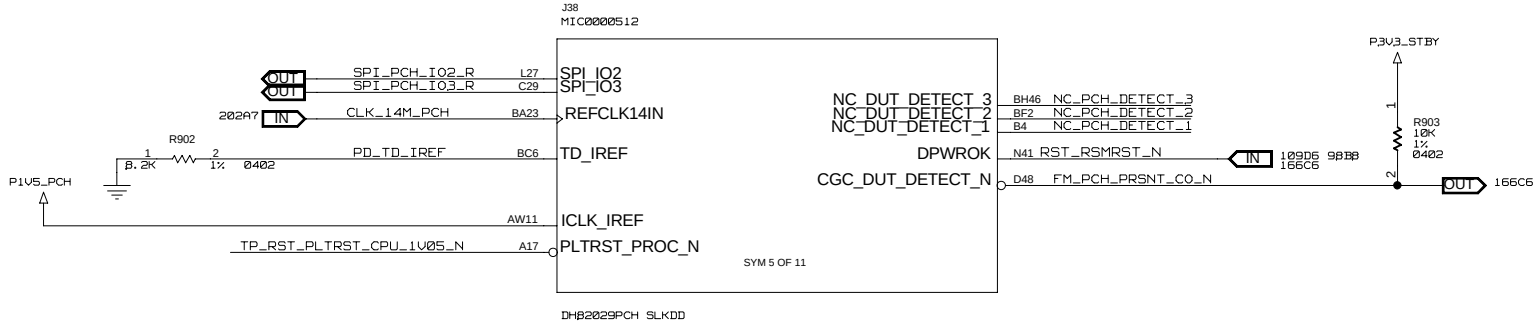
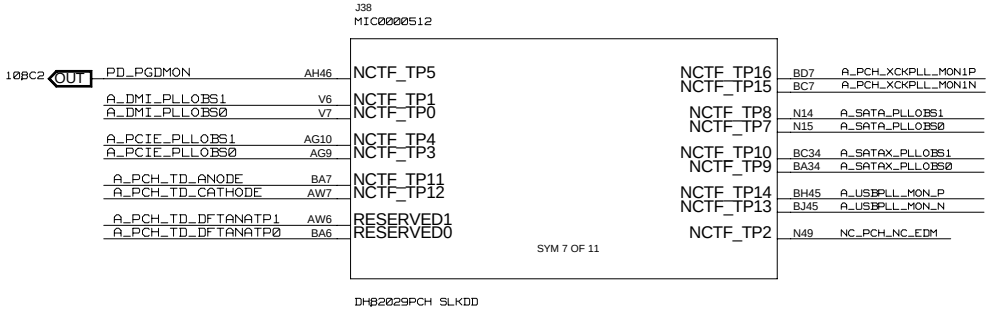
DATE: Fri Aug 08 20:51:51 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 98OF360





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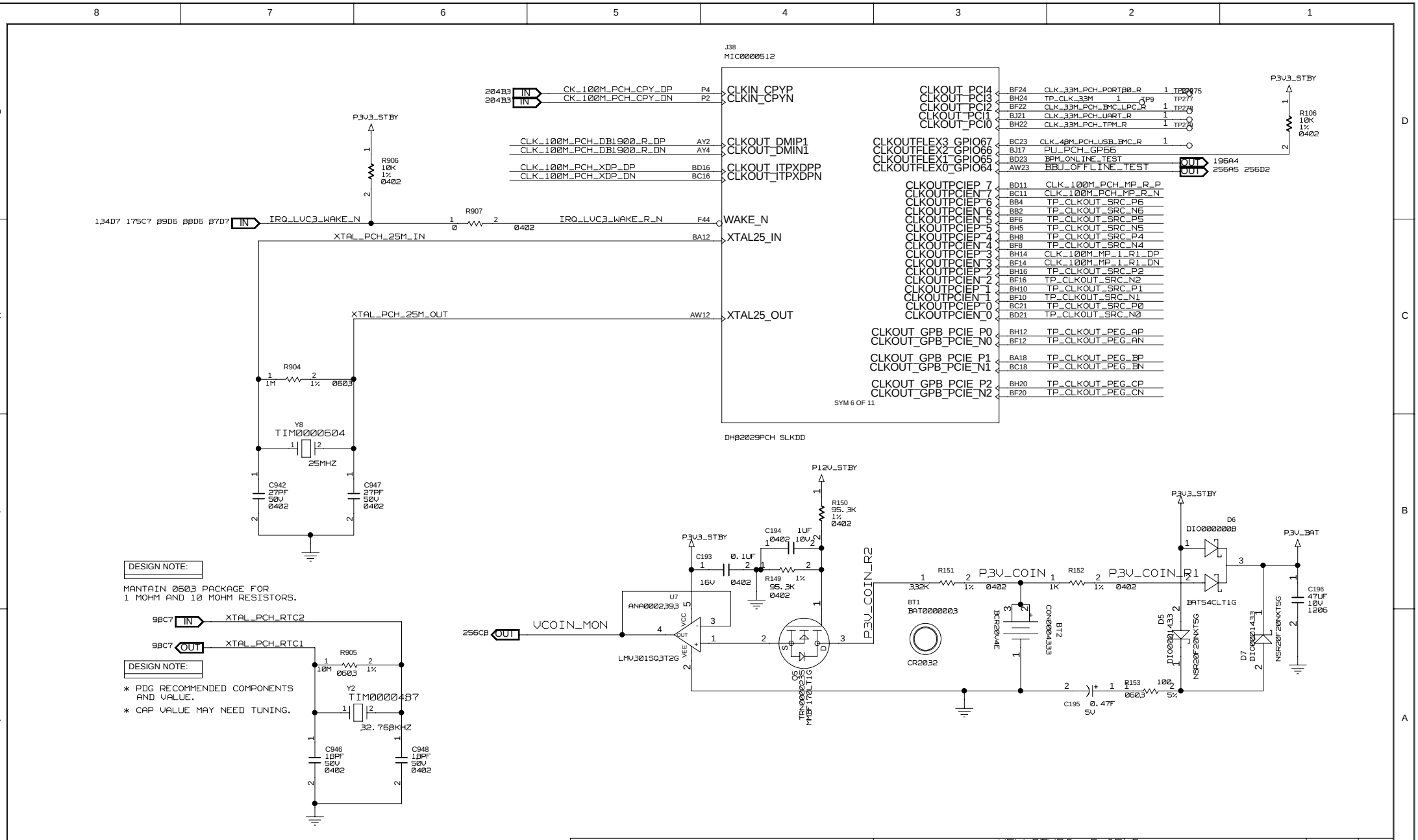
WELLSBURG (5 OF 8) wolfcreek_controller	DATE: Wed Jul 30 14:58:52 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 99OF360	



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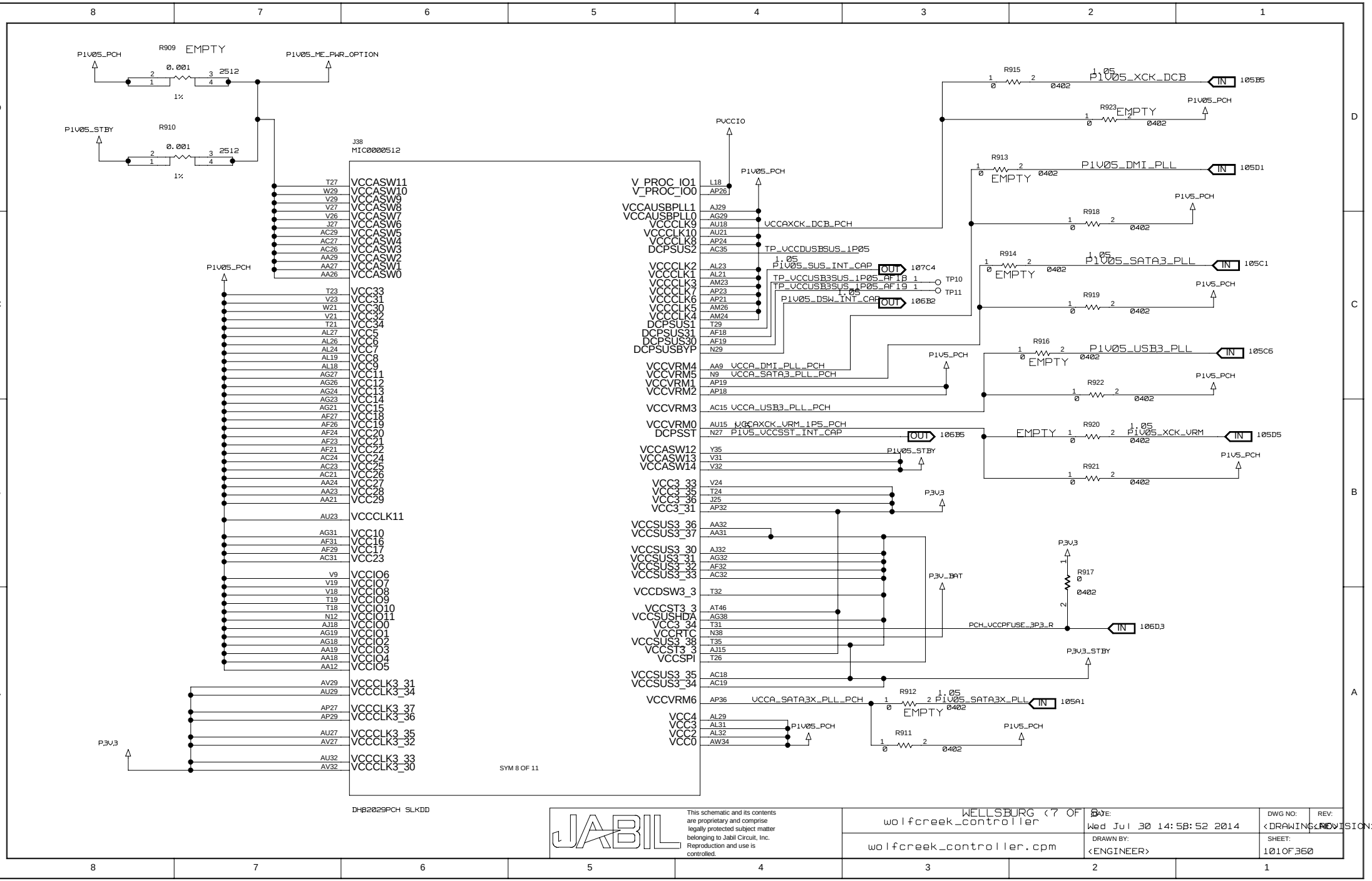
WELLSBURG (6 OF 8) wolfcreek_controller	DATE: Fri Aug 08 20:07:28 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 10 OF 360	



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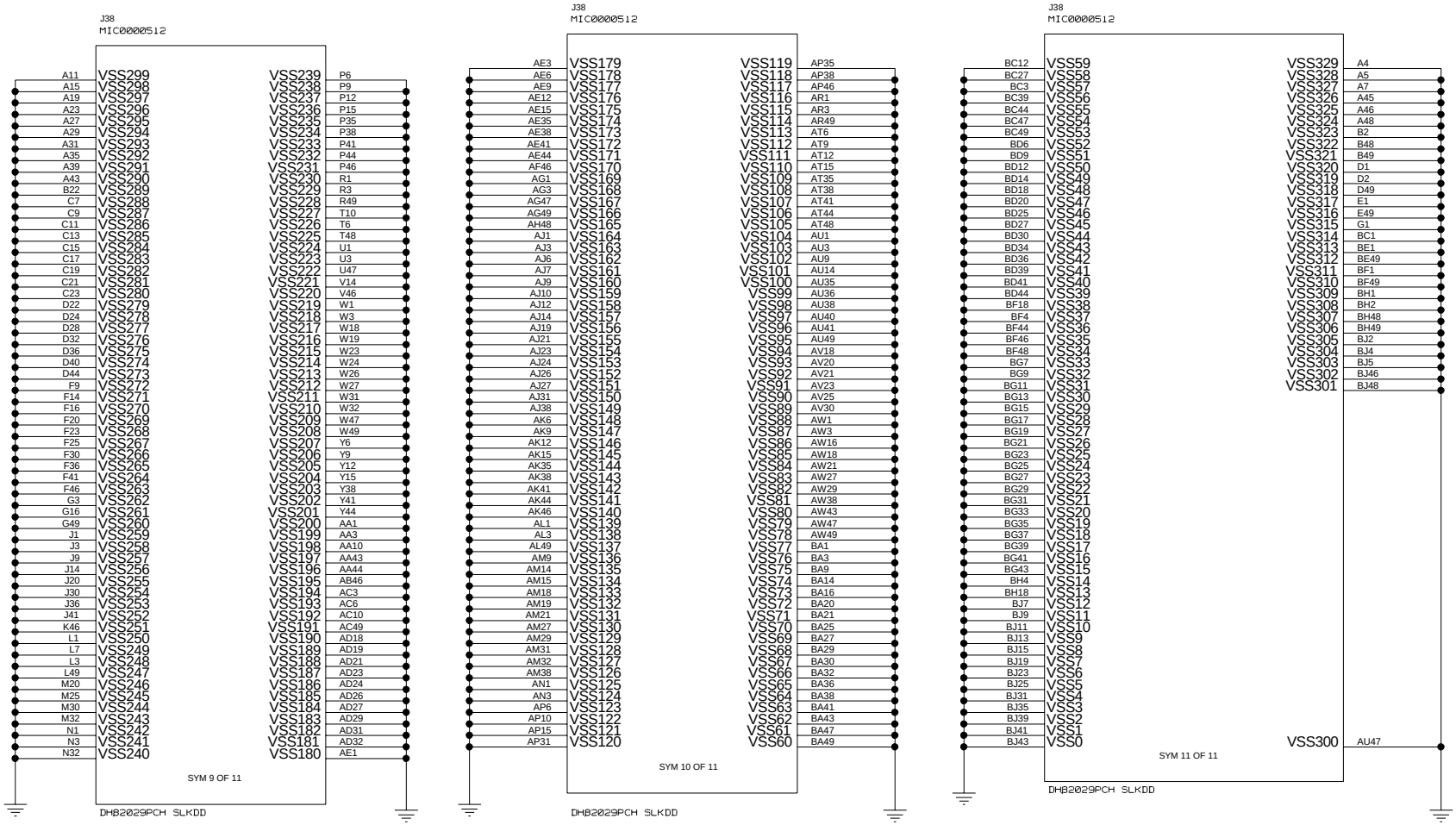
WELLSBURG (7 OF 8) wolfcreek_controller	DATE: Wed Jul 30 14:58:52 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 101 OF 360	



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WELLSBURG (8 OF 8) wolfcreek_controller	DATE: Wed Jul 30 15:00:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 102OF360	

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BLANK wolfcreek_controller	DATE: Sat Jun 28 11:05:48 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 103OF360	

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WBG DCMI
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Mon Jul 21 17:41:57 2014

DRAWN BY: <ENGINEER>

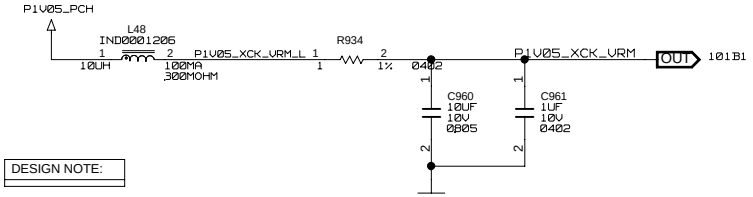
DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 104OF360

ROOM=WBG_FILTERING

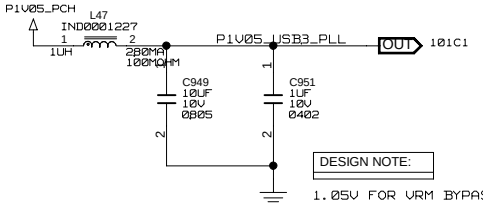
P1V05_XCK_VRM - CLOCK INTEGRATION



DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

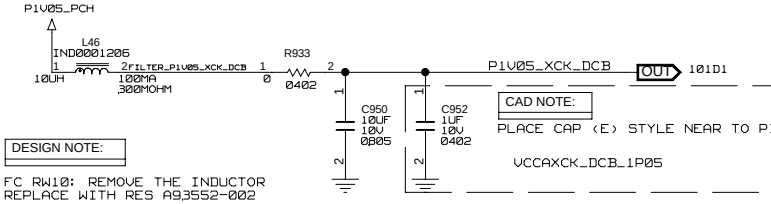
USB3 PLL FILTER



DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

P1V05_XCK_DCB - CLOCK INTEGRATION



CAD NOTE:

PLACE CAP (E) STYLE NEAR TO PIN.

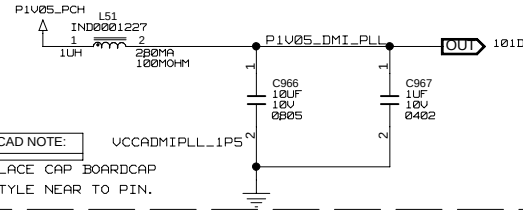
VCCAXCK_DCB_1P05

DESIGN NOTE:

FC RW10: REMOVE THE INDUCTOR
REPLACE WITH RES A93552-002
EMPTY CAP 10UF
ALLOWS FOR BYPASS OPTION WITH DISCRETE CAP.

DMI PLL FILTER

1.05V PCIE/DMI SECTION

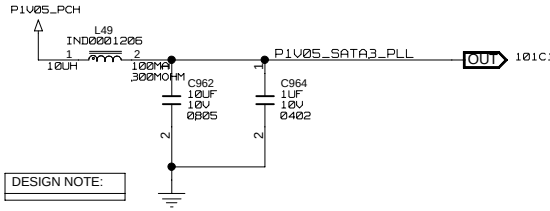


CAD NOTE:

VCCADMIPLL_1P5

PLACE CAP BOARDCAP
STYLE NEAR TO PIN.

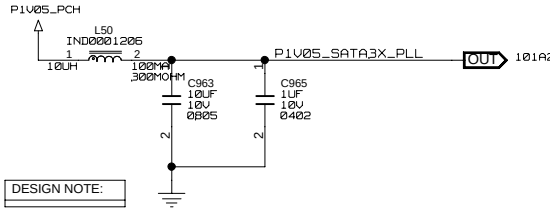
SATA PLL FILTER



DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

SATAX PLL FILTER



DESIGN NOTE:

1.05V FOR VRM BYPASS MODE (FILT REQUIRED).
1.5 WHEN USING INTERNAL VRM (NO FILT REQUIRED).
THIS POWER IS SUPPLIED WITH CORE WELL.

CAD NOTE:

PUT L & C AS CLOSE AS POSSIBLE WITH THE 10MIL TRACE MAX LENGTH OF 240MIL
A MINIMUM TRACE WIDTH OF 35MIL IS REQUIRED TO INTERCONNECT THE RESISTANCES

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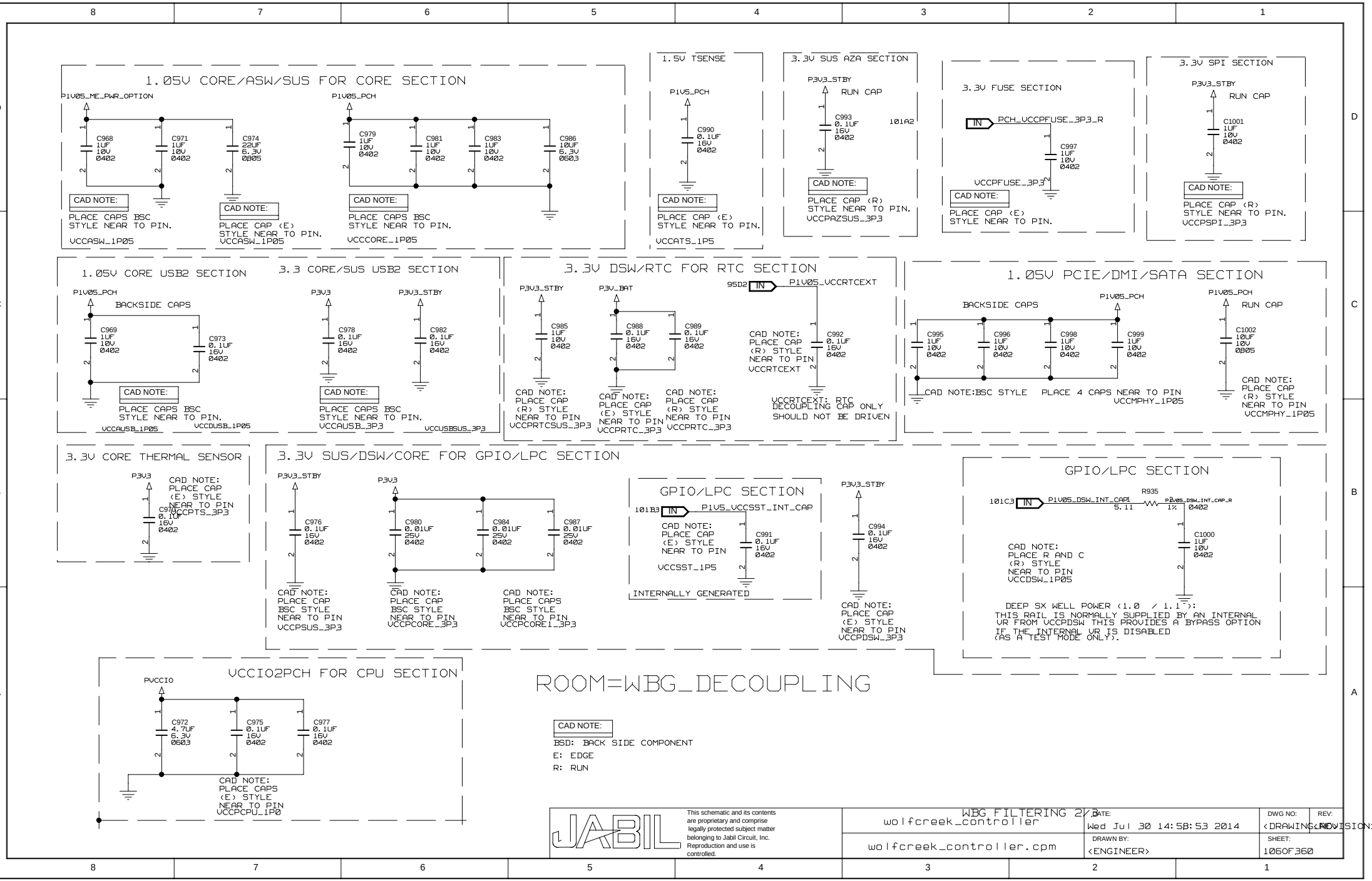
WBG FILTERING 1/3 wolfcreek_controller	DATE: Wed Jul 30 14:58:53 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 105OF360	


1.05V CORE/ASW/SUS FOR CORE SECTION
P1V05_ME_PWR_OPTION
C968 1UF 10V 0402
C971 1UF 10V 0402
C974 22UF 6.3V 0805
CAD NOTE:
PLACE CAPS BSC STYLE NEAR TO PIN.
VCCASW_1P05
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN.
VCCASW_1P05
P1V05_PCH
C979 1UF 10V 0402
C981 1UF 10V 0402
C983 1UF 10V 0402
C986 10UF 6.3V 0603
CAD NOTE:
PLACE CAPS BSC STYLE NEAR TO PIN.
VCCCORE_1P05
1.5V TSENSE
P1V5_PCH
C990 0.1UF 16V 0402
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN.
VCCATS_1P5
3.3V SUS AZA SECTION
P3V3_STBY
RUN CAP
C993 0.1UF 16V 0402
101A2
CAD NOTE:
PLACE CAP (R) STYLE NEAR TO PIN.
VCCPAZSUS_3P3
3.3V FUSE SECTION
IN
PCH_VCCPFUSE_3P3_R
C997 1UF 10V 0402
VCCPFUSE_3P3
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN.
3.3V SPI SECTION
P3V3_STBY
RUN CAP
C1001 1UF 10V 0402
CAD NOTE:
PLACE CAP (R) STYLE NEAR TO PIN.
VCCPSPI_3P3
1.05V CORE USB2 SECTION
P1V05_PCH
BACKSIDE CAPS
C969 1UF 10V 0402
C973 0.1UF 16V 0402
CAD NOTE:
PLACE CAPS BSC STYLE NEAR TO PIN.
VCCAUSB_1P05
VCCDUSB_1P05
3.3 CORE/SUS USB2 SECTION
P3V3
C978 0.1UF 16V 0402
P3V3_STBY
C982 0.1UF 16V 0402
CAD NOTE:
PLACE CAPS BSC STYLE NEAR TO PIN.
VCCAUSB_3P3
VCCUSBSUS_3P3
3.3V DSW/RTC FOR RTC SECTION
P3V3_STBY
C985 1UF 10V 0402
P3V_BAT
C988 0.1UF 16V 0402
C989 0.1UF 16V 0402
95D2
IN
P1V05_VCCRTCEXT
C992 0.1UF 16V 0402
CAD NOTE:
PLACE CAP (R) STYLE NEAR TO PIN
VCCRTCEXT
CAD NOTE:
PLACE CAP (R) STYLE NEAR TO PIN
VCCPRTCSUS_3P3
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN
VCCPRTC_3P3
CAD NOTE:
PLACE CAP (R) STYLE NEAR TO PIN
VCCPRTC_3P3
VCCRTCEXT: RTC DECOUPLING CAP ONLY SHOULD NOT BE DRIVEN
1.05V PCIE/DMI/SATA SECTION
BACKSIDE CAPS
P1V05_PCH
C995 1UF 10V 0402
C996 1UF 10V 0402
C998 1UF 10V 0402
C999 1UF 10V 0402
CAD NOTE:BSC STYLE
PLACE 4 CAPS NEAR TO PIN
VCCMPHY_1P05
P1V05_PCH
RUN CAP
C1002 10UF 10V 0805
CAD NOTE:
PLACE CAP (R) STYLE NEAR TO PIN
VCCMPHY_1P05
3.3V CORE THERMAL SENSOR
P3V3
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN
C970 0.1UF 16V 0402
VCCPTS_3P3
3.3V SUS/DSW/CORE FOR GPIO/LPC SECTION
P3V3_STBY
C976 0.1UF 16V 0402
CAD NOTE:
PLACE CAP BSC STYLE NEAR TO PIN
VCCPSUS_3P3
P3V3
C980 0.01UF 25V 0402
C984 0.01UF 25V 0402
C987 0.01UF 25V 0402
CAD NOTE:
PLACE CAP BSC STYLE NEAR TO PIN
VCCPCORE_3P3
CAD NOTE:
PLACE CAPS BSC STYLE NEAR TO PIN
VCCPCORE1_3P3
GPIO/LPC SECTION
101B3
IN
P1V5_VCCSST_INT_CAP
C991 0.1UF 16V 0402
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN
VCCSST_1P5
INTERNALLY GENERATED
P3V3_STBY
C994 0.1UF 16V 0402
CAD NOTE:
PLACE CAP (E) STYLE NEAR TO PIN
VCCPDSW_3P3
GPIO/LPC SECTION
101C3
IN
P1V05_DSW_INT_CAP1
R935
5.11
1%
P1V05_DSW_INT_CAP_R
0402
C1000 1UF 10V 0402
CAD NOTE:
PLACE R AND C (R) STYLE NEAR TO PIN
VCCDSW_1P05
DEEP SX WELL POWER (1.0 / 1.1):
THIS RAIL IS NORMALLY SUPPLIED BY AN INTERNAL VR FROM VCCPDSW THIS PROVIDES A BYPASS OPTION IF THE INTERNAL VR IS DISABLED (AS A TEST MODE ONLY).
VCCIO2PCH FOR CPU SECTION
PVCCIO
C972 4.7UF 6.3V 0603
C975 0.1UF 16V 0402
C977 0.1UF 16V 0402
CAD NOTE:
PLACE CAPS (E) STYLE NEAR TO PIN
VCCPCPU_1P0
ROOM=WBG_DECOUPLING
CAD NOTE:
BSD: BACK SIDE COMPONENT
E: EDGE
R: RUN
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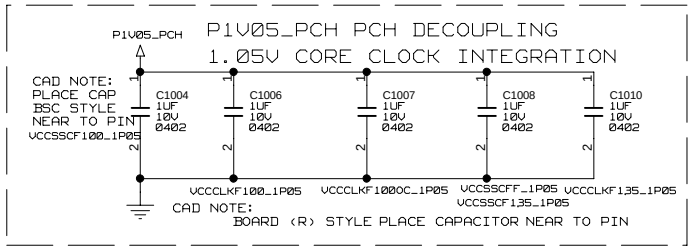
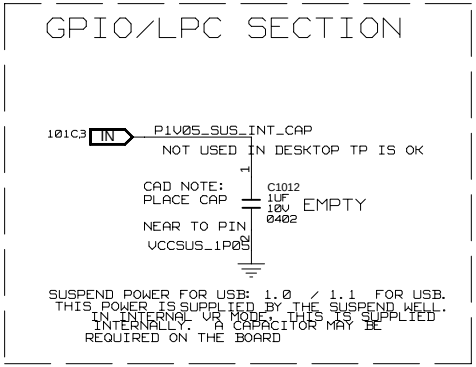
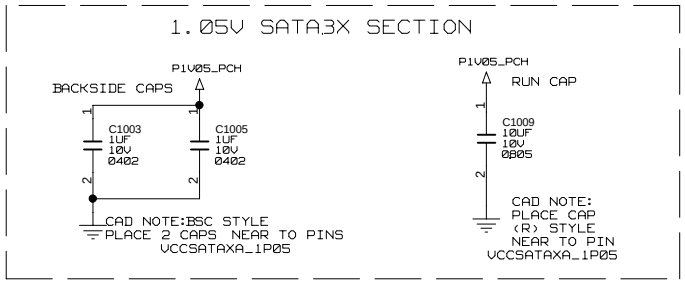
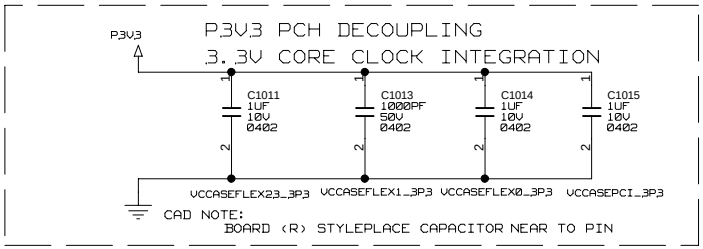
WBG FILTERING 2/2
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Wed Jul 30 14:58:53 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
106OF360





ROOM=WBG_DECOUPLING





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WBG FILTERING 3/3
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:54 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 107OF360

P3V3_STBY

EMPTY R939 10K 1% 0402 MCU_INIT OUT 130C5 168C8

EMPTY R1600 10K 1% 0402 ADR_STATUS OUT 168D7 130C5

R941 10K 1% 0402 PU_PCH_RI_N OUT 98B2

R942 10K 1% 0402 FM_CACHE_FLUSH_COMPLETE OUT 98D2 166B6

R944 10K 1% 0402 FM_BMC_PCH_SCI_LPC_N OUT 135A2 98B2

R945 10K 1% 0402 PWRGD_DRAMPWRGD_CO OUT 98B2 84B2 166C4

R946 10K 1% 0402 FM_PCH_BMC_THERMTRIP_R_N OUT 98C8 163B6

R947 10K 1% 0402 PBG_CPLD_CNTL0 OUT 96B7 168C1

R1316 10K 1% 0402 BPM_PRESENT_L OUT 196A4 97C8

R949 10K 1% 0402 IRQ_SML1_PMBUS_ALERT_N OUT 135B7

R2124 10K 1% 0402 PBG_CPLD_CNTL1 OUT 98C2 168D8

EMPTY R2406 10K 1% 0402 FM_BACKUP_MODE_PCH OUT 98C2 166C6

P3V3

R954 10K 1% 0402 IRQD_N_DEDI_PCH_R OUT 95C7

R955 10K 1% 0402 PU_SGPIO_GSX_RESET OUT

R956 10K 1% 0402 IRQ_PCH_SCI_WHEA_N OUT 98B2

R958 10K 1% 0402 PU_GP18 OUT 130B1

R961 10K 1% 0402 FM_CPU_ERR0_CO_N OUT 77B1 95C7

D37 DIO0000012 MBR05330T1G

IRQ_D R962 10K 1% 0402 IRQ_SERIAL OUT 97B2 133B5 134B7

R957 10K 1% 0402 FM_ERR1_DLY_N OUT 166B6 95C7

R2408 10K 1% 0402 FM_BMC_PCH_SMI_LPC_N OUT 135A2 95C7

R1971 10K 1% 0402 SFAOS_RUNNING OUT 95D8 136B8

R950 10K 1% 0402 PD_PCH_GP21 OUT 97C2

R951 10K 1% 0402 PWRGD_SYS_PWROK OUT 166C4 98A2

CAD NOTE: PLACE RES AS CLOSE AS POSSIBLE TO WBG

EMPTY R974 1K 1% 0402 CLK_33K_SUSCLK_PLD 98D2

DESIGN NOTE:
PLL ON-DIE VOLTAGE REGULATOR ENABLE
ENABLED WHEN SAMPLED HIGH (DEFAULT)
DISABLED WHEN SAMPLED LOW
WEAK INTERNAL PULL-UP (15K - 40K)

P3V3

R969 3.3K 1% 0402 SPEAKER_PCH OUT 98B2

DESIGN NOTE:
NO REBOOT
REBOOT DISABLE WHEN HIGH (DEFAULT)
INTERNAL PULL DOWN (15K-40K)

EMPTY R968 1K 1% 0402 PD_PGDMON OUT 99B6

DESIGN NOTE:
DFXTESTMODE ACTIVE
P/U: TEST MODE IS DISABLED (DEFAULT)
P/D: TEST MODE IS ENABLED
PCH PROVIDES WEAK INTERNAL P/U (8K-15K)

P3V3

R975 1K 1% 0402 2PU_ADR_TRIGGER_N OUT 169C1 97C2

DESIGN NOTE:
TLS CONFIDENTIALITY ENABLE
ENABLED WHEN SAMPLED HIGH (DEFAULT)
DISABLED WHEN SAMPLED LOW
INTERNAL PULL DOWN (15K-40K)

EMPTY R938 1K 1% 0402 RST_PCIE_PCH_N OUT 130D1 166C6

BOOT BIOS STRAPS (BBS)		
GNT[1]_GSXDOUT BBS[1]	BIOS_SPI_WP BBS[0]	
0	0	LPC
1	1	SPI (DEFAULT)

INTERNAL PULL-UP (15K-40K).
DISABLED AFTER PLTRST# DEASSERTS.

P3V3_BAT

R964 3.32K 1% 0402 PU_PCH_DSWODVREN OUT 98C7

EMPTY R965 1K 1% 0402

DESIGN NOTE:
DSWODVREN: DEEP SLEEP WELL ON-DIE VOLTAGE REGULATOR ENABLE-
P/U: DSW ODVR IS ENABLED (DEFAULT)
P/D: DSW ODVR IS DISABLED

P3V3_BAT

R971 3.32K 1% 0402 PU_PCH_INTVRMEN OUT 98C7

DESIGN NOTE:
INTERNAL VRM ENABLE: THIS SIGNAL IS USED TO ENABLE OR DISABLE THE INTEGRATED 1.05 VOLTAGE REGULATORS FOR THE SUSPEND WELL ON THE WELLSBURG
P/U: ENABLED VR (DEFAULT)
P/D: DISABLES VR

P/D OPTION NOT BEING PROVIDED

P3V3_STBY

R937 1K 1% 0402 AUD_AZA_SDO_R

J41 CON0001091 22-28-4026

1AUD_AZA_SDO OUT 98D7

FLASH DESCRIPTOR SECURITY OVERRIDE
FLASH DESCRIPTOR SECURITY OVERRIDE WHEN HIGH SET JUMPER
FLASH DESCRIPTOR SECURITY NO OVERRIDE WHEN LOW (DEFAULT, NO JPR)

INTERNAL PULL-DOWN(9K-50K)
NOTE: MANUFACTURING JUMPER ALSO CAN BE USED TO SET THIS STRAP

ROOM = WBG_PU_STRAPS

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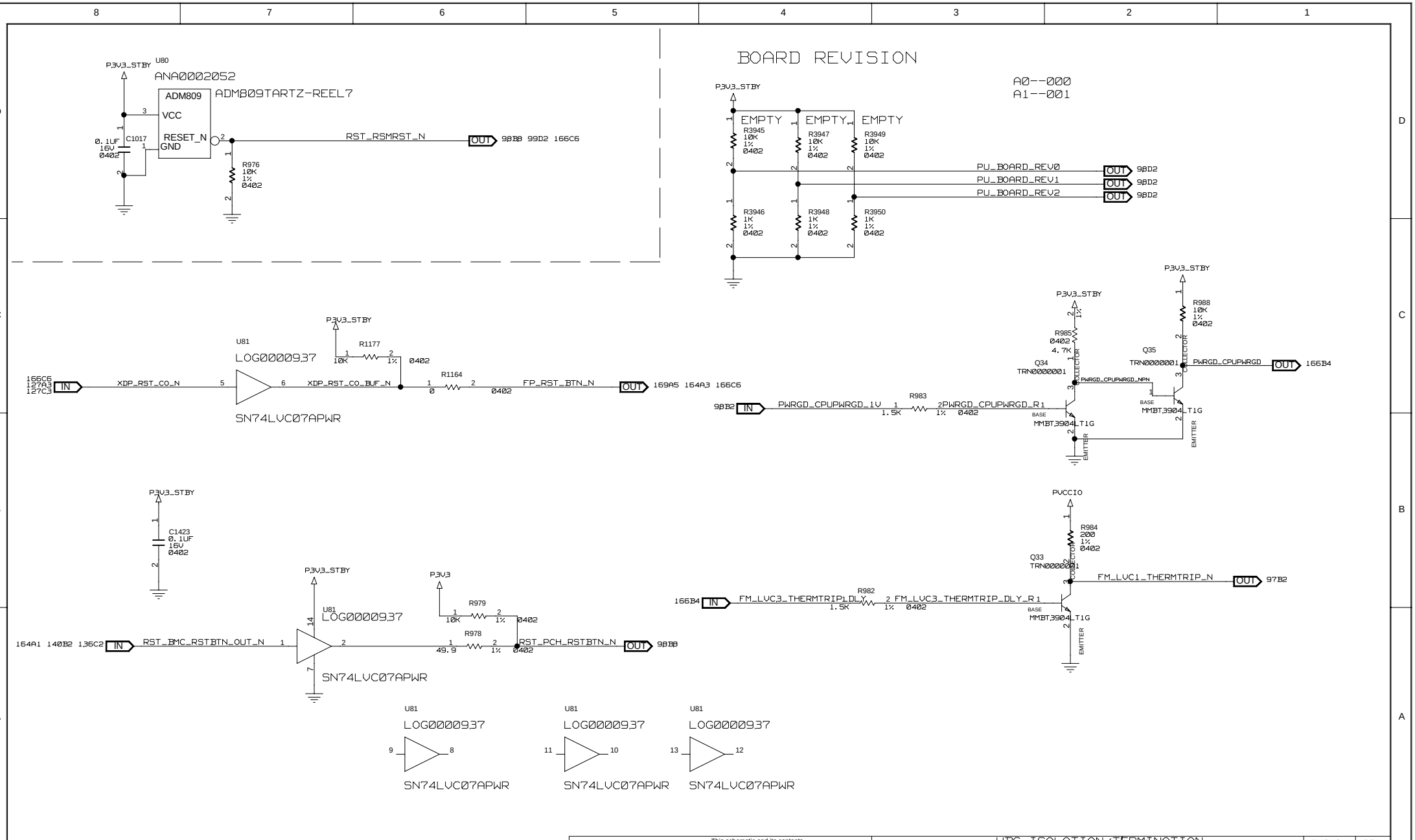
WBG STRAPPING/MISC wolfcreek_controller	PAGE: 1-2 Fri Aug 08 20:24:30 2014	DWG NO: (DRAWING NO)	REV: (REVISION)
wolfcreek_controller.cpm	DRAWN BY: (ENGINEER)	SHEET: 108OF360	


BOARD REVISION
A0--000
A1--001
P3V3_STBY
U80
ANA0002052
ADM809
ADM809TARTZ-REEL7
VCC
RESET_N
GND
C1017
0.1UF
16V
0402
RST_RSMRST_N
OUT
98B8 99D2 166C6
R976
10K
1%
0402
EMPTY
R3945
R3947
R3949
R3946
R3948
R3950
PU_BOARD_REV0
PU_BOARD_REV1
PU_BOARD_REV2
99D2
U81
LOG00009,37
R1177
R1164
XDP_RST_CO_N
XDP_RST_CO_BUF_N
FP_RST_BTN_N
169A5 164A3 166C6
SN74LVC07APWR
R988
R985
4.7K
Q34
TRN0000001
Q35
PWRGD_CPUPWRGD
166B4
PWRGD_CPUPWRGD_NPN
R983
PWRGD_CPUPWRGD_1V
PWRGD_CPUPWRGD_R1
MMBT3904LT1G
COLLECTOR
BASE
EMITTER
C1423
0.1UF
16V
0402
R979
R978
RST_BMC_RSTBTN_OUT_N
RST_PCH_RSTBTN_N
164A1 140B2 136C2
PVCCIO
R984
200
Q33
FM_LVC1_THERMTRIP_N
97B2
R982
FM_LVC3_THERMTRIP_DLY
FM_LVC3_THERMTRIP_DLY_R1
WBG ISOLATION/TERMINATION
wolfcreek_controller
wolfcreek_controller.cpm
Thu Aug 07 10:48:41 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
109OF360
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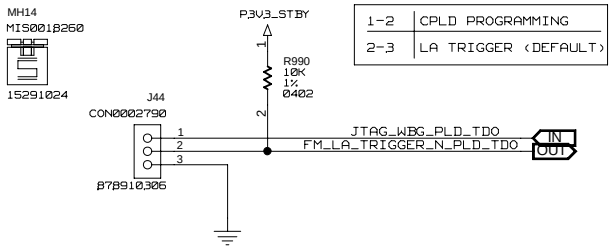
MANUFACTURING MODE JUMPER

STORAGE SV TRIGGER



1-2	CPLD PROGRAMMING
2-3	LA TRIGGER <DEFAULT>

HDD ACTIVITY

MGPIO HEADER

ADR_COMPLETE JUMPER

ROOM = WBG_HEADERS_BIOS

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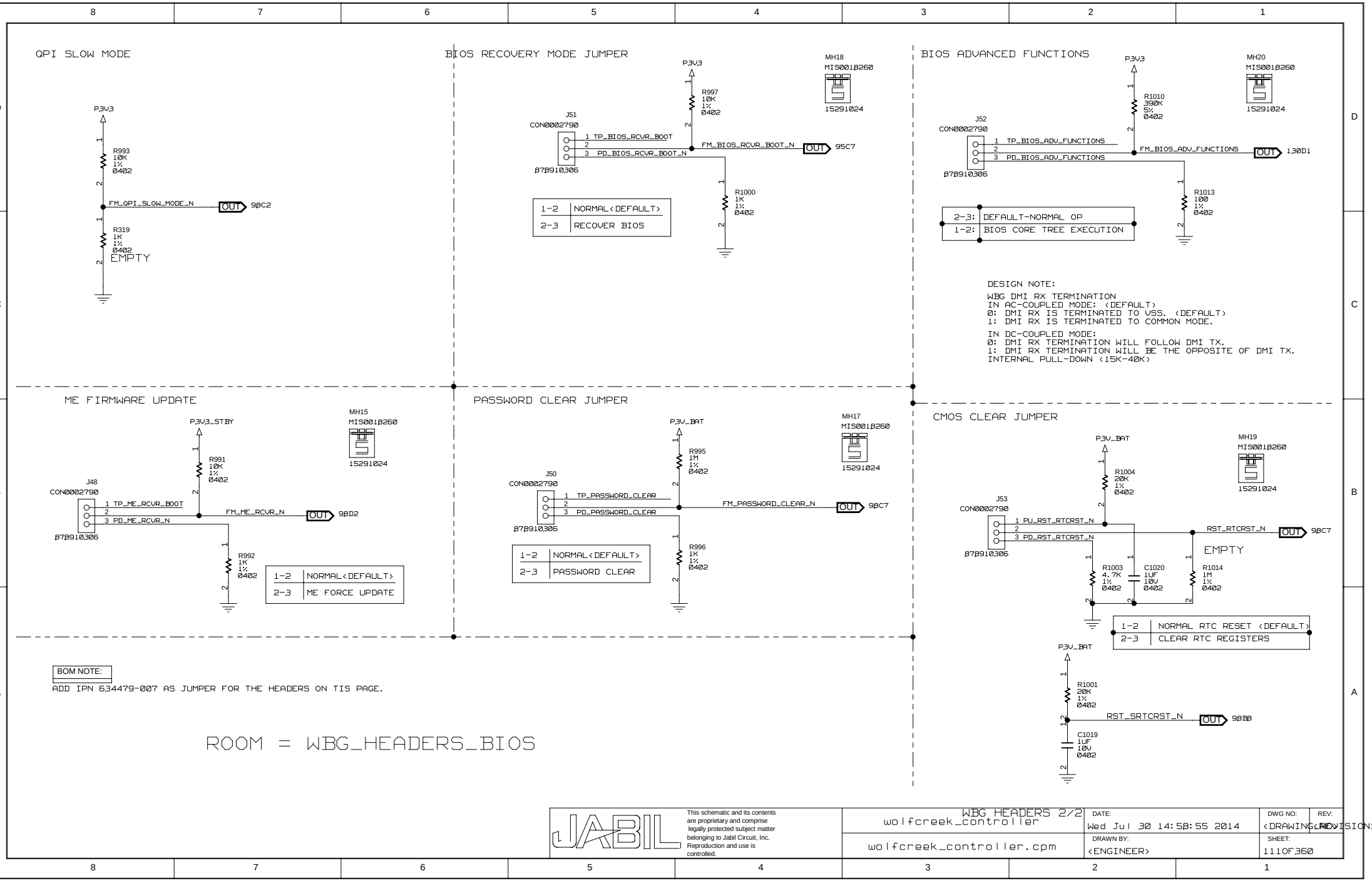
WBG HEADERS 1/2
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:54 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 110OF360


QPI SLOW MODE
P3V3
R993
10K
1%
0402
FM_QPI_SLOW_MODE_N
OUT
9BC2
R319
1K
1%
0402
EMPTY
BIOS RECOVERY MODE JUMPER
P3V3
R997
10K
1%
0402
MH18
MIS001B260
15291024
J51
CON0002790
1 TP_BIOS_RCVR_BOOT
2
3 PD_BIOS_RCVR_BOOT_N
87B910306
FM_BIOS_RCVR_BOOT_N
OUT
95C7
R1000
1K
1%
0402
1-2 NORMAL<DEFAULT>
2-3 RECOVER BIOS
BIOS ADVANCED FUNCTIONS
P3V3
R1010
390K
5%
0402
MH20
MIS001B260
15291024
J52
CON0002790
1 TP_BIOS_ADV_FUNCTIONS
2
3 PD_BIOS_ADV_FUNCTIONS
87B910306
FM_BIOS_ADV_FUNCTIONS
OUT
130D1
R1013
100
1%
0402
2-3: DEFAULT-NORMAL OP
1-2: BIOS CORE TREE EXECUTION
DESIGN NOTE:
WBG DMI RX TERMINATION
IN AC-COUPLED MODE: <DEFAULT>
0: DMI RX IS TERMINATED TO VSS. <DEFAULT>
1: DMI RX IS TERMINATED TO COMMON MODE.
IN DC-COUPLED MODE:
0: DMI RX TERMINATION WILL FOLLOW DMI TX.
1: DMI RX TERMINATION WILL BE THE OPPOSITE OF DMI TX.
INTERNAL PULL-DOWN (15K-40K)
ME FIRMWARE UPDATE
P3V3_STBY
R991
10K
1%
0402
MH15
MIS001B260
15291024
J48
CON0002790
1 TP_ME_RCVR_BOOT
2
3 PD_ME_RCVR_N
87B910306
FM_ME_RCVR_N
OUT
9BD2
R992
1K
1%
0402
1-2 NORMAL<DEFAULT>
2-3 ME FORCE UPDATE
PASSWORD CLEAR JUMPER
P3V_BAT
R995
1M
1%
0402
MH17
MIS001B260
15291024
J50
CON0002790
1 TP_PASSWORD_CLEAR
2
3 PD_PASSWORD_CLEAR
87B910306
FM_PASSWORD_CLEAR_N
OUT
9BC7
R996
1K
1%
0402
1-2 NORMAL<DEFAULT>
2-3 PASSWORD CLEAR
CMOS CLEAR JUMPER
P3V_BAT
R1004
20K
1%
0402
MH19
MIS001B260
15291024
J53
CON0002790
1 PU_RST_RTCRST_N
2
3 PD_RST_RTCRST_N
87B910306
RST_RTCRST_N
OUT
9BC7
EMPTY
R1003
4.7K
1%
0402
C1020
1UF
10V
0402
R1014
1M
1%
0402
1-2 NORMAL RTC RESET (DEFAULT)
2-3 CLEAR RTC REGISTERS
P3V_BAT
R1001
20K
1%
0402
RST_SRTCRST_N
OUT
9BBB
C1019
1UF
10V
0402
BOM NOTE:
ADD IPN 634479-007 AS JUMPER FOR THE HEADERS ON TIS PAGE.
ROOM = WBG_HEADERS_BIOS
JABIL
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WBG HEADERS 2/2
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Wed Jul 30 14:58:55 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
111OF360

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BLANK wolfcreek_controller	DATE: Wed Jul 02 11:35:55 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 112OF360	

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WBG GSX
wolfcreek_controller

wolfcreek_controller.cpm

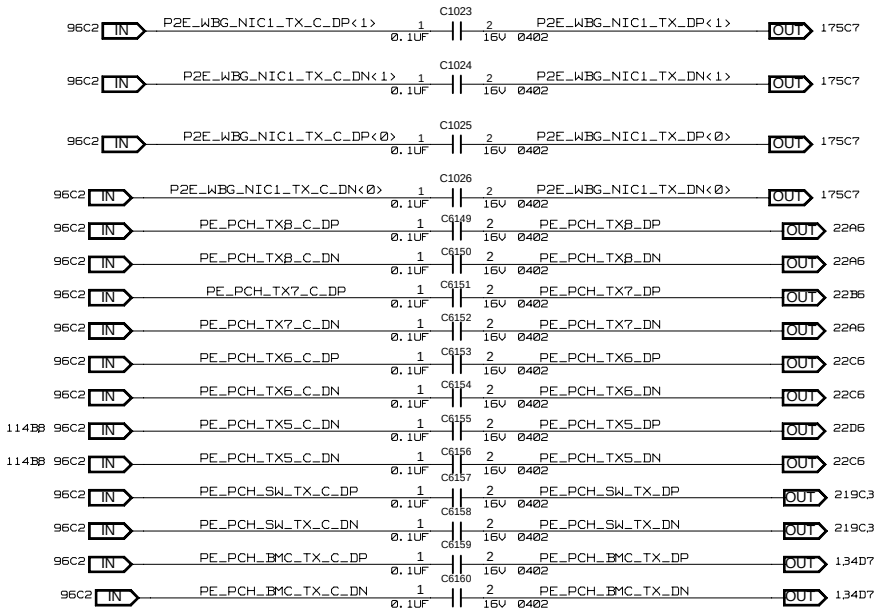
DATE: Sat Aug 02 19:14:50 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 113 OF 360



PLACE THESE 0.1UF CAPS NEAR WELLSBURG

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WBG PCIE AC COUPLING CAPS

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:56 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 114OF360

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WBG STRAPPING/MISC

wolfcreek_controller

wolfcreek_controller.cpm

DATE: 2-2
Wed Aug 06 17:33:47 2014

DRAWN BY:
<ENGINEER>

DWG NO:
<DRAWING>

REV:
<REVISION>

SHEET:
115OF360

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WBG HYBRID CLOCKING

wolfcreek_controller

wolfcreek_controller.cpm

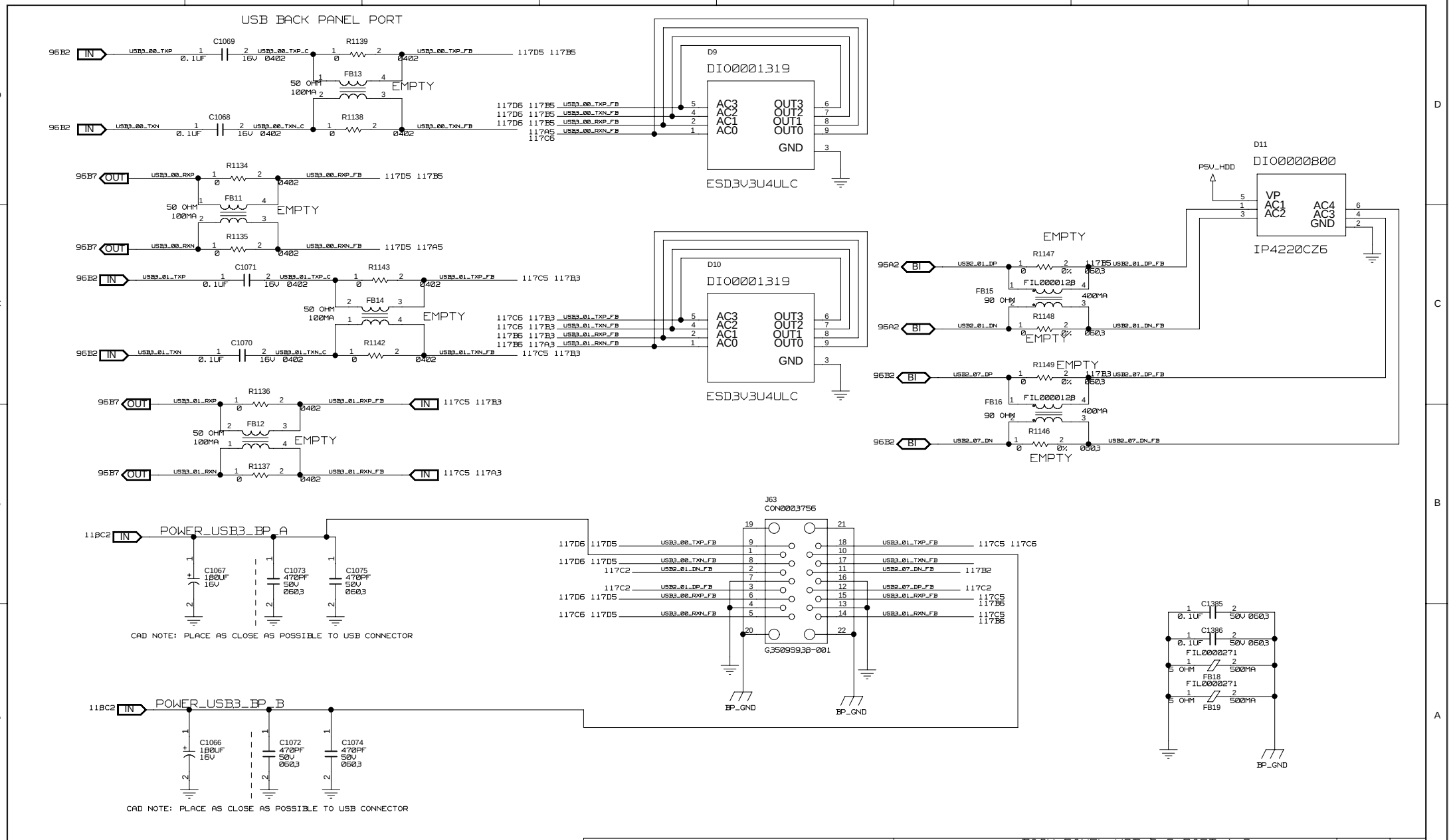
DATE: Sat Aug 02 17:24:07 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 116OF360



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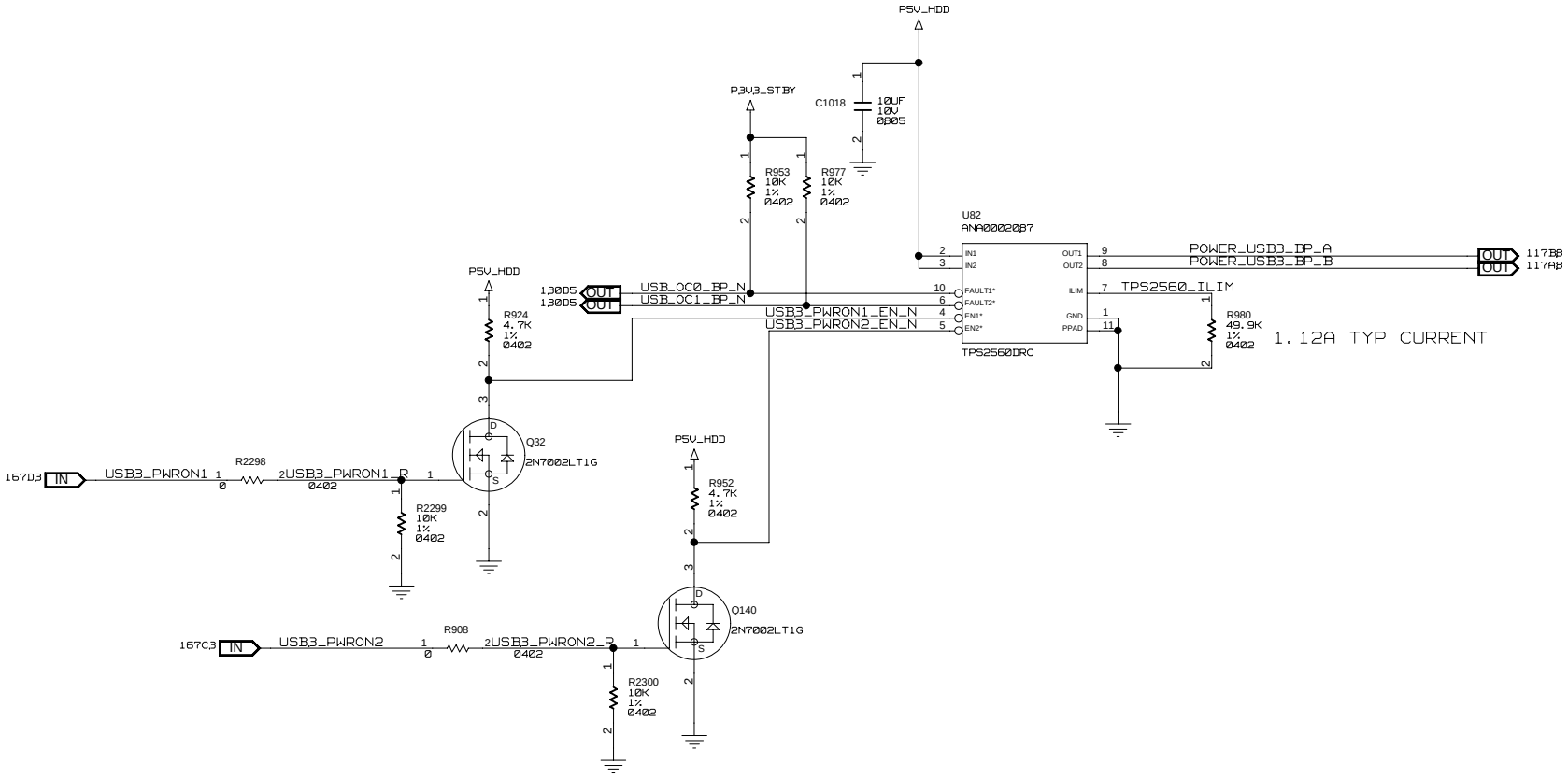
BACK PANEL USB BACK PORT 1/2		DWG NO:	REV:
wolfcreek_controller	DATE: Fri Aug 01 10:40:13 2014	<DRAWING>	<REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 1170F,360	



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BACK PANEL USB 3.0 PORT 2/2

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:57 2014

DRAWN BY: <ENGINEER>

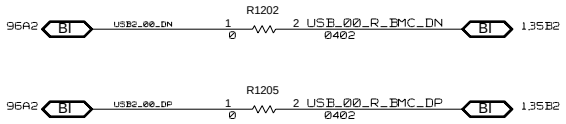
DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 118OF360

BMC USB PORT

CAD NOTE:
RESISTOR SWITCH
PUT PAD OVER PAD BOTH RESISTORS
IN ORDER TO AVOID STUB



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TO BMC USB PORT
wolfcreek_controller

wolfcreek_controller.cpm

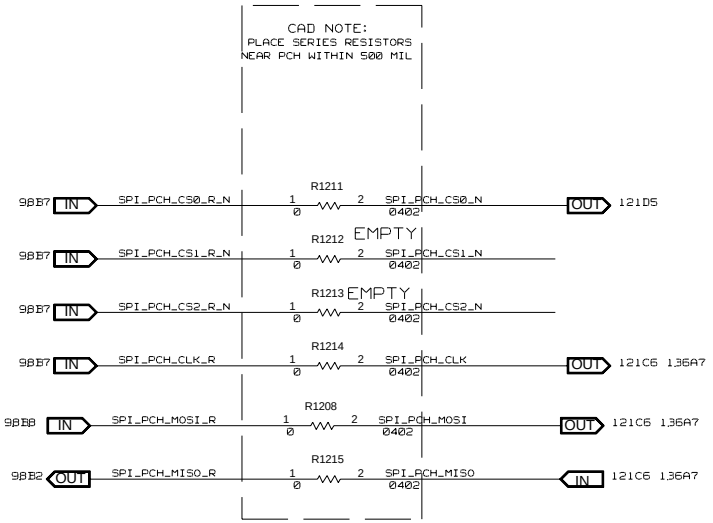
DATE: Thu Aug 07 17:07:54 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 1190F,360



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WELLSBURG SPI FLASH 1/2	PAGE:	DWG NO:	REV:
wolfcreek_controller	Sat Aug 02 19:20:02 2014	<DRAWING>	<REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 120OF360	

BIOS FLASH

U183
ANA0000950
NC7SB3157
NC7SB3157P6X

1.35B2 IN — SPI_FLASH_MUX_SEL — S
1.36A7 OUT — SPI_SYS_CS_N — B1
B0
VCC — P3V3_STBY
A — SPI_PCH_CS0_N — IN 120C6
GND

R879 1K 1% 0402
C1102 0.1UF 16V 0402

CAD NOTE:
PLACE ALL SERIES RESISTORS
EXCEPT MISO R NEAR WBG < 0.5"
AND MISO R NEAR SPI < 0.5"

1.36A7 120C6 IN — SPI_PCH_CLK — R1174 1 33 2
1.36A7 120C6 IN — SPI_PCH_MOSI — R1176 1 33 2% 0402 1% 0402
120C6 1.36A7 OUT — SPI_PCH_MISO — R1218 1 33 2
SPI_CKT0_CS0_N — R1219 1 33 2% 0402 1% 0402

P3V3_STBY
R1236 10K 0402 1%
R1238 10K 1% 0402

P3V3_STBY
U89
C1105 0.1UF 16V 0402
C1107 1UF 10V 0402

CAD NOTE:
PLACE CAPACITORS AS CLOSE
AS POSSIBLE TO SKT POWER PINS

CON0003416

VCC	2	NC<7>	14 — NC_SPI_BIOS0_BT_7
CLK	16 — SPI_SKT0_CLK_R	NC<6>	13 — NC_SPI_BIOS0_BT_6
DI_IO0	15 — SPI_SKT0_MOSI_R	NC<5>	12 — NC_SPI_BIOS0_BT_5
WP_N_IO2	9 — SPI_SKT0_WP_N	NC<4>	11 — NC_SPI_BIOS0_BT_4
DO_IO1	8 — SPI_SKT0_MISO_R	NC<3>	6 — NC_SPI_BIOS0_BT_3
CS_N	7 — SPI_CKT0_CS0_R_N	NC<2>	5 — NC_SPI_BIOS0_BT_2
HOLD_N_IO3	1 — SPI_SKT0_HLD_N	NC<1>	4 — NC_SPI_BIOS0_BT_1
		NC<0>	3 — NC_SPI_BIOS0_BT_0
		GND	10

ACA-SPI-006-K01
U88
MEM0000606
W25Q128BVFIG

SYS RECOVERY FLASH

CAD NOTE:
PLACE ALL SERIES RESISTORS
EXCEPT MISO R NEAR WBG < 0.5"
AND MISO R NEAR SPI < 0.5"

P3V3_STBY
R30 10K 0402 1%
R31 10K 1% 0402

P3V3_STBY
C1104 0.1UF 16V 0402
C1106 1UF 10V 0402

CAD NOTE:
PLACE CAPACITORS AS CLOSE
AS POSSIBLE TO SKT POWER PINS

1.36A3 IN — BACKUP_SPI_CLK — R9 1 33 2
1.36A3 IN — BACKUP_SPI_MOSI — R1098 1 33 2% 0402 1% 0402
1.36A3 OUT — BACKUP_SPI_MISO — R1165 1 33 2
1.36A3 IN — BACKUP_SPI_CS_N — R1166 1 33 2% 0402 1% 0402

U78
CON0003416

VCC	2	NC<7>	14 — NC_SPI_BIOS1_BT_7
CLK	16 — BACKUP_SPI_CLK_R	NC<6>	13 — NC_SPI_BIOS1_BT_6
DI_IO0	15 — BACKUP_SPI_MOSI_R	NC<5>	12 — NC_SPI_BIOS1_BT_5
WP_N_IO2	9 — SPI_SKT1_WP_N	NC<4>	11 — NC_SPI_BIOS1_BT_4
DO_IO1	8 — BACKUP_SPI_MISO_R	NC<3>	6 — NC_SPI_BIOS1_BT_3
CS_N	7 — BACKUP_SPI_CS_R_N	NC<2>	5 — NC_SPI_BIOS1_BT_2
HOLD_N_IO3	1 — SPI_SKT1_HLD_N	NC<1>	4 — NC_SPI_BIOS1_BT_1
		NC<0>	3 — NC_SPI_BIOS1_BT_0
		GND	10

ACA-SPI-006-K01
U77
MEM0000606
W25Q128BVFIG

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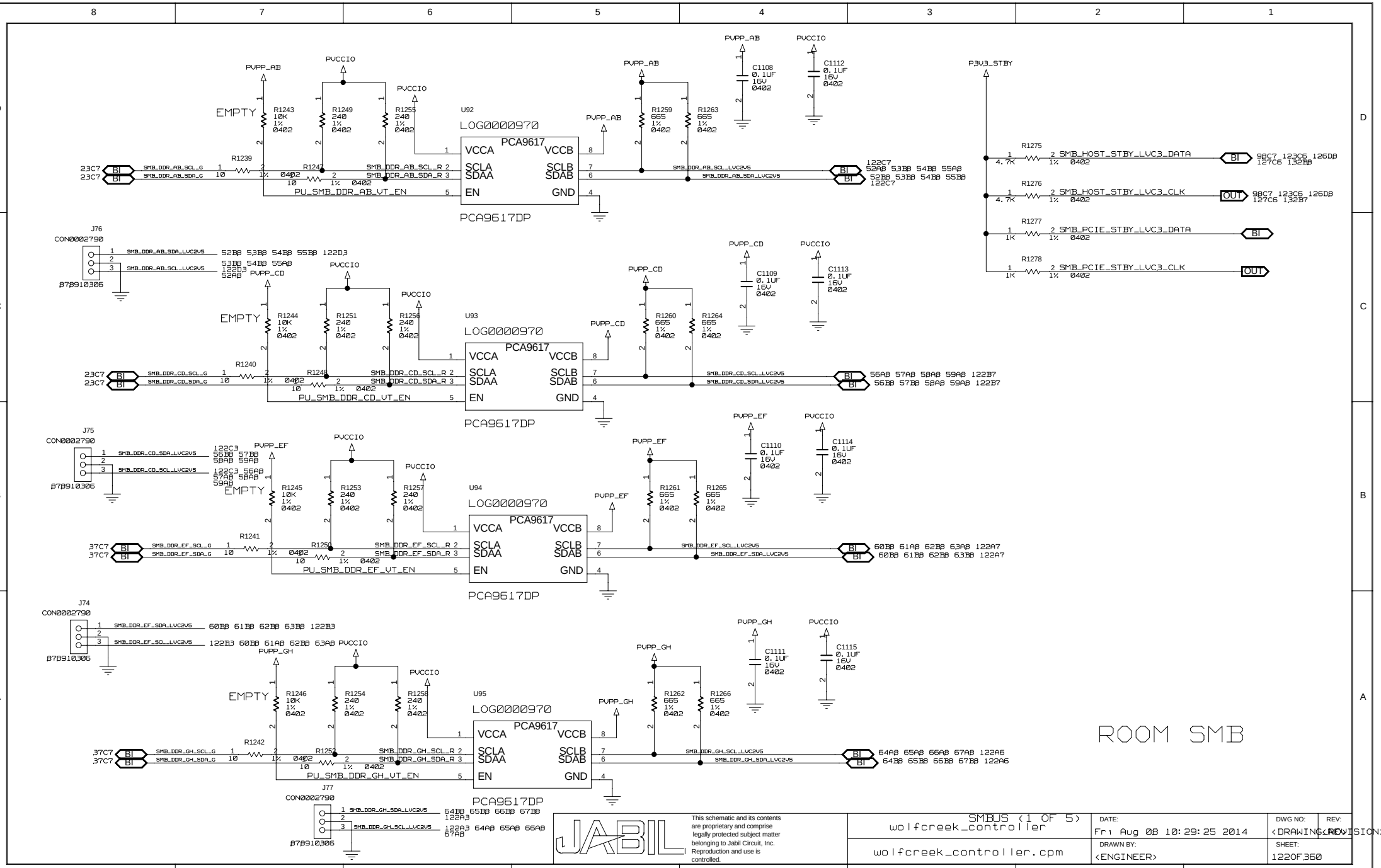
WELLSBURG SPI FLASH 2/2
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Fri Aug 08 17:04:58 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 121 OF 360


U92
LOG0000970
PCA9617
VCCA
VCCB
SCLA
SCLB
SDAA
SDAB
EN
GND
PCA9617DP
U93
U94
U95
PVPP_AB
PVPP_CD
PVPP_EF
PVPP_GH
PVCCIO
P3V3_STBY
EMPTY
R1243 10K 1% 0402
R1249 240 1% 0402
R1255 240 1% 0402
R1259 665 1% 0402
R1263 665 1% 0402
R1239
R1247
C1108 0.1UF 16V 0402
C1112 0.1UF 16V 0402
R1275 4.7K 1% 0402 2 SMB_HOST_STBY_LVC3_DATA
R1276 4.7K 1% 0402 2 SMB_HOST_STBY_LVC3_CLK
R1277 1K 1% 0402 2 SMB_PCIE_STBY_LVC3_DATA
R1278 1K 1% 0402 2 SMB_PCIE_STBY_LVC3_CLK
98C7 123C6 126D8 127C6 132B7
J76
CON0002790
B7B910306
R1244 10K 1% 0402
R1251 240 1% 0402
R1256 240 1% 0402
R1260 665 1% 0402
R1264 665 1% 0402
C1109 0.1UF 16V 0402
C1113 0.1UF 16V 0402
R1240
R1248
PU_SMB_DDR_CD_VT_EN
J75
R1245 10K 1% 0402
R1253 240 1% 0402
R1257 240 1% 0402
R1261 665 1% 0402
R1265 665 1% 0402
C1110 0.1UF 16V 0402
C1114 0.1UF 16V 0402
R1241
R1250
PU_SMB_DDR_EF_VT_EN
J74
R1246 10K 1% 0402
R1254 240 1% 0402
R1258 240 1% 0402
R1262 665 1% 0402
R1266 665 1% 0402
C1111 0.1UF 16V 0402
C1115 0.1UF 16V 0402
R1242
R1252
PU_SMB_DDR_GH_VT_EN
J77
ROOM SMB
JABIL
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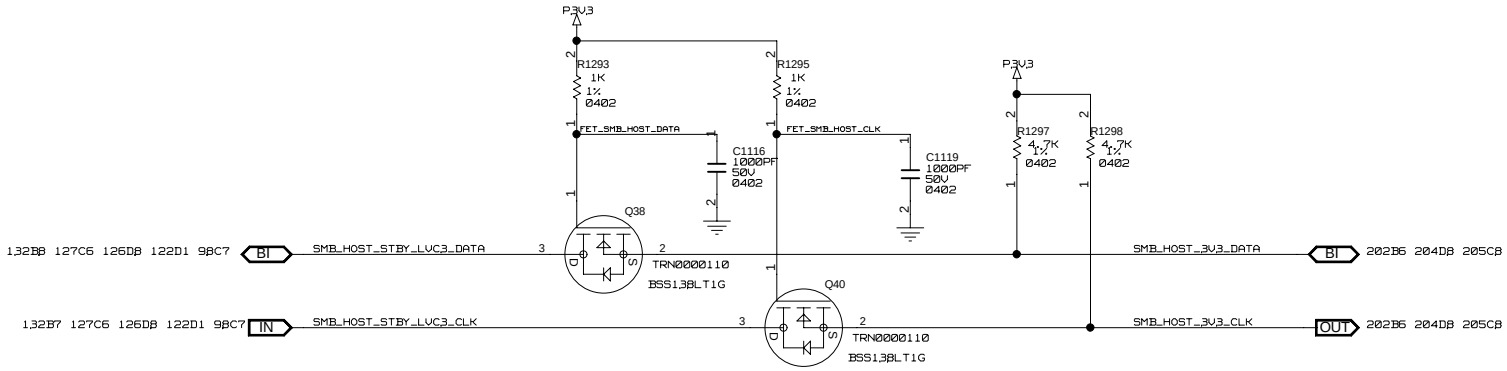
SMBUS (1 OF 5)
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Fri Aug 08 10:29:25 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING NO>
REV:
<REVISION>
SHEET:
122OF360



ROOM SMB

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SMBUS (2 OF 5) wolfcreek_controller	DATE: Thu Aug 07 21:10:29 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 123OF360	

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SMBUS (3 OF 5)
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 10:30:03 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 124OF360

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SMBUS (4 OF 5)
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 10:32:49 2014

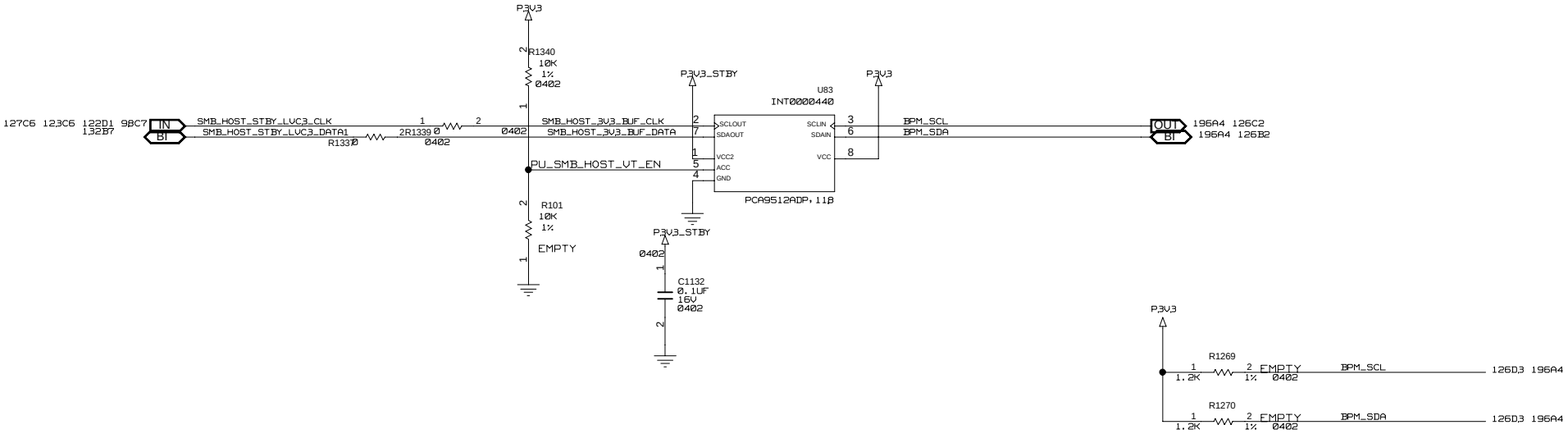
DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 125OF360

ROOM SMB



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SMBUS (5 OF 5) wolfcreek_controller	DATE: Fri Aug 08 15:36:10 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 126OF,360	

ROOM = CPU_XDP_DEBUG

CPU_XDP

J82 BSH-030-01-F-D-A-TR

CON00018,39

SCONN60_C21100002

PVCCIO

XDP_CPU0_PREQ_G_N
XDP_CPU0_PRDY_G_N
XDP_CPU0_OBSDATA_A_MBP2_G_N
XDP_CPU0_OBSDATA_A_MBP3_G_N
XDP_CPU0_OBSDATA_A_MBP4_G_N
XDP_CPU0_OBSDATA_A_MBP5_G_N
XDP_CPU_OBSFN_B_MBP6_G_N
XDP_CPU_OBSFN_B_MBP7_G_N
XDP_CPU1_OBSDATA_B_MBP2_G_N
XDP_CPU1_OBSDATA_B_MBP3_G_N
XDP_CPU1_OBSDATA_B_MBP4_G_N
XDP_CPU1_OBSDATA_B_MBP5_G_N
XDP_CPU_PWRGD
XDP_PWRGD_RST_N
SRP_CPU_PWR_DEBUG_N
XDP_CPU_SYSPWROK
SMB_HOST_STBY_LVC3_DATA
SMB_HOST_STBY_LVC3_CLK
TP_XDP_CPU_TCK1
XDP_CPU_TCK_G

TP_XDP_CPU_OBSFN_C0
TP_XDP_CPU_OBSFN_C1
TP_XDP_CPU_OBSDATA_C_MBP2
TP_XDP_CPU_OBSDATA_C_MBP3
TP_XDP_CPU_OBSDATA_C_MBP4
TP_XDP_CPU_OBSDATA_C_MBP5
TP_XDP_CPU_OBSFN_D0
TP_XDP_CPU_OBSFN_D1
TP_XDP_CPU_OBSDATA_D_MBP2
TP_XDP_CPU_OBSDATA_D_MBP3
TP_XDP_CPU_OBSDATA_D_MBP4
TP_XDP_CPU_OBSDATA_D_MBP5
CK_100M_XDP_DP
CK_100M_XDP_DN
XDP_CPU_RST_N
XDP_RST_CO_N
XDP_CPU_TDO
XDP_CPU_TRST_G_N
XDP_CPU_TDI
XDP_CPU_TMS_G
XDP_PRESENT_R_N

C1134 1UF 10V 0402
C1135 1UF 10V 0402

CAD NOTE:
PLACE R776 WITH 0 STUB FROM THE MAIN TRACE.

R1346 1K 1% 0402 PWRGD_CPU0_G

CAD NOTE:
PLACE R775 WITH 0 STUB FROM THE MAIN TRACE.

R1351 1K 1% 0402 RST_CPU0_G_N

R1352 0 0402 XDP_PRESENT_N

R981 100 1% 0402 EMPTY XDP_CPU1_OBSDATA_B_MBP5_G_N
R1076 100 1% 0402 EMPTY XDP_CPU1_OBSDATA_B_MBP4_G_N
R1077 100 1% 0402 EMPTY XDP_CPU1_OBSDATA_B_MBP3_G_N
R1083 100 1% 0402 EMPTY XDP_CPU1_OBSDATA_B_MBP2_G_N
R1112 100 1% 0402 EMPTY XDP_CPU0_OBSDATA_A_MBP5_G_N
R1113 100 1% 0402 EMPTY XDP_CPU0_OBSDATA_A_MBP4_G_N
R1114 100 1% 0402 EMPTY XDP_CPU0_OBSDATA_A_MBP3_G_N
R1115 100 1% 0402 EMPTY XDP_CPU0_OBSDATA_A_MBP2_G_N
R1349 200 1% 0402 XDP_CPU_OBSFN_B_MBP7_G_N
R1350 200 1% 0402 XDP_CPU_OBSFN_B_MBP6_G_N
R1347 475 1% 0402 XDP_PRESENT_N
R1348 150 1% 0402 SRP_CPU_PWR_DEBUG_N
C1133 0.1UF 16V 0402

CAD NOTE:
PLACE ALL THE CAPACITORS CLOSE TO THE XDP PIN.

P3V3_STBY

R1353 1K 1% 0402 XDP_CPU_SYSPWROK
C1136 0.1UF 16V 0402
R1354 1K 1% 0402 XDP_RST_CO_N
C1137 0.1UF 16V 0402
R1355 1K 1% 0402 XDP_PWRGD_RST_N
C1138 0.1UF 16V 0402

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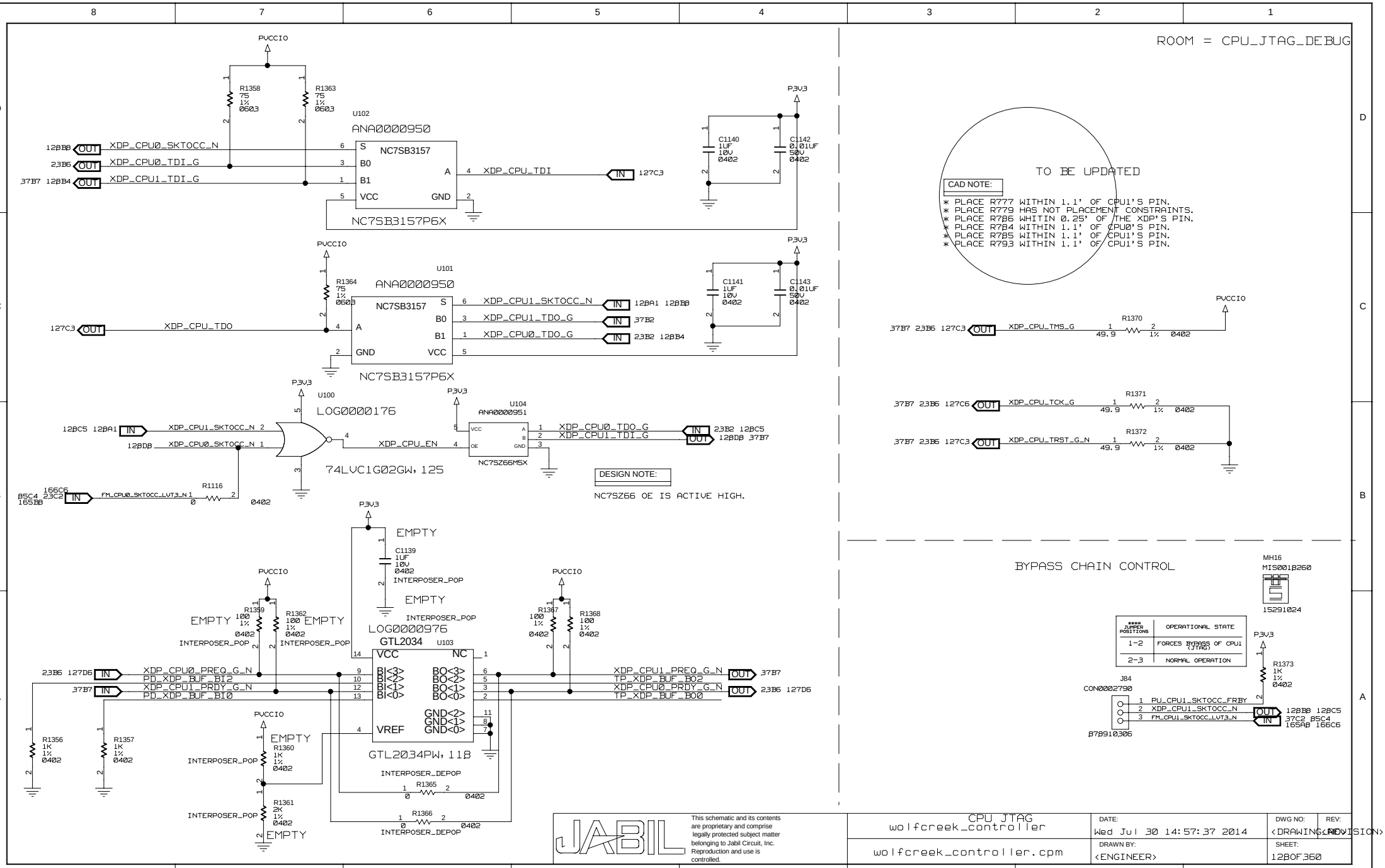
CPU_XDP wolfcreek_controller	DATE: Wed Jul 30 14:59:02 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 127OF360	


ROOM = CPU_JTAG_DEBUG
TO BE UPDATED
CAD NOTE:
* PLACE R777 WITHIN 1.1' OF CPU1'S PIN.
* PLACE R779 HAS NOT PLACEMENT CONSTRAINTS.
* PLACE R786 WHITIN 0.25' OF THE XDP'S PIN.
* PLACE R784 WITHIN 1.1' OF CPU0'S PIN.
* PLACE R785 WITHIN 1.1' OF CPU1'S PIN.
* PLACE R793 WITHIN 1.1' OF CPU1'S PIN.
PVCCIO
R1358 75 1% 0603
R1363 75 1% 0603
U102
ANA0000950
NC7SB3157
NC7SB3157P6X
XDP_CPU0_SKTOCC_N
XDP_CPU0_TDI_G
XDP_CPU1_TDI_G
XDP_CPU_TDI
P3V3
C1140 1UF 10V 0402
C1142 0.01UF 50V 0402
R1364 75 1% 0603
U101
XDP_CPU_TDO
XDP_CPU1_SKTOCC_N
XDP_CPU1_TDO_G
XDP_CPU0_TDO_G
C1141 1UF 10V 0402
C1143 0.01UF 50V 0402
U100
LOG0000176
74LVC1G02GW,125
XDP_CPU_EN
U104
ANA0000951
NC7SZ66M5X
XDP_CPU0_TDO_G
XDP_CPU1_TDI_G
DESIGN NOTE:
NC7SZ66 OE IS ACTIVE HIGH.
FM_CPU0_SKTOCC_LVT3_N
R1116 0 0402
XDP_CPU_TMS_G
R1370 49.9 1% 0402
XDP_CPU_TCK_G
R1371 49.9 1% 0402
XDP_CPU_TRST_G_N
R1372 49.9 1% 0402
BYPASS CHAIN CONTROL
MH16
MIS001B260
15291024
**** JUMPER POSITIONS
OPERATIONAL STATE
1-2
FORCES BYPASS OF CPU1 (JTAG)
2-3
NORMAL OPERATION
R1373 1K 1% 0402
J84
CON0002790
PU_CPU1_SKTOCC_FRBY
XDP_CPU1_SKTOCC_N
FM_CPU1_SKTOCC_LVT3_N
EMPTY
C1139 1UF 10V 0402
INTERPOSER_POP
R1359 100 1% 0402
R1362 100 1% 0402
LOG0000976
GTL2034
U103
VCC
NC
BI<3>
BI<2>
BI<1>
BI<0>
BO<3>
BO<2>
BO<1>
BO<0>
GND<2>
GND<1>
GND<0>
VREF
GTL2034PW,118
XDP_CPU0_PREQ_G_N
PD_XDP_BUF_BI2
XDP_CPU1_PRDY_G_N
PD_XDP_BUF_BI0
XDP_CPU1_PREQ_G_N
TP_XDP_BUF_BO2
XDP_CPU0_PRDY_G_N
TP_XDP_BUF_BO0
R1367 100 1% 0402
R1368 100 1% 0402
R1356 1K 1% 0402
R1357 1K 1% 0402
R1360 1K 1% 0402
R1361 2K 1% 0402
R1365 0 0402
R1366 0 0402
INTERPOSER_DEPOP
JABIL
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CPU JTAG
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Wed Jul 30 14:57:37 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
128OF360

ROOM = PCH_XDP_DEBUG
BOM_COST = DEBUG

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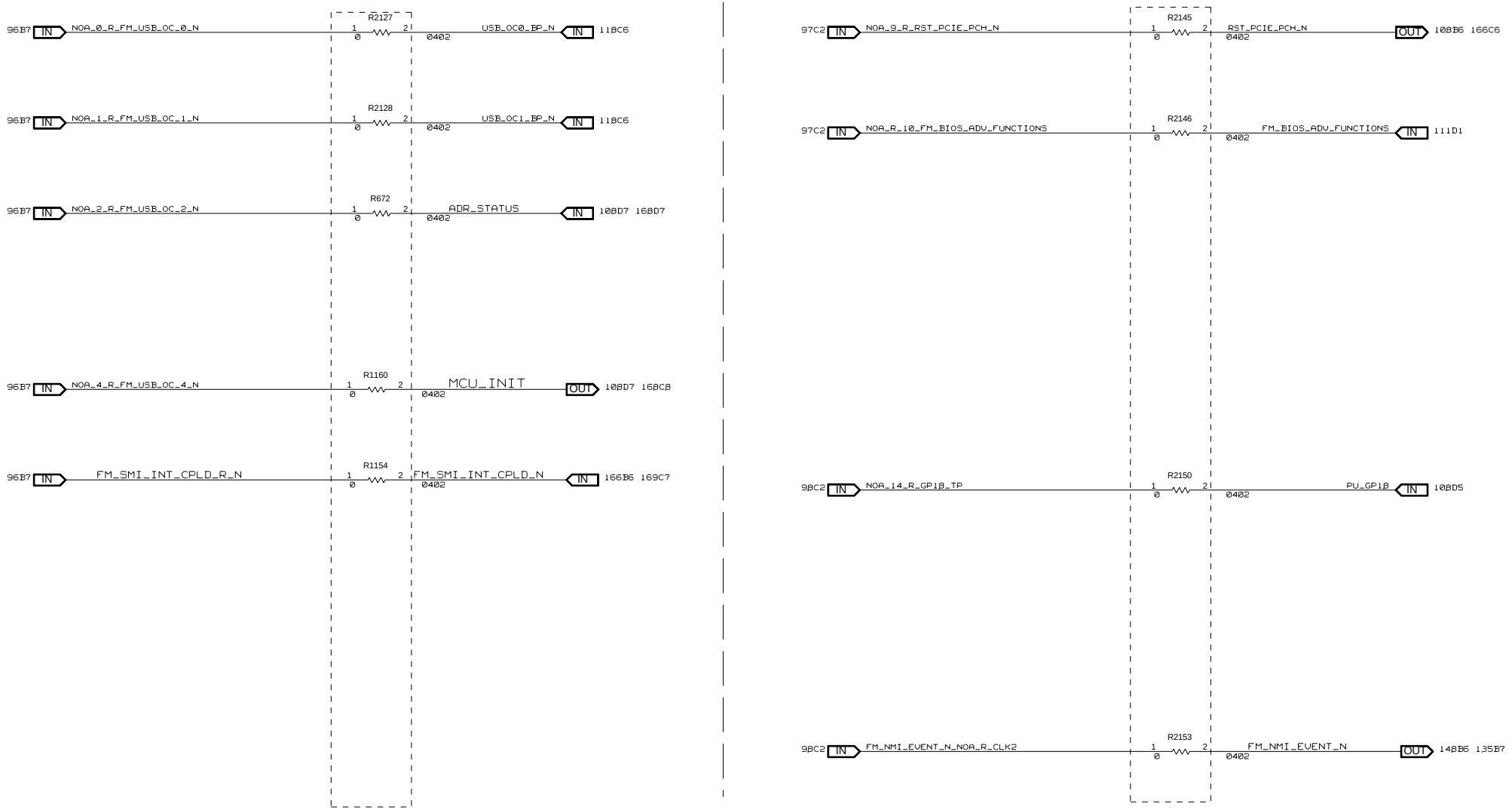
PCH XDP wolfcreek_controller	DATE: Mon Jul 14 13:31:37 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 129OF360	

ROOM = PCH_XDP_DEBUG
BOM_COST = DEBUG



DESIGN NOTE:

REMOVE 0 OHMS FOR NOA OBSERVABILITY.

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PCH NOA wolfcreek_controller	DATE: Fri Aug 08 12:03:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 130OF360	

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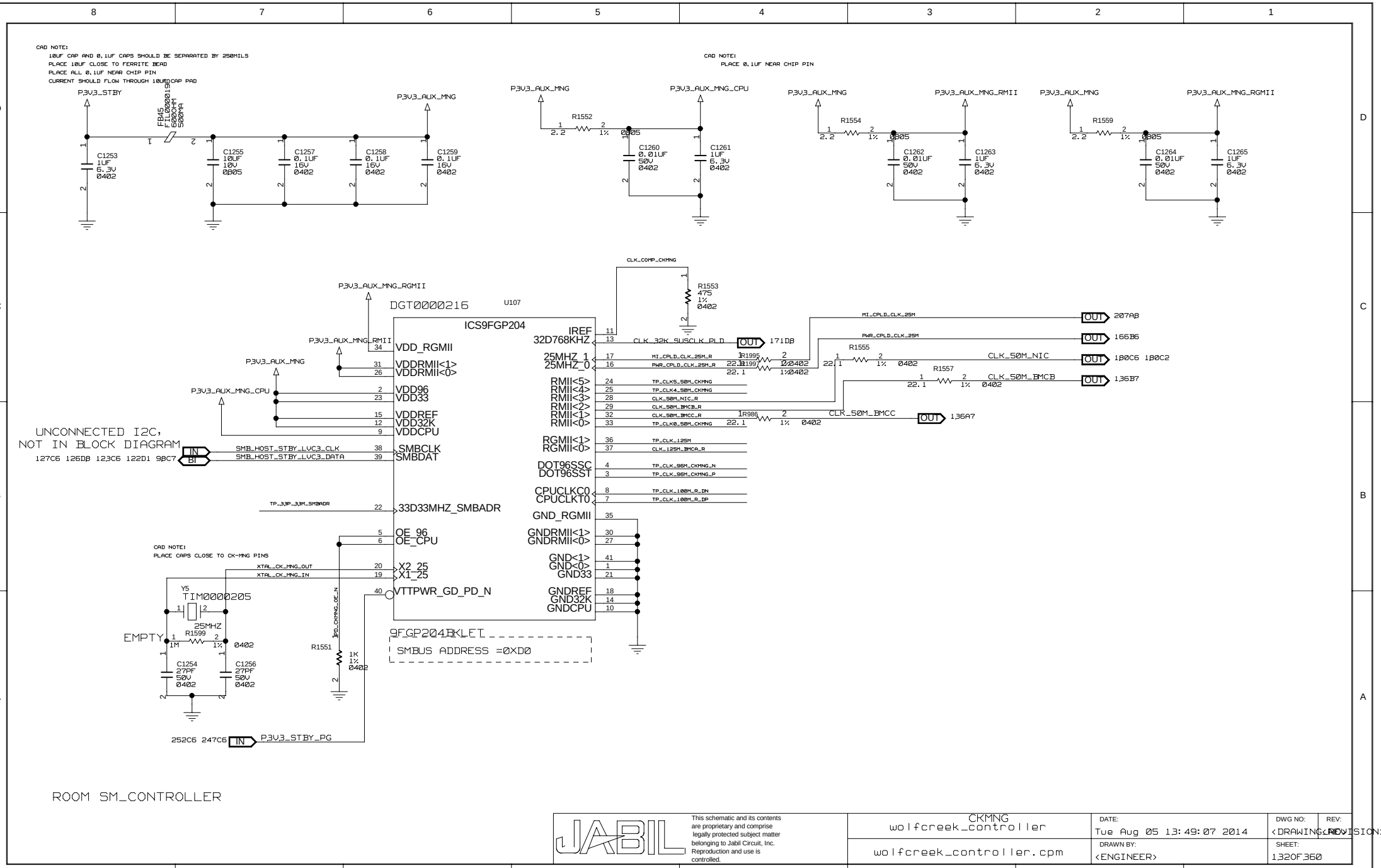
BLANK wolfcreek_controller	DATE: Wed Jul 02 11:40:46 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 131OF360	


CAD NOTE:
10UF CAP AND 0.1UF CAPS SHOULD BE SEPARATED BY 250MILS
PLACE 10UF CLOSE TO FERRITE BEAD
PLACE ALL 0.1UF NEAR CHIP PIN
CURRENT SHOULD FLOW THROUGH 10UF CAP PAD
P3V3_STBY
FB45 FIL0000195 600OHM 500MA
P3V3_AUX_MNG
C1253 1UF 6.3V 0402
C1255 10UF 10V 0805
C1257 0.1UF 16V 0402
C1258 0.1UF 16V 0402
C1259 0.1UF 16V 0402
CAD NOTE:
PLACE 0.1UF NEAR CHIP PIN
P3V3_AUX_MNG_CPU
R1552 2.2 1% 0805
C1260 0.01UF 50V 0402
C1261 1UF 6.3V 0402
P3V3_AUX_MNG_RMII
R1554 2.2 1% 0805
C1262 0.01UF 50V 0402
C1263 1UF 6.3V 0402
P3V3_AUX_MNG_RGMII
R1559 2.2 1% 0805
C1264 0.01UF 50V 0402
C1265 1UF 6.3V 0402
CLK_COMP_CKMNG
R1553 475 1% 0402
U107
DGT0000216
ICS9FGP204
IREF
32D768KHZ
25MHZ_1
25MHZ_0
RMII<5>
RMII<4>
RMII<3>
RMII<2>
RMII<1>
RMII<0>
RGMII<1>
RGMII<0>
DOT96SSC
DOT96SST
CPUCLKC0
CPUCLKT0
GND_RGMII
GNDRMII<1>
GNDRMII<0>
GND<1>
GND<0>
GND33
GNDREF
GND32K
GNDCPU
VDD_RGMII
VDDRMII<1>
VDDRMII<0>
VDD96
VDD33
VDDREF
VDD32K
VDDCPU
SMBCLK
SMBDAT
33D33MHZ_SMBADR
OE_96
OE_CPU
X2_25
X1_25
VTTPWR_GD_PD_N
CLK_32K_SUSCLK_PLD
OUT 171DB
MI_CPLD_CLK_25M
OUT 207AB
PWR_CPLD_CLK_25M
OUT 166B6
R1555
CLK_50M_NIC
OUT 1B0C6 1B0C2
R1557
CLK_50M_BMCB
OUT 136B7
CLK_50M_BMCC
OUT 136A7
R1995 22.1 1% 0402
R1997 22.1 1% 0402
R1986 22.1 1% 0402
TP_CLK5_50M_CKMNG
TP_CLK4_50M_CKMNG
CLK_50M_NIC_R
CLK_50M_BMCB_R
CLK_50M_BMCC_R
TP_CLK0_50M_CKMNG
TP_CLK_125M
CLK_125M_BMCA_R
TP_CLK_96M_CKMNG_N
TP_CLK_96M_CKMNG_P
TP_CLK_100M_R_DN
TP_CLK_100M_R_DP
TP_33P_33M_SMBADR
UNCONNECTED I2C,
NOT IN BLOCK DIAGRAM
127C6 126DB 123C6 122D1 9BC7
IN SMB_HOST_STBY_LVC3_CLK
BI SMB_HOST_STBY_LVC3_DATA
CAD NOTE:
PLACE CAPS CLOSE TO CK-MNG PINS
XTAL_CK_MNG_OUT
XTAL_CK_MNG_IN
Y5
TIM0000205
25MHZ
EMPTY
R1599 1M 1% 0402
C1254 27PF 50V 0402
C1256 27PF 50V 0402
PD_CKMNG_OE_N
R1551 1K 1% 0402
252C6 247C6 IN P3V3_STBY_PG
9FGP204BKLFT
SMBUS ADDRESS =0XD0
ROOM SM_CONTROLLER
JABIL
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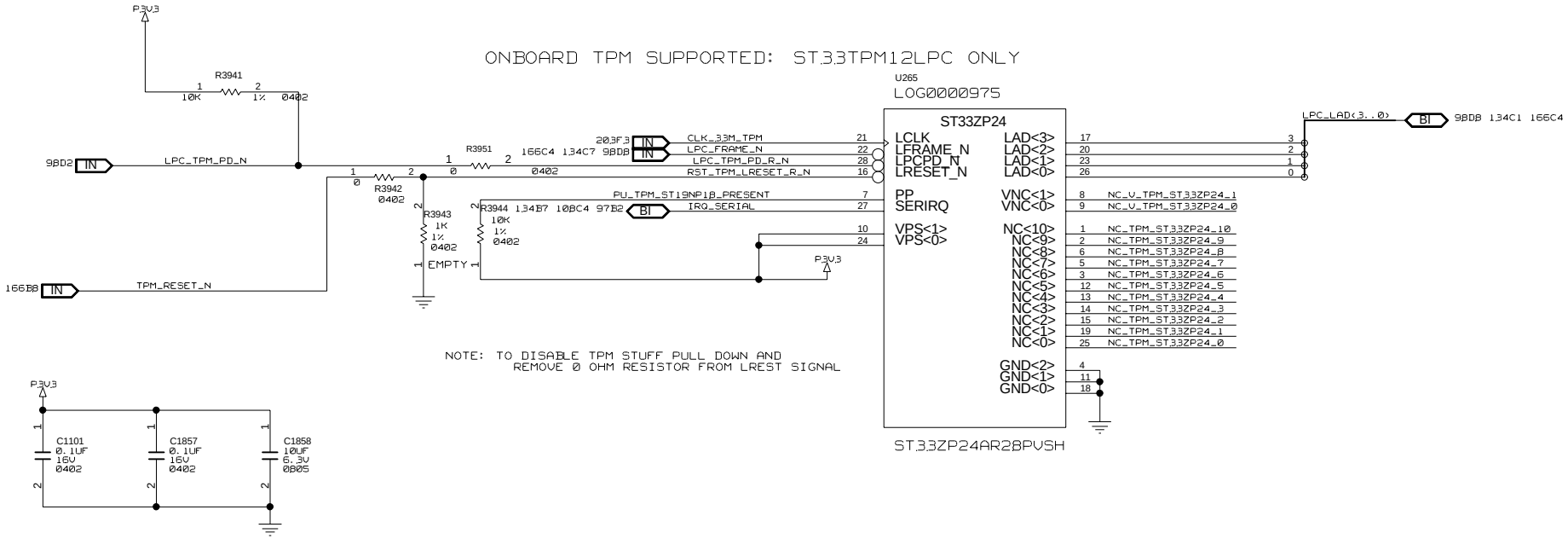
CKMNG
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Tue Aug 05 13:49:07 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 130 OF 360



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TPM MODULE CONNECTOR

wolfcreek_controller

wolfcreek_controller.cpm

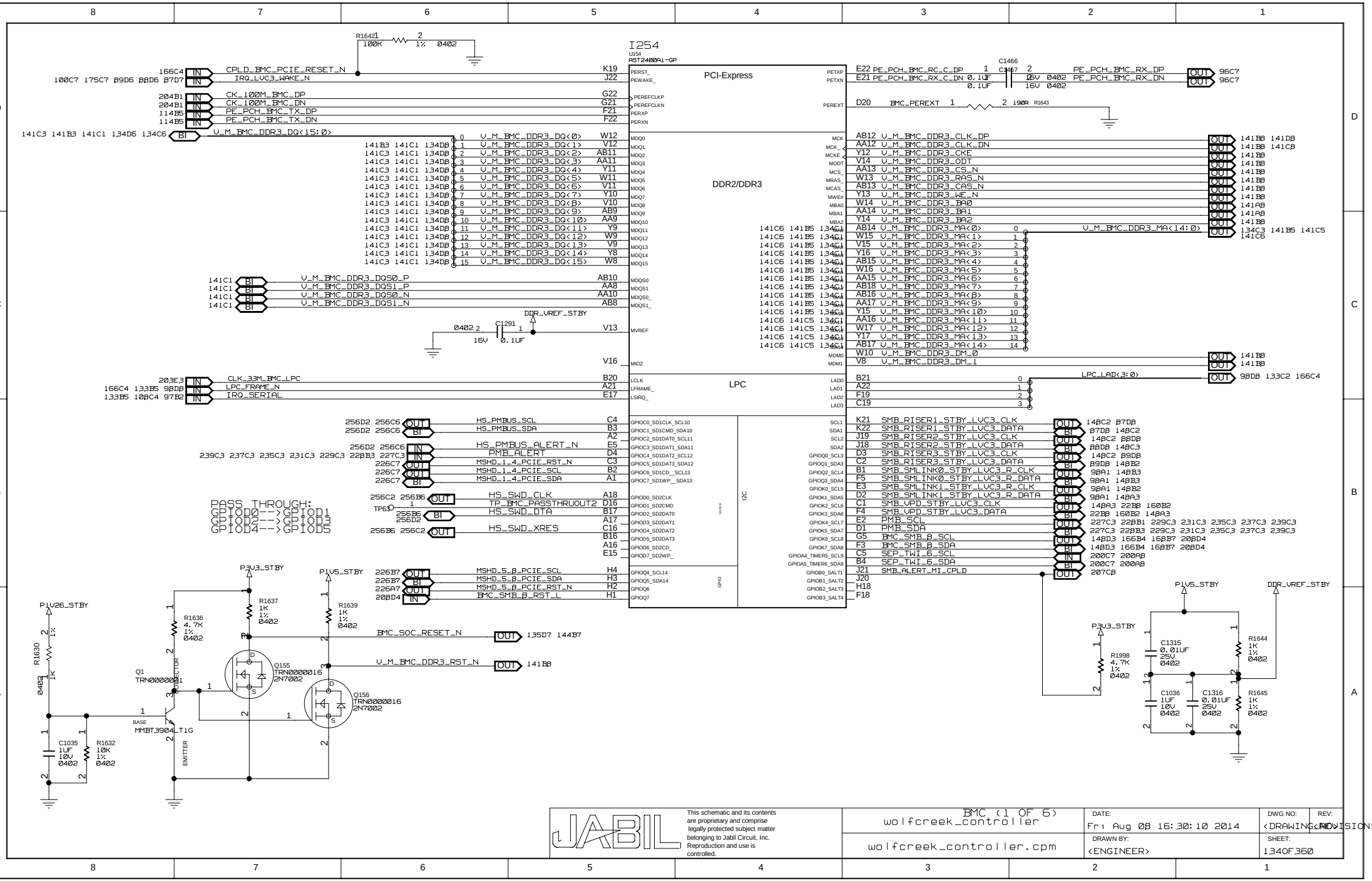
DATE: Thu Aug 07 11:33:20 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 133OF360



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BMC (1 OF 6) wolfcreek_controller	DATE: Fri Aug 08 16:30:10 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 134OF360	

ROOM=BMC

P3V3_STBY

U166 48MHZ

C1317 0.1UF 16V 0402

20,3E,3 IN CLK_48M_USB_BMC — R1647 EMPTY 0 0402 — 2CLK_48M_USB_BMC_AB22

3 OSC_48M_R — R1646 22 1% 0402 — 1,35D7 CLK_48M_USB_BMC_AB22

144B7 1,34A5 IN BMC_SOC_RESET_N

R1648 10K 1% 0402 — BMC_ENTEST1

162B5 IN FAN_CPU_TACH0

162B2 IN FAN_CPU_TACH1

161B1 IN A_P12V_AUX_SCALED 2.0

161C1 IN A_P12V_SCALED 2.0

161D1 IN A_P3V3_AUX_SCALED 2.0

161A3 IN A_P1V0_PVL_SENSOR 1.0

161B3 IN A_P1V05_STBY_PCH_SENSOR 1.05

161C3 IN A_P1V05_PCH_SENSOR 1.05

161D3 IN A_P1V5_PCH_SENSOR 1.5

161A5 IN A_PVCCIO_SENSOR 1.0

10BC7 IN IRQ_SML1_PMBUS_ALERT_N

79C4 7BD3 IN FM_CPU_CATERR_LVT3_N

1,36BB 14BC6 77A1 IN FM_CPU_ERR2_CO_N

1,36C2 140D2 9BC2 IN FM_BIOS_POST_CMPLT_N

1,36C2 16,3C3 14BC6 140D2 IN IRQ_SML0_ALERT_N

16BC7 169C7 140C2 9BD2 IN FM_SMI_ACTIVE_N — R23031 0 0402 — FM_SMI_R_ACTIVE_N

14BB6 1,30A1 IN FM_NMI_EVENT_N

161A1 IN A_P3V_BAT_SENSOR

144B7 IN JTAG_BMC_NTRST_N

144B7 IN JTAG_BMC_TDI

144B7 IN JTAG_BMC_TMS

144B7 IN JTAG_BMC_TCK

144B7 IN JTAG_BMC_RTCK

144B7 OUT JTAG_BMC_TDO

140C2 1,39B4 1,36C2 IN FM_FORCE_BMC_UPDATE_N

14,3B2 OUT BMC_WDTRST1

BMC_WDTRST2

9BB2 16BDB IN AC_GOOD_LATCHED_N

256D2 256B4 OUT COLD_RESTART

I26B

U154 AST2400A1-GP

MISC: CLKIN AB22; SRST_ W20; ENTEST E4

FAN: GPIOO0_TACH0_VPIG8 V6; GPIOO1_TACH1_VPIG9 Y5; GPIOO2_TACH2_VPIR0 AA4; GPIOO3_TACH3_VPIR1 AB3; GPIOO4_TACH4_VPIR2 W6; GPIOO5_TACH5_VPIR3 AA5; GPIOO6_TACH6_VPIR4 AB4; GPIOO7_TACH7_VPIR5 V7; GPIOP0_TACH8_VPIR6 Y6; GPIOP1_TACH9_VPIR7 AB5; GPIOP2_TACH10_VPIR8 W7; GPIOP3_TACH11_VPIR9 AA6; GPIOP4_TACH12 AB6; GPIOP5_TACH13 Y7; GPIOP6_TACH14_BMCINT AA7; GPIOP7_TACH15_FLACK AB7

ADC: ADC0_GPIW0 L5; ADC1_GPIW1 L4; ADC2_GPIW2 L3; ADC3_GPIW3 L2; ADC4_GPIW4 L1; ADC5_GPIW5 M5; ADC6_GPIW6 M4; ADC7_GPIW7 M3; ADC8_GPIX0 M2; ADC9_GPIX1 M1; ADC10_GPIX2 N5; ADC11_GPIX3 N4; ADC12_GPIX4 N3; ADC13_GPIX5 N2; ADC14_GPIX6 N1; ADC15_GPIX7 P5

JTAG: NTRST E1; TDI_BDM F1; TMS G2; TCK F2; RTCK G4; TDO G3

GPIO: GPIOA0_MAC1LINK D6; GPIOA1_MAC2LINK B5; GPIOA2_TIMER3 A4; GPIOA3_TIMER4 E6; GPIOG4_WDTRST1_OSCCLK B13; GPIOG5_WDTRST2_USBCKI Y21; GPIOG6_FLBUSY_ AA22; GPIOG7_FLWP_ U18

VGA: DACB R4; DACG R3; DACR R2; VGAHS_GPIOJ4 T4; VGAVS_GPIOJ5 U2; DDCCLK_GPIOJ6 T2; DDCDAT_GPIOJ7 T1

FAN: GPION0_PWM0_VPIG0 W4; GPION1_PWM1_VPIG1 Y3; GPION2_PWM2_VPIG2 AA2; GPION3_PWM3_VPIG3 AB1; GPION4_PWM4_VPIG4 W5; GPION5_PWM5_VPIG5 Y4; GPION6_PWM6_VPIG6 AA3; GPION7_PWM7_VPIG7 AB2

USB: USB2AV33 W18; USB2VRES AA20; USB2AVSS Y19; USB2_DP/USB2_HDP AB21; USB2_DN/USB2_HDN AB20; USB11_HDP J1; USB11_HDN J2; USB11_DP/USB11_HDP2 K4; USB11_DN/USB11_HDN2 K3

PECI: PECIVDD V19; PECI AA21

GPIO: GPIOJ0_SGPMCK J5; GPIOJ1_SGPMLD J4; GPIOJ2_SGPMO K5; GPIOJ3_SGPMI J3; GPIOG0_SGPSCK A14; GPIOG1_SGPSLD E13; GPIOG2_SGPSI0 D13; GPIOG3_SGPSI1 C13; GPIOA4_LPCRST_ E19; GPIOB5_LPCPD#_LPCSMI_ H19; GPIOB6_LPCPME_ H20; GPIOB7_EXTRST_SPICS1_ E18; GPIOY0_SIOS3_ C21; GPIOY1_SIOS5_ F20; GPIOY2_SIOPWREQ_ G20; GPIOY3_SIOONCTRL_ K20

V_BMC_GFX_BLU 1,37C,3

V_BMC_GFX_GRN 1,37C7

V_BMC_GFX_RED 1,37C,3

V_BMC_GFX_HSYN 1,37B7

V_BMC_GFX_VSYN 1,37B7

V_BMC_DDC_SCL 146C6

V_BMC_DDC_SDA 146C6

PLACE THESE RESISTORS CLOSE TO BMC

R1595 150 1% 0402

R1596 150 1% 0402

R1607 150 1% 0402

FAN_CPU0_PWM 162BB

FAN_CPU1_PWM 162B4

PVCCIO

C1037 1UF 10V 0402

CLOSED TO V19 PIN

P3V3_STBY

FB23 FIL0000023 330OHM 1800MA

BMC_USB2AV33

BMC_USB2VRES

8.2KR1649 0402 1%

C1318 100PF 50V 0402

C1319 4.7UF 16V 0805

USB_00_R_BMC_DP BI 119D3

USB_00_R_BMC_DN BI 119D3

USB11_BMC_DP_TP

USB11_BMC_DN_TP

0402 1.5K R1626 1%

PECI_BMC BI 15BC7 1,35A3

SPI_FLASH_MUX_SEL OUT 121DB

FM_CPU0_SKTOCC_BMC_LVT3_N IN 165B5

FM_CPU1_SKTOCC_BMC_LVT3_N IN 165A5

FM_CPU0_FIVR_FAULT_LVT3_N IN B6C2

FM_CPU1_FIVR_FAULT_LVT3_N IN B6A2

FM_CPU0_BDX_PRSNT_LVT3_N IN 23C2 B5C2 166C6 24,3C7

FM_CPU1_BDX_PRSNT_LVT3_N IN 37C2 B5C2 166C6

CPLD_BMC_RESET_N IN 14BC6 16BD1

FM_BMC_PCH_SMI_LPC_N OUT 10BC4 95C7

FM_SLP53_N IN 9BD2 16BD7

FM_SLP55_N IN 9BD2 16BD7

FM_BMC_PCH_SCI_LPC_N OUT 10BD7 9BB2

PSU_ON_R_N — R1640 0 0402 — PSU_ON_N

R3957 10K 1% 0402 — OUT 166C4 20BB1

15BC7 1,35B2 PECI_BMC — R1091 10K 1% 0402

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BMC (2 OF 6)

wolfcreek_controller

wolfcreek_controller.cpm

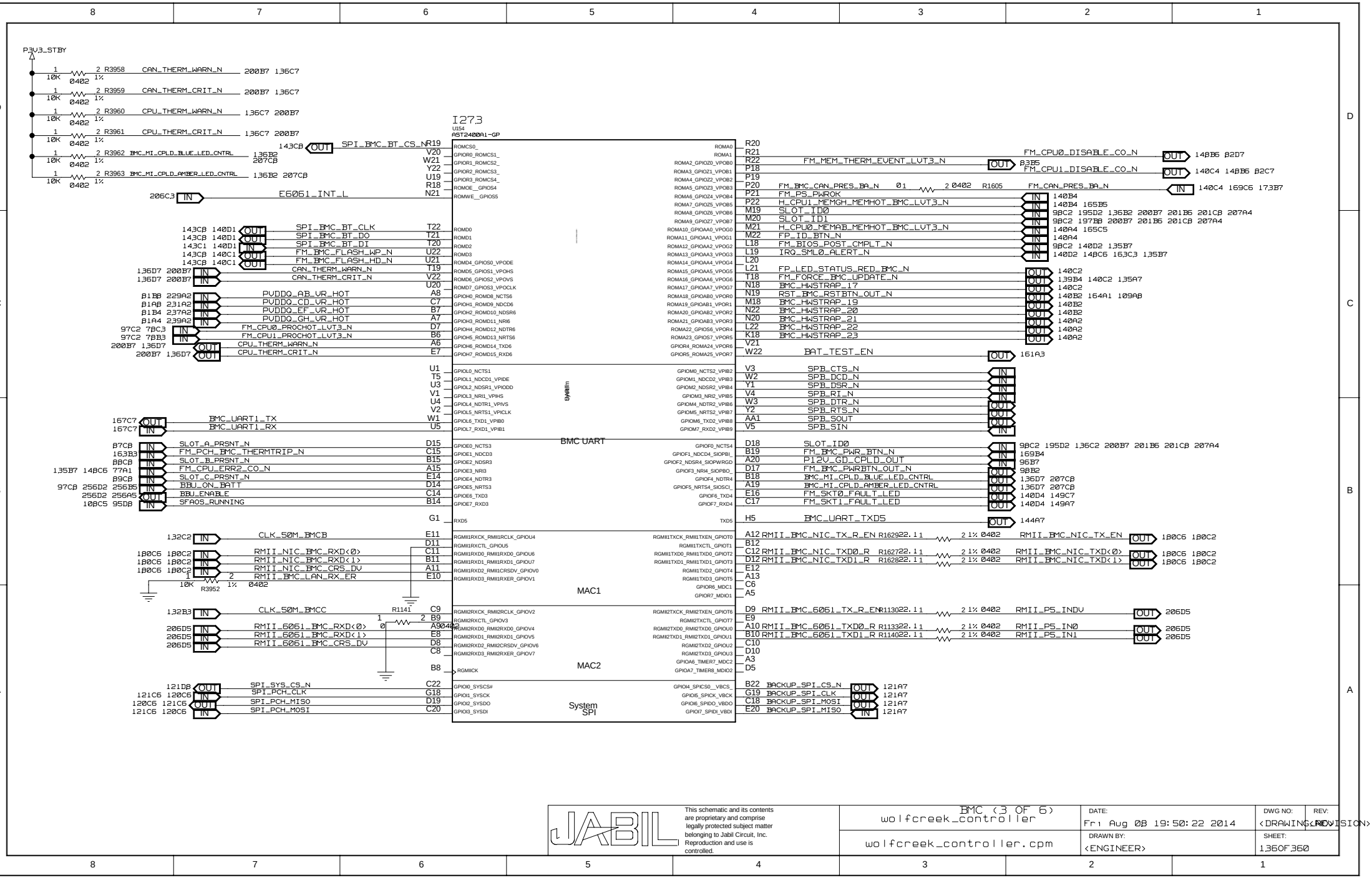
DATE: Fri Aug 08 17:27:14 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING_NO>

REV: <REVISION>

SHEET: 1,350F,360


P3V3_STBY
R3958 CAN_THERM_WARN_N 200B7 136C7
R3959 CAN_THERM_CRIT_N 200B7 136C7
R3960 CPU_THERM_WARN_N 136C7 200B7
R3961 CPU_THERM_CRIT_N 136C7 200B7
R3962 BMC_MI_CPLD_BLUE_LED_CNTRL 136B2 207CB
R3963 BMC_MI_CPLD_AMBER_LED_CNTRL 136B2 207CB
10K 0402 1%
I273
U154
AST2400A1-GP
SPI_BMC_BT_CS_N
E6061_INT_L
SPI_BMC_BT_CLK
SPI_BMC_BT_DO
SPI_BMC_BT_DI
FM_BMC_FLASH_WP_N
FM_BMC_FLASH_HD_N
CAN_THERM_WARN_N
CAN_THERM_CRIT_N
PVDDQ_AB_VR_HOT
PVDDQ_CD_VR_HOT
PVDDQ_EF_VR_HOT
PVDDQ_GH_VR_HOT
FM_CPU0_PROCHOT_LVT3_N
FM_CPU1_PROCHOT_LVT3_N
CPU_THERM_WARN_N
CPU_THERM_CRIT_N
BMC_UART1_TX
BMC_UART1_RX
SLOT_A_PRSNT_N
FM_PCH_BMC_THERMTRIP_N
SLOT_B_PRSNT_N
FM_CPU_ERR2_CO_N
SLOT_C_PRSNT_N
BBU_ON_BATT
BBU_ENABLE
SFAOS_RUNNING
CLK_50M_BMCB
RMII_NIC_BMC_RXD<0>
RMII_NIC_BMC_RXD<1>
RMII_NIC_BMC_CRS_DV
RMII_BMC_LAN_RX_ER
R3952
CLK_50M_BMCC
R1141
RMII_6061_BMC_RXD<0>
RMII_6061_BMC_RXD<1>
RMII_6061_BMC_CRS_DV
SPI_SYS_CS_N
SPI_PCH_CLK
SPI_PCH_MISO
SPI_PCH_MOSI
FM_CPU0_DISABLE_CO_N
FM_MEM_THERM_EVENT_LVT3_N
FM_CPU1_DISABLE_CO_N
FM_BMC_CAN_PRES_BA_N
R1605
FM_CAN_PRES_BA_N
FM_PS_PWROK
H_CPU1_MEMIGH_MEMHOT_BMC_LVT3_N
SLOT_ID0
SLOT_ID1
H_CPU0_MEMAB_MEMHOT_BMC_LVT3_N
FP_ID_BTN_N
FM_BIOS_POST_CMPLT_N
IRQ_SML0_ALERT_N
FP_LED_STATUS_RED_BMC_N
FM_FORCE_BMC_UPDATE_N
BMC_HWSTRAP_17
RST_BMC_RSTBTN_OUT_N
BMC_HWSTRAP_19
BMC_HWSTRAP_20
BMC_HWSTRAP_21
BMC_HWSTRAP_22
BMC_HWSTRAP_23
BAT_TEST_EN
SPB_CTS_N
SPB_DCD_N
SPB_DSR_N
SPB_RI_N
SPB_DTR_N
SPB_RTS_N
SPB_SOUT
SPB_SIN
SLOT_ID0
FM_BMC_PWR_BTN_N
P12V_GD_CPLD_OUT
FM_BMC_PWRBTN_OUT_N
BMC_MI_CPLD_BLUE_LED_CNTRL
BMC_MI_CPLD_AMBER_LED_CNTRL
FM_SKT0_FAULT_LED
FM_SKT1_FAULT_LED
BMC_UART_TXD5
RMII_BMC_NIC_TX_R_EN
RMII_BMC_NIC_TXD0_R
RMII_BMC_NIC_TXD1_R
RMII_BMC_NIC_TX_EN
RMII_BMC_NIC_TXD<0>
RMII_BMC_NIC_TXD<1>
RMII_BMC_6061_TX_R_EN
RMII_BMC_6061_TXD0_R
RMII_BMC_6061_TXD1_R
RMII_P5_INDV
RMII_P5_IN0
RMII_P5_IN1
BACKUP_SPI_CS_N
BACKUP_SPI_CLK
BACKUP_SPI_MOSI
BACKUP_SPI_MISO
System SPI
MAC2
MAC1
BMC UART
SYSTEM
JABIL
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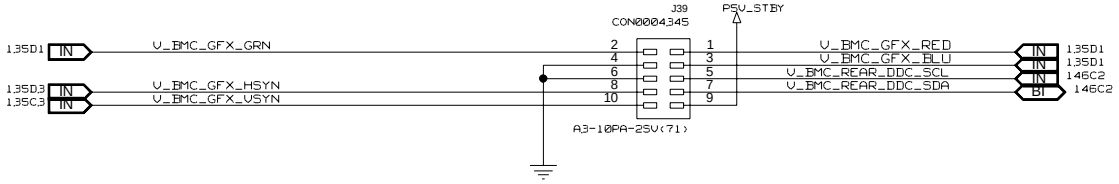
BMC (3 OF 6)
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Fri Aug 08 19:50:22 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
136OF360

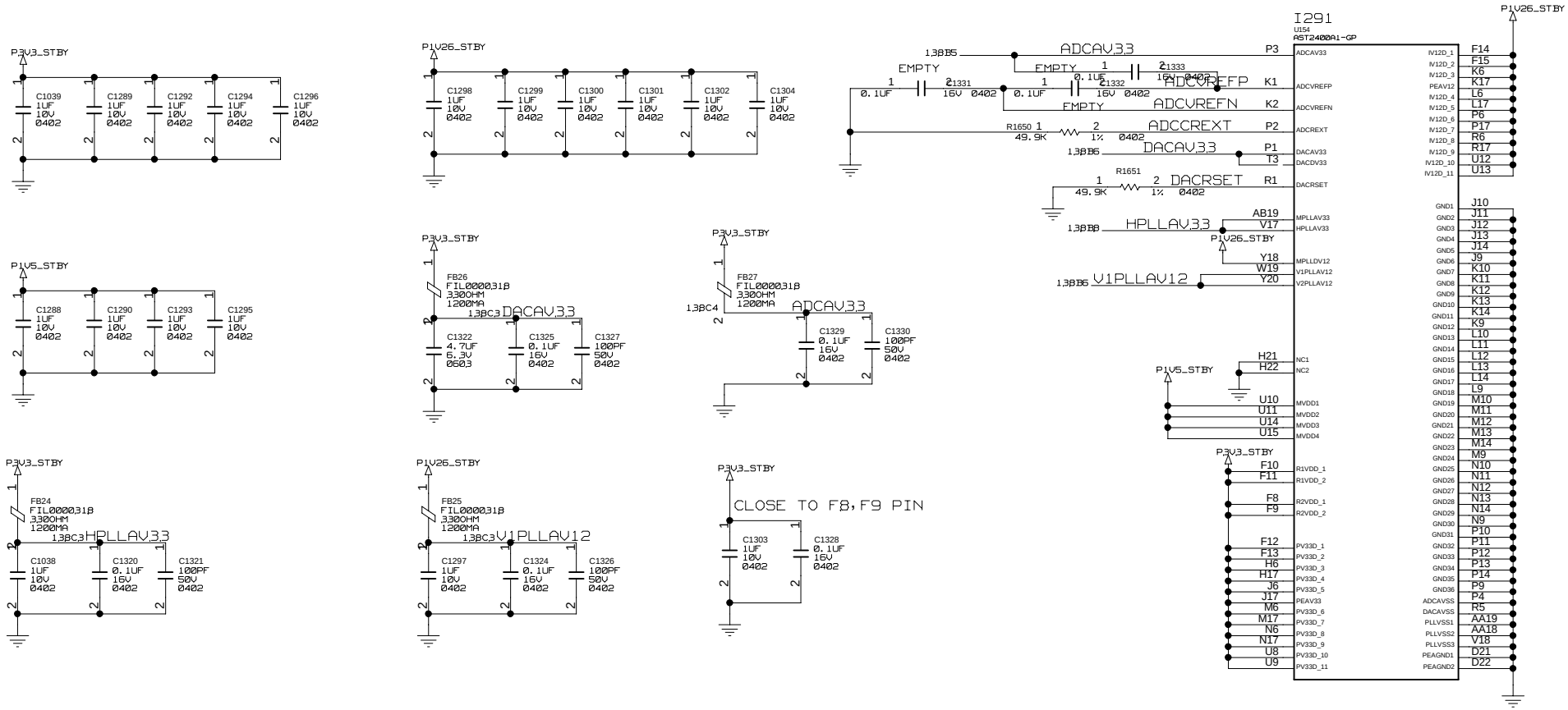
ROOM=BMC



JABIL	This schematic and its contents are proprietary and comprise legally protected subject matter belonging to Jabil Circuit, Inc. Reproduction and use is controlled.	BMC VGA (4 OF 6) wolfcreek_controller	DATE: Sun Aug 03 10:48:17 2014
		wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>

DWG NO:	REV:
<DRAWING>	<REVISION>
SHEET: 137OF360	

ROOM=BMC



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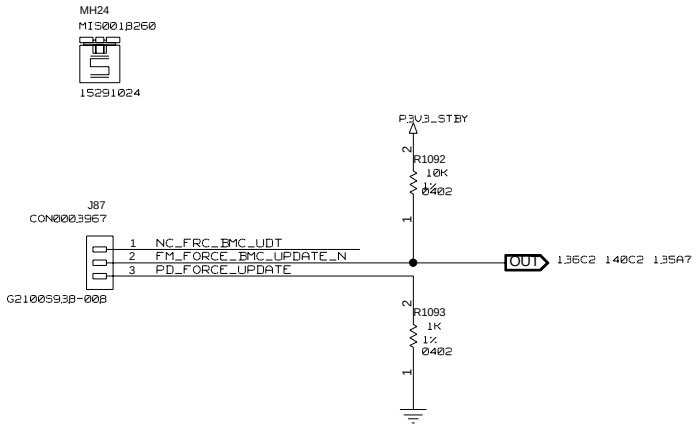
BMC (5 OF 6) wolfcreek_controller	DATE: Sat Aug 02 19:30:55 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 130 OF 360	

FORCE BMC UPDATE JUMPER		
JUMPER POSITION	SIGNAL STATE	OPERATION MODE
1-2<DEFAULT>	PULLED HIGH	NORMAL
2-3	PULLED DOWN	UPDATE



BMC CONFIGURATION

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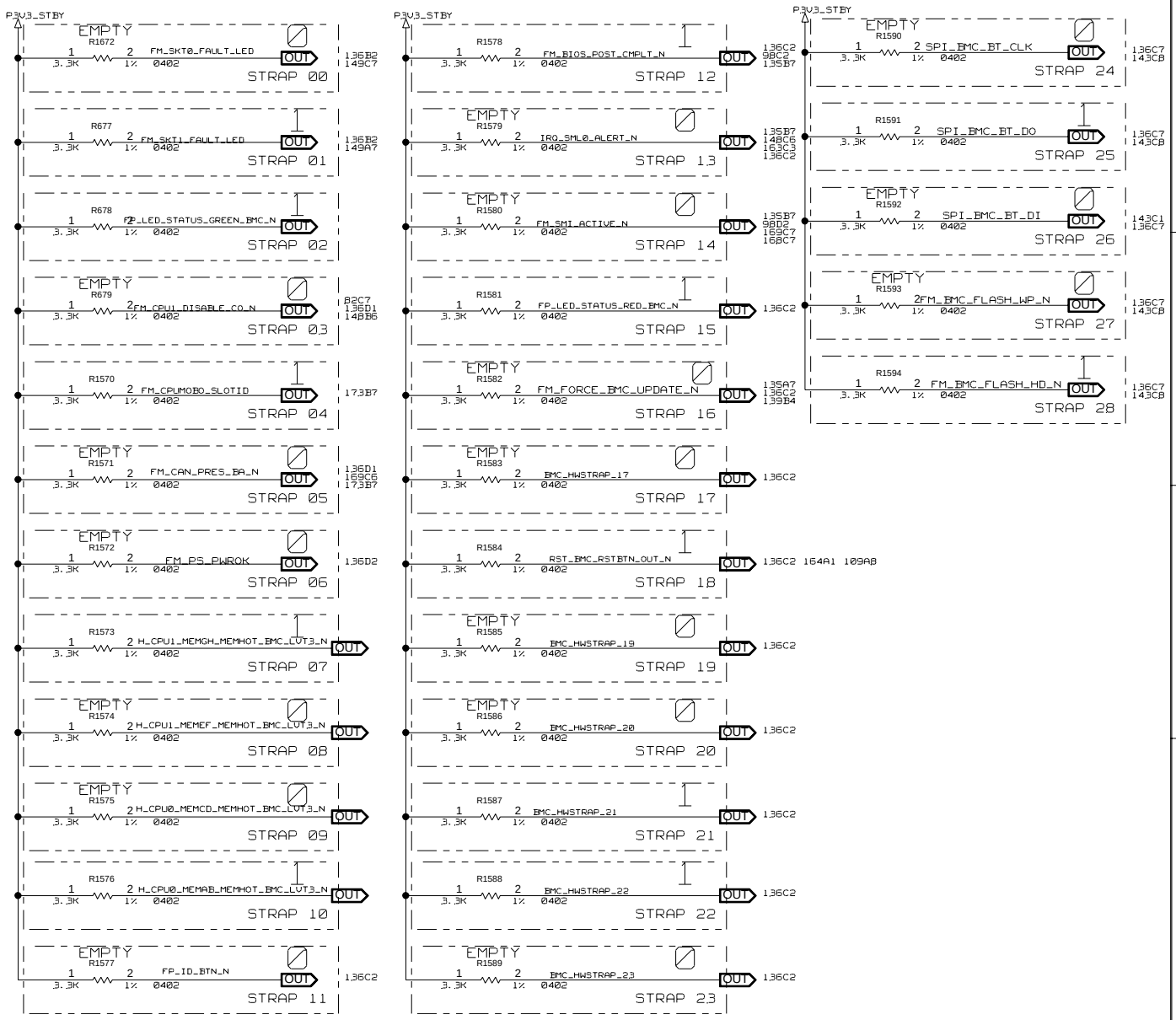
BMC <6 OF 6> wolfcreek_controller	DATE: Wed Jul 30 14:59:24 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 139OF360	

BMC STRAP OPTIONS TABLE

STRAP NUM	BALL NUM	BALL NAME	STRAP NAME / FUNCTIONAL DESCRIPTION
28 27	U21 U22	ROMD4 ROMD3	DRAM CONFIGURATON SETTING 00:64MB 01:128MB 10:256MB 11:512MB
26 25 24	T20 T21 T22	ROMD2 ROMD1 ROMD0	DRAM CONFIGURATON SETTING 000:DDR3 SDRAM WITH CL=5, CWL=5 010:DDR3 SDRAM WITH CL=6, CWL=5 DEFAULT 100:DDR3 SDRAM WITH CL=7, CWL=6 110:DDR3 SDRAM WITH CL=8, CWL=6
22 21	L22 N20	ROMA22 ROMA21	ENABLE GPIOE PASS-THROUGH MODE 0:DISABLE ENABLE GPIOD PASS-THROUGH MODE 1:ENABLE
20	N22	ROMA20	DISABLE LPC TO DECODE SUPER IO 0X2E/0X4E ADDRESS 0:ENABLE ADDRESS DECODING 1:DISABLE ADDRESS DECODING
19	M18	ROMA19	DISABLE ACPI FUNCTION 0:ENABLE ACPI 1:DISABLE ACPI
23 18	K18 N19	ROMA23 ROMA18	CLOCK SOURCE SELECTION 01:CLKIN=48MHZ 10:CLKIN=25MHZ, USBCKI=24MHZ 11:CLKIN=25MHZ, USBCKI=48MHZ
17	N18	ROMA17	ENABLE BMC 2ND BOOT WATCHDOG TIMER 0: DISABLE 1: ENABLE BMC 2ND WATCHDOG TIMER START COUNTING AT POWER UP. THE WATCH DOG WAS LOCATED AT WDT2. AFTER WATCHDOG TIMEOUT(1 MINUTE), IT WILL RESET BMC AND RESTART BOOTING FROM THE 2ND BOOT FLASH AT CS1# CS1# MUST BE THE SAME FLASH TYPE AS CS0# AND COULD BE CS1# MUST BE THE SAME FLASH TYPE AS CS0# AND COULD BE
16	T18	ROMA16	SUPERIO CONFIGURATION ADDRESS SELECTION 0: DECODE 0X2E 1: DECODE 0X4E
15	L21	ROMA15	VGA CLASS CODE SELECTION 0:SELECT THE CLASS CODE FOR VIDEO DEVICE 1:SELECT THE CLASS CODE FOR VGA DEVICE
14	L20	ROMA14	ENABLE LPC DEDICATED RESET PIN FUNCTION 0:LPC RESET IS SHARED WITH PCI RESET PIN 1:LPC RESET IS SHARED WITH GPIOB4
13 12	L19 L18	ROMA13 ROMA12	SPI MODE SELECTION 00:DISABLE SPI 01:ENABLE SPI MASTER 10:ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE 11:ENABLE SPI BYPASS
11 10	M22 M21	ROMA11 ROMA10	CPU/AHB CLOCK FREQUENCY RATIO SELECTION 00:CPU:AHB=1:1 01:CPU:AHB=2:1 10:CPU:AHB=4:1 11:CPU:AHB=3:1
09 08	M20 M19	ROMA9 ROMA8	H-PLL DEFAULT CLOCK FREQUENCY SELECTION 00:384MHZ 01:360MHZ 10:336MHZ 11:408MHZ
07 06	P22 P21	ROMA7 ROMA6	DEFINE MAC#2, MAC#1 INTERFACE 0: RMII/NCSI 1: RGMII
05	P20	ROMA5	ENABLE VGA BIOS ROM 0: NO VGA BIOS ROM (FOR ON BOARD APPLICATION) 1: ENABLE VGA BIOS ROM (FOR ADD-ON APPLICATION)
04	P19	ROMA4	SPI TYPE FLASH: BOOT ADDRESS MODE SELECTION 0: BOOT WITH 24BITS ADDRESS MODE 1: BOOT WITH 32BITS ADDRESS MODE
03 02	P18 R22	ROMA3 ROMA2	VGA MEMORY SIZE SELECTION 00: SELECT 8 MB VGA MEMORY 00: SELECT 8 MB VGA MEMORY
01 00	R21 R20	ROMA1 ROMA0	ARM CPU BOOT CODE SELECTION 00: BOOT FROM NOR FLASH MEMORY 01: BOOT FROM NAND FLASH MEMORY 10: BOOT FROM SPI FLASH MEMORY 11: DISABLE CPU OPERATION



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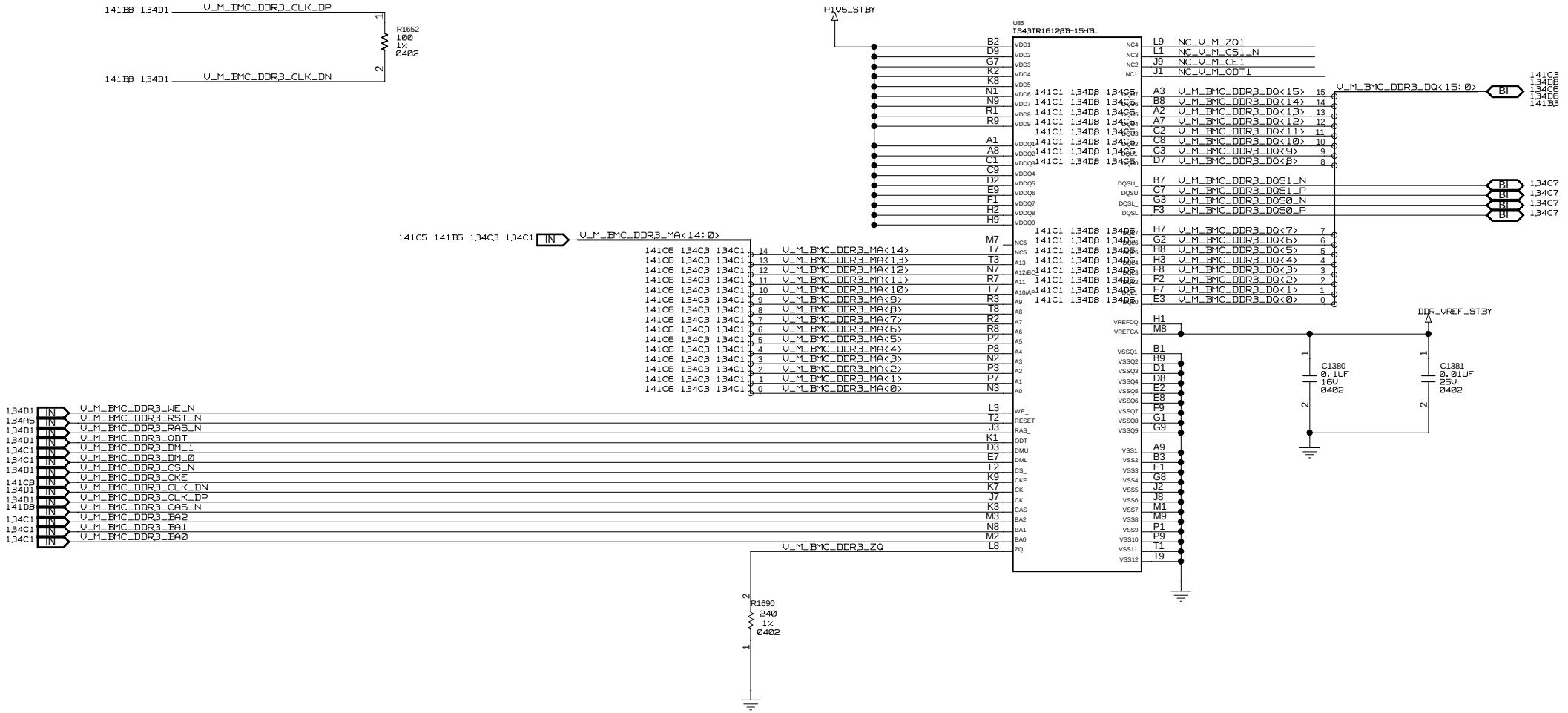
BMC STRAPS wolfcreek_controller	DATE: Wed Jul 30 14:59:25 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 140OF360	

ROOM=BMC_MEMORY



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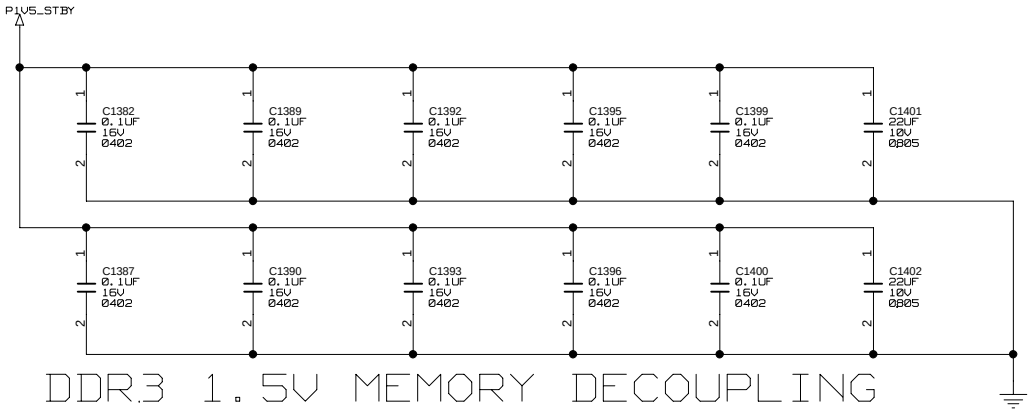
BMC DDR3 MEMORY wolfcreek_controller	PAGE: 157 OF 2) Wed Jul 30 14:59:04 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 141OF360	

ROOM=BMC_MEMORY



DDR3 1.5V MEMORY DECOUPLING

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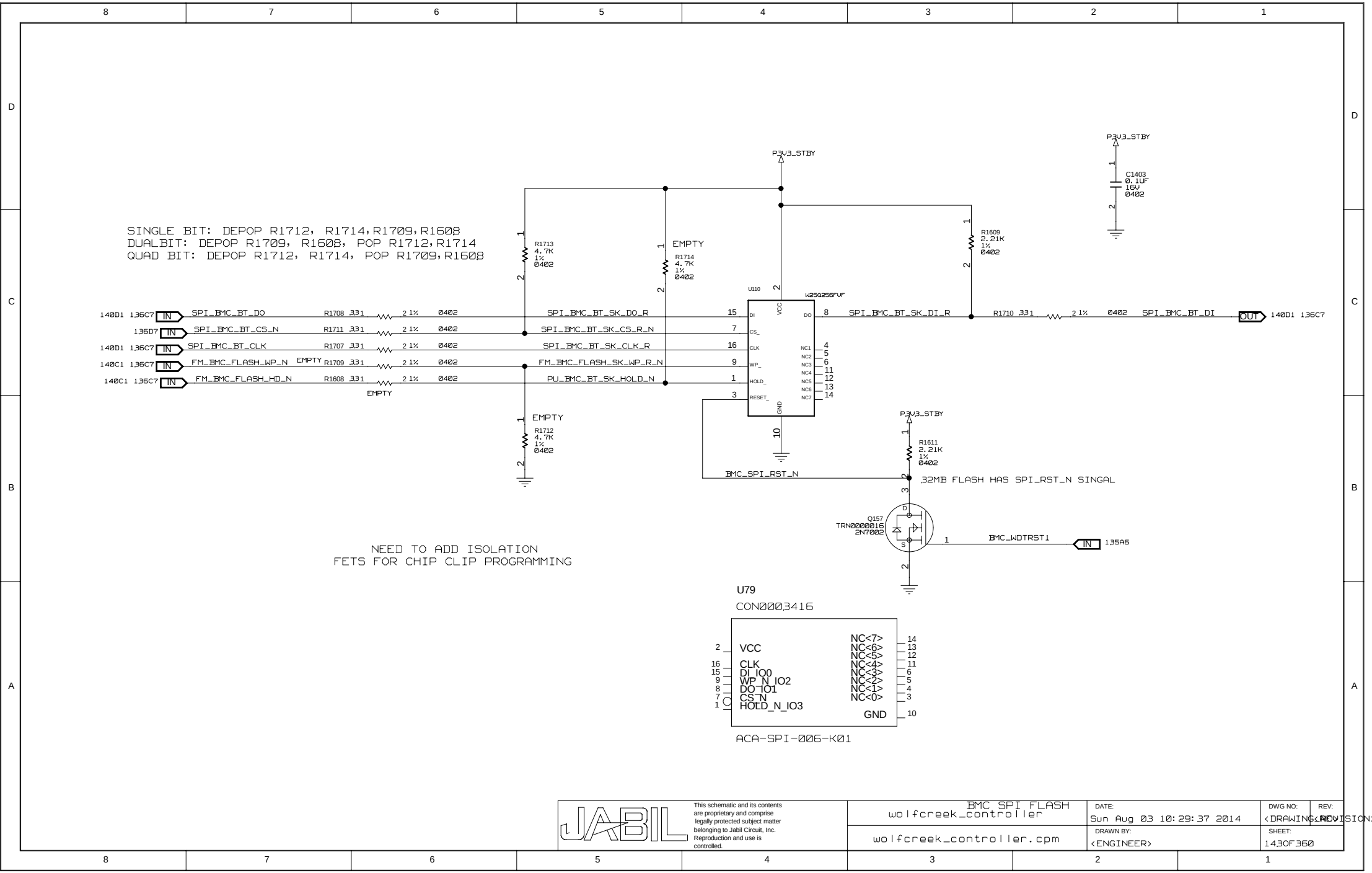
BMC DDR3 MEMORY (2 OF 2)	PAGE:	DWG NO:	REV:
wolfcreek_controller	Wed Jul 30 14:59:04 2014	<DRAWING NO>	<REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 142OF360	



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BMC SPI FLASH
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Sun Aug 03 10:29:37 2014

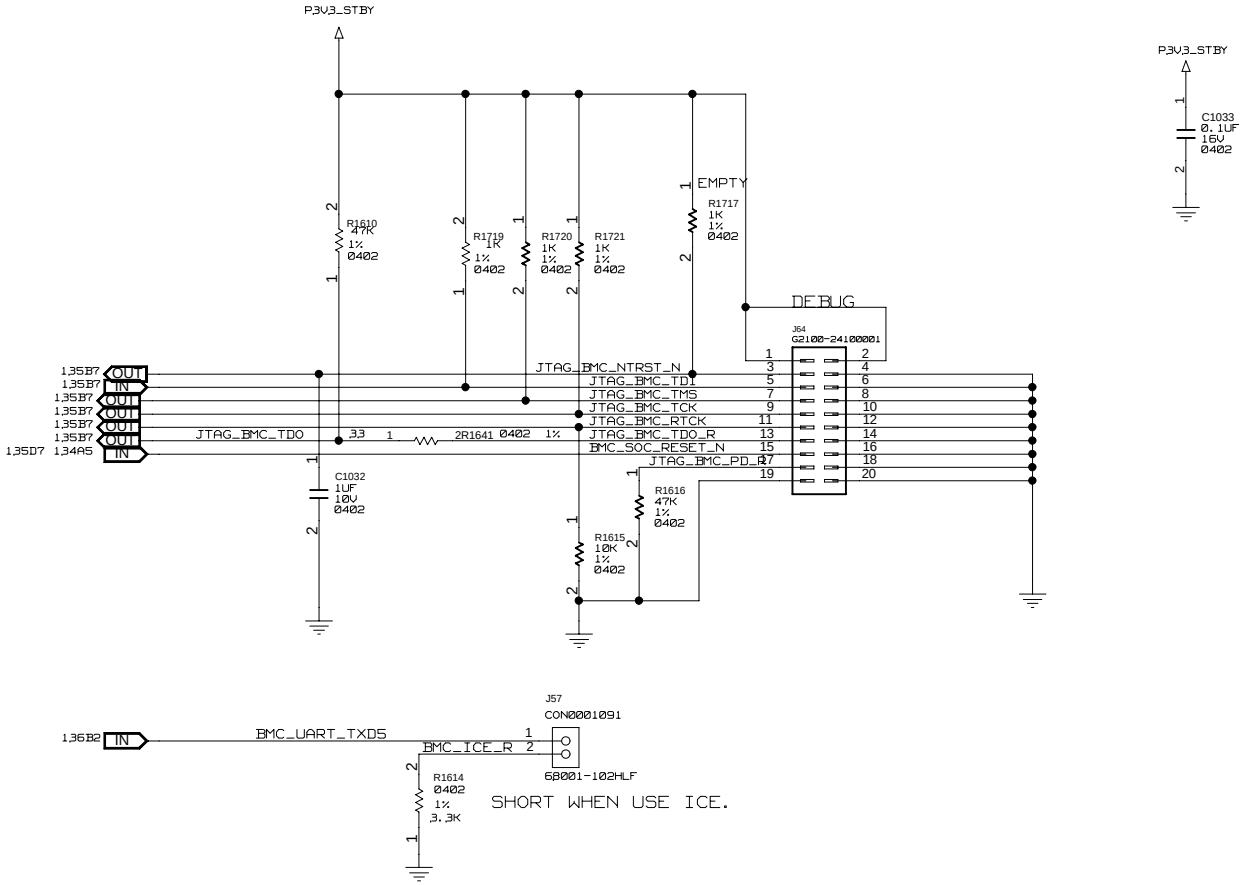
DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 143 OF 360

ROOM=BMC_DEBUG_HEADER



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BMC DEBUG HEADER wolfcreek_controller	DATE: Wed Jul 30 14:59:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 144OF360	

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BLANK

wolfcreek_controller

wolfcreek_controller.cpm

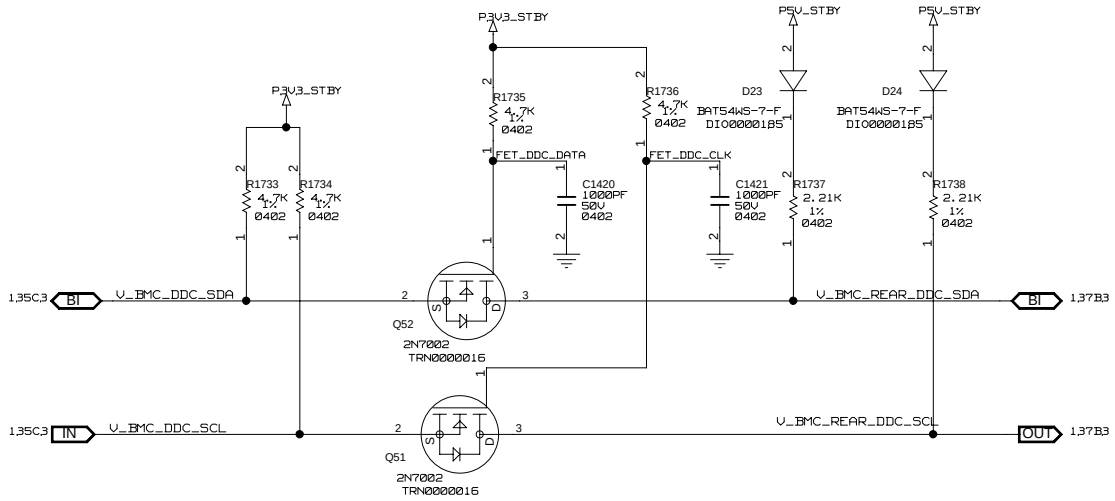
DATE: Tue Jul 08 09:37:06 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 145OF360



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BMC VIDEO SMBUS
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Sun Aug 03 10:48:19 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 146OF,360

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EMC MISC (1 OF 4)

wolfcreek_controller

wolfcreek_controller.cpm

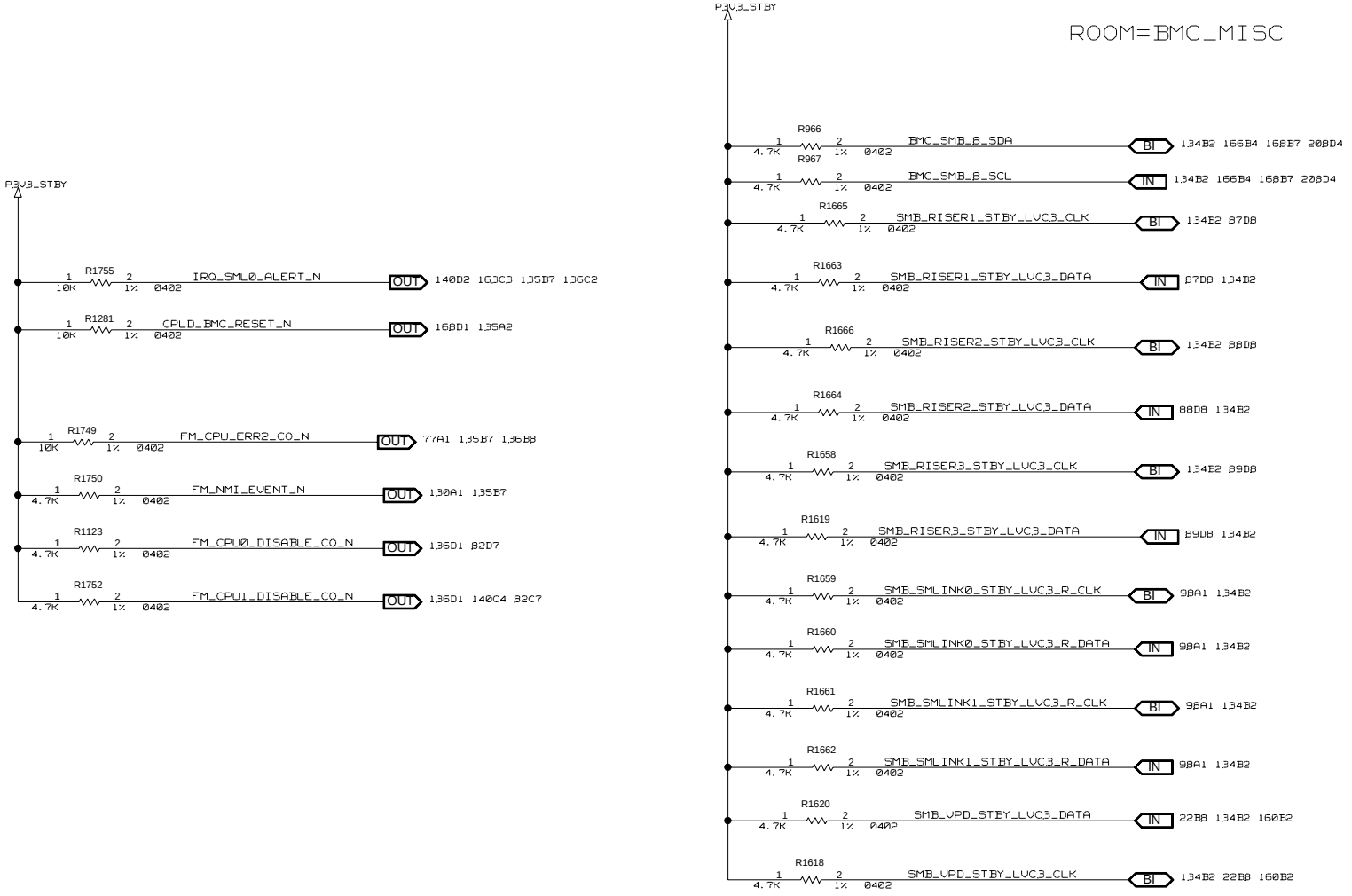
DATE: Wed Aug 06 16:07:25 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 147OF360



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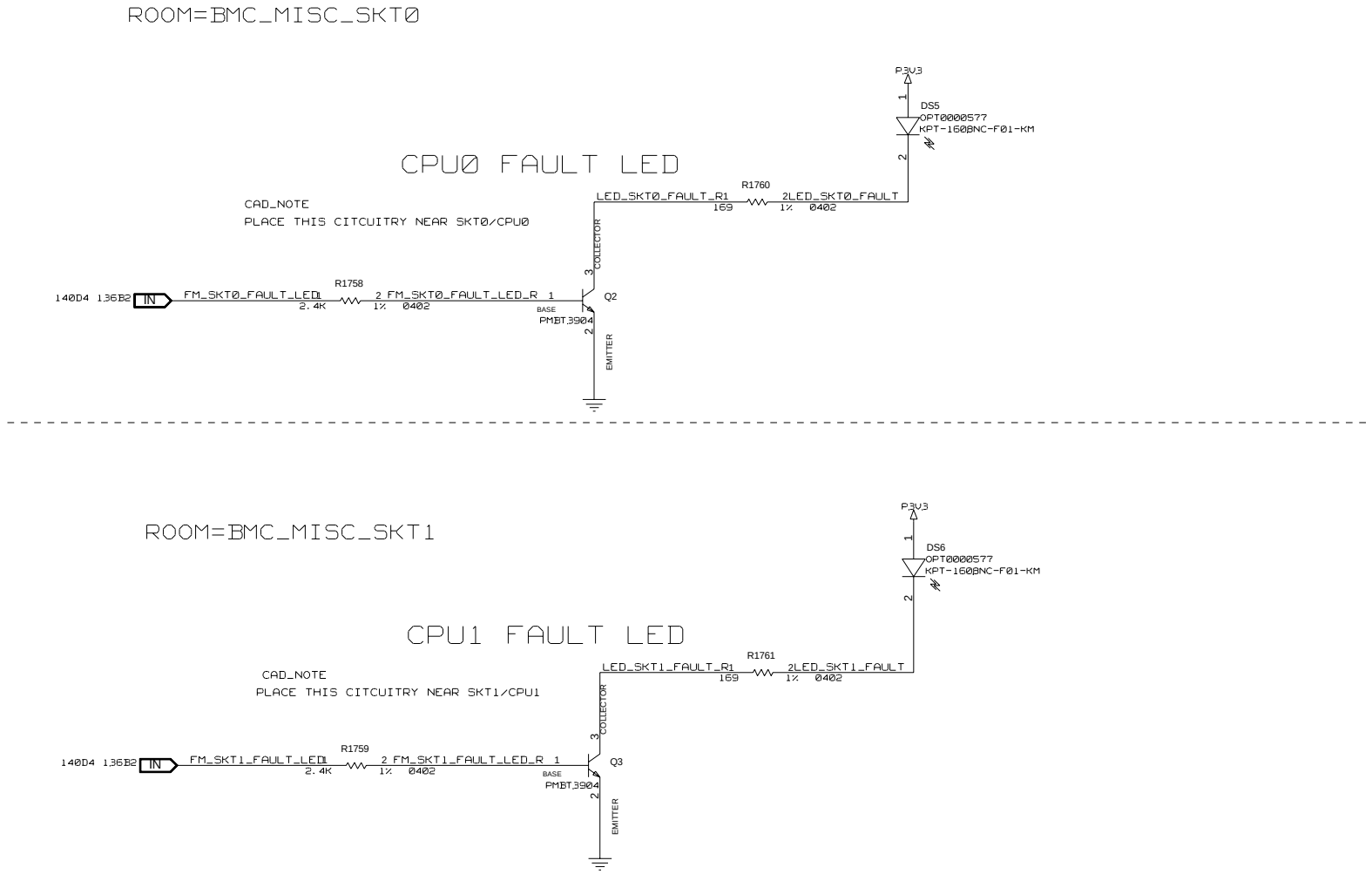
BMC MISC (2 OF 4)
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 17:35:26 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 148OF360



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BMC MISC (3 OF 4) wolfcreek_controller	DATE: Wed Jul 30 14:59:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 149OF360	

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EMC MISC (4 OF 4)

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Sat Jun 28 11:12:00 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 150OF360

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BLANK

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 11:45:50 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 151OF360

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BLANK

wolfcreek_controller

wolfcreek_controller.cpm

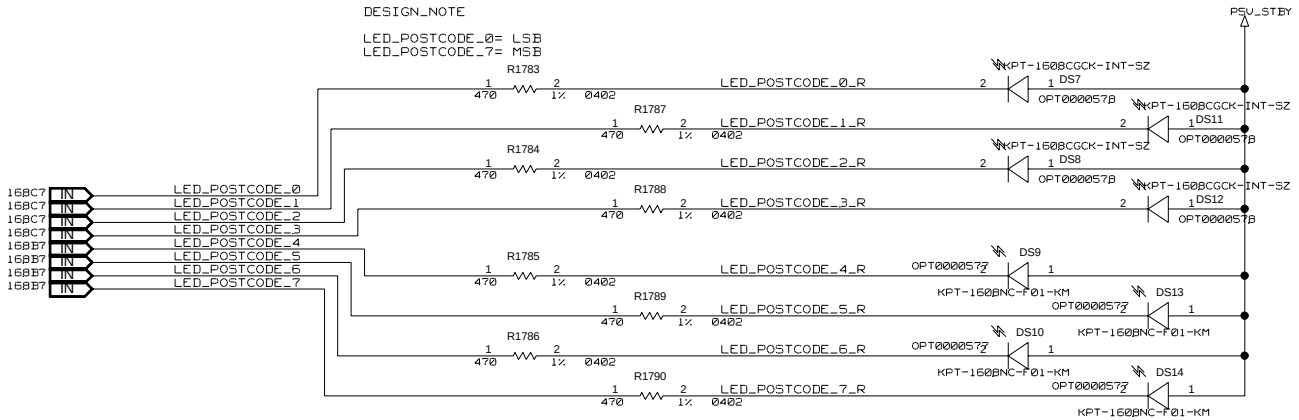
DATE: Wed Jul 02 11:45:50 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 152OF360



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80 PORT LEDS
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 01 15:42:16 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 153 OF 360

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BLANK wolfcreek_controller	DATE: Fri Aug 01 16:36:37 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 154OF360	

ROOM=BMC_SGPI

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BMC SGPIO (3 OF 3)

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 01 16:38:46 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 155OF360

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BLANK

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 02 12:52:39 2014

DRAWN BY: <ENGINEER>

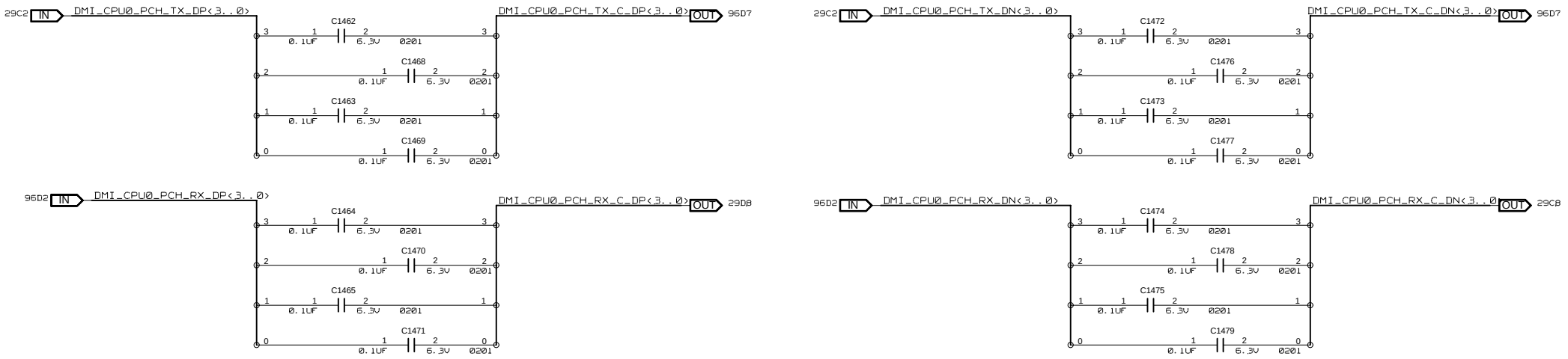
DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 156OF360

ROOM = DMI
BOM_COST = SB

DMI AC CAPS



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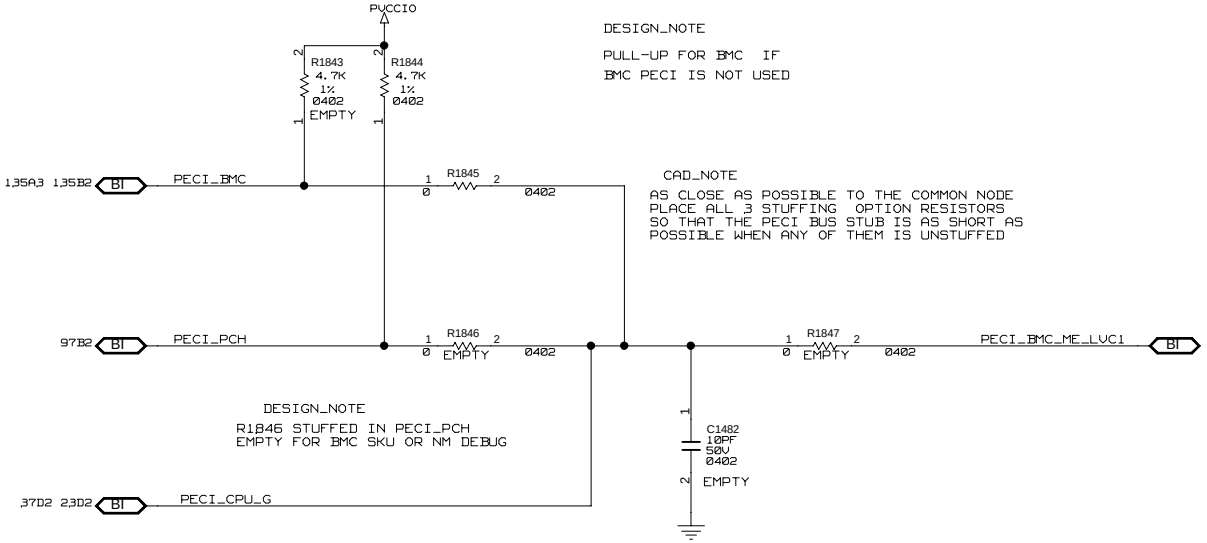
DMI & BMC AC COUPLING CAPS wolfcreek_controller	DATE: Wed Jul 30 14:59:08 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 157OF360	

ROOM=PECI



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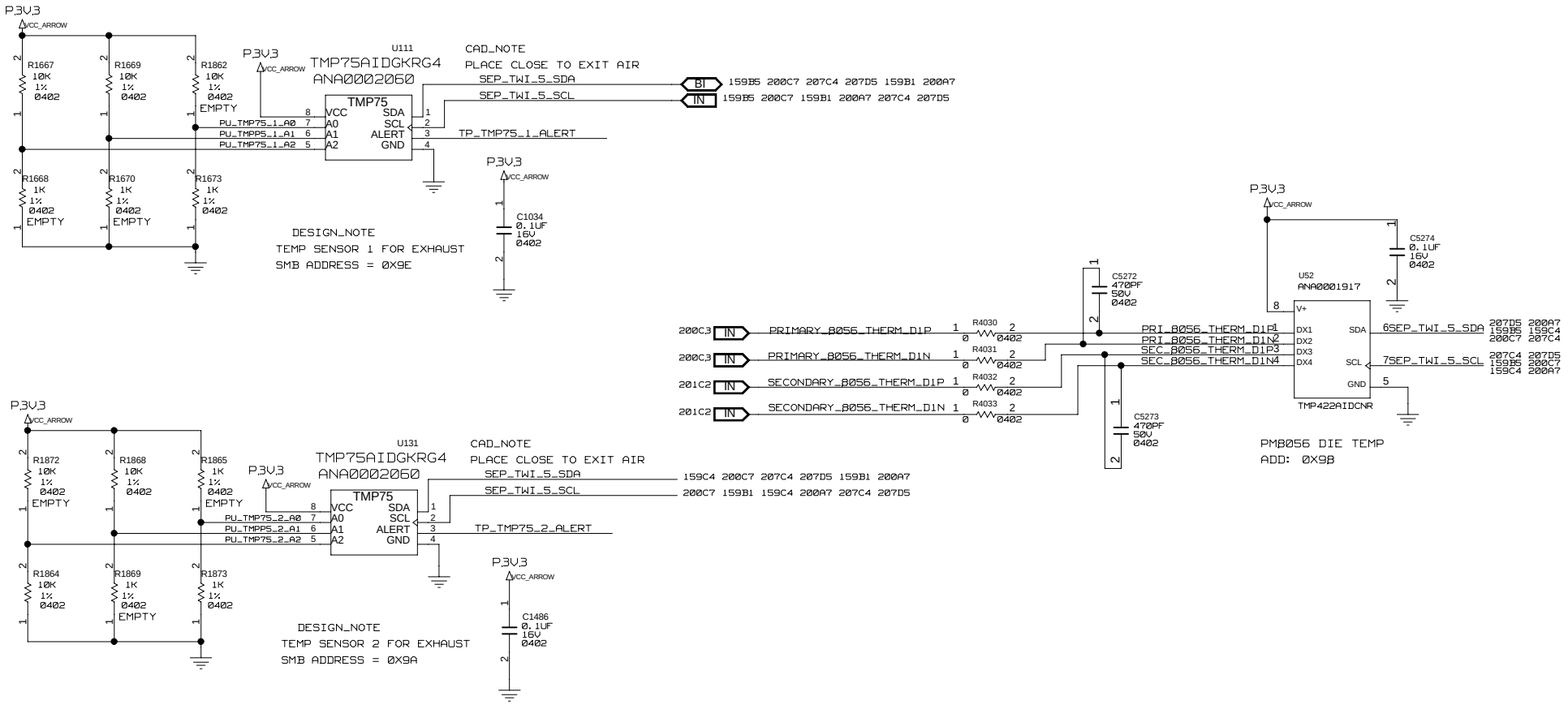
PECI wolfcreek_controller	DATE: Wed Jul 30 14:59:09 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 158OF360	

ROOM=TEMP_SENSORS



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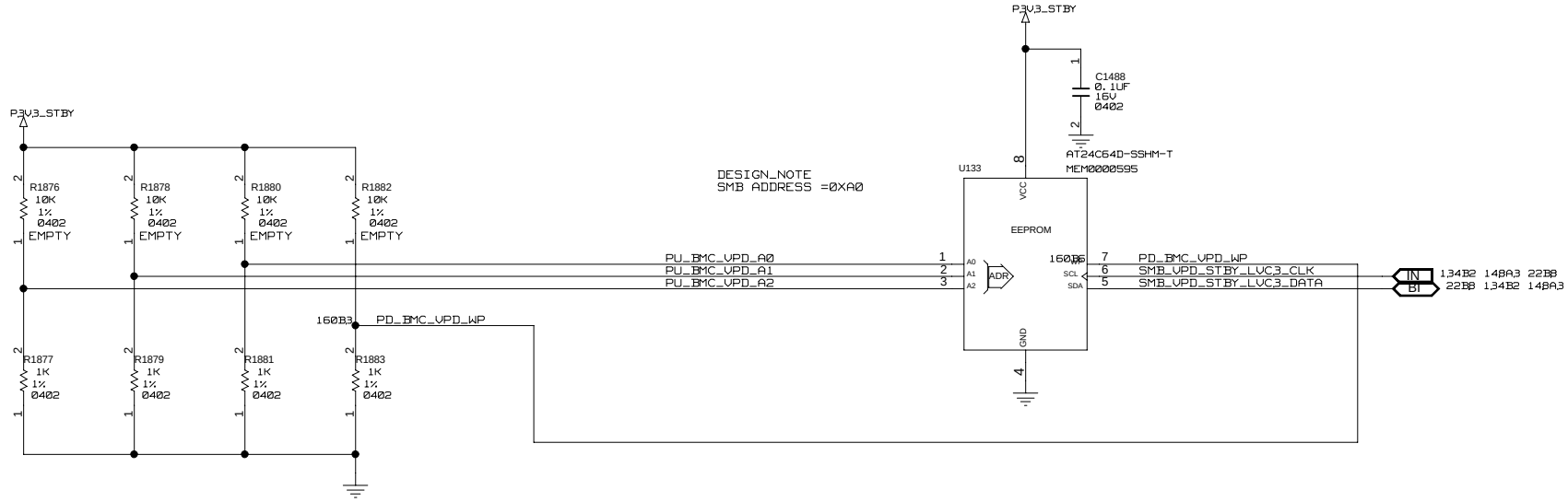
TEMPERATURE SENSORS		DWG NO: <DRAWING_NO>	REV: <REVISION>
wolfcreek_controller	Thu Aug 07 18:52:24 2014		
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 159OF360	



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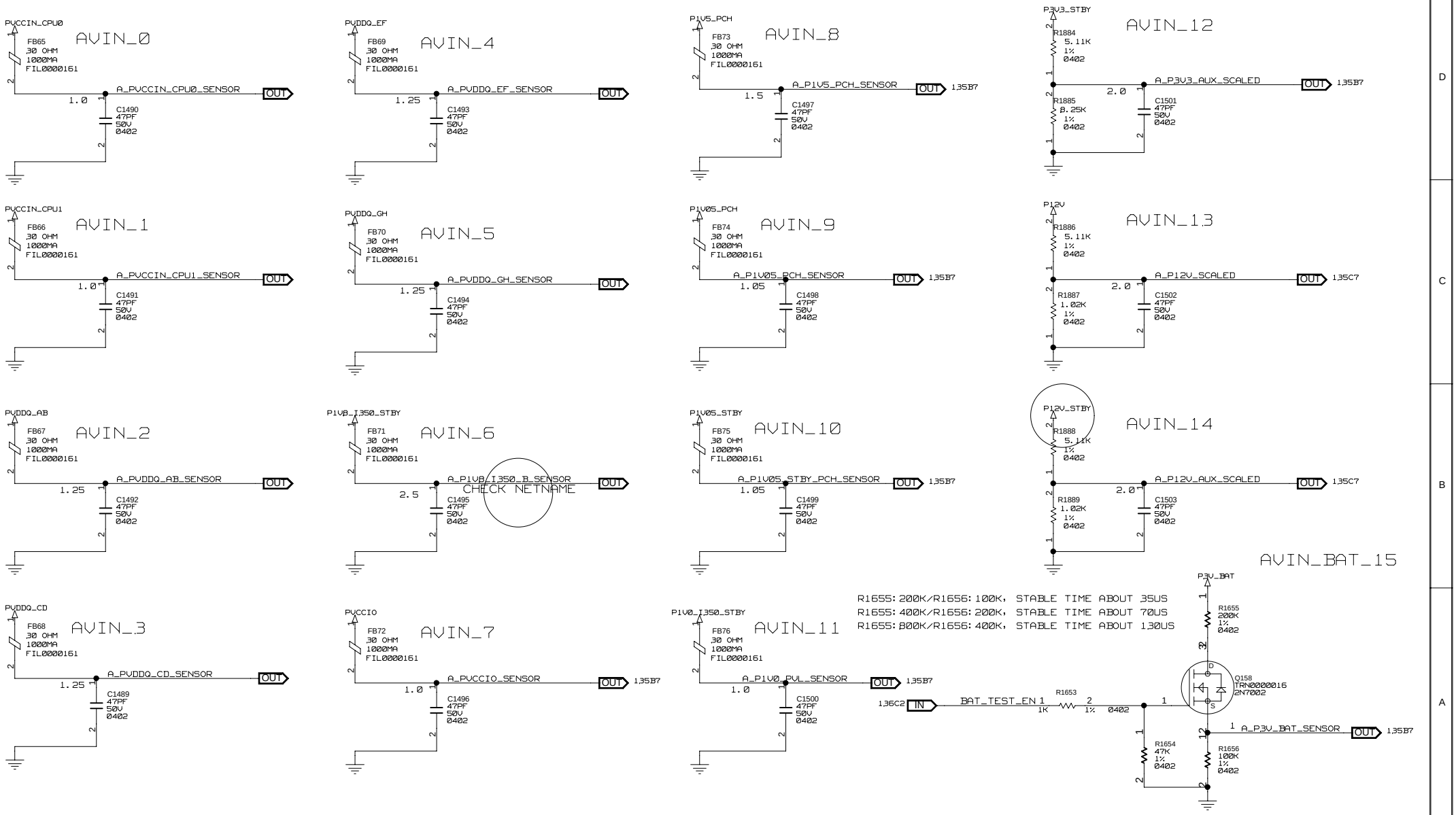
BMC VPD wolfcreek_controller	DATE: Sun Aug 03 10:54:29 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 160OF360	



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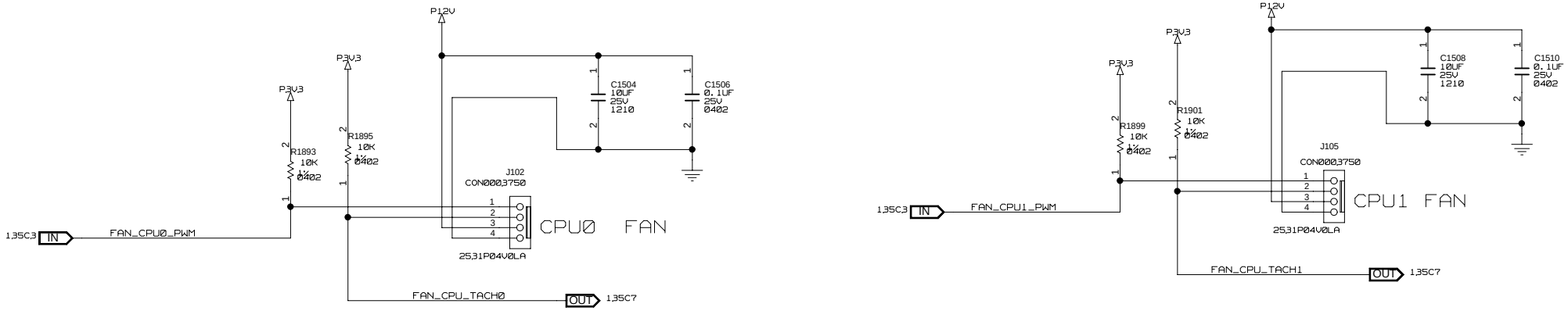
VOLTAGE MONITORING wolfcreek_controller	DATE: Fri Aug 08 18:02:50 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 161OF360	

CPU FAN CONNECTORS



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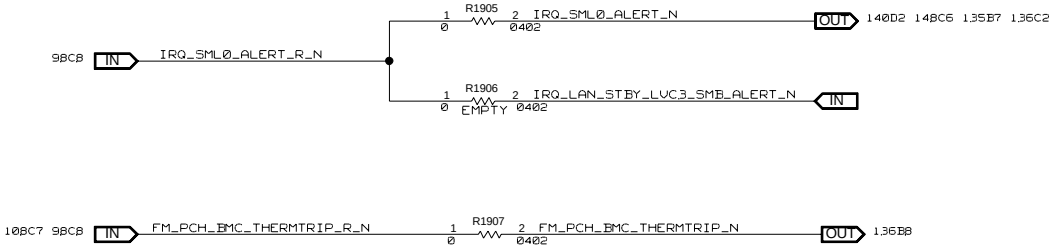
CPU FAN CONNECTORS wolfcreek_controller	DATE: Tue Aug 05 16:35:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 1620F,360	

ROOM=STUF_RES_BMC<->DCMI

PCH-RELATED MISC SIGNALS



DESIGN_NOTE
THIS PAGE SHOWS THE BMC SKU CONNECTIVITY; FOR DCMI SKU,
DEPOP WHAT IT IS EMPTY

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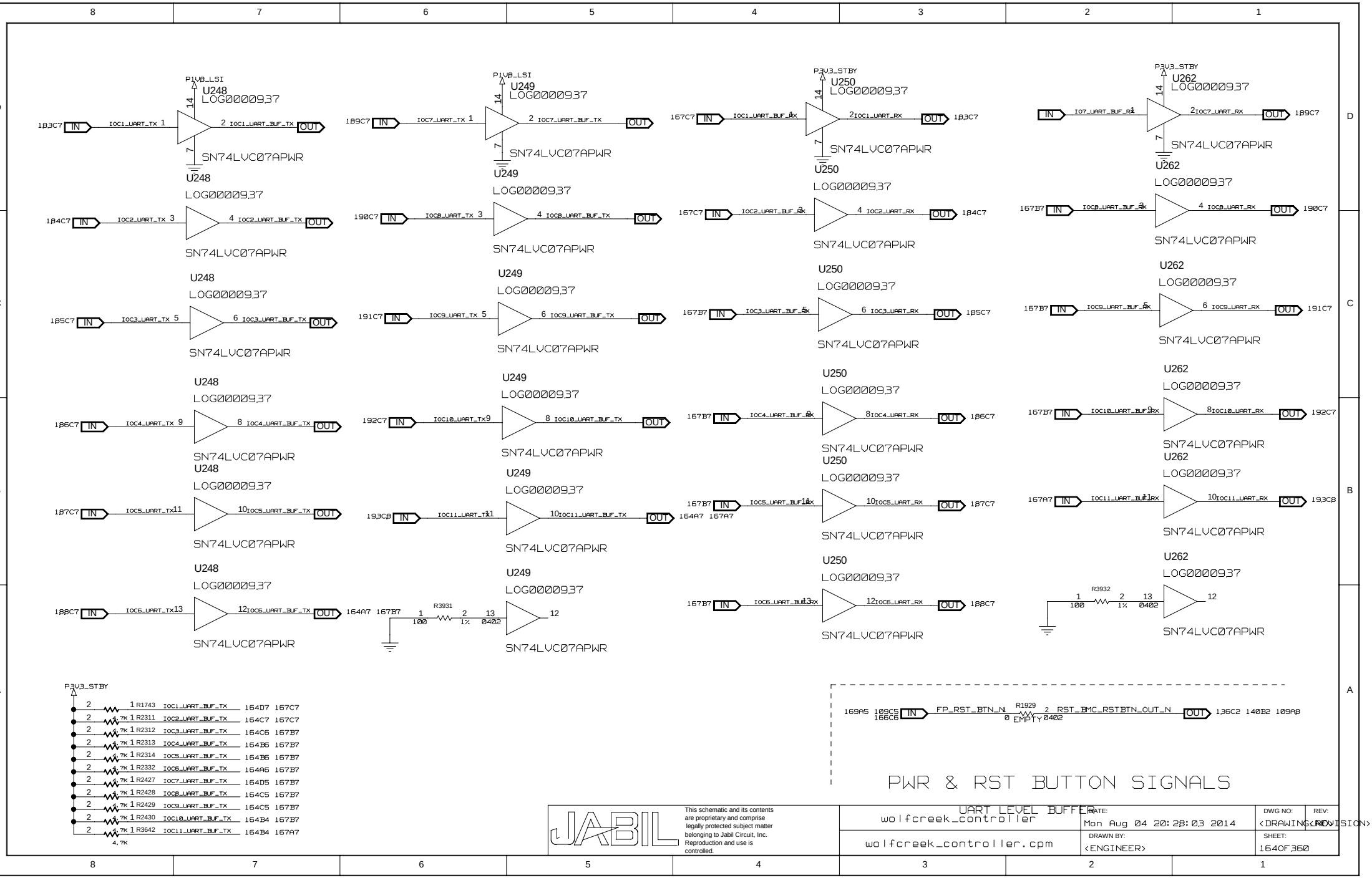
STUFFING RES BMC<->DCMI (1 OF 3)	DATE: Wed Jul 30 14:59:12 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 163OF360	


P1V8_LSI
U248
LOG00009,37
SN74LVC07APWR
IOC1_UART_TX
IOC1_UART_BUF_TX
IOC2_UART_TX
IOC2_UART_BUF_TX
IOC3_UART_TX
IOC3_UART_BUF_TX
IOC4_UART_TX
IOC4_UART_BUF_TX
IOC5_UART_TX
IOC5_UART_BUF_TX
IOC6_UART_TX
IOC6_UART_BUF_TX
P1V8_LSI
U249
IOC7_UART_TX
IOC7_UART_BUF_TX
IOC8_UART_TX
IOC8_UART_BUF_TX
IOC9_UART_TX
IOC9_UART_BUF_TX
IOC10_UART_TX
IOC10_UART_BUF_TX
IOC11_UART_TX
IOC11_UART_BUF_TX
R3931
P3V3_STBY
U250
IOC1_UART_BUF_RX
IOC1_UART_RX
IOC2_UART_BUF_RX
IOC2_UART_RX
IOC3_UART_BUF_RX
IOC3_UART_RX
IOC4_UART_BUF_RX
IOC4_UART_RX
IOC5_UART_BUF_RX
IOC5_UART_RX
IOC6_UART_BUF_RX
IOC6_UART_RX
U262
IOC7_UART_BUF_RX
IOC7_UART_RX
IOC8_UART_BUF_RX
IOC8_UART_RX
IOC9_UART_BUF_RX
IOC9_UART_RX
IOC10_UART_BUF_RX
IOC10_UART_RX
IOC11_UART_BUF_RX
IOC11_UART_RX
R3932
R1743
R2311
R2312
R2313
R2314
R2332
R2427
R2428
R2429
R2430
R3642
4.7K
FP_RST_BTN_N
R1929
RST_BMC_RSTBTN_OUT_N
PWR & RST BUTTON SIGNALS
UART LEVEL BUFFER
wolfcreek_controller
wolfcreek_controller.cpm
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DATE:
Mon Aug 04 20:28:03 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
164OF360

ROOM=STUF_RES_BMC<->DCMI

7BA1 IN H_CPU0_MEMAB_MEMHOT_LVT3_N 1 R1930 2 H_CPU0_MEMAB_MEMHOT_BMC_LVT3_N OUT 140A4 136C2
0 0402

7BA1 IN H_CPU0_MEMCD_MEMHOT_LVT3_N 1 R1932 2 H_CPU0_MEMCD_MEMHOT_BMC_LVT3_N OUT 140A4
0 0402

7BA1 IN H_CPU1_MEMEF_MEMHOT_LVT3_N 1 R1934 2 H_CPU1_MEMEF_MEMHOT_BMC_LVT3_N OUT 140B4
0 0402

7BA1 IN H_CPU1_MEMGH_MEMHOT_LVT3_N 1 R1936 2 H_CPU1_MEMGH_MEMHOT_BMC_LVT3_N OUT 140B4 136C2
0 0402

166C6 12BB8 85C4 23C2 IN FM_CPU0_SKTOCC_LVT3_N 1 R1938 2 FM_CPU0_SKTOCC_BMC_LVT3_N OUT 135B2
0 0402

166C6 12BA1 85C4 37C2 IN FM_CPU1_SKTOCC_LVT3_N 1 R1940 2 FM_CPU1_SKTOCC_BMC_LVT3_N OUT 135B2
0 0402

PCH'S GPIO EXPANDER SIGNALS

DESIGN_NOTE
THIS PAGE SHOWS THE BMC SKU CONNECTIVITY; FOR DCMI SKU,
DEPOP WHAT IT IS EMPTY

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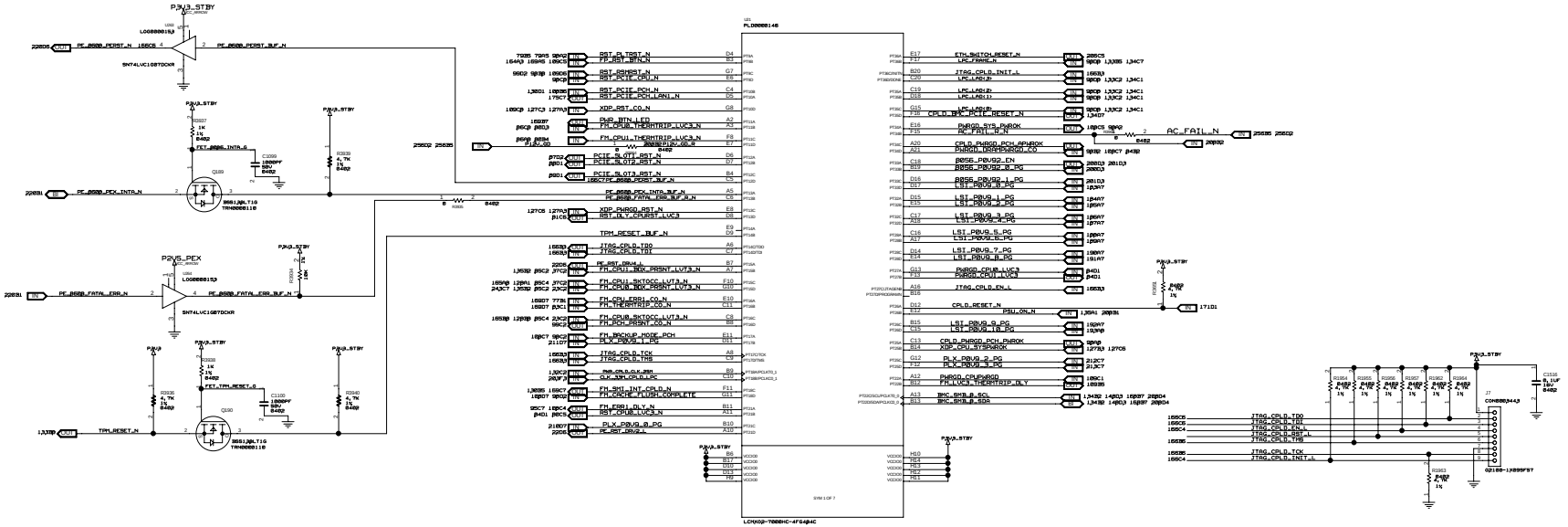
STUFFING RES BMC<->DCMI (3 OF 3)	DATE: Fri Aug 08 17:35:01 2014	DWG NO: <DRAWING NO>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 165OF360	



JABIL

wolfcreek_controller

wolfcreek_controller.cpm

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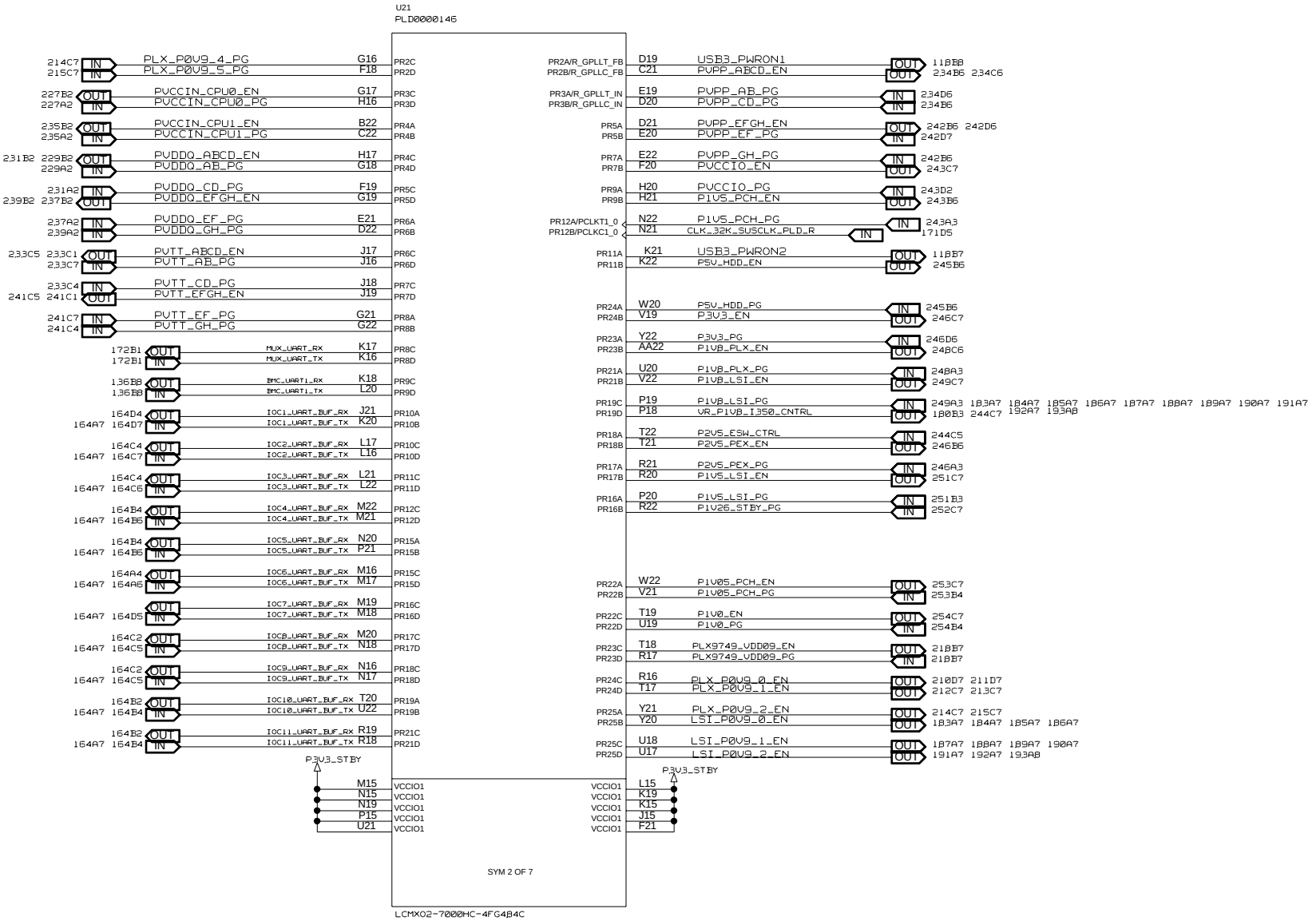
DATE: Fri Aug 08 13:26:26 2014	DWG NO: <DWG>
DRAWN BY: <ENGINEER>	SHEET: 166OF350
	REV: A-0



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CPLD (2 OF 6)
wolfcreek_controller

wolfcreek_controller.cpm

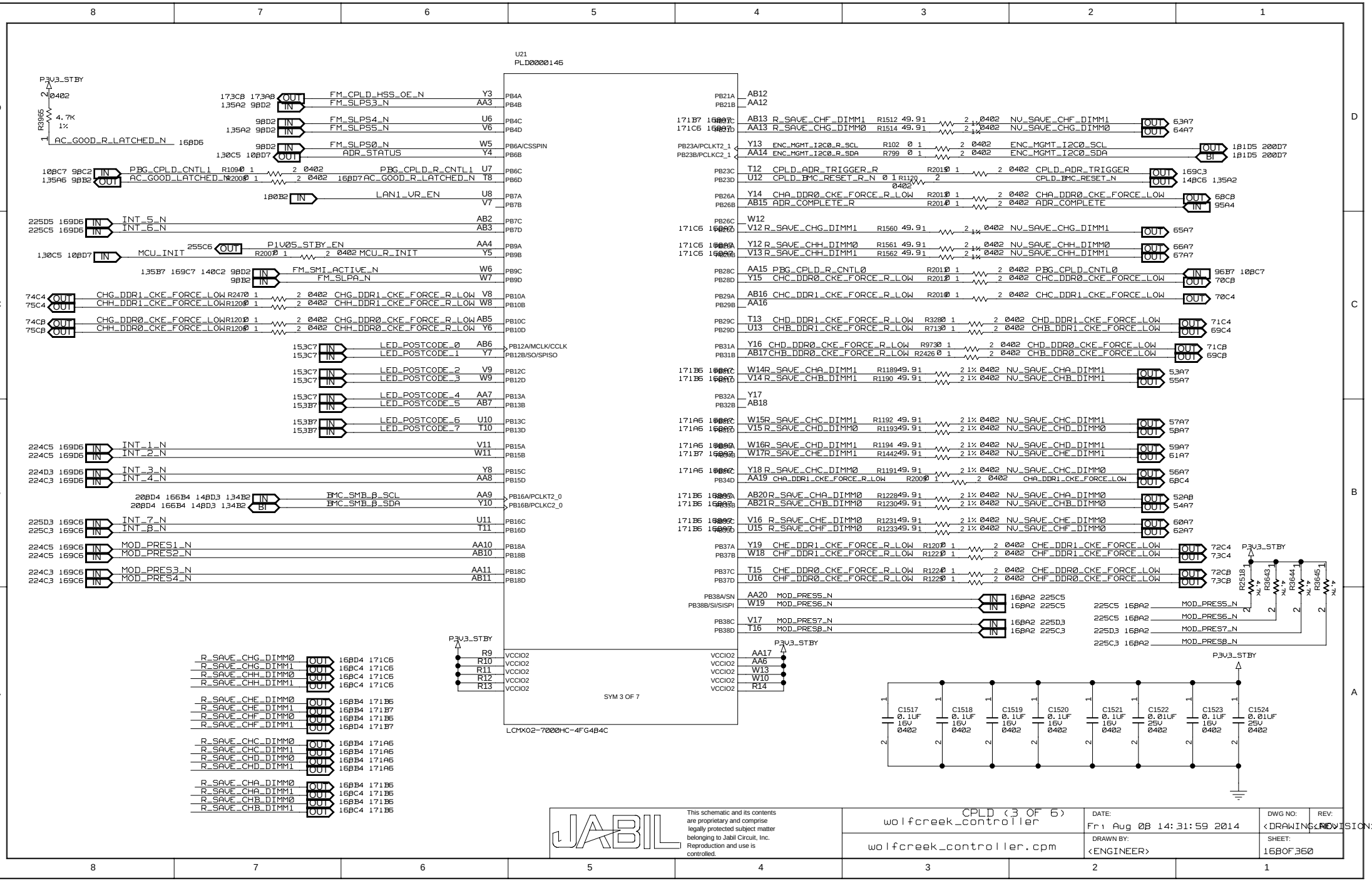
DATE: Fri Aug 08 13:49:47 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 167OF360



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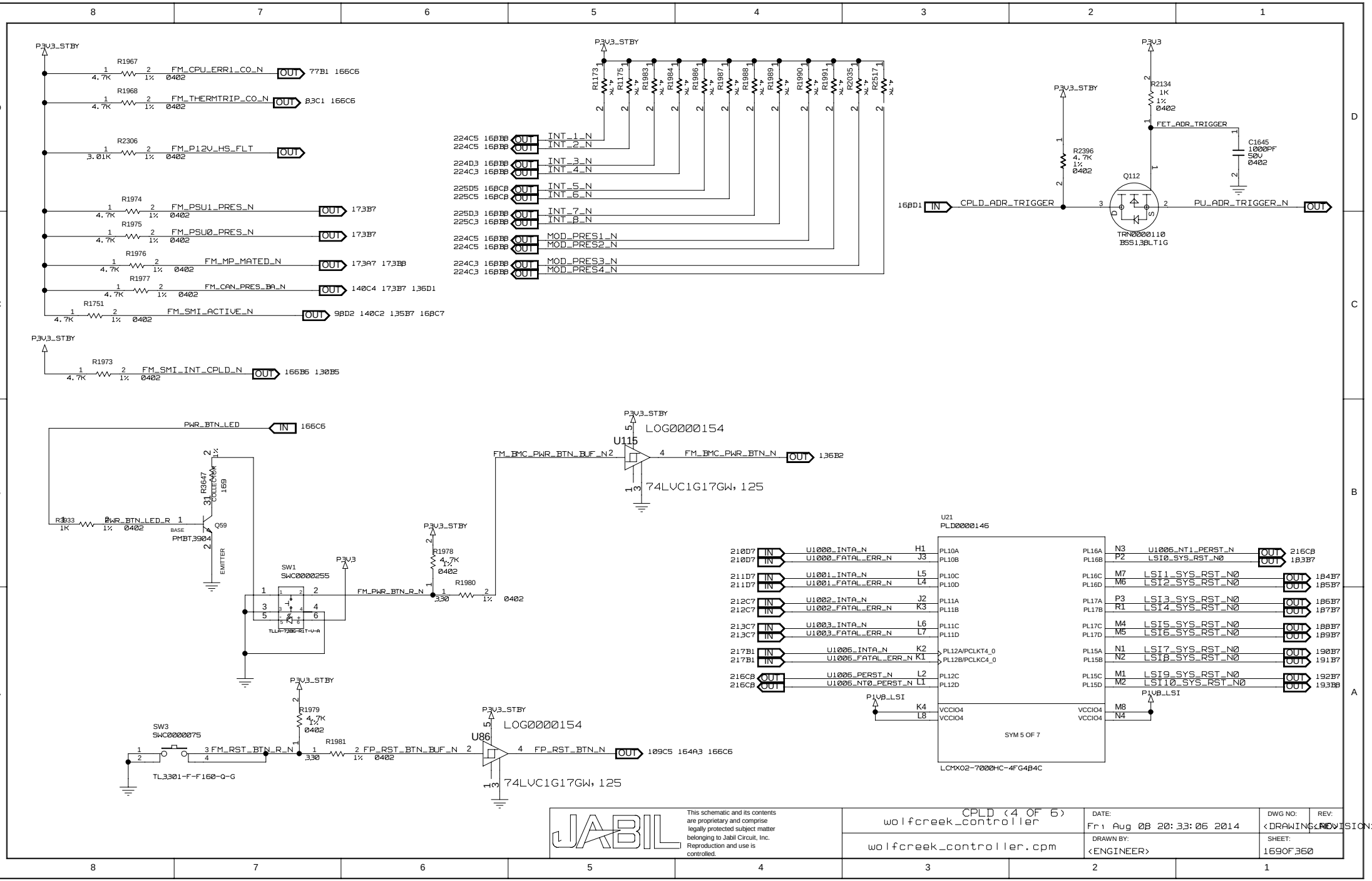
CPLD (3 OF 6) wolfcreek_controller	DATE: Fri Aug 08 14:31:59 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 168 OF 360	


P3V3_STBY
R1967 4.7K 1% 0402 FM_CPU_ERR1_CO_N OUT 77B1 166C6
R1968 4.7K 1% 0402 FM_THERMTRIP_CO_N OUT 83C1 166C6
R2306 3.01K 1% 0402 FM_P12V_HS_FLT OUT
R1974 4.7K 1% 0402 FM_PSU1_PRES_N OUT 173B7
R1975 4.7K 1% 0402 FM_PSU0_PRES_N OUT 173B7
R1976 4.7K 1% 0402 FM_MP_MATED_N OUT 173A7 173B8
R1977 4.7K 1% 0402 FM_CAN_PRES_BA_N OUT 140C4 173B7 136D1
R1751 4.7K 1% 0402 FM_SMI_ACTIVE_N OUT 98D2 140C2 135B7 168C7
R1973 4.7K 1% 0402 FM_SMI_INT_CPLD_N OUT 166B6 130B5
R1173 R1175 R1983 R1984 R1986 R1987 R1988 R1989 R1990 R1991 R2035 R2517 4.7K
224C5 168B8 OUT INT_1_N
224C5 168B8 OUT INT_2_N
224D3 168B8 OUT INT_3_N
224C3 168B8 OUT INT_4_N
225D5 168C8 OUT INT_5_N
225C5 168C8 OUT INT_6_N
225D3 168B8 OUT INT_7_N
225C3 168B8 OUT INT_8_N
224C5 168B8 OUT MOD_PRES1_N
224C5 168B8 OUT MOD_PRES2_N
224C3 168B8 OUT MOD_PRES3_N
224C3 168B8 OUT MOD_PRES4_N
P3V3
R2134 1K 1% 0402
FET_ADR_TRIGGER
C1645 1000PF 50V 0402
R2396 4.7K 1% 0402
Q112
168D1 IN CPLD_ADR_TRIGGER
PU_ADR_TRIGGER_N OUT
TRN0000110
BSS138LT1G
PWR_BTN_LED IN 166C6
R3647 COLLECTOR 169
R3033 1K 1% 0402 PWR_BTN_LED_R
Q59 PMBT3904
BASE
EMITTER
SW1 SWC0000255
TLLA-73BG-RIT-V-A
FM_PWR_BTN_R_N
R1978 4.7K 1% 0402
R1980 330 1% 0402
FM_BMC_PWR_BTN_BUF_N
U115 LOG0000154
74LVC1G17GW,125
FM_BMC_PWR_BTN_N OUT 136B2
U21 PLD0000146
210D7 IN U1000_INTA_N H1 PL10A
210D7 IN U1000_FATAL_ERR_N J3 PL10B
211D7 IN U1001_INTA_N L5 PL10C
211D7 IN U1001_FATAL_ERR_N L4 PL10D
212C7 IN U1002_INTA_N J2 PL11A
212C7 IN U1002_FATAL_ERR_N K3 PL11B
213C7 IN U1003_INTA_N L6 PL11C
213C7 IN U1003_FATAL_ERR_N L7 PL11D
217B1 IN U1006_INTA_N K2 PL12A/PCLKT4_0
217B1 IN U1006_FATAL_ERR_N K1 PL12B/PCLKC4_0
216C8 OUT U1006_PERST_N L2 PL12C
216C8 OUT U1006_NT0_PERST_N L1 PL12D
P1V8_LSI K4 VCCIO4
L8 VCCIO4
PL16A N3 U1006_NT1_PERST_N OUT 216C8
PL16B P2 LSI0_SYS_RST_N0 OUT 183B7
PL16C M7 LSI1_SYS_RST_N0 OUT 184B7
PL16D M6 LSI2_SYS_RST_N0 OUT 185B7
PL17A P3 LSI3_SYS_RST_N0 OUT 186B7
PL17B R1 LSI4_SYS_RST_N0 OUT 187B7
PL17C M4 LSI5_SYS_RST_N0 OUT 188B7
PL17D M5 LSI6_SYS_RST_N0 OUT 189B7
PL15A N1 LSI7_SYS_RST_N0 OUT 190B7
PL15B N2 LSI8_SYS_RST_N0 OUT 191B7
PL15C M1 LSI9_SYS_RST_N0 OUT 192B7
PL15D M2 LSI10_SYS_RST_N0 OUT 193B8
P1V8_LSI M8 VCCIO4
N4 VCCIO4
SYM 5 OF 7
LCMXO2-7000HC-4FG484C
SW3 SWC0000075
TL3301-F-F160-Q-G
R1979 4.7K 1% 0402
FM_RST_BTN_R_N
R1981 330 1% 0402 FP_RST_BTN_BUF_N
U86 LOG0000154
74LVC1G17GW,125
FP_RST_BTN_N OUT 109C5 164A3 166C6
JABIL
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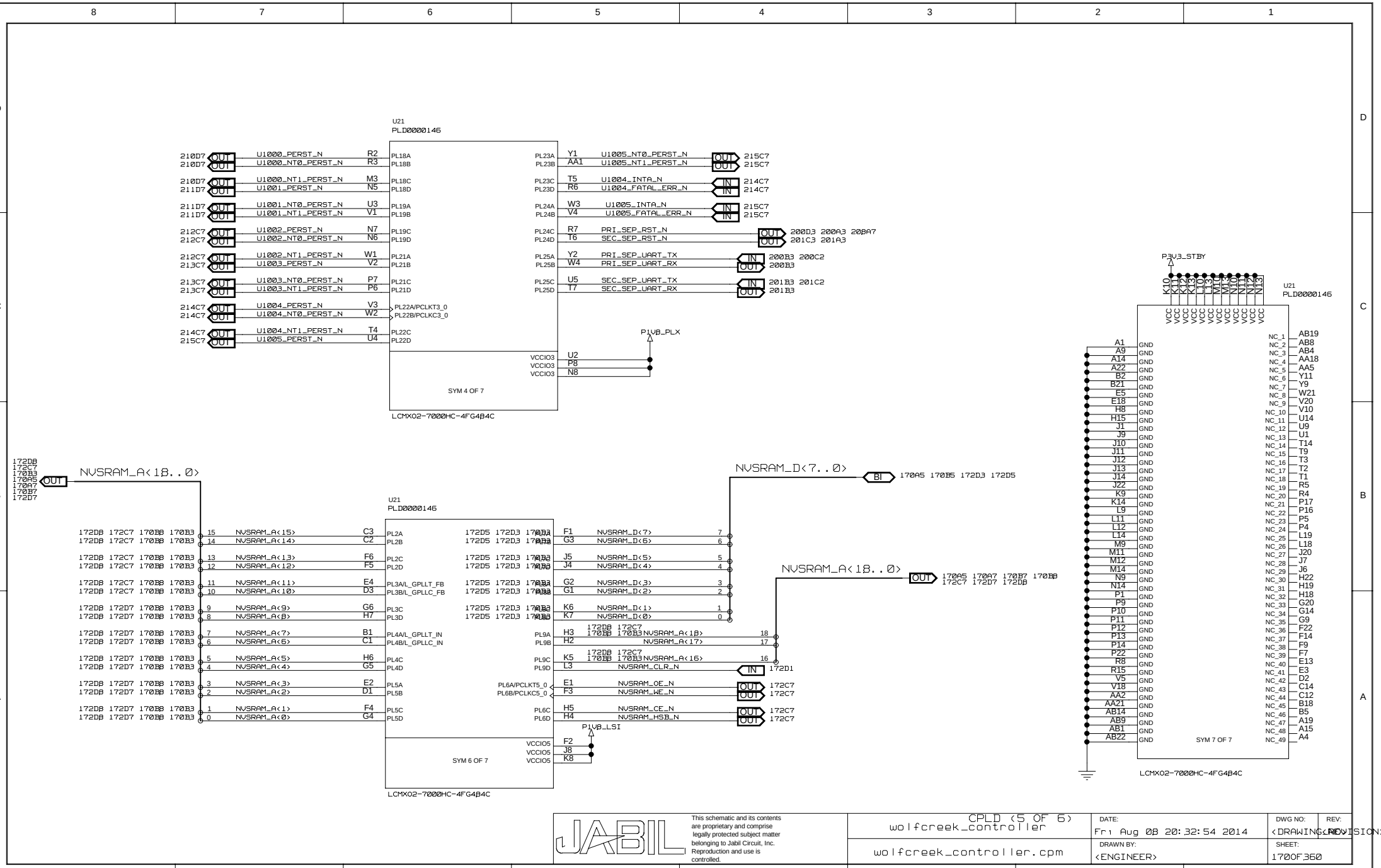
CPLD (4 OF 6)
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Fri Aug 08 20:33:06 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 169OF360



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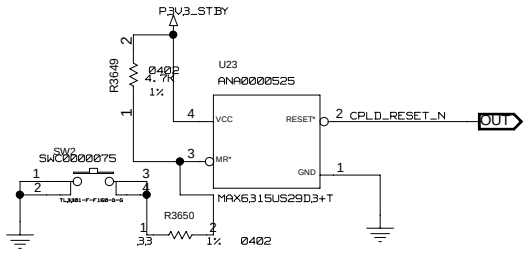
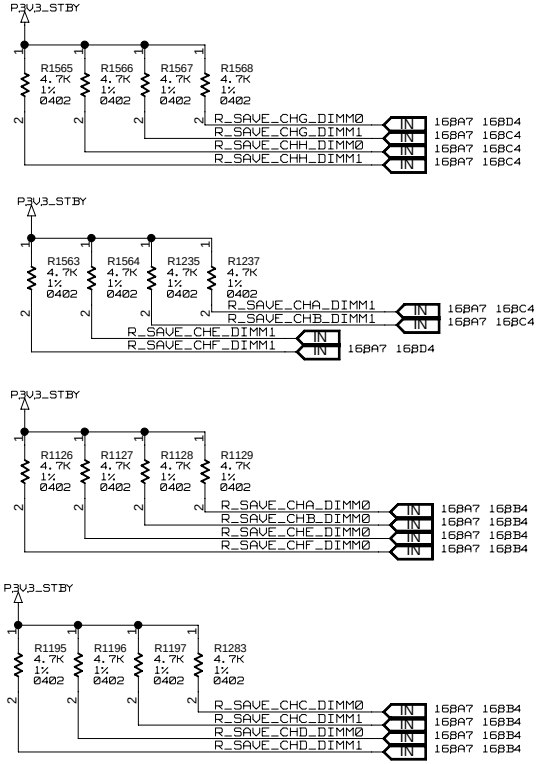
CPLD (5 OF 6) wolfcreek_controller	DATE: Fri Aug 08 20:32:54 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 170OF360	

CAD NOTE: PLACE TERMINATION RESISTOR WITHIN 1" FROM PLD

1,32C4 IN CLK_32K_SUSCLK_PLD 1 R1996 22.1 2 CLK_32K_SUSCLK_PLD_R 1% 0402 OUT 167C4





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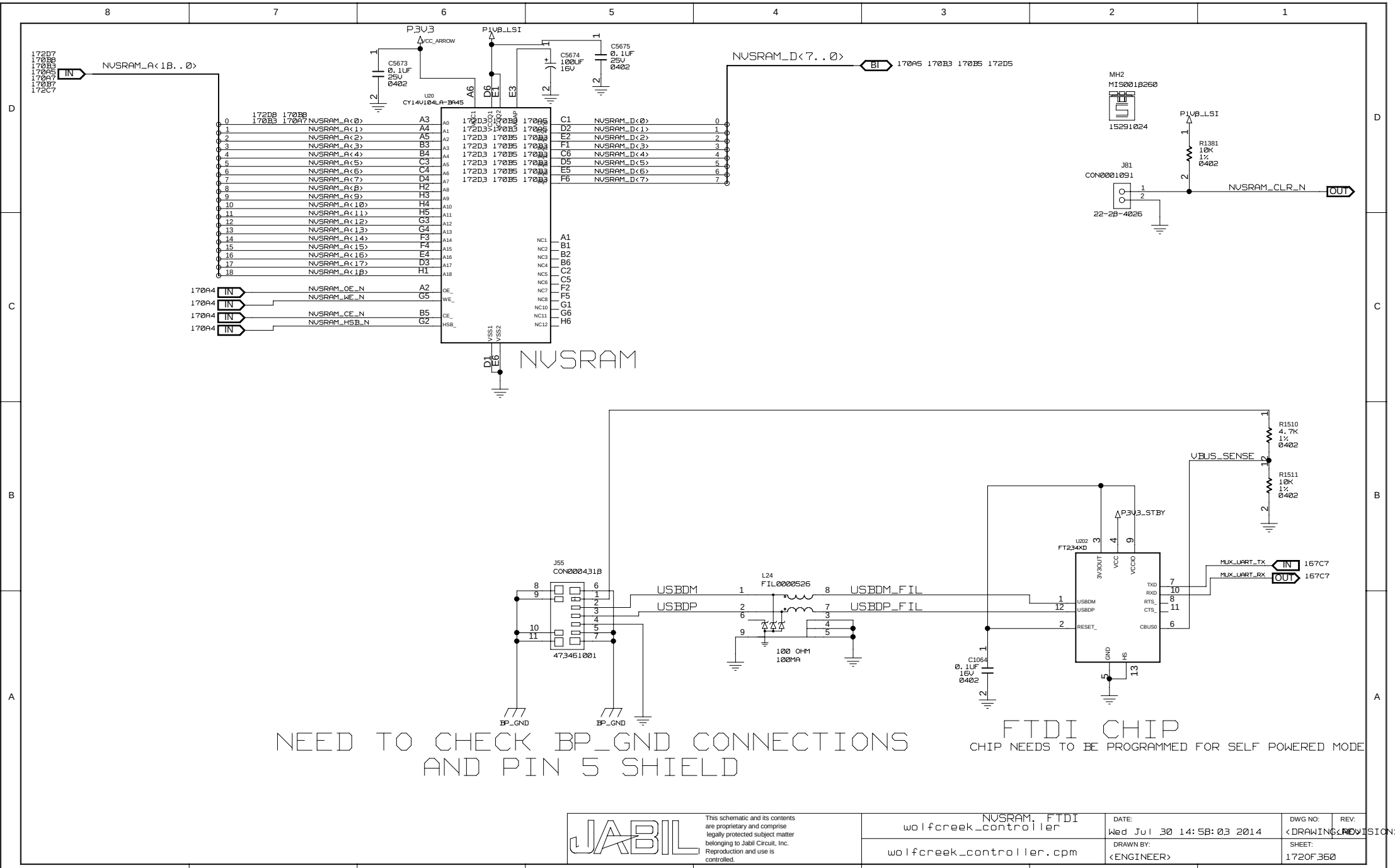
CPLD (6 OF 6) wolfcreek_controller	DATE: Thu Aug 07 20:57:44 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 17 OF 360	



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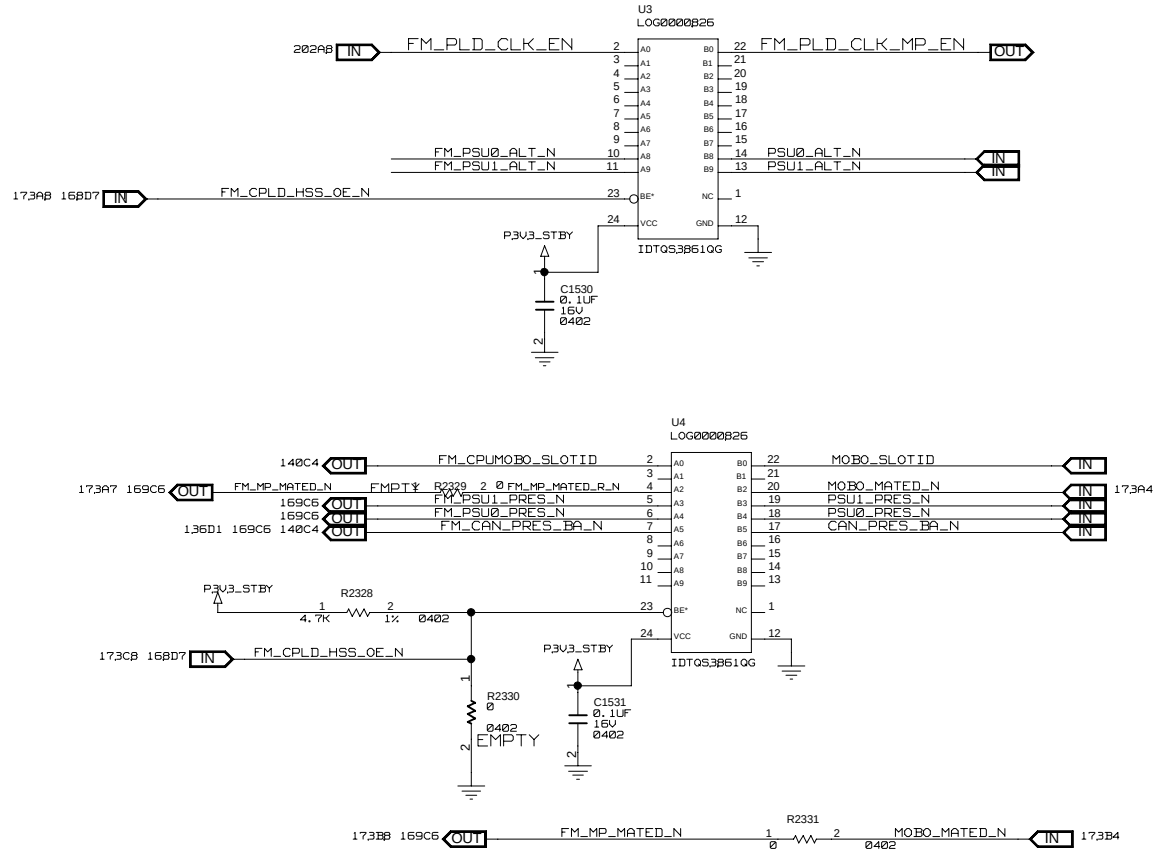
NVSRAM, FTDI wolfcreek_controller	DATE: Wed Jul 30 14:58:03 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 17 OF 360	

HOTSWAP FOR MIDPLANE SIGNALS
NEEDS TO BE UPDATED WITH CURRENT
SIGNALS



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MP HOTSWAP SINGALS wolfcreek_controller	DATE: Fri Aug 01 15:51:53 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 173OF360	

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MP HOTSWAP SMBUS
wolfcreek_controller

wolfcreek_controller.cpm

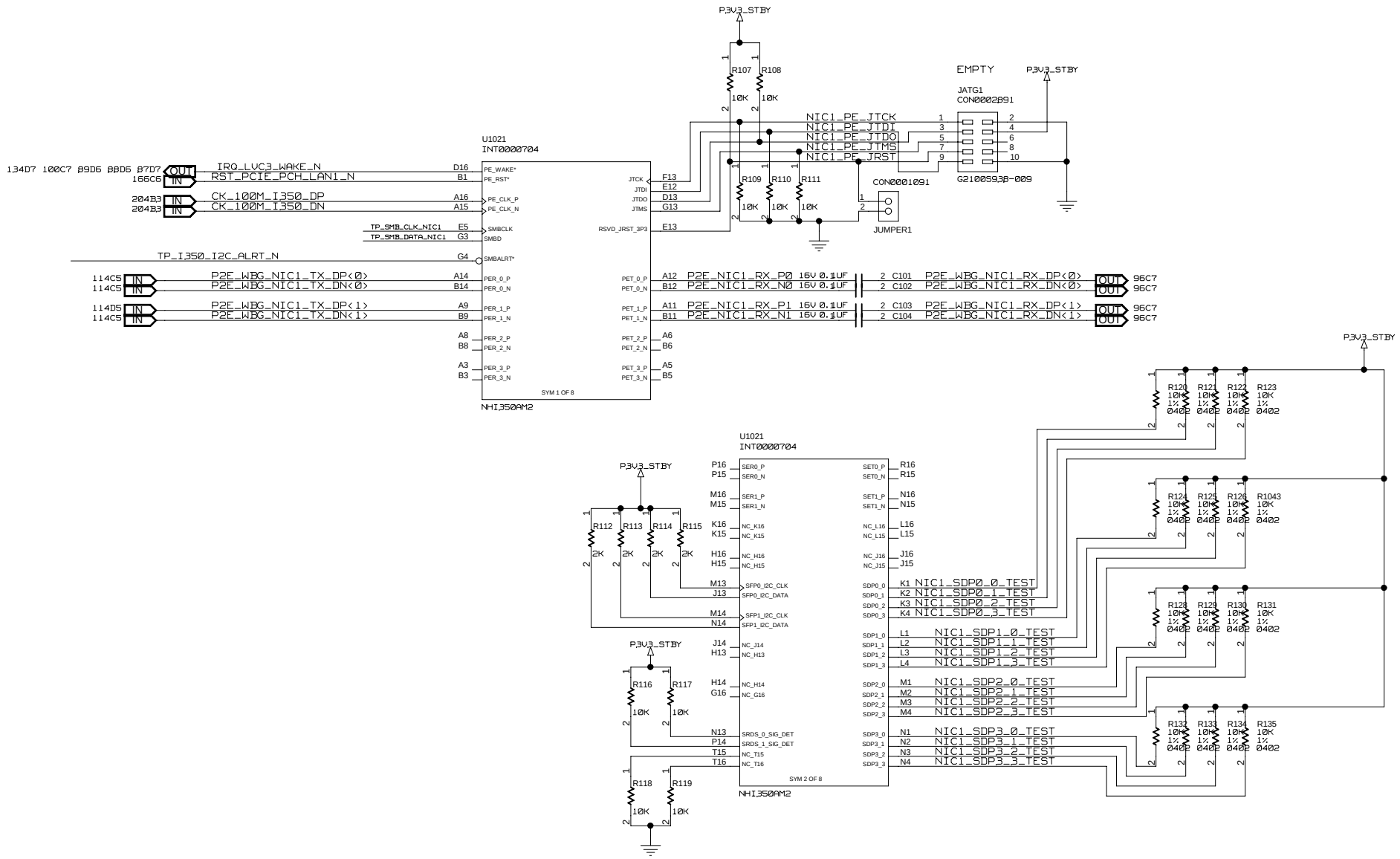
DATE: Fri Aug 08 09:55:13 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 174OF360



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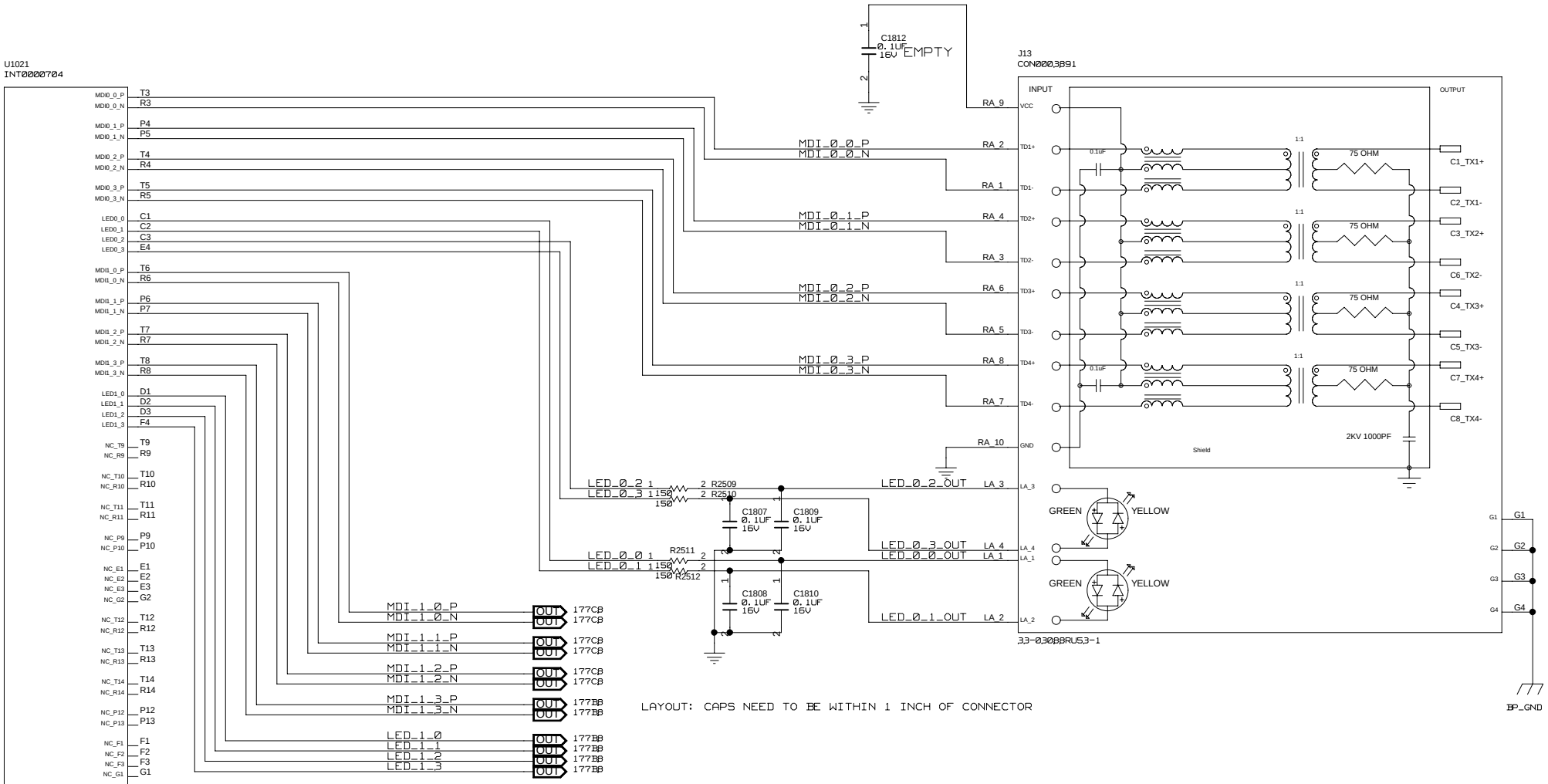
POWERVILLE NIC (1 OF 6)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Fri Aug 08 10:23:11 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 175OF360



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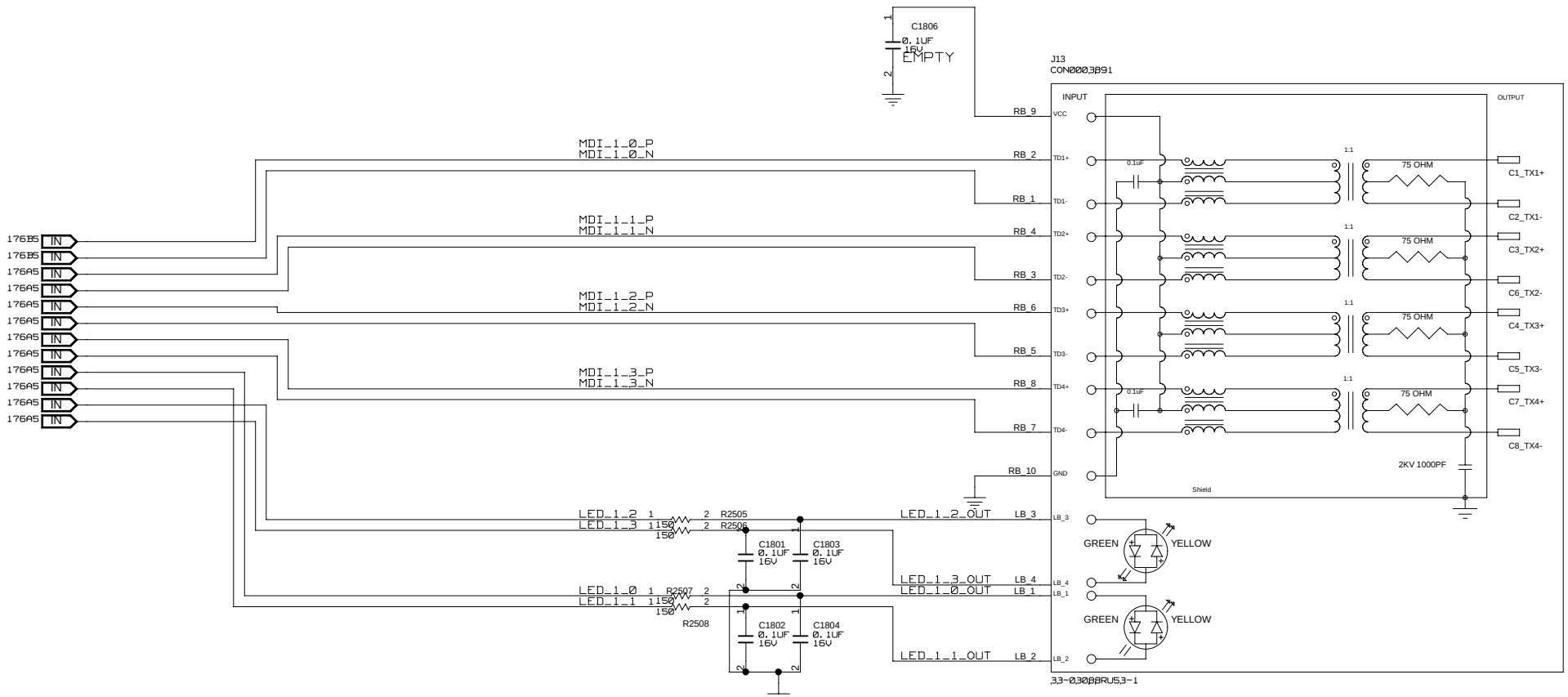
POWERVILLE NIC (2 OF 6)	DATE: Wed Jul 30 14:58:01 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 176OF360	



LAYOUT: CAPS NEED TO BE WITHIN 1 INCH OF CONNECTOR

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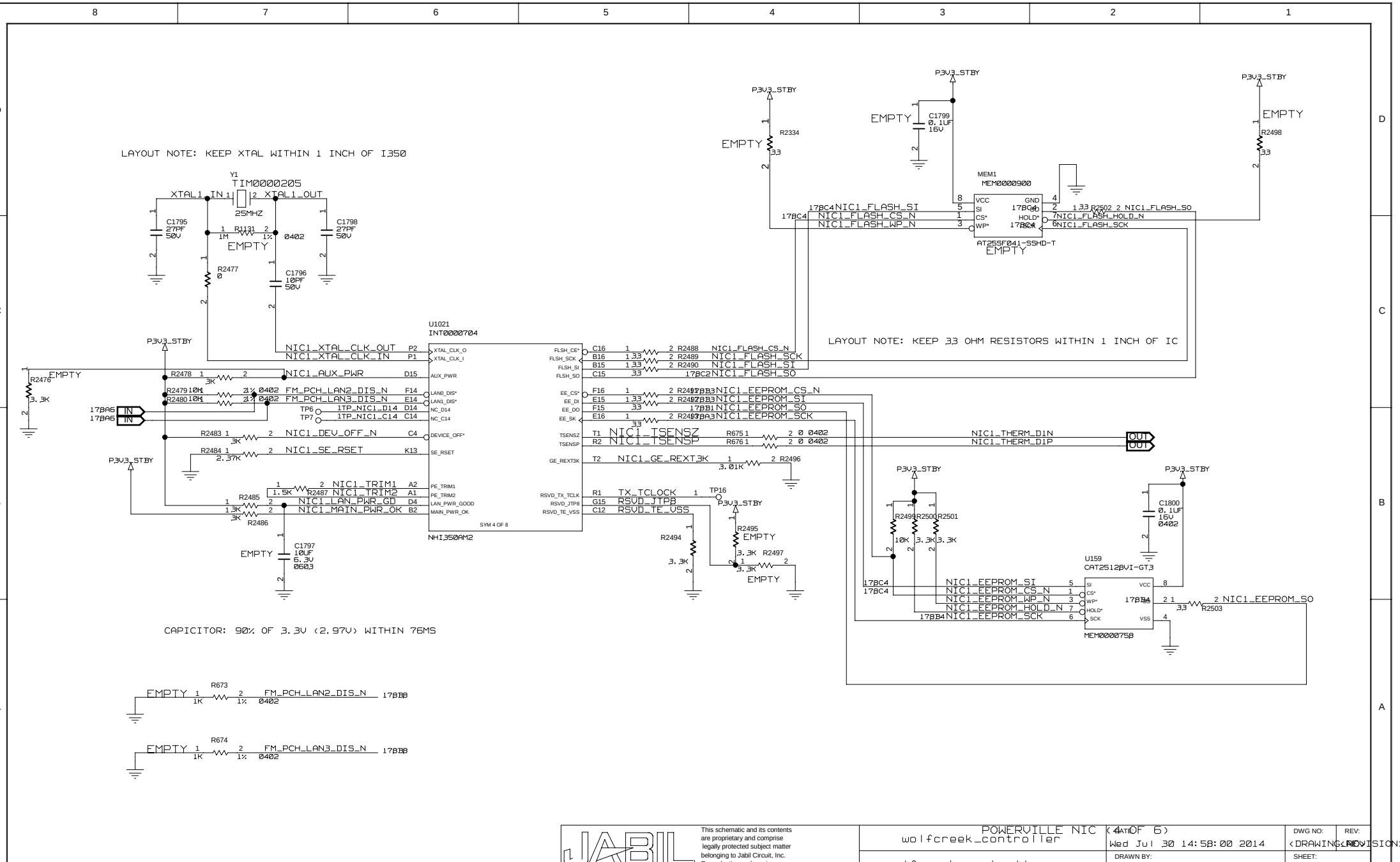
POWERVILLE NIC wolfcreek_controller	<3 OF 6>	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DATE: Wed Jul 30 14:58:00 2014	DRAWN BY: <ENGINEER>	SHEET: 177OF360



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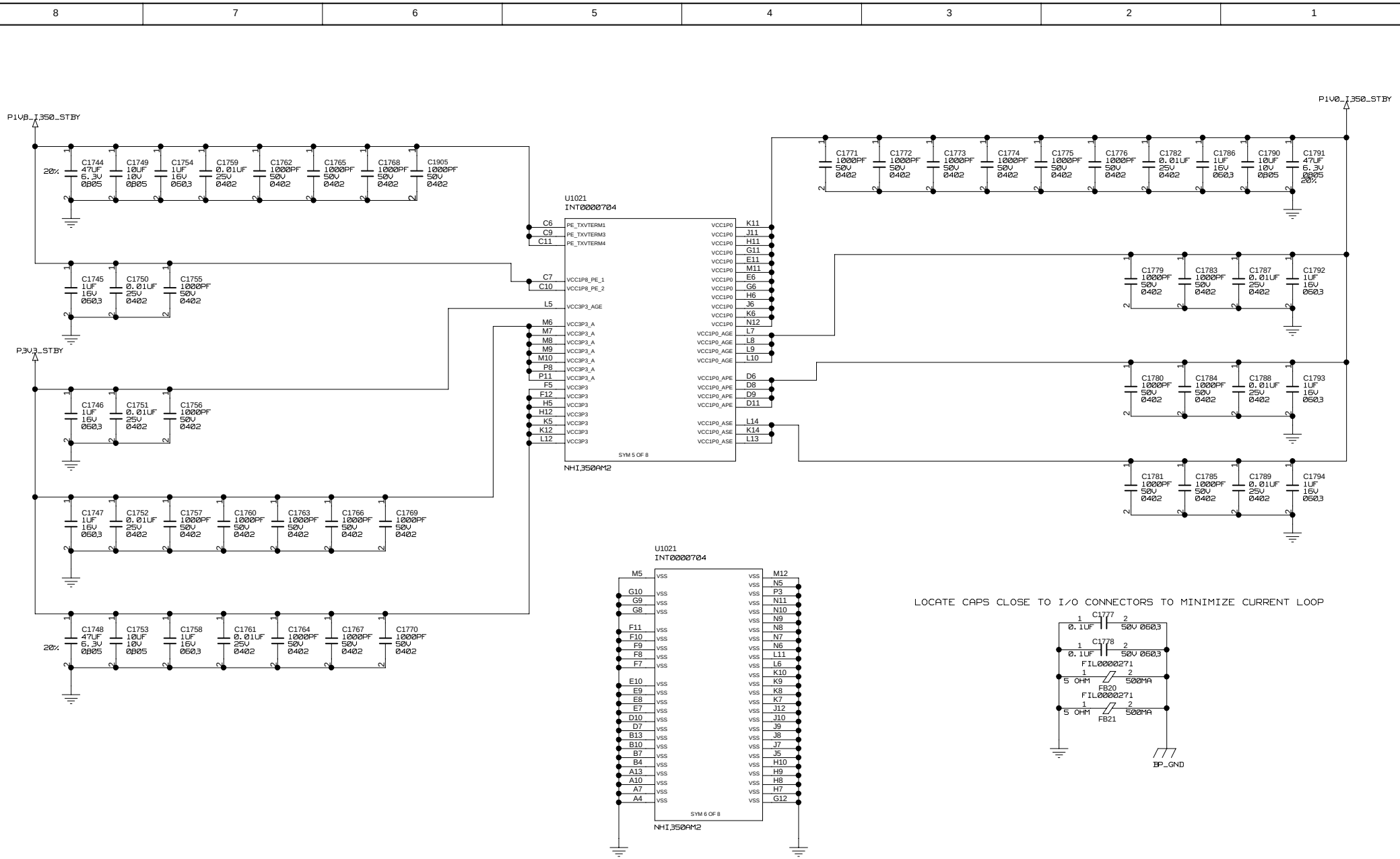
POWERVILLE NIC (4 OF 6)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Wed Jul 30 14:58:00 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: 17B OF 36B



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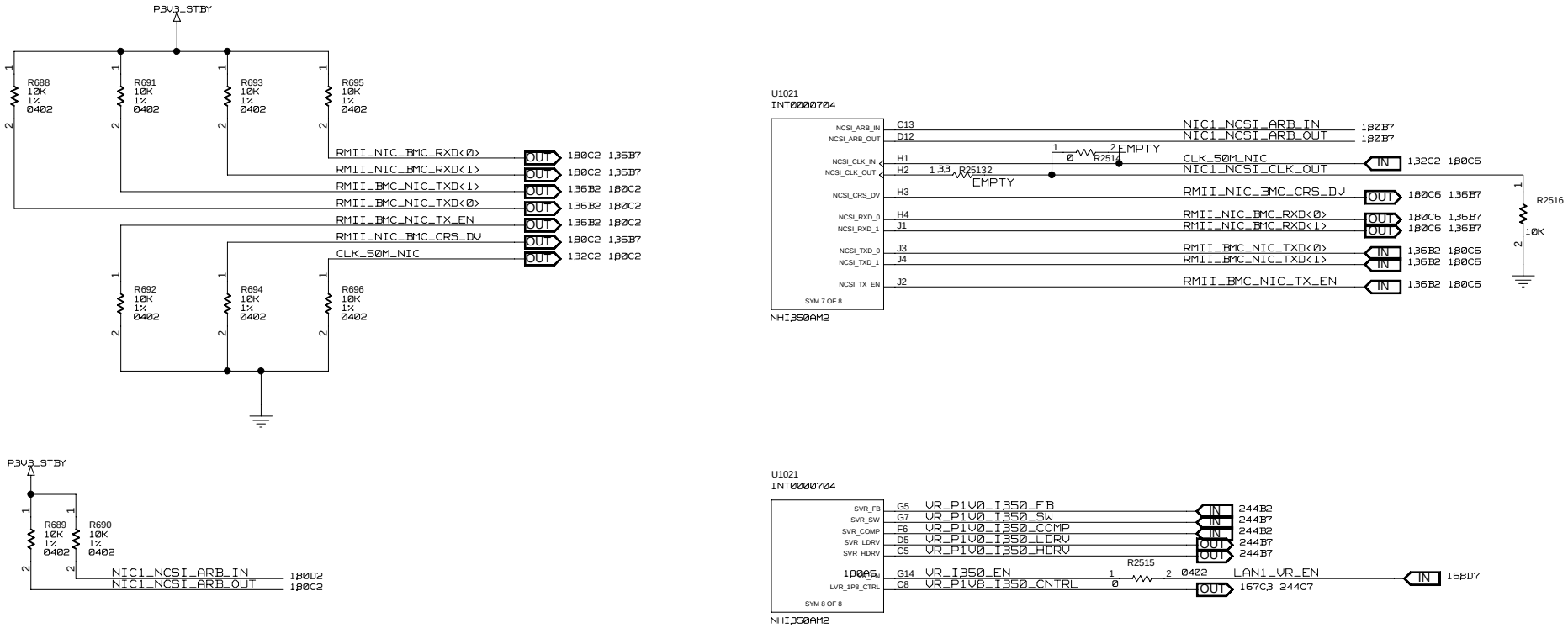
POWERVILLE NIC (5 OF 6) wolfcreek_controller	DATE: Wed Jul 30 14:59:38 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 179OF360	



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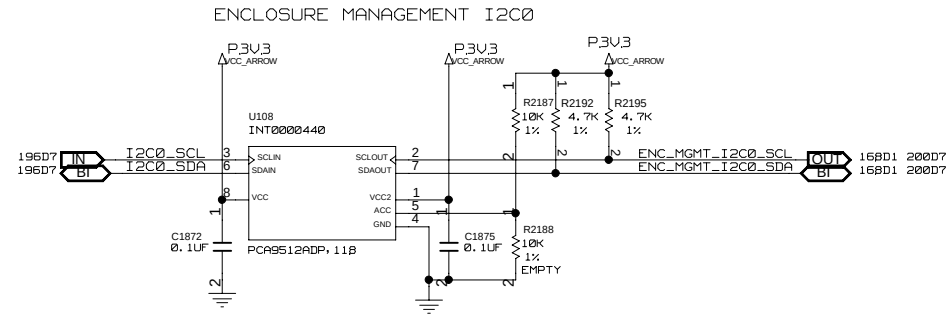
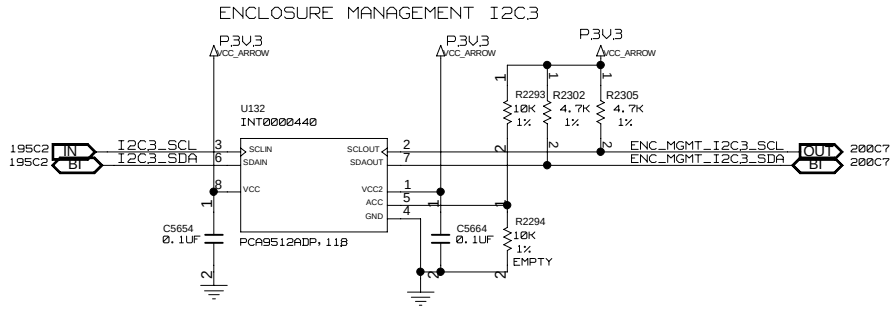
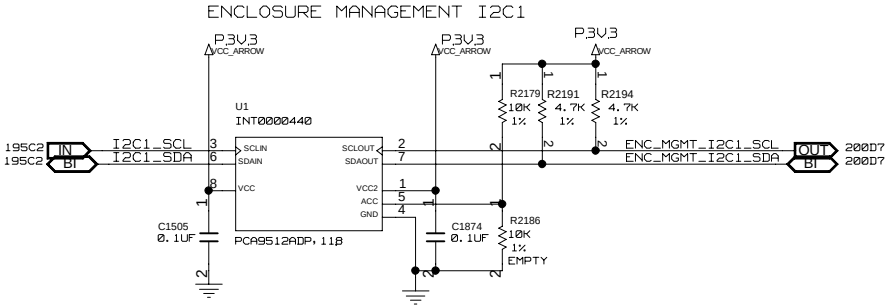
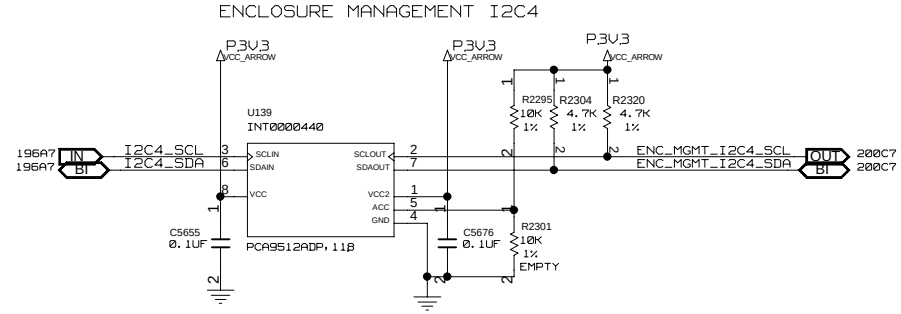
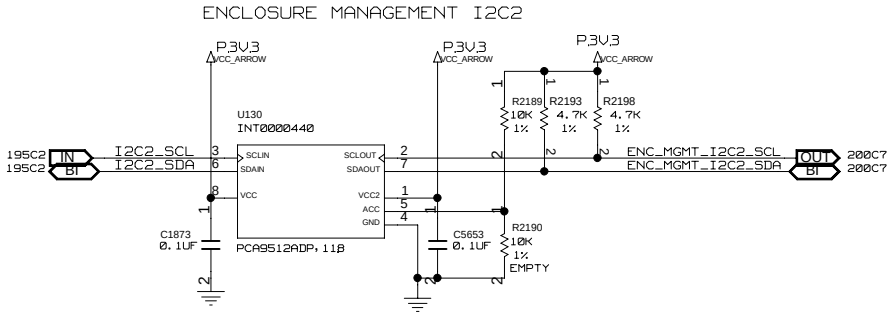
POWERVILLE NIC1 (6 OF 6)	DATE: Wed Jul 30 14:58:01 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 100F360	

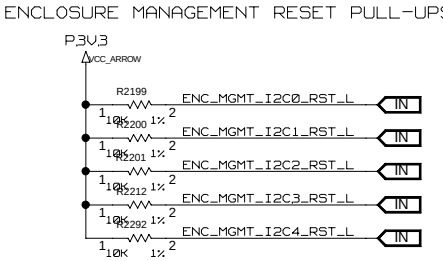












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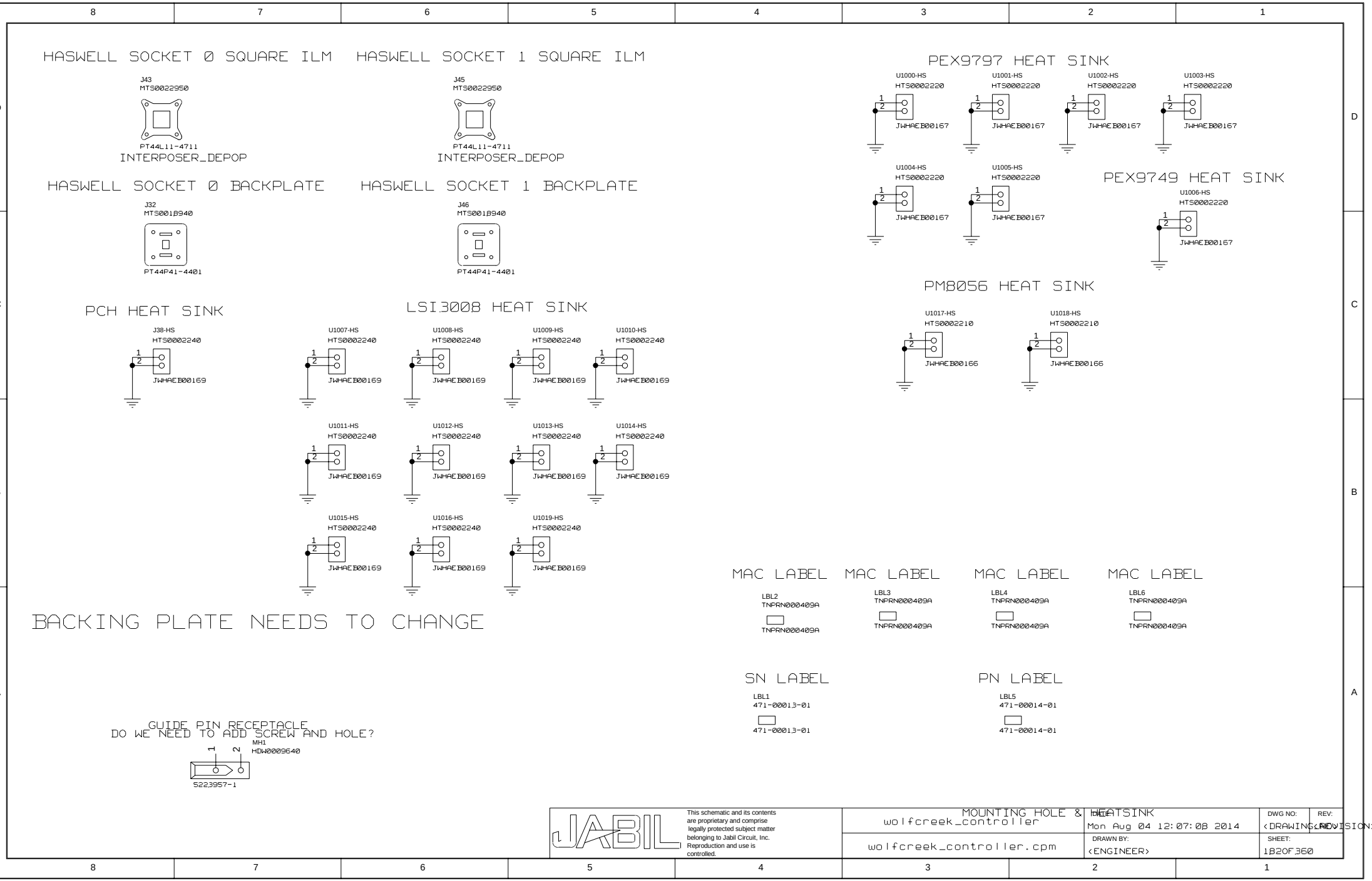
BLANK wolfcreek_controller	DATE: Wed Jul 30 14:58:08 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 1B1OF360	


HASWELL SOCKET 0 SQUARE ILM
J43
MTS0022950
PT44L11-4711
INTERPOSER_DEPOP
HASWELL SOCKET 1 SQUARE ILM
J45
MTS0022950
PT44L11-4711
INTERPOSER_DEPOP
HASWELL SOCKET 0 BACKPLATE
J32
MTS0018940
PT44P41-4401
HASWELL SOCKET 1 BACKPLATE
J46
MTS0018940
PT44P41-4401
PEX9797 HEAT SINK
U1000-HS
HTS0002220
JWHAEB00167
U1001-HS
HTS0002220
JWHAEB00167
U1002-HS
HTS0002220
JWHAEB00167
U1003-HS
HTS0002220
JWHAEB00167
U1004-HS
HTS0002220
JWHAEB00167
U1005-HS
HTS0002220
JWHAEB00167
PEX9749 HEAT SINK
U1006-HS
HTS0002220
JWHAEB00167
PM8056 HEAT SINK
U1017-HS
HTS0002210
JWHAEB00166
U1018-HS
HTS0002210
JWHAEB00166
PCH HEAT SINK
J38-HS
HTS0002240
JWHAEB00169
LSI3008 HEAT SINK
U1007-HS
HTS0002240
JWHAEB00169
U1008-HS
HTS0002240
JWHAEB00169
U1009-HS
HTS0002240
JWHAEB00169
U1010-HS
HTS0002240
JWHAEB00169
U1011-HS
HTS0002240
JWHAEB00169
U1012-HS
HTS0002240
JWHAEB00169
U1013-HS
HTS0002240
JWHAEB00169
U1014-HS
HTS0002240
JWHAEB00169
U1015-HS
HTS0002240
JWHAEB00169
U1016-HS
HTS0002240
JWHAEB00169
U1019-HS
HTS0002240
JWHAEB00169
BACKING PLATE NEEDS TO CHANGE
MAC LABEL
LBL2
TNPRN000409A
TNPRN000409A
MAC LABEL
LBL3
TNPRN000409A
TNPRN000409A
MAC LABEL
LBL4
TNPRN000409A
TNPRN000409A
MAC LABEL
LBL6
TNPRN000409A
TNPRN000409A
SN LABEL
LBL1
471-00013-01
471-00013-01
PN LABEL
LBL5
471-00014-01
471-00014-01
GUIDE PIN RECEPTACLE
DO WE NEED TO ADD SCREW AND HOLE?
MH1
HDW0009640
1
2
5223957-1
JABIL
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MOUNTING HOLE & HEATSINK
wolfcreek_controller
DATE:
Mon Aug 04 12:07:08 2014
DWG NO:
<DRAWING NO>
REV:
<REVISION>
wolfcreek_controller.cpm
DRAWN BY:
<ENGINEER>
SHEET:
182OF360

U1007

SAS_3008

199D4 IN IOC1_MS1_INT_L_1V8 → MINISAS1_INT_L
MINISAS2_INT_L
199D5 IN IOC1_MS1_MODPRES_L_1V8 → MINISAS1_MODPRES_L
MINISAS2_MODPRES_L
MINISAS1_VACT_OC
MINISAS2_VACT_OC

MINISAS1_AMBER → IOC1_MS1_AMBER OUT 221B3
MINISAS1_GREEN → IOC1_MS1_GREEN OUT 221B6
MINISAS1_VACT → IOC1_MS1_VACT_L_1V8 OUT
MINISAS1_VMAN → IOC1_MS1_VMAN_L_1V8 OUT
MINISAS2_AMBER
MINISAS2_GREEN
MINISAS2_VACT
MINISAS2_VMAN

164D3 IN IOC1_UART_RX → UART0_RX
164D8 OUT IOC1_UART_TX → UART0_TX

IIC0_SDA → U1007_MS_SCL_1V8 OUT 1B3C3
IIC0_SCL → U1007_MS_SDA_1V8 OUT 1B3D3
IIC1_SCL
IIC1_SDA

169B1 IN LSI0_SYS_RST_N0 → SYS_RST_N0

SAS_TX+<7..0> → U1007_TX+<7..0> → 7..4 SAS_U1007_MS_DP<3..0> OUT 221C1; 3..0 SAS_U1007_U1017_DP<3..0> OUT 200D8
SAS_TX-<7..0> → U1007_TX-<7..0> → 7..4 SAS_U1007_MS_DN<3..0> OUT 221C1; 3..0 SAS_U1007_U1017_DN<3..0> OUT 200C8

205D3 IN CK_100M_IOC1_DP → PCE_REF_CLK+
205D3 IN CK_100M_IOC1_DN → PCE_REF_CLK-

SAS_RX+<7..0> → U1007_RX+<7..0> → 7..4 SAS_MS_U1007_DP<3..0> IN 221B8; 3..0 SAS_U1017_U1007_DP<3..0> IN 200D1
SAS_RX-<7..0> → U1007_RX-<7..0> → 7..4 SAS_MS_U1007_DN<3..0> IN 221B8; 3..0 SAS_U1017_U1007_DN<3..0> IN 200C1

210B1 OUT PE_U1007_U1000_DP<7..0> → PCE_TX+<7..0>
210B1 OUT PE_U1007_U1000_DN<7..0> → PCE_TX-<7..0>

210C1 IN PE_U1000_U1007_DP<7..0> → PCE_RX+<7..0>
210D1 IN PE_U1000_U1007_DN<7..0> → PCE_RX-<7..0>

1B9A7 1B8A7 1B7A7 1B6A7 1B5A7 1B4A7 167C3 249A3 193A8 192A7 191A7 190A7 IN P1V8_LSI_PG → P1V8_PG

1B6A7 1B5A7 1B4A7 167A3 IN LSI_P0V9_0_EN → P0V9_EN
166C4 OUT LSI_P0V9_0_PG → P0V9_PG

P1V8_LSI
R3501 1K
C6122 0.1UF 16V 0402
P3V3 VCC_ARROW
R3503 4.7K
1B3C3 U1007_MS_SDA_1V8 → U1007_MS_SDA_3V3 OUT 221C2
TRN00005B2 NTJD4001NT1G Q63

P1V8_LSI
R3500 1K
C6121 0.1UF 16V 0402
P3V3 VCC_ARROW
R3502 4.7K
1B3C3 U1007_MS_SCL_1V8 → U1007_MS_SCL_3V3 OUT 221D2
TRN00005B2 NTJD4001NT1G Q63

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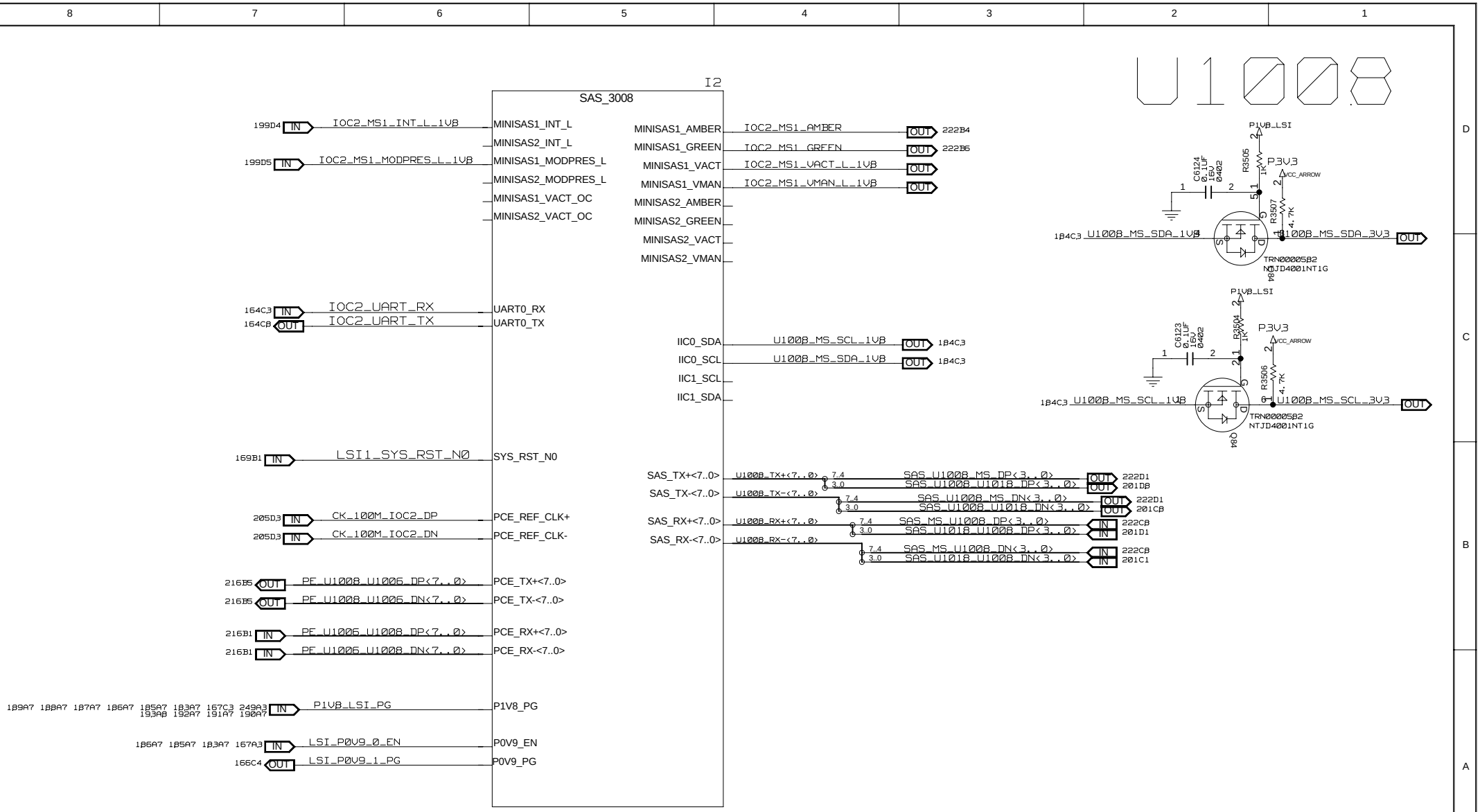
CHANGE HISTORY 1

wolfcreek_controller	DATE: Thu Aug 07 16:58:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 1B30F360	



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CHANGE HISTORY 11	DATE: Thu Aug 07 16:58:30 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 184OF360	

U1009

I3

SAS_3008

199D4 IN IOC3_MS1_INT_L_1V8 → MINISAS1_INT_L
MINISAS2_INT_L
199D5 IN IOC3_MS1_MODPRES_L_1V8 → MINISAS1_MODPRES_L
MINISAS2_MODPRES_L
MINISAS1_VACT_OC
MINISAS2_VACT_OC

MINISAS1_AMBER → IOC3_MS1_AMBER OUT 221B3
MINISAS1_GREEN → IOC3_MS1_GREEN OUT 221B6
MINISAS1_VACT → IOC3_MS1_VACT_L_1V8 OUT
MINISAS1_VMAN → IOC3_MS1_VMAN_L_1V8 OUT
MINISAS2_AMBER
MINISAS2_GREEN
MINISAS2_VACT
MINISAS2_VMAN

164C3 IN IOC3_UART_RX → UART0_RX
164C8 OUT IOC3_UART_TX → UART0_TX

IIC0_SDA → U1009_MS_SCL_1V8 OUT 185B3
IIC0_SCL → U1009_MS_SDA_1V8 OUT 185C3
IIC1_SCL
IIC1_SDA

169B1 IN LSI2_SYS_RST_N0 → SYS_RST_N0

205C3 IN CK_100M_IOC3_DP → PCE_REF_CLK+
205C3 IN CK_100M_IOC3_DN → PCE_REF_CLK-

210B1 OUT PE_U1009_U1000_DP<7..0> → PCE_TX+<7..0>
210B1 OUT PE_U1009_U1000_DN<7..0> → PCE_TX-<7..0>

210C1 IN PE_U1000_U1009_DP<7..0> → PCE_RX+<7..0>
210D1 IN PE_U1000_U1009_DN<7..0> → PCE_RX-<7..0>

188A7 187A7 186A7 184A7 183A7 167C3 249A3 193A8 192A7 191A7 190A7 189A7 IN P1V8_LSI_PG → P1V8_PG

186A7 184A7 183A7 167A3 IN LSI_P0V9_0_EN → P0V9_EN
166C4 OUT LSI_P0V9_2_PG → P0V9_PG

SAS_TX+<7..0> → U1009_TX+<7..0> 7..4 / 3..0 → SAS_U1009_MS_DP<3..0> OUT 221D1; SAS_U1009_U1017_DP<3..0> OUT 200D8
SAS_TX-<7..0> → U1009_TX-<7..0> 7..4 / 3..0 → SAS_U1009_MS_DN<3..0> OUT 221D1; SAS_U1009_U1017_DN<3..0> OUT 200C8
SAS_RX+<7..0> → U1009_RX+<7..0> 7..4 / 3..0 → SAS_MS_U1009_DP<3..0> IN 221C8; SAS_U1017_U1009_DP<3..0> IN 200D1
SAS_RX-<7..0> → U1009_RX-<7..0> 7..4 / 3..0 → SAS_MS_U1009_DN<3..0> IN 221C8; SAS_U1017_U1009_DN<3..0> IN 200C1

P1V8_LSI
C6126 0.1UF 16V 0402
R3509 1K
P3V3 VCC_ARROW
R3511 4.7K
185C3 U1009_MS_SDA_1V8 → U1009_MS_SDA_3V3 OUT 221D2
TRN00005B2 NTJD4001NT1G Q85

P1V8_LSI
C6125 0.1UF 16V 0402
R3508 1K
P3V3 VCC_ARROW
R3510 4.7K
185C3 U1009_MS_SCL_1V8 → U1009_MS_SCL_3V3 OUT 221D2
TRN00005B2 NTJD4001NT1G Q85

CHANGE HISTORY 1.1

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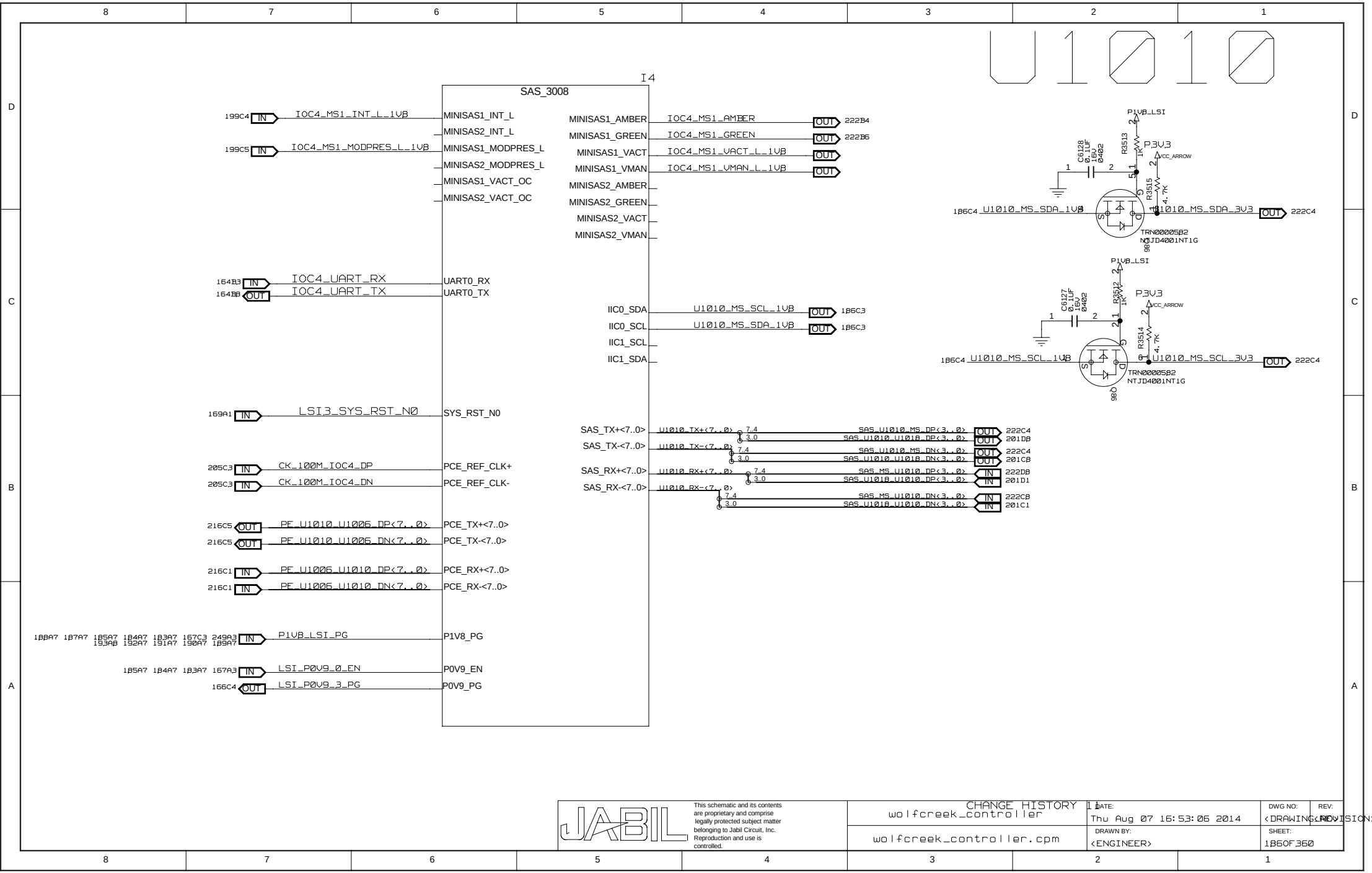
wolfcreek_controller	DATE: Thu Aug 07 16:58:52 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 185OF360	



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CHANGE HISTORY 1

wolfcreek_controller	DATE: Thu Aug 07 16:53:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 186OF360	

U1011

I5

SAS_3008

199C4 IN IOC5_MS1_INT_L_1V8 → MINISAS1_INT_L
MINISAS2_INT_L
199C5 IN IOC5_MS1_MODPRES_L_1V8 → MINISAS1_MODPRES_L
MINISAS2_MODPRES_L
MINISAS1_VACT_OC
MINISAS2_VACT_OC

MINISAS1_AMBER → IOC5_MS1_AMBER OUT 221A3
MINISAS1_GREEN → IOC5_MS1_GREEN OUT 221A6
MINISAS1_VACT → IOC5_MS1_VACT_L_1V8 OUT
MINISAS1_VMAN → IOC5_MS1_VMAN_L_1V8 OUT
MINISAS2_AMBER
MINISAS2_GREEN
MINISAS2_VACT
MINISAS2_VMAN

164B3 IN IOC5_UART_RX → UART0_RX
164B8 OUT IOC5_UART_TX → UART0_TX

IIC0_SDA → U1011_MS_SCL_1V8 OUT 187C3
IIC0_SCL → U1011_MS_SDA_1V8 OUT 187C3
IIC1_SCL
IIC1_SDA

169A1 IN LSI4_SYS_RST_N0 → SYS_RST_N0

SAS_TX+<7..0> → U1011_TX+<7..0> → 7..4 SAS_U1011_MS_DP<3..0> OUT 221C4; 3..0 SAS_U1011_U1017_DP<3..0> OUT 200D8
SAS_TX-<7..0> → U1011_TX-<7..0> → 7..4 SAS_U1011_MS_DN<3..0> OUT 221C4; 3..0 SAS_U1011_U1017_DN<3..0> OUT 200C8
SAS_RX+<7..0> → U1011_RX+<7..0> → 7..4 SAS_MS_U1011_DP<3..0> IN 221D8; 3..0 SAS_U1017_U1011_DP<3..0> IN 200D1
SAS_RX-<7..0> → U1011_RX-<7..0> → 7..4 SAS_MS_U1011_DN<3..0> IN 221C8; 3..0 SAS_U1017_U1011_DN<3..0> IN 200C1

205E1 IN CK_100M_IOC5_DP → PCE_REF_CLK+
205E1 IN CK_100M_IOC5_DN → PCE_REF_CLK-

210B1 OUT PE_U1011_U1000_DP<7..0> → PCE_TX+<7..0>
210B1 OUT PE_U1011_U1000_DN<7..0> → PCE_TX-<7..0>

210C1 IN PE_U1000_U1011_DP<7..0> → PCE_RX+<7..0>
210D1 IN PE_U1000_U1011_DN<7..0> → PCE_RX-<7..0>

189A7 188A7 186A7 185A7 184A7 183A7 167C3 249A3 193A8 192A7 191A7 190A7 IN P1V8_LSI_PG → P1V8_PG

190A7 189A7 188A7 167A3 IN LSI_P0V9_1_EN → P0V9_EN
166C4 OUT LSI_P0V9_4_PG → P0V9_PG

P1V8_LSI
R3517 1K
C6130 0.1UF 16V 0402
P3V3 VCC_ARROW
R3519 4.7K
187C3 U1011_MS_SDA_1V8 → U1011_MS_SDA_3V3 OUT 221C4
Q87 TRN00005B2 NTJD4001NT1G

P1V8_LSI
R3516 1K
C6129 0.1UF 16V 0402
P3V3 VCC_ARROW
R3518 4.7K
187C3 U1011_MS_SCL_1V8 → U1011_MS_SCL_3V3 OUT 221C4
Q87 TRN00005B2 NTJD4001NT1G

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CHANGE HISTORY 1.1

wolfcreek_controller	DATE: Thu Aug 07 16:59:03 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 187OF,360	

U1012

I6

SAS_3008

199C4 IN IOC6_MS1_INT_L_1V8 — MINISAS1_INT_L
MINISAS2_INT_L
199C5 IN IOC6_MS1_MODPRES_L_1V8 — MINISAS1_MODPRES_L
MINISAS2_MODPRES_L
MINISAS1_VACT_OC
MINISAS2_VACT_OC

164A3 IN IOC6_UART_RX — UART0_RX
164A8 OUT IOC6_UART_TX — UART0_TX

169A1 IN LSI5_SYS_RST_N0 — SYS_RST_N0

205E1 IN CK_100M_IOC6_DP — PCE_REF_CLK+
205E1 IN CK_100M_IOC6_DN — PCE_REF_CLK-

211B1 OUT PE_U1012_U1001_DP<7..0> — PCE_TX+<7..0>
211B1 OUT PE_U1012_U1001_DN<7..0> — PCE_TX-<7..0>

211C1 IN PE_U1001_U1012_DP<7..0> — PCE_RX+<7..0>
211D1 IN PE_U1001_U1012_DN<7..0> — PCE_RX-<7..0>

189A7 187A7 186A7 185A7 184A7 183A7 167C3 249A3 193A8 192A7 191A7 190A7 IN P1V8_LSI_PG — P1V8_PG

190A7 189A7 187A7 167A3 IN LSI_P0V9_1_EN — P0V9_EN
166C4 OUT LSI_P0V9_5_PG — P0V9_PG

MINISAS1_AMBER — IOC6_MS1_AMBER — OUT 222A4
MINISAS1_GREEN — IOC6_MS1_GREEN — OUT 222A6
MINISAS1_VACT — IOC6_MS1_VACT_L_1V8 — OUT
MINISAS1_VMAN — IOC6_MS1_VMAN_L_1V8 — OUT
MINISAS2_AMBER
MINISAS2_GREEN
MINISAS2_VACT
MINISAS2_VMAN

IIC0_SDA — U1012_MS_SCL_1V8 — OUT 180C3
IIC0_SCL — U1012_MS_SDA_1V8 — OUT 180C3
IIC1_SCL
IIC1_SDA

SAS_TX+<7..0> — U1012_TX+<7..0> — 7..4 SAS_U1012_MS_DP<3..0> OUT 222D4; 3..0 SAS_U1012_U1018_DP<3..0> OUT 201D8
SAS_TX-<7..0> — U1012_TX-<7..0> — 7..4 SAS_U1012_MS_DN<3..0> OUT 222D4; 3..0 SAS_U1012_U1018_DN<3..0> OUT 201C8
SAS_RX+<7..0> — U1012_RX+<7..0> — 7..4 SAS_MS_U1012_DP<3..0> IN 222D8; 3..0 SAS_U1018_U1012_DP<3..0> IN 201D1
SAS_RX-<7..0> — U1012_RX-<7..0> — 7..4 SAS_MS_U1012_DN<3..0> IN 222D8; 3..0 SAS_U1018_U1012_DN<3..0> IN 201C1

P1V8_LSI
C6132 0.1UF 16V 0402
R3521 1K
P3V3 VCC_ARROW
R3523 4.7K
180C3 U1012_MS_SDA_1V8 — U1012_MS_SDA_3V3 OUT 222D4
TRN00005B2 NTJD4001NT1G Q113

P1V8_LSI
C6131 0.1UF 16V 0402
R3520 1K
P3V3 VCC_ARROW
R3522 4.7K
180C3 U1012_MS_SCL_1V8 — U1012_MS_SCL_3V3 OUT 222D4
TRN00005B2 NTJD4001NT1G Q113

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		wolfcreek_controller	DRAWN BY: <ENGINEER>	SHEET: 180 OF 360	
		wolfcreek_controller.cpm			

U1013

I7

SAS_3008

199B4	IN	IOC7_MS1_INT_L_1V8	MINISAS1_INT_L		
			MINISAS2_INT_L		
199B5	IN	IOC7_MS1_MODPRES_L_1V8	MINISAS1_MODPRES_L		
			MINISAS2_MODPRES_L		
			MINISAS1_VACT_OC		
			MINISAS2_VACT_OC		
			MINISAS1_AMBER	IOC7_MS1_AMBER	OUT 221A3
			MINISAS1_GREEN	IOC7_MS1_GREEN	OUT 221A6
			MINISAS1_VACT	IOC7_MS1_VACT_L_1V8	OUT
			MINISAS1_VMAN	IOC7_MS1_VMAN_L_1V8	OUT
			MINISAS2_AMBER		
			MINISAS2_GREEN		
			MINISAS2_VACT		
			MINISAS2_VMAN		
164D1	IN	IOC7_UART_RX	UART0_RX		
164D6	OUT	IOC7_UART_TX	UART0_TX		
			IIC0_SDA	U1013_MS_SCL_1V8	OUT 189C3
			IIC0_SCL	U1013_MS_SDA_1V8	OUT 189C3
			IIC1_SCL		
			IIC1_SDA		
169A1	IN	LSI6_SYS_RST_N0	SYS_RST_N0		
			SAS_TX+<7..0>	U1013_TX+<7..0>	7.4 SAS_U1013_MS_DP<3..0> OUT 221D4; 3.0 SAS_U1013_U1017_DP<3..0> OUT 200D8
			SAS_TX-<7..0>	U1013_TX-<7..0>	7.4 SAS_U1013_MS_DN<3..0> OUT 221D4; 3.0 SAS_U1013_U1017_DN<3..0> OUT 200C8
205D1	IN	CK_100M_IOC7_DP	PCE_REF_CLK+		
205D1	IN	CK_100M_IOC7_DN	PCE_REF_CLK-		
			SAS_RX+<7..0>	U1013_RX+<7..0>	7.4 SAS_MS_U1013_DP<3..0> IN 221D8; 3.0 SAS_U1017_U1013_DP<3..0> IN 200D1
			SAS_RX-<7..0>	U1013_RX-<7..0>	7.4 SAS_MS_U1013_DN<3..0> IN 221D8; 3.0 SAS_U1017_U1013_DN<3..0> IN 200C1
210B1	OUT	PE_U1013_U1000_DP<7..0>	PCE_TX+<7..0>		
210B1	OUT	PE_U1013_U1000_DN<7..0>	PCE_TX-<7..0>		
210C1	IN	PE_U1000_U1013_DP<7..0>	PCE_RX+<7..0>		
210D1	IN	PE_U1000_U1013_DN<7..0>	PCE_RX-<7..0>		
185A7 185A7 184A7 183A7 167C3 249A3 193A8 192A7 191A7 190A7 188A7 187A7	IN	P1V8_LSI_PG	P1V8_PG		
190A7 188A7 187A7 167A3	IN	LSI_P0V9_1_EN	P0V9_EN		
166C4	OUT	LSI_P0V9_6_PG	P0V9_PG		

U1013_MS_SDA_1V8 → U1013_MS_SDA_3V3

P1V8_LSI; C6134 0.1UF 16V 0402; R3525 1K; P3V3 (VCC_ARROW); R3527 4.7K; Q114 TRN00005B2 NTJD4001NT1G

189C4 U1013_MS_SDA_1V8 → U1013_MS_SDA_3V3 OUT 221D4

U1013_MS_SCL_1V8 → U1013_MS_SCL_3V3

P1V8_LSI; C6133 0.1UF 16V 0402; R3524 1K; P3V3 (VCC_ARROW); R3526 4.7K; Q114 TRN00005B2 NTJD4001NT1G

189C4 U1013_MS_SCL_1V8 → U1013_MS_SCL_3V3 OUT 221D4

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CHANGE HISTORY 1

wolfcreek_controller	DATE: Thu Aug 07 16:59:30 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 189 OF 360	

U1014

I8

SAS_3008

199B4 IN — IOC8_MS1_INT_L_1V8 — MINISAS1_INT_L
MINISAS2_INT_L
199B5 IN — IOC8_MS1_MODPRES_L_1V8 — MINISAS1_MODPRES_L
MINISAS2_MODPRES_L
MINISAS1_VACT_OC
MINISAS2_VACT_OC

MINISAS1_AMBER — IOC8_MS1_AMBER — OUT 223B3
MINISAS1_GREEN — IOC8_MS1_GREEN — OUT 223B5
MINISAS1_VACT — IOC8_MS1_VACT_L_1V8 — OUT
MINISAS1_VMAN — IOC8_MS1_VMAN_L_1V8 — OUT
MINISAS2_AMBER
MINISAS2_GREEN
MINISAS2_VACT
MINISAS2_VMAN

164C1 IN — IOC8_UART_RX — UART0_RX
164C6 OUT — IOC8_UART_TX — UART0_TX

IIC0_SDA — U1014_MS_SCL_1V8 — OUT 190C3
IIC0_SCL — U1014_MS_SDA_1V8 — OUT 190C3
IIC1_SCL
IIC1_SDA

169A1 IN — LSI7_SYS_RST_N0 — SYS_RST_N0

SAS_TX+<7..0> — U1014_TX+<7..0> — 7..4 SAS_U1014_MS_DP<3..0> — OUT 223C4; 3..0 SAS_U1014_U1018_DP<3..0> — OUT 201D8
SAS_TX-<7..0> — U1014_TX-<7..0> — 7..4 SAS_U1014_MS_DN<3..0> — OUT 223C4; 3..0 SAS_U1014_U1018_DN<3..0> — OUT 201C8

205D1 IN — CK_100M_IOC8_DP — PCE_REF_CLK+
205D1 IN — CK_100M_IOC8_DN — PCE_REF_CLK-

SAS_RX+<7..0> — U1014_RX+<7..0> — 7..4 SAS_MS_U1014_DP<3..0> — IN 223D8; 3..0 SAS_U1018_U1014_DP<3..0> — IN 201D1
SAS_RX-<7..0> — U1014_RX-<7..0> — 7..4 SAS_MS_U1014_DN<3..0> — IN 223C8; 3..0 SAS_U1018_U1014_DN<3..0> — IN 201C1

211B1 OUT — PE_U1014_U1001_DP<7..0> — PCE_TX+<7..0>
211B1 OUT — PE_U1014_U1001_DN<7..0> — PCE_TX-<7..0>

211C1 IN — PE_U1001_U1014_DP<7..0> — PCE_RX+<7..0>
211D1 IN — PE_U1001_U1014_DN<7..0> — PCE_RX-<7..0>

188A7 187A7 186A7 185A7 184A7 183A7 167C3 249A3 193A8 192A7 191A7 189A7 IN — P1V8_LSI_PG — P1V8_PG

189A7 188A7 187A7 167A3 IN — LSI_P0V9_1_EN — P0V9_EN
166C4 OUT — LSI_P0V9_7_PG — P0V9_PG

P1V8_LSI
R3529 1K
C6136 0.1UF 16V 0402
P3V3 VCC_ARROW
R3531 4.7K
190C3 U1014_MS_SDA_1V8 — U1014_MS_SDA_3V3 — OUT 223C4
TRN00005B2 NTJD4001NT1G Q117

P1V8_LSI
R3528 1K
C6135 0.1UF 16V 0402
P3V3 VCC_ARROW
R3530 4.7K
190C3 U1014_MS_SCL_1V8 — U1014_MS_SCL_3V3 — OUT 223C4
TRN00005B2 NTJD4001NT1G Q117

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CHANGE HISTORY 1

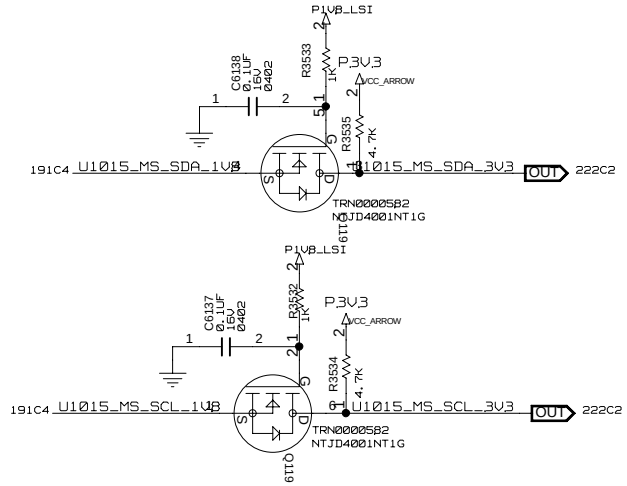
wolfcreek_controller	DATE: Thu Aug 07 16:56:30 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 190OF,360	

U1015

I9

SAS_3008

199B4 IN	IOC9_MS1_INT_L_1V8	MINISAS1_INT_L	MINISAS1_AMBER	IOC9_MS1_AMBER	OUT 222A4
		MINISAS2_INT_L	MINISAS1_GREEN	IOC9_MS1_GREEN	OUT 222A6
199B5 IN	IOC9_MS1_MODPRES_L_1V8	MINISAS1_MODPRES_L	MINISAS1_VACT	IOC9_MS1_VACT_L_1V8	OUT
		MINISAS2_MODPRES_L	MINISAS1_VMAN	IOC9_MS1_VMAN_L_1V8	OUT
		MINISAS1_VACT_OC	MINISAS2_AMBER		
		MINISAS2_VACT_OC	MINISAS2_GREEN		
			MINISAS2_VACT		
			MINISAS2_VMAN		
164C1 IN	IOC9_UART_RX	UART0_RX			
164C6 OUT	IOC9_UART_TX	UART0_TX			
			IIC0_SDA	U1015_MS_SCL_1V8	OUT 191C3
			IIC0_SCL	U1015_MS_SDA_1V8	OUT 191C3
			IIC1_SCL		
			IIC1_SDA		
169A1 IN	LSI8_SYS_RST_N0	SYS_RST_N0			
			SAS_TX+<7..0>	U1015_TX+<7..0>	7..4 SAS_U1015_MS_DP<3..0> OUT 222C1; 3..0 SAS_U1015_U1017_DP<3..0> OUT 200D8
			SAS_TX-<7..0>	U1015_TX-<7..0>	7..4 SAS_U1015_MS_DN<3..0> OUT 222C1; 3..0 SAS_U1015_U1017_DN<3..0> OUT 200C8
205C1 IN	CK_100M_IOC9_DP	PCE_REF_CLK+			
205C1 IN	CK_100M_IOC9_DN	PCE_REF_CLK-			
			SAS_RX+<7..0>	U1015_RX+<7..0>	7..4 SAS_MS_U1015_DP<3..0> IN 222B8; 3..0 SAS_U1017_U1015_DP<3..0> IN 200D1
			SAS_RX-<7..0>	U1015_RX-<7..0>	7..4 SAS_MS_U1015_DN<3..0> IN 222B9; 3..0 SAS_U1017_U1015_DN<3..0> IN 200C1
216D5 OUT	PE_U1015_U1006_DP<7..0>	PCE_TX+<7..0>			
216D5 OUT	PE_U1015_U1006_DN<7..0>	PCE_TX-<7..0>			
216D1 IN	PE_U1006_U1015_DP<7..0>	PCE_RX+<7..0>			
216D1 IN	PE_U1006_U1015_DN<7..0>	PCE_RX-<7..0>			
187A7 186A7 185A7 184A7 183A7 167C3 249A3 193A8 192A7 190A7 189A7 188A7 IN	P1V8_LSI_PG	P1V8_PG			
193A8 192A7 167A3 IN	LSI_P0V9_2_EN	P0V9_EN			
166C4 OUT	LSI_P0V9_8_PG	P0V9_PG			



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CHANGE HISTORY 1

wolfcreek_controller	DATE: Thu Aug 07 16:59:41 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 191OF,360	

U1016

I10

SAS_3008

199A4 IN IOC10_MS1_INT_L_1V8 → MINISAS1_INT_L
MINISAS2_INT_L
199A5 IN IOC10_MS1_MODPRES_L_1V8 → MINISAS1_MODPRES_L
MINISAS2_MODPRES_L
MINISAS1_VACT_OC
MINISAS2_VACT_OC

MINISAS1_AMBER — IOC10_MS1_AMBER — OUT 223B3
MINISAS1_GREEN — IOC10_MS1_GREEN — OUT 223B6
MINISAS1_VACT — IOC10_MS1_VACT_L_1V8 — OUT
MINISAS1_VMAN — IOC10_MS1_VMAN_L_1V8 — OUT
MINISAS2_AMBER
MINISAS2_GREEN
MINISAS2_VACT
MINISAS2_VMAN

164B1 IN IOC10_UART_RX → UART0_RX
164B6 OUT IOC10_UART_TX → UART0_TX

IIC0_SDA — U1016_MS_SCL_1V8 — OUT 192B3
IIC0_SCL — U1016_MS_SDA_1V8 — OUT 192C3
IIC1_SCL
IIC1_SDA

169A1 IN LSI9_SYS_RST_N0 → SYS_RST_N0

205C1 IN CK_100M_IOC10_DP → PCE_REF_CLK+
205C1 IN CK_100M_IOC10_DN → PCE_REF_CLK-

211B1 OUT PE_U1016_U1001_DP<7..0> → PCE_TX+<7..0>
211B1 OUT PE_U1016_U1001_DN<7..0> → PCE_TX-<7..0>

211C1 IN PE_U1001_U1016_DP<7..0> → PCE_RX+<7..0>
211D1 IN PE_U1001_U1016_DN<7..0> → PCE_RX-<7..0>

1B7A7 1B6A7 1B5A7 1B4A7 1B3A7 167C3 249A3 193A8 191A7 190A7 189A7 188A7 IN P1V8_LSI_PG → P1V8_PG

193A8 191A7 167A3 IN LSI_P0V9_2_EN → P0V9_EN
166C4 OUT LSI_P0V9_9_PG → P0V9_PG

SAS_TX+<7..0> — U1016_TX+<7..0> — 7..4 / 3..0 — SAS_U1016_MS_DP<3..0> OUT 223D4 — SAS_U1016_U1018_DP<3..0> OUT 201D8
SAS_TX-<7..0> — U1016_TX-<7..0> — 7..4 / 3..0 — SAS_U1016_MS_DN<3..0> OUT 223D4 — SAS_U1016_U1018_DN<3..0> OUT 201C8
SAS_RX+<7..0> — U1016_RX+<7..0> — 7..4 / 3..0 — SAS_MS_U1016_DP<3..0> IN 223D8 — SAS_U1018_U1016_DP<3..0> IN 201D1
SAS_RX-<7..0> — U1016_RX-<7..0> — 7..4 / 3..0 — SAS_MS_U1016_DN<3..0> IN 223D8 — SAS_U1018_U1016_DN<3..0> IN 201C1

P1V8_LSI
C6140 0.1UF 16V 0402
R3537 1K
P3V3 VCC_ARROW
R3539 4.7K
192C4 U1016_MS_SDA_1V8 → U1016_MS_SDA_3V3 OUT 223D4
TRN00005B2 NTJD4001NT1G
Q120

P1V8_LSI
C6139 0.1UF 16V 0402
R3536 1K
P3V3 VCC_ARROW
R3538 4.7K
192C4 U1016_MS_SCL_1V8 → U1016_MS_SCL_3V3 OUT 223D4
TRN00005B2 NTJD4001NT1G
Q120

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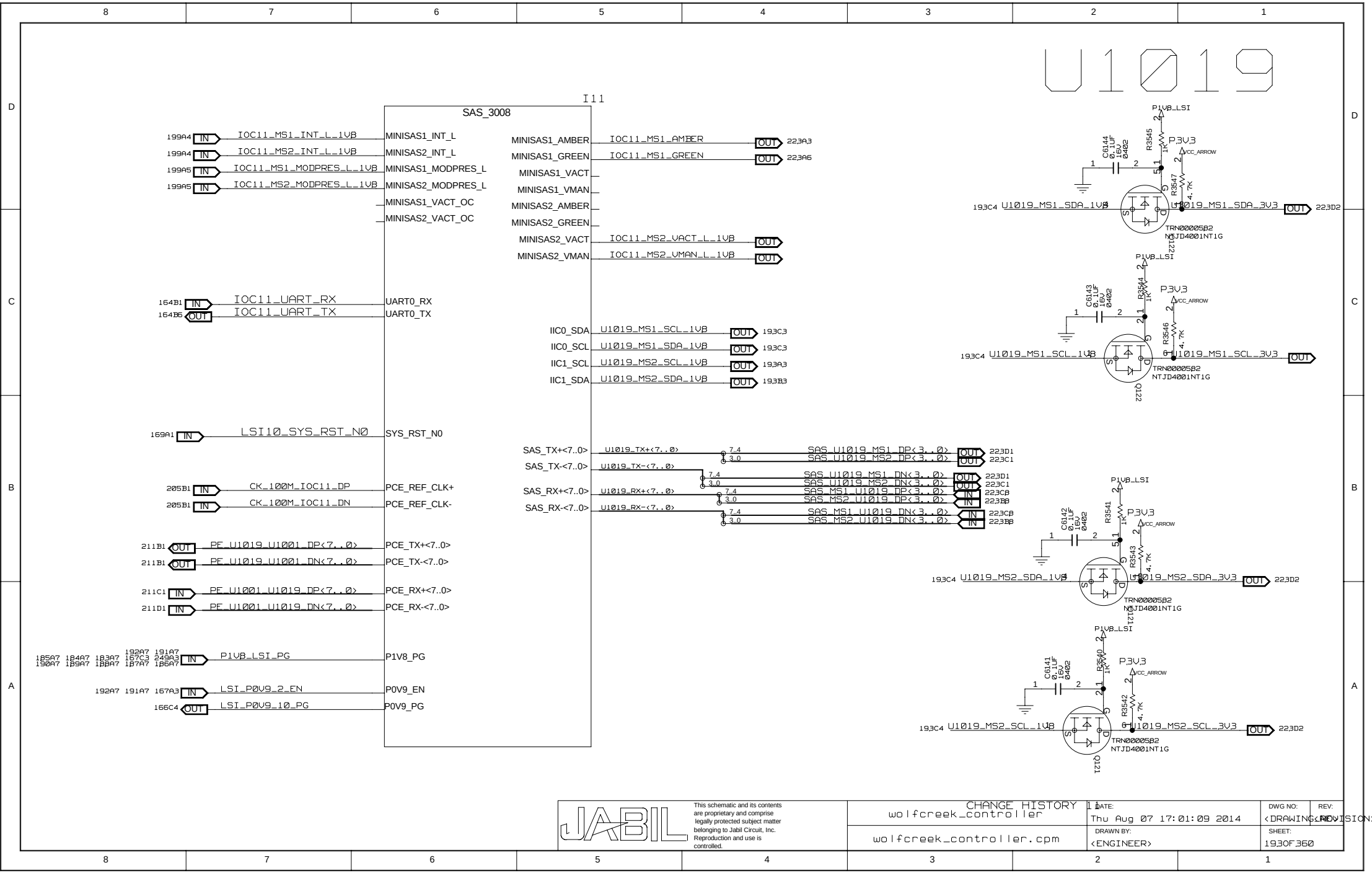
CHANGE HISTORY 1

wolfcreek_controller	DATE: Thu Aug 07 17:08:31 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 192OF,360	



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CHANGE HISTORY 1	DATE: Thu Aug 07 17:01:09 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 193OF,360	

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MIDPLANE CONNECTOR

wolfcreek_controller

wolfcreek_controller.cpm

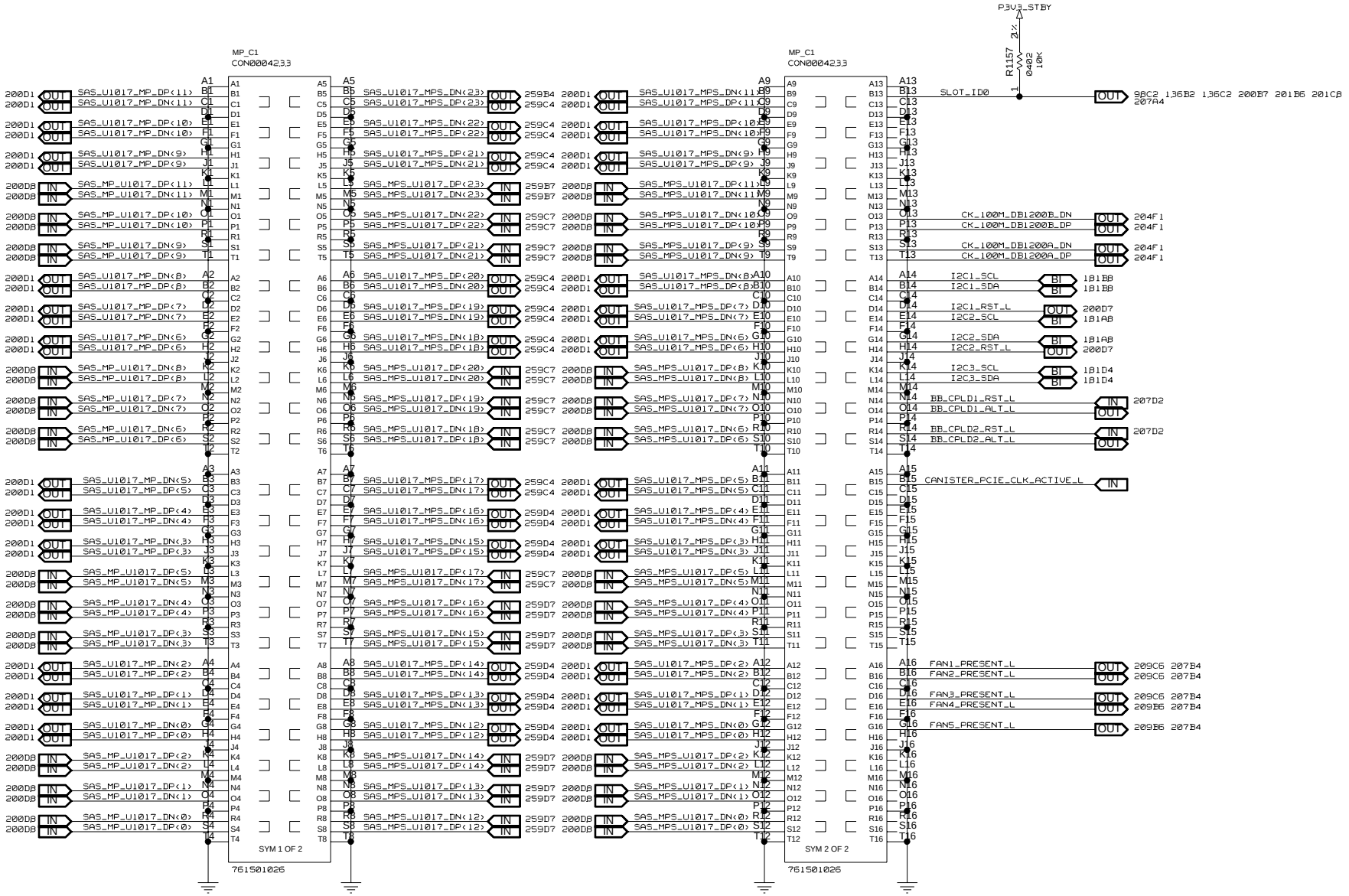
DATE: Wed Jul 30 14:59:40 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 194OF360



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MIDPLANE CONNECTOR
wolfcreek_controller

wolfcreek_controller.cpm

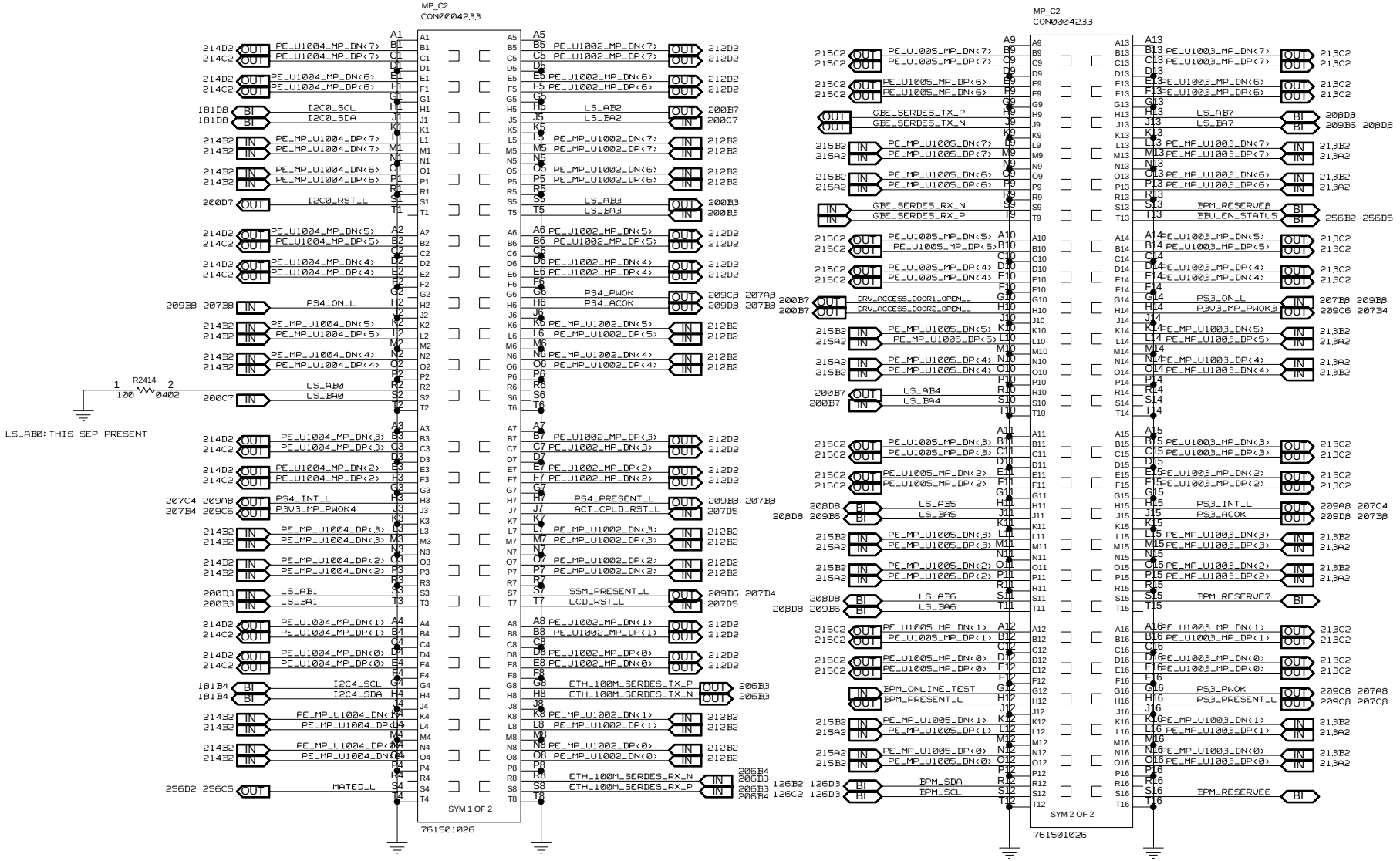
DATE: Fri Aug 08 19:47:41 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 195OF360



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MIDPLANE CONNECTOR

wolfcreek_controller

wolfcreek_controller.cpm

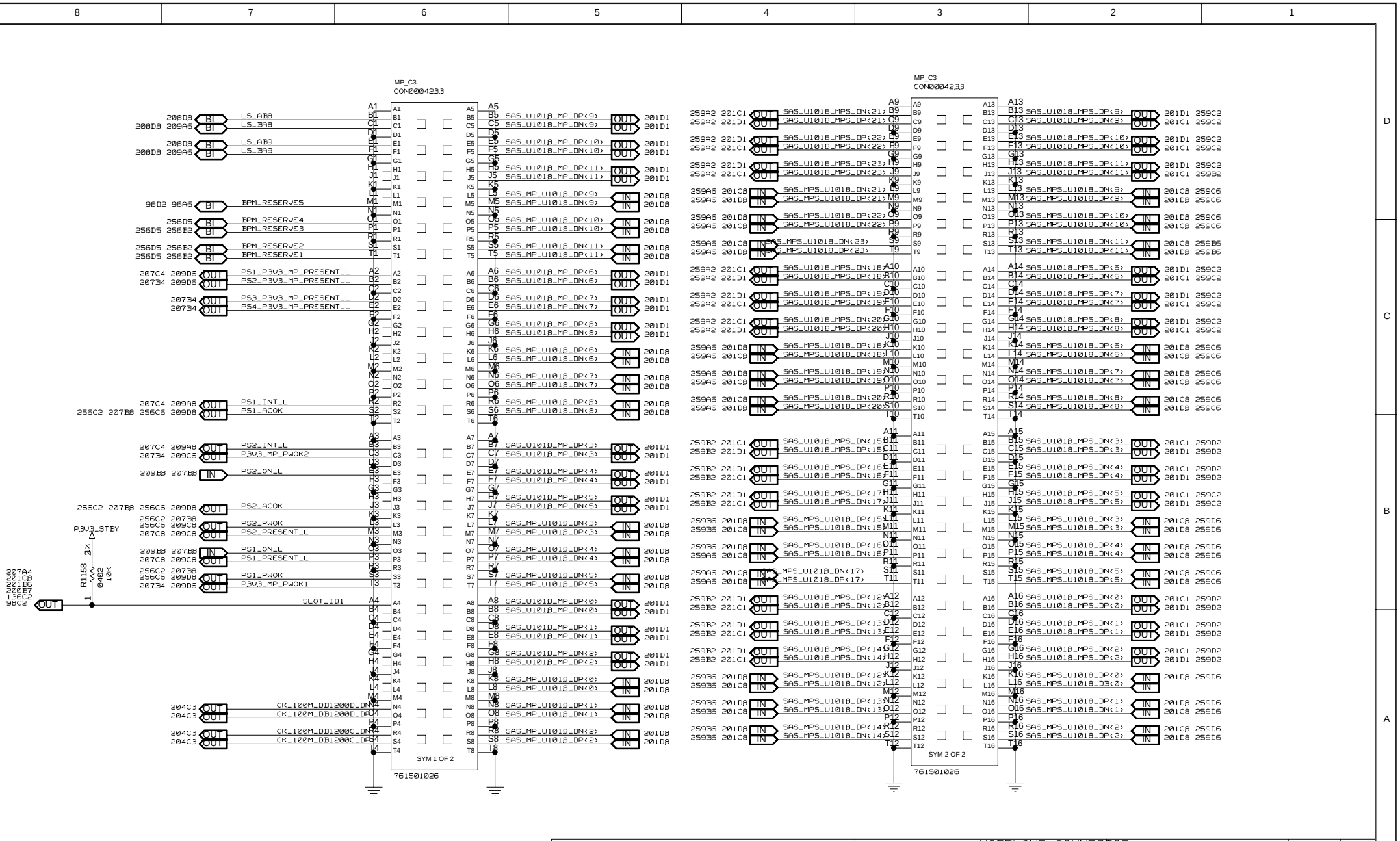
DATE: Thu Aug 07 20:55:48 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING NO>

REV: <REVISION>

SHEET: 196OF360



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MIDPLANE CONNECTOR
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 19:56:02 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 197OF360

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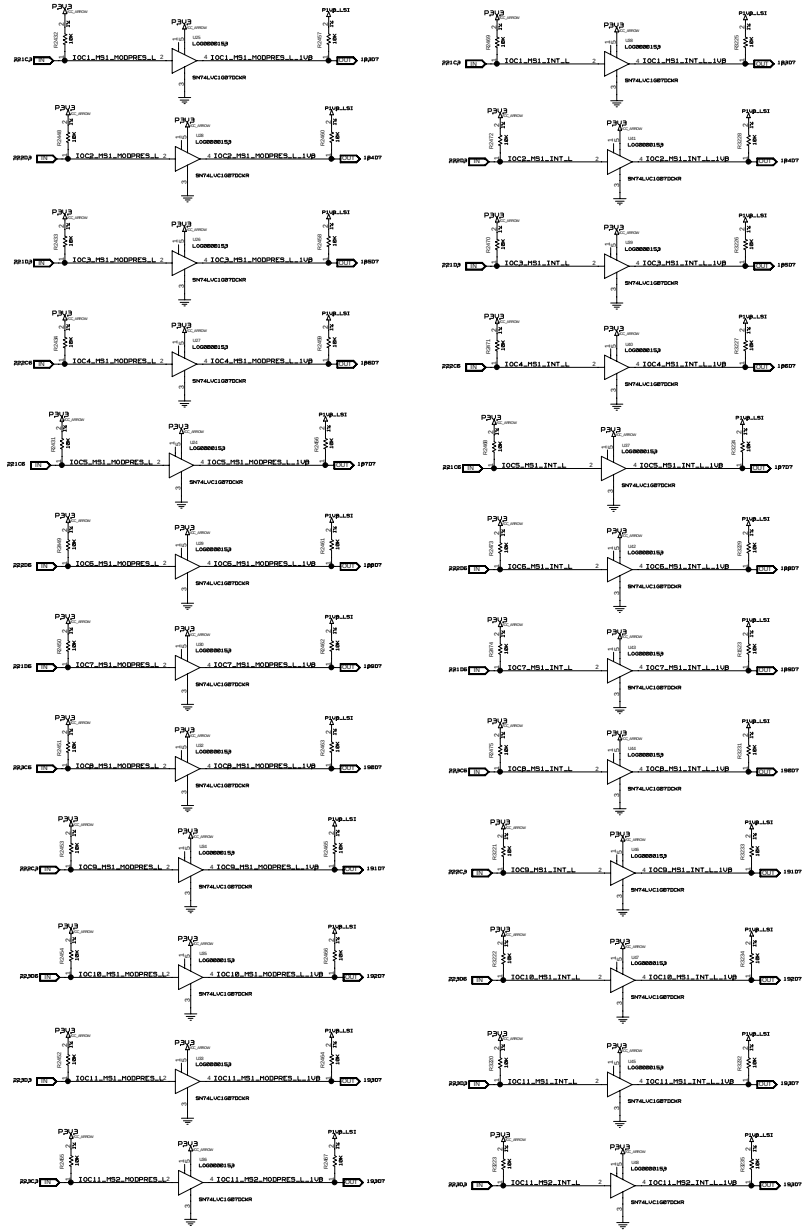
MIDPLANE CONNECTOR
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Wed Jul 30 14:59:41 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 19 OF 360



JABIL	wolfcreek_controller	
	<CON_DESIGN_NAME>	
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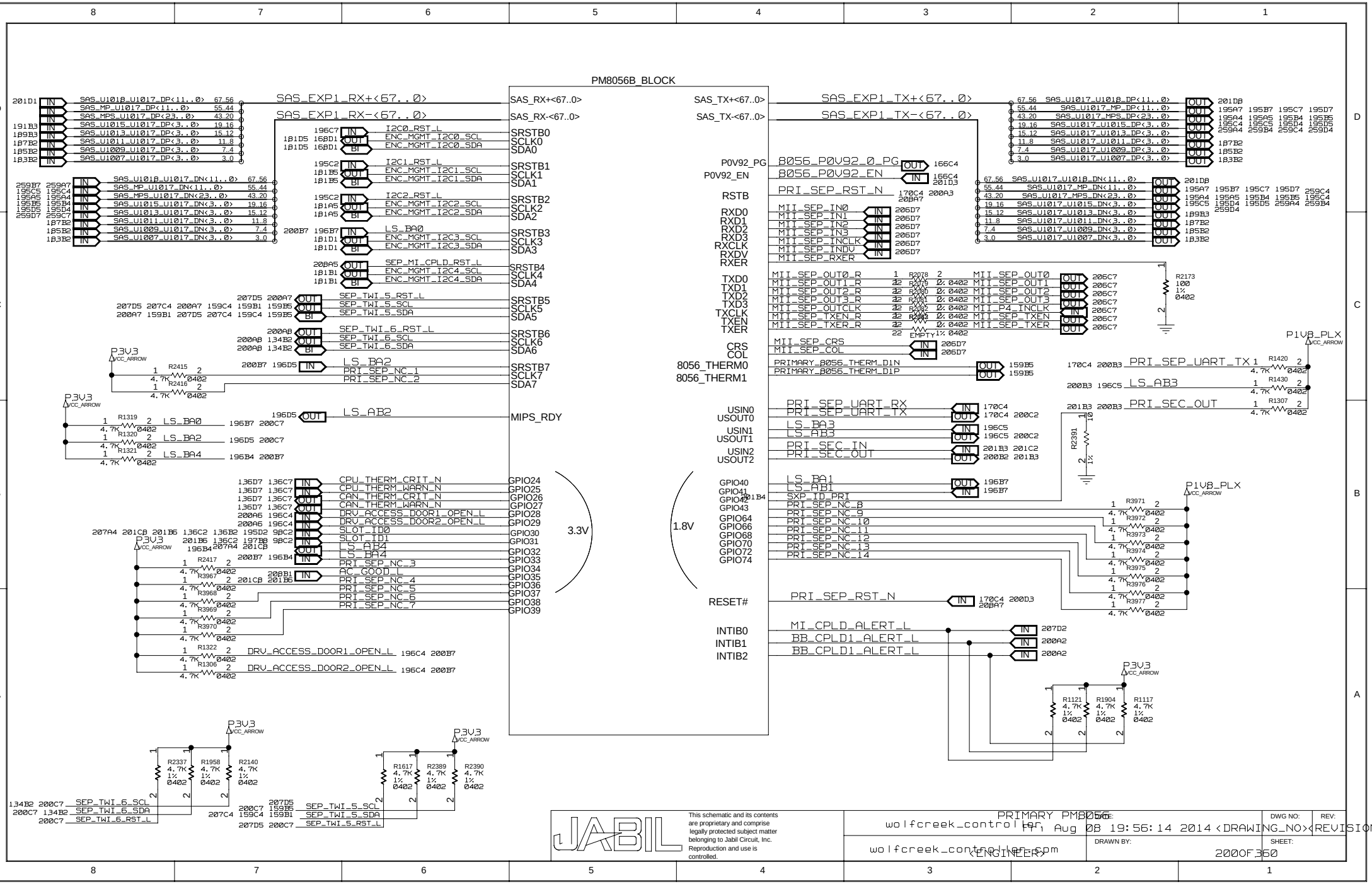
	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>


PM8056B_BLOCK
SAS_EXP1_RX+<67..0>
SAS_EXP1_RX-<67..0>
SAS_EXP1_TX+<67..0>
SAS_EXP1_TX-<67..0>
SAS_RX+<67..0>
SAS_RX-<67..0>
SAS_TX+<67..0>
SAS_TX-<67..0>
SRSTB0
SCLK0
SDA0
SRSTB1
SCLK1
SDA1
SRSTB2
SCLK2
SDA2
SRSTB3
SCLK3
SDA3
SRSTB4
SCLK4
SDA4
SRSTB5
SCLK5
SDA5
SRSTB6
SCLK6
SDA6
SRSTB7
SCLK7
SDA7
MIPS_RDY
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO29
GPIO30
GPIO31
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
3.3V
1.8V
P0V92_PG
P0V92_EN
RSTB
RXD0
RXD1
RXD2
RXD3
RXCLK
RXDV
RXER
TXD0
TXD1
TXD2
TXD3
TXCLK
TXEN
TXER
CRS
COL
8056_THERM0
8056_THERM1
USIN0
USOUT0
USIN1
USOUT1
USIN2
USOUT2
GPIO40
GPIO41
GPIO42
GPIO43
GPIO64
GPIO66
GPIO68
GPIO70
GPIO72
GPIO74
RESET#
INTIB0
INTIB1
INTIB2
8056_P0V92_0_PG
8056_P0V92_EN
PRI_SEP_RST_N
MII_SEP_IN0
MII_SEP_IN1
MII_SEP_IN2
MII_SEP_IN3
MII_SEP_INCLK
MII_SEP_INDV
MII_SEP_RXER
MII_SEP_OUT0_R
MII_SEP_OUT1_R
MII_SEP_OUT2_R
MII_SEP_OUT3_R
MII_SEP_OUTCLK
MII_SEP_TXEN_R
MII_SEP_TXER_R
MII_SEP_OUT0
MII_SEP_OUT1
MII_SEP_OUT2
MII_SEP_OUT3
MII_P4_INCLK
MII_SEP_TXEN
MII_SEP_TXER
MII_SEP_CRS
MII_SEP_COL
PRIMARY_8056_THERM_DIN
PRIMARY_8056_THERM_DIP
PRI_SEP_UART_RX
PRI_SEP_UART_TX
LS_AB3
PRI_SEC_IN
PRI_SEC_OUT
LS_BA1
LS_AB1
SXP_ID_PRI
PRI_SEP_NC_8
PRI_SEP_NC_9
PRI_SEP_NC_10
PRI_SEP_NC_11
PRI_SEP_NC_12
PRI_SEP_NC_13
PRI_SEP_NC_14
MI_CPLD_ALERT_L
BB_CPLD1_ALERT_L
P1V8_PLX
P3V3
LS_BA0
LS_BA2
LS_BA4
LS_AB2
PRI_SEP_NC_1
PRI_SEP_NC_2
CPU_THERM_CRIT_N
CPU_THERM_WARN_N
CAN_THERM_CRIT_N
CAN_THERM_WARN_N
DRV_ACCESS_DOOR1_OPEN_L
DRV_ACCESS_DOOR2_OPEN_L
SLOT_ID0
SLOT_ID1
LS_AB4
LS_BA4
PRI_SEP_NC_3
AC_GOOD_L
PRI_SEP_NC_4
PRI_SEP_NC_5
PRI_SEP_NC_6
PRI_SEP_NC_7
SEP_TWI_5_RST_L
SEP_TWI_5_SCL
SEP_TWI_5_SDA
SEP_TWI_6_RST_L
SEP_TWI_6_SCL
SEP_TWI_6_SDA
SEP_MI_CPLD_RST_L
ENC_MGMT_I2C0_SCL
ENC_MGMT_I2C0_SDA
ENC_MGMT_I2C1_SCL
ENC_MGMT_I2C1_SDA
ENC_MGMT_I2C2_SCL
ENC_MGMT_I2C2_SDA
ENC_MGMT_I2C3_SCL
ENC_MGMT_I2C3_SDA
ENC_MGMT_I2C4_SCL
ENC_MGMT_I2C4_SDA
I2C0_RST_L
I2C1_RST_L
I2C2_RST_L
LS_BA0
SAS_U1018_U1017_DP<11..0>
SAS_MP_U1017_DP<11..0>
SAS_MPS_U1017_DP<23..0>
SAS_U1015_U1017_DP<3..0>
SAS_U1013_U1017_DP<3..0>
SAS_U1011_U1017_DP<3..0>
SAS_U1009_U1017_DP<3..0>
SAS_U1007_U1017_DP<3..0>
SAS_U1018_U1017_DN<11..0>
SAS_MP_U1017_DN<11..0>
SAS_MPS_U1017_DN<23..0>
SAS_U1015_U1017_DN<3..0>
SAS_U1013_U1017_DN<3..0>
SAS_U1011_U1017_DN<3..0>
SAS_U1009_U1017_DN<3..0>
SAS_U1007_U1017_DN<3..0>
SAS_U1017_U1018_DP<11..0>
SAS_U1017_MP_DP<11..0>
SAS_U1017_MPS_DP<23..0>
SAS_U1017_U1015_DP<3..0>
SAS_U1017_U1013_DP<3..0>
SAS_U1017_U1011_DP<3..0>
SAS_U1017_U1009_DP<3..0>
SAS_U1017_U1007_DP<3..0>
SAS_U1017_U1018_DN<11..0>
SAS_U1017_MP_DN<11..0>
SAS_U1017_MPS_DN<23..0>
SAS_U1017_U1015_DN<3..0>
SAS_U1017_U1013_DN<3..0>
SAS_U1017_U1011_DN<3..0>
SAS_U1017_U1009_DN<3..0>
SAS_U1017_U1007_DN<3..0>
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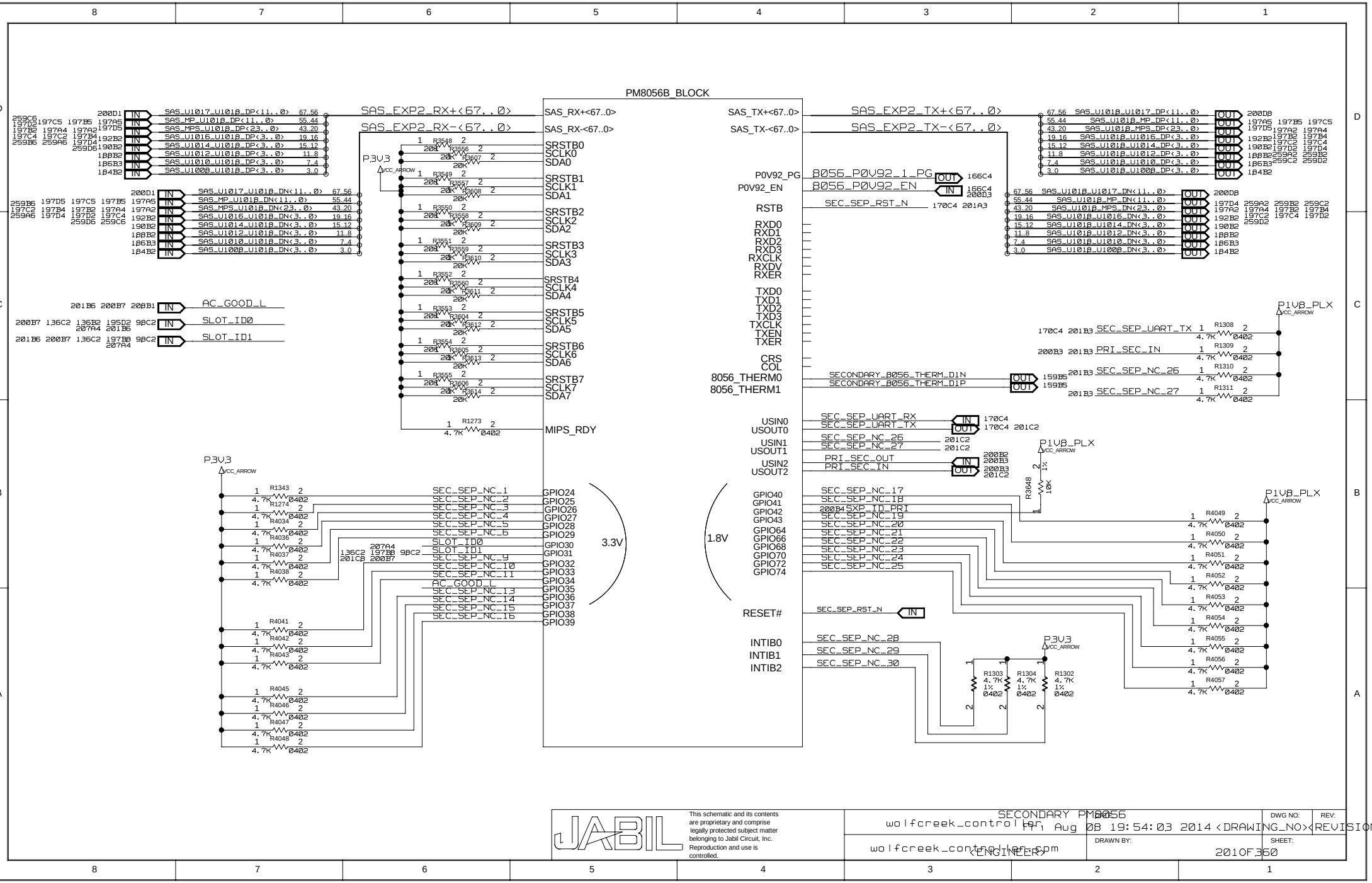
JABIL
PRIMARY PM8056
wolfcreek_controller
Fri Aug 08 19:56:14 2014 <DRAWING_NO><REVISION>
wolfcreek_controller.sch
<ENGINEER>
DWG NO:
REV:
DRAWN BY:
SHEET:
2000F360



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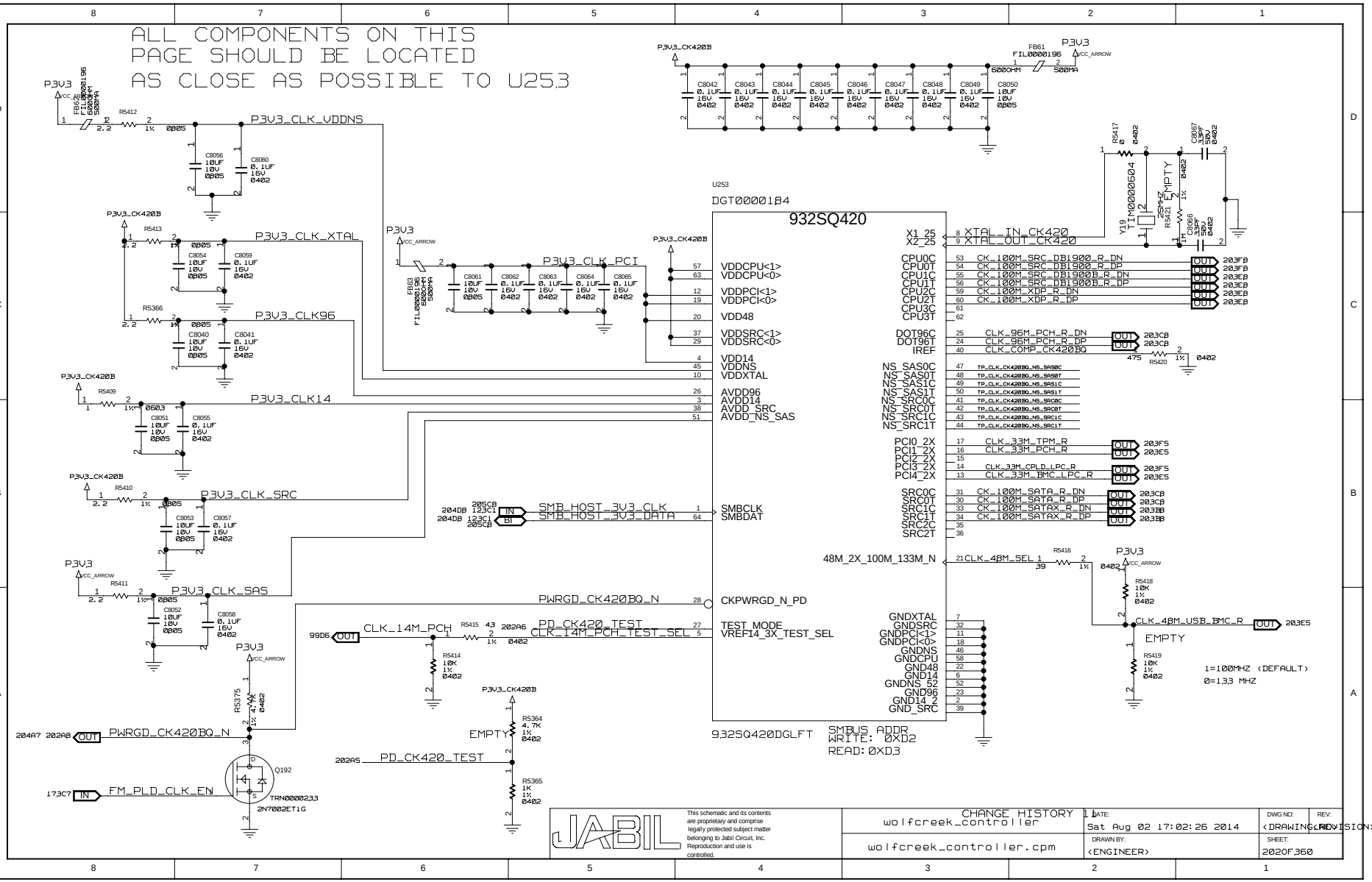
SECONDARY PM8056
wolfcreek_controller
Fri Aug 08 19:54:03 2014 <DRAWING_NO><REVISION>
wolfcreek_controller.sch
<ENGINEER>
DWG NO:
REV:
DRAWN BY:
SHEET:
2010F360


ALL COMPONENTS ON THIS
PAGE SHOULD BE LOCATED
AS CLOSE AS POSSIBLE TO U25.3
932SQ420
U253
DGT00001B4
9.32SQ420DGLFT
SMBUS ADDR
WRITE: 0XD2
READ: 0XD3
P3V3_CLK_VDDNS
P3V3_CLK_XTAL
P3V3_CLK96
P3V3_CLK14
P3V3_CLK_SRC
P3V3_CLK_SAS
P3V3_CLK_PCI
SMB_HOST_3V3_CLK
SMB_HOST_3V3_DATA
PWRGD_CK420BQ_N
PD_CK420_TEST
CLK_14M_PCH
CLK_14M_PCH_TEST_SEL
FM_PLD_CLK_EN
Q192
TRN0000233
2N7002ET1G
XTAL_IN_CK420
XTAL_OUT_CK420
CK_100M_SRC_DB1900_R_DN
CK_100M_SRC_DB1900_R_DP
CK_100M_SRC_DB1900B_R_DN
CK_100M_SRC_DB1900B_R_DP
CK_100M_XDP_R_DN
CK_100M_XDP_R_DP
CLK_96M_PCH_R_DN
CLK_96M_PCH_R_DP
CLK_COMP_CK420BQ
CLK_33M_TPM_R
CLK_33M_PCH_R
CLK_33M_CPLD_LPC_R
CLK_33M_BMC_LPC_R
CK_100M_SATA_R_DN
CK_100M_SATA_R_DP
CK_100M_SATAX_R_DN
CK_100M_SATAX_R_DP
CLK_48M_SEL
CLK_48M_USB_BMC_R
EMPTY
1=100MHZ (DEFAULT)
0=133 MHZ
CHANGE HISTORY
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Sat Aug 02 17:02:26 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
2020F360
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CK420

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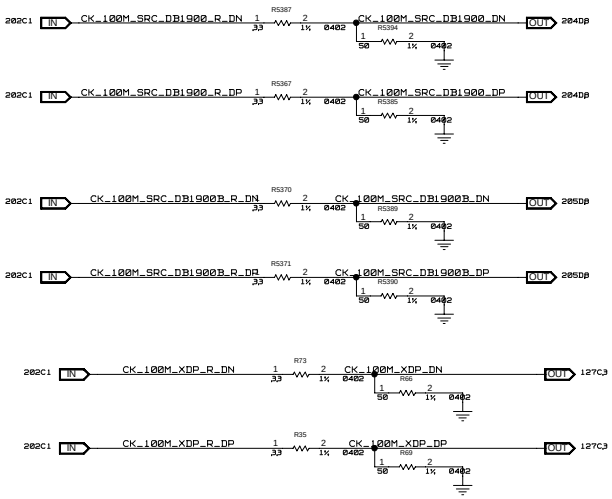

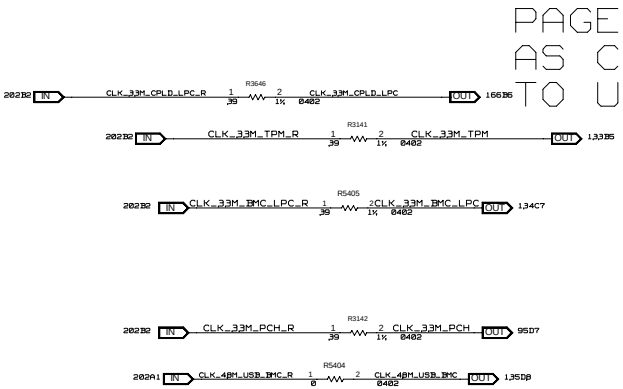

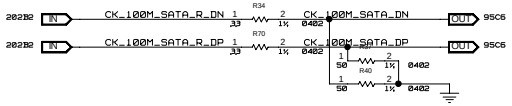

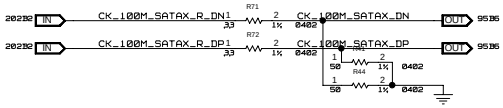

CK420

JABIL

wolfcreek_controller

<CON_DESIGN_NAME>

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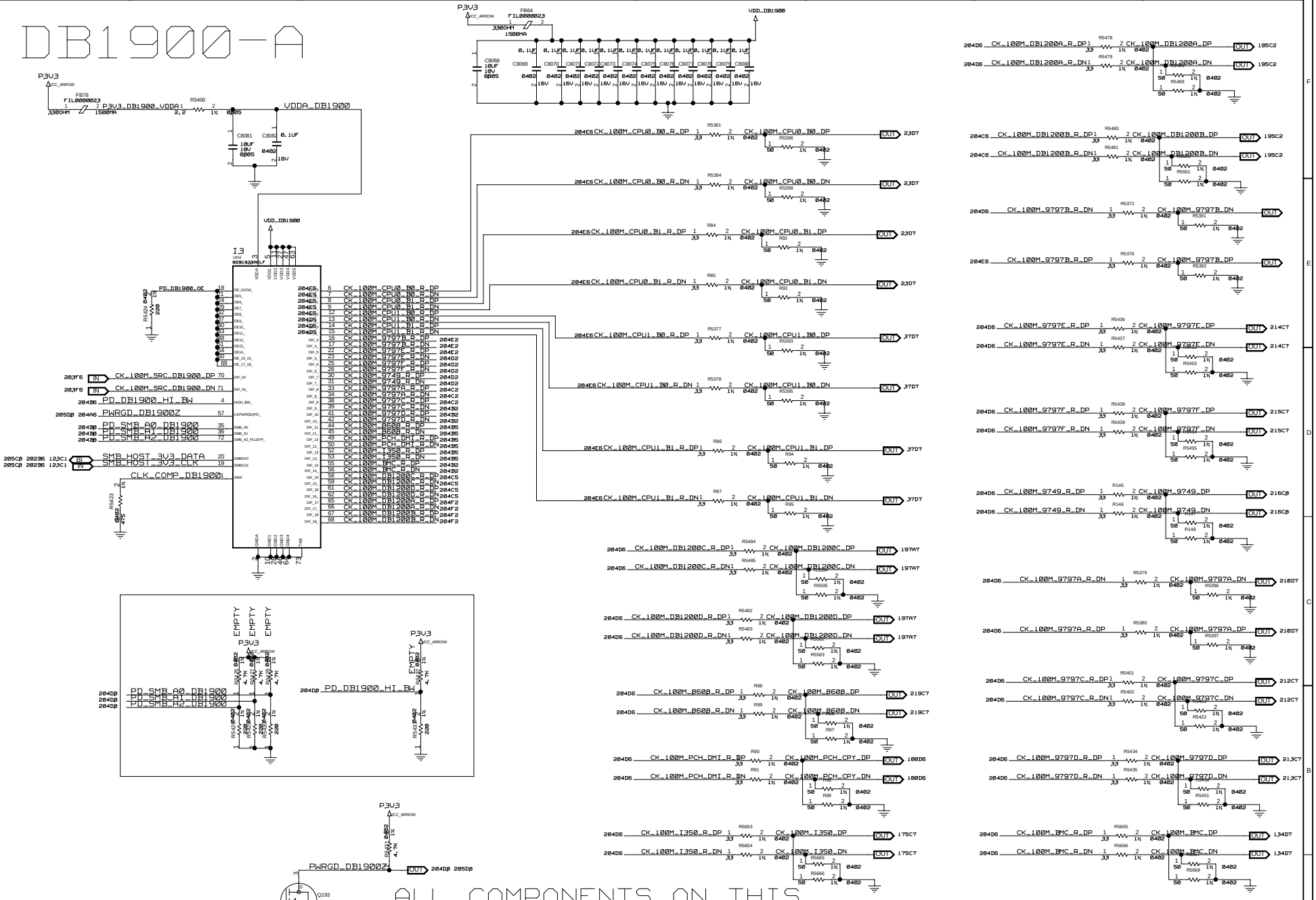
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	

DB1900-A



JABIL

wolfcreek_controller

<CON_DESIGN_NAME>

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DATE: <CON_LAST_MODIFIED>

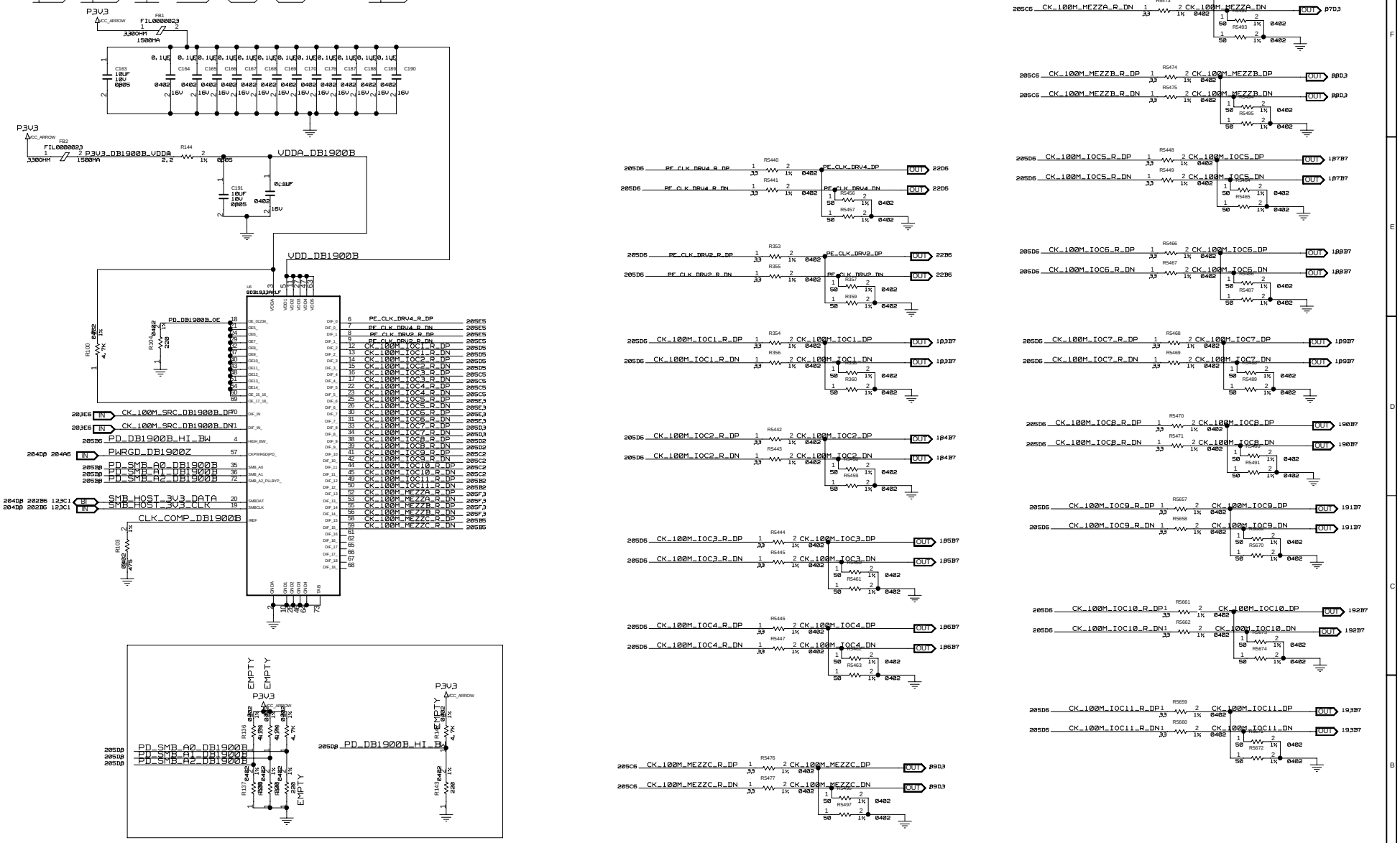
DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DB1900-B



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JABIL

wolfcreek_controller

<CON_DESIGN_NAME>

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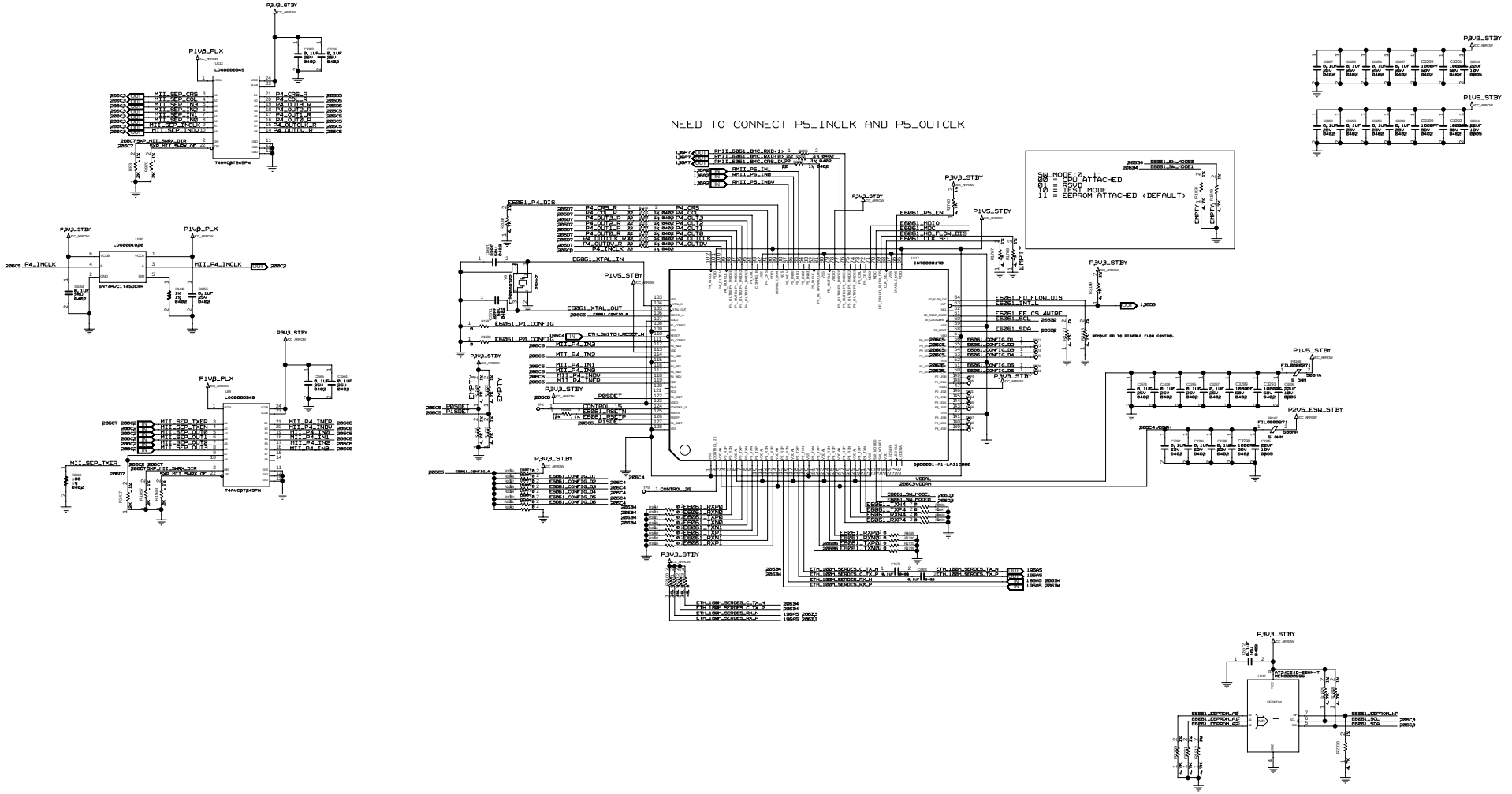
DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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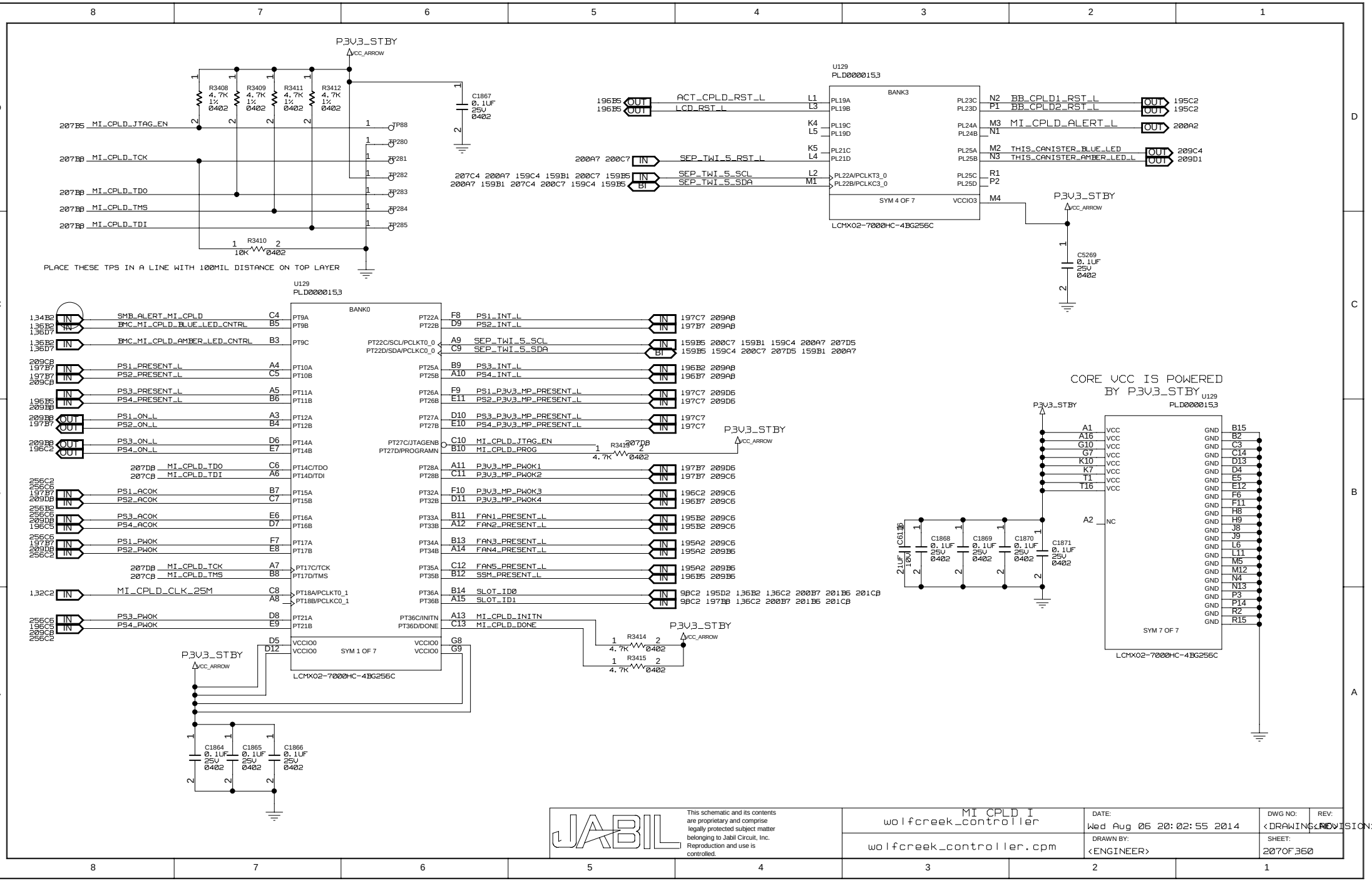
	DRAWN BY: <ENGINEER> · SHEET: 206OF360


P3V3_STBY
VCC_ARROW
R3408 4.7K 1% 0402
R3409 4.7K 1% 0402
R3411 4.7K 1% 0402
R3412 4.7K 1% 0402
C1867 0.1UF 25V 0402
207B5 MI_CPLD_JTAG_EN
207B8 MI_CPLD_TCK
207B8 MI_CPLD_TDO
207B8 MI_CPLD_TMS
207B8 MI_CPLD_TDI
TP88
TP280
TP281
TP282
TP283
TP284
TP285
R3410 10K 0402
PLACE THESE TPS IN A LINE WITH 100MIL DISTANCE ON TOP LAYER
U129
PLD0000153
BANK3
196B5 OUT ACT_CPLD_RST_L
196B5 OUT LCD_RST_L
200A7 200C7 IN SEP_TWI_5_RST_L
207C4 200A7 159C4 159B1 200C7 159B5 IN SEP_TWI_5_SCL
200A7 159B1 207C4 200C7 159C4 159B5 BI SEP_TWI_5_SDA
L1 PL19A
L3 PL19B
K4 PL19C
L5 PL19D
K5 PL21C
L4 PL21D
L2 PL22A/PCLKT3_0
M1 PL22B/PCLKC3_0
SYM 4 OF 7
VCCIO3
N2 PL23C
P1 PL23D
M3 PL24A
N1 PL24B
M2 PL25A
N3 PL25B
R1 PL25C
P2 PL25D
M4
BB_CPLD1_RST_L OUT 195C2
BB_CPLD2_RST_L OUT 195C2
MI_CPLD_ALERT_L OUT 200A2
THIS_CANISTER_BLUE_LED OUT 209C4
THIS_CANISTER_AMBER_LED_L OUT 209D1
LCMXO2-7000HC-4BG256C
C5269 0.1UF 25V 0402
BANK0
1,34B2 IN SMB_ALERT_MI_CPLD C4 PT9A
1,36B2 IN BMC_MI_CPLD_BLUE_LED_CNTRL B5 PT9B
1,36B2 1,36D7 IN BMC_MI_CPLD_AMBER_LED_CNTRL B3 PT9C
209C8 197B7 IN PS1_PRESENT_L A4 PT10A
197B7 209C8 IN PS2_PRESENT_L C5 PT10B
IN PS3_PRESENT_L A5 PT11A
196B5 209B8 IN PS4_PRESENT_L B6 PT11B
209B8 197B7 OUT PS1_ON_L A3 PT12A
OUT PS2_ON_L B4 PT12B
209B8 196C2 OUT PS3_ON_L D6 PT14A
OUT PS4_ON_L E7 PT14B
207D8 MI_CPLD_TDO C6 PT14C/TDO
207C8 MI_CPLD_TDI A6 PT14D/TDI
256C2 256C6 197B7 209D8 IN PS1_ACOK B7 PT15A
IN PS2_ACOK C7 PT15B
256B2 256C6 209D8 IN PS3_ACOK E6 PT16A
IN PS4_ACOK D7 PT16B
256C6 197B7 209D8 IN PS1_PWOK F7 PT17A
IN PS2_PWOK E8 PT17B
207D8 MI_CPLD_TCK A7 PT17C/TCK
207C8 MI_CPLD_TMS B8 PT17D/TMS
1,32C2 IN MI_CPLD_CLK_25M C8 PT18A/PCLKT0_1
A8 PT18B/PCLKC0_1
256C6 196C5 209C8 256C2 IN PS3_PWOK D8 PT21A
IN PS4_PWOK E9 PT21B
D5 VCCIO0
D12 VCCIO0
SYM 1 OF 7
PT22A F8 PS1_INT_L
PT22B D9 PS2_INT_L
PT22C/SCL/PCLKT0_0 A9 SEP_TWI_5_SCL
PT22D/SDA/PCLKC0_0 C9 SEP_TWI_5_SDA
PT25A B9 PS3_INT_L
PT25B A10 PS4_INT_L
PT26A F9 PS1_P3V3_MP_PRESENT_L
PT26B E11 PS2_P3V3_MP_PRESENT_L
PT27A D10 PS3_P3V3_MP_PRESENT_L
PT27B E10 PS4_P3V3_MP_PRESENT_L
PT27C/JTAGENB C10 MI_CPLD_JTAG_EN
PT27D/PROGRAMN B10 MI_CPLD_PROG
R3413 4.7K 0402 207D8
PT28A A11 P3V3_MP_PWOK1
PT28B C11 P3V3_MP_PWOK2
PT32A F10 P3V3_MP_PWOK3
PT32B D11 P3V3_MP_PWOK4
PT33A B11 FAN1_PRESENT_L
PT33B A12 FAN2_PRESENT_L
PT34A B13 FAN3_PRESENT_L
PT34B A14 FAN4_PRESENT_L
PT35A C12 FAN5_PRESENT_L
PT35B B12 SSM_PRESENT_L
PT36A B14 SLOT_ID0
PT36B A15 SLOT_ID1
PT36C/INITN A13 MI_CPLD_INITN
PT36D/DONE C13 MI_CPLD_DONE
VCCIO0 G8
VCCIO0 G9
197C7 209A8 IN
197B7 209A8 IN
159B5 200C7 159B1 159C4 200A7 207D5 IN
159B5 159C4 200C7 207D5 159B1 200A7 BI
196B2 209A8 IN
196B7 209A8 IN
197C7 209D6 IN
197C7 209D6 IN
197C7 IN
197C7 IN
197B7 209D6 IN
197B7 209C6 IN
196C2 209C6 IN
196B7 209C6 IN
195B2 209C6 IN
195B2 209C6 IN
195A2 209C6 IN
195A2 209B6 IN
195A2 209B6 IN
196B5 209B6 IN
9BC2 195D2 1,36B2 1,36C2 200B7 201B6 201C8 IN
9BC2 197B8 1,36C2 200B7 201B6 201C8 IN
R3414 4.7K 0402
R3415 4.7K 0402
LCMXO2-7000HC-4BG256C
C1864 0.1UF 25V 0402
C1865 0.1UF 25V 0402
C1866 0.1UF 25V 0402
CORE VCC IS POWERED BY P3V3_STBY
U129
PLD0000153
A1 VCC
A16 VCC
G10 VCC
G7 VCC
K10 VCC
K7 VCC
T1 VCC
T16 VCC
A2 NC
SYM 7 OF 7
B15 GND
B2 GND
C3 GND
C14 GND
D13 GND
D4 GND
E5 GND
E12 GND
F6 GND
F11 GND
H8 GND
H9 GND
J8 GND
J9 GND
L6 GND
L11 GND
M5 GND
M12 GND
N4 GND
N13 GND
P3 GND
P14 GND
R2 GND
R15 GND
C1868 0.1UF 25V 0402
C1869 0.1UF 25V 0402
C1870 0.1UF 25V 0402
C1871 0.1UF 25V 0402
C6186 21UF 10V
LCMXO2-7000HC-4BG256C
JABIL
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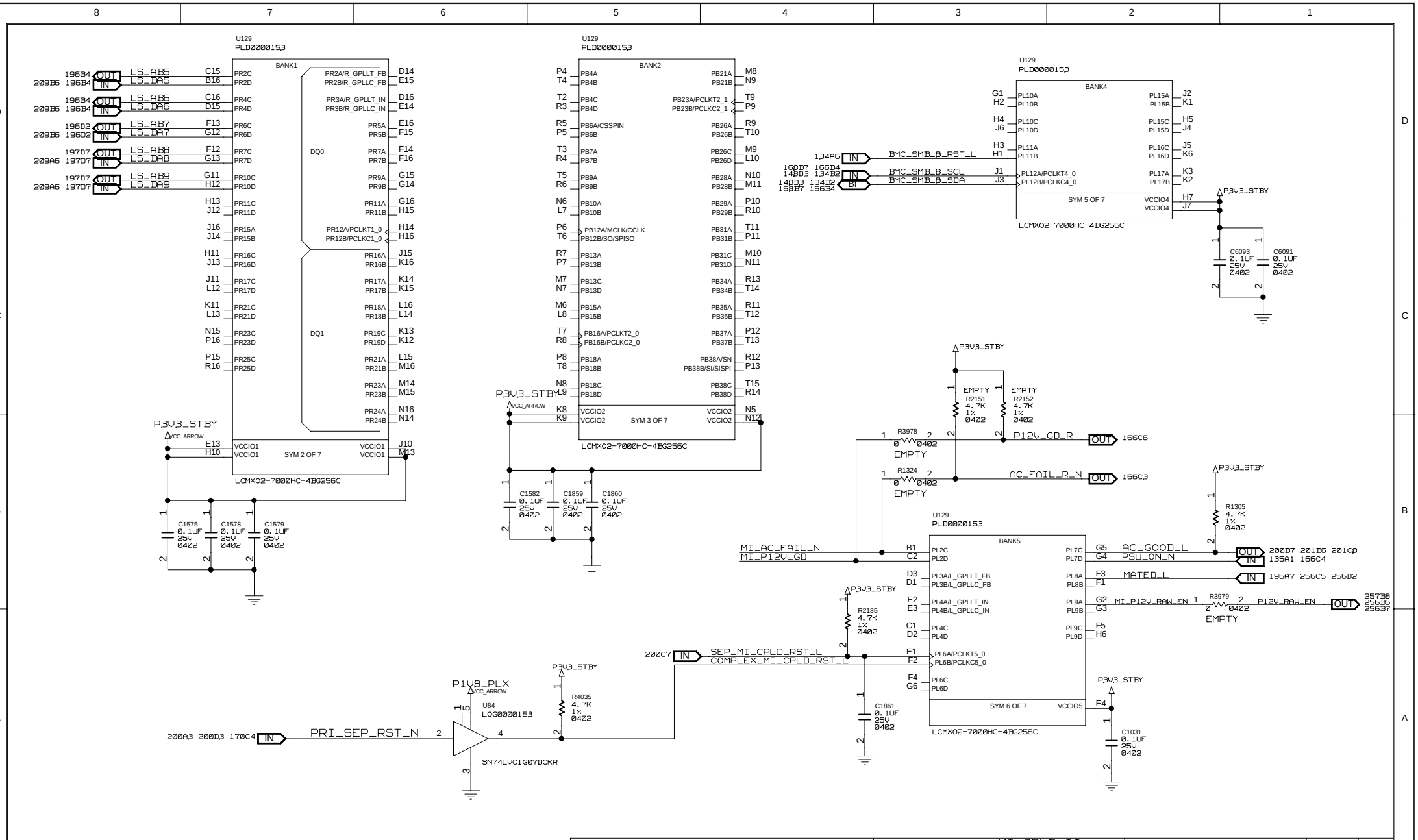
MI CPLD I
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Wed Aug 06 20:02:55 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING NO>
REV:
<REVISION>
SHEET:
207OF360


U129
PLD000015.3
BANK1
LCMX02-7000HC-4BG256C
SYM 2 OF 7
DQ0
DQ1
LS_AB5
LS_BA5
LS_AB6
LS_BA6
LS_AB7
LS_BA7
LS_AB8
LS_BA8
LS_AB9
LS_BA9
P3V3_STBY
VCC_ARROW
C1575 0.1UF 25V 0402
C1578 0.1UF 25V 0402
C1579 0.1UF 25V 0402
BANK2
SYM 3 OF 7
PB12A/PCLKT1_0
PB12B/PCLKC1_0
PB12A/MCLK/CCLK
PB12B/SO/SPISO
PB16A/PCLKT2_0
PB16B/PCLKC2_0
PB23A/PCLKT2_1
PB23B/PCLKC2_1
C1582 0.1UF 25V 0402
C1859 0.1UF 25V 0402
C1860 0.1UF 25V 0402
BANK4
SYM 5 OF 7
BMC_SMB_B_RST_L
BMC_SMB_B_SCL
BMC_SMB_B_SDA
PL12A/PCLKT4_0
PL12B/PCLKC4_0
C6093 0.1UF 25V 0402
C6091 0.1UF 25V 0402
EMPTY
R2151 4.7K 1% 0402
R2152 4.7K 1% 0402
R3978 0 0402
P12V_GD_R
R1324 0 0402
AC_FAIL_R_N
BANK5
SYM 6 OF 7
MI_AC_FAIL_N
MI_P12V_GD
AC_GOOD_L
PSU_ON_N
MATED_L
MI_P12V_RAW_EN
R3979 0 0402
P12V_RAW_EN
R1305 4.7K 1% 0402
R2135 4.7K 1% 0402
SEP_MI_CPLD_RST_L
COMPLEX_MI_CPLD_RST_L
C1861 0.1UF 25V 0402
C1031 0.1UF 25V 0402
P1V8_PLX
U84
LOG000015.3
SN74LVC1G07DCKR
R4035 4.7K 1% 0402
PRI_SEP_RST_N
JABIL
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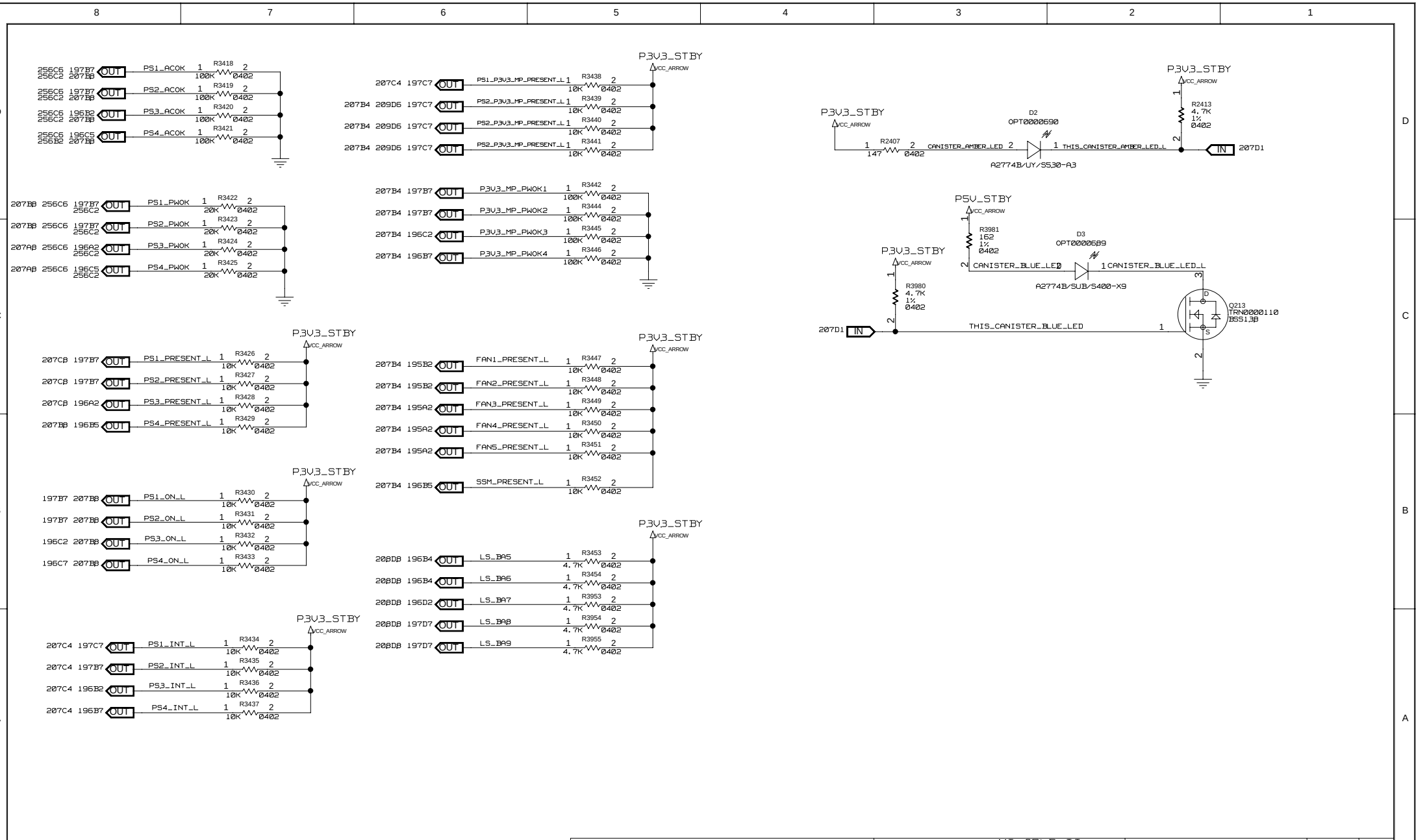
MI CPLD II
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Fri Aug 08 19:56:26 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
20 OF 360



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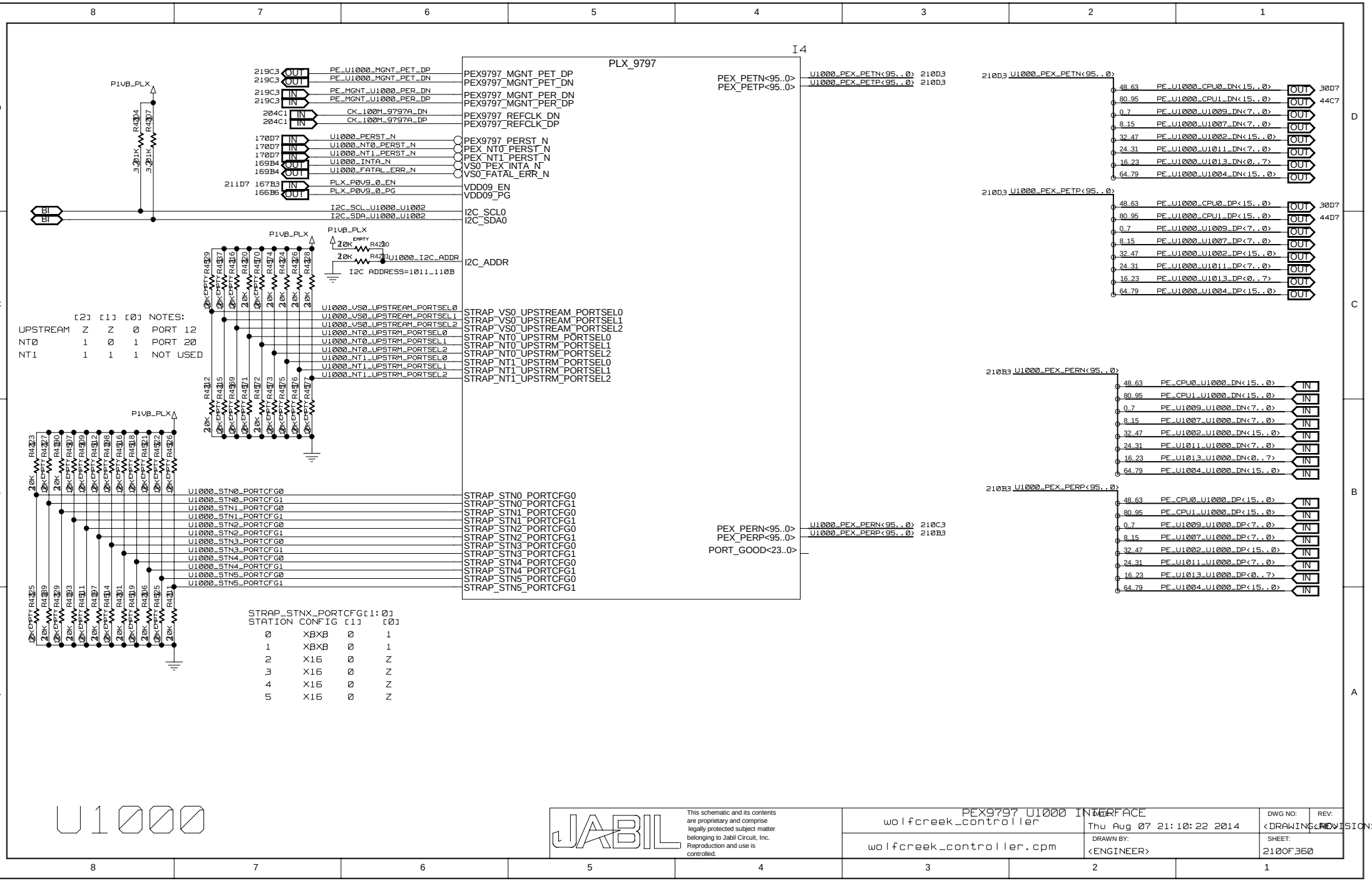
MI CPLD II wolfcreek_controller	DATE: Thu Aug 07 17:51:07 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 209OF360	


I4
PLX_9797
P1V8_PLX
PE_U1000_MGNT_PET_DP
PE_U1000_MGNT_PET_DN
PE_MGNT_U1000_PER_DN
PE_MGNT_U1000_PER_DP
CK_100M_9797A_DN
CK_100M_9797A_DP
U1000_PERST_N
U1000_NT0_PERST_N
U1000_NT1_PERST_N
U1000_INTA_N
U1000_FATAL_ERR_N
PLX_P0V9_0_EN
PLX_P0V9_0_PG
I2C_SCL_U1000_U1002
I2C_SDA_U1000_U1002
U1000_I2C_ADDR
I2C ADDRESS=1011_110B
PEX9797_MGNT_PET_DP
PEX9797_MGNT_PET_DN
PEX9797_MGNT_PER_DN
PEX9797_MGNT_PER_DP
PEX9797_REFCLK_DN
PEX9797_REFCLK_DP
PEX9797_PERST_N
PEX_NT0_PERST_N
PEX_NT1_PERST_N
VS0_PEX_INTA_N
VS0_FATAL_ERR_N
VDD09_EN
VDD09_PG
I2C_SCL0
I2C_SDA0
I2C_ADDR
STRAP_VS0_UPSTREAM_PORTSEL0
STRAP_VS0_UPSTREAM_PORTSEL1
STRAP_VS0_UPSTREAM_PORTSEL2
STRAP_NT0_UPSTRM_PORTSEL0
STRAP_NT0_UPSTRM_PORTSEL1
STRAP_NT0_UPSTRM_PORTSEL2
STRAP_NT1_UPSTRM_PORTSEL0
STRAP_NT1_UPSTRM_PORTSEL1
STRAP_NT1_UPSTRM_PORTSEL2
STRAP_STN0_PORTCFG0
STRAP_STN0_PORTCFG1
STRAP_STN1_PORTCFG0
STRAP_STN1_PORTCFG1
STRAP_STN2_PORTCFG0
STRAP_STN2_PORTCFG1
STRAP_STN3_PORTCFG0
STRAP_STN3_PORTCFG1
STRAP_STN4_PORTCFG0
STRAP_STN4_PORTCFG1
STRAP_STN5_PORTCFG0
STRAP_STN5_PORTCFG1
PEX_PETN<95..0>
PEX_PETP<95..0>
PEX_PERN<95..0>
PEX_PERP<95..0>
PORT_GOOD<23..0>
U1000_PEX_PETN<95..0>
U1000_PEX_PETP<95..0>
U1000_PEX_PERN<95..0>
U1000_PEX_PERP<95..0>
PE_U1000_CPU0_DN<15..0>
PE_U1000_CPU1_DN<15..0>
PE_U1000_U1009_DN<7..0>
PE_U1000_U1007_DN<7..0>
PE_U1000_U1002_DN<15..0>
PE_U1000_U1011_DN<7..0>
PE_U1000_U1013_DN<0..7>
PE_U1000_U1004_DN<15..0>
PE_U1000_CPU0_DP<15..0>
PE_U1000_CPU1_DP<15..0>
PE_U1000_U1009_DP<7..0>
PE_U1000_U1007_DP<7..0>
PE_U1000_U1002_DP<15..0>
PE_U1000_U1011_DP<7..0>
PE_U1000_U1013_DP<0..7>
PE_U1000_U1004_DP<15..0>
PE_CPU0_U1000_DN<15..0>
PE_CPU1_U1000_DN<15..0>
PE_U1009_U1000_DN<7..0>
PE_U1007_U1000_DN<7..0>
PE_U1002_U1000_DN<15..0>
PE_U1011_U1000_DN<7..0>
PE_U1013_U1000_DN<0..7>
PE_U1004_U1000_DN<15..0>
PE_CPU0_U1000_DP<15..0>
PE_CPU1_U1000_DP<15..0>
PE_U1009_U1000_DP<7..0>
PE_U1007_U1000_DP<7..0>
PE_U1002_U1000_DP<15..0>
PE_U1011_U1000_DP<7..0>
PE_U1013_U1000_DP<0..7>
PE_U1004_U1000_DP<15..0>
[2] [1] [0] NOTES:
UPSTREAM Z Z 0 PORT 12
NT0 1 0 1 PORT 20
NT1 1 1 1 NOT USED
STRAP_STNX_PORTCFG[1:0]
STATION CONFIG [1] [0]
0 X8X8 0 1
1 X8X8 0 1
2 X16 0 Z
3 X16 0 Z
4 X16 0 Z
5 X16 0 Z
U1000
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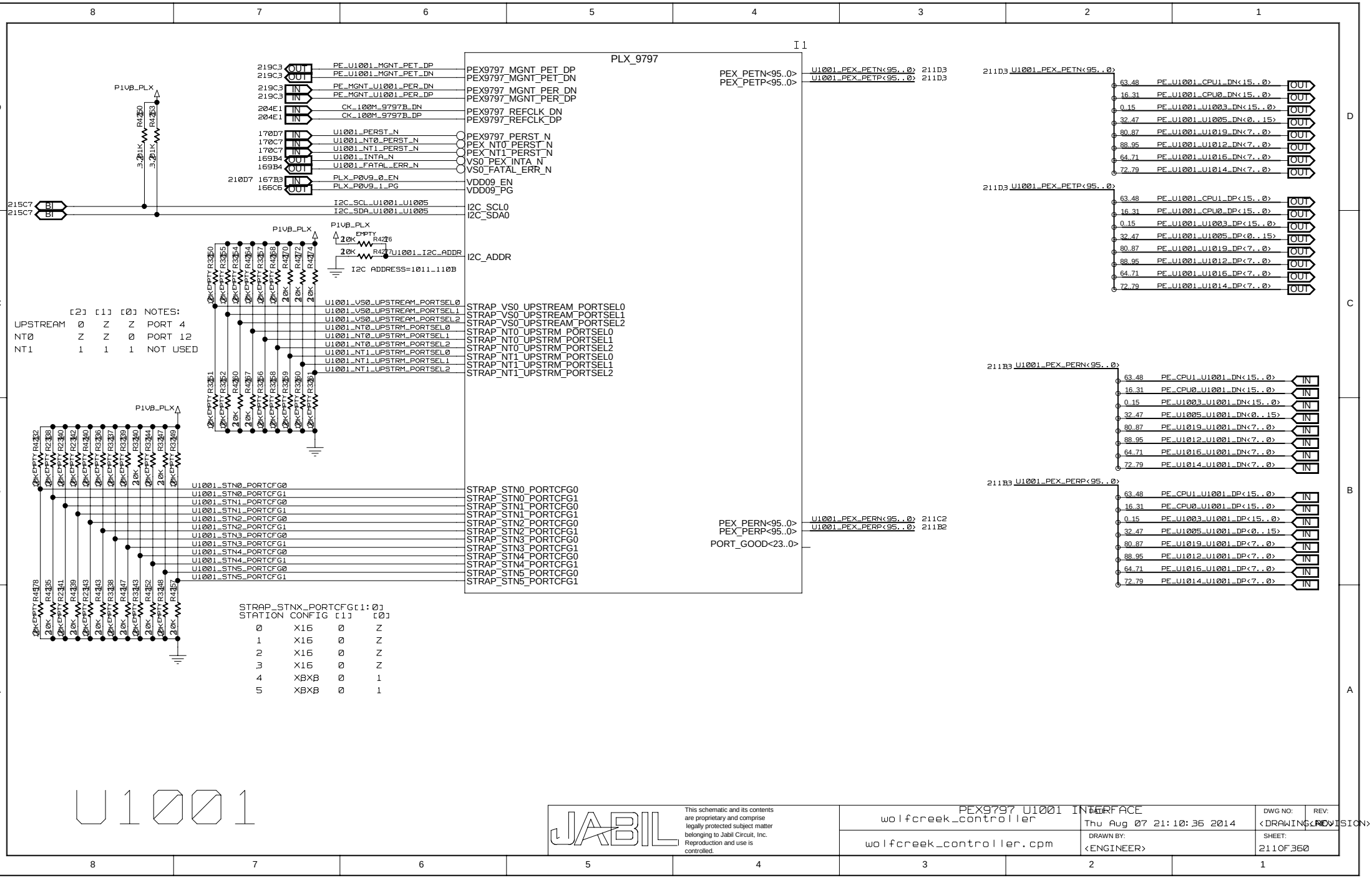
PEX9797 U1000 INTERFACE
wolfcreek_controller
wolfcreek_controller.cpm
DATE: Thu Aug 07 21:10:22 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING NO>
REV: <REVISION>
SHEET: 210OF360


PLX_9797
I1
PE_U1001_MGNT_PET_DP
PE_U1001_MGNT_PET_DN
PE_MGNT_U1001_PER_DN
PE_MGNT_U1001_PER_DP
CK_100M_9797B_DN
CK_100M_9797B_DP
U1001_PERST_N
U1001_NT0_PERST_N
U1001_NT1_PERST_N
U1001_INTA_N
U1001_FATAL_ERR_N
PLX_P0V9_0_EN
PLX_P0V9_1_PG
I2C_SCL_U1001_U1005
I2C_SDA_U1001_U1005
U1001_I2C_ADDR
I2C ADDRESS=1011_110B
U1001_VS0_UPSTREAM_PORTSEL0
U1001_VS0_UPSTREAM_PORTSEL1
U1001_VS0_UPSTREAM_PORTSEL2
U1001_NT0_UPSTRM_PORTSEL0
U1001_NT0_UPSTRM_PORTSEL1
U1001_NT0_UPSTRM_PORTSEL2
U1001_NT1_UPSTRM_PORTSEL0
U1001_NT1_UPSTRM_PORTSEL1
U1001_NT1_UPSTRM_PORTSEL2
U1001_STN0_PORTCFG0
U1001_STN0_PORTCFG1
U1001_STN1_PORTCFG0
U1001_STN1_PORTCFG1
U1001_STN2_PORTCFG0
U1001_STN2_PORTCFG1
U1001_STN3_PORTCFG0
U1001_STN3_PORTCFG1
U1001_STN4_PORTCFG0
U1001_STN4_PORTCFG1
U1001_STN5_PORTCFG0
U1001_STN5_PORTCFG1
PEX9797_MGNT_PET_DP
PEX9797_MGNT_PET_DN
PEX9797_MGNT_PER_DN
PEX9797_MGNT_PER_DP
PEX9797_REFCLK_DN
PEX9797_REFCLK_DP
PEX9797_PERST_N
PEX_NT0_PERST_N
PEX_NT1_PERST_N
VS0_PEX_INTA_N
VS0_FATAL_ERR_N
VDD09_EN
VDD09_PG
I2C_SCL0
I2C_SDA0
I2C_ADDR
STRAP_VS0_UPSTREAM_PORTSEL0
STRAP_VS0_UPSTREAM_PORTSEL1
STRAP_VS0_UPSTREAM_PORTSEL2
STRAP_NT0_UPSTRM_PORTSEL0
STRAP_NT0_UPSTRM_PORTSEL1
STRAP_NT0_UPSTRM_PORTSEL2
STRAP_NT1_UPSTRM_PORTSEL0
STRAP_NT1_UPSTRM_PORTSEL1
STRAP_NT1_UPSTRM_PORTSEL2
STRAP_STN0_PORTCFG0
STRAP_STN0_PORTCFG1
STRAP_STN1_PORTCFG0
STRAP_STN1_PORTCFG1
STRAP_STN2_PORTCFG0
STRAP_STN2_PORTCFG1
STRAP_STN3_PORTCFG0
STRAP_STN3_PORTCFG1
STRAP_STN4_PORTCFG0
STRAP_STN4_PORTCFG1
STRAP_STN5_PORTCFG0
STRAP_STN5_PORTCFG1
PEX_PETN<95..0>
PEX_PETP<95..0>
PEX_PERN<95..0>
PEX_PERP<95..0>
PORT_GOOD<23..0>
U1001_PEX_PETN<95..0>
U1001_PEX_PETP<95..0>
U1001_PEX_PERN<95..0>
U1001_PEX_PERP<95..0>
PE_U1001_CPU1_DN<15..0>
PE_U1001_CPU0_DN<15..0>
PE_U1001_U1003_DN<15..0>
PE_U1001_U1005_DN<0..15>
PE_U1001_U1019_DN<7..0>
PE_U1001_U1012_DN<7..0>
PE_U1001_U1016_DN<7..0>
PE_U1001_U1014_DN<7..0>
PE_U1001_CPU1_DP<15..0>
PE_U1001_CPU0_DP<15..0>
PE_U1001_U1003_DP<15..0>
PE_U1001_U1005_DP<0..15>
PE_U1001_U1019_DP<7..0>
PE_U1001_U1012_DP<7..0>
PE_U1001_U1016_DP<7..0>
PE_U1001_U1014_DP<7..0>
PE_CPU1_U1001_DN<15..0>
PE_CPU0_U1001_DN<15..0>
PE_U1003_U1001_DN<15..0>
PE_U1005_U1001_DN<0..15>
PE_U1019_U1001_DN<7..0>
PE_U1012_U1001_DN<7..0>
PE_U1016_U1001_DN<7..0>
PE_U1014_U1001_DN<7..0>
PE_CPU1_U1001_DP<15..0>
PE_CPU0_U1001_DP<15..0>
PE_U1003_U1001_DP<15..0>
PE_U1005_U1001_DP<0..15>
PE_U1019_U1001_DP<7..0>
PE_U1012_U1001_DP<7..0>
PE_U1016_U1001_DP<7..0>
PE_U1014_U1001_DP<7..0>
P1V8_PLX
I2C ADDRESS=1011_110B
[2] [1] [0] NOTES:
UPSTREAM 0 Z Z PORT 4
NT0 Z Z 0 PORT 12
NT1 1 1 1 NOT USED
STRAP_STNX_PORTCFG[1:0]
STATION CONFIG [1] [0]
0 X16 0 Z
1 X16 0 Z
2 X16 0 Z
3 X16 0 Z
4 X8X8 0 1
5 X8X8 0 1
U1001
JABIL
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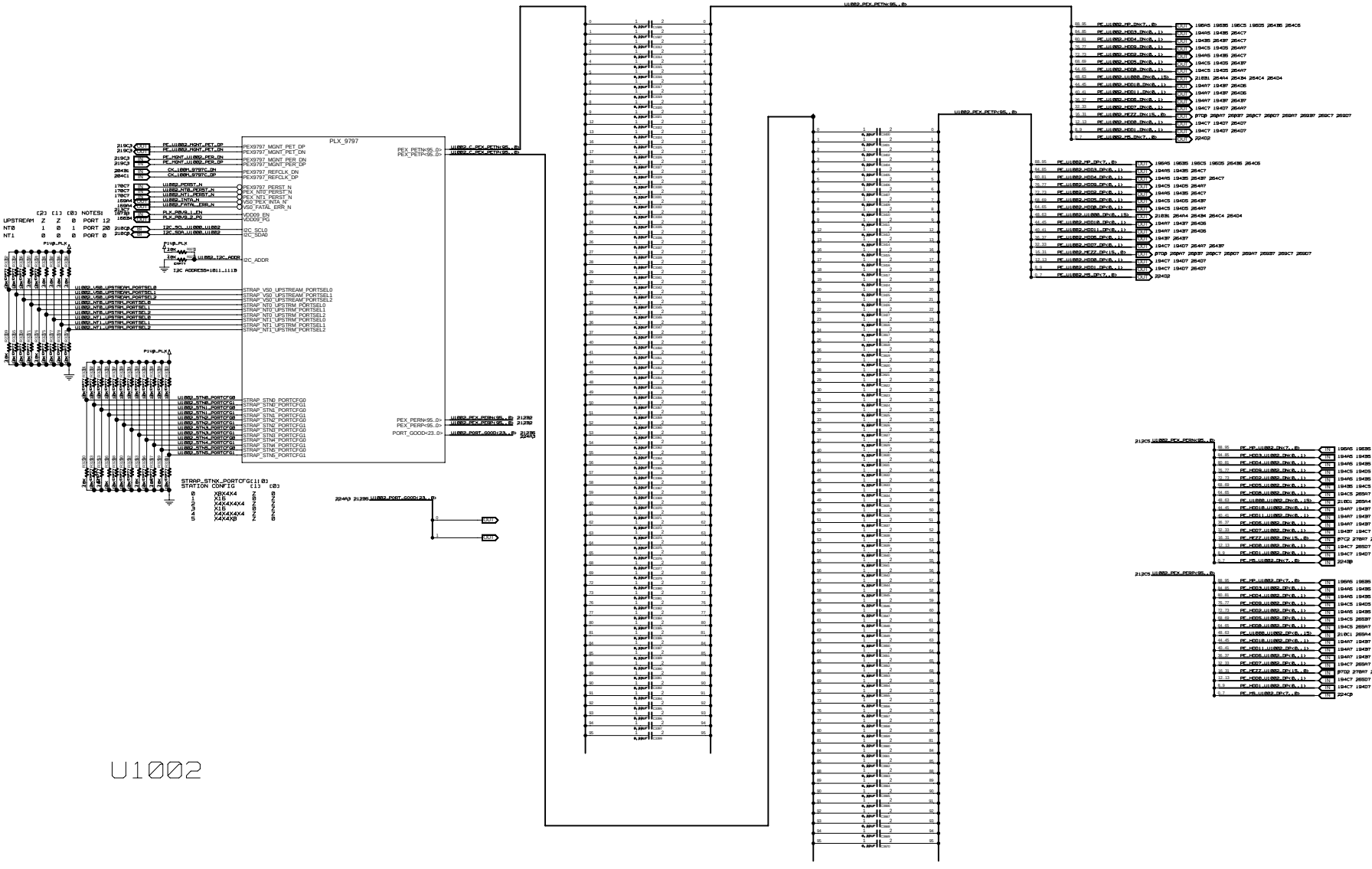
PEX9797 U1001 INTERFACE
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Thu Aug 07 21:10:36 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
211OF360



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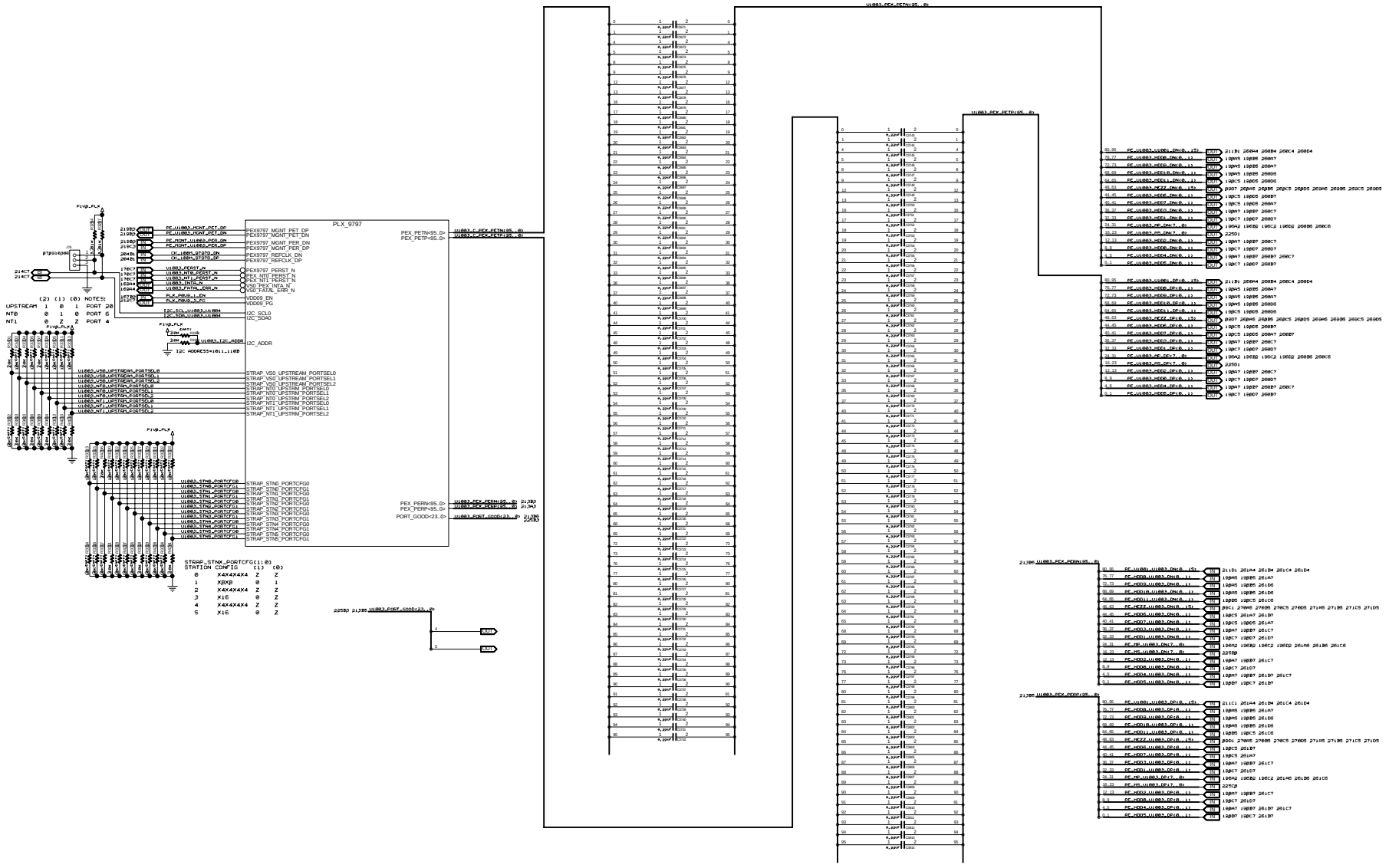

JABIL

wolfcreek_controller

wolfcreek_controller.cpm

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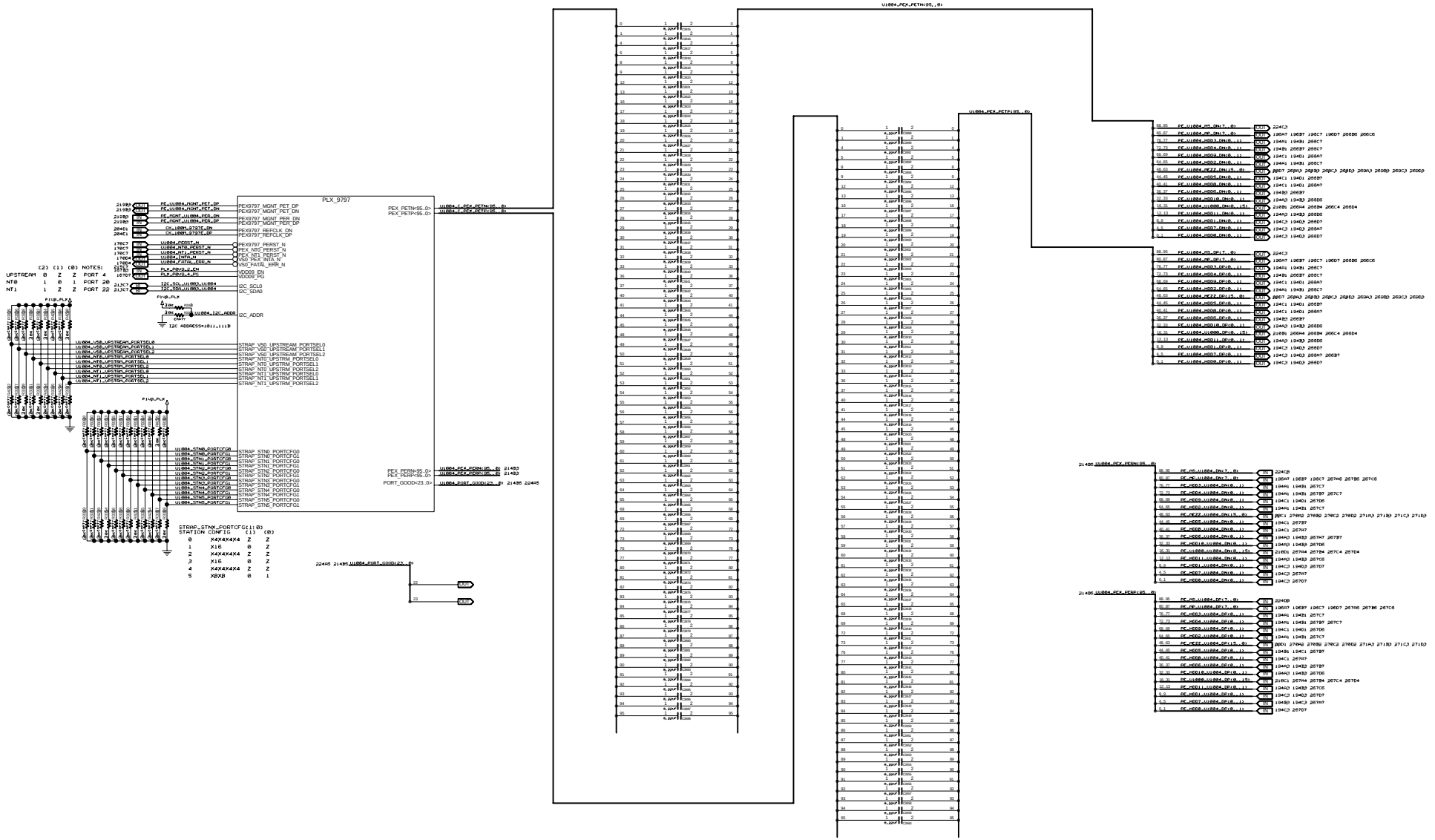
DATE: Thu Aug 07 18:04:14 2014

DWG NO: <DWG>

REV: A-0

DRAWNBY: <ENGINEER>

SHEET: 213OF360



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wolfcreek_controller

wolfcreek_controller.cpm

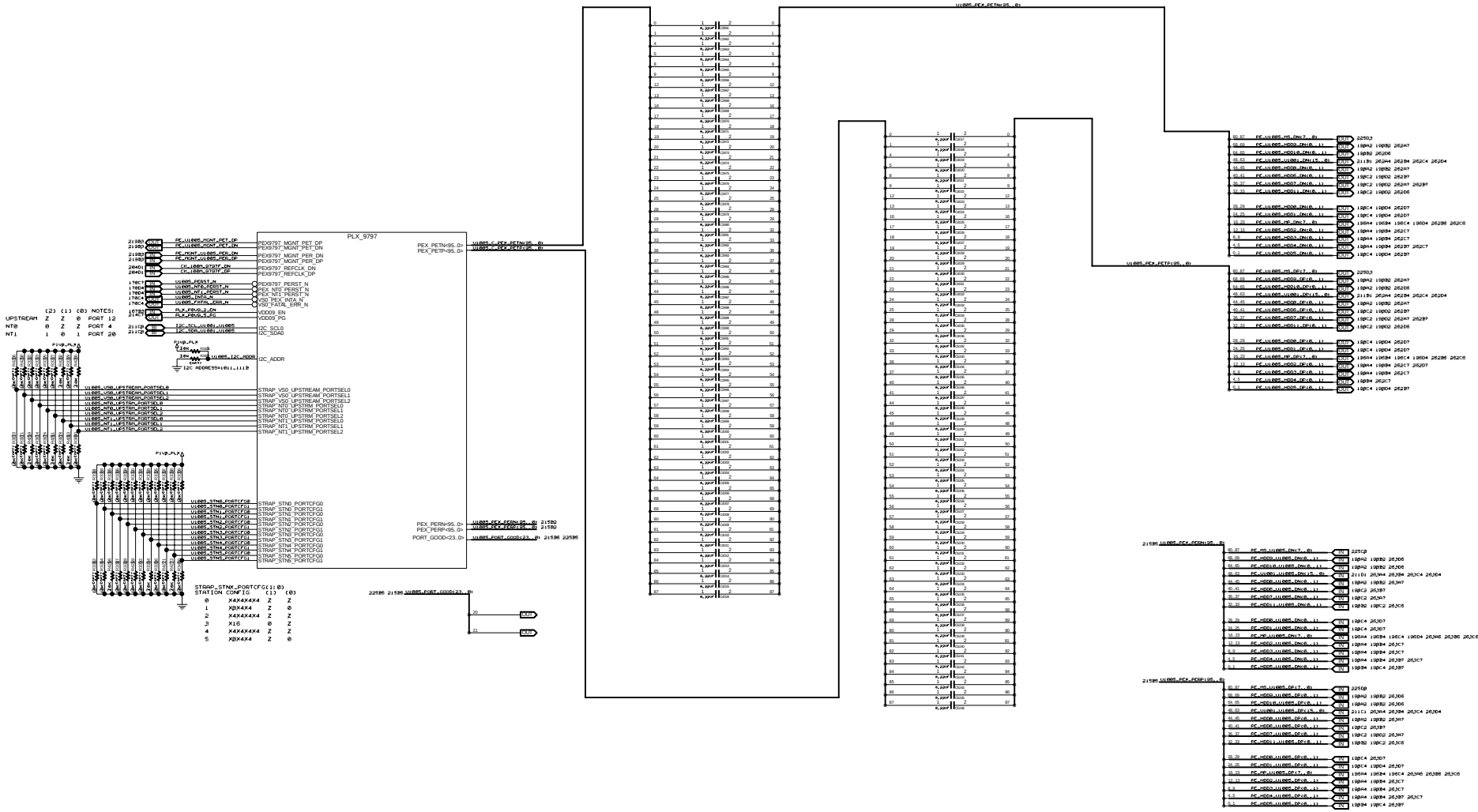
DATE: Thu Aug 07 17:52:44 2014

DWG NO: <DWG>

REV: A-0

DRAWNBY: <ENGINEER>

SHEET: 21 OF 360



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JABIL

wolfcreek_controller

wolfcreek_controller.cpm

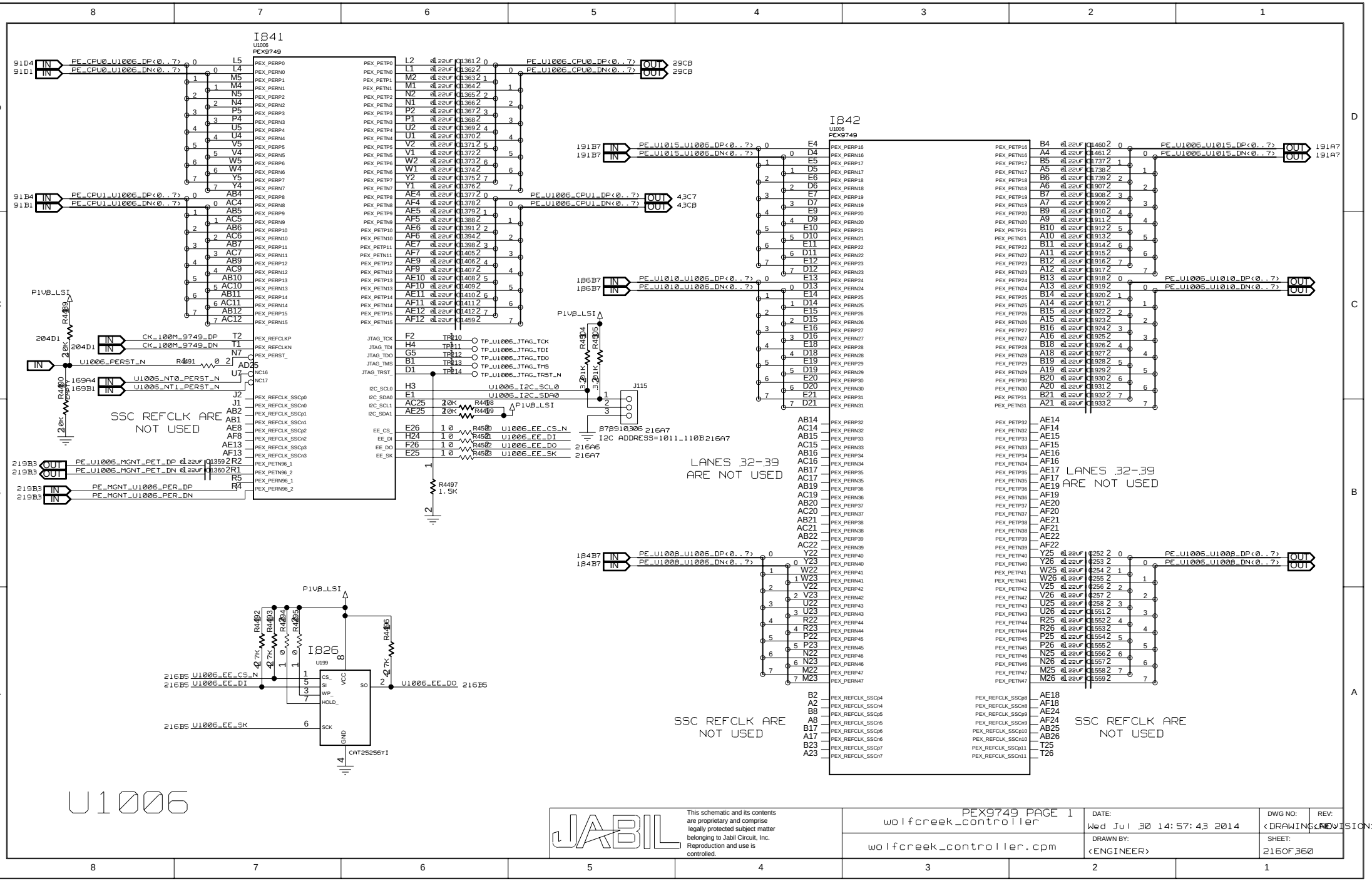
DATE: Thu Aug 07 18:04:17 2014

DRAWN BY: <ENGINEER>

DWG NO: <DWG>

REV: A-0

SHEET: 215OF360



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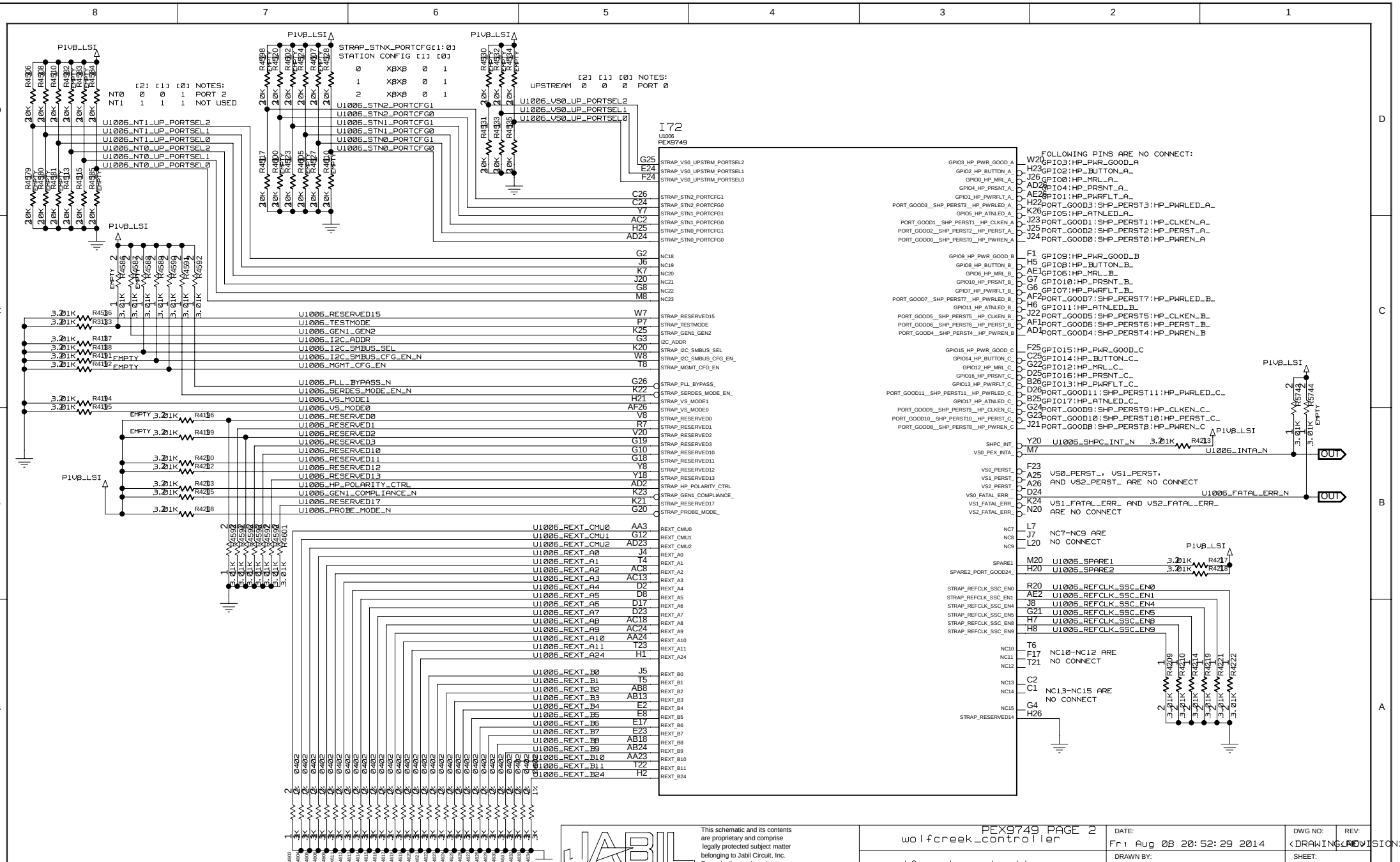
PEX9749 PAGE 1 wolfcreek_controller	DATE: Wed Jul 30 14:57:43 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 216OF360	


P1V8_LSI
STRAP_STNX_PORTCFG[1:0]
STATION CONFIG [1] [0]
0 X8X8 0 1
1 X8X8 0 1
2 X8X8 0 1
[2] [1] [0] NOTES:
NT0 0 0 1 PORT 2
NT1 1 1 1 NOT USED
UPSTREAM 0 0 0 PORT 0
U1006_STN2_PORTCFG1
U1006_STN2_PORTCFG0
U1006_STN1_PORTCFG1
U1006_STN1_PORTCFG0
U1006_STN0_PORTCFG1
U1006_STN0_PORTCFG0
U1006_VS0_UP_PORTSEL2
U1006_VS0_UP_PORTSEL1
U1006_VS0_UP_PORTSEL0
U1006_NT1_UP_PORTSEL2
U1006_NT1_UP_PORTSEL1
U1006_NT1_UP_PORTSEL0
U1006_NT0_UP_PORTSEL2
U1006_NT0_UP_PORTSEL1
U1006_NT0_UP_PORTSEL0
I72
U1006
PEX9749
FOLLOWING PINS ARE NO CONNECT:
U1006_RESERVED15
U1006_TESTMODE
U1006_GEN1_GEN2
U1006_I2C_ADDR
U1006_I2C_SMBUS_SEL
U1006_I2C_SMBUS_CFG_EN_N
U1006_MGMT_CFG_EN
U1006_PLL_BYPASS_N
U1006_SERDES_MODE_EN_N
U1006_VS_MODE1
U1006_VS_MODE0
U1006_RESERVED0
U1006_RESERVED1
U1006_RESERVED2
U1006_RESERVED3
U1006_RESERVED10
U1006_RESERVED11
U1006_RESERVED12
U1006_RESERVED13
U1006_HP_POLARITY_CTRL
U1006_GEN1_COMPLIANCE_N
U1006_RESERVED17
U1006_PROBE_MODE_N
U1006_REXT_CMU0
U1006_REXT_CMU1
U1006_REXT_CMU2
U1006_REXT_A0
U1006_REXT_A1
U1006_REXT_A2
U1006_REXT_A3
U1006_REXT_A4
U1006_REXT_A5
U1006_REXT_A6
U1006_REXT_A7
U1006_REXT_A8
U1006_REXT_A9
U1006_REXT_A10
U1006_REXT_A11
U1006_REXT_A24
U1006_REXT_B0
U1006_REXT_B1
U1006_REXT_B2
U1006_REXT_B3
U1006_REXT_B4
U1006_REXT_B5
U1006_REXT_B6
U1006_REXT_B7
U1006_REXT_B8
U1006_REXT_B9
U1006_REXT_B10
U1006_REXT_B11
U1006_REXT_B24
U1006_SHPC_INT_N
U1006_INTA_N
U1006_FATAL_ERR_N
OUT
VS0_PERST_, VS1_PERST,
AND VS2_PERST_ ARE NO CONNECT
VS1_FATAL_ERR_ AND VS2_FATAL_ERR_
ARE NO CONNECT
NC7-NC9 ARE
NO CONNECT
U1006_SPARE1
U1006_SPARE2
U1006_REFCLK_SSC_EN0
U1006_REFCLK_SSC_EN1
U1006_REFCLK_SSC_EN4
U1006_REFCLK_SSC_EN5
U1006_REFCLK_SSC_EN8
U1006_REFCLK_SSC_EN9
NC10-NC12 ARE
NO CONNECT
NC13-NC15 ARE
NO CONNECT
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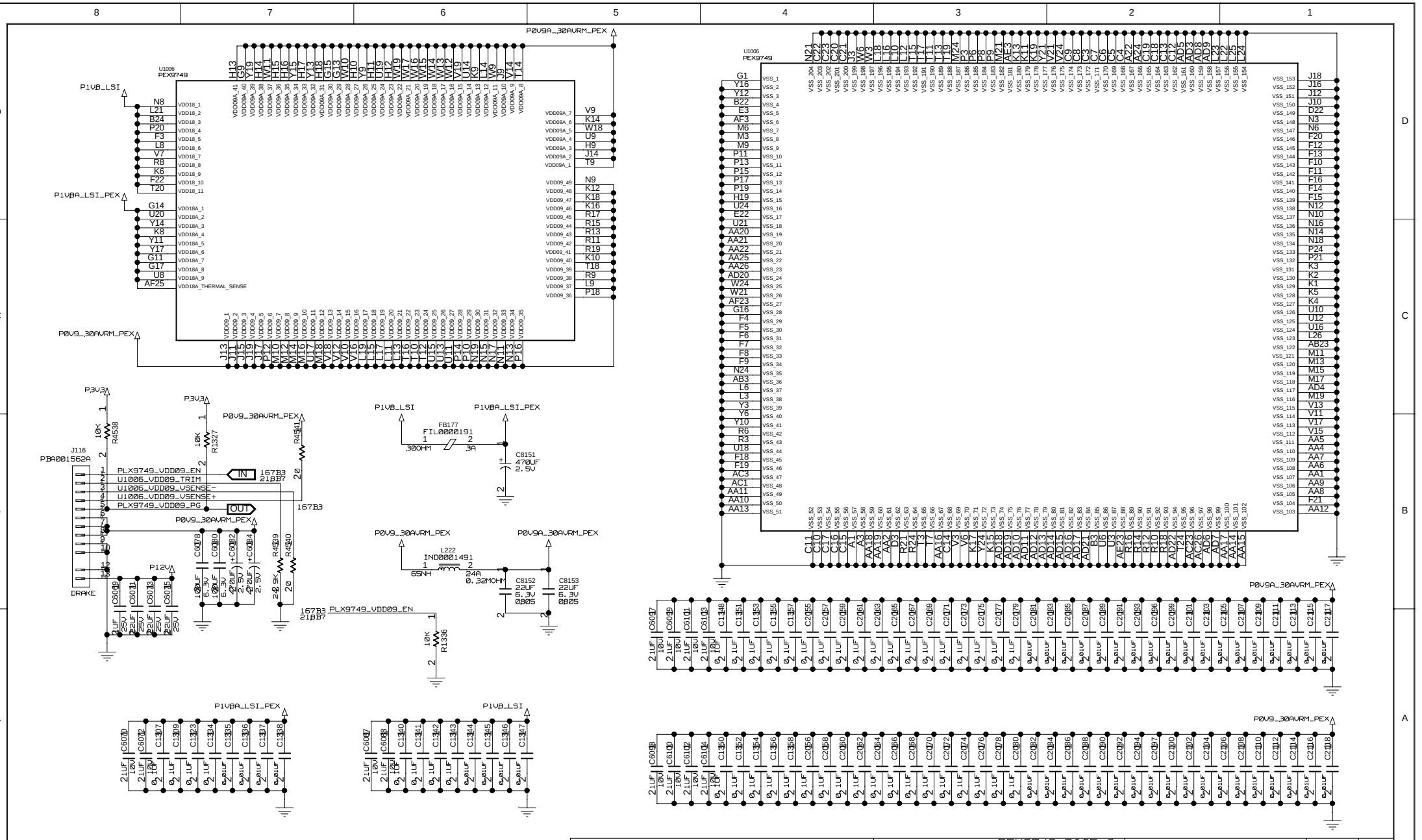
PEX9749 PAGE 2
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Fri Aug 08 20:52:29 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
217OF360



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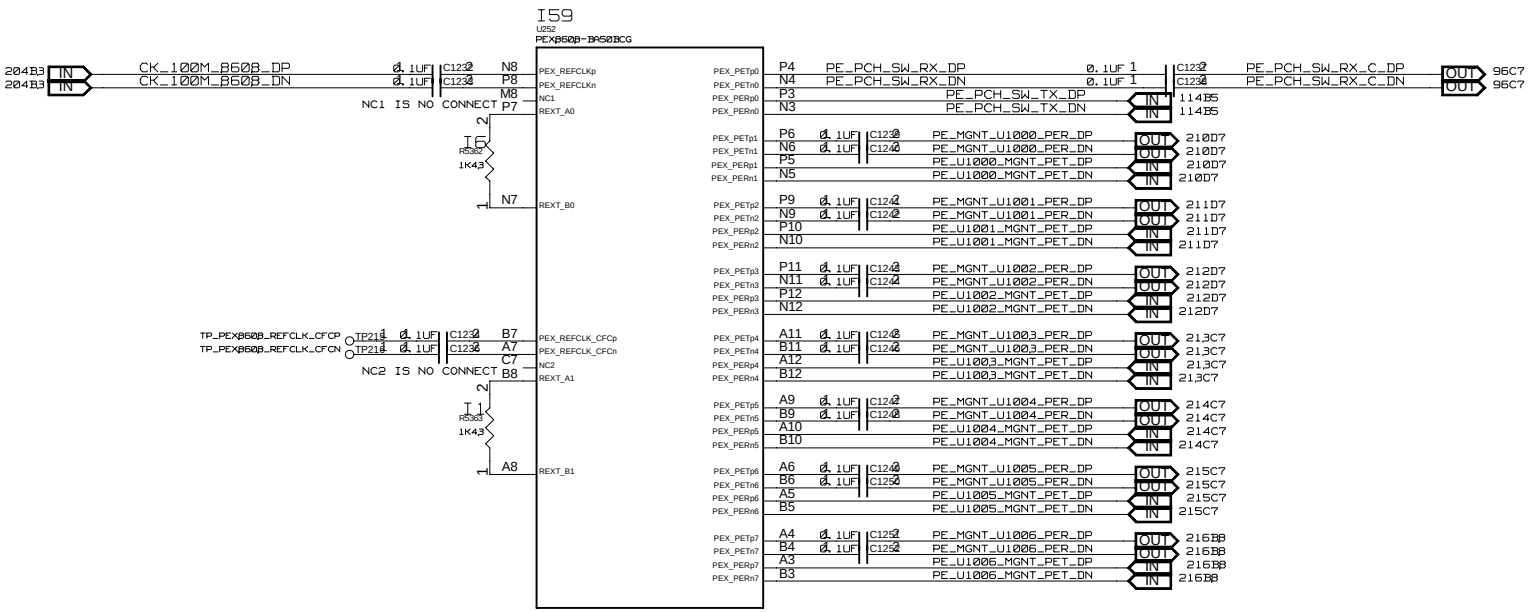
PEX9749 PAGE 3 wolfcreek_controller	DATE: Fri Aug 08 19:56:38 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 218OF360	



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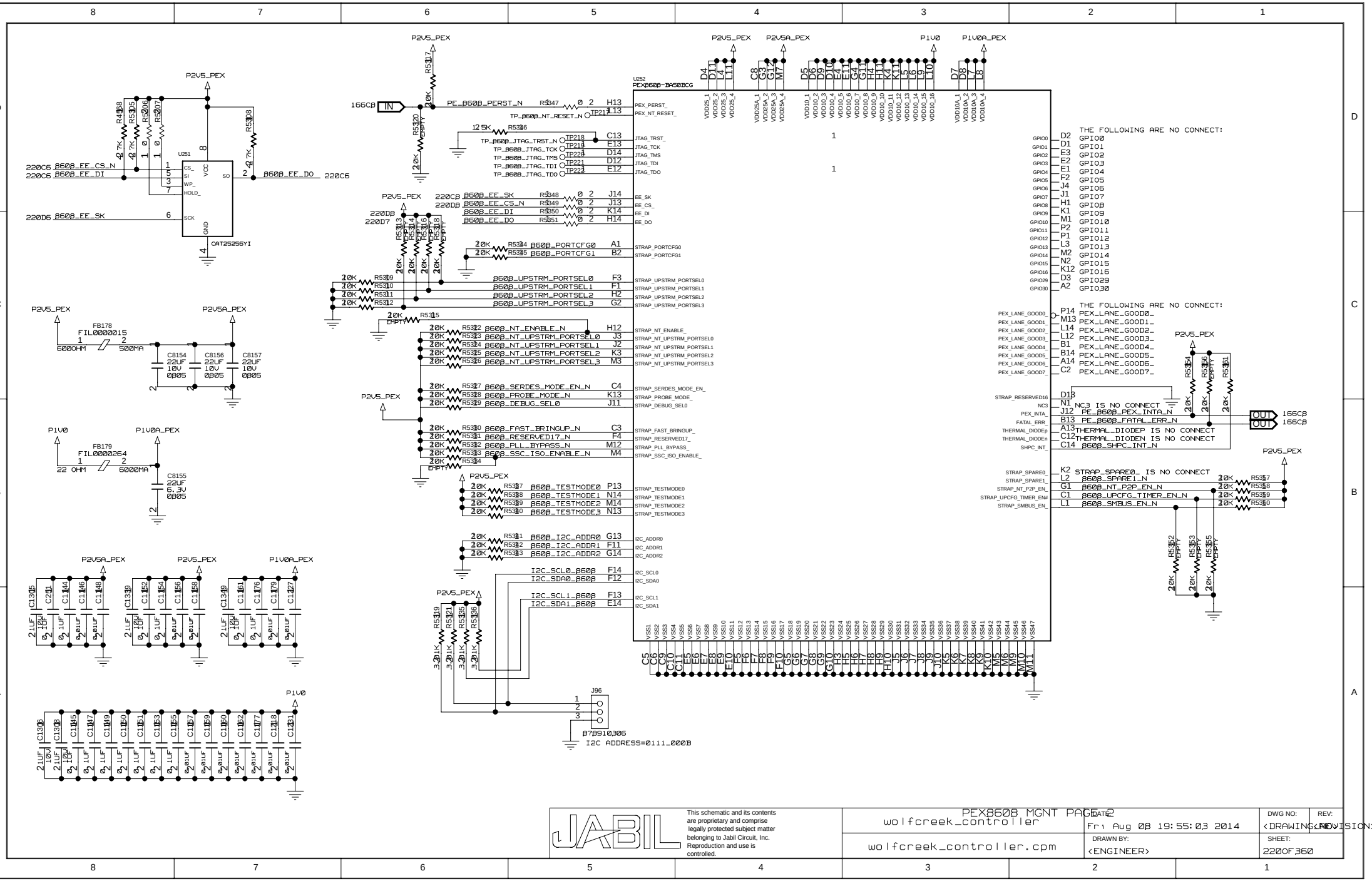
PEX8608 MGNT PAGE	DATE: Sat Aug 02 18:19:32 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: 219OF360	


U252
PEX8608-BA80BCG
U251
CAT25256YI
J96
B7B910306
I2C ADDRESS=0111_000B
THE FOLLOWING ARE NO CONNECT:
GPIO0 D2 GPIO0
GPIO1 D1 GPIO1
GPIO2 E3 GPIO2
GPIO3 E2 GPIO3
GPIO4 E1 GPIO4
GPIO5 F2 GPIO5
GPIO6 J4 GPIO6
GPIO7 J1 GPIO7
GPIO8 H1 GPIO8
GPIO9 K1 GPIO9
GPIO10 M1 GPIO10
GPIO11 P2 GPIO11
GPIO12 P1 GPIO12
GPIO13 L3 GPIO13
GPIO14 M2 GPIO14
GPIO15 N2 GPIO15
GPIO16 K12 GPIO16
GPIO29 D3 GPIO29
GPIO30 A2 GPIO30
THE FOLLOWING ARE NO CONNECT:
PEX_LANE_GOOD0_ P14 PEX_LANE_GOOD0_
PEX_LANE_GOOD1_ M13 PEX_LANE_GOOD1_
PEX_LANE_GOOD2_ L14 PEX_LANE_GOOD2_
PEX_LANE_GOOD3_ L12 PEX_LANE_GOOD3_
PEX_LANE_GOOD4_ B1 PEX_LANE_GOOD4_
PEX_LANE_GOOD5_ B14 PEX_LANE_GOOD5_
PEX_LANE_GOOD6_ A14 PEX_LANE_GOOD6_
PEX_LANE_GOOD7_ C2 PEX_LANE_GOOD7_
STRAP_RESERVED16 D13
NC3 N1 NC3 IS NO CONNECT
PEX_INTA_ J12 PE_B60B_PEX_INTA_N
FATAL_ERR_ B13 PE_B60B_FATAL_ERR_N
THERMAL_DIODEp A13 THERMAL_DIODEP IS NO CONNECT
THERMAL_DIODEn C12 THERMAL_DIODEN IS NO CONNECT
SHPC_INT_ C14 B60B_SHPC_INT_N
STRAP_SPARE0_ K2 STRAP_SPARE0_ IS NO CONNECT
STRAP_SPARE1_ L2 B60B_SPARE1_N
STRAP_NT_P2P_EN_ G1 B60B_NT_P2P_EN_N
STRAP_UPCFG_TIMER_EN_ C1 B60B_UPCFG_TIMER_EN_N
STRAP_SMBUS_EN_ L1 B60B_SMBUS_EN_N
166CB IN
PE_B60B_PERST_N
TP_B60B_NT_RESET_N
TP_B60B_JTAG_TRST_N
TP_B60B_JTAG_TCK
TP_B60B_JTAG_TMS
TP_B60B_JTAG_TDI
TP_B60B_JTAG_TDO
220C6 B60B_EE_CS_N
220C6 B60B_EE_DI
B60B_EE_DO 220C6
220D6 B60B_EE_SK
220C8 B60B_EE_SK
220D8 B60B_EE_CS_N
B60B_EE_DI
B60B_EE_DO
220D8
220D7
B60B_PORTCFG0
B60B_PORTCFG1
B60B_UPSTRM_PORTSEL0
B60B_UPSTRM_PORTSEL1
B60B_UPSTRM_PORTSEL2
B60B_UPSTRM_PORTSEL3
B60B_NT_ENABLE_N
B60B_NT_UPSTRM_PORTSEL0
B60B_NT_UPSTRM_PORTSEL1
B60B_NT_UPSTRM_PORTSEL2
B60B_NT_UPSTRM_PORTSEL3
B60B_SERDES_MODE_EN_N
B60B_PROBE_MODE_N
B60B_DEBUG_SEL0
B60B_FAST_BRINGUP_N
B60B_RESERVED17_N
B60B_PLL_BYPASS_N
B60B_SSC_ISO_ENABLE_N
B60B_TESTMODE0
B60B_TESTMODE1
B60B_TESTMODE2
B60B_TESTMODE3
B60B_I2C_ADDR0
B60B_I2C_ADDR1
B60B_I2C_ADDR2
I2C_SCL0_B60B
I2C_SDA0_B60B
I2C_SCL1_B60B
I2C_SDA1_B60B
166CB OUT
166CB OUT
FB178 FIL0000015 6000HM 500MA
FB179 FIL0000264 22 OHM 6000MA
C8154 22UF 10V 0805
C8156 22UF 10V 0805
C8157 22UF 10V 0805
C8155 22UF 6.3V 0805
P2V5_PEX
P2V5A_PEX
P1V0
P1V0A_PEX
PEX8608 MGNT PAGE
wolfcreek_controller
wolfcreek_controller.cpm
DATE:
Fri Aug 08 19:55:03 2014
DRAWN BY:
<ENGINEER>
DWG NO:
<DRAWING>
REV:
<REVISION>
SHEET:
220OF360
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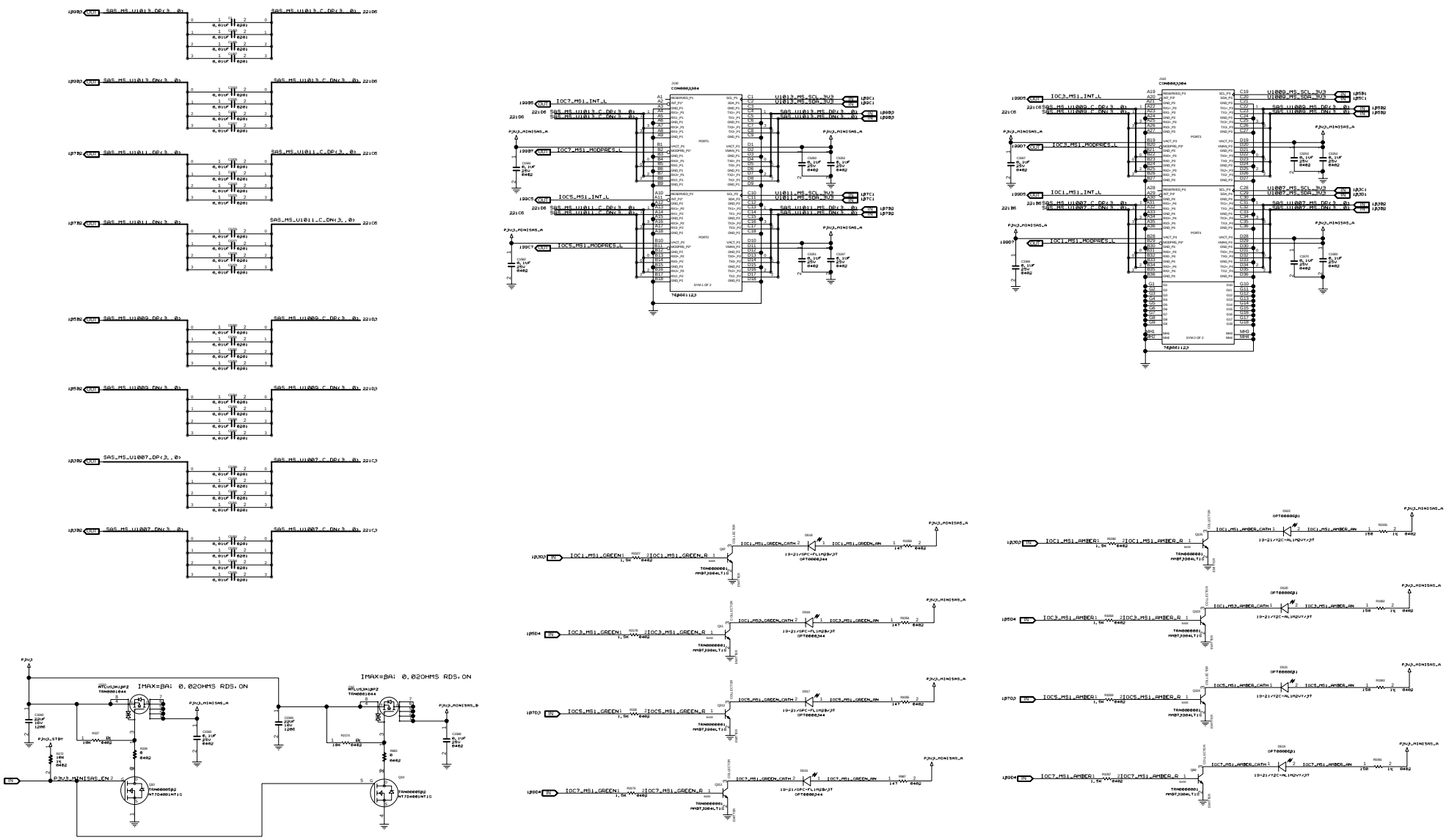
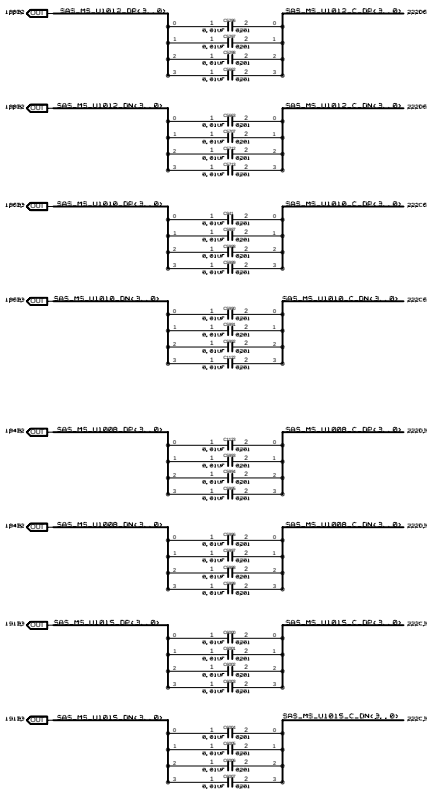
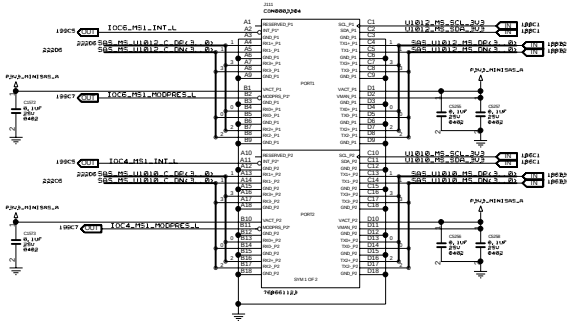
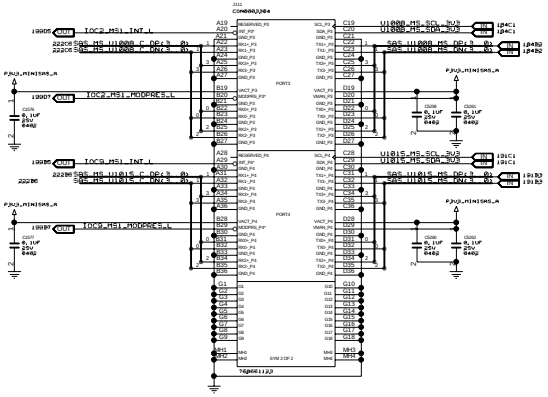
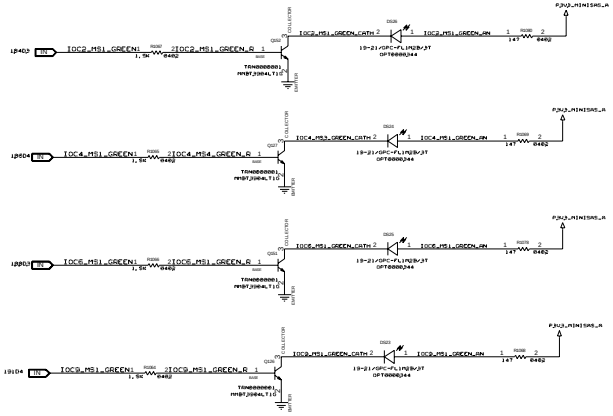
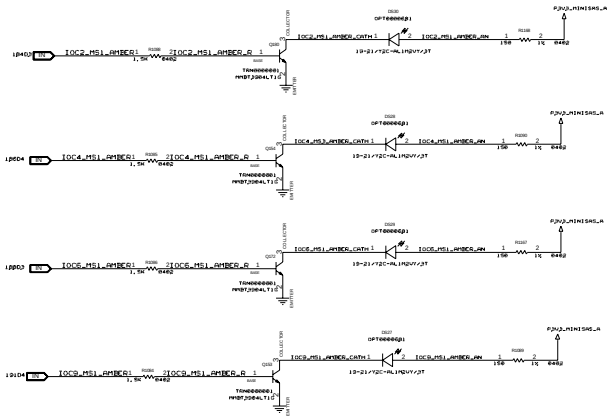

IMAX=BA: 0.020HMS RDS.ON
IMAX=BA: 0.020HMS RDS.ON
JABIL
wolfcreek_controller
wolfcreek_controller.cpm
Fri Aug 08 19:44:07 2014
<ENGINEER>
2210F360











JABIL

wolfcreek_controller

wolfcreek_controller.cpm

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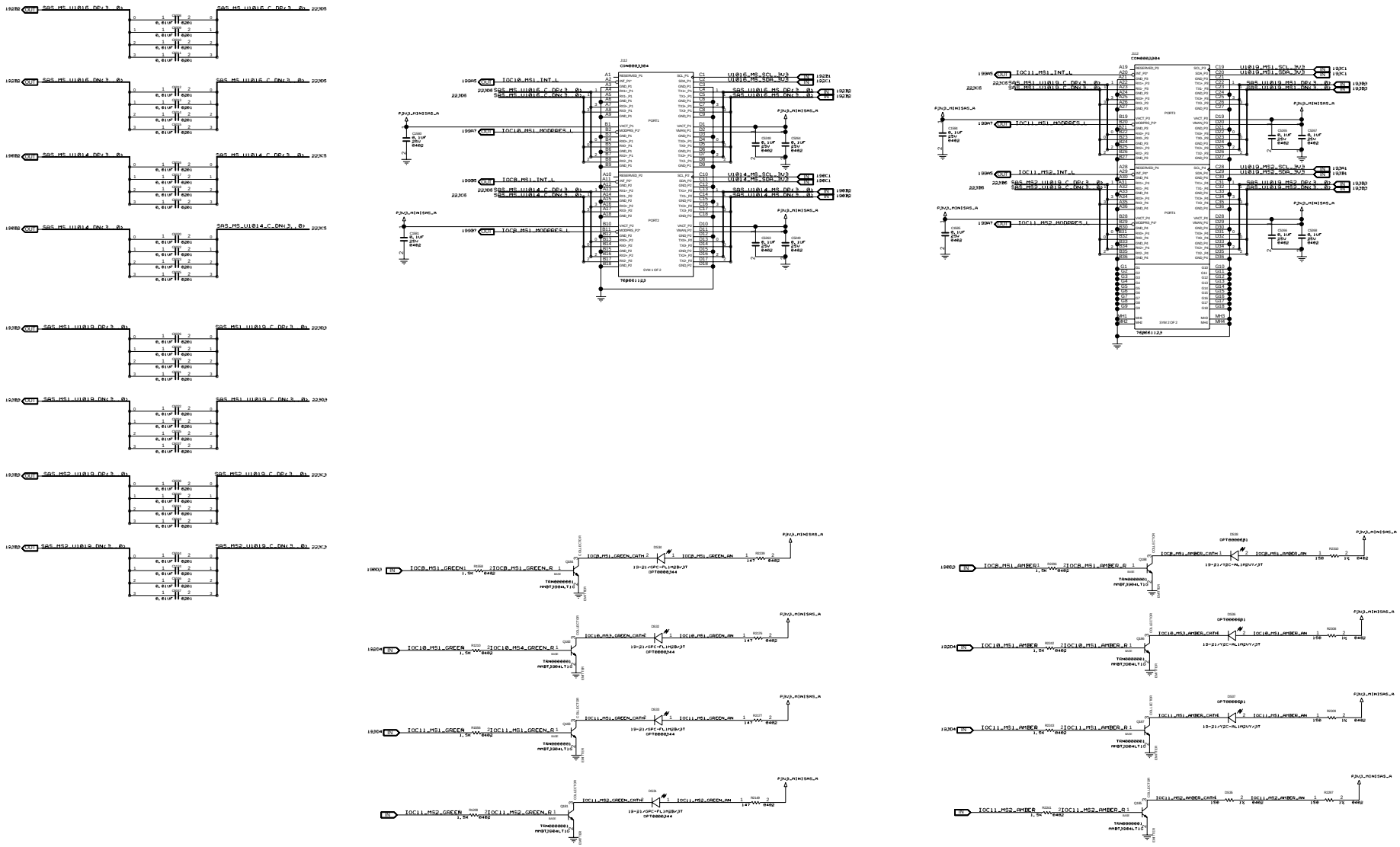
DATE: Fri Aug 08 19:43:16 2014

DWG NO: <DWG>

REV: A-0

DRAWNBY: <ENGINEER>

SHEET: 222OF360



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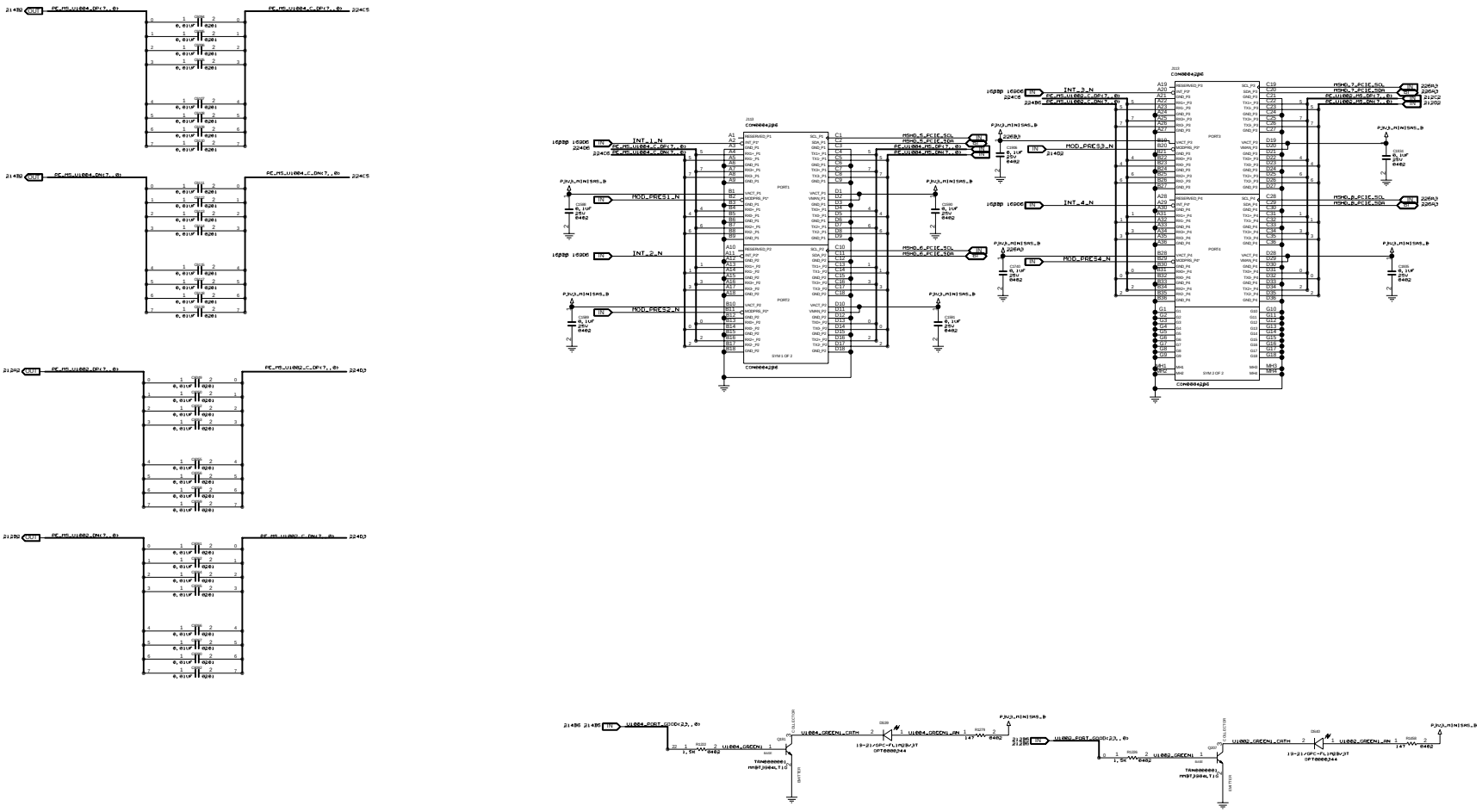
JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
DATE: Fri Aug 08 19:43:29 2014	DWG NO: (DWG) REV: A-0
DRAWNBY: <ENGINEER>	SHEET: 22 OF 360



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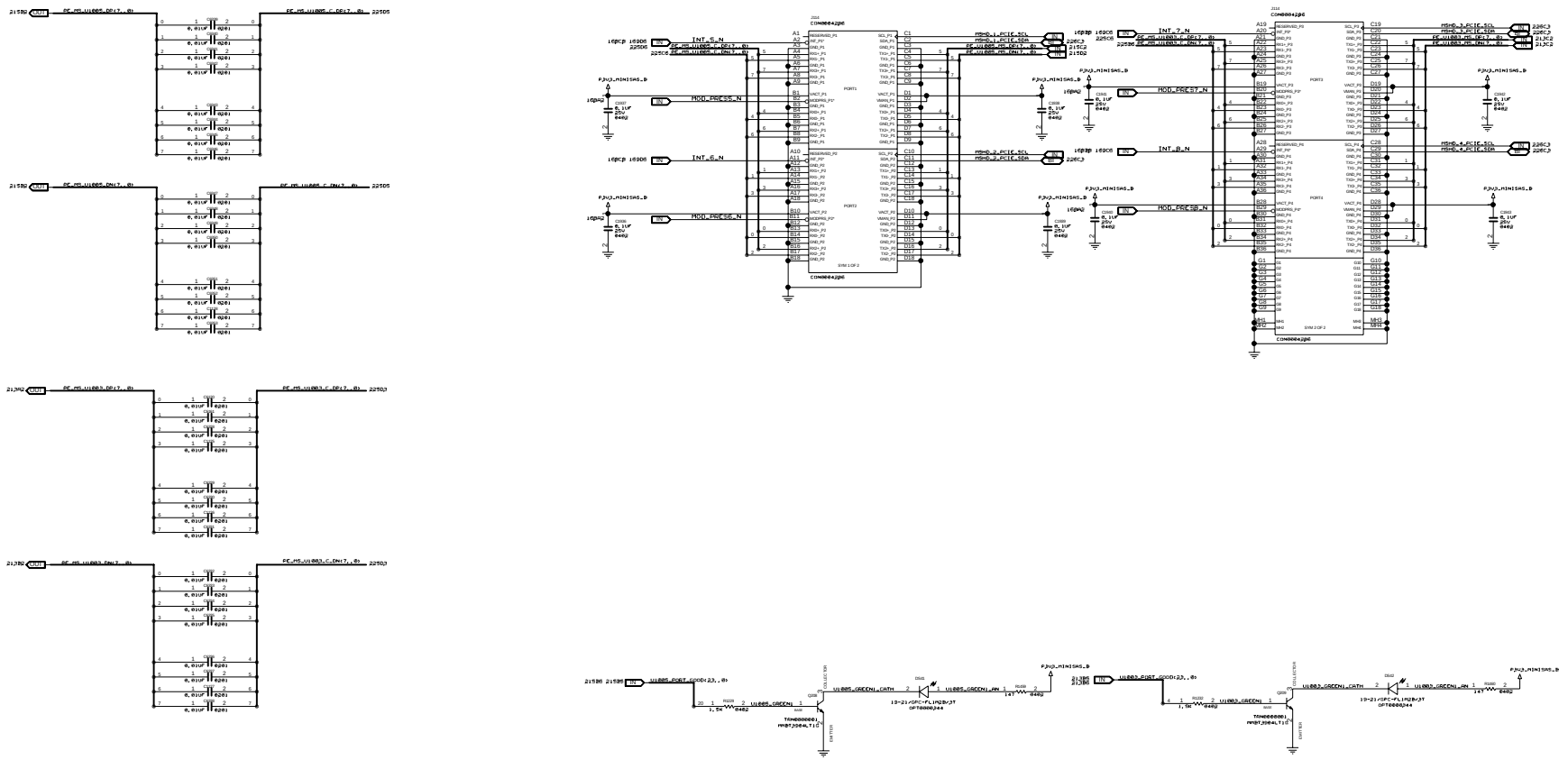
wolfcreek_controller	
wolfcreek_controller.cpm	
DATE: Fri Aug 08 19:43:41 2014	DWG NO: <DWG> REV: A-0
DRAWN BY: <ENGINEER>	SHEET: 224OF360



JABIL

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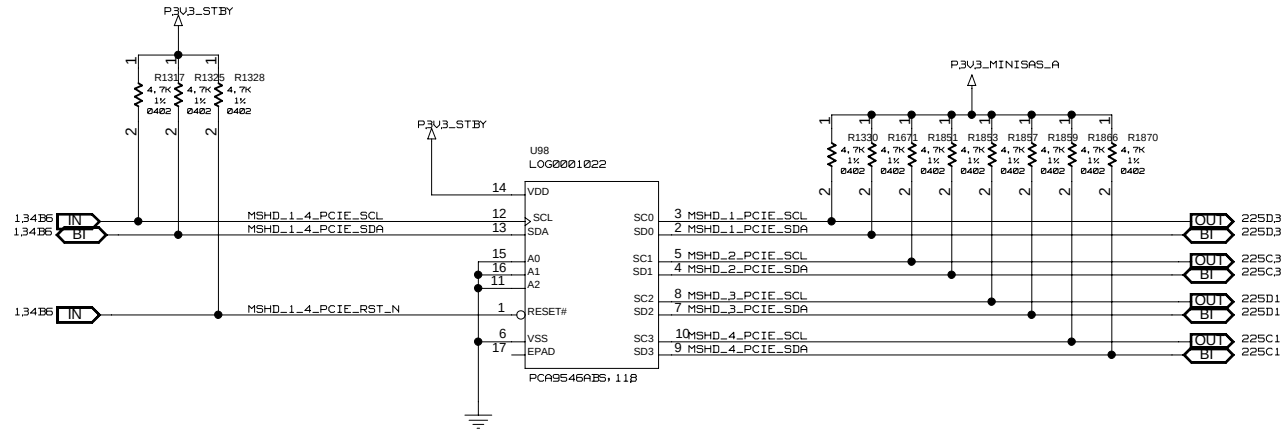
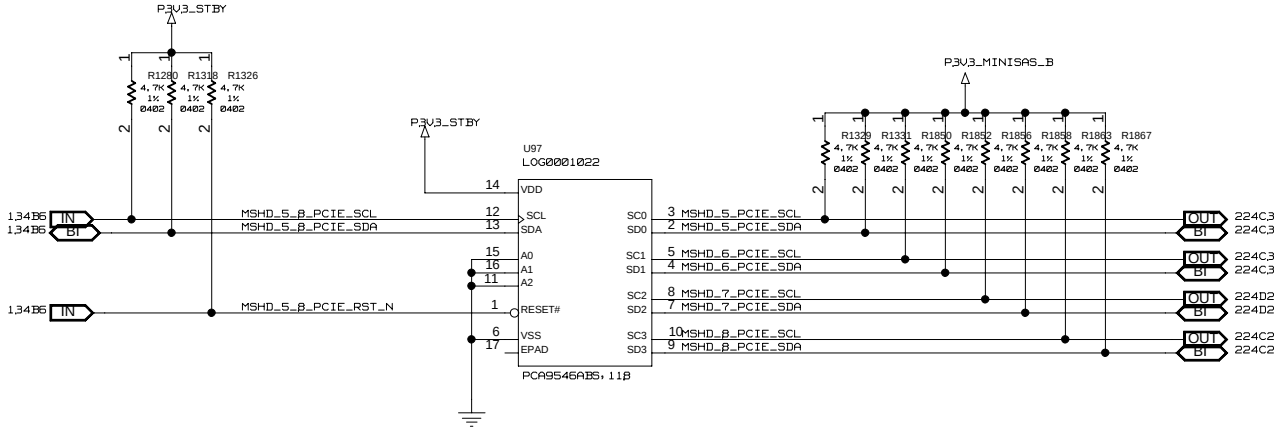
wolfcreek_controller

wolfcreek_controller.cpm

DATE:	Fri Aug 08 19:43:55 2014	DWG NO: <DWG>	REV: A-0
DRAWN BY:	<ENGINEER>	SHEET: 225OF360	





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MINI-SAS HD PCIE I2C MUX

wolfcreek_controller

wolfcreek_controller.cpm

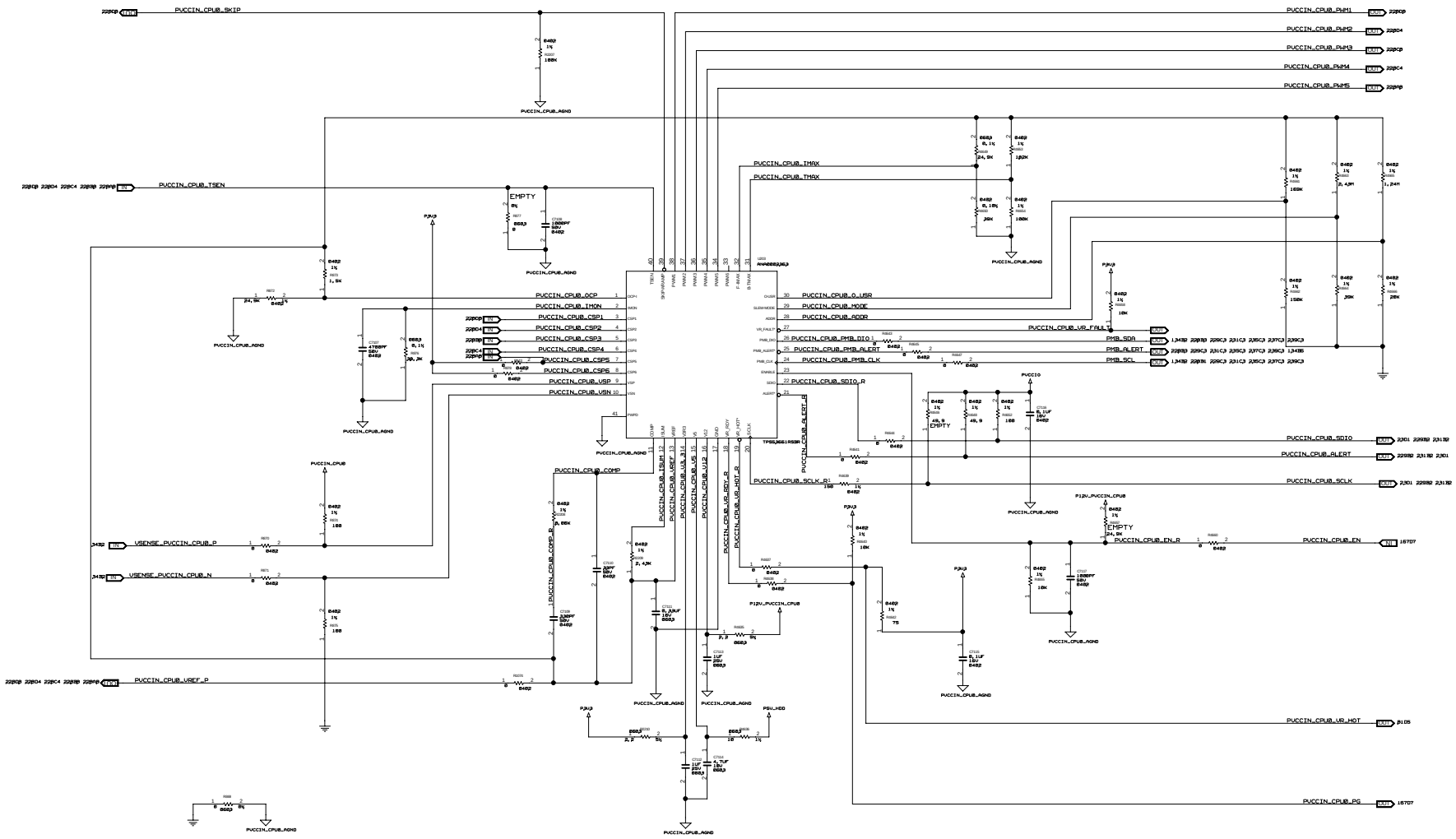
DATE: Wed Jul 30 14:59:55 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 226OF360



DESIGN SPEC:

VR12.5 GRANTLEY EP 120W
OUTPUT VOLTAGE: 1.82V
ICC TDC/PEAK: 73A/156A
MAX STEP LOAD: 109A
VBOOT: 1.7V
SVID ADDRESS: 0000
PMBUS ADDRESS: 1100000
SWITCHING FREQUENCY: 600K
PER-PHASE VALLEY CURRENT: 51A

PUCCIN_CPU0_1

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
DATE: Fri Aug 08 14:41:14 2014	DWG NO: <DWG> REV: A-0
DRAWN BY: <ENGINEER>	SHEET: 227OF350

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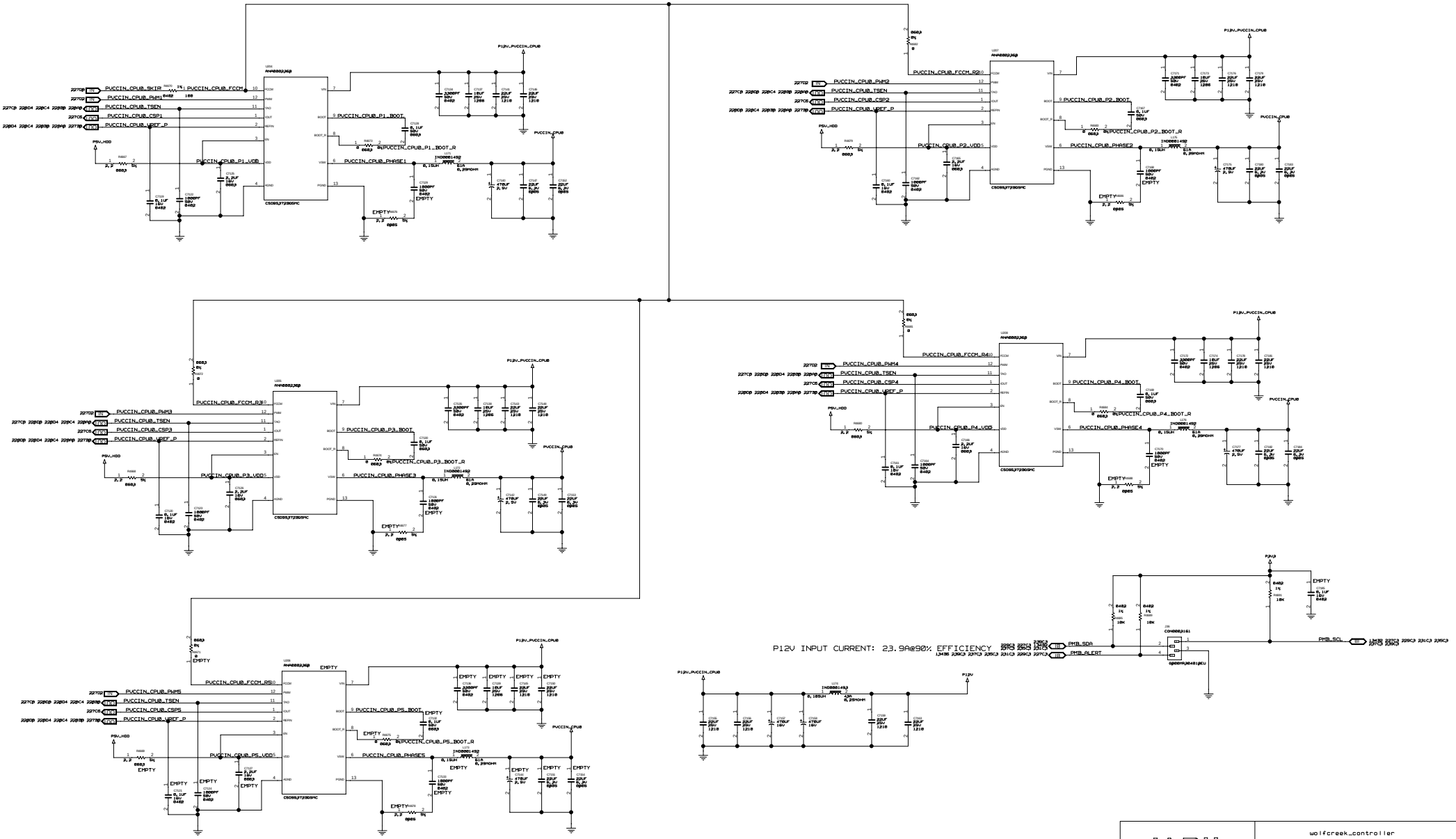
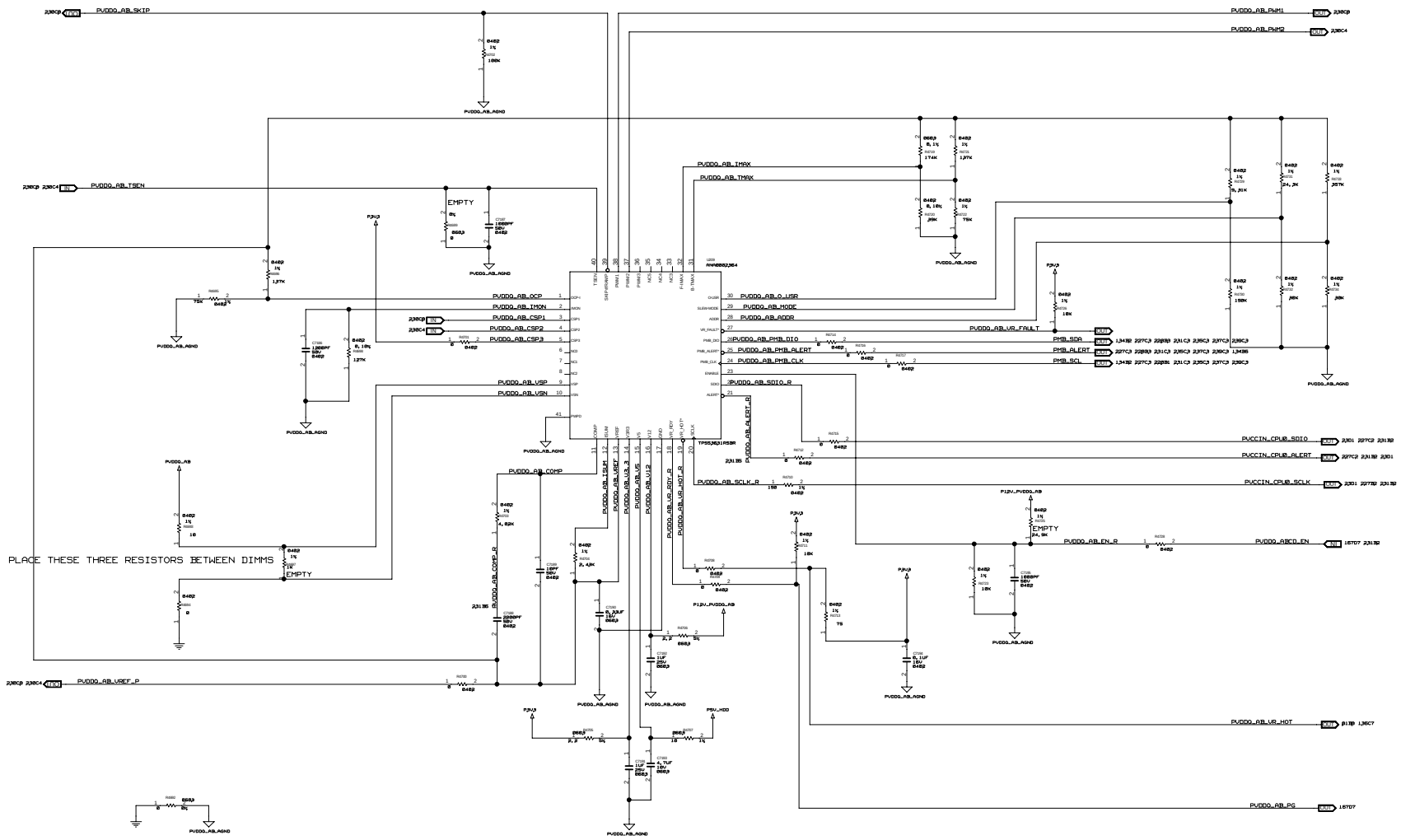

PUCCIN_CPU0_SKIP
PUCCIN_CPU0_PWM1
PUCCIN_CPU0_TSEN
PUCCIN_CPU0_CSP1
PUCCIN_CPU0_VREF_P
PUCCIN_CPU0_FCCM_R3
PUCCIN_CPU0_PWM3
PUCCIN_CPU0_CSP3
PUCCIN_CPU0_P3_BOOT
PUCCIN_CPU0_P3_BOOT_R
PUCCIN_CPU0_P3_VDD
PUCCIN_CPU0_PHASE3
PUCCIN_CPU0_FCCM_R5
PUCCIN_CPU0_PWM5
PUCCIN_CPU0_CSP5
PUCCIN_CPU0_P5_BOOT
PUCCIN_CPU0_P5_BOOT_R
PUCCIN_CPU0_P5_VDD
PUCCIN_CPU0_PHASE5
P12V_PUCCIN_CPU0
PUCCIN_CPU0
PSV_HDD
P12V INPUT CURRENT: 23.9A@90% EFFICIENCY
PMB_SDA
PMB_ALERT
PMB_SCL
P12V
JABIL
wolfcreek_controller
wolfcreek_controller.cpm
Thu Aug 07 20:32:44 2014
A-0
22B0F360
PVCCIN_CPU0_2



DESIGN SPEC:

VR12.5 GRANTLEY EP 4DIMM
OUTPUT VOLTAGE: 1.2V
ICC TDC/PEAK: 34.8A/53.7A
MAX STEP LOAD: 26.8A
VBOOT:1.2V
SVID ADDRESS: 0010
PMBUS ADDRESS: 1100010
SWITCHING FREQUENCY: 600K
PER-PHASE VALLEY CURRENT: 39A

PVDDQ_AB_1

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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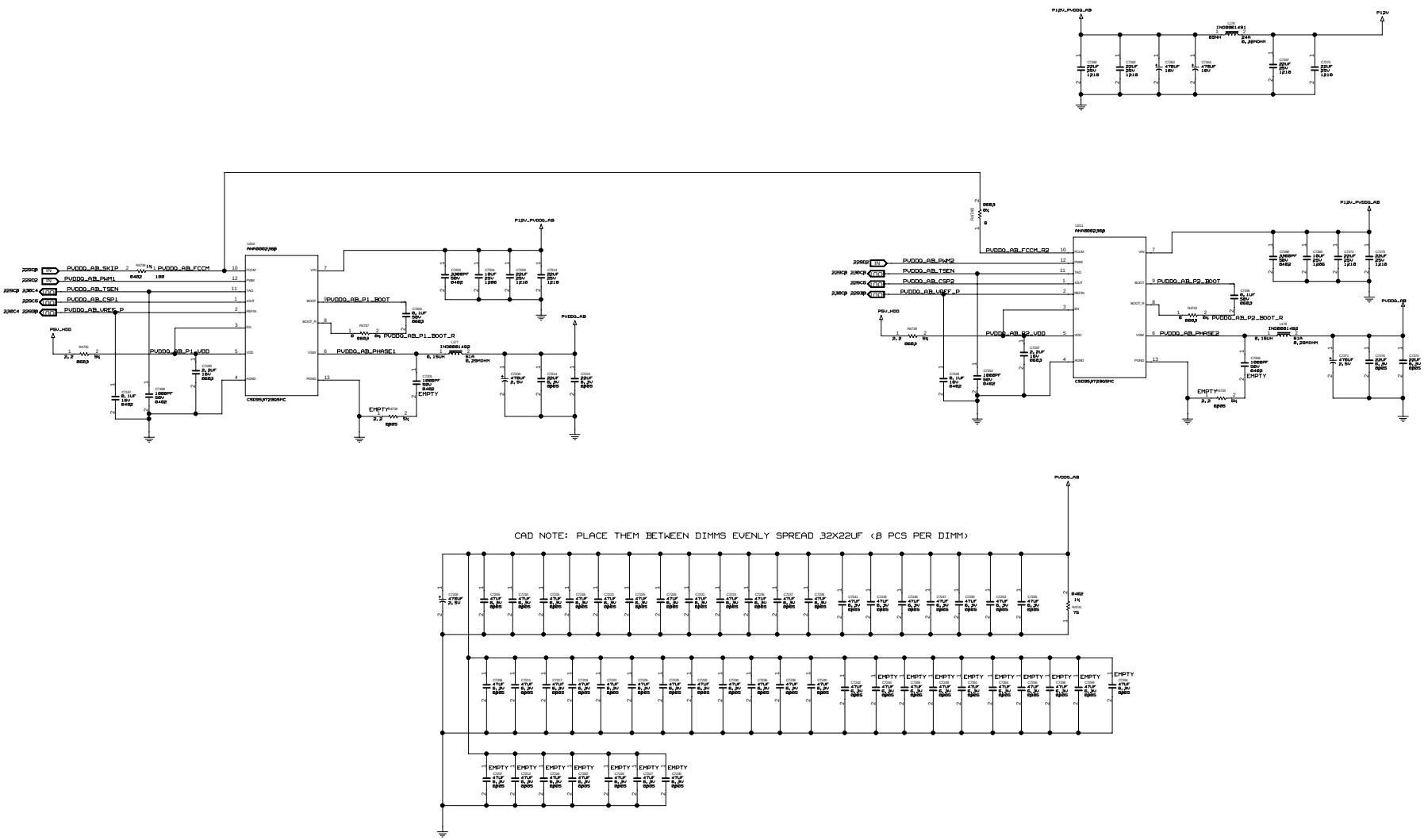
	DRAWN BY: <ENGINEER> · SHEET: 229OF360

P12V INPUT CURRENT: 5.97A@90% EFFICIENCY



PVDDQ_AB_2

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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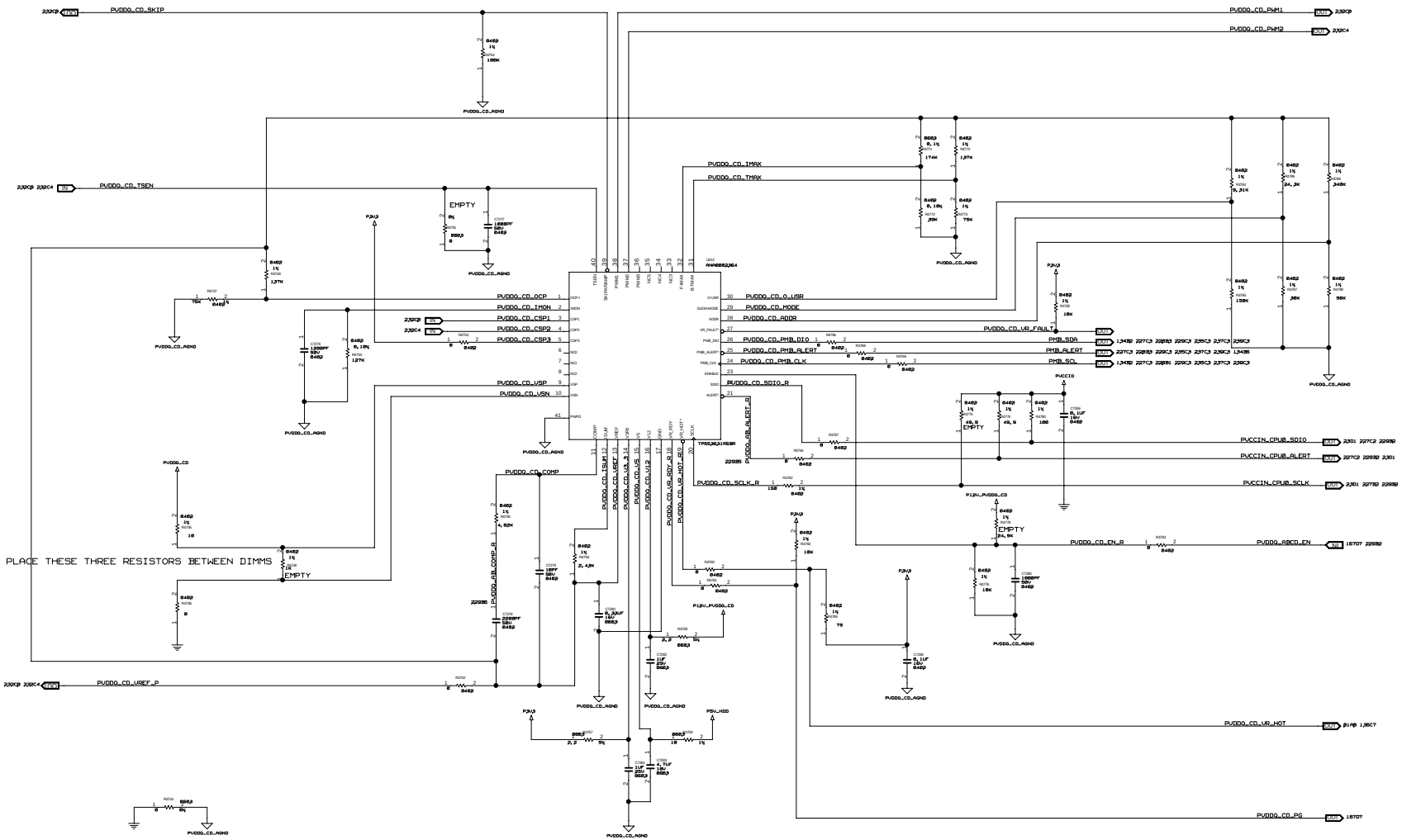
	DRAWN BY: <ENGINEER> · SHEET: 23OF360



DESIGN SPEC:

VR12.5 GRANTLEY EP 4DIMM
OUTPUT VOLTAGE: 1.2V
ICC TDC/PEAK: 34.8A/53.7A
MAX STEP LOAD: 26.8A
VBOOT: 1.2V
SVID ADDRESS: 0100
PMBUS ADDRESS: 1100100
SWITCHING FREQUENCY: 600K
PER-PHASE VALLEY CURRENT: 39A

PVDDQ_CD_1

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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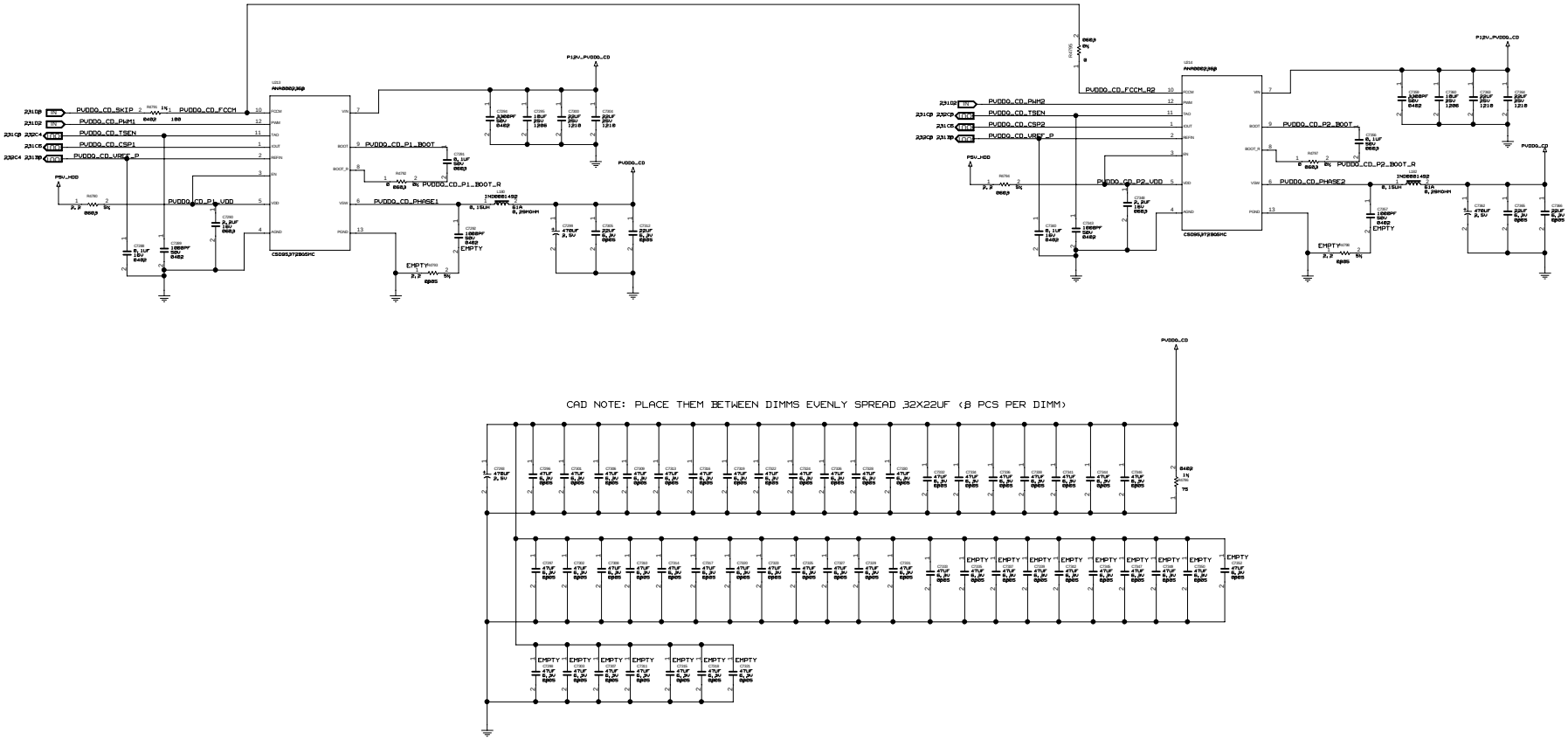
	DRAWN BY: <ENGINEER> · SHEET: 231OF360

P12V INPUT CURRENT: 5.97A@90% EFFICIENCY



PVDDQ_CD_2

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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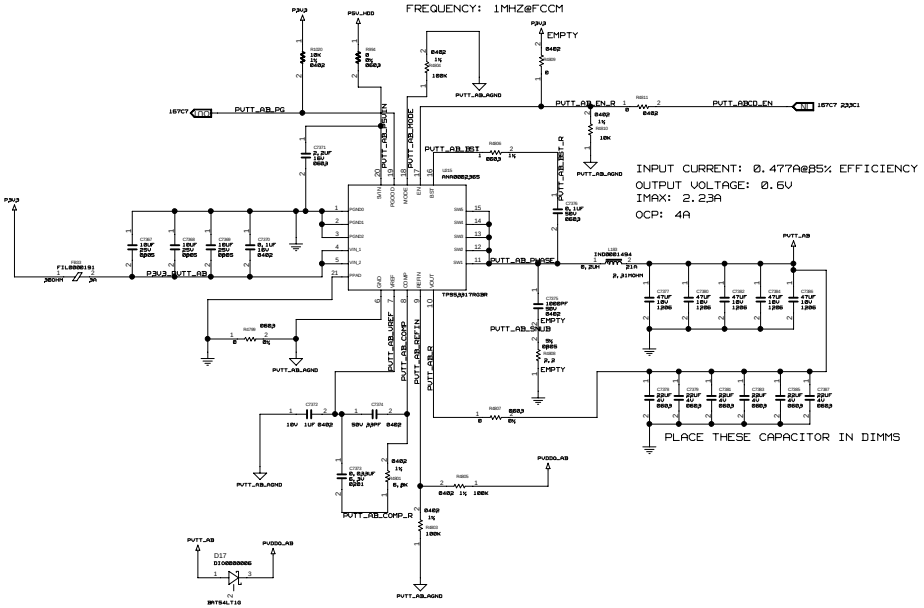
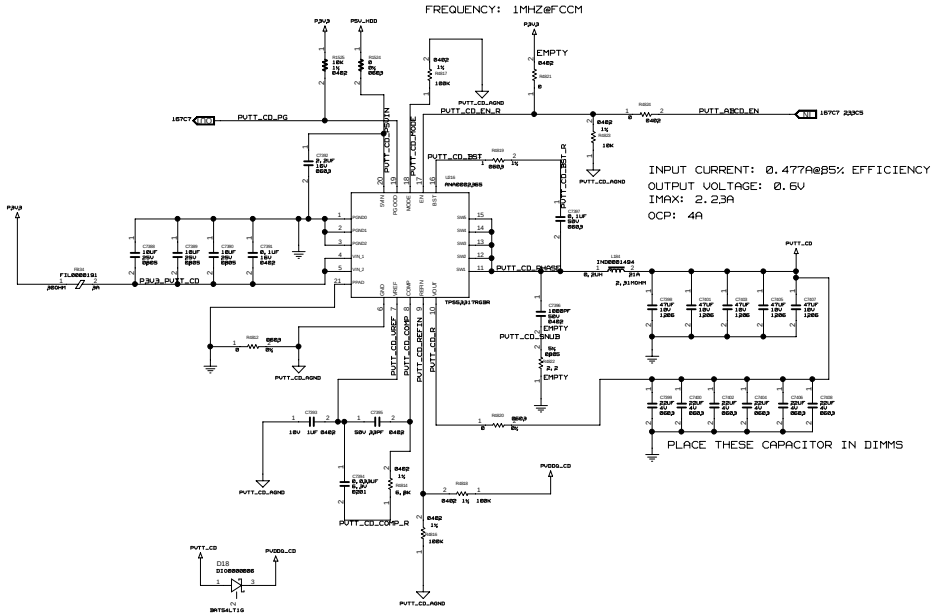
	DRAWN BY: <ENGINEER> — SHEET: 23 OF 360





PVTT_ABCD

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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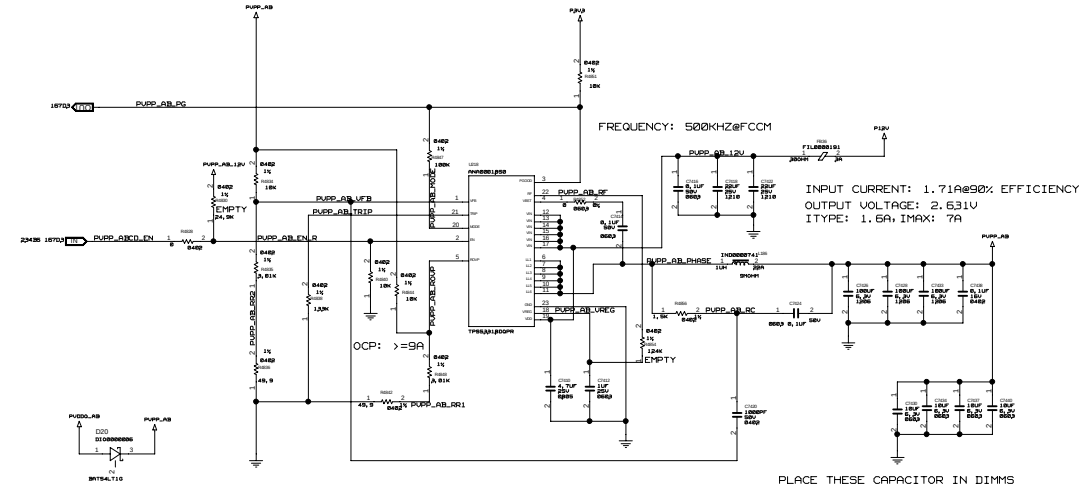
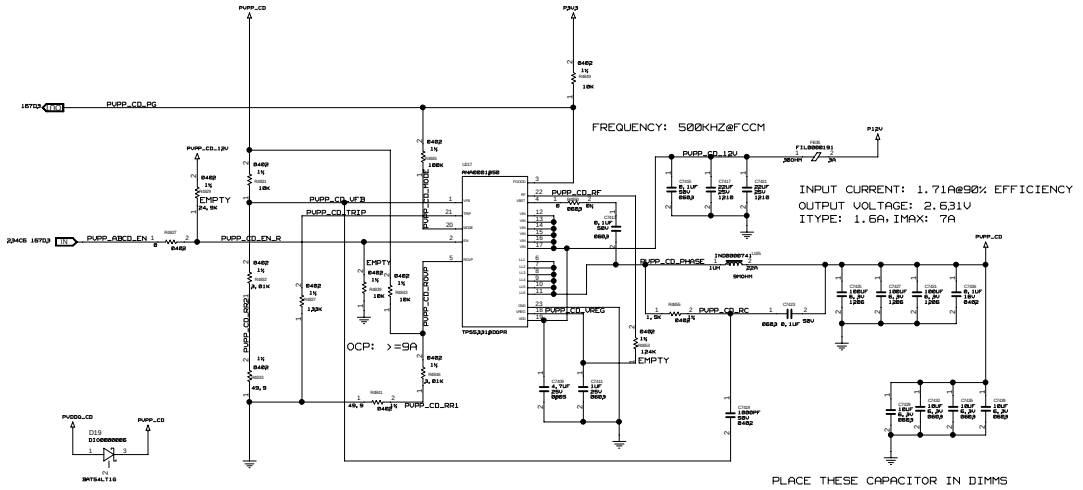
	DRAWN BY: <ENGINEER> — SHEET: 23,330F360





PVPP_ABCD

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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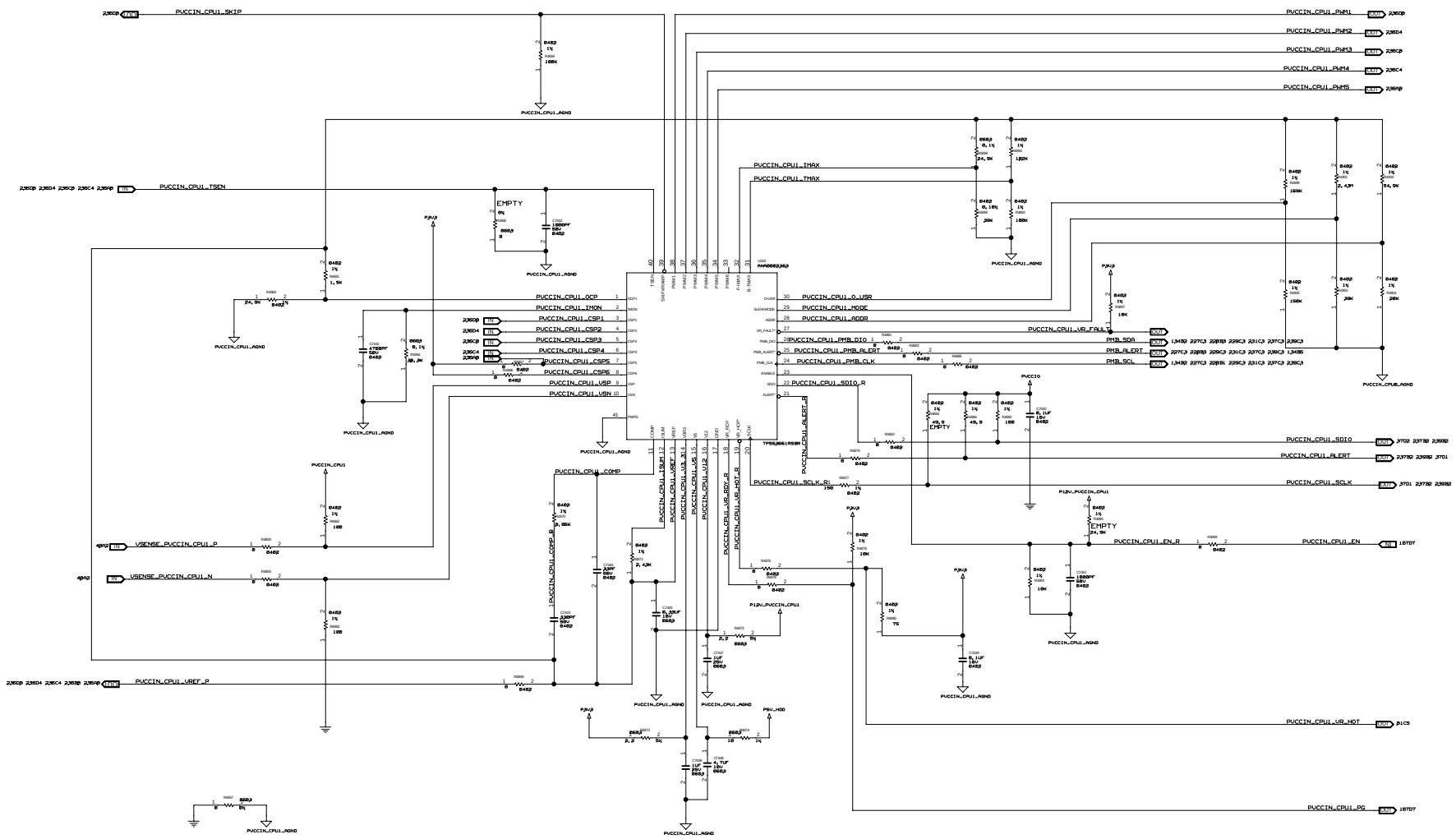
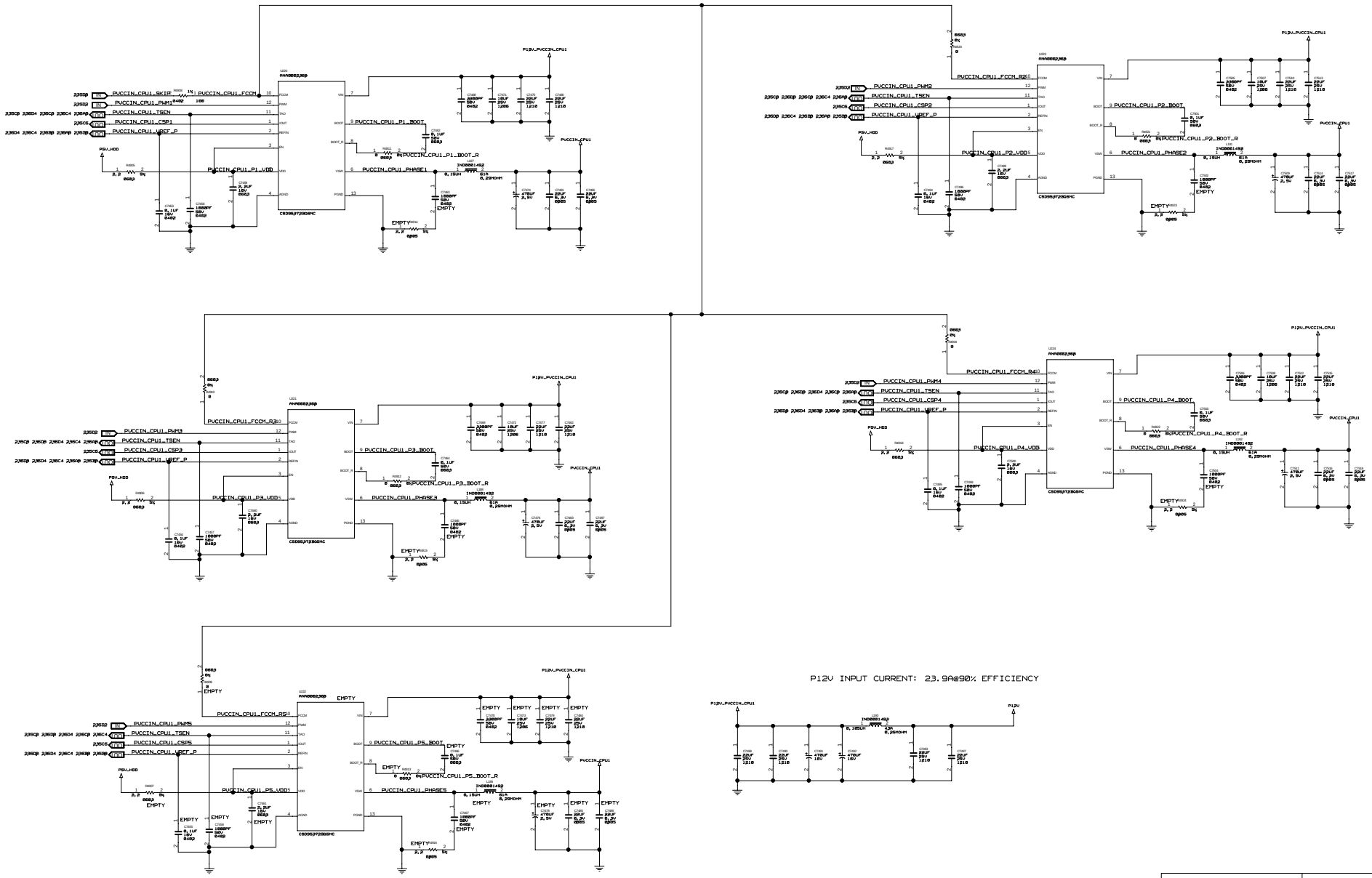
	DRAWNBY: <ENGINEER> · SHEET: 234OF360


PVCCIN_CPU1_SKIP
PVCCIN_CPU1_AGND
PVCCIN_CPU1_TSEN
PVCCIN_CPU1_OCP
PVCCIN_CPU1_IMON
PVCCIN_CPU1_CSP1
PVCCIN_CPU1_CSP2
PVCCIN_CPU1_CSP3
PVCCIN_CPU1_CSP4
PVCCIN_CPU1_CSP5
PVCCIN_CPU1_CSP6
PVCCIN_CPU1_VSP
PVCCIN_CPU1_VSN
PVCCIN_CPU1_COMP
PVCCIN_CPU1_ISUM
PVCCIN_CPU1_VSET
PVCCIN_CPU1_IOUT
PVCCIN_CPU1_VR_RDY_R
PVCCIN_CPU1_VR_HOT_R
PVCCIN_CPU1_VR_HOT
PVCCIN_CPU1_PG
PVCCIN_CPU1_EN_R
PVCCIN_CPU1_EN
PVCCIN_CPU1_SCLK_R
PVCCIN_CPU1_SCLK
PVCCIN_CPU1_ALERT
PVCCIN_CPU1_SDIO
PVCCIN_CPU1_SDIO_R
PVCCIN_CPU1_PMB_CLK
PVCCIN_CPU1_PMB_ALERT
PVCCIN_CPU1_PMB_DIO
PVCCIN_CPU1_ADDR
PVCCIN_CPU1_MODE
PVCCIN_CPU1_O_USR
PVCCIN_CPU1_VR_FAULT
PVCCIN_CPU1_IMAX
PVCCIN_CPU1_TMAX
PMB_SDA
PMB_ALERT
PMB_SCL
PVCCIN_CPU1_PWM1
PVCCIN_CPU1_PWM2
PVCCIN_CPU1_PWM3
PVCCIN_CPU1_PWM4
PVCCIN_CPU1_PWM5
VSENSE_PVCCIN_CPU1_P
VSENSE_PVCCIN_CPU1_N
PVCCIN_CPU1_VREF_P
PVCCIN_CPU1_COMP_R
PVCCIN_CPU1_VR_RDY_R
PVCCIN_CPU1_VR_HOT_R
PVCCIN_CPU1_VR_HOT
PVCCIN_CPU1_PG
PVCCIN_CPU1_EN
PVCCIN_CPU1_SCLK
PVCCIN_CPU1_ALERT
PVCCIN_CPU1_SDIO
PVCCIN_CPU1_CPU8_AGND
PVCCIN_CPU1_VR_FAULT
PVCCIN_CPU1_PMB_ALERT_R
PVCCIN_CPU1_ISUM_R
PVCCIN_CPU1_VSET_R
PVCCIN_CPU1_IOUT_R
PVCCIN_CPU1_VR_RDY_R
PVCCIN_CPU1_VR_HOT_R
PVCCIN_CPU1_EN_R
PVCCIN_CPU1_SCLK_R
PVCCIN_CPU1_SDIO_R
PVCCIO
PJ1V_PVCCIN_CPU1
PSU_HOD
EMPTY
TPS53681RSBR
DESIGN SPEC:
VR12.5 GRANTLEY EP 120W
OUTPUT VOLTAGE: 1.82V
ICC TDC/PEAK: 73A/156A
MAX STEP LOAD: 109A
VBOOT:1.7V
SVID ADDRESS: 0000
PMBUS ADDRESS: 1110000
SWITCHING FREQUENCY: 600K
PER-PHASE VALLEY CURRENT: 51A
JABIL
wolfcreek_controller
wolfcreek_controller.cpm
Fri Aug 08 14:44:29 2014
A-0
<ENGINEER>
235OF350
PVCCIN_CPU1_1



P12V INPUT CURRENT: 23.9A@90% EFFICIENCY

PVCCIN_CPU1_2

JABIL

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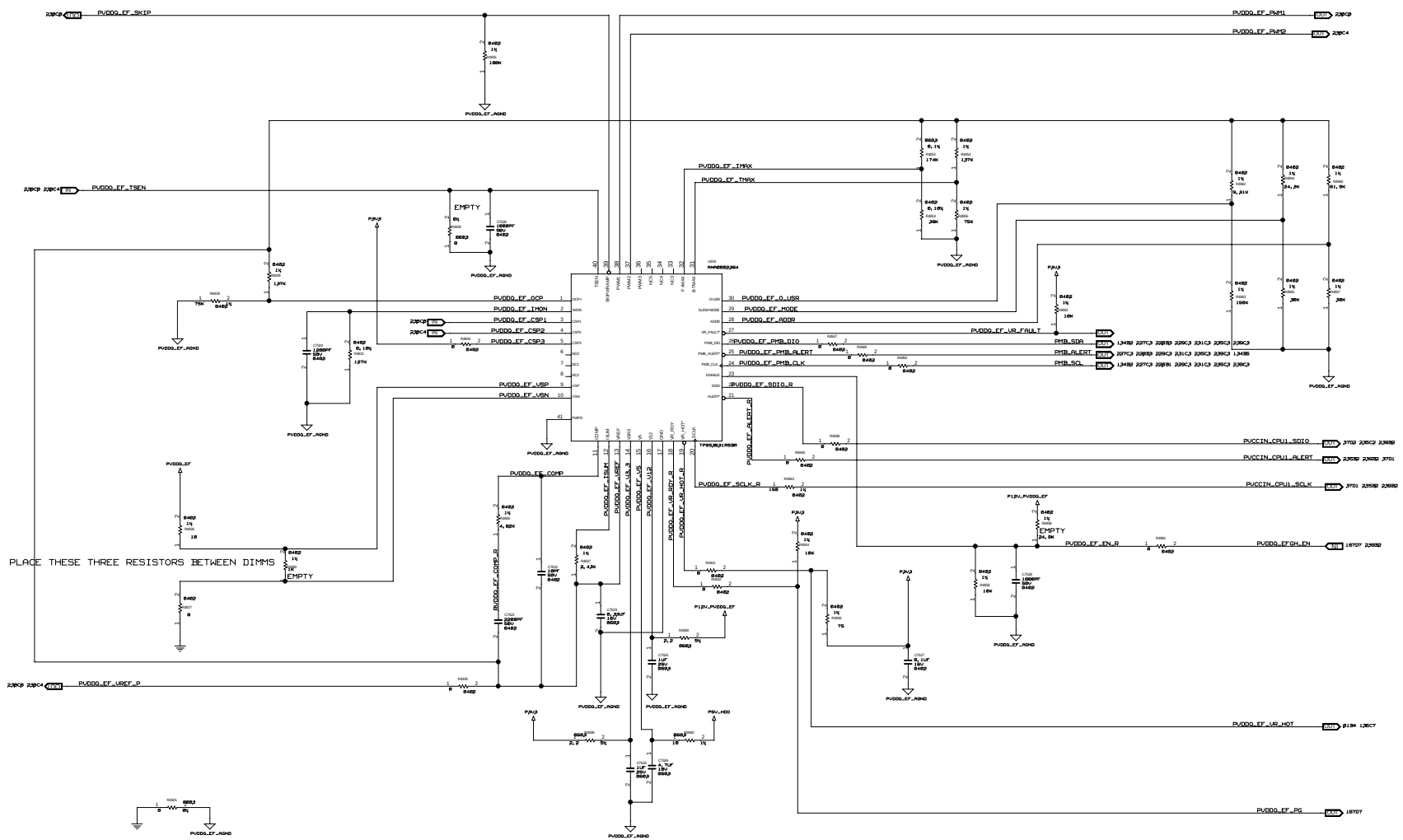
wolfcreek_controller	
wolfcreek_controller.cpm	
DATE: Wed Jul 30 14:57:46 2014	DWG NO: <DWG> REV: A-0
DRAWN BY: <ENGINEER>	SHEET: 236OF360



DESIGN SPEC:

VR12.5 GRANTLEY EP 4DIMM
OUTPUT VOLTAGE: 1.2V
ICC TDC/PEAK: 34.8A/53.7A
MAX STEP LOAD: 26.8A
VBOOT: 1.2V
SVID ADDRESS: 0010
PMBUS ADDRESS: 1110010
SWITCHING FREQUENCY: 600K
PER-PHASE VALLEY CURRENT: 39A

PVDDQ_EF_1

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
DATE: Fri Aug 08 14:54:54 2014	DWG NO: <DWG> REV: A-0
DRAWNBY: <ENGINEER>	SHEET: 2,370F360

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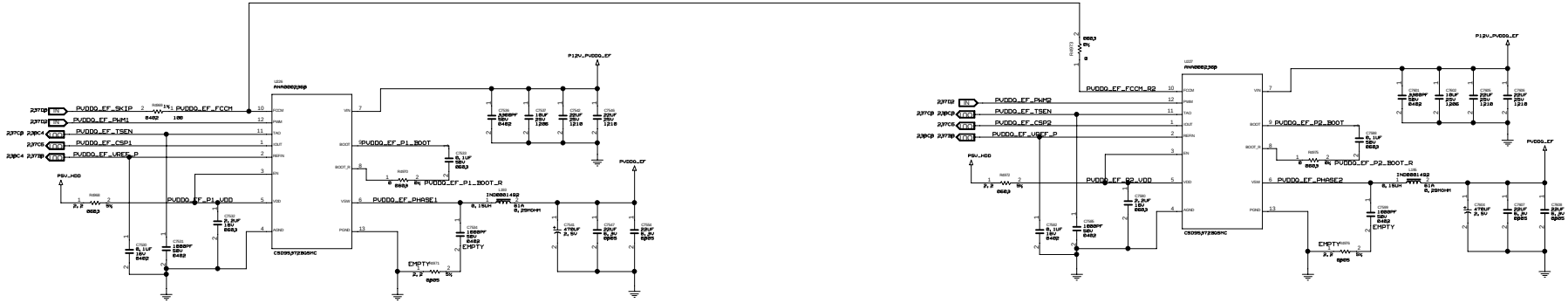
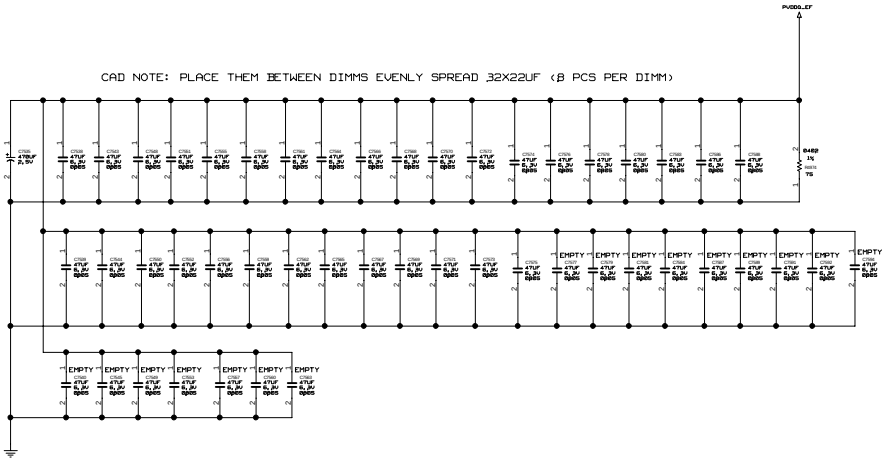
P12V INPUT CURRENT: 5.97A@90% EFFICIENCY



CAD NOTE: PLACE THEM BETWEEN DIMMS EVENLY SPREAD 32X22UF (8 PCS PER DIMM)



PVDDQ_EF_2

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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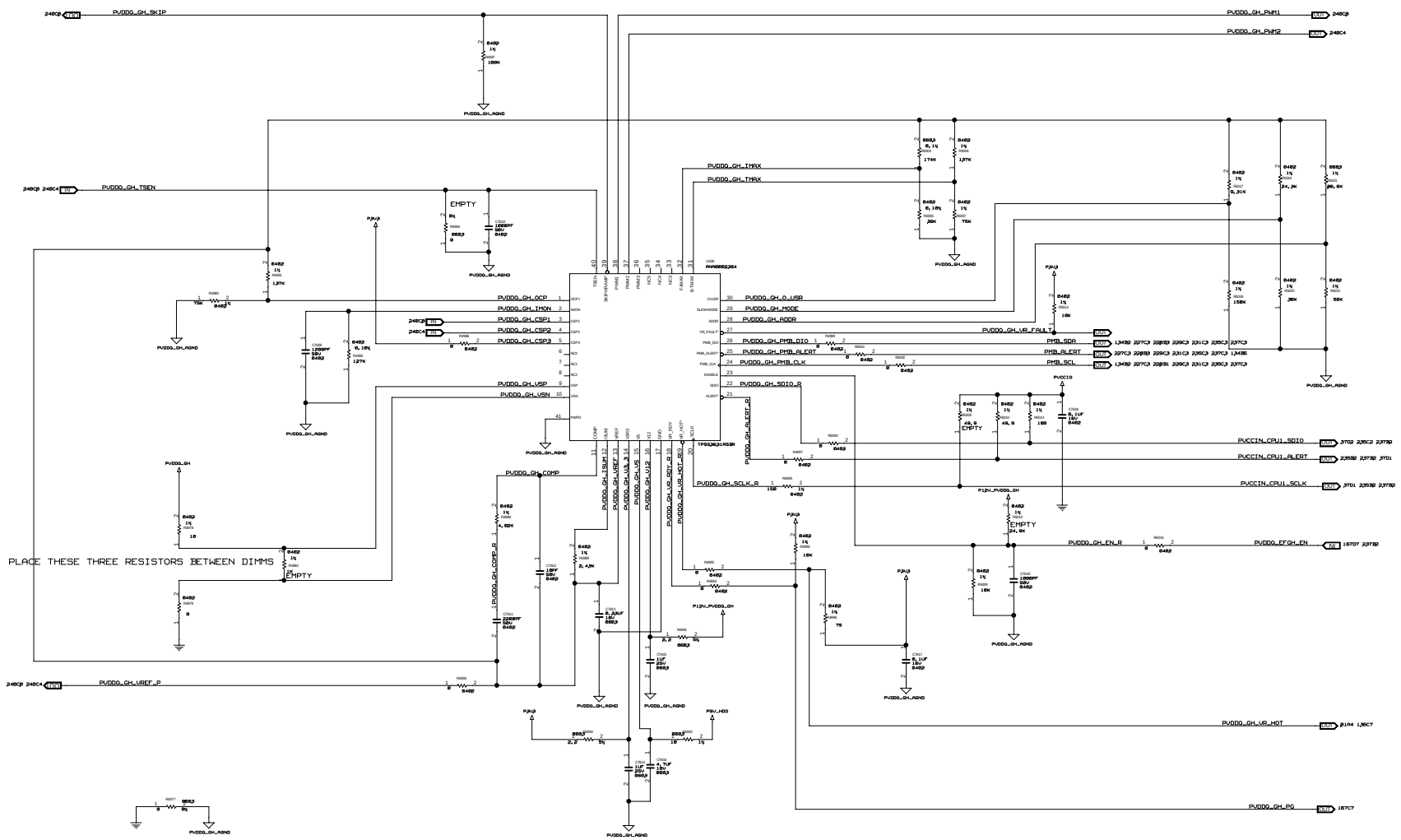
	DRAWN BY: <ENGINEER> · SHEET: 23 OF 350



DESIGN SPEC:

VR12.5 GRANTLEY EP 4DIMM
OUTPUT VOLTAGE: 1.2V
ICC TDC/PEAK: 34.8A/53.7A
MAX STEP LOAD: 26.8BA
VBOOT: 1.2V
SVID ADDRESS: 0100
PMBUS ADDRESS: 1110100
SWITCHING FREQUENCY: 600K
PER-PHASE VALLEY CURRENT: 39A

PVDDQ_GH_1

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
DATE: Fri Aug 08 14:55:07 2014	DWG NO: <DWG> REV: A-0
DRAWN BY: <ENGINEER>	SHEET: 239OF360

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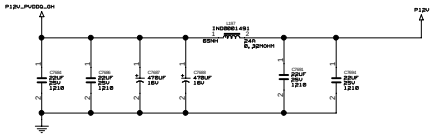
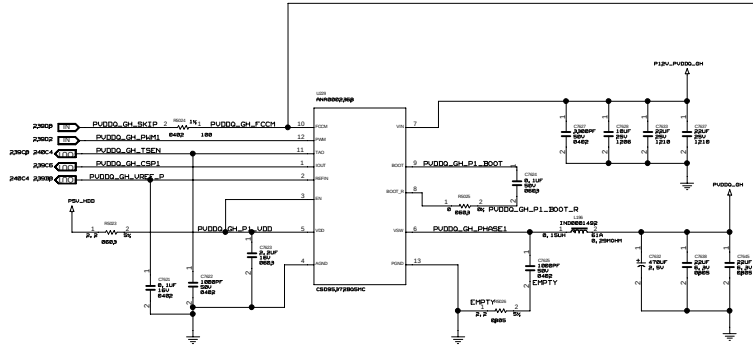
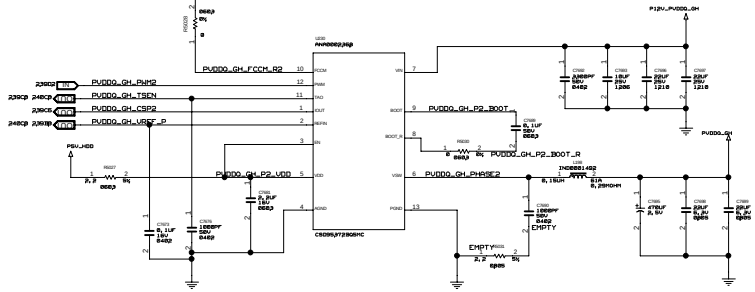
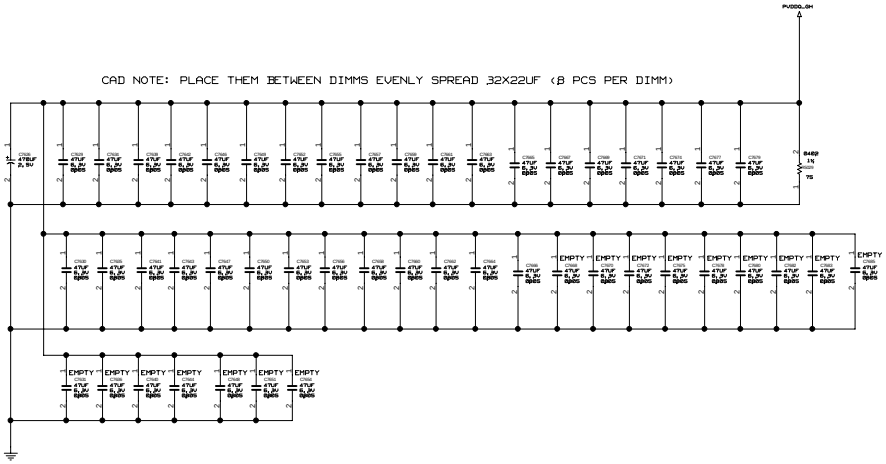
P12V INPUT CURRENT: 5.97A@90% EFFICIENCY

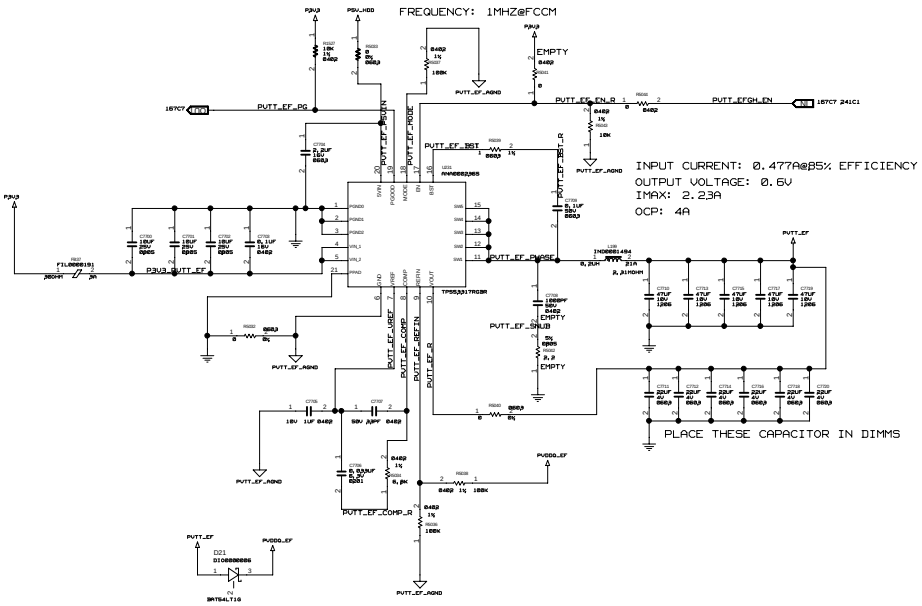


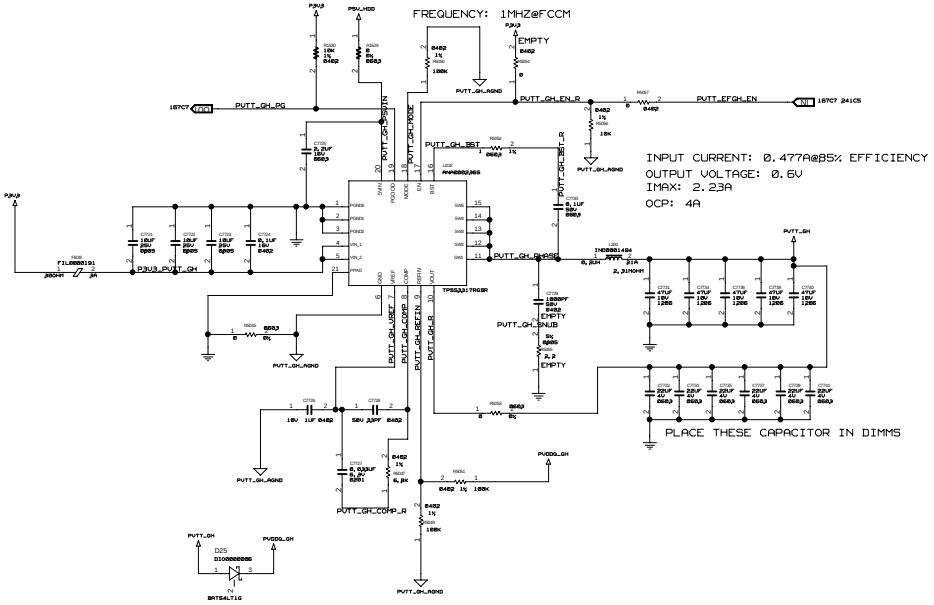




CAD NOTE: PLACE THEM BETWEEN DIMMS EVENLY SPREAD 32X22UF (8 PCS PER DIMM)


PVDDQ_GH
C7908 470UF 2.5V
C7909 47UF 6.3V 0805
C7906 47UF 6.3V 0805
C7908 47UF 6.3V 0805
C7940 47UF 6.3V 0805
C7948 47UF 6.3V 0805
C7949 47UF 6.3V 0805
C7952 47UF 6.3V 0805
C7951 47UF 6.3V 0805
C7947 47UF 6.3V 0805
C7950 47UF 6.3V 0805
C7941 47UF 6.3V 0805
C7943 47UF 6.3V 0805
C7960 47UF 6.3V 0805
C7942 47UF 6.3V 0805
C7944 47UF 6.3V 0805
C7957 47UF 6.3V 0805
C7946 47UF 6.3V 0805
C7956 47UF 6.3V 0805
C7955 47UF 6.3V 0805
C7953 47UF 6.3V 0805
C7954 47UF 6.3V 0805
C7952 47UF 6.3V 0805
C7951 47UF 6.3V 0805
C7947 47UF 6.3V 0805
C7950 47UF 6.3V 0805
C7941 47UF 6.3V 0805
C7943 47UF 6.3V 0805
C7960 47UF 6.3V 0805
C7942 47UF 6.3V 0805
C7944 47UF 6.3V 0805
C7957 47UF 6.3V 0805
C7946 47UF 6.3V 0805
C7956 47UF 6.3V 0805
C7955 47UF 6.3V 0805
C7953 47UF 6.3V 0805
C7954 47UF 6.3V 0805
EMPTY
C7962 47UF 6.3V 0805
C7958 47UF 6.3V 0805
C7959 47UF 6.3V 0805
C7963 47UF 6.3V 0805
C7961 47UF 6.3V 0805
C7964 47UF 6.3V 0805
C7965 47UF 6.3V 0805
C7966 47UF 6.3V 0805
C7967 47UF 6.3V 0805
C7968 47UF 6.3V 0805
C7969 47UF 6.3V 0805
C7970 47UF 6.3V 0805
C7971 47UF 6.3V 0805
C7972 47UF 6.3V 0805
C7973 47UF 6.3V 0805





PVTT_EFGH

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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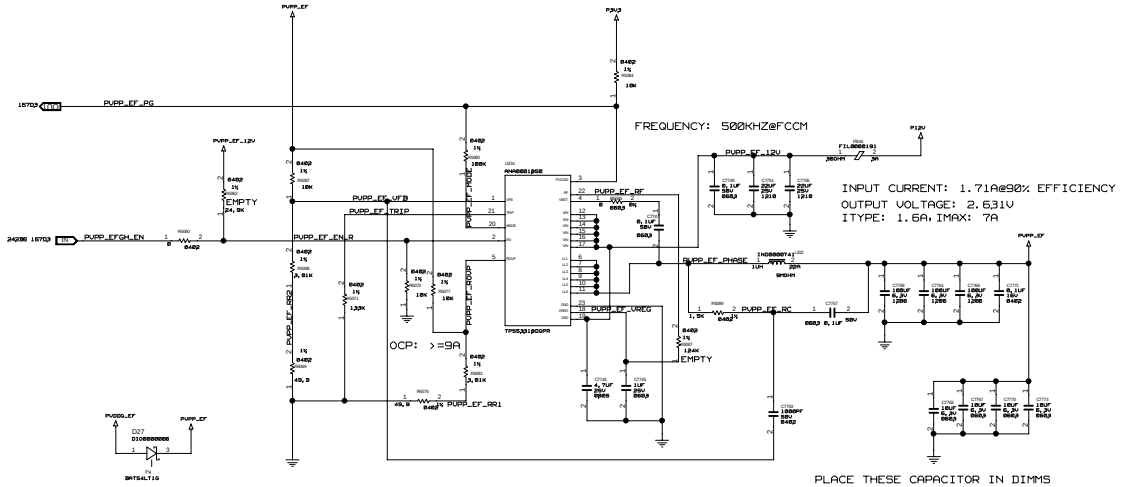
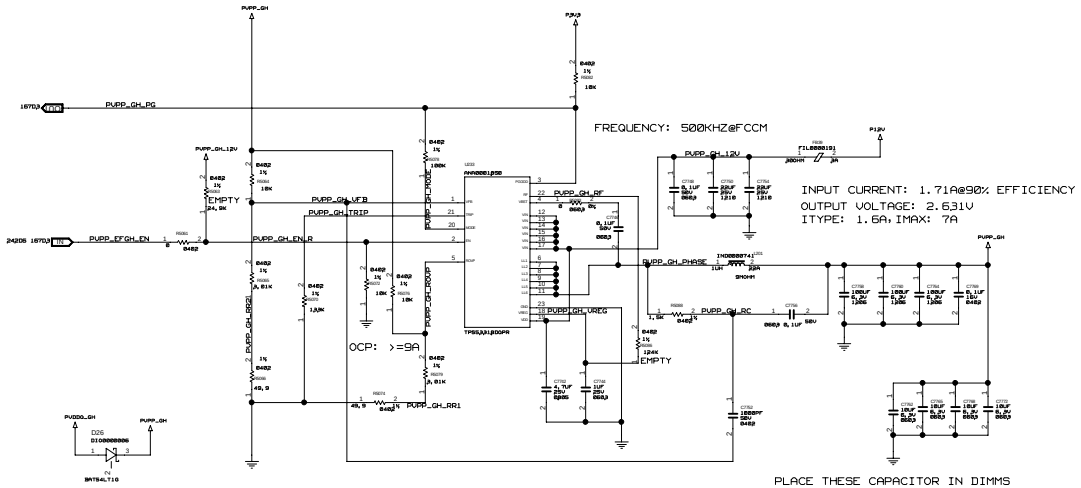
	DRAWNBY: <ENGINEER> · SHEET: 24 OF 350





PVPP_EFGH

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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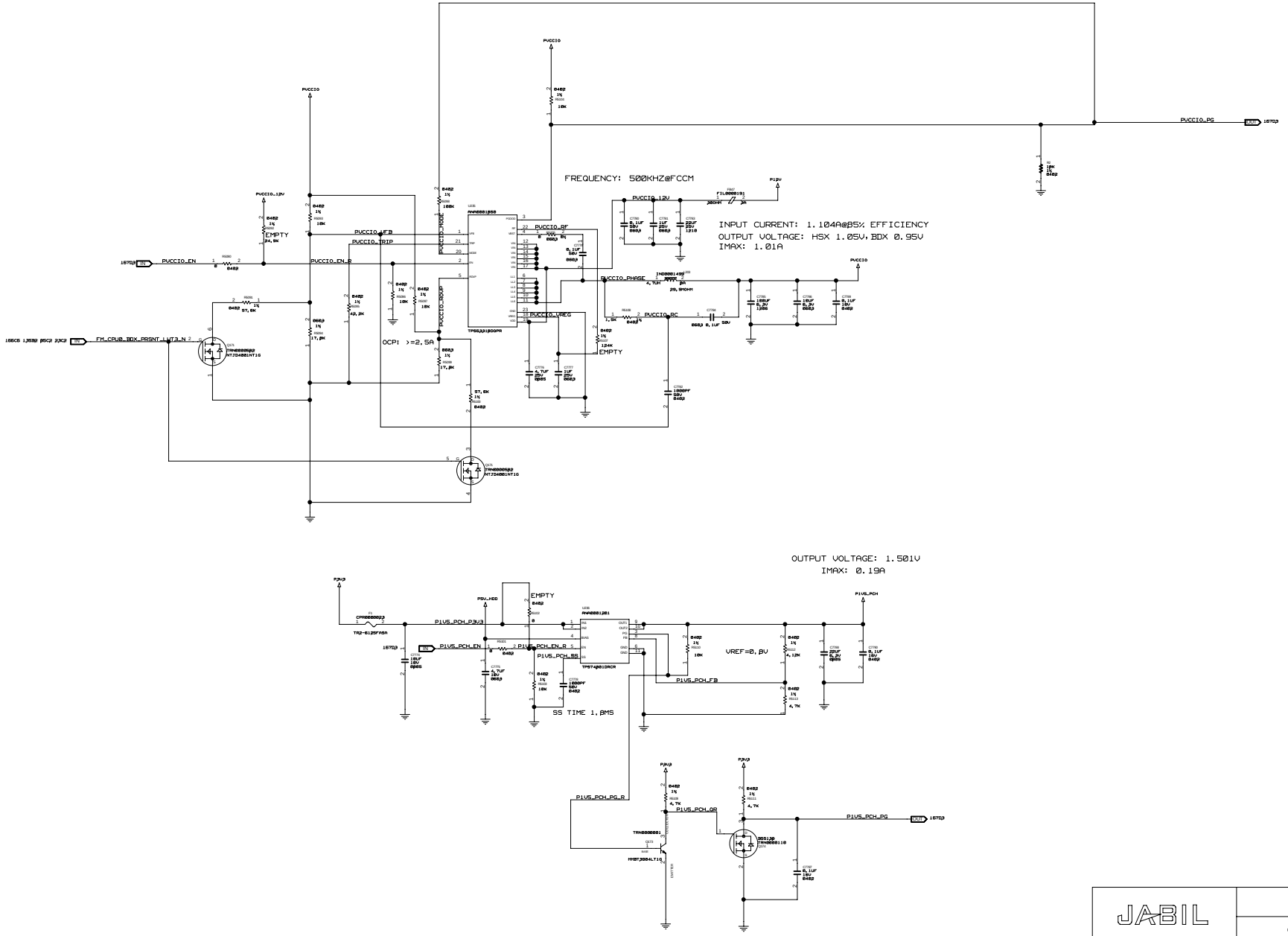
	DRAWN BY: <ENGINEER> · SHEET: 24 OF 350



JABIL

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 14:55:45 2014

DWG NO: <DWG>

REV: A-0

DRAWN BY: <ENGINEER>

SHEET: 24 OF 350

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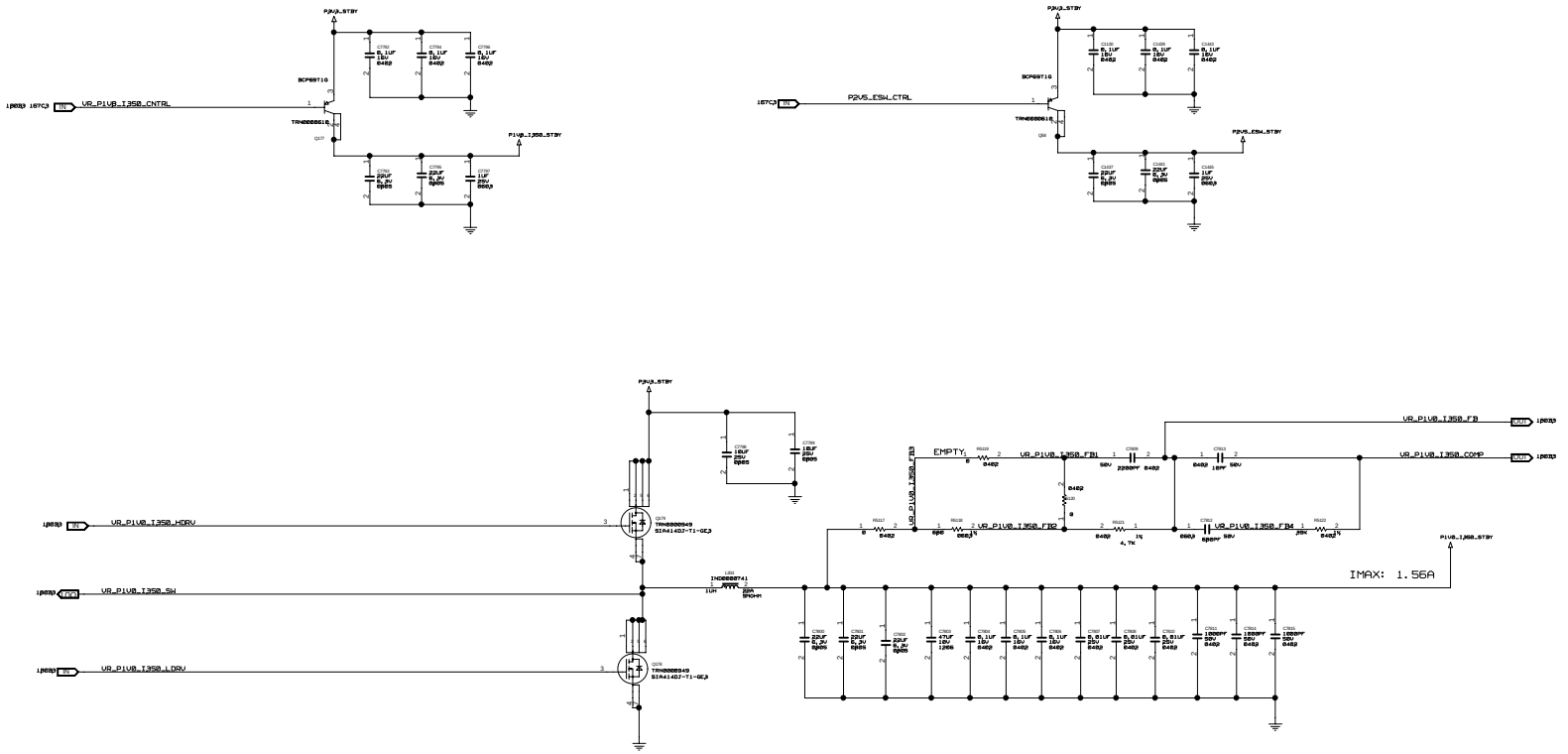

P1V8_I350_STBY & P1V0_I350_STBY & P2V5_ESW_STBY

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
DATE: Wed Jul 30 14:59:35 2014	DWG NO: <DWG> REV: A-0
DRAWN BY: <ENGINEER>	SHEET: 244OF350

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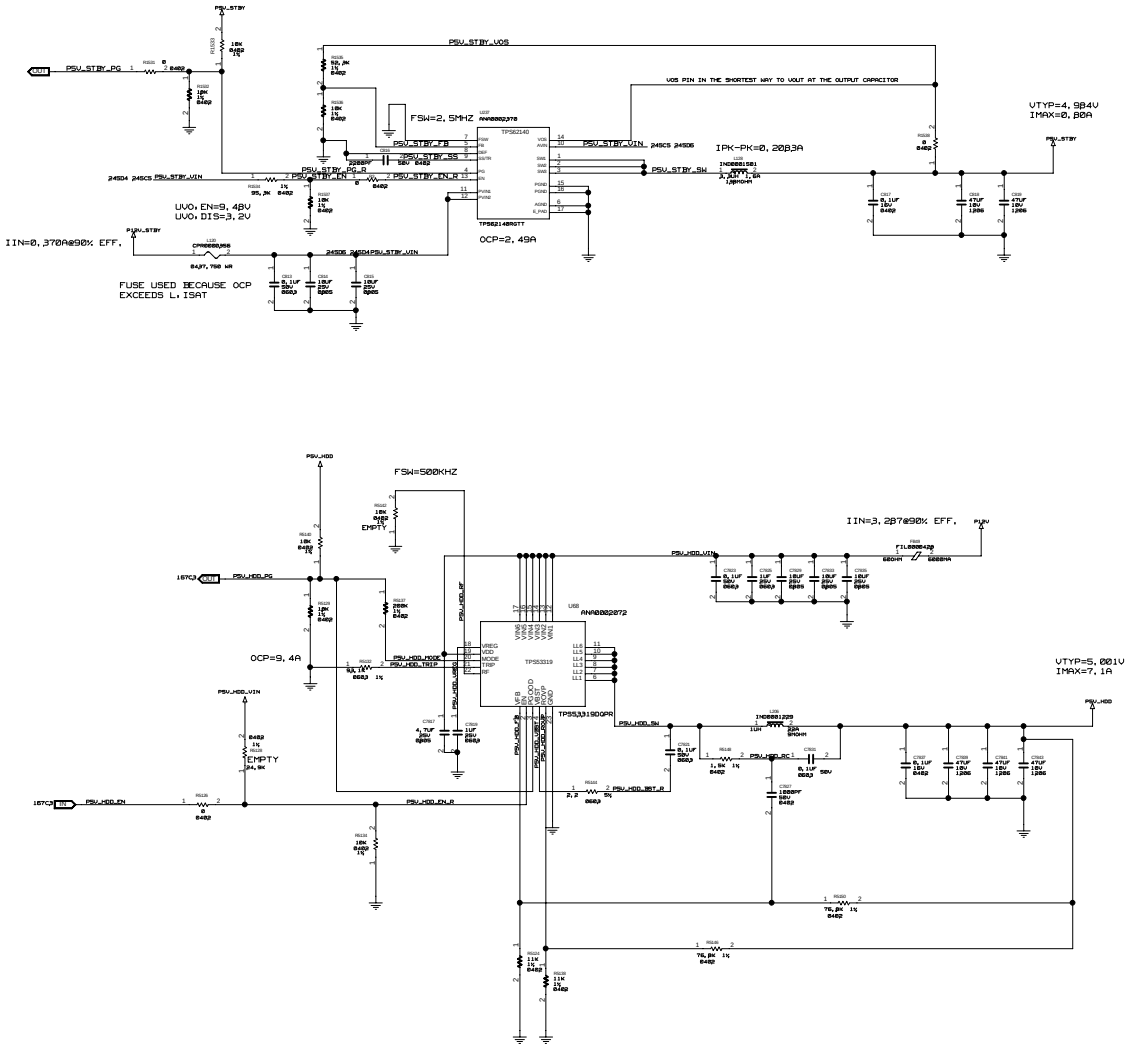

P5V_STBY & P5V_HDD

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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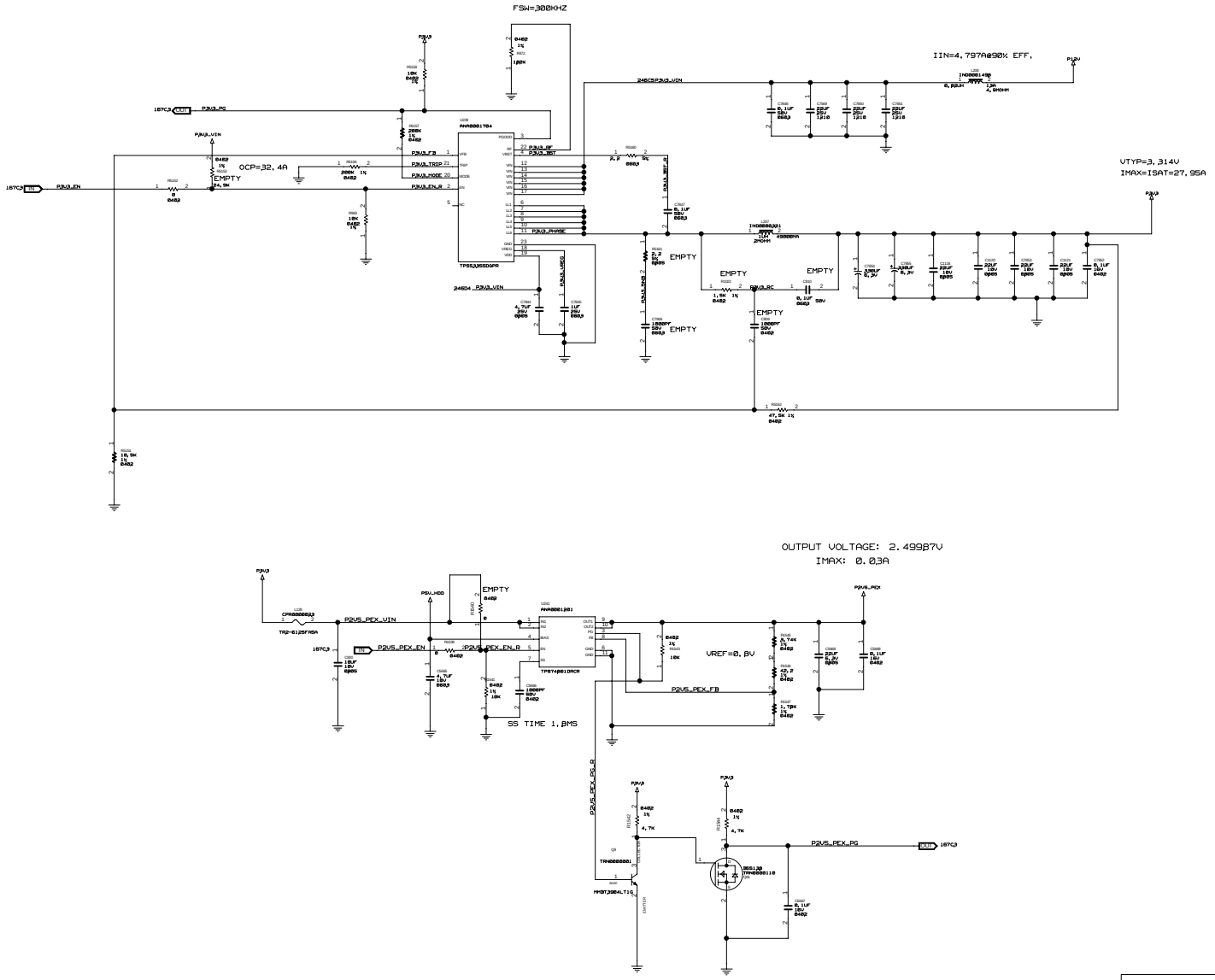
	DRAWN BY: <ENGINEER> · SHEET: 24 OF 350



P3V3 & P2V5_PEX

JABIL

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 14:56:10 2014

DWG NO: <DWG>

REV: A-0

DRAWN BY: <ENGINEER>

SHEET: 24 OF 350

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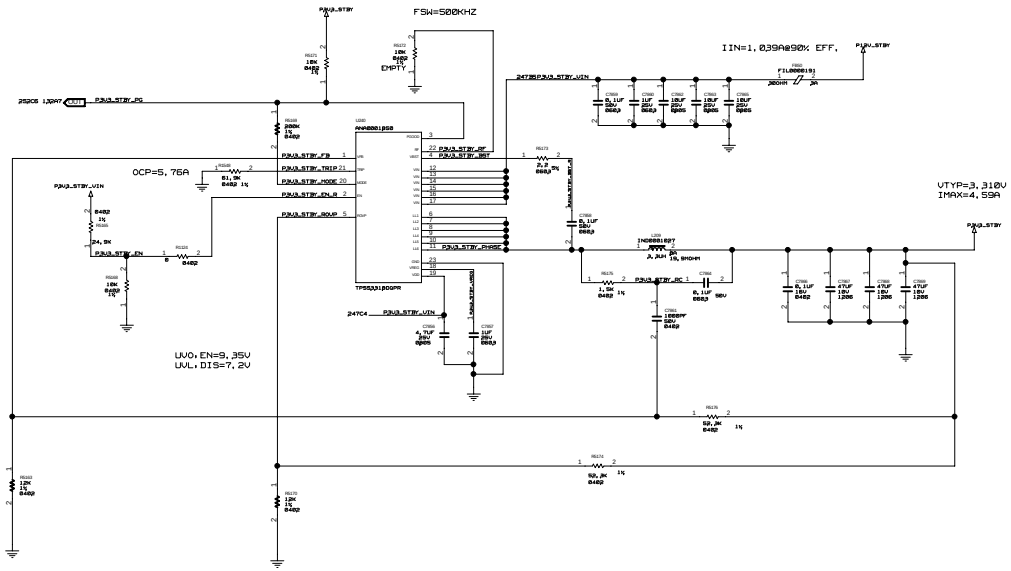

P3V3_STBY

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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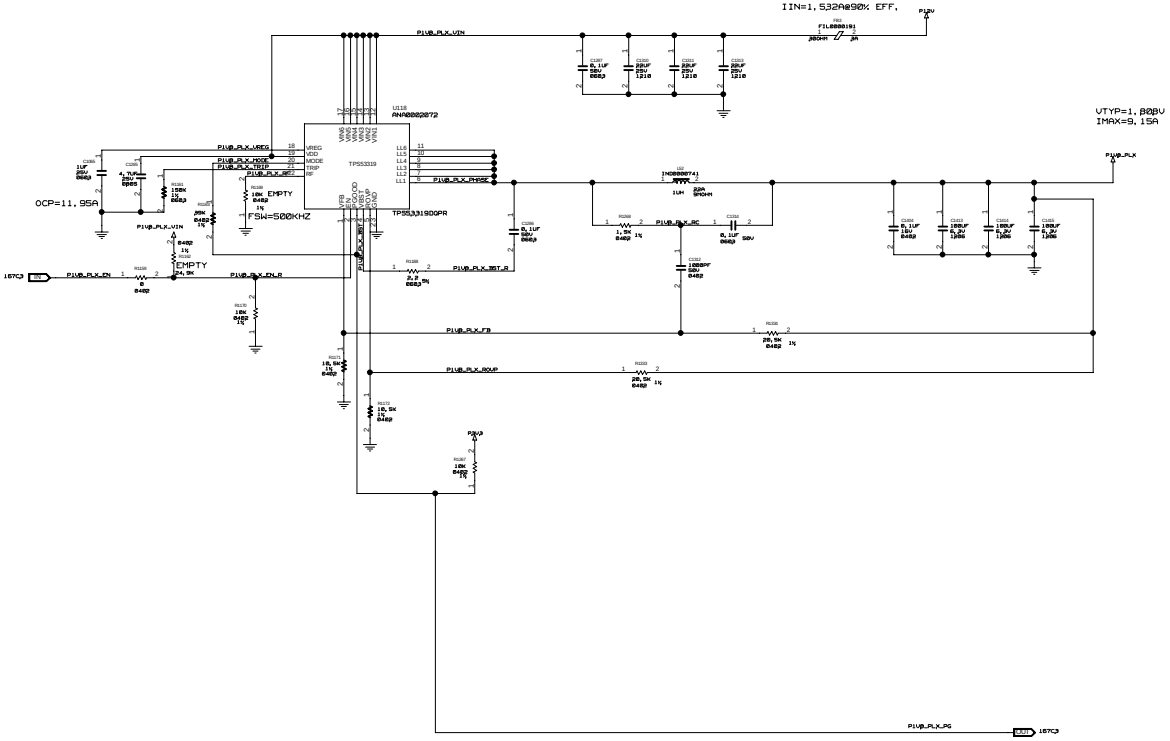
	DRAWN BY: <ENGINEER> · SHEET: 247OF360



P1V8_PLX

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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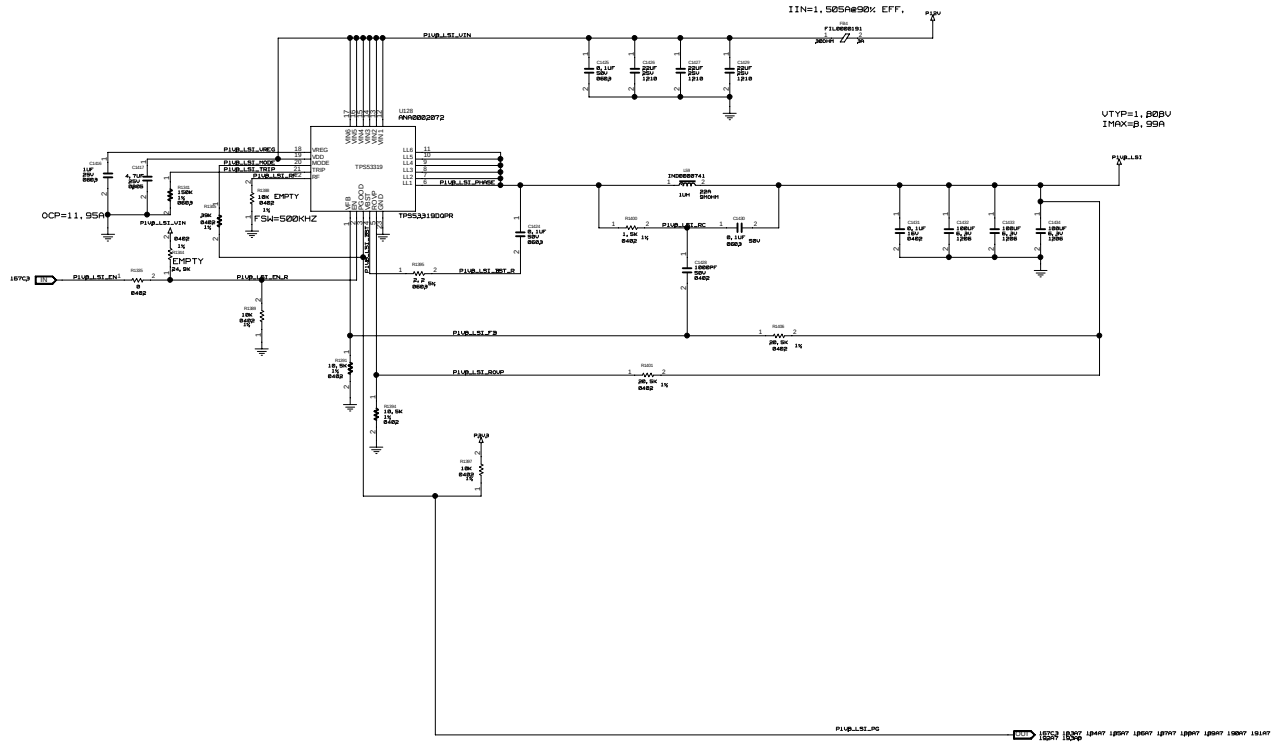
	DRAWN BY: <ENGINEER> · SHEET: 24 OF 350



P1V8_LSI

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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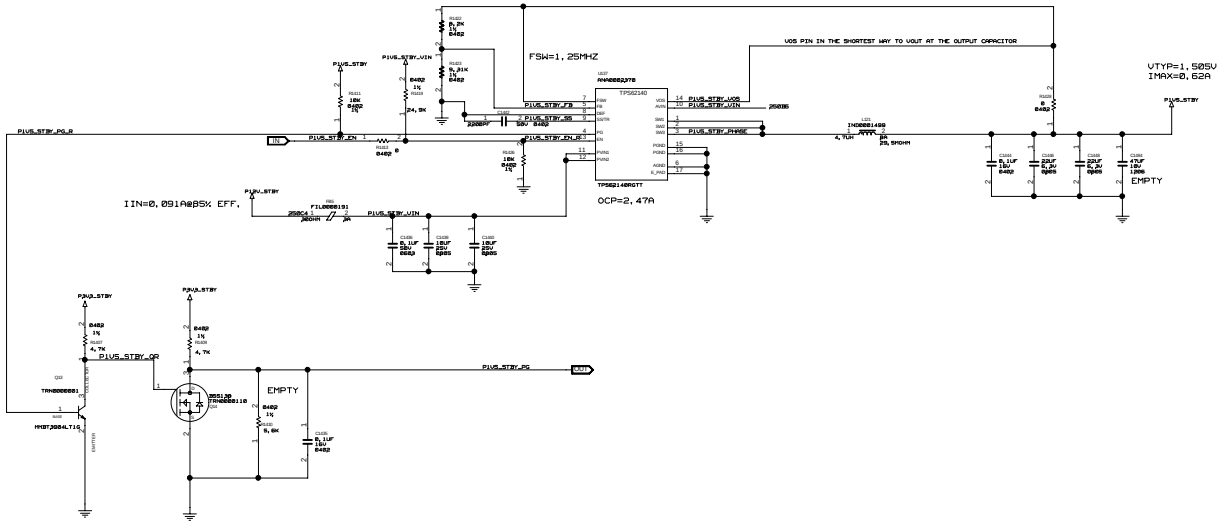
	DRAWN BY: <ENGINEER> · SHEET: 24908360



P1V5_STBY

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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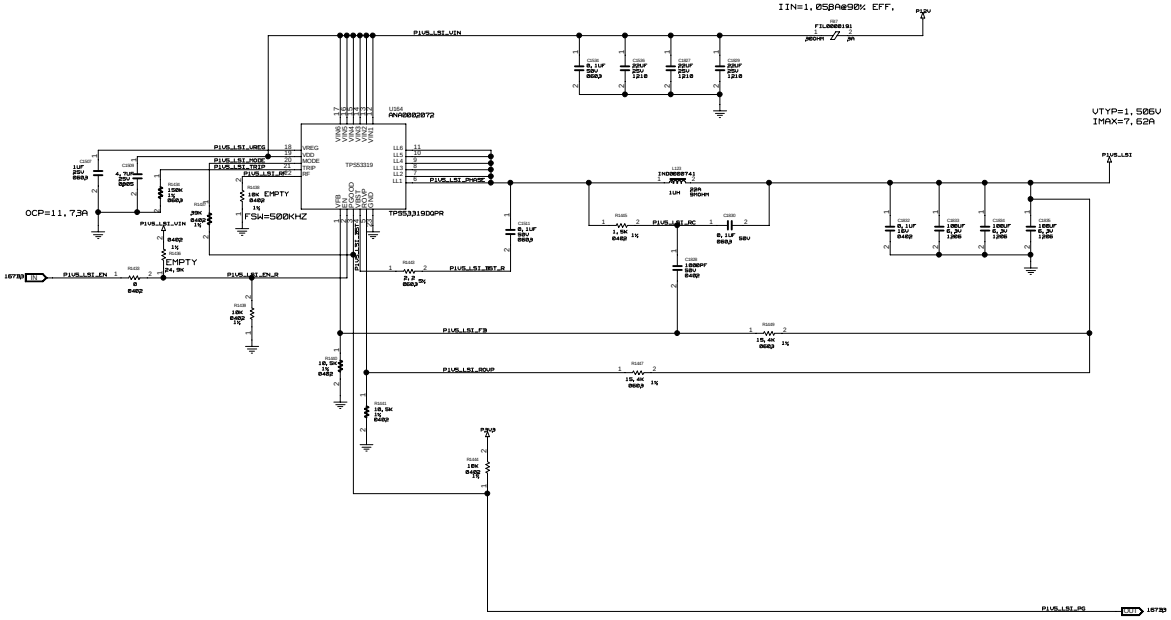
	DRAWN BY: <ENGINEER> · SHEET: 25 OF 360



P1V5_LSI

JABIL

wolfcreek_controller

wolfcreek_controller.cpm

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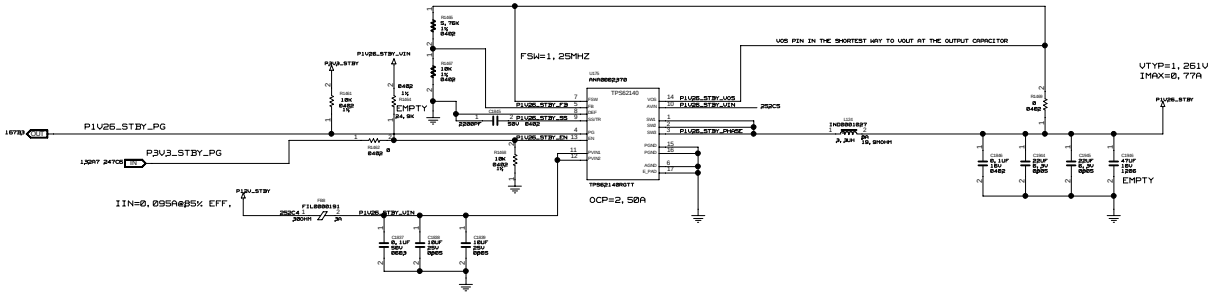
DATE: Fri Aug 08 14:51:54 2014

DWG NO: <DWG>

REV: A-0

DRAWN BY: <ENGINEER>

SHEET: 251OF350



P1V26_STBY

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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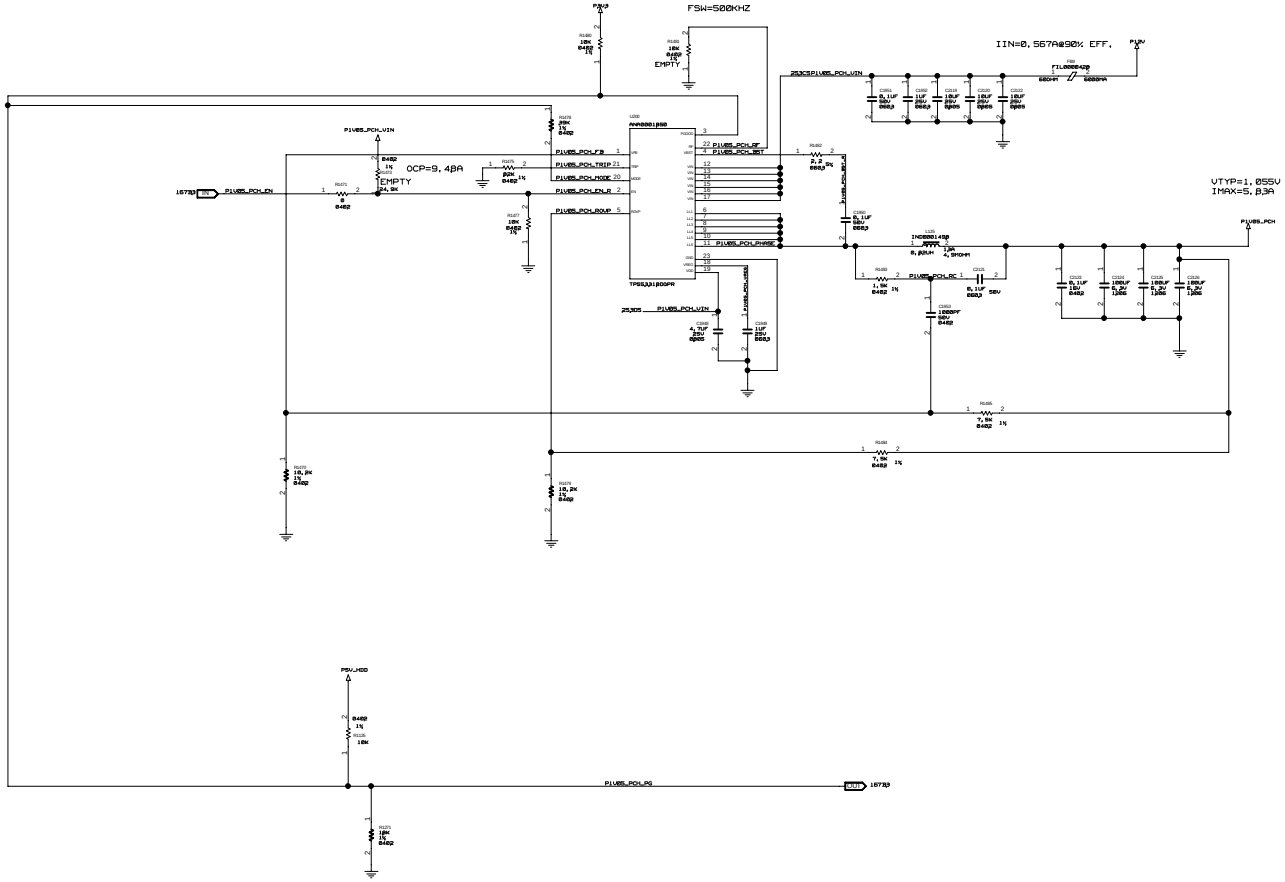
	DRAWN BY: <ENGINEER> · SHEET: 25 OF 36



P1V05_PCH

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
DATE: Fri Aug 08 14:56:48 2014	DWG NO: <DWG> REV: A-0
DRAWN BY: <ENGINEER>	SHEET: 253OF360

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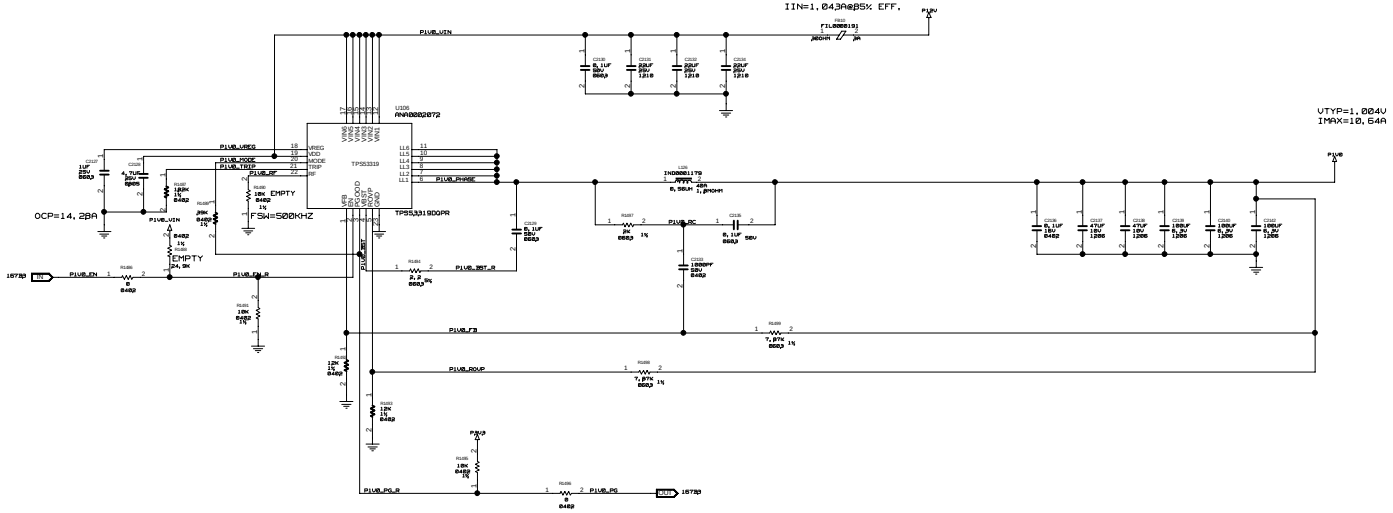

P1V0

JABIL

wolfcreek_controller

wolfcreek_controller.cpm

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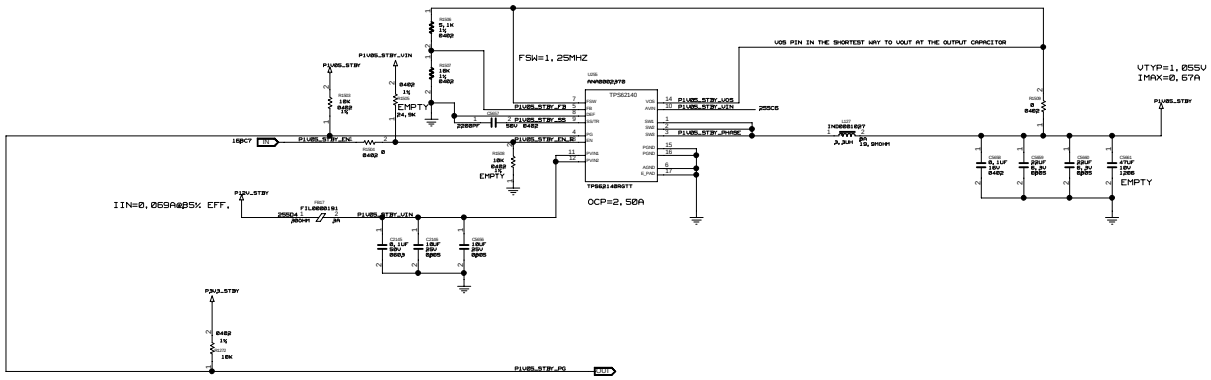
DATE: Wed Jul 30 14:59:50 2014

DWG NO: <DWG>

REV: A-0

DRAWN BY: <ENGINEER>

SHEET: 254OF360



P1V05_STBY

JABIL	wolfcreek_controller
	wolfcreek_controller.cpm
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	DRAWN BY: <ENGINEER> · SHEET: 255OF360

CONTROL 1

MONITOR 8

VREFF=1.024V & VDIV = VIN * 0.0625
EACH BIT = 0.004VIN +/-1%
VIN.MAX=16.384V

P12V_MON
P12V_SB_MON
P12V_RAW_MON
VBATT_RAW_MON
VMEM_MON

VREFF=1.024V & VDIV = VIN * 0.2500
EACH BIT = 0.001VIN +/-1%
VIN.MAX=4.096V

VCOIN_MON
VCOIN_R_MON
P3V3_STBY_MON
P3V3_MON

SYSTEM 7

MATED_L
COLD_RESTART
FORCE_STBY_ON
AC_FAIL_N
BBU_ENABLE
BBU_OFFLINE_TEST
P12V_GD
BBU_ON_BATT

PMBUS 2

HS_PMBUS_ALERT_N
HS_PMBUS_SDA
HS_PMBUS_SCL

SWD 3

EMPTY HS_SWD_DTA
EMPTY HS_SWD_CLK
EMPTY HS_SWD_XRES

PSU 8

PS1_PWOK
PS1_ACOK
PS2_PWOK
PS2_ACOK
PS3_PWOK
PS3_ACOK
PS4_PWOK
PS4_ACOK

OPEN DRAIN PULLED TO PSU INTERNAL 3.3V

BPM 5

BBU_EN_STATUS
BPM_RESERVE1
BPM_RESERVE2
BPM_RESERVE3
BPM_RESERVED4

HOT-SWAP 20

P12V_SB_RAW_PG
P12V_SB_RAW_FAULT_N
P12V_SB_RAW_IMON
P12V_SB_RAW_DIODEON NOT USED
P12V_SB_RAW_EN OPEN DRAIN

P12V_RAW_PG
P12V_RAW_FAULT_N
P12V_RAW_IMON
P12V_RAW_DIODEON NOT USED
P12V_RAW_EN OPEN DRAIN

VBATT_RAW_PG
VBATT_RAW_FAULT_N
VBATT_RAW_IMON
VBATT_RAW_DIODEON NOT USED
VBATT_RAW_EN MUST DRIVE HIGH!

VMEM_RAW_PG
VMEM_RAW_FAULT_N
VMEM_RAW_IMON
VMEM_RAW_DIODEON NOT USED
VMEM_RAW_EN OPEN DRAIN

STBY DIODE 3

P12V_DIODE_PG
P12V_DIODE_FAULT_N
P12V_DIODE_ON

MUST PUT BOOST CIRCUT CLOSE TO PSOC

PSOC/HOT-SWAP POWER CONTROLER

JABIL

wolfcreek_controller

wolfcreek_controller.cpm

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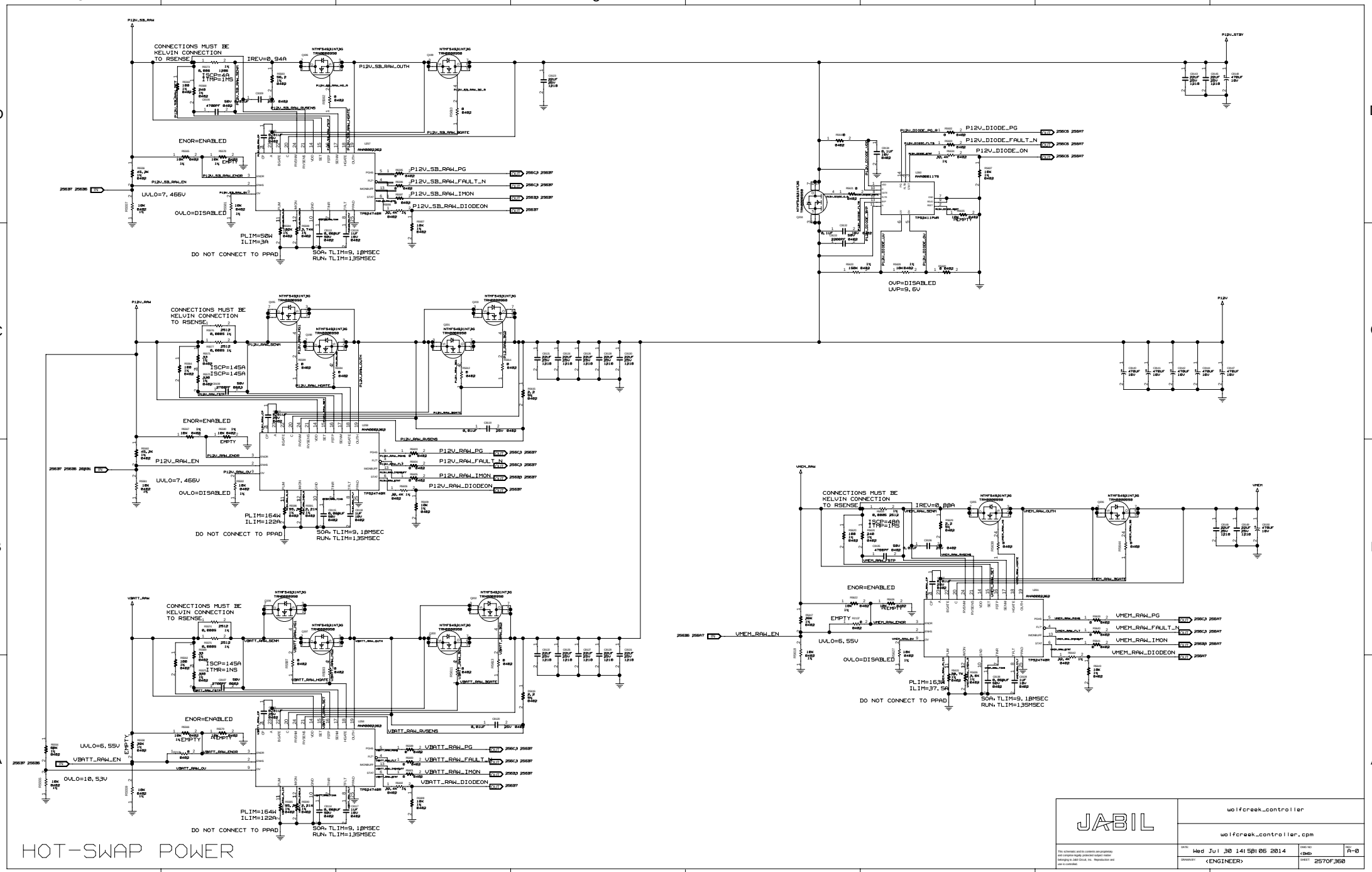
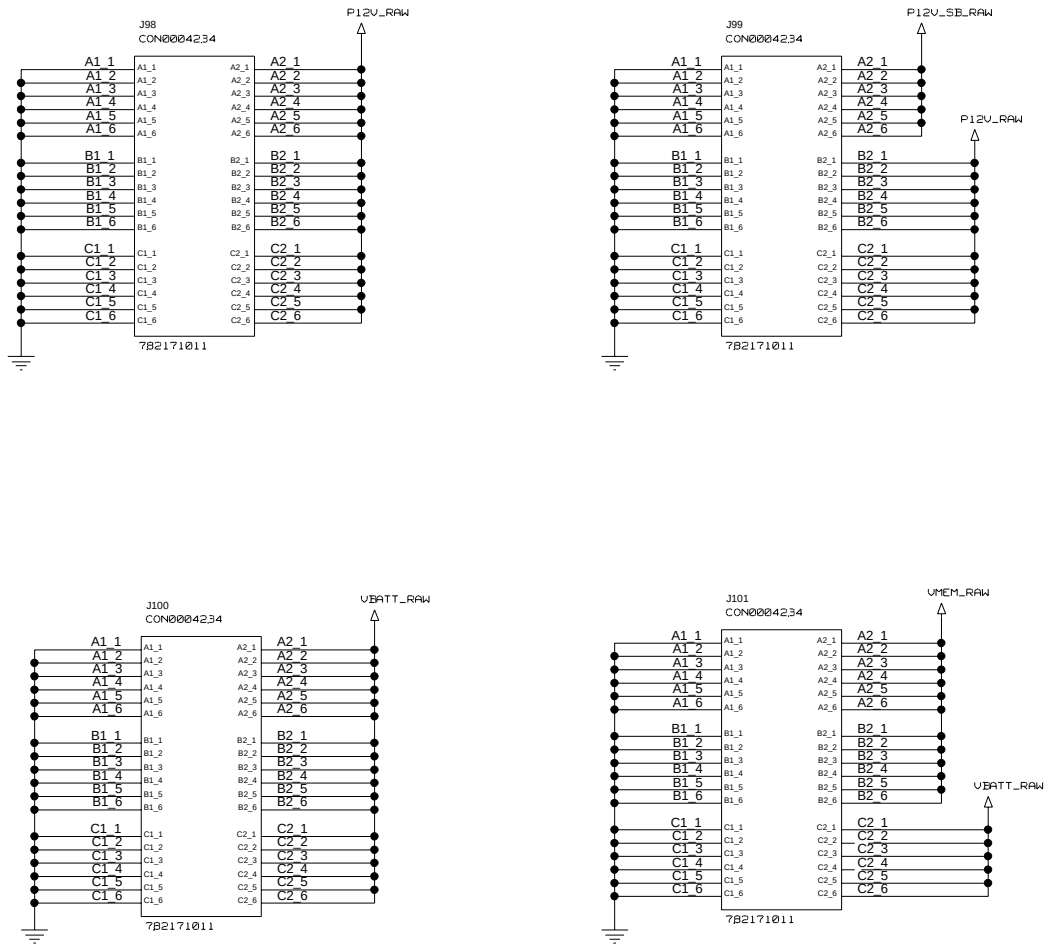
DATE: Fri Aug 08 20:52:11 2014
DWG NO: <DWG>
REV: A-0
DRAWN BY: <ENGINEER>
SHEET: 256OF360


CONNECTIONS MUST BE KELVIN CONNECTION TO RSENSE
ENOR=ENABLED
UVLO=7.46V
OVLO=DISABLED
PLIM=50W
ILIM=3A
DO NOT CONNECT TO PPAD
SOA: TLIM=9.18MSEC
RUN: TLIM=135MSEC
P12V_SB_RAW_PG
P12V_SB_RAW_FAULT_N
P12V_SB_RAW_IMON
P12V_SB_RAW_DIODEON
P12V_DIODE_PG
P12V_DIODE_FAULT_N
P12V_DIODE_ON
OVP=DISABLED
UVP=9.6V
P12V_RAW_EN
P12V_RAW_PG
P12V_RAW_FAULT_N
P12V_RAW_IMON
P12V_RAW_DIODEON
PLIM=164W
ILIM=122A
VBATT_RAW_EN
VBATT_RAW_PG
VBATT_RAW_FAULT_N
VBATT_RAW_IMON
VBATT_RAW_DIODEON
OVLO=10.53V
UVLO=6.55V
VMEM_RAW_EN
VMEM_RAW_PG
VMEM_RAW_FAULT_N
VMEM_RAW_IMON
VMEM_RAW_DIODEON
PLIM=163W
ILIM=37.5A
HOT-SWAP POWER
JABIL
wolfcreek_controller
wolfcreek_controller.cpm
Wed Jul 30 14:58:06 2014
A-0
<ENGINEER>
2570F360



HOT-SWAP POWER CONNECTOR

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POWER CONNECTORS
wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 19:26:14 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 258OF360

HSV1	1AS_MPS_U1017_DP<0>	IN	195A4 200D8	HSV25	1AS_MPS_U101B_DP<0>
	2AS_MPS_U1017_DN<0>	IN	195A4 200D8		2AS_MPS_U101B_DN<0>
HSV2	1AS_MPS_U1017_DP<1>	IN	195A4 200D8	HSV26	1AS_MPS_U101B_DP<1>
	2AS_MPS_U1017_DN<1>	IN	195A4 200D8		2AS_MPS_U101B_DN<1>
HSV3	1AS_MPS_U1017_DP<2>	IN	195A4 200D8	HSV27	1AS_MPS_U101B_DP<2>
	2AS_MPS_U1017_DN<2>	IN	195A4 200D8		2AS_MPS_U101B_DN<2>
HSV4	1AS_MPS_U1017_DP<3>	IN	195B4 200D8	HSV28	1AS_MPS_U101B_DP<3>
	2AS_MPS_U1017_DN<3>	IN	195B4 200D8		2AS_MPS_U101B_DN<3>
HSV5	1AS_MPS_U1017_DP<4>	IN	195B4 200D8	HSV29	1AS_MPS_U101B_DP<4>
	2AS_MPS_U1017_DN<4>	IN	195B4 200D8		2AS_MPS_U101B_DN<4>
HSV6	1AS_MPS_U1017_DP<5>	IN	195B4 200D8	HSV30	1AS_MPS_U101B_DP<5>
	2AS_MPS_U1017_DN<5>	IN	195B4 200D8		2AS_MPS_U101B_DN<5>
HSV7	1AS_MPS_U1017_DP<6>	IN	195C4 200D8	HSV31	1AS_MPS_U101B_DP<6>
	2AS_MPS_U1017_DN<6>	IN	195C4 200D8		2AS_MPS_U101B_DN<6>
HSV8	1AS_MPS_U1017_DP<7>	IN	195C4 200D8	HSV32	1AS_MPS_U101B_DP<7>
	2AS_MPS_U1017_DN<7>	IN	195C4 200D8		2AS_MPS_U101B_DN<7>
HSV9	1AS_MPS_U1017_DP<8>	IN	195C4 200D8	HSV33	1AS_MPS_U101B_DP<8>
	2AS_MPS_U1017_DN<8>	IN	195C4 200D8		2AS_MPS_U101B_DN<8>
HSV10	1AS_MPS_U1017_DP<9>	IN	195C4 200D8	HSV34	1AS_MPS_U101B_DP<9>
	2AS_MPS_U1017_DN<9>	IN	195C4 200D8		2AS_MPS_U101B_DN<9>
HSV11	1AS_MPS_U1017_DP<10>	IN	195C4 200D8	HSV35	1AS_MPS_U101B_DP<10>
	2AS_MPS_U1017_DN<10>	IN	195C4 200D8		2AS_MPS_U101B_DN<10>
HSV12	1AS_MPS_U1017_DP<11>	IN	195D4 200D8	HSV36	1AS_MPS_U101B_DP<11>
	2AS_MPS_U1017_DN<11>	IN	195D4 200D8		2AS_MPS_U101B_DN<11>
HSV13	1AS_MPS_U1017_DP<12>	IN	195A5 200D8	HSV37	1AS_MPS_U101B_DP<12>
	2AS_MPS_U1017_DN<12>	IN	195A5 200D8		2AS_MPS_U101B_DN<12>
HSV14	1AS_MPS_U1017_DP<13>	IN	195A5 200D8	HSV38	1AS_MPS_U101B_DP<13>
	2AS_MPS_U1017_DN<13>	IN	195A5 200D8		2AS_MPS_U101B_DN<13>
HSV15	1AS_MPS_U1017_DP<14>	IN	195A5 200D8	HSV39	1AS_MPS_U101B_DP<14>
	2AS_MPS_U1017_DN<14>	IN	195A5 200D8		2AS_MPS_U101B_DN<14>
HSV16	1AS_MPS_U1017_DP<15>	IN	195B5 200D8	HSV40	1AS_MPS_U101B_DP<15>
	2AS_MPS_U1017_DN<15>	IN	195B5 200D8		2AS_MPS_U101B_DN<15>
HSV17	1AS_MPS_U1017_DP<16>	IN	195B5 200D8	HSV41	1AS_MPS_U101B_DP<16>
	2AS_MPS_U1017_DN<16>	IN	195B5 200D8		2AS_MPS_U101B_DN<16>
HSV18	1AS_MPS_U1017_DP<17>	IN	195B5 200D8	HSV42	1AS_MPS_U101B_DP<17>
	2AS_MPS_U1017_DN<17>	IN	195B5 200D8		2AS_MPS_U101B_DN<17>
HSV19	1AS_MPS_U1017_DP<18>	IN	195C5 200D8	HSV43	1AS_MPS_U101B_DP<18>
	2AS_MPS_U1017_DN<18>	IN	195C5 200D8		2AS_MPS_U101B_DN<18>
HSV20	1AS_MPS_U1017_DP<19>	IN	195C5 200D8	HSV44	1AS_MPS_U101B_DP<19>
	2AS_MPS_U1017_DN<19>	IN	195C5 200D8		2AS_MPS_U101B_DN<19>
HSV21	1AS_MPS_U1017_DP<20>	IN	195C5 200D8	HSV45	1AS_MPS_U101B_DP<20>
	2AS_MPS_U1017_DN<20>	IN	195C5 200D8		2AS_MPS_U101B_DN<20>
HSV22	1AS_MPS_U1017_DP<21>	IN	195C5 200D8	HSV46	1AS_MPS_U101B_DP<21>
	2AS_MPS_U1017_DN<21>	IN	195C5 200D8		2AS_MPS_U101B_DN<21>
HSV23	1AS_MPS_U1017_DP<22>	IN	195C5 200D8	HSV47	1AS_MPS_U101B_DP<22>
	2AS_MPS_U1017_DN<22>	IN	195C5 200D8		2AS_MPS_U101B_DN<22>
HSV24	1AS_MPS_U1017_DP<23>	IN	195D5 200D8	HSV48	1AS_MPS_U101B_DP<23>
	2AS_MPS_U1017_DN<23>	IN	195D5 200D8		2AS_MPS_U101B_DN<23>

HSV49	1AS_U1017_MPS_DP<0>	IN	195A4 200D1	HSV73	1AS_U101B_MPS_DP<0>
	2AS_U1017_MPS_DN<0>	IN	195A4 200D1		2AS_U101B_MPS_DN<0>
HSV50	1AS_U1017_MPS_DP<1>	IN	195A4 200D1	HSV74	1AS_U101B_MPS_DP<1>
	2AS_U1017_MPS_DN<1>	IN	195A4 200D1		2AS_U101B_MPS_DN<1>
HSV51	1AS_U1017_MPS_DP<2>	IN	195B4 200D1	HSV75	1AS_U101B_MPS_DP<2>
	2AS_U1017_MPS_DN<2>	IN	195B4 200D1		2AS_U101B_MPS_DN<2>
HSV52	1AS_U1017_MPS_DP<3>	IN	195B4 200D1	HSV76	1AS_U101B_MPS_DP<3>
	2AS_U1017_MPS_DN<3>	IN	195B4 200D1		2AS_U101B_MPS_DN<3>
HSV53	1AS_U1017_MPS_DP<4>	IN	195B4 200D1	HSV77	1AS_U101B_MPS_DP<4>
	2AS_U1017_MPS_DN<4>	IN	195B4 200D1		2AS_U101B_MPS_DN<4>
HSV54	1AS_U1017_MPS_DP<5>	IN	195B4 200D1	HSV78	1AS_U101B_MPS_DP<5>
	2AS_U1017_MPS_DN<5>	IN	195B4 200D1		2AS_U101B_MPS_DN<5>
HSV55	1AS_U1017_MPS_DP<6>	IN	195C4 200D1	HSV79	1AS_U101B_MPS_DP<6>
	2AS_U1017_MPS_DN<6>	IN	195C4 200D1		2AS_U101B_MPS_DN<6>
HSV56	1AS_U1017_MPS_DP<7>	IN	195C4 200D1	HSV80	1AS_U101B_MPS_DP<7>
	2AS_U1017_MPS_DN<7>	IN	195C4 200D1		2AS_U101B_MPS_DN<7>
HSV57	1AS_U1017_MPS_DP<8>	IN	195C4 200D1	HSV81	1AS_U101B_MPS_DP<8>
	2AS_U1017_MPS_DN<8>	IN	195C4 200D1		2AS_U101B_MPS_DN<8>
HSV58	1AS_U1017_MPS_DP<9>	IN	195D4 200D1	HSV82	1AS_U101B_MPS_DP<9>
	2AS_U1017_MPS_DN<9>	IN	195D4 200D1		2AS_U101B_MPS_DN<9>
HSV59	1AS_U1017_MPS_DP<10>	IN	195D4 200D1	HSV83	1AS_U101B_MPS_DP<10>
	2AS_U1017_MPS_DN<10>	IN	195D4 200D1		2AS_U101B_MPS_DN<10>
HSV60	1AS_U1017_MPS_DP<11>	IN	195D4 200D1	HSV84	1AS_U101B_MPS_DP<11>
	2AS_U1017_MPS_DN<11>	IN	195D4 200D1		2AS_U101B_MPS_DN<11>
HSV61	1AS_U1017_MPS_DP<12>	IN	195A5 200D1	HSV85	1AS_U101B_MPS_DP<12>
	2AS_U1017_MPS_DN<12>	IN	195A5 200D1		2AS_U101B_MPS_DN<12>
HSV62	1AS_U1017_MPS_DP<13>	IN	195A5 200D1	HSV86	1AS_U101B_MPS_DP<13>
	2AS_U1017_MPS_DN<13>	IN	195A5 200D1		2AS_U101B_MPS_DN<13>
HSV63	1AS_U1017_MPS_DP<14>	IN	195B5 200D1	HSV87	1AS_U101B_MPS_DP<14>
	2AS_U1017_MPS_DN<14>	IN	195B5 200D1		2AS_U101B_MPS_DN<14>
HSV64	1AS_U1017_MPS_DP<15>	IN	195B5 200D1	HSV88	1AS_U101B_MPS_DP<15>
	2AS_U1017_MPS_DN<15>	IN	195B5 200D1		2AS_U101B_MPS_DN<15>
HSV65	1AS_U1017_MPS_DP<16>	IN	195B5 200D1	HSV89	1AS_U101B_MPS_DP<16>
	2AS_U1017_MPS_DN<16>	IN	195B5 200D1		2AS_U101B_MPS_DN<16>
HSV66	1AS_U1017_MPS_DP<17>	IN	195B5 200D1	HSV90	1AS_U101B_MPS_DP<17>
	2AS_U1017_MPS_DN<17>	IN	195B5 200D1		2AS_U101B_MPS_DN<17>
HSV67	1AS_U1017_MPS_DP<18>	IN	195C5 200D1	HSV91	1AS_U101B_MPS_DP<18>
	2AS_U1017_MPS_DN<18>	IN	195C5 200D1		2AS_U101B_MPS_DN<18>
HSV68	1AS_U1017_MPS_DP<19>	IN	195C5 200D1	HSV92	1AS_U101B_MPS_DP<19>
	2AS_U1017_MPS_DN<19>	IN	195C5 200D1		2AS_U101B_MPS_DN<19>
HSV69	1AS_U1017_MPS_DP<20>	IN	195C5 200D1	HSV93	1AS_U101B_MPS_DP<20>
	2AS_U1017_MPS_DN<20>	IN	195C5 200D1		2AS_U101B_MPS_DN<20>
HSV70	1AS_U1017_MPS_DP<21>	IN	195D5 200D1	HSV94	1AS_U101B_MPS_DP<21>
	2AS_U1017_MPS_DN<21>	IN	195D5 200D1		2AS_U101B_MPS_DN<21>
HSV71	1AS_U1017_MPS_DP<22>	IN	195D5 200D1	HSV95	1AS_U101B_MPS_DP<22>
	2AS_U1017_MPS_DN<22>	IN	195D5 200D1		2AS_U101B_MPS_DN<22>
HSV72	1AS_U1017_MPS_DP<23>	IN	195D5 200D1	HSV96	1AS_U101B_MPS_DP<23>
	2AS_U1017_MPS_DN<23>	IN	195D5 200D1		2AS_U101B_MPS_DN<23>

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HASWELL SOCKET 0 (13 OF 14)

wolfcreek_controller

wolfcreek_controller.cpm

DATE: Fri Aug 08 19:26:15 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING>

REV: <REVISION>

SHEET: 259OF360

CR-260 : @WOLFCREEK_CONTROLLER_LIB.WOLFCREEK_CONTROLLER(SCH_1):PAGE664

HSV97	PE_U1003_HDD0_DP(0)	19BD7 213C2	PE_U1003_HDD0_DN(0)	19BD7 213C2
HSV98	PE_U1003_HDD0_DP(1)	19BC7 213C2	PE_U1003_HDD0_DN(1)	19BC7 213C2
HSV104	PE_U1003_HDD1_DP(0)	19BD7 213C2	PE_U1003_HDD1_DN(0)	19BD7 213C2
HSV105	PE_U1003_HDD1_DP(1)	19BC7 213C2	PE_U1003_HDD1_DN(1)	19BC7 213C2
HSV106	PE_U1003_HDD2_DP(0)	19BB7 213C2	PE_U1003_HDD2_DN(0)	19BB7 213C2
HSV101	PE_U1003_HDD2_DP(1)	19BA7 213C2	PE_U1003_HDD2_DN(1)	19BA7 213C2
HSV107	PE_U1003_HDD3_DP(0)	19BB7 213C2	PE_U1003_HDD3_DN(0)	19BB7 213C2
HSV108	PE_U1003_HDD3_DP(1)	19BA7 213C2	PE_U1003_HDD3_DN(1)	19BA7 213C2
HSV109	PE_U1003_HDD4_DP(0)	19BB7 213C2	PE_U1003_HDD4_DN(0)	19BB7 213C2
HSV110	PE_U1003_HDD4_DP(1)	19BA7 213C2	PE_U1003_HDD4_DN(1)	19BA7 213C2
HSV99	PE_U1003_HDD5_DP(0)	19BD7 213C2	PE_U1003_HDD5_DN(0)	19BD7 213C2
HSV102	PE_U1003_HDD5_DP(1)	19BC7 213C2	PE_U1003_HDD5_DN(1)	19BC7 213C2
HSV111	PE_U1003_HDD6_DP(0)	19BD5 213C2	PE_U1003_HDD6_DN(0)	19BD5 213C2
HSV112	PE_U1003_HDD6_DP(1)	19BC5 213C2	PE_U1003_HDD6_DN(1)	19BC5 213C2
HSV113	PE_U1003_HDD7_DP(0)	19BD5 213C2	PE_U1003_HDD7_DN(0)	19BD5 213C2
HSV114	PE_U1003_HDD7_DP(1)	19BC5 213C2	PE_U1003_HDD7_DN(1)	19BC5 213C2
HSV115	PE_U1003_HDD8_DP(0)	19BB5 213C2	PE_U1003_HDD8_DN(0)	19BB5 213D2
HSV116	PE_U1003_HDD8_DP(1)	19BA5 213C2	PE_U1003_HDD8_DN(1)	19BA5 213D2
HSV117	PE_U1003_HDD9_DP(0)	19BB5 213C2	PE_U1003_HDD9_DN(0)	19BB5 213C2
HSV118	PE_U1003_HDD9_DP(1)	19BA5 213C2	PE_U1003_HDD9_DN(1)	19BA5 213C2

HSV100	PE_U1003_HDD10_DP(0)	19BB5 213C2	PE_U1003_HDD10_DN(0)	19BB5 213C2
HSV103	PE_U1003_HDD10_DP(1)	19BA5 213C2	PE_U1003_HDD10_DN(1)	19BA5 213C2
HSV119	PE_U1003_HDD11_DP(0)	19BD5 213C2	PE_U1003_HDD11_DN(0)	19BD5 213C2
HSV120	PE_U1003_HDD11_DP(1)	19BC5 213C2	PE_U1003_HDD11_DN(1)	19BC5 213C2
HSV121	PE_U1003_MP_DP(0)	196A2 213C2	PE_U1003_MP_DN(0)	196A2 213C2
HSV122	PE_U1003_MP_DP(1)	196A2 213C2	PE_U1003_MP_DN(1)	196A2 213C2
HSV123	PE_U1003_MP_DP(2)	196B2 213C2	PE_U1003_MP_DN(2)	196B2 213C2
HSV124	PE_U1003_MP_DP(3)	196B2 213C2	PE_U1003_MP_DN(3)	196B2 213C2
HSV125	PE_U1003_MP_DP(4)	196C2 213C2	PE_U1003_MP_DN(4)	196C2 213C2
HSV126	PE_U1003_MP_DP(5)	196C2 213C2	PE_U1003_MP_DN(5)	196C2 213C2
HSV127	PE_U1003_MP_DP(6)	196D2 213C2	PE_U1003_MP_DN(6)	196D2 213C2
HSV128	PE_U1003_MP_DP(7)	196D2 213C2	PE_U1003_MP_DN(7)	196D2 213C2

HSV129	PE_U1003_U1001_DP(0)	213C2 211B1	PE_U1003_U1001_DN(0)	213D2 211B1
HSV130	PE_U1003_U1001_DP(1)	213C2 211B1	PE_U1003_U1001_DN(1)	213D2 211B1
HSV131	PE_U1003_U1001_DP(2)	213C2 211B1	PE_U1003_U1001_DN(2)	213D2 211B1
HSV132	PE_U1003_U1001_DP(3)	213C2 211B1	PE_U1003_U1001_DN(3)	213D2 211B1
HSV133	PE_U1003_U1001_DP(4)	213C2 211B1	PE_U1003_U1001_DN(4)	213D2 211B1
HSV134	PE_U1003_U1001_DP(5)	213C2 211B1	PE_U1003_U1001_DN(5)	213D2 211B1
HSV135	PE_U1003_U1001_DP(6)	213C2 211B1	PE_U1003_U1001_DN(6)	213D2 211B1
HSV136	PE_U1003_U1001_DP(7)	213C2 211B1	PE_U1003_U1001_DN(7)	213D2 211B1
HSV137	PE_U1003_U1001_DP(8)	213C2 211B1	PE_U1003_U1001_DN(8)	213D2 211B1
HSV138	PE_U1003_U1001_DP(9)	213C2 211B1	PE_U1003_U1001_DN(9)	213D2 211B1
HSV139	PE_U1003_U1001_DP(10)	213C2 211B1	PE_U1003_U1001_DN(10)	213D2 211B1
HSV140	PE_U1003_U1001_DP(11)	213C2 211B1	PE_U1003_U1001_DN(11)	213D2 211B1
HSV141	PE_U1003_U1001_DP(12)	213C2 211B1	PE_U1003_U1001_DN(12)	213D2 211B1
HSV142	PE_U1003_U1001_DP(13)	213C2 211B1	PE_U1003_U1001_DN(13)	213D2 211B1
HSV143	PE_U1003_U1001_DP(14)	213C2 211B1	PE_U1003_U1001_DN(14)	213D2 211B1
HSV144	PE_U1003_U1001_DP(15)	213C2 211B1	PE_U1003_U1001_DN(15)	213D2 211B1

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HSV291	1 PE_HDD0_U1003_DP<0>	19BC7 213A2	
	2 PE_HDD0_U1003_DN<0>	19BC7 213B2	
HSV292	1 PE_HDD0_U1003_DP<1>	19BC7 213A2	
	2 PE_HDD0_U1003_DN<1>	19BC7 213B2	
HSV293	1 PE_HDD1_U1003_DP<0>	19BC7 213A2	
	2 PE_HDD1_U1003_DN<0>	19BD7 213B2	
HSV294	1 PE_HDD1_U1003_DP<1>	19BC7 213A2	
	2 PE_HDD1_U1003_DN<1>	19BC7 213B2	
HSV295	1 PE_HDD2_U1003_DP<0>	19BB7 213A2	
	2 PE_HDD2_U1003_DN<0>	19BB7 213B2	
HSV296	1 PE_HDD2_U1003_DP<1>	19BA7 213A2	
	2 PE_HDD2_U1003_DN<1>	19BA7 213B2	
HSV297	1 PE_HDD3_U1003_DP<0>	19BB7 213A2	
	2 PE_HDD3_U1003_DN<0>	19BB7 213B2	
HSV298	1 PE_HDD3_U1003_DP<1>	19BA7 213A2	
	2 PE_HDD3_U1003_DN<1>	19BA7 213B2	
HSV299	1 PE_HDD4_U1003_DP<0>	19BB7 213A2	
	2 PE_HDD4_U1003_DN<0>	19BB7 213B2	
HSV300	1 PE_HDD4_U1003_DP<1>	19BA7 213A2	
	2 PE_HDD4_U1003_DN<1>	19BA7 213B2	
HSV301	1 PE_HDD5_U1003_DP<0>	19BC7 213A2	
	2 PE_HDD5_U1003_DN<0>	19BC7 213B2	
HSV302	1 PE_HDD5_U1003_DP<1>	19BB7 213A2	
	2 PE_HDD5_U1003_DN<1>	19BB7 213B2	
HSV303	1 PE_HDD6_U1003_DP<0>	19BC5 213A2	
	2 PE_HDD6_U1003_DN<0>	19BC5 213B2	
HSV304	1 PE_HDD6_U1003_DP<1>	19BC5 213A2	
	2 PE_HDD6_U1003_DN<1>	19BC5 213B2	
HSV305	1 PE_HDD7_U1003_DP<0>	19BC5 213A2	
	2 PE_HDD7_U1003_DN<0>	19BD5 213B2	
HSV306	1 PE_HDD7_U1003_DP<1>	19BC5 213A2	
	2 PE_HDD7_U1003_DN<1>	19BC5 213B2	
HSV307	1 PE_HDD8_U1003_DP<0>	19BB5 213A2	
	2 PE_HDD8_U1003_DN<0>	19BB5 213B2	
HSV308	1 PE_HDD8_U1003_DP<1>	19BA5 213A2	
	2 PE_HDD8_U1003_DN<1>	19BA5 213B2	

HSV309	1 PE_HDD9_U1003_DP<0>	19BB5 213A2	
	2 PE_HDD9_U1003_DN<0>	19BB5 213B2	
HSV310	1 PE_HDD9_U1003_DP<1>	19BA5 213A2	
	2 PE_HDD9_U1003_DN<1>	19BA5 213B2	
HSV311	1 PE_HDD10_U1003_DP<0>	19BB5 213A2	
	2 PE_HDD10_U1003_DN<0>	19BB5 213B2	
HSV312	1 PE_HDD10_U1003_DP<1>	19BA5 213A2	
	2 PE_HDD10_U1003_DN<1>	19BA5 213B2	
HSV313	1 PE_HDD11_U1003_DP<0>	19BC5 213A2	
	2 PE_HDD11_U1003_DN<0>	19BC5 213B2	
HSV314	1 PE_HDD11_U1003_DP<1>	19BB5 213A2	
	2 PE_HDD11_U1003_DN<1>	19BB5 213B2	
HSV315	1 PE_MP_U1003_DP<0>	196A2 213A2	
	2 PE_MP_U1003_DN<0>	196A2 213B2	
HSV316	1 PE_MP_U1003_DP<1>	196A2 213A2	
	2 PE_MP_U1003_DN<1>	196A2 213B2	
HSV317	1 PE_MP_U1003_DP<2>	196B2 213A2	
	2 PE_MP_U1003_DN<2>	196B2 213B2	
HSV318	1 PE_MP_U1003_DP<3>	196B2 213A2	
	2 PE_MP_U1003_DN<3>	196B2 213B2	
HSV319	1 PE_MP_U1003_DP<4>	196C2 213A2	
	2 PE_MP_U1003_DN<4>	196C2 213B2	
HSV320	1 PE_MP_U1003_DP<5>	196C2 213A2	
	2 PE_MP_U1003_DN<5>	196C2 213B2	
HSV321	1 PE_MP_U1003_DP<6>	196C2 213A2	
	2 PE_MP_U1003_DN<6>	196C2 213B2	
HSV322	1 PE_MP_U1003_DP<7>	196C2 213A2	
	2 PE_MP_U1003_DN<7>	196D2 213B2	

HSV323	1 PE_U1001_U1003_DP<0>	211C1 213A2	
	2 PE_U1001_U1003_DN<0>	211D1 213B2	
HSV324	1 PE_U1001_U1003_DP<1>	211C1 213A2	
	2 PE_U1001_U1003_DN<1>	211D1 213B2	
HSV325	1 PE_U1001_U1003_DP<2>	211C1 213A2	
	2 PE_U1001_U1003_DN<2>	211D1 213B2	
HSV326	1 PE_U1001_U1003_DP<3>	211C1 213A2	
	2 PE_U1001_U1003_DN<3>	211D1 213B2	
HSV327	1 PE_U1001_U1003_DP<4>	211C1 213A2	
	2 PE_U1001_U1003_DN<4>	211D1 213B2	
HSV328	1 PE_U1001_U1003_DP<5>	211C1 213A2	
	2 PE_U1001_U1003_DN<5>	211D1 213B2	
HSV329	1 PE_U1001_U1003_DP<6>	211C1 213A2	
	2 PE_U1001_U1003_DN<6>	211D1 213B2	
HSV330	1 PE_U1001_U1003_DP<7>	211C1 213A2	
	2 PE_U1001_U1003_DN<7>	211D1 213B2	
HSV331	1 PE_U1001_U1003_DP<8>	211C1 213A2	
	2 PE_U1001_U1003_DN<8>	211D1 213B2	
HSV332	1 PE_U1001_U1003_DP<9>	211C1 213A2	
	2 PE_U1001_U1003_DN<9>	211D1 213B2	
HSV333	1 PE_U1001_U1003_DP<10>	211C1 213A2	
	2 PE_U1001_U1003_DN<10>	211D1 213B2	
HSV334	1 PE_U1001_U1003_DP<11>	211C1 213A2	
	2 PE_U1001_U1003_DN<11>	211D1 213B2	
HSV335	1 PE_U1001_U1003_DP<12>	211C1 213A2	
	2 PE_U1001_U1003_DN<12>	211D1 213B2	
HSV336	1 PE_U1001_U1003_DP<13>	211C1 213A2	
	2 PE_U1001_U1003_DN<13>	211D1 213B2	
HSV337	1 PE_U1001_U1003_DP<14>	211C1 213A2	
	2 PE_U1001_U1003_DN<14>	211D1 213B2	
HSV338	1 PE_U1001_U1003_DP<15>	211C1 213A2	
	2 PE_U1001_U1003_DN<15>	211D1 213B2	

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CR-262 : @WOLFCREEK_CONTROLLER_LIB.WOLFCREEK_CONTROLLER(SCH_1):PAGE666

HSV435	1 PE_U1005_HDD0_DP(0)	IN	19BD4	215C2
	2 PE_U1005_HDD0_DN(0)	IN	19BD4	215C2
HSV436	1 PE_U1005_HDD0_DP(1)	IN	19BC4	215C2
	2 PE_U1005_HDD0_DN(1)	IN	19BC4	215C2
HSV437	1 PE_U1005_HDD1_DP(0)	IN	19BD4	215C2
	2 PE_U1005_HDD1_DN(0)	IN	19BD4	215C2
HSV438	1 PE_U1005_HDD1_DP(1)	IN	19BC4	215C2
	2 PE_U1005_HDD1_DN(1)	IN	19BC4	215C2
HSV439	1 PE_U1005_HDD2_DP(0)	IN	19BB4	215C2
	2 PE_U1005_HDD2_DN(0)	IN	19BB4	215C2
HSV440	1 PE_U1005_HDD2_DP(1)	IN	19BA4	215C2
	2 PE_U1005_HDD2_DN(1)	IN	19BA4	215C2
HSV441	1 PE_U1005_HDD3_DP(0)	IN	19BB4	215C2
	2 PE_U1005_HDD3_DN(0)	IN	19BB4	215C2
HSV442	1 PE_U1005_HDD3_DP(1)	IN	19BA4	215C2
	2 PE_U1005_HDD3_DN(1)	IN	19BA4	215C2
HSV443	1 PE_U1005_HDD4_DP(0)	IN	19BB4	215C2
	2 PE_U1005_HDD4_DN(0)	IN	19BB4	215C2
HSV444	1 PE_U1005_HDD4_DP(1)	IN	19BB4	215C2
	2 PE_U1005_HDD4_DN(1)	IN	19BA4	215C2
HSV445	1 PE_U1005_HDD5_DP(0)	IN	19BD4	215C2
	2 PE_U1005_HDD5_DN(0)	IN	19BD4	215C2
HSV446	1 PE_U1005_HDD5_DP(1)	IN	19BC4	215C2
	2 PE_U1005_HDD5_DN(1)	IN	19BC4	215C2
HSV447	1 PE_U1005_HDD6_DP(0)	IN	19BD2	215C2
	2 PE_U1005_HDD6_DN(0)	IN	19BD2	215C2
HSV448	1 PE_U1005_HDD6_DP(1)	IN	19BC2	215C2
	2 PE_U1005_HDD6_DN(1)	IN	19BC2	215C2
HSV449	1 PE_U1005_HDD7_DP(0)	IN	19BD2	215C2
	2 PE_U1005_HDD7_DN(0)	IN	19BD2	215C2
HSV450	1 PE_U1005_HDD7_DP(1)	IN	19BC2	215C2
	2 PE_U1005_HDD7_DN(1)	IN	19BC2	215C2
HSV451	1 PE_U1005_HDD8_DP(0)	IN	19BB2	215C2
	2 PE_U1005_HDD8_DN(0)	IN	19BB2	215D2
HSV452	1 PE_U1005_HDD8_DP(1)	IN	19BA2	215C2
	2 PE_U1005_HDD8_DN(1)	IN	19BA2	215D2
HSV453	1 PE_U1005_HDD9_DP(0)	IN	19BB2	215C2
	2 PE_U1005_HDD9_DN(0)	IN	19BB2	215D2
HSV454	1 PE_U1005_HDD9_DP(1)	IN	19BA2	215C2
	2 PE_U1005_HDD9_DN(1)	IN	19BA2	215D2

HSV455	1 PE_U1005_HDD10_DP(0)	IN	19BB2	215C2
	2 PE_U1005_HDD10_DN(0)	IN	19BB2	215D2
HSV456	1 PE_U1005_HDD10_DP(1)	IN	19BA2	215C2
	2 PE_U1005_HDD10_DN(1)	IN	19BB2	215D2
HSV623	1 PE_U1005_HDD11_DP(0)	IN	19BD2	215C2
	2 PE_U1005_HDD11_DN(0)	IN	19BD2	215C2
HSV624	1 PE_U1005_HDD11_DP(1)	IN	19BC2	215C2
	2 PE_U1005_HDD11_DN(1)	IN	19BC2	215C2
HSV457	1 PE_U1005_MP_DP(0)	IN	196A4	215C2
	2 PE_U1005_MP_DN(0)	IN	196A4	215C2
HSV458	1 PE_U1005_MP_DP(1)	IN	196A4	215C2
	2 PE_U1005_MP_DN(1)	IN	196A4	215C2
HSV459	1 PE_U1005_MP_DP(2)	IN	196B4	215C2
	2 PE_U1005_MP_DN(2)	IN	196B4	215C2
HSV460	1 PE_U1005_MP_DP(3)	IN	196B4	215C2
	2 PE_U1005_MP_DN(3)	IN	196B4	215C2
HSV461	1 PE_U1005_MP_DP(4)	IN	196C4	215C2
	2 PE_U1005_MP_DN(4)	IN	196C4	215C2
HSV462	1 PE_U1005_MP_DP(5)	IN	196C4	215C2
	2 PE_U1005_MP_DN(5)	IN	196C4	215C2
HSV463	1 PE_U1005_MP_DP(6)	IN	196D4	215C2
	2 PE_U1005_MP_DN(6)	IN	196D4	215C2
HSV464	1 PE_U1005_MP_DP(7)	IN	196D4	215C2
	2 PE_U1005_MP_DN(7)	IN	196D4	215C2

HSV465	1 PE_U1005_U1001_DP(0)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(0)	IN	215D2	211B1
HSV466	1 PE_U1005_U1001_DP(1)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(1)	IN	215D2	211B1
HSV467	1 PE_U1005_U1001_DP(2)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(2)	IN	215D2	211B1
HSV468	1 PE_U1005_U1001_DP(3)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(3)	IN	215D2	211B1
HSV469	1 PE_U1005_U1001_DP(4)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(4)	IN	215D2	211B1
HSV470	1 PE_U1005_U1001_DP(5)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(5)	IN	215D2	211B1
HSV471	1 PE_U1005_U1001_DP(6)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(6)	IN	215D2	211B1
HSV472	1 PE_U1005_U1001_DP(7)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(7)	IN	215D2	211B1
HSV473	1 PE_U1005_U1001_DP(8)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(8)	IN	215D2	211B1
HSV474	1 PE_U1005_U1001_DP(9)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(9)	IN	215D2	211B1
HSV475	1 PE_U1005_U1001_DP(10)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(10)	IN	215D2	211B1
HSV476	1 PE_U1005_U1001_DP(11)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(11)	IN	215D2	211B1
HSV477	1 PE_U1005_U1001_DP(12)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(12)	IN	215D2	211B1
HSV478	1 PE_U1005_U1001_DP(13)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(13)	IN	215D2	211B1
HSV479	1 PE_U1005_U1001_DP(14)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(14)	IN	215D2	211B1
HSV480	1 PE_U1005_U1001_DP(15)	IN	215C2	211B1
	2 PE_U1005_U1001_DN(15)	IN	215D2	211B1

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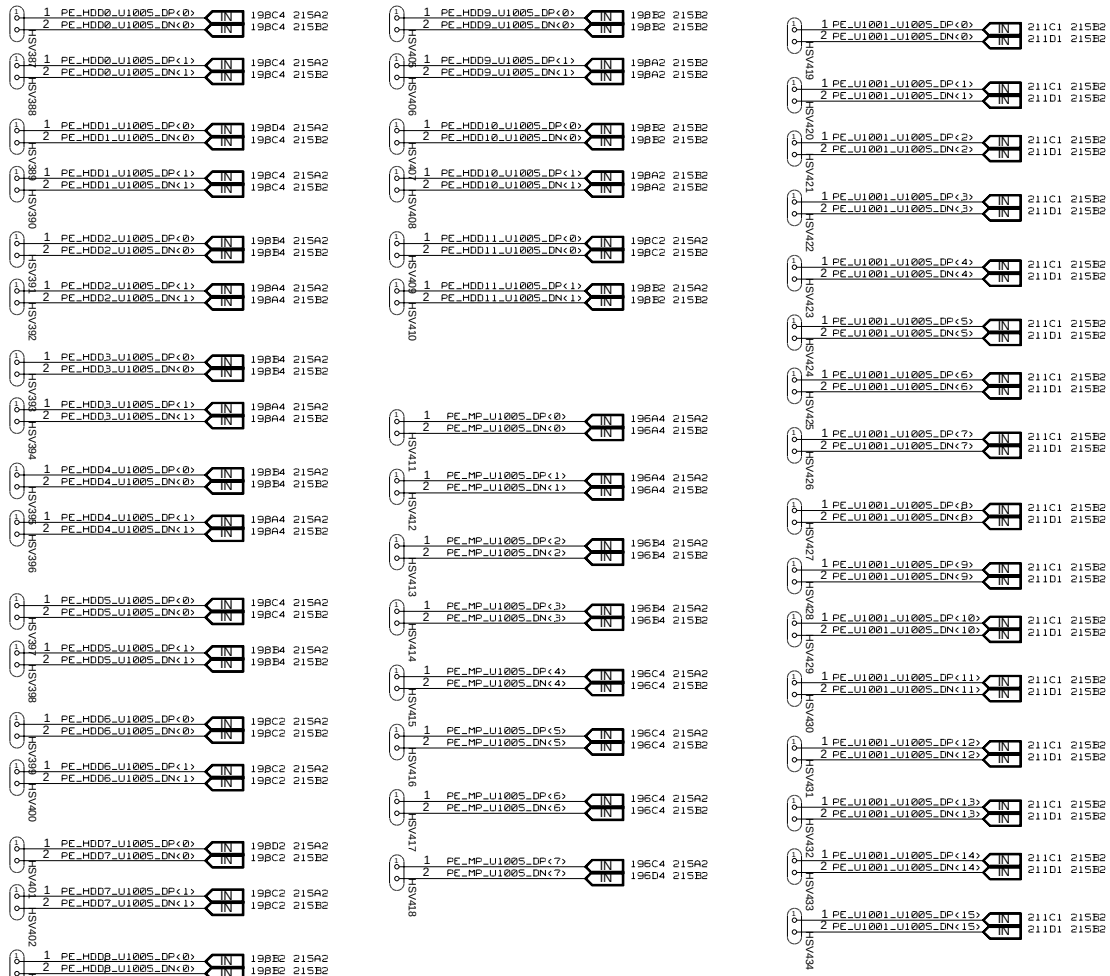
CR-263 : @WOLFCREEK_CONTROLLER_LIB.WOLFCREEK_CONTROLLER(SCH_1):PAGE667



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REV: <REVISION>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

HSV145	1	PE_U1002_HDD0_DP<0>	IN	194D7	212C2		
	2	PE_U1002_HDD0_DN<0>	IN	194D7	212D2		
HSV146	1	PE_U1002_HDD0_DP<1>	IN	194C7	212C2		
	2	PE_U1002_HDD0_DN<1>	IN	194C7	212D2		
HSV147	1	PE_U1002_HDD1_DP<0>	IN	194D7	212C2		
	2	PE_U1002_HDD1_DN<0>	IN	194D7	212D2		
HSV148	1	PE_U1002_HDD1_DP<1>	IN	194C7	212C2		
	2	PE_U1002_HDD1_DN<1>	IN	194C7	212D2		
HSV149	1	PE_U1002_HDD2_DP<0>	IN	194E5	212C2		
	2	PE_U1002_HDD2_DN<0>	IN	194E5	212D2		
HSV150	1	PE_U1002_HDD2_DP<1>	IN	194A5	212C2		
	2	PE_U1002_HDD2_DN<1>	IN	194A5	212D2		
HSV151	1	PE_U1002_HDD3_DP<0>	IN	194E5	212C2		
	2	PE_U1002_HDD3_DN<0>	IN	194E5	212D2		
HSV152	1	PE_U1002_HDD3_DP<1>	IN	194A5	212C2		
	2	PE_U1002_HDD3_DN<1>	IN	194A5	212D2		
HSV153	1	PE_U1002_HDD4_DP<0>	IN	194E5	212C2		
	2	PE_U1002_HDD4_DN<0>	IN	194E5	212D2		
HSV154	1	PE_U1002_HDD4_DP<1>	IN	194A5	212C2		
	2	PE_U1002_HDD4_DN<1>	IN	194E5	212D2		
HSV155	1	PE_U1002_HDD5_DP<0>	IN	194D5	212C2		
	2	PE_U1002_HDD5_DN<0>	IN	194D5	212D2		
HSV156	1	PE_U1002_HDD5_DP<1>	IN	194C5	212C2		
	2	PE_U1002_HDD5_DN<1>	IN	194C5	212D2		
HSV157	1	PE_U1002_HDD6_DP<0>	IN	194E7	212C2		
	2	PE_U1002_HDD6_DN<0>	IN	194E7	212D2		
HSV158	1	PE_U1002_HDD6_DP<1>	IN	194E7	212C2		
	2	PE_U1002_HDD6_DN<1>	IN	194A7	212D2		
HSV159	1	PE_U1002_HDD7_DP<0>	IN	194D7	212C2		
	2	PE_U1002_HDD7_DN<0>	IN	194D7	212D2		
HSV160	1	PE_U1002_HDD7_DP<1>	IN	194C7	212C2		
	2	PE_U1002_HDD7_DN<1>	IN	194C7	212D2		
HSV161	1	PE_U1002_HDD8_DP<0>	IN	194D5	212C2		
	2	PE_U1002_HDD8_DN<0>	IN	194D5	212D2		
HSV162	1	PE_U1002_HDD8_DP<1>	IN	194C5	212C2		
	2	PE_U1002_HDD8_DN<1>	IN	194C5	212D2		
HSV163	1	PE_U1002_HDD9_DP<0>	IN	194D5	212C2		
	2	PE_U1002_HDD9_DN<0>	IN	194D5	212D2		
HSV164	1	PE_U1002_HDD9_DP<1>	IN	194C5	212C2		
	2	PE_U1002_HDD9_DN<1>	IN	194C5	212D2		
HSV165	1	PE_U1002_HDD10_DP<0>	IN	194E7	212C2		
	2	PE_U1002_HDD10_DN<0>	IN	194E7	212D2		
HSV166	1	PE_U1002_HDD10_DP<1>	IN	194A7	212C2		
	2	PE_U1002_HDD10_DN<1>	IN	194A7	212D2		
HSV481	1	PE_U1002_HDD11_DP<0>	IN	194E7	212C2		
	2	PE_U1002_HDD11_DN<0>	IN	194E7	212D2		
HSV482	1	PE_U1002_HDD11_DP<1>	IN	194A7	212C2		
	2	PE_U1002_HDD11_DN<1>	IN	194A7	212D2		
HSV167	1	PE_U1002_MP_DP<0>	IN	196A5	212D2		
	2	PE_U1002_MP_DN<0>	IN	196A5	212D2		
HSV168	1	PE_U1002_MP_DP<1>	IN	196A5	212D2		
	2	PE_U1002_MP_DN<1>	IN	196E5	212D2		
HSV169	1	PE_U1002_MP_DP<2>	IN	196E5	212D2		
	2	PE_U1002_MP_DN<2>	IN	196E5	212D2		
HSV170	1	PE_U1002_MP_DP<3>	IN	196E5	212D2		
	2	PE_U1002_MP_DN<3>	IN	196E5	212D2		
HSV171	1	PE_U1002_MP_DP<4>	IN	196C5	212D2		
	2	PE_U1002_MP_DN<4>	IN	196C5	212D2		
HSV172	1	PE_U1002_MP_DP<5>	IN	196C5	212D2		
	2	PE_U1002_MP_DN<5>	IN	196C5	212D2		
HSV173	1	PE_U1002_MP_DP<6>	IN	196D5	212D2		
	2	PE_U1002_MP_DN<6>	IN	196D5	212D2		
HSV174	1	PE_U1002_MP_DP<7>	IN	196D5	212D2		
	2	PE_U1002_MP_DN<7>	IN	196D5	212D2		
HSV175	1	PE_U1002_U1000_DP<0>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<0>	IN	212D2	210B1		
HSV176	1	PE_U1002_U1000_DP<1>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<1>	IN	212D2	210B1		
HSV177	1	PE_U1002_U1000_DP<2>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<2>	IN	212D2	210B1		
HSV178	1	PE_U1002_U1000_DP<3>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<3>	IN	212D2	210B1		
HSV179	1	PE_U1002_U1000_DP<4>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<4>	IN	212D2	210B1		
HSV180	1	PE_U1002_U1000_DP<5>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<5>	IN	212D2	210B1		
HSV181	1	PE_U1002_U1000_DP<6>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<6>	IN	212D2	210B1		
HSV182	1	PE_U1002_U1000_DP<7>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<7>	IN	212D2	210B1		
HSV183	1	PE_U1002_U1000_DP<8>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<8>	IN	212D2	210B1		
HSV184	1	PE_U1002_U1000_DP<9>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<9>	IN	212D2	210B1		
HSV185	1	PE_U1002_U1000_DP<10>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<10>	IN	212D2	210B1		
HSV186	1	PE_U1002_U1000_DP<11>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<11>	IN	212D2	210B1		
HSV187	1	PE_U1002_U1000_DP<12>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<12>	IN	212D2	210B1		
HSV188	1	PE_U1002_U1000_DP<13>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<13>	IN	212D2	210B1		
HSV189	1	PE_U1002_U1000_DP<14>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<14>	IN	212D2	210B1		
HSV190	1	PE_U1002_U1000_DP<15>	IN	212C2	210B1		
	2	PE_U1002_U1000_DN<15>	IN	212D2	210B1		

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CR-265 : @WOLFCREEK_CONTROLLER_LIB.WOLFCREEK_CONTROLLER(SCH_1):PAGE669

HSV191	1 PE_HDD0_U1002_DP(0)	IN	194C7	212B2
	2 PE_HDD0_U1002_DN(0)	IN	194C7	212B2
HSV192	1 PE_HDD0_U1002_DP(1)	IN	194C7	212B2
	2 PE_HDD0_U1002_DN(1)	IN	194C7	212B2
HSV193	1 PE_HDD1_U1002_DP(0)	IN	194D7	212B2
	2 PE_HDD1_U1002_DN(0)	IN	194D7	212B2
HSV194	1 PE_HDD1_U1002_DP(1)	IN	194C7	212B2
	2 PE_HDD1_U1002_DN(1)	IN	194C7	212B2
HSV195	1 PE_HDD2_U1002_DP(0)	IN	194B5	212B2
	2 PE_HDD2_U1002_DN(0)	IN	194B5	212B2
HSV196	1 PE_HDD2_U1002_DP(1)	IN	194A5	212B2
	2 PE_HDD2_U1002_DN(1)	IN	194A5	212B2
HSV197	1 PE_HDD3_U1002_DP(0)	IN	194B5	212B2
	2 PE_HDD3_U1002_DN(0)	IN	194B5	212B2
HSV198	1 PE_HDD3_U1002_DP(1)	IN	194A5	212B2
	2 PE_HDD3_U1002_DN(1)	IN	194A5	212B2
HSV199	1 PE_HDD4_U1002_DP(0)	IN	194B5	212B2
	2 PE_HDD4_U1002_DN(0)	IN	194B5	212B2
HSV200	1 PE_HDD4_U1002_DP(1)	IN	194A5	212B2
	2 PE_HDD4_U1002_DN(1)	IN	194A5	212B2
HSV201	1 PE_HDD5_U1002_DP(0)	IN	194C5	212B2
	2 PE_HDD5_U1002_DN(0)	IN	194C5	212B2
HSV202	1 PE_HDD5_U1002_DP(1)	IN	194C5	212B2
	2 PE_HDD5_U1002_DN(1)	IN	194B5	212B2
HSV203	1 PE_HDD6_U1002_DP(0)	IN	194B7	212B2
	2 PE_HDD6_U1002_DN(0)	IN	194B7	212B2
HSV204	1 PE_HDD6_U1002_DP(1)	IN	194A7	212B2
	2 PE_HDD6_U1002_DN(1)	IN	194A7	212B2
HSV205	1 PE_HDD7_U1002_DP(0)	IN	194C7	212B2
	2 PE_HDD7_U1002_DN(0)	IN	194C7	212B2
HSV206	1 PE_HDD7_U1002_DP(1)	IN	194C7	212B2
	2 PE_HDD7_U1002_DN(1)	IN	194B7	212B2
HSV207	1 PE_HDD8_U1002_DP(0)	IN	194C5	212B2
	2 PE_HDD8_U1002_DN(0)	IN	194C5	212B2
HSV208	1 PE_HDD8_U1002_DP(1)	IN	194C5	212B2
	2 PE_HDD8_U1002_DN(1)	IN	194C5	212B2
HSV209	1 PE_HDD9_U1002_DP(0)	IN	194D5	212B2
	2 PE_HDD9_U1002_DN(0)	IN	194D5	212B2
HSV210	1 PE_HDD9_U1002_DP(1)	IN	194C5	212B2
	2 PE_HDD9_U1002_DN(1)	IN	194C5	212B2
HSV211	1 PE_HDD10_U1002_DP(0)	IN	194B7	212B2
	2 PE_HDD10_U1002_DN(0)	IN	194B7	212B2
HSV212	1 PE_HDD10_U1002_DP(1)	IN	194A7	212B2
	2 PE_HDD10_U1002_DN(1)	IN	194A7	212B2
HSV213	1 PE_HDD11_U1002_DP(0)	IN	194B7	212B2
	2 PE_HDD11_U1002_DN(0)	IN	194B7	212B2
HSV214	1 PE_HDD11_U1002_DP(1)	IN	194A7	212B2
	2 PE_HDD11_U1002_DN(1)	IN	194A7	212B2
HSV215	1 PE_MP_U1002_DP(0)	IN	195A5	212B2
	2 PE_MP_U1002_DN(0)	IN	195A5	212B2
HSV216	1 PE_MP_U1002_DP(1)	IN	195A5	212B2
	2 PE_MP_U1002_DN(1)	IN	195A5	212B2
HSV217	1 PE_MP_U1002_DP(2)	IN	195B5	212B2
	2 PE_MP_U1002_DN(2)	IN	195B5	212B2
HSV218	1 PE_MP_U1002_DP(3)	IN	195B5	212B2
	2 PE_MP_U1002_DN(3)	IN	195B5	212B2
HSV219	1 PE_MP_U1002_DP(4)	IN	195C5	212B2
	2 PE_MP_U1002_DN(4)	IN	195C5	212B2
HSV220	1 PE_MP_U1002_DP(5)	IN	195C5	212B2
	2 PE_MP_U1002_DN(5)	IN	195C5	212B2
HSV221	1 PE_MP_U1002_DP(6)	IN	195C5	212B2
	2 PE_MP_U1002_DN(6)	IN	195C5	212B2
HSV222	1 PE_MP_U1002_DP(7)	IN	195C5	212B2
	2 PE_MP_U1002_DN(7)	IN	195D5	212B2
HSV223	1 PE_U1000_U1002_DP(0)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(0)	IN	210D1	212B2
HSV224	1 PE_U1000_U1002_DP(1)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(1)	IN	210D1	212B2
HSV225	1 PE_U1000_U1002_DP(2)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(2)	IN	210D1	212B2
HSV226	1 PE_U1000_U1002_DP(3)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(3)	IN	210D1	212B2
HSV227	1 PE_U1000_U1002_DP(4)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(4)	IN	210D1	212B2
HSV228	1 PE_U1000_U1002_DP(5)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(5)	IN	210D1	212B2
HSV229	1 PE_U1000_U1002_DP(6)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(6)	IN	210D1	212B2
HSV230	1 PE_U1000_U1002_DP(7)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(7)	IN	210D1	212B2
HSV231	1 PE_U1000_U1002_DP(8)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(8)	IN	210D1	212B2
HSV232	1 PE_U1000_U1002_DP(9)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(9)	IN	210D1	212B2
HSV233	1 PE_U1000_U1002_DP(10)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(10)	IN	210D1	212B2
HSV234	1 PE_U1000_U1002_DP(11)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(11)	IN	210D1	212B2
HSV235	1 PE_U1000_U1002_DP(12)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(12)	IN	210D1	212B2
HSV236	1 PE_U1000_U1002_DP(13)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(13)	IN	210D1	212B2
HSV237	1 PE_U1000_U1002_DP(14)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(14)	IN	210D1	212B2
HSV238	1 PE_U1000_U1002_DP(15)	IN	210C1	212B2
	2 PE_U1000_U1002_DN(15)	IN	210D1	212B2

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HSV238	1	PE_U1004_HDD0_DP(0)	IN	194D3	214C2		
	2	PE_U1004_HDD0_DN(0)	IN	194D3	214C2		
HSV240	1	PE_U1004_HDD0_DP(1)	IN	194C3	214C2		
	2	PE_U1004_HDD0_DN(1)	IN	194C3	214C2		
HSV241	1	PE_U1004_HDD1_DP(0)	IN	194D3	214C2		
	2	PE_U1004_HDD1_DN(0)	IN	194D3	214C2		
HSV242	1	PE_U1004_HDD1_DP(1)	IN	194C3	214C2		
	2	PE_U1004_HDD1_DN(1)	IN	194C3	214C2		
HSV243	1	PE_U1004_HDD2_DP(0)	IN	194B1	214C2		
	2	PE_U1004_HDD2_DN(0)	IN	194B1	214C2		
HSV244	1	PE_U1004_HDD2_DP(1)	IN	194A1	214C2		
	2	PE_U1004_HDD2_DN(1)	IN	194A1	214C2		
HSV245	1	PE_U1004_HDD3_DP(0)	IN	194B1	214C2		
	2	PE_U1004_HDD3_DN(0)	IN	194B1	214D2		
HSV246	1	PE_U1004_HDD3_DP(1)	IN	194A1	214C2		
	2	PE_U1004_HDD3_DN(1)	IN	194A1	214D2		
HSV247	1	PE_U1004_HDD4_DP(0)	IN	194B1	214C2		
	2	PE_U1004_HDD4_DN(0)	IN	194B1	214D2		
HSV248	1	PE_U1004_HDD4_DP(1)	IN	194B1	214C2		
	2	PE_U1004_HDD4_DN(1)	IN	194B1	214D2		
HSV249	1	PE_U1004_HDD5_DP(0)	IN	194D1	214C2		
	2	PE_U1004_HDD5_DN(0)	IN	194D1	214C2		
HSV250	1	PE_U1004_HDD5_DP(1)	IN	194C1	214C2		
	2	PE_U1004_HDD5_DN(1)	IN	194C1	214C2		
HSV251	1	PE_U1004_HDD6_DP(0)	IN	194B3	214C2		
	2	PE_U1004_HDD6_DN(0)	IN	194B3	214C2		
HSV252	1	PE_U1004_HDD6_DP(1)	IN	194B3	214C2		
	2	PE_U1004_HDD6_DN(1)	IN	194B3	214C2		
HSV253	1	PE_U1004_HDD7_DP(0)	IN	194D3	214C2		
	2	PE_U1004_HDD7_DN(0)	IN	194D3	214C2		
HSV254	1	PE_U1004_HDD7_DP(1)	IN	194C3	214C2		
	2	PE_U1004_HDD7_DN(1)	IN	194C3	214C2		
HSV255	1	PE_U1004_HDD8_DP(0)	IN	194D1	214C2		
	2	PE_U1004_HDD8_DN(0)	IN	194D1	214C2		
HSV256	1	PE_U1004_HDD8_DP(1)	IN	194C1	214C2		
	2	PE_U1004_HDD8_DN(1)	IN	194C1	214C2		
HSV257	1	PE_U1004_HDD9_DP(0)	IN	194D1	214C2		
	2	PE_U1004_HDD9_DN(0)	IN	194D1	214D2		
HSV258	1	PE_U1004_HDD9_DP(1)	IN	194C1	214C2		
	2	PE_U1004_HDD9_DN(1)	IN	194C1	214D2		
HSV259	1	PE_U1004_HDD10_DP(0)	IN	194B3	214C2		
	2	PE_U1004_HDD10_DN(0)	IN	194B3	214C2		
HSV260	1	PE_U1004_HDD10_DP(1)	IN	194A3	214C2		
	2	PE_U1004_HDD10_DN(1)	IN	194A3	214C2		
HSV483	1	PE_U1004_HDD11_DP(0)	IN	194B3	214C2		
	2	PE_U1004_HDD11_DN(0)	IN	194B3	214C2		
HSV484	1	PE_U1004_HDD11_DP(1)	IN	194A3	214C2		
	2	PE_U1004_HDD11_DN(1)	IN	194A3	214C2		
HSV261	1	PE_U1004_MP_DP(0)	IN	196A7	214C2		
	2	PE_U1004_MP_DN(0)	IN	196A7	214D2		
HSV262	1	PE_U1004_MP_DP(1)	IN	196A7	214C2		
	2	PE_U1004_MP_DN(1)	IN	196B7	214D2		
HSV263	1	PE_U1004_MP_DP(2)	IN	196B7	214C2		
	2	PE_U1004_MP_DN(2)	IN	196B7	214D2		
HSV264	1	PE_U1004_MP_DP(3)	IN	196B7	214C2		
	2	PE_U1004_MP_DN(3)	IN	196B7	214D2		
HSV265	1	PE_U1004_MP_DP(4)	IN	196C7	214C2		
	2	PE_U1004_MP_DN(4)	IN	196C7	214D2		
HSV266	1	PE_U1004_MP_DP(5)	IN	196C7	214C2		
	2	PE_U1004_MP_DN(5)	IN	196C7	214D2		
HSV267	1	PE_U1004_MP_DP(6)	IN	196D7	214C2		
	2	PE_U1004_MP_DN(6)	IN	196D7	214D2		
HSV268	1	PE_U1004_MP_DP(7)	IN	196D7	214C2		
	2	PE_U1004_MP_DN(7)	IN	196D7	214D2		
HSV269	1	PE_U1004_U1000_DP(0)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(0)	IN	214C2	210B1		
HSV270	1	PE_U1004_U1000_DP(1)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(1)	IN	214C2	210B1		
HSV271	1	PE_U1004_U1000_DP(2)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(2)	IN	214C2	210B1		
HSV272	1	PE_U1004_U1000_DP(3)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(3)	IN	214C2	210B1		
HSV273	1	PE_U1004_U1000_DP(4)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(4)	IN	214C2	210B1		
HSV274	1	PE_U1004_U1000_DP(5)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(5)	IN	214C2	210B1		
HSV275	1	PE_U1004_U1000_DP(6)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(6)	IN	214C2	210B1		
HSV276	1	PE_U1004_U1000_DP(7)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(7)	IN	214C2	210B1		
HSV277	1	PE_U1004_U1000_DP(8)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(8)	IN	214C2	210B1		
HSV278	1	PE_U1004_U1000_DP(9)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(9)	IN	214C2	210B1		
HSV279	1	PE_U1004_U1000_DP(10)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(10)	IN	214C2	210B1		
HSV280	1	PE_U1004_U1000_DP(11)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(11)	IN	214C2	210B1		
HSV281	1	PE_U1004_U1000_DP(12)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(12)	IN	214C2	210B1		
HSV282	1	PE_U1004_U1000_DP(13)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(13)	IN	214C2	210B1		
HSV283	1	PE_U1004_U1000_DP(14)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(14)	IN	214C2	210B1		
HSV284	1	PE_U1004_U1000_DP(15)	IN	214C2	210B1		
	2	PE_U1004_U1000_DN(15)	IN	214C2	210B1		

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HSV339	1 PE_HDD0_U1004_DP(0)	IN	194C3	214A2
	2 PE_HDD0_U1004_DN(0)	IN	194C3	214B2
HSV340	1 PE_HDD0_U1004_DP(1)	IN	194C3	214A2
	2 PE_HDD0_U1004_DN(1)	IN	194C3	214B2
HSV341	1 PE_HDD1_U1004_DP(0)	IN	194D3	214A2
	2 PE_HDD1_U1004_DN(0)	IN	194D3	214B2
HSV342	1 PE_HDD1_U1004_DP(1)	IN	194C3	214A2
	2 PE_HDD1_U1004_DN(1)	IN	194C3	214B2
HSV343	1 PE_HDD2_U1004_DP(0)	IN	194B1	214B2
	2 PE_HDD2_U1004_DN(0)	IN	194B1	214B2
HSV344	1 PE_HDD2_U1004_DP(1)	IN	194A1	214B2
	2 PE_HDD2_U1004_DN(1)	IN	194A1	214B2
HSV345	1 PE_HDD3_U1004_DP(0)	IN	194B1	214B2
	2 PE_HDD3_U1004_DN(0)	IN	194B1	214B2
HSV346	1 PE_HDD3_U1004_DP(1)	IN	194A1	214B2
	2 PE_HDD3_U1004_DN(1)	IN	194A1	214B2
HSV347	1 PE_HDD4_U1004_DP(0)	IN	194B1	214B2
	2 PE_HDD4_U1004_DN(0)	IN	194B1	214B2
HSV348	1 PE_HDD4_U1004_DP(1)	IN	194A1	214B2
	2 PE_HDD4_U1004_DN(1)	IN	194A1	214B2
HSV349	1 PE_HDD5_U1004_DP(0)	IN	194C1	214B2
	2 PE_HDD5_U1004_DN(0)	IN	194C1	214B2
HSV350	1 PE_HDD5_U1004_DP(1)	IN	194B1	214B2
	2 PE_HDD5_U1004_DN(1)	IN	194C1	214B2
HSV351	1 PE_HDD6_U1004_DP(0)	IN	194B3	214A2
	2 PE_HDD6_U1004_DN(0)	IN	194B3	214B2
HSV352	1 PE_HDD6_U1004_DP(1)	IN	194A3	214A2
	2 PE_HDD6_U1004_DN(1)	IN	194A3	214B2
HSV353	1 PE_HDD7_U1004_DP(0)	IN	194C3	214A2
	2 PE_HDD7_U1004_DN(0)	IN	194C3	214B2
HSV354	1 PE_HDD7_U1004_DP(1)	IN	194B3	214A2
	2 PE_HDD7_U1004_DN(1)	IN	194C3	214B2
HSV355	1 PE_HDD8_U1004_DP(0)	IN	194C1	214B2
	2 PE_HDD8_U1004_DN(0)	IN	194C1	214B2
HSV356	1 PE_HDD8_U1004_DP(1)	IN	194C1	214B2
	2 PE_HDD8_U1004_DN(1)	IN	194C1	214B2

HSV357	1 PE_HDD9_U1004_DP(0)	IN	194D1	214B2
	2 PE_HDD9_U1004_DN(0)	IN	194D1	214B2
HSV358	1 PE_HDD9_U1004_DP(1)	IN	194C1	214B2
	2 PE_HDD9_U1004_DN(1)	IN	194C1	214B2
HSV359	1 PE_HDD10_U1004_DP(0)	IN	194B3	214A2
	2 PE_HDD10_U1004_DN(0)	IN	194B3	214B2
HSV360	1 PE_HDD10_U1004_DP(1)	IN	194A3	214A2
	2 PE_HDD10_U1004_DN(1)	IN	194A3	214B2
HSV361	1 PE_HDD11_U1004_DP(0)	IN	194B3	214A2
	2 PE_HDD11_U1004_DN(0)	IN	194B3	214B2
HSV362	1 PE_HDD11_U1004_DP(1)	IN	194A3	214A2
	2 PE_HDD11_U1004_DN(1)	IN	194A3	214B2
HSV363	1 PE_MP_U1004_DP(0)	IN	196A7	214B2
	2 PE_MP_U1004_DN(0)	IN	196A7	214B2
HSV364	1 PE_MP_U1004_DP(1)	IN	196A7	214B2
	2 PE_MP_U1004_DN(1)	IN	196A7	214B2
HSV365	1 PE_MP_U1004_DP(2)	IN	196B7	214B2
	2 PE_MP_U1004_DN(2)	IN	196B7	214B2
HSV366	1 PE_MP_U1004_DP(3)	IN	196B7	214B2
	2 PE_MP_U1004_DN(3)	IN	196B7	214B2
HSV367	1 PE_MP_U1004_DP(4)	IN	196C7	214B2
	2 PE_MP_U1004_DN(4)	IN	196C7	214B2
HSV368	1 PE_MP_U1004_DP(5)	IN	196C7	214B2
	2 PE_MP_U1004_DN(5)	IN	196C7	214B2
HSV369	1 PE_MP_U1004_DP(6)	IN	196C7	214B2
	2 PE_MP_U1004_DN(6)	IN	196C7	214B2
HSV370	1 PE_MP_U1004_DP(7)	IN	196D7	214B2
	2 PE_MP_U1004_DN(7)	IN	196C7	214B2

HSV371	1 PE_U1000_U1004_DP(0)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(0)	IN	210D1	214B2
HSV372	1 PE_U1000_U1004_DP(1)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(1)	IN	210D1	214B2
HSV373	1 PE_U1000_U1004_DP(2)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(2)	IN	210D1	214B2
HSV374	1 PE_U1000_U1004_DP(3)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(3)	IN	210D1	214B2
HSV375	1 PE_U1000_U1004_DP(4)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(4)	IN	210D1	214B2
HSV376	1 PE_U1000_U1004_DP(5)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(5)	IN	210D1	214B2
HSV377	1 PE_U1000_U1004_DP(6)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(6)	IN	210D1	214B2
HSV378	1 PE_U1000_U1004_DP(7)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(7)	IN	210D1	214B2
HSV379	1 PE_U1000_U1004_DP(8)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(8)	IN	210D1	214B2
HSV380	1 PE_U1000_U1004_DP(9)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(9)	IN	210D1	214B2
HSV381	1 PE_U1000_U1004_DP(10)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(10)	IN	210D1	214B2
HSV382	1 PE_U1000_U1004_DP(11)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(11)	IN	210D1	214B2
HSV383	1 PE_U1000_U1004_DP(12)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(12)	IN	210D1	214B2
HSV384	1 PE_U1000_U1004_DP(13)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(13)	IN	210D1	214B2
HSV385	1 PE_U1000_U1004_DP(14)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(14)	IN	210D1	214B2
HSV386	1 PE_U1000_U1004_DP(15)	IN	210C1	214A2
	2 PE_U1000_U1004_DN(15)	IN	210D1	214B2

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HSV485	1 PE_U1002_MEZZ_DP<0>	IN	212C2 B7DB 269D7	
	2 PE_U1002_MEZZ_DN<0>	IN	212D2 B7DB 269D7	
HSV486	1 PE_U1002_MEZZ_DP<1>	IN	212C2 B7DB 269D7	
	2 PE_U1002_MEZZ_DN<1>	IN	212D2 B7DB 269D7	
HSV487	1 PE_U1002_MEZZ_DP<2>	IN	212C2 B7DB 269D7	
	2 PE_U1002_MEZZ_DN<2>	IN	212D2 B7DB 269D7	
HSV488	1 PE_U1002_MEZZ_DP<3>	IN	212C2 B7DB 269D7	
	2 PE_U1002_MEZZ_DN<3>	IN	212D2 B7DB 269D7	
HSV489	1 PE_U1002_MEZZ_DP<4>	IN	212C2 B7DB 269C7	
	2 PE_U1002_MEZZ_DN<4>	IN	212D2 B7DB 269C7	
HSV490	1 PE_U1002_MEZZ_DP<5>	IN	212C2 B7DB 269C7	
	2 PE_U1002_MEZZ_DN<5>	IN	212D2 B7DB 269C7	
HSV491	1 PE_U1002_MEZZ_DP<6>	IN	212C2 B7DB 269C7	
	2 PE_U1002_MEZZ_DN<6>	IN	212D2 B7DB 269C7	
HSV492	1 PE_U1002_MEZZ_DP<7>	IN	212C2 B7DB 269C7	
	2 PE_U1002_MEZZ_DN<7>	IN	212D2 B7DB 269C7	
HSV493	1 PE_U1002_MEZZ_DP<8>	IN	212C2 B7DB 269C7	
	2 PE_U1002_MEZZ_DN<8>	IN	212D2 B7DB 269C7	
HSV494	1 PE_U1002_MEZZ_DP<9>	IN	212C2 B7DB 269B7	
	2 PE_U1002_MEZZ_DN<9>	IN	212D2 B7DB 269B7	
HSV495	1 PE_U1002_MEZZ_DP<10>	IN	212C2 B7DB 269B7	
	2 PE_U1002_MEZZ_DN<10>	IN	212D2 B7DB 269B7	
HSV496	1 PE_U1002_MEZZ_DP<11>	IN	212C2 B7DB 269B7	
	2 PE_U1002_MEZZ_DN<11>	IN	212D2 B7DB 269B7	
HSV497	1 PE_U1002_MEZZ_DP<12>	IN	212C2 B7DB 269B7	
	2 PE_U1002_MEZZ_DN<12>	IN	212D2 B7DB 269B7	
HSV498	1 PE_U1002_MEZZ_DP<13>	IN	212C2 B7DB 269B7	
	2 PE_U1002_MEZZ_DN<13>	IN	212D2 B7DB 269B7	
HSV499	1 PE_U1002_MEZZ_DP<14>	IN	212C2 B7DB 269A7	
	2 PE_U1002_MEZZ_DN<14>	IN	212D2 B7DB 269A7	
HSV500	1 PE_U1002_MEZZ_DP<15>	IN	212C2 B7DB 269A7	
	2 PE_U1002_MEZZ_DN<15>	IN	212D2 B7DB 269A7	

HSV501	1 PE_U1003_MEZZ_DP<0>	IN	213C2 B9D7 269D5	
	2 PE_U1003_MEZZ_DN<0>	IN	213C2 B9D7 269D5	
HSV502	1 PE_U1003_MEZZ_DP<1>	IN	213C2 B9D7 269D5	
	2 PE_U1003_MEZZ_DN<1>	IN	213C2 B9D7 269D5	
HSV503	1 PE_U1003_MEZZ_DP<2>	IN	213C2 B9D7 269D5	
	2 PE_U1003_MEZZ_DN<2>	IN	213C2 B9D7 269D5	
HSV504	1 PE_U1003_MEZZ_DP<3>	IN	213C2 B9D7 269D5	
	2 PE_U1003_MEZZ_DN<3>	IN	213C2 B9D7 269D5	
HSV505	1 PE_U1003_MEZZ_DP<4>	IN	213C2 B9D7 269C5	
	2 PE_U1003_MEZZ_DN<4>	IN	213C2 B9D7 269C5	
HSV506	1 PE_U1003_MEZZ_DP<5>	IN	213C2 B9D7 269C5	
	2 PE_U1003_MEZZ_DN<5>	IN	213C2 B9D7 269C5	
HSV507	1 PE_U1003_MEZZ_DP<6>	IN	213C2 B9D7 269C5	
	2 PE_U1003_MEZZ_DN<6>	IN	213C2 B9D7 269C5	
HSV508	1 PE_U1003_MEZZ_DP<7>	IN	213C2 B9D7 269C5	
	2 PE_U1003_MEZZ_DN<7>	IN	213C2 B9D7 269C5	
HSV509	1 PE_U1003_MEZZ_DP<8>	IN	213C2 B9D7 269C5	
	2 PE_U1003_MEZZ_DN<8>	IN	213C2 B9D7 269C5	
HSV510	1 PE_U1003_MEZZ_DP<9>	IN	213C2 B9D7 269B5	
	2 PE_U1003_MEZZ_DN<9>	IN	213C2 B9D7 269B5	
HSV511	1 PE_U1003_MEZZ_DP<10>	IN	213C2 B9D7 269B5	
	2 PE_U1003_MEZZ_DN<10>	IN	213C2 B9D7 269B5	
HSV512	1 PE_U1003_MEZZ_DP<11>	IN	213C2 B9D7 269B5	
	2 PE_U1003_MEZZ_DN<11>	IN	213C2 B9D7 269B5	
HSV513	1 PE_U1003_MEZZ_DP<12>	IN	213C2 B9D7 269B5	
	2 PE_U1003_MEZZ_DN<12>	IN	213C2 B9D7 269B5	
HSV514	1 PE_U1003_MEZZ_DP<13>	IN	213C2 B9D7 269B5	
	2 PE_U1003_MEZZ_DN<13>	IN	213C2 B9D7 269B5	
HSV515	1 PE_U1003_MEZZ_DP<14>	IN	213C2 B9D7 269A5	
	2 PE_U1003_MEZZ_DN<14>	IN	213C2 B9D7 269A5	
HSV516	1 PE_U1003_MEZZ_DP<15>	IN	213C2 B9D7 269A5	
	2 PE_U1003_MEZZ_DN<15>	IN	213C2 B9D7 269A5	

HSV517	1 PE_U1004_MEZZ_DP<0>	IN	214C2 BBD7 269D3	
	2 PE_U1004_MEZZ_DN<0>	IN	214C2 BBD7 269D3	
HSV518	1 PE_U1004_MEZZ_DP<1>	IN	214C2 BBD7 269D3	
	2 PE_U1004_MEZZ_DN<1>	IN	214C2 BBD7 269D3	
HSV519	1 PE_U1004_MEZZ_DP<2>	IN	214C2 BBD7 269D3	
	2 PE_U1004_MEZZ_DN<2>	IN	214C2 BBD7 269D3	
HSV520	1 PE_U1004_MEZZ_DP<3>	IN	214C2 BBD7 269D3	
	2 PE_U1004_MEZZ_DN<3>	IN	214C2 BBD7 269D3	
HSV521	1 PE_U1004_MEZZ_DP<4>	IN	214C2 BBD7 269C3	
	2 PE_U1004_MEZZ_DN<4>	IN	214C2 BBD7 269C3	
HSV522	1 PE_U1004_MEZZ_DP<5>	IN	214C2 BBD7 269C3	
	2 PE_U1004_MEZZ_DN<5>	IN	214C2 BBD7 269C3	
HSV523	1 PE_U1004_MEZZ_DP<6>	IN	214C2 BBD7 269C3	
	2 PE_U1004_MEZZ_DN<6>	IN	214C2 BBD7 269C3	
HSV524	1 PE_U1004_MEZZ_DP<7>	IN	214C2 BBD7 269C3	
	2 PE_U1004_MEZZ_DN<7>	IN	214C2 BBD7 269C3	
HSV525	1 PE_U1004_MEZZ_DP<8>	IN	214C2 BBD7 269C3	
	2 PE_U1004_MEZZ_DN<8>	IN	214C2 BBD7 269C3	
HSV526	1 PE_U1004_MEZZ_DP<9>	IN	214C2 BBD7 269B3	
	2 PE_U1004_MEZZ_DN<9>	IN	214C2 BBD7 269B3	
HSV527	1 PE_U1004_MEZZ_DP<10>	IN	214C2 BBD7 269B3	
	2 PE_U1004_MEZZ_DN<10>	IN	214C2 BBD7 269B3	
HSV528	1 PE_U1004_MEZZ_DP<11>	IN	214C2 BBD7 269B3	
	2 PE_U1004_MEZZ_DN<11>	IN	214C2 BBD7 269B3	
HSV529	1 PE_U1004_MEZZ_DP<12>	IN	214C2 BBD7 269B3	
	2 PE_U1004_MEZZ_DN<12>	IN	214C2 BBD7 269B3	
HSV530	1 PE_U1004_MEZZ_DP<13>	IN	214C2 BBD7 269B3	
	2 PE_U1004_MEZZ_DN<13>	IN	214C2 BBD7 269B3	
HSV531	1 PE_U1004_MEZZ_DP<14>	IN	214C2 BBD7 269A3	
	2 PE_U1004_MEZZ_DN<14>	IN	214C2 BBD7 269A3	
HSV532	1 PE_U1004_MEZZ_DP<15>	IN	214C2 BBD7 269A3	
	2 PE_U1004_MEZZ_DN<15>	IN	214C2 BBD7 269A3	

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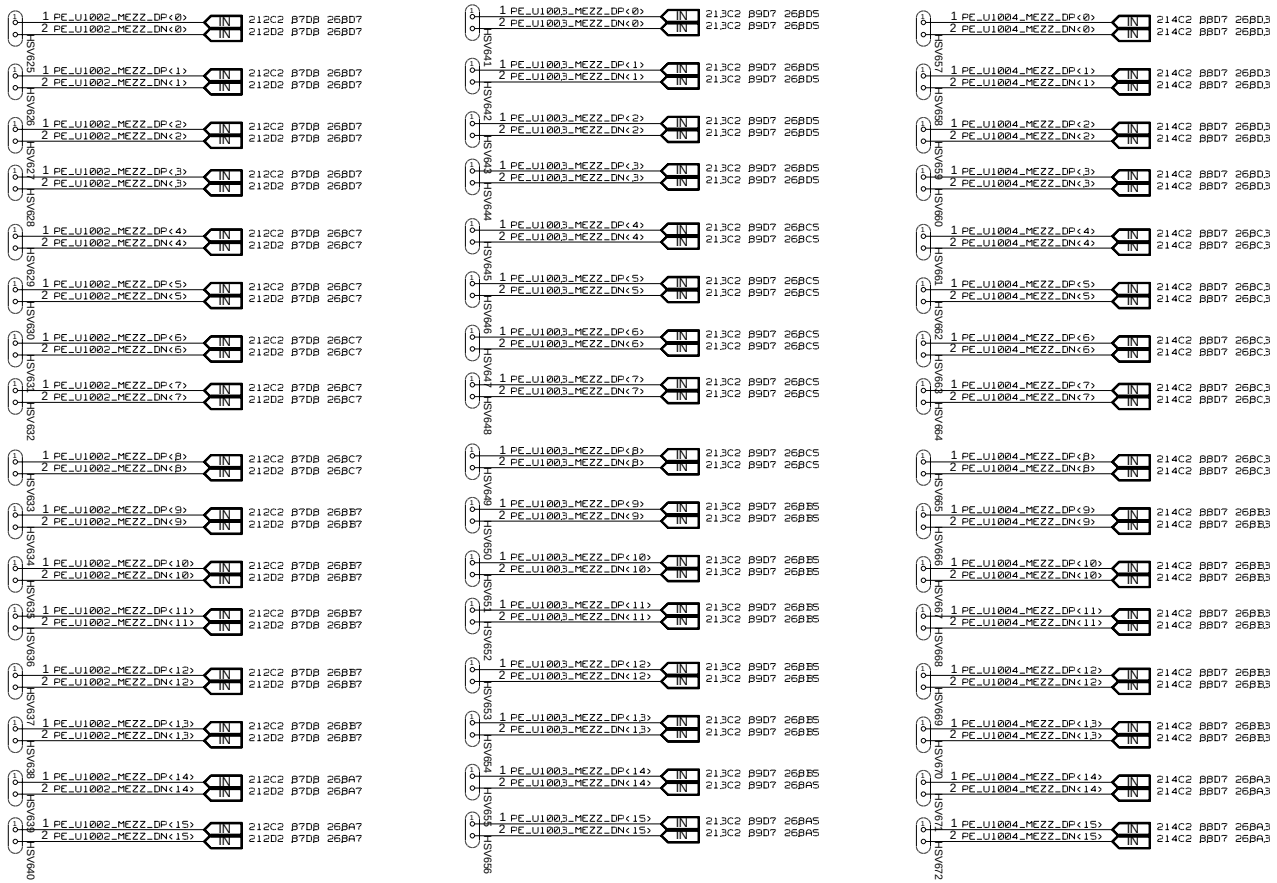
CR-269 : @WOLFCREEK_CONTROLLER_LIB.WOLFCREEK_CONTROLLER(SCH_1):PAGE67,3



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HSV533	1 PE_MEZZ_U1002_DP(0)	87D2 212B2 271D7	
	2 PE_MEZZ_U1002_DN(0)	87C2 212B2 271D7	
HSV534	1 PE_MEZZ_U1002_DP(1)	87D2 212B2 271D7	
	2 PE_MEZZ_U1002_DN(1)	87C2 212B2 271D7	
HSV535	1 PE_MEZZ_U1002_DP(2)	87D2 212B2 271D7	
	2 PE_MEZZ_U1002_DN(2)	87C2 212B2 271D7	
HSV536	1 PE_MEZZ_U1002_DP(3)	87D2 212B2 271D7	
	2 PE_MEZZ_U1002_DN(3)	87C2 212B2 271D7	
HSV537	1 PE_MEZZ_U1002_DP(4)	87D2 212B2 271C7	
	2 PE_MEZZ_U1002_DN(4)	87C2 212B2 271C7	
HSV538	1 PE_MEZZ_U1002_DP(5)	87D2 212B2 271C7	
	2 PE_MEZZ_U1002_DN(5)	87C2 212B2 271C7	
HSV539	1 PE_MEZZ_U1002_DP(6)	87D2 212B2 271C7	
	2 PE_MEZZ_U1002_DN(6)	87C2 212B2 271C7	
HSV540	1 PE_MEZZ_U1002_DP(7)	87D2 212B2 271C7	
	2 PE_MEZZ_U1002_DN(7)	87C2 212B2 271C7	
HSV541	1 PE_MEZZ_U1002_DP(8)	87D2 212B2 271B7	
	2 PE_MEZZ_U1002_DN(8)	87C2 212B2 271B7	
HSV542	1 PE_MEZZ_U1002_DP(9)	87D2 212B2 271B7	
	2 PE_MEZZ_U1002_DN(9)	87C2 212B2 271B7	
HSV543	1 PE_MEZZ_U1002_DP(10)	87D2 212B2 271B7	
	2 PE_MEZZ_U1002_DN(10)	87C2 212B2 271B7	
HSV544	1 PE_MEZZ_U1002_DP(11)	87D2 212B2 271B7	
	2 PE_MEZZ_U1002_DN(11)	87C2 212B2 271B7	
HSV545	1 PE_MEZZ_U1002_DP(12)	87D2 212B2 271A7	
	2 PE_MEZZ_U1002_DN(12)	87C2 212B2 271A7	
HSV546	1 PE_MEZZ_U1002_DP(13)	87D2 212B2 271A7	
	2 PE_MEZZ_U1002_DN(13)	87C2 212B2 271A7	
HSV547	1 PE_MEZZ_U1002_DP(14)	87D2 212B2 271A7	
	2 PE_MEZZ_U1002_DN(14)	87C2 212B2 271A7	
HSV548	1 PE_MEZZ_U1002_DP(15)	87D2 212B2 271A7	
	2 PE_MEZZ_U1002_DN(15)	87C2 212B2 271A7	

HSV549	1 PE_MEZZ_U1003_DP(0)	89D1 213A2 271D5	
	2 PE_MEZZ_U1003_DN(0)	89C1 213B2 271D5	
HSV550	1 PE_MEZZ_U1003_DP(1)	89D1 213A2 271D5	
	2 PE_MEZZ_U1003_DN(1)	89C1 213B2 271D5	
HSV551	1 PE_MEZZ_U1003_DP(2)	89D1 213A2 271D5	
	2 PE_MEZZ_U1003_DN(2)	89C1 213B2 271D5	
HSV552	1 PE_MEZZ_U1003_DP(3)	89D1 213A2 271D5	
	2 PE_MEZZ_U1003_DN(3)	89C1 213B2 271C5	
HSV553	1 PE_MEZZ_U1003_DP(4)	89D1 213A2 271C5	
	2 PE_MEZZ_U1003_DN(4)	89C1 213B2 271C5	
HSV554	1 PE_MEZZ_U1003_DP(5)	89D1 213A2 271C5	
	2 PE_MEZZ_U1003_DN(5)	89C1 213B2 271C5	
HSV555	1 PE_MEZZ_U1003_DP(6)	89D1 213A2 271C5	
	2 PE_MEZZ_U1003_DN(6)	89C1 213B2 271C5	
HSV556	1 PE_MEZZ_U1003_DP(7)	89D1 213A2 271C5	
	2 PE_MEZZ_U1003_DN(7)	89C1 213B2 271C5	
HSV557	1 PE_MEZZ_U1003_DP(8)	89D1 213A2 271B5	
	2 PE_MEZZ_U1003_DN(8)	89C1 213B2 271B5	
HSV558	1 PE_MEZZ_U1003_DP(9)	89D1 213A2 271B5	
	2 PE_MEZZ_U1003_DN(9)	89C1 213B2 271B5	
HSV559	1 PE_MEZZ_U1003_DP(10)	89D1 213A2 271B5	
	2 PE_MEZZ_U1003_DN(10)	89C1 213B2 271B5	
HSV560	1 PE_MEZZ_U1003_DP(11)	89D1 213A2 271B5	
	2 PE_MEZZ_U1003_DN(11)	89C1 213B2 271B5	
HSV561	1 PE_MEZZ_U1003_DP(12)	89D1 213A2 271A5	
	2 PE_MEZZ_U1003_DN(12)	89C1 213B2 271A5	
HSV562	1 PE_MEZZ_U1003_DP(13)	89D1 213A2 271A5	
	2 PE_MEZZ_U1003_DN(13)	89C1 213B2 271A5	
HSV563	1 PE_MEZZ_U1003_DP(14)	89D1 213A2 271A5	
	2 PE_MEZZ_U1003_DN(14)	89C1 213B2 271A5	
HSV564	1 PE_MEZZ_U1003_DP(15)	89D1 213A2 271A5	
	2 PE_MEZZ_U1003_DN(15)	89C1 213B2 271A5	

HSV565	1 PE_MEZZ_U1004_DP(0)	8BD1 214B2 271D3	
	2 PE_MEZZ_U1004_DN(0)	8BC1 214B2 271D3	
HSV566	1 PE_MEZZ_U1004_DP(1)	8BD1 214B2 271D3	
	2 PE_MEZZ_U1004_DN(1)	8BC1 214B2 271D3	
HSV567	1 PE_MEZZ_U1004_DP(2)	8BD1 214B2 271D3	
	2 PE_MEZZ_U1004_DN(2)	8BC1 214B2 271D3	
HSV568	1 PE_MEZZ_U1004_DP(3)	8BD1 214B2 271D3	
	2 PE_MEZZ_U1004_DN(3)	8BC1 214B2 271D3	
HSV569	1 PE_MEZZ_U1004_DP(4)	8BD1 214B2 271C3	
	2 PE_MEZZ_U1004_DN(4)	8BC1 214B2 271C3	
HSV570	1 PE_MEZZ_U1004_DP(5)	8BD1 214B2 271C3	
	2 PE_MEZZ_U1004_DN(5)	8BC1 214B2 271C3	
HSV571	1 PE_MEZZ_U1004_DP(6)	8BD1 214B2 271C3	
	2 PE_MEZZ_U1004_DN(6)	8BC1 214B2 271C3	
HSV572	1 PE_MEZZ_U1004_DP(7)	8BD1 214B2 271C3	
	2 PE_MEZZ_U1004_DN(7)	8BC1 214B2 271C3	
HSV573	1 PE_MEZZ_U1004_DP(8)	8BD1 214B2 271B3	
	2 PE_MEZZ_U1004_DN(8)	8BC1 214B2 271B3	
HSV574	1 PE_MEZZ_U1004_DP(9)	8BD1 214B2 271B3	
	2 PE_MEZZ_U1004_DN(9)	8BC1 214B2 271B3	
HSV575	1 PE_MEZZ_U1004_DP(10)	8BD1 214B2 271B3	
	2 PE_MEZZ_U1004_DN(10)	8BC1 214B2 271B3	
HSV576	1 PE_MEZZ_U1004_DP(11)	8BD1 214B2 271B3	
	2 PE_MEZZ_U1004_DN(11)	8BC1 214B2 271B3	
HSV577	1 PE_MEZZ_U1004_DP(12)	8BD1 214B2 271A3	
	2 PE_MEZZ_U1004_DN(12)	8BC1 214B2 271A3	
HSV285	1 PE_MEZZ_U1004_DP(13)	8BD1 214B2 271A3	
	2 PE_MEZZ_U1004_DN(13)	8BC1 214B2 271A3	
HSV286	1 PE_MEZZ_U1004_DP(14)	8BD1 214B2 271A3	
	2 PE_MEZZ_U1004_DN(14)	8BC1 214B2 271A3	
HSV287	1 PE_MEZZ_U1004_DP(15)	8BD1 214B2 271A3	
	2 PE_MEZZ_U1004_DN(15)	8BC1 214B2 271A3	

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HASWELL SOCKET 0 (3 OF 14)
wolfcreek_controller
wolfcreek_controller.cpm

DATE: Fri Aug 08 19:40:35 2014
DRAWN BY: <ENGINEER>
DWG NO: <DRAWING>
REV: <REVISION>
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

HSV289	1 PE_MEZZ_U1002_DP<0>	IN	B7D2 212B2 270D7	HSV592	1 PE_MEZZ_U1003_DP<0>	IN	B9D1 213A2 270D5
	2 PE_MEZZ_U1002_DN<0>	IN	B7C2 212B2 270D7		2 PE_MEZZ_U1003_DN<0>	IN	B9C1 213B2 270D5
HSV290	1 PE_MEZZ_U1002_DP<1>	IN	B7D2 212B2 270D7	HSV593	1 PE_MEZZ_U1003_DP<1>	IN	B9D1 213A2 270D5
	2 PE_MEZZ_U1002_DN<1>	IN	B7C2 212B2 270D7		2 PE_MEZZ_U1003_DN<1>	IN	B9C1 213B2 270D5
HSV578	1 PE_MEZZ_U1002_DP<2>	IN	B7D2 212B2 270D7	HSV594	1 PE_MEZZ_U1003_DP<2>	IN	B9D1 213A2 270D5
	2 PE_MEZZ_U1002_DN<2>	IN	B7C2 212B2 270D7		2 PE_MEZZ_U1003_DN<2>	IN	B9C1 213B2 270D5
HSV579	1 PE_MEZZ_U1002_DP<3>	IN	B7D2 212B2 270D7	HSV595	1 PE_MEZZ_U1003_DP<3>	IN	B9D1 213A2 270D5
	2 PE_MEZZ_U1002_DN<3>	IN	B7C2 212B2 270D7		2 PE_MEZZ_U1003_DN<3>	IN	B9C1 213B2 270D5
HSV580	1 PE_MEZZ_U1002_DP<4>	IN	B7D2 212B2 270C7	HSV596	1 PE_MEZZ_U1003_DP<4>	IN	B9D1 213A2 270C5
	2 PE_MEZZ_U1002_DN<4>	IN	B7C2 212B2 270C7		2 PE_MEZZ_U1003_DN<4>	IN	B9C1 213B2 270C5
HSV581	1 PE_MEZZ_U1002_DP<5>	IN	B7D2 212B2 270C7	HSV597	1 PE_MEZZ_U1003_DP<5>	IN	B9D1 213A2 270C5
	2 PE_MEZZ_U1002_DN<5>	IN	B7C2 212B2 270C7		2 PE_MEZZ_U1003_DN<5>	IN	B9C1 213B2 270C5
HSV582	1 PE_MEZZ_U1002_DP<6>	IN	B7D2 212B2 270C7	HSV598	1 PE_MEZZ_U1003_DP<6>	IN	B9D1 213A2 270C5
	2 PE_MEZZ_U1002_DN<6>	IN	B7C2 212B2 270C7		2 PE_MEZZ_U1003_DN<6>	IN	B9C1 213B2 270C5
HSV583	1 PE_MEZZ_U1002_DP<7>	IN	B7D2 212B2 270C7	HSV599	1 PE_MEZZ_U1003_DP<7>	IN	B9D1 213A2 270C5
	2 PE_MEZZ_U1002_DN<7>	IN	B7C2 212B2 270C7		2 PE_MEZZ_U1003_DN<7>	IN	B9C1 213B2 270C5
HSV584	1 PE_MEZZ_U1002_DP<8>	IN	B7D2 212B2 270B7	HSV600	1 PE_MEZZ_U1003_DP<8>	IN	B9D1 213A2 270B5
	2 PE_MEZZ_U1002_DN<8>	IN	B7C2 212B2 270B7		2 PE_MEZZ_U1003_DN<8>	IN	B9C1 213B2 270B5
HSV585	1 PE_MEZZ_U1002_DP<9>	IN	B7D2 212B2 270B7	HSV601	1 PE_MEZZ_U1003_DP<9>	IN	B9D1 213A2 270B5
	2 PE_MEZZ_U1002_DN<9>	IN	B7C2 212B2 270B7		2 PE_MEZZ_U1003_DN<9>	IN	B9C1 213B2 270B5
HSV586	1 PE_MEZZ_U1002_DP<10>	IN	B7D2 212B2 270B7	HSV602	1 PE_MEZZ_U1003_DP<10>	IN	B9D1 213A2 270B5
	2 PE_MEZZ_U1002_DN<10>	IN	B7C2 212B2 270B7		2 PE_MEZZ_U1003_DN<10>	IN	B9C1 213B2 270B5
HSV587	1 PE_MEZZ_U1002_DP<11>	IN	B7D2 212B2 270B7	HSV603	1 PE_MEZZ_U1003_DP<11>	IN	B9D1 213A2 270B5
	2 PE_MEZZ_U1002_DN<11>	IN	B7C2 212B2 270B7		2 PE_MEZZ_U1003_DN<11>	IN	B9C1 213B2 270B5
HSV588	1 PE_MEZZ_U1002_DP<12>	IN	B7D2 212B2 270A7	HSV604	1 PE_MEZZ_U1003_DP<12>	IN	B9D1 213A2 270A5
	2 PE_MEZZ_U1002_DN<12>	IN	B7C2 212B2 270A7		2 PE_MEZZ_U1003_DN<12>	IN	B9C1 213B2 270A5
HSV589	1 PE_MEZZ_U1002_DP<13>	IN	B7D2 212B2 270A7	HSV605	1 PE_MEZZ_U1003_DP<13>	IN	B9D1 213A2 270A5
	2 PE_MEZZ_U1002_DN<13>	IN	B7C2 212B2 270A7		2 PE_MEZZ_U1003_DN<13>	IN	B9C1 213B2 270A5
HSV590	1 PE_MEZZ_U1002_DP<14>	IN	B7D2 212B2 270A7	HSV606	1 PE_MEZZ_U1003_DP<14>	IN	B9D1 213A2 270A5
	2 PE_MEZZ_U1002_DN<14>	IN	B7C2 212B2 270A7		2 PE_MEZZ_U1003_DN<14>	IN	B9C1 213B2 270A5
HSV591	1 PE_MEZZ_U1002_DP<15>	IN	B7D2 212B2 270A7	HSV607	1 PE_MEZZ_U1003_DP<15>	IN	B9D1 213A2 270A5
	2 PE_MEZZ_U1002_DN<15>	IN	B7C2 212B2 270A7		2 PE_MEZZ_U1003_DN<15>	IN	B9C1 213B2 270A5

HSV618	1 PE_MEZZ_U1004_DP<0>	IN	BBD1 214B2 270D2	HSV288	1 PE_MEZZ_U1004_DP<15>	IN	BBD1 214B2 270A2
	2 PE_MEZZ_U1004_DN<0>	IN	BBC1 214B2 270D2		2 PE_MEZZ_U1004_DN<15>	IN	BBC1 214B2 270A2
HSV608	1 PE_MEZZ_U1004_DP<1>	IN	BBD1 214B2 270D2				
	2 PE_MEZZ_U1004_DN<1>	IN	BBC1 214B2 270D2				
HSV609	1 PE_MEZZ_U1004_DP<2>	IN	BBD1 214B2 270D2				
	2 PE_MEZZ_U1004_DN<2>	IN	BBC1 214B2 270D2				
HSV610	1 PE_MEZZ_U1004_DP<3>	IN	BBD1 214B2 270D2				
	2 PE_MEZZ_U1004_DN<3>	IN	BBC1 214B2 270D2				
HSV611	1 PE_MEZZ_U1004_DP<4>	IN	BBD1 214B2 270C2				
	2 PE_MEZZ_U1004_DN<4>	IN	BBC1 214B2 270C2				
HSV612	1 PE_MEZZ_U1004_DP<5>	IN	BBD1 214B2 270C2				
	2 PE_MEZZ_U1004_DN<5>	IN	BBC1 214B2 270C2				
HSV613	1 PE_MEZZ_U1004_DP<6>	IN	BBD1 214B2 270C2				
	2 PE_MEZZ_U1004_DN<6>	IN	BBC1 214B2 270C2				
HSV614	1 PE_MEZZ_U1004_DP<7>	IN	BBD1 214B2 270C2				
	2 PE_MEZZ_U1004_DN<7>	IN	BBC1 214B2 270C2				
HSV615	1 PE_MEZZ_U1004_DP<8>	IN	BBD1 214B2 270B2				
	2 PE_MEZZ_U1004_DN<8>	IN	BBC1 214B2 270B2				
HSV620	1 PE_MEZZ_U1004_DP<9>	IN	BBD1 214B2 270B2				
	2 PE_MEZZ_U1004_DN<9>	IN	BBC1 214B2 270B2				
HSV616	1 PE_MEZZ_U1004_DP<10>	IN	BBD1 214B2 270B2				
	2 PE_MEZZ_U1004_DN<10>	IN	BBC1 214B2 270B2				
HSV617	1 PE_MEZZ_U1004_DP<11>	IN	BBD1 214B2 270B2				
	2 PE_MEZZ_U1004_DN<11>	IN	BBC1 214B2 270B2				
HSV621	1 PE_MEZZ_U1004_DP<12>	IN	BBD1 214B2 270A2				
	2 PE_MEZZ_U1004_DN<12>	IN	BBC1 214B2 270A2				
HSV622	1 PE_MEZZ_U1004_DP<13>	IN	BBD1 214B2 270A2				
	2 PE_MEZZ_U1004_DN<13>	IN	BBC1 214B2 270A2				
	1 PE_MEZZ_U1004_DP<14>	IN	BBD1 214B2 270A2				
	2 PE_MEZZ_U1004_DN<14>	IN	BBC1 214B2 270A2				

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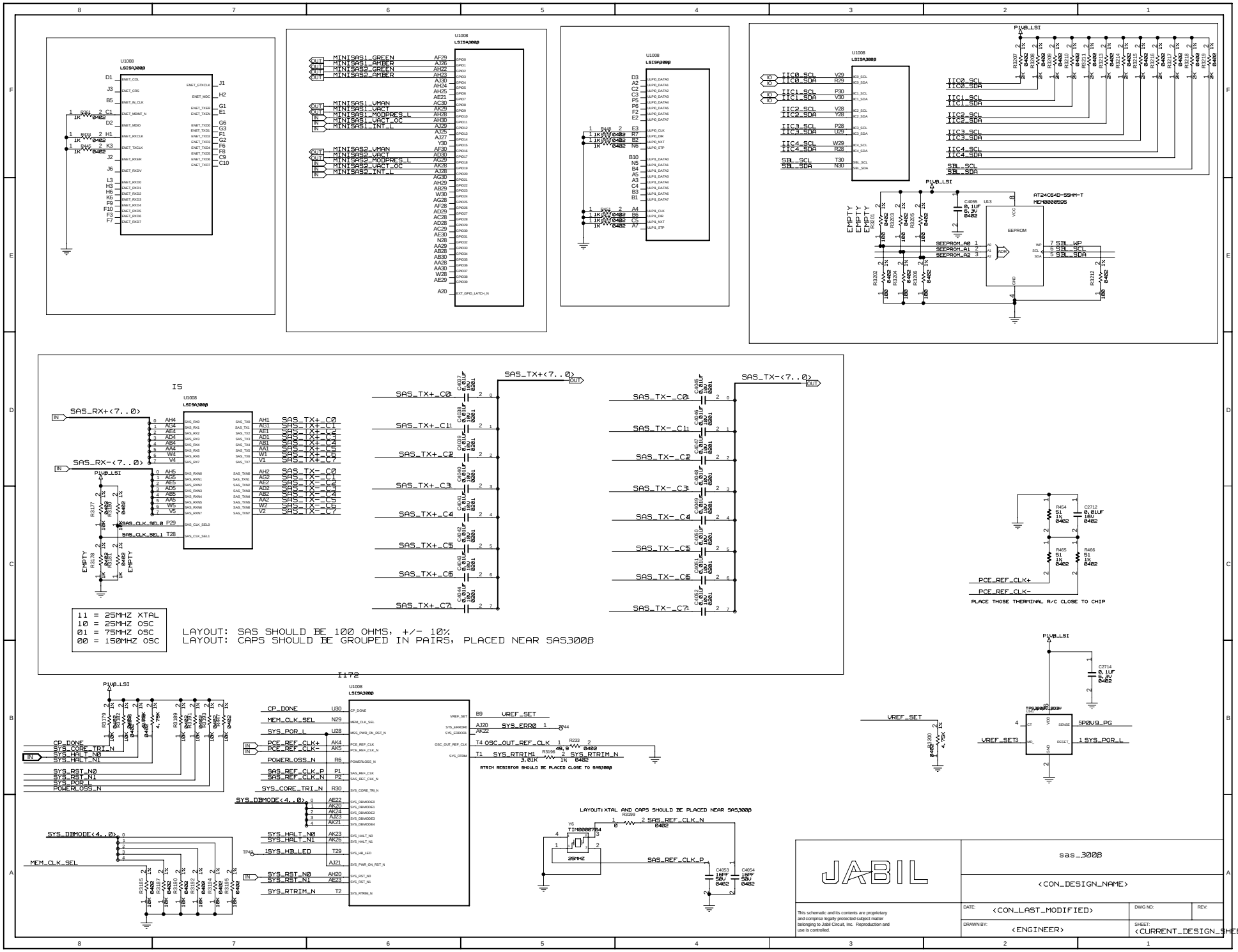
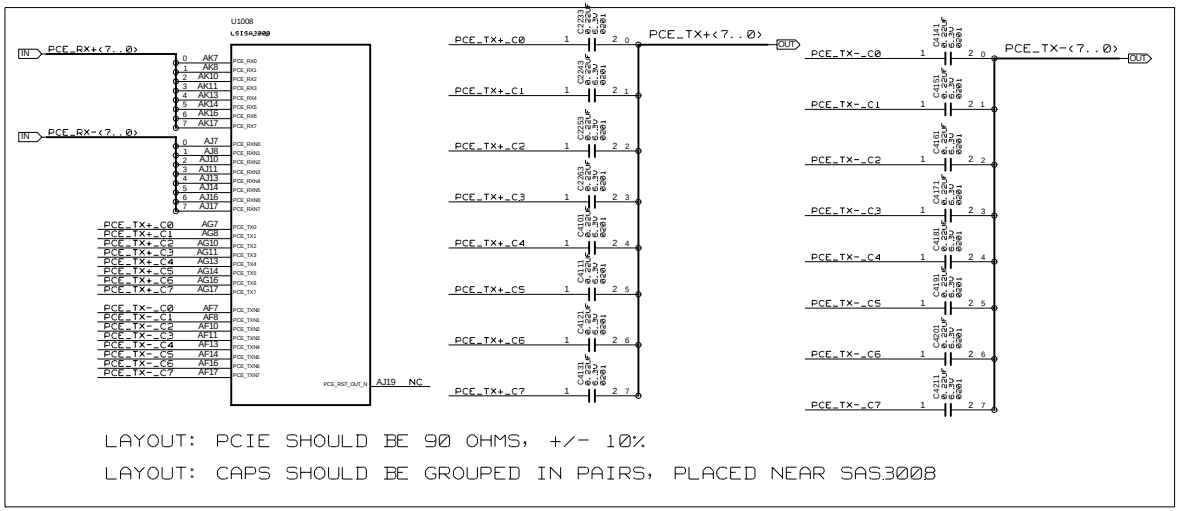
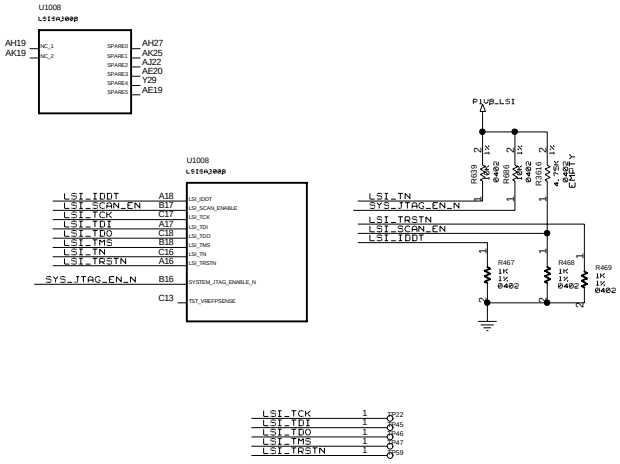
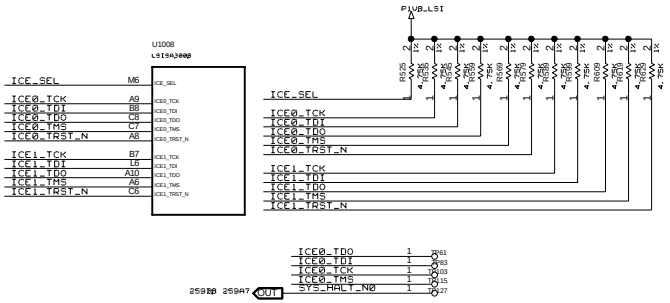
HASWELL SOCKET wolfcreek_controller	DATE: Fri Aug 08 19:40:47 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



DO WE NEED TO CONNECT TESTMUX?







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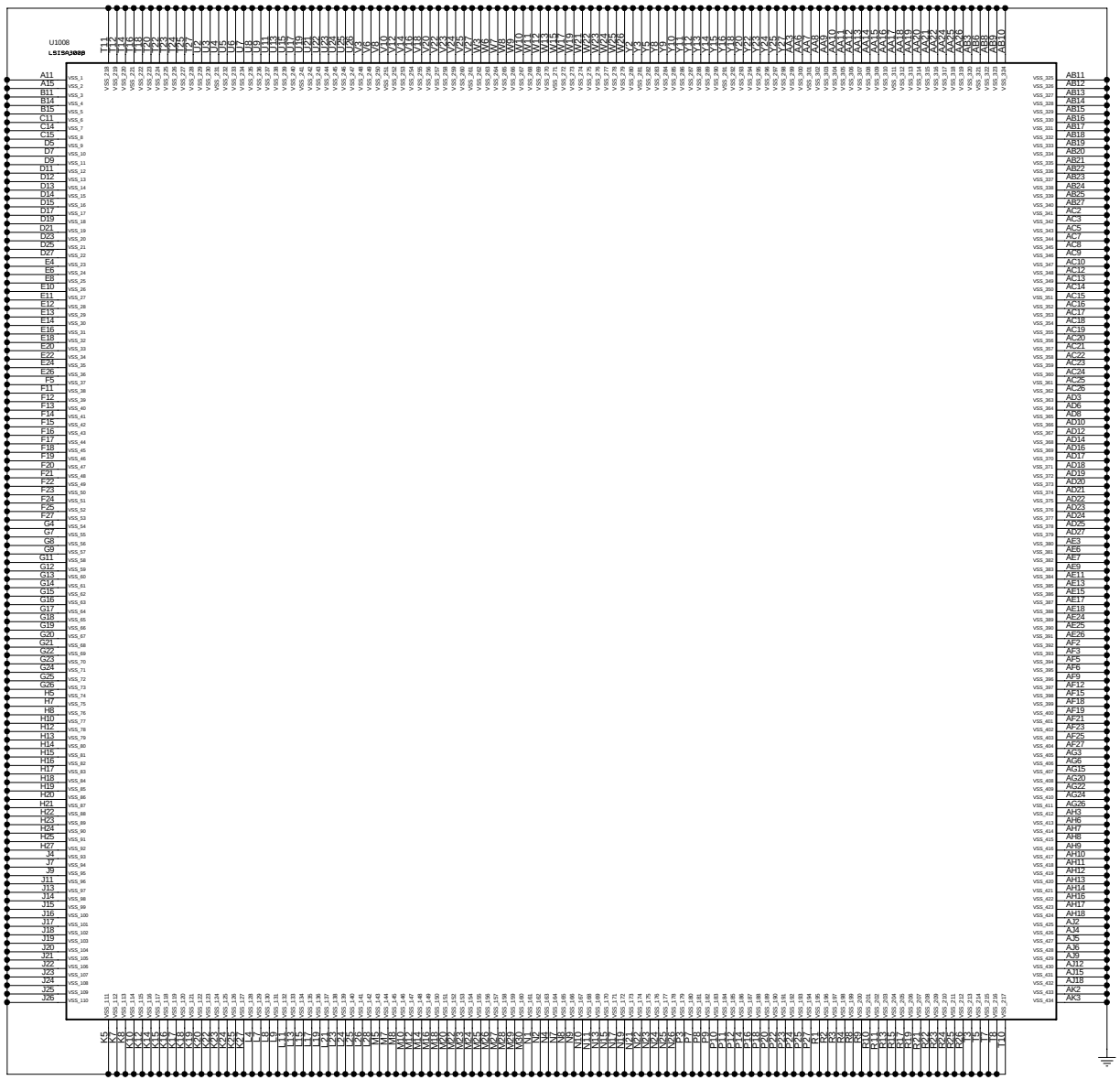
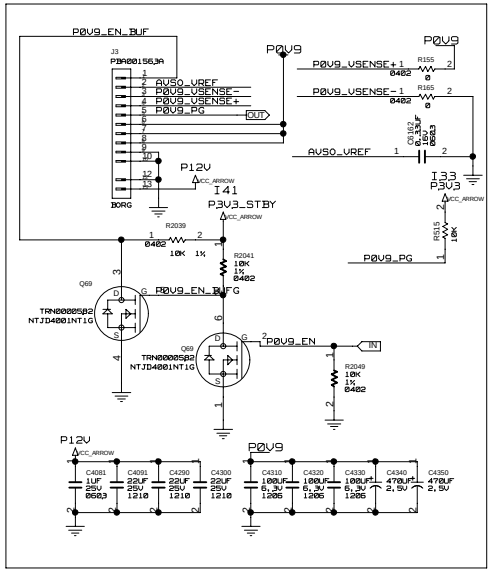
	DRAWN BY: <ENGINEER> SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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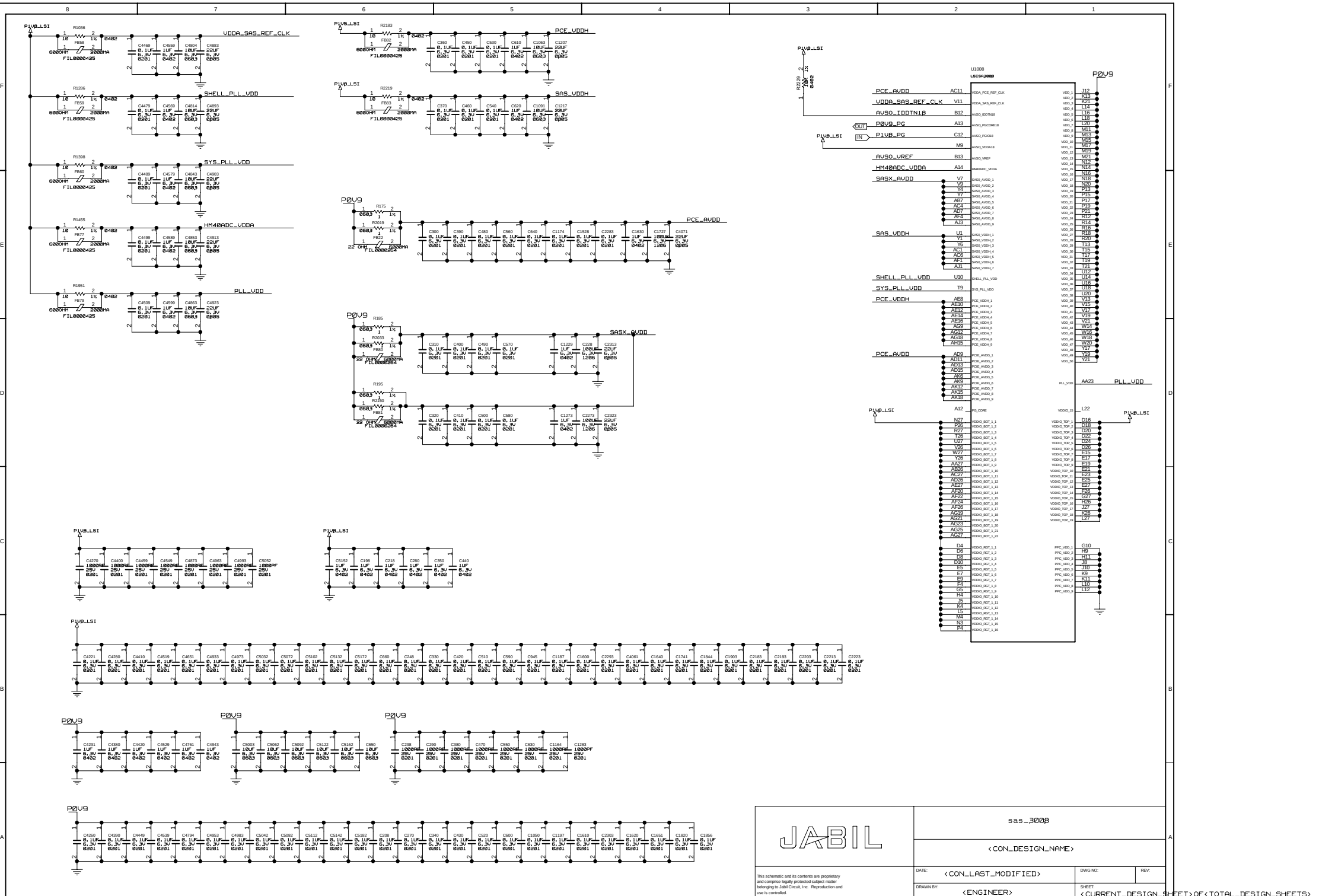
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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<CON_DESIGN_NAME>

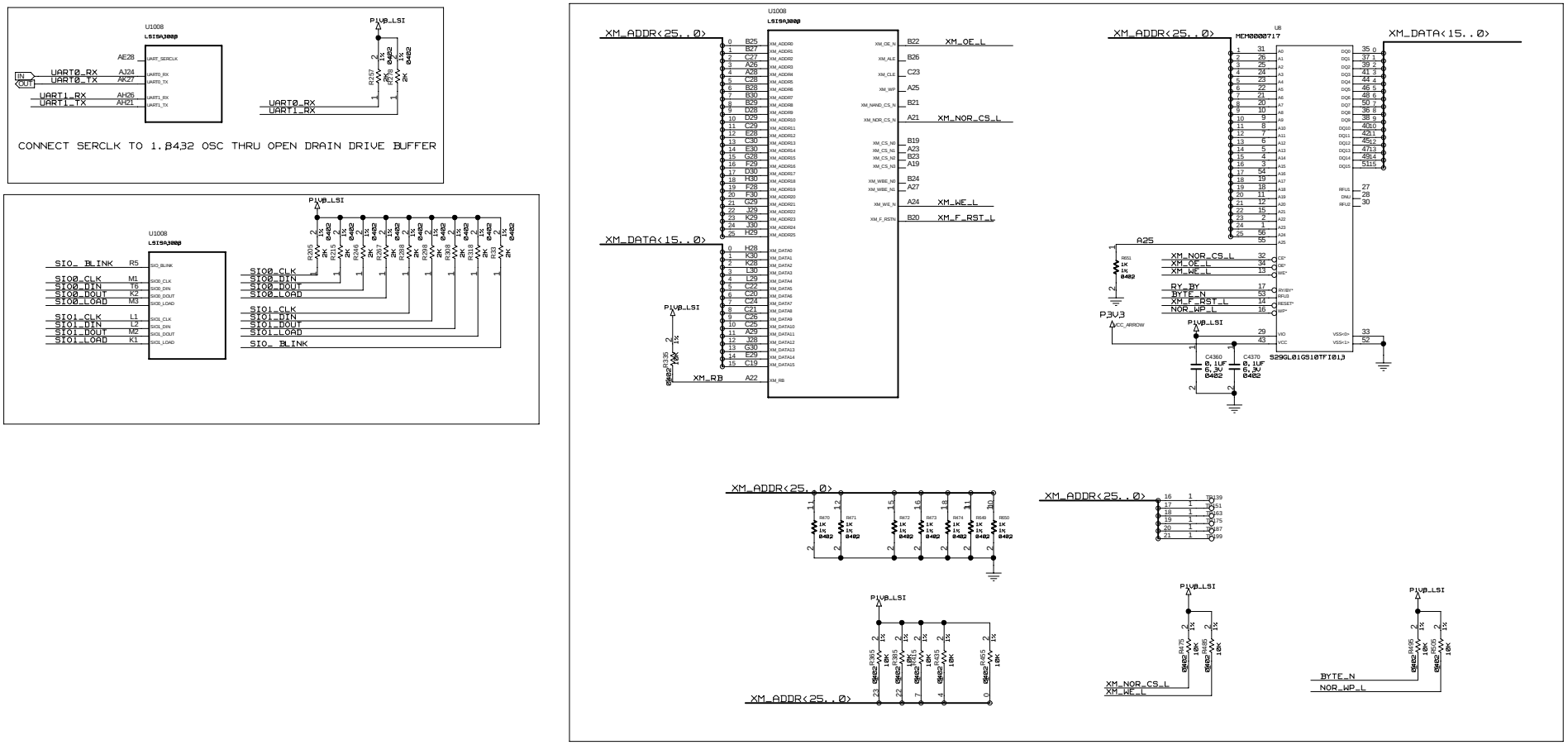
DATE: <CON_LAST_MODIFIED>

DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



POWER-ON SENSE OPTIONS:

XM_ADDR[0]: SERIAL BOOTSTRAP LOADER ENABLE
  0: DISABLED
  1: ENABLED *

XM_ADDR[1]: SERIAL BOOTSTRAP ROM ADDRESS SELECT
  0: 0XA0 *
  1: 0XAB

XM_ADDR[2]: SERIAL BOOTSTRAP ROM BYTE ADDRESS SELECT
  0: START AT BYTE ADDRESS *
  1: START AT BYTE ADDRESS + 8'H80

XM_ADDR[4]: FUSION MESSAGE UNIT MDE
  0: I20 MODE
  1: FUSION MODE (MPT MODE) *

XM_ADDR[6:5]: PCIE MAXIMUM LINK SPEED
  00: 2.5G *
  01: 5.0G
  10: 8.0G
  11: RESERVED

XM_ADDR[7]: RESERVED FOR FUTURE USED. PULL HIGH

XM_ADDR[8]: RESERVED FOR FUTURE USED. PULL LOW

XM_ADDR[11]: DISABLE PCIE LANE 7 TO 4
  0: ENABLED *
  1: DISABLED AND POWERD DOWN

XM_ADDR[23:16]: AVSO MODE
  11XXXXXX: PASS VALUE FROM E-FUSE WITHOUT ADJUSTMENT *

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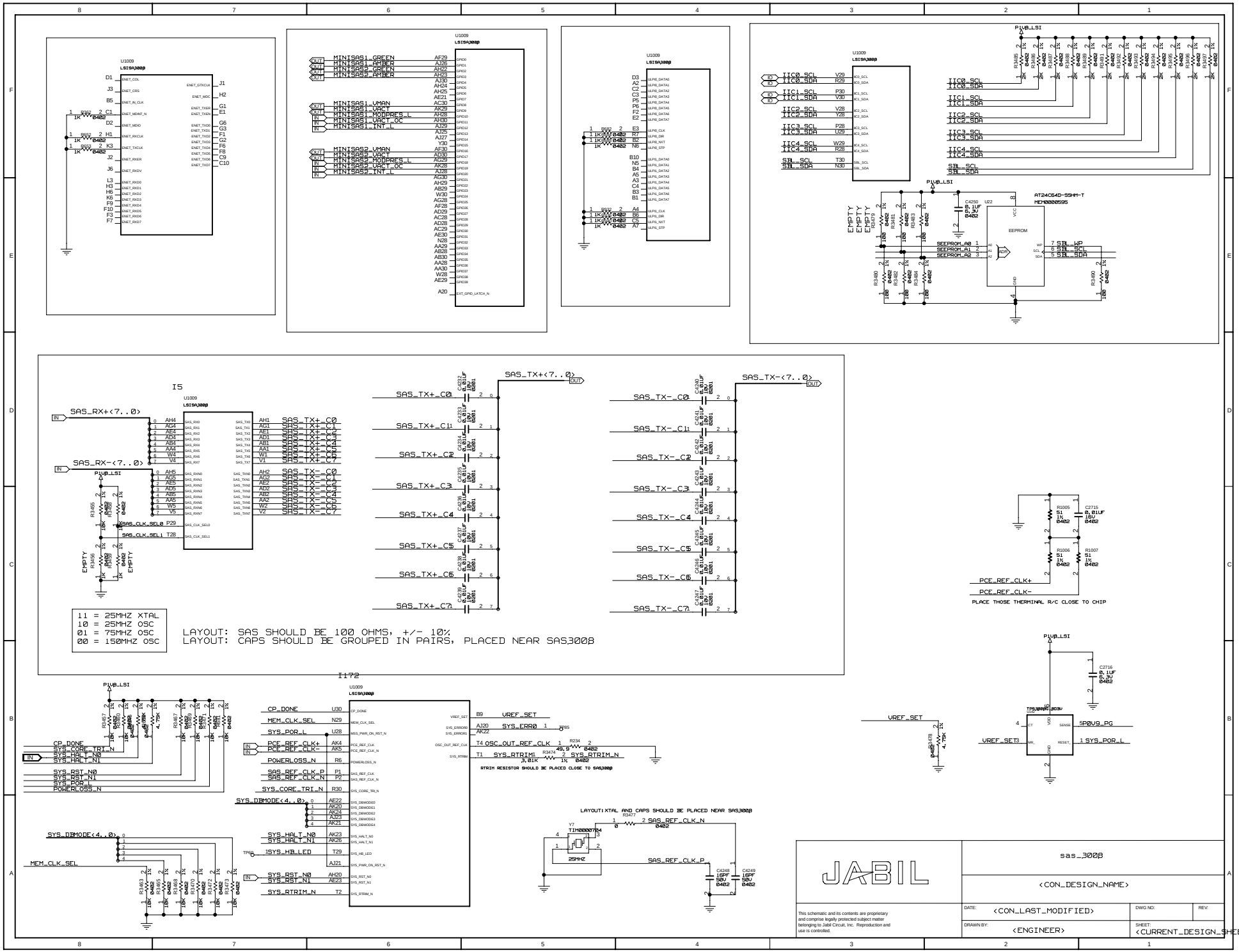
DWG NO:

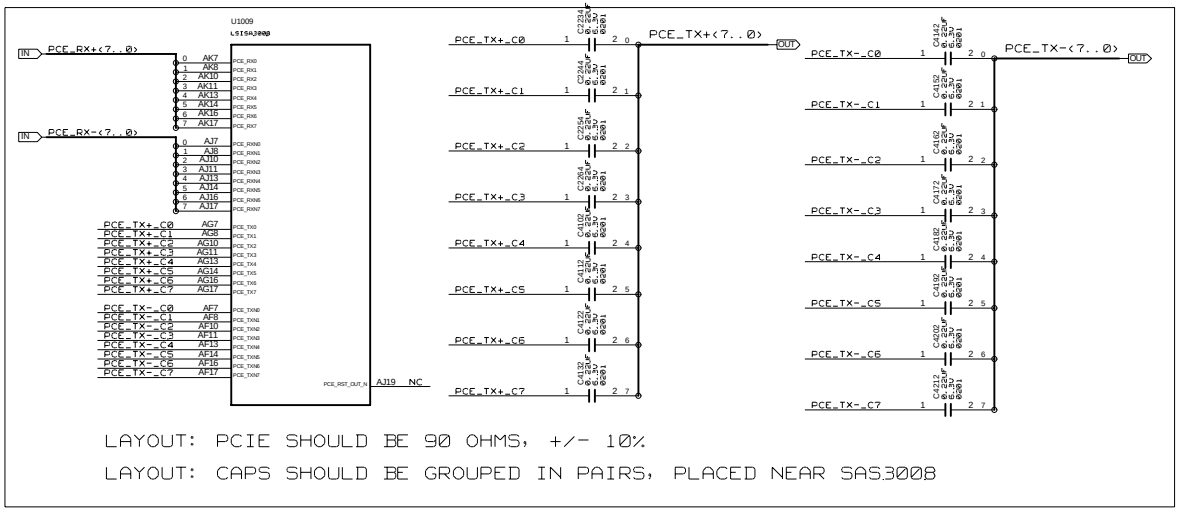
REV:

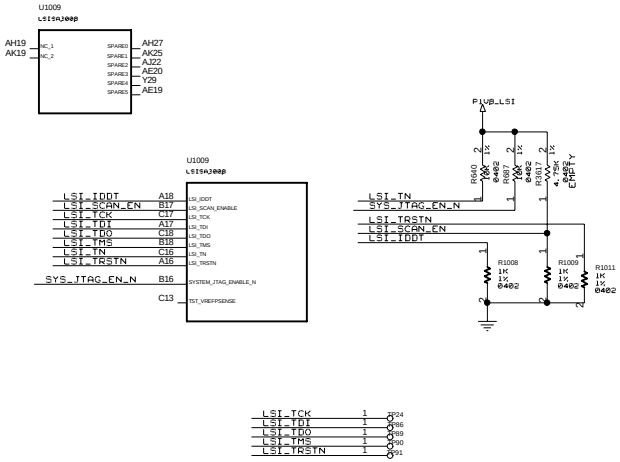
DRAWN BY: <ENGINEER>

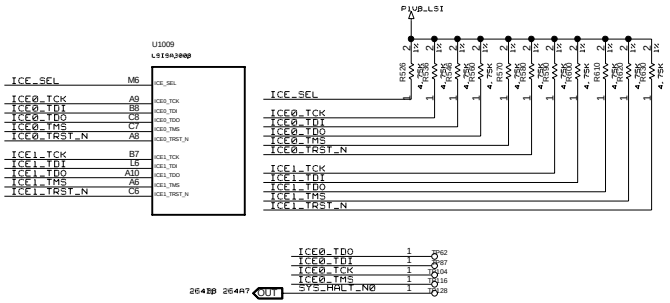
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



DO WE NEED TO CONNECT TESTMUX?







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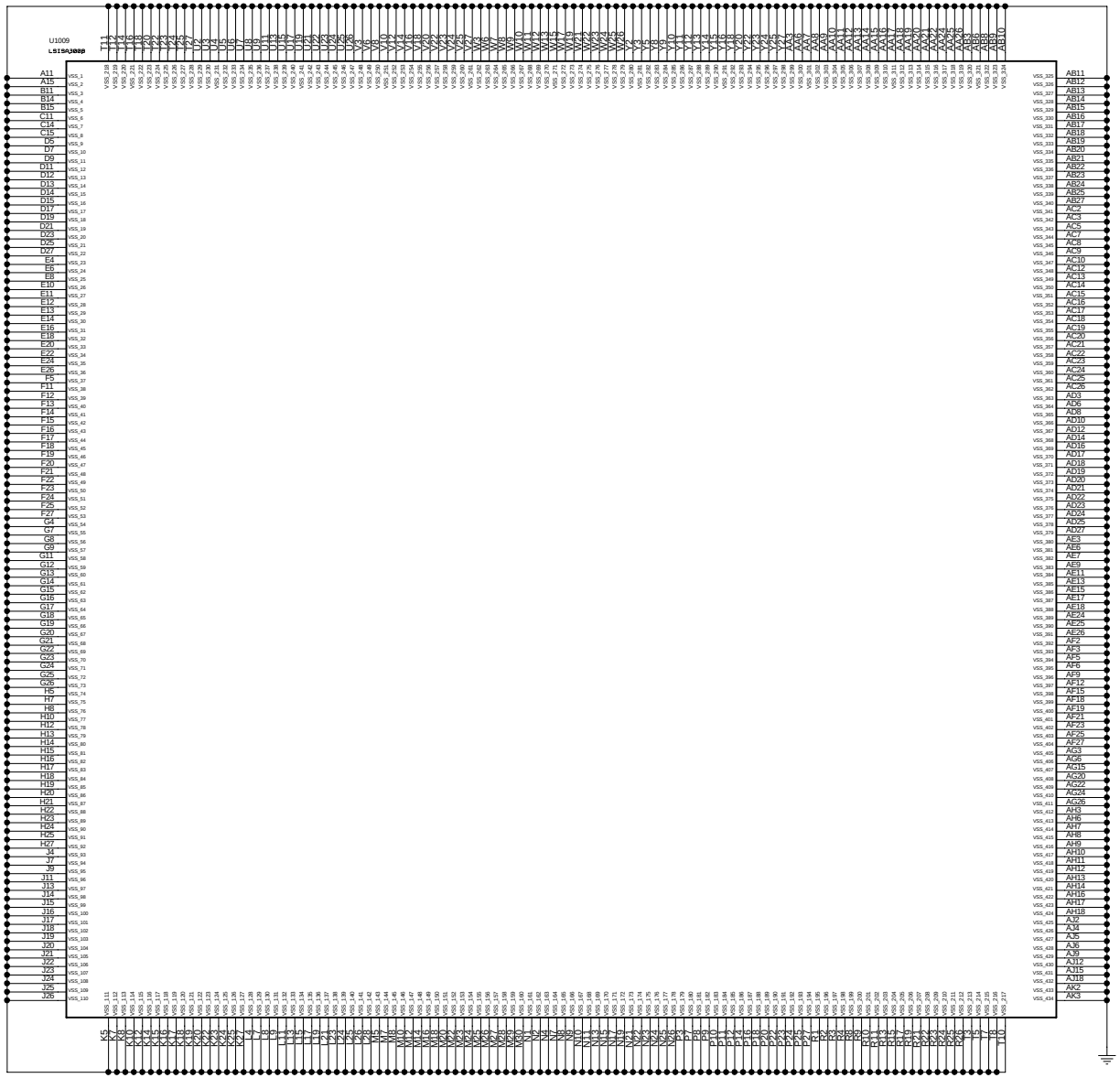
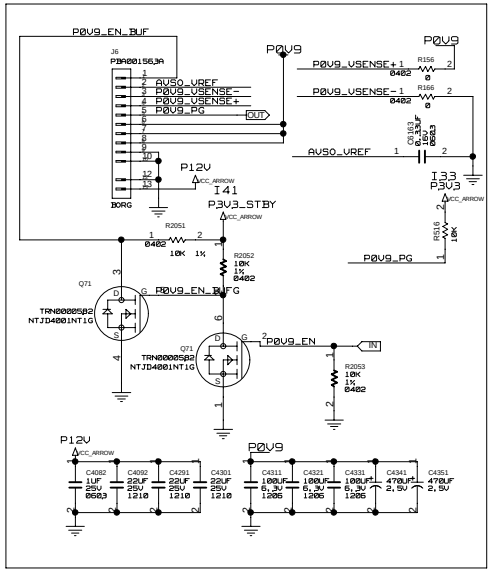
	DRAWN BY: <ENGINEER> / SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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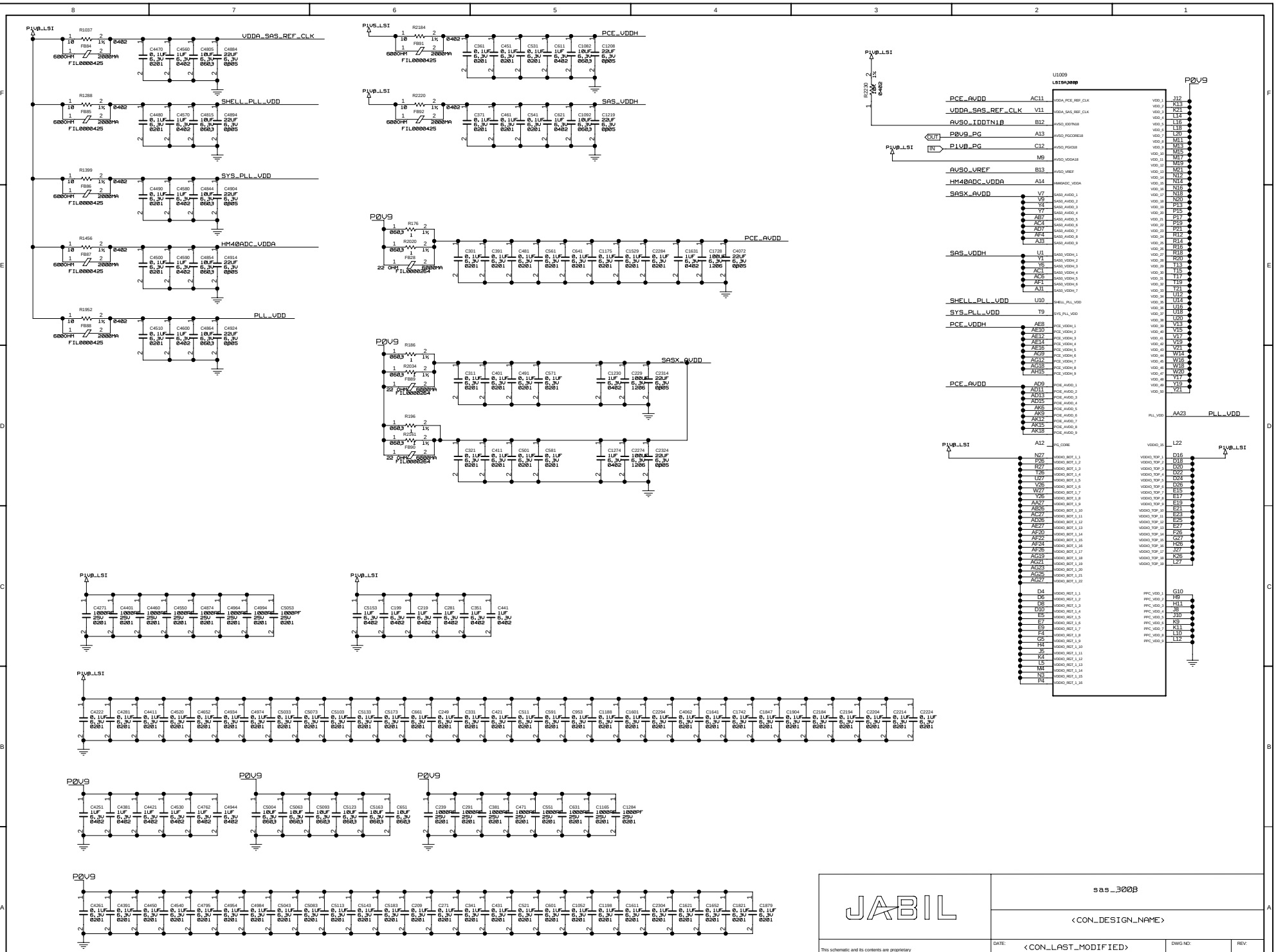
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:
DRAWN BY: <ENGINEER>	REV:
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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<CON_DESIGN_NAME>

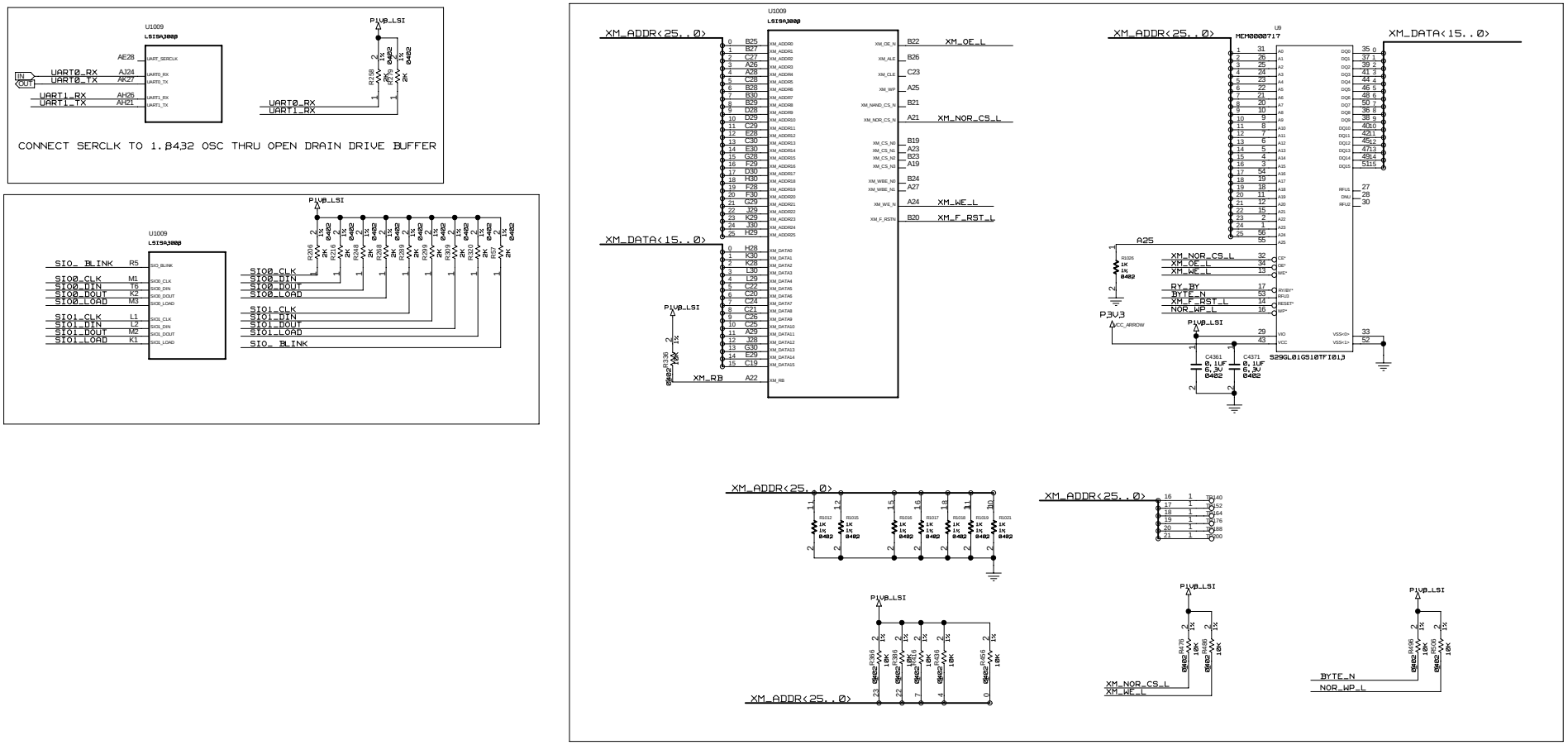
DATE: <CON_LAST_MODIFIED>

DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



POWER-ON SENSE OPTIONS:

XM_ADDR[0]: SERIAL BOOTSTRAP LOADER ENABLE
  0: DISABLED
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  0: 0XA0 *
  1: 0XAB

XM_ADDR[2]: SERIAL BOOTSTRAP ROM BYTE ADDRESS SELECT
  0: START AT BYTE ADDRESS *
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XM_ADDR[4]: FUSION MESSAGE UNIT MDE
  0: I20 MODE
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  00: 2.5G *
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XM_ADDR[8]: RESERVED FOR FUTURE USED. PULL LOW

XM_ADDR[11]: DISABLE PCIE LANE 7 TO 4
  0: ENABLED *
  1: DISABLED AND POWERD DOWN

XM_ADDR[23:16]: AVSO MODE
  11XXXXXX: PASS VALUE FROM E-FUSE WITHOUT ADJUSTMENT *

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<CON_DESIGN_NAME>

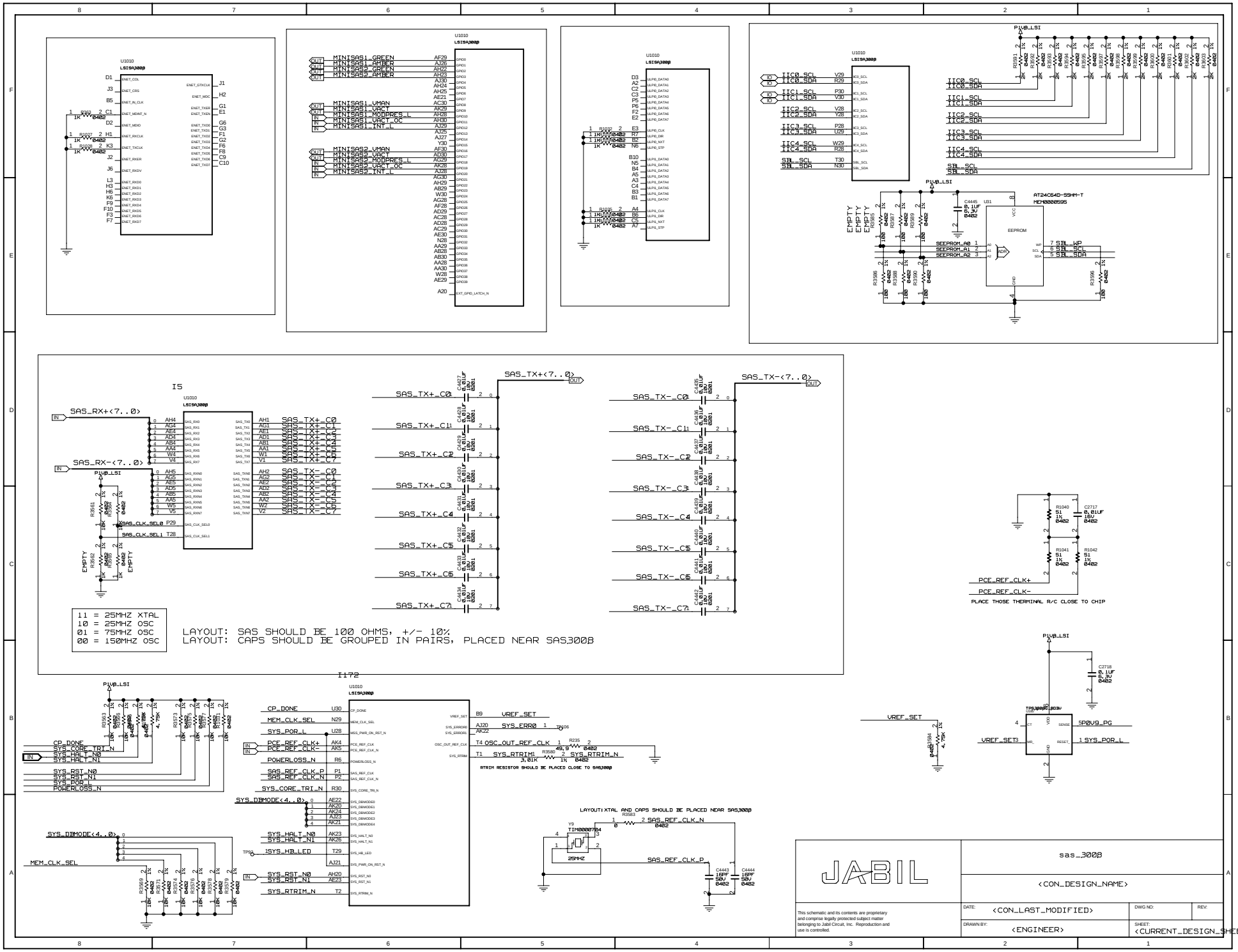
DATE: <CON_LAST_MODIFIED>

DWG NO:

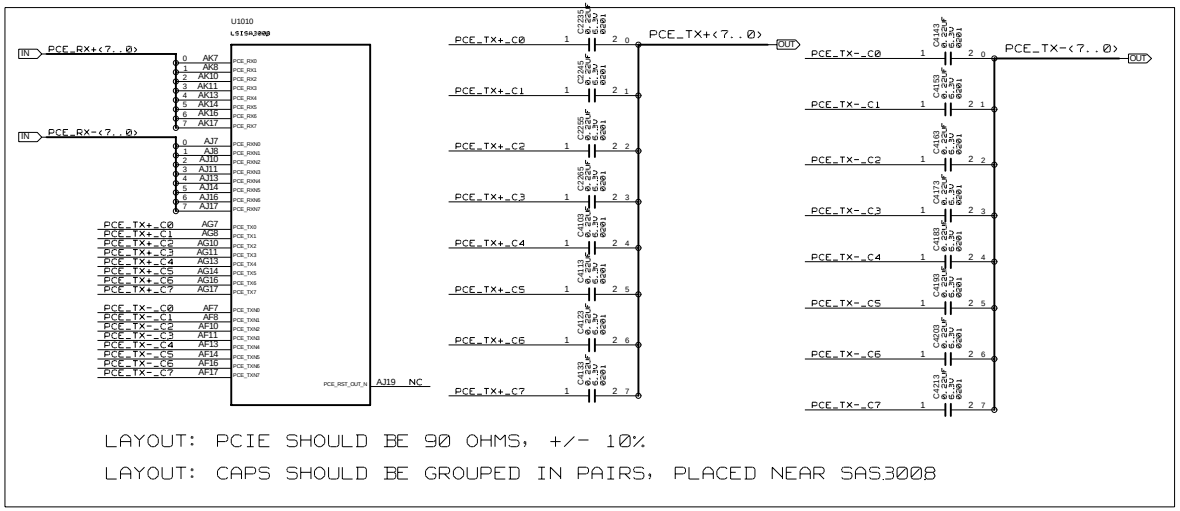
REV:

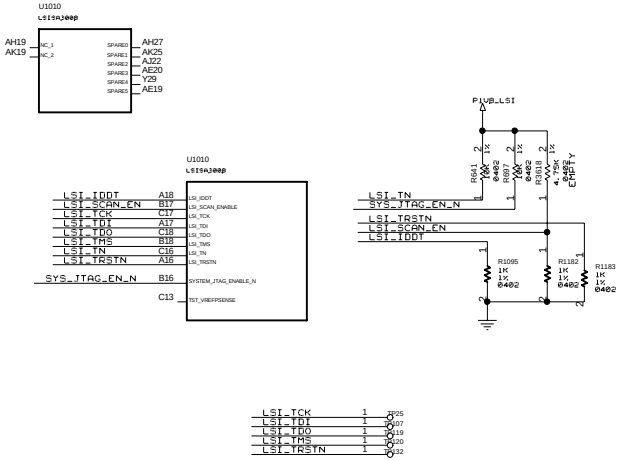
DRAWN BY: <ENGINEER>

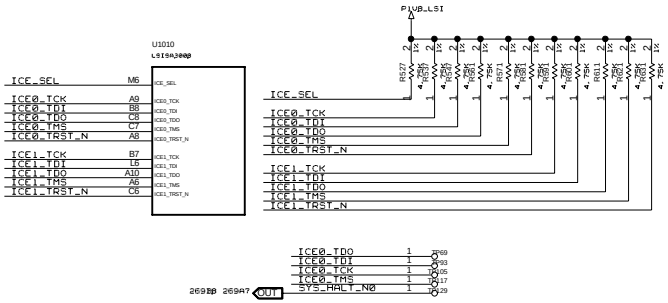
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



DO WE NEED TO CONNECT TESTMUX?







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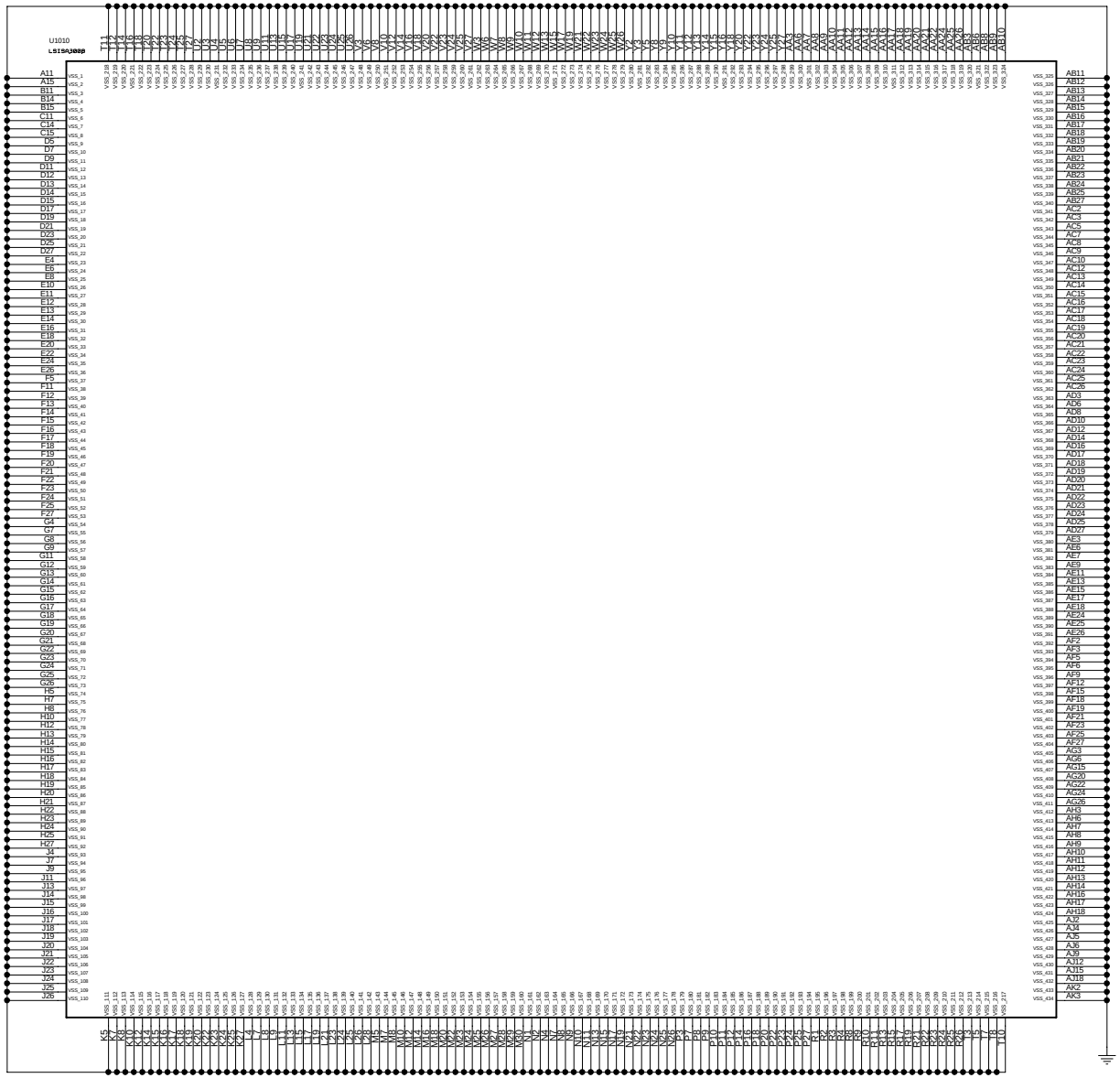
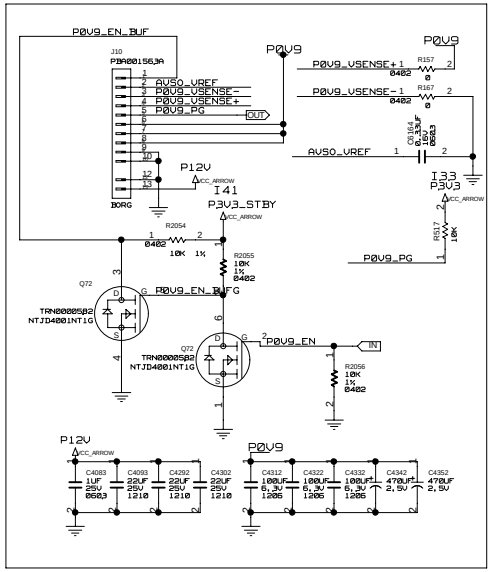
	DRAWN BY: <ENGINEER> / SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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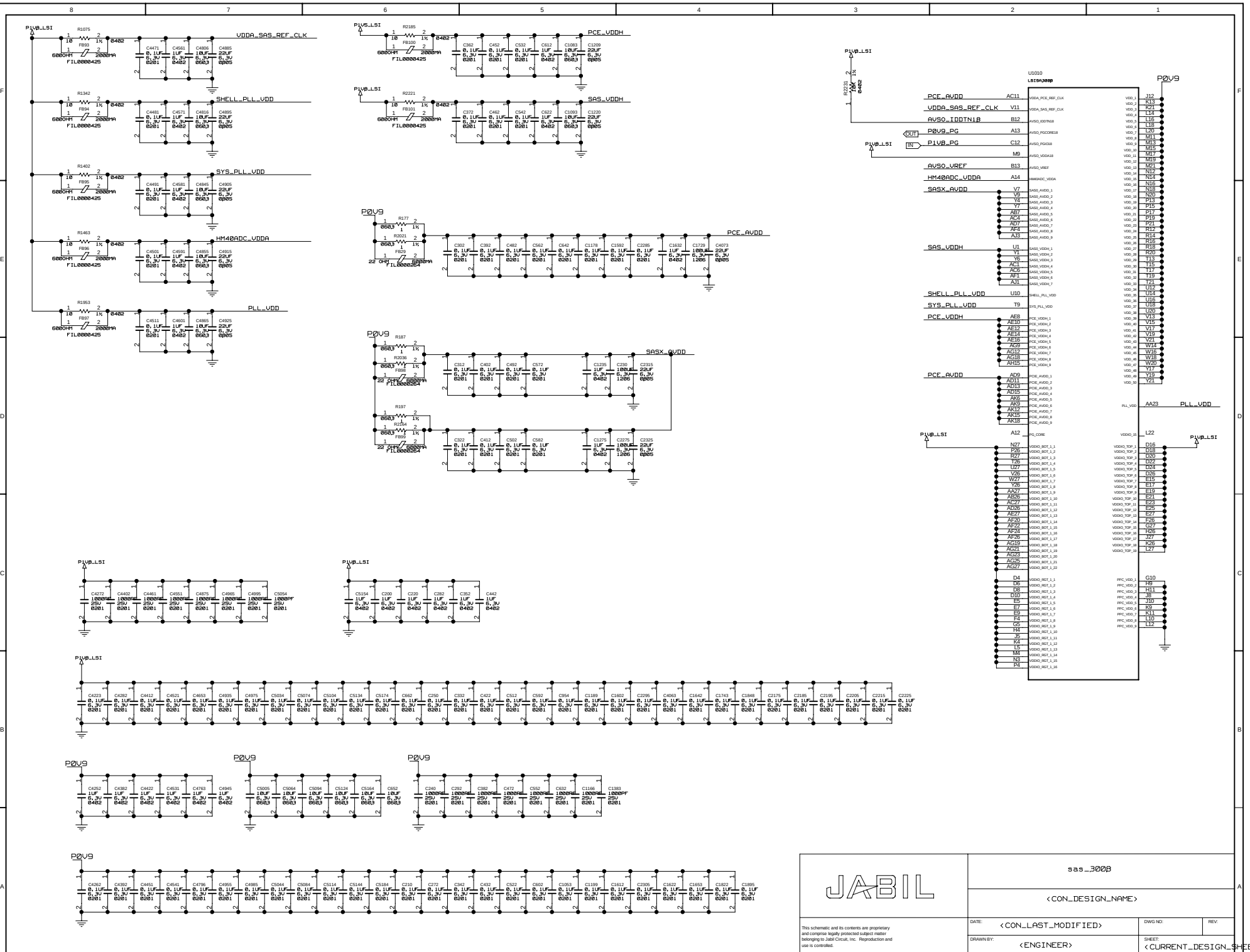
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:
	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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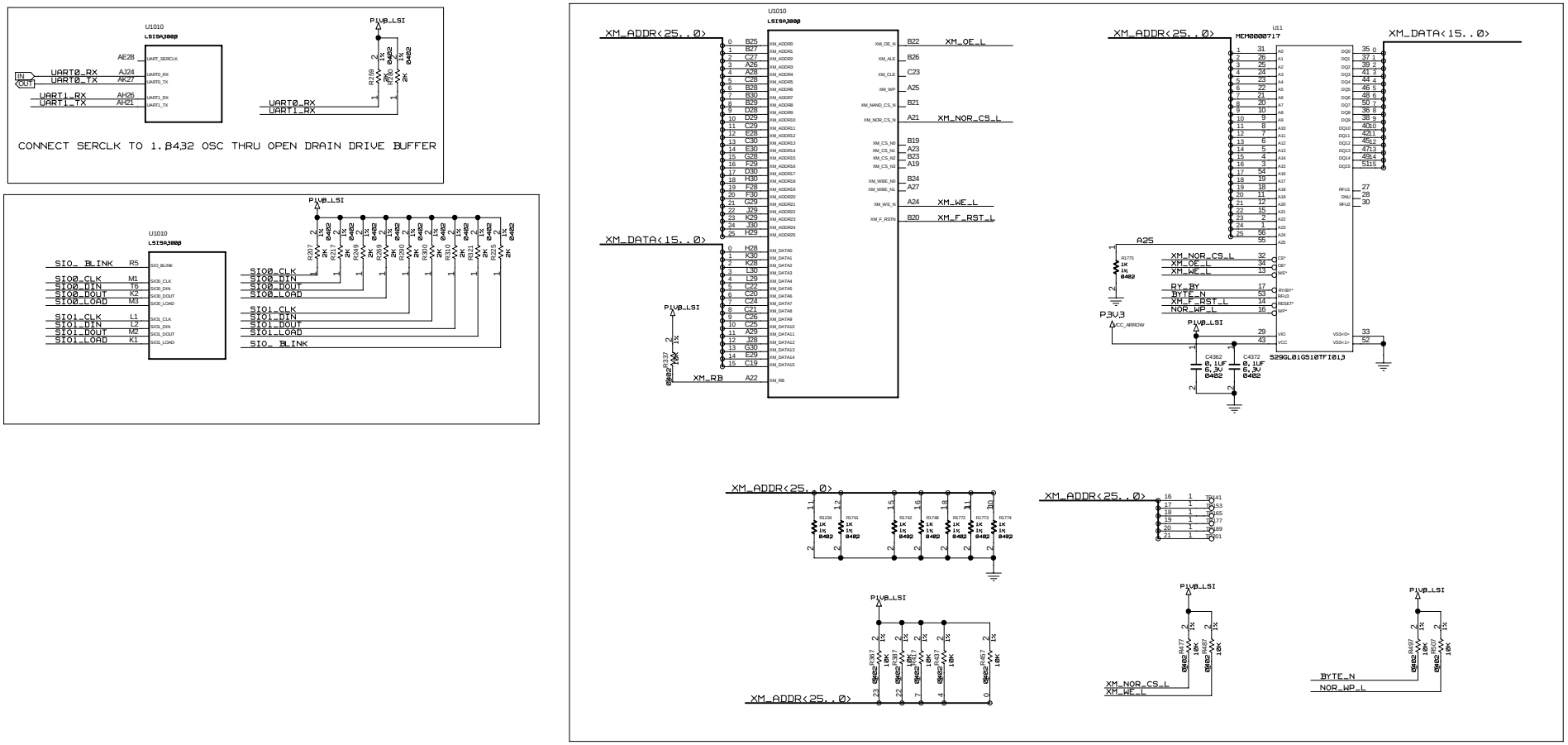
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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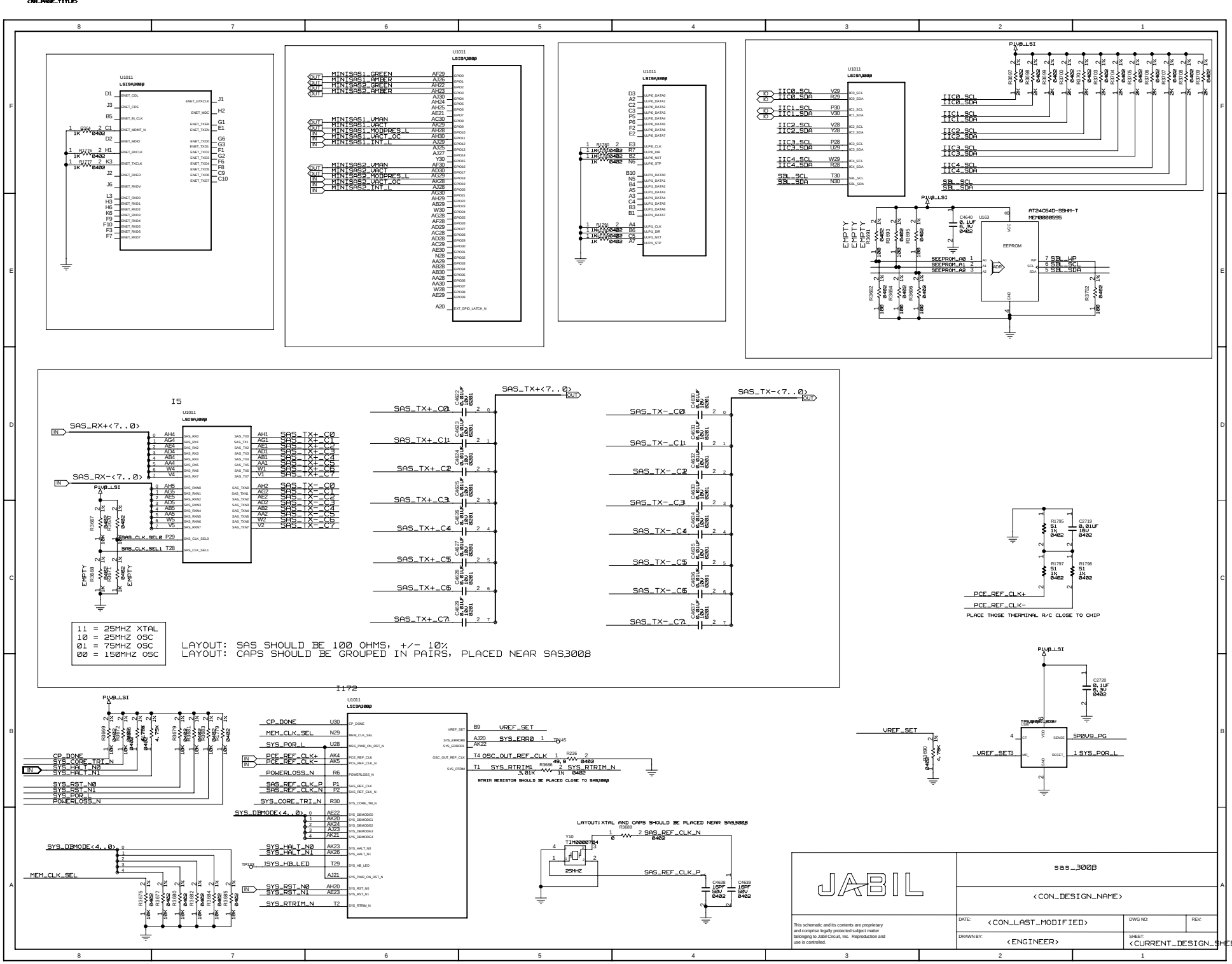
DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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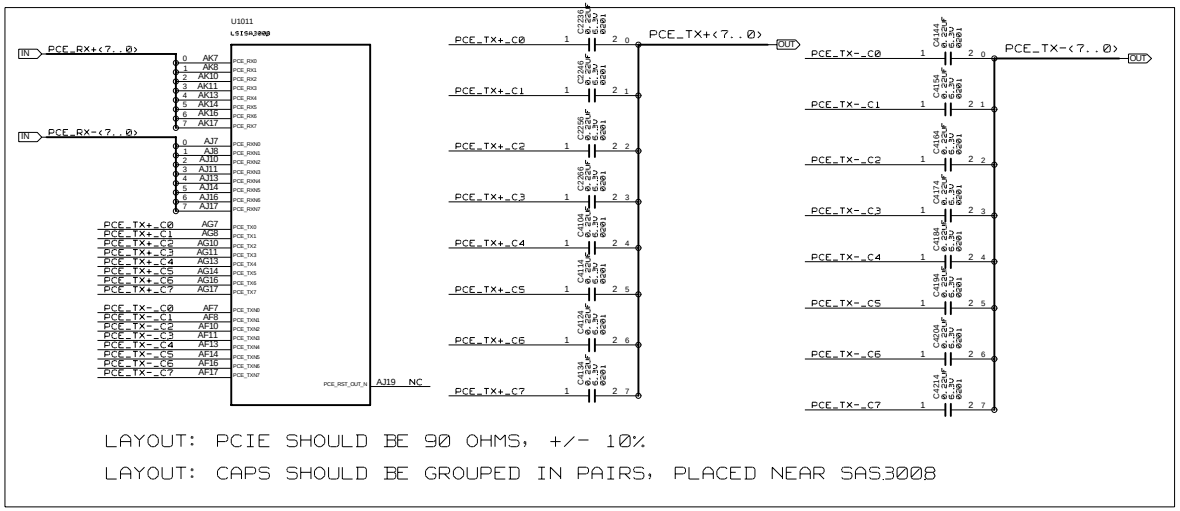

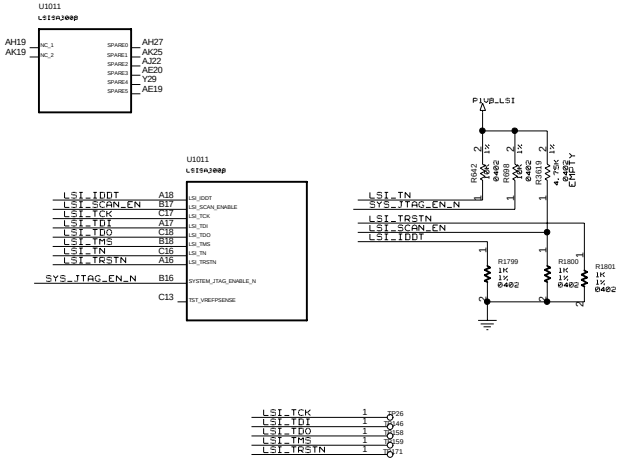

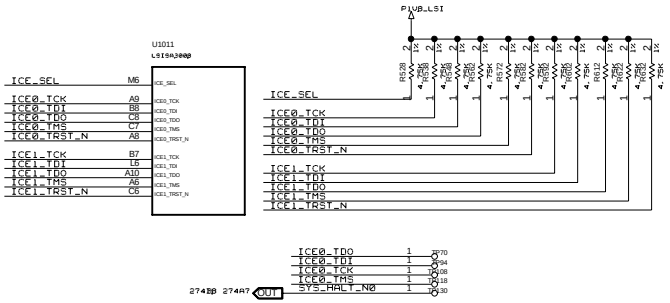

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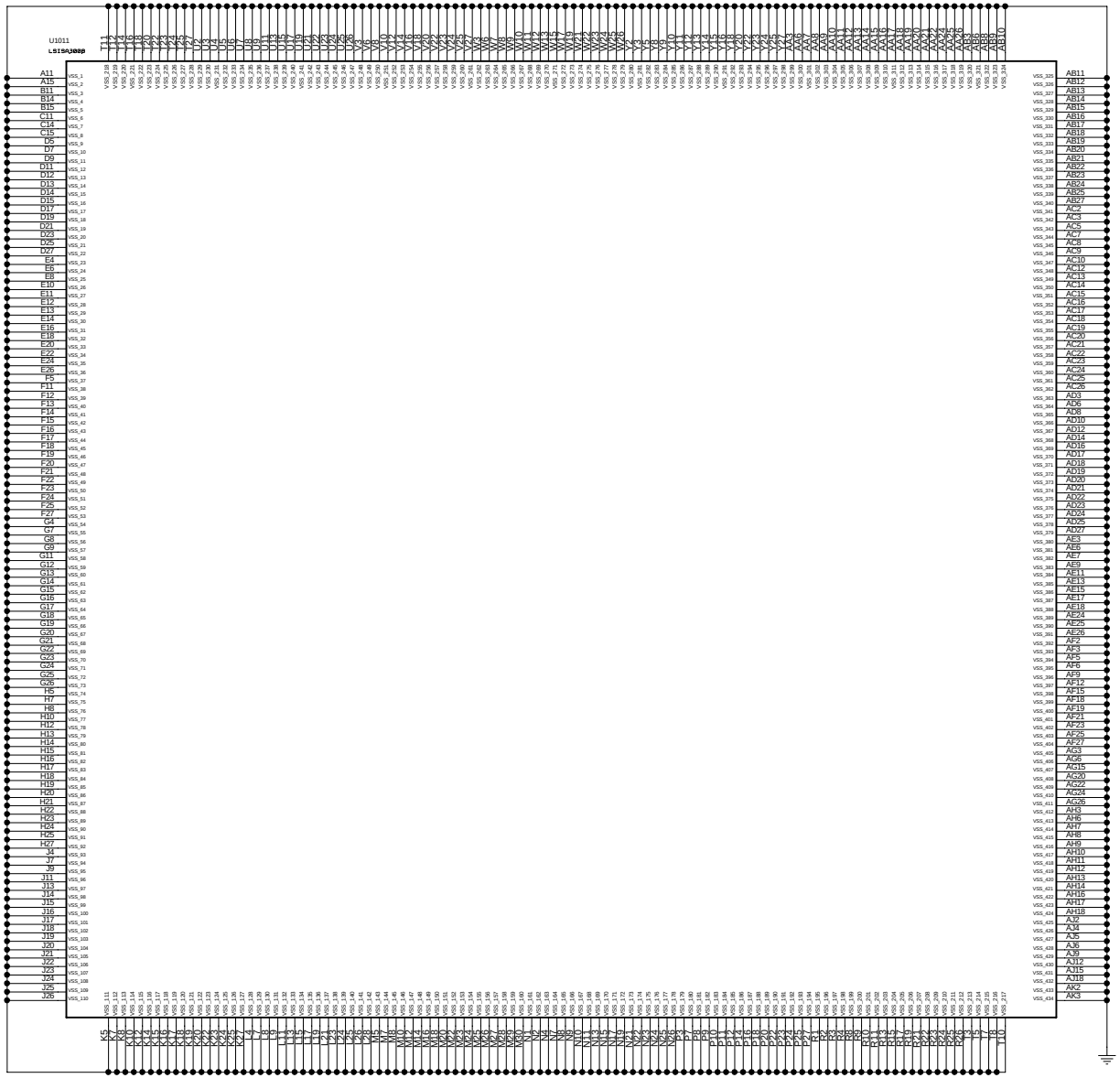
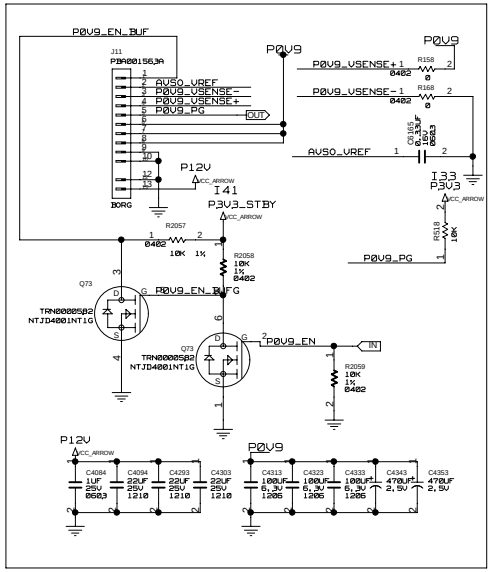
	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	





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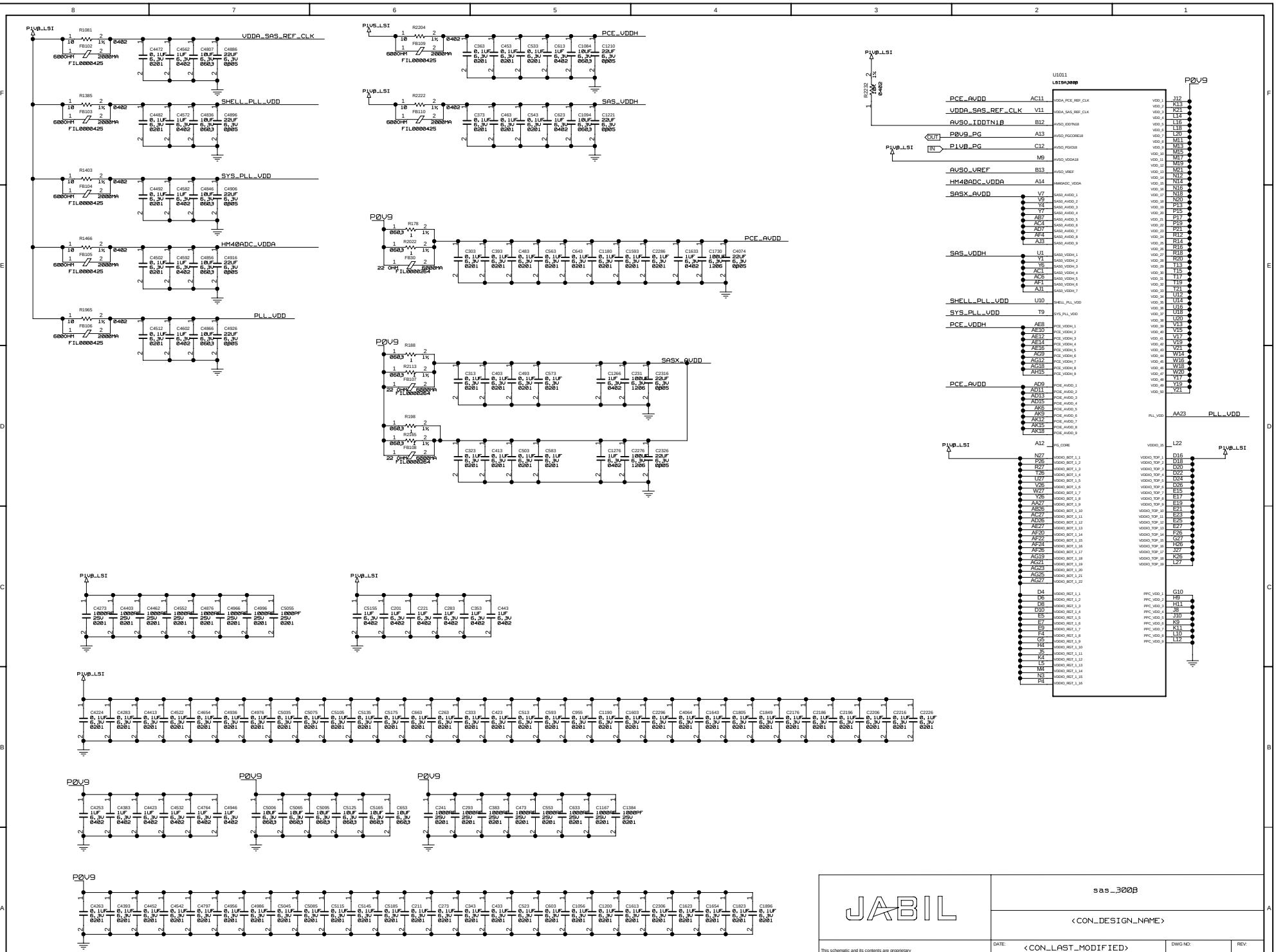
DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	


P1V8_LSI
R1081
FB102
6000HM
FIL0000425
2000MA
0402
C4472 0.1UF 6.3V 0201
C4562 1UF 6.3V 0402
C4807 10UF 6.3V 0603
C4886 22UF 6.3V 0805
VDDA_SAS_REF_CLK
R1385
FB103
C4482 0.1UF 6.3V 0201
C4572 1UF 6.3V 0402
C4836 10UF 6.3V 0603
C4896 22UF 6.3V 0805
SHELL_PLL_VDD
R1403
FB104
C4492 0.1UF 6.3V 0201
C4582 1UF 6.3V 0402
C4846 10UF 6.3V 0603
C4906 22UF 6.3V 0805
SYS_PLL_VDD
R1466
FB105
C4502 0.1UF 6.3V 0201
C4592 1UF 6.3V 0402
C4856 10UF 6.3V 0603
C4916 22UF 6.3V 0805
HM40ADC_VDDA
R1965
FB106
C4512 0.1UF 6.3V 0201
C4602 1UF 6.3V 0402
C4866 10UF 6.3V 0603
C4926 22UF 6.3V 0805
PLL_VDD
P1V5_LSI
R2204
FB109
C363 0.1UF 6.3V 0201
C453 0.1UF 6.3V 0201
C533 0.1UF 6.3V 0201
C613 1UF 6.3V 0402
C1084 10UF 6.3V 0603
C1210 22UF 6.3V 0805
PCE_VDDH
R2222
FB110
C373 0.1UF 6.3V 0201
C463 0.1UF 6.3V 0201
C543 0.1UF 6.3V 0201
C623 1UF 6.3V 0402
C1094 10UF 6.3V 0603
C1221 22UF 6.3V 0805
SAS_VDDH
P0V9
R178
R2022
FB30
22 OHM
C303 0.1UF 6.3V 0201
C393 0.1UF 6.3V 0201
C483 0.1UF 6.3V 0201
C563 0.1UF 6.3V 0201
C643 0.1UF 6.3V 0201
C1180 0.1UF 6.3V 0201
C1593 0.1UF 6.3V 0201
C2286 0.1UF 6.3V 0201
C1633 1UF 6.3V 0402
C1730 100UF 6.3V 1206
C4074 22UF 6.3V 0805
PCE_AVDD
R188
R2113
FB107
C313 0.1UF 6.3V 0201
C403 0.1UF 6.3V 0201
C493 0.1UF 6.3V 0201
C573 0.1UF 6.3V 0201
C1266 1UF 6.3V 0402
C231 100UF 6.3V 1206
C2316 22UF 6.3V 0805
SASX_QVDD
R198
R2125
FB108
C323 0.1UF 6.3V 0201
C413 0.1UF 6.3V 0201
C503 0.1UF 6.3V 0201
C583 0.1UF 6.3V 0201
C1276 1UF 6.3V 0402
C2276 100UF 6.3V 1206
C2326 22UF 6.3V 0805
R2232 10K 1%
U1011
LSISA200P
PCE_AVDD AC11
VDDA_SAS_REF_CLK V11
AVSQ_IDDTN18 B12
P0V9_PG A13
P1V8_PG C12
M9
AVSQ_VREF B13
HM40ADC_VDDA A14
SASX_AVDD
SAS_VDDH
SHELL_PLL_VDD U10
SYS_PLL_VDD T9
PCE_VDDH
PCE_AVDD
PLL_VDD AA23
VDDIO_15 L22
PG_CORE A12
OUT
IN
C4273 1000PF 25V 0201
C4403 1000PF 25V 0201
C4462 1000PF 25V 0201
C4552 1000PF 25V 0201
C4876 1000PF 25V 0201
C4966 1000PF 25V 0201
C4996 1000PF 25V 0201
C5055 1000PF 25V 0201
C5155 1UF 6.3V 0402
C201 1UF 6.3V 0402
C221 1UF 6.3V 0402
C283 1UF 6.3V 0402
C353 1UF 6.3V 0402
C443 1UF 6.3V 0402
C4224 0.1UF 6.3V 0201
C4283 0.1UF 6.3V 0201
C4413 0.1UF 6.3V 0201
C4522 0.1UF 6.3V 0201
C4654 0.1UF 6.3V 0201
C4936 0.1UF 6.3V 0201
C4976 0.1UF 6.3V 0201
C5035 0.1UF 6.3V 0201
C5075 0.1UF 6.3V 0201
C5105 0.1UF 6.3V 0201
C5135 0.1UF 6.3V 0201
C5175 0.1UF 6.3V 0201
C663 0.1UF 6.3V 0201
C263 0.1UF 6.3V 0201
C333 0.1UF 6.3V 0201
C423 0.1UF 6.3V 0201
C513 0.1UF 6.3V 0201
C593 0.1UF 6.3V 0201
C955 0.1UF 6.3V 0201
C1190 0.1UF 6.3V 0201
C1603 0.1UF 6.3V 0201
C2296 0.1UF 6.3V 0201
C4064 0.1UF 6.3V 0201
C1643 0.1UF 6.3V 0201
C1805 0.1UF 6.3V 0201
C1849 0.1UF 6.3V 0201
C2176 0.1UF 6.3V 0201
C2186 0.1UF 6.3V 0201
C2196 0.1UF 6.3V 0201
C2206 0.1UF 6.3V 0201
C2216 0.1UF 6.3V 0201
C2226 0.1UF 6.3V 0201
C4253 1UF 6.3V 0402
C4383 1UF 6.3V 0402
C4423 1UF 6.3V 0402
C4532 1UF 6.3V 0402
C4764 1UF 6.3V 0402
C4946 1UF 6.3V 0402
C5006 10UF 6.3V 0603
C5065 10UF 6.3V 0603
C5095 10UF 6.3V 0603
C5125 10UF 6.3V 0603
C5165 10UF 6.3V 0603
C653 10UF 6.3V 0603
C241 1000PF 25V 0201
C293 1000PF 25V 0201
C383 1000PF 25V 0201
C473 1000PF 25V 0201
C553 1000PF 25V 0201
C633 1000PF 25V 0201
C1167 1000PF 25V 0201
C1384 1000PF 25V 0201
C4263 0.1UF 6.3V 0201
C4393 0.1UF 6.3V 0201
C4452 0.1UF 6.3V 0201
C4542 0.1UF 6.3V 0201
C4797 0.1UF 6.3V 0201
C4956 0.1UF 6.3V 0201
C4986 0.1UF 6.3V 0201
C5045 0.1UF 6.3V 0201
C5085 0.1UF 6.3V 0201
C5115 0.1UF 6.3V 0201
C5145 0.1UF 6.3V 0201
C5185 0.1UF 6.3V 0201
C211 0.1UF 6.3V 0201
C273 0.1UF 6.3V 0201
C343 0.1UF 6.3V 0201
C433 0.1UF 6.3V 0201
C523 0.1UF 6.3V 0201
C603 0.1UF 6.3V 0201
C1056 0.1UF 6.3V 0201
C1200 0.1UF 6.3V 0201
C1613 0.1UF 6.3V 0201
C2306 0.1UF 6.3V 0201
C1623 0.1UF 6.3V 0201
C1654 0.1UF 6.3V 0201
C1823 0.1UF 6.3V 0201
C1896 0.1UF 6.3V 0201
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DWG NO:
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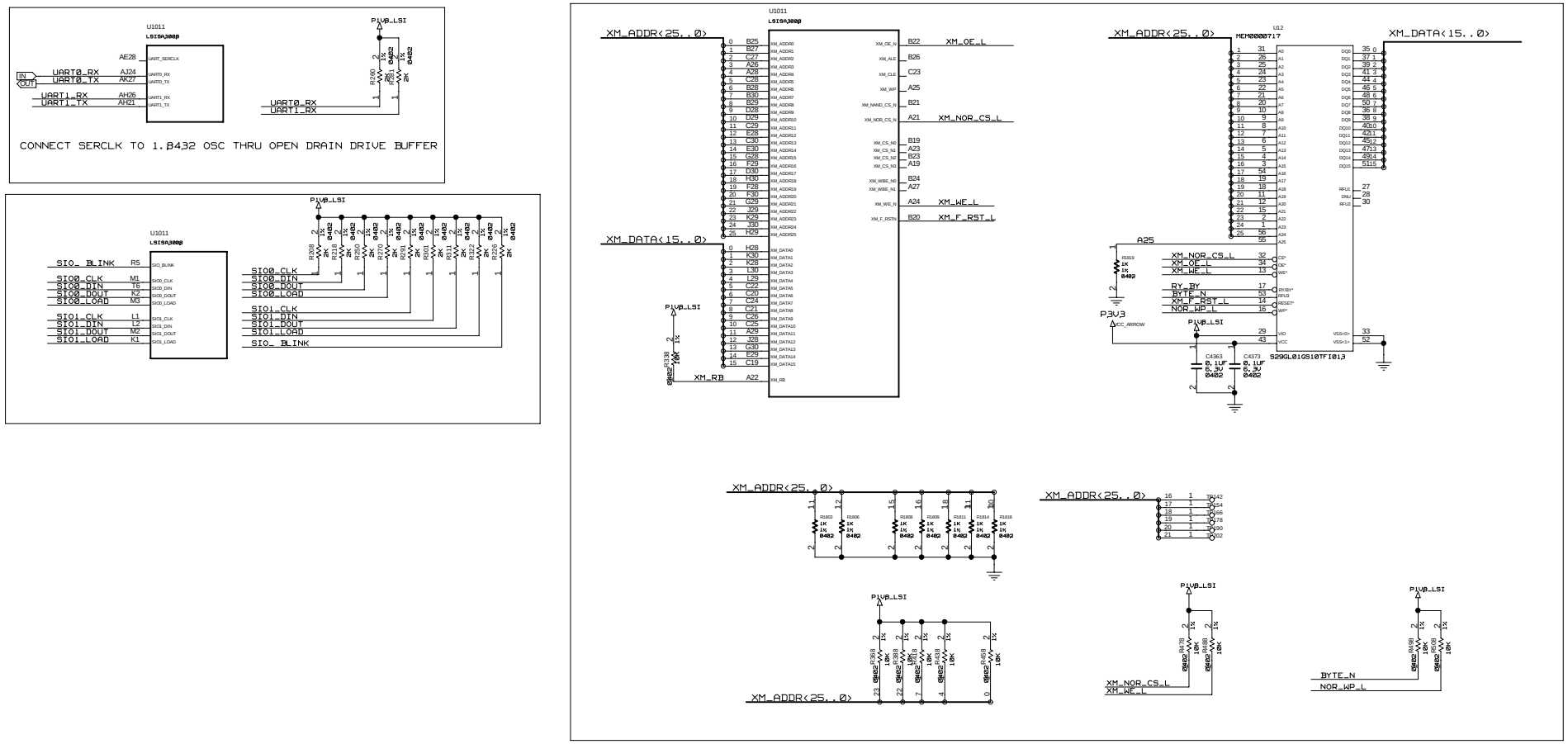
SHEET: <CURRENT_DESIGN_SHEET>OF<TOTAL_DESIGN_SHEETS>



POWER-ON SENSE OPTIONS:

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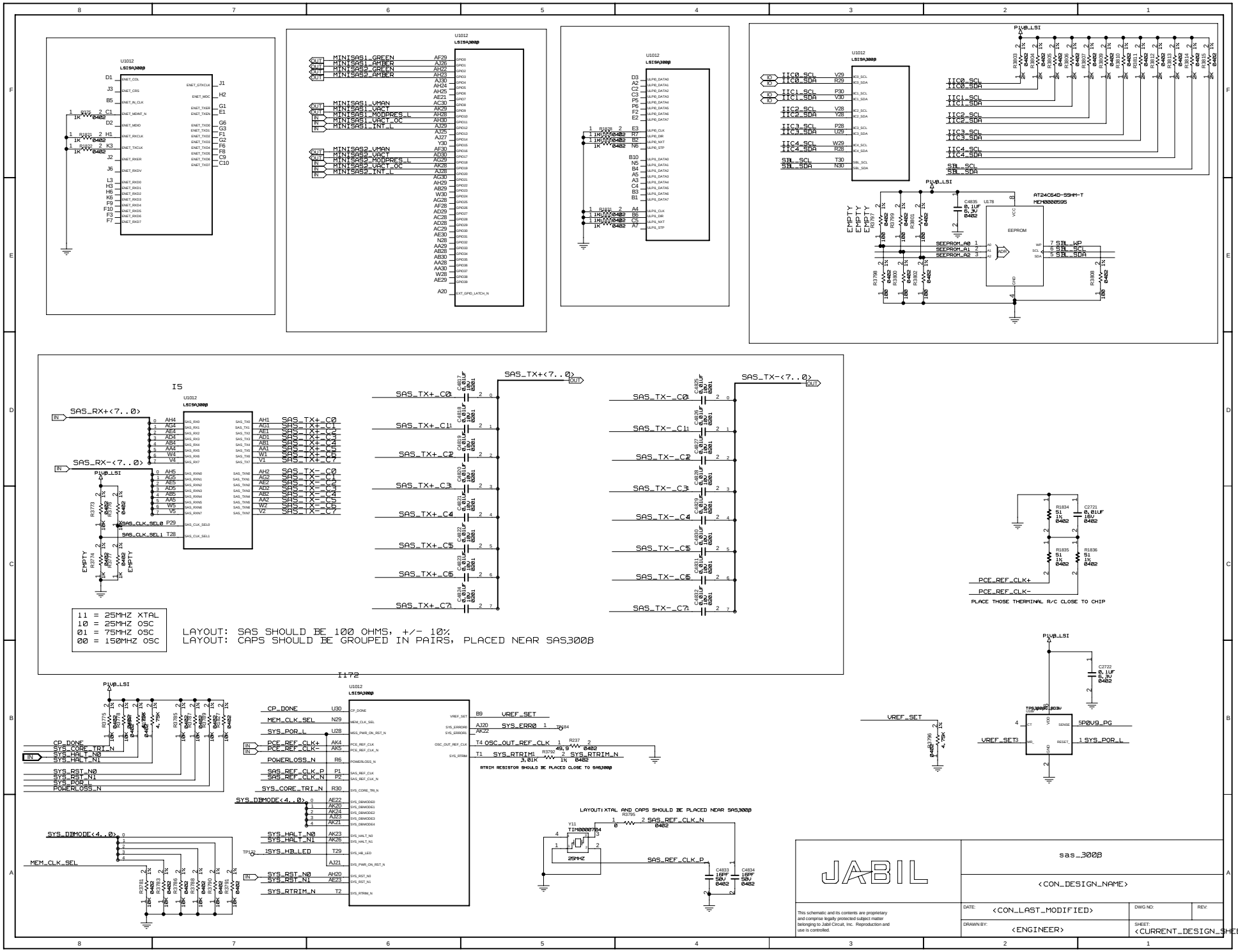
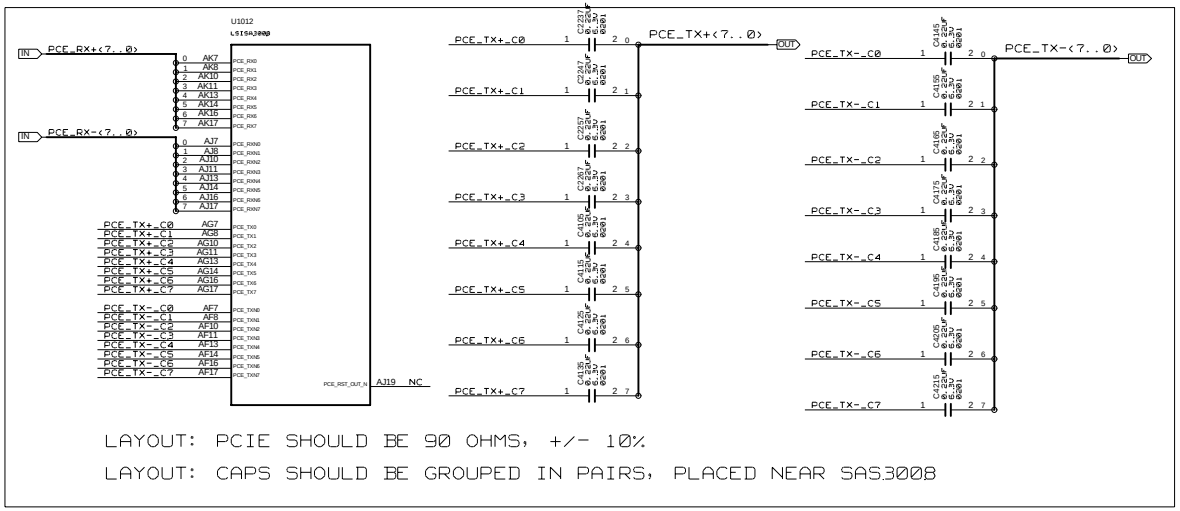
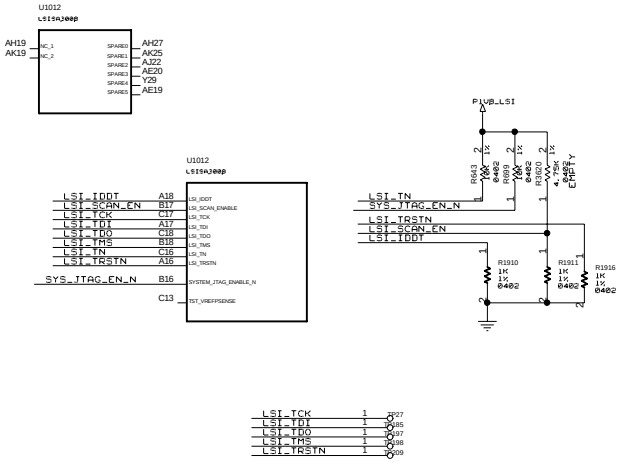
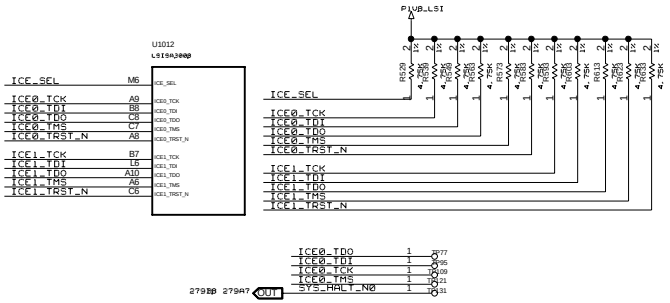
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



DO WE NEED TO CONNECT TESTMUX?







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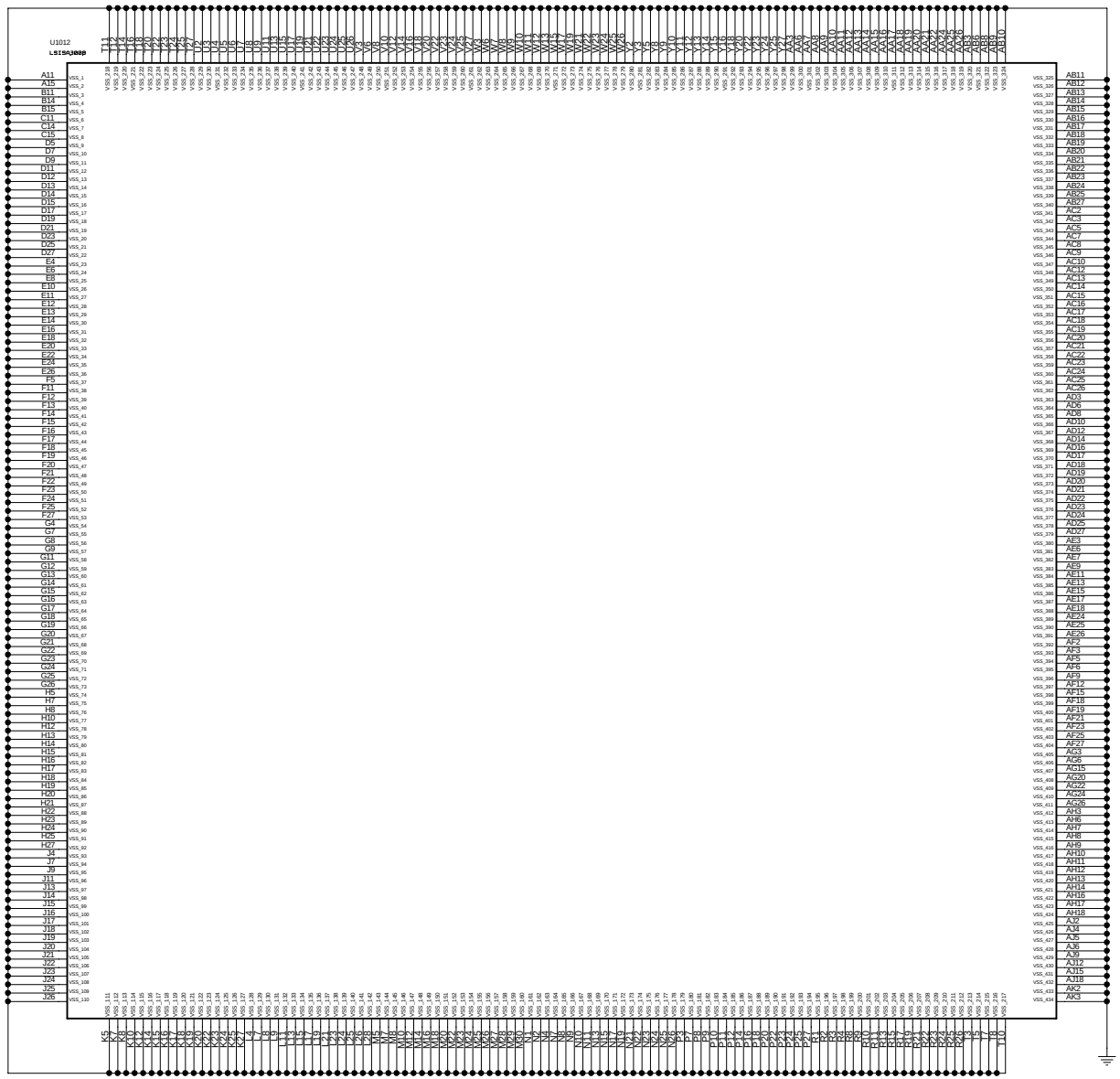
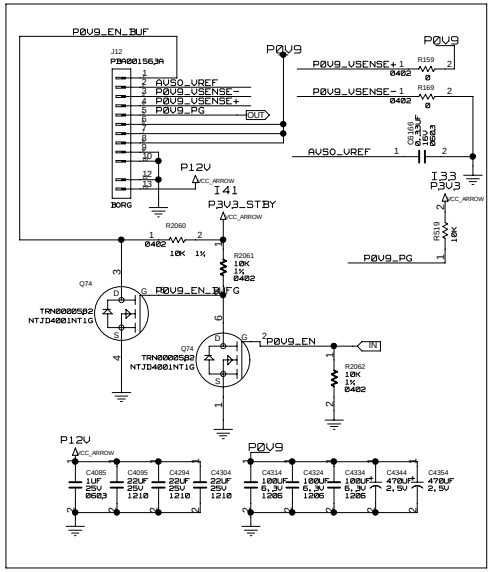
	DRAWN BY: <ENGINEER> SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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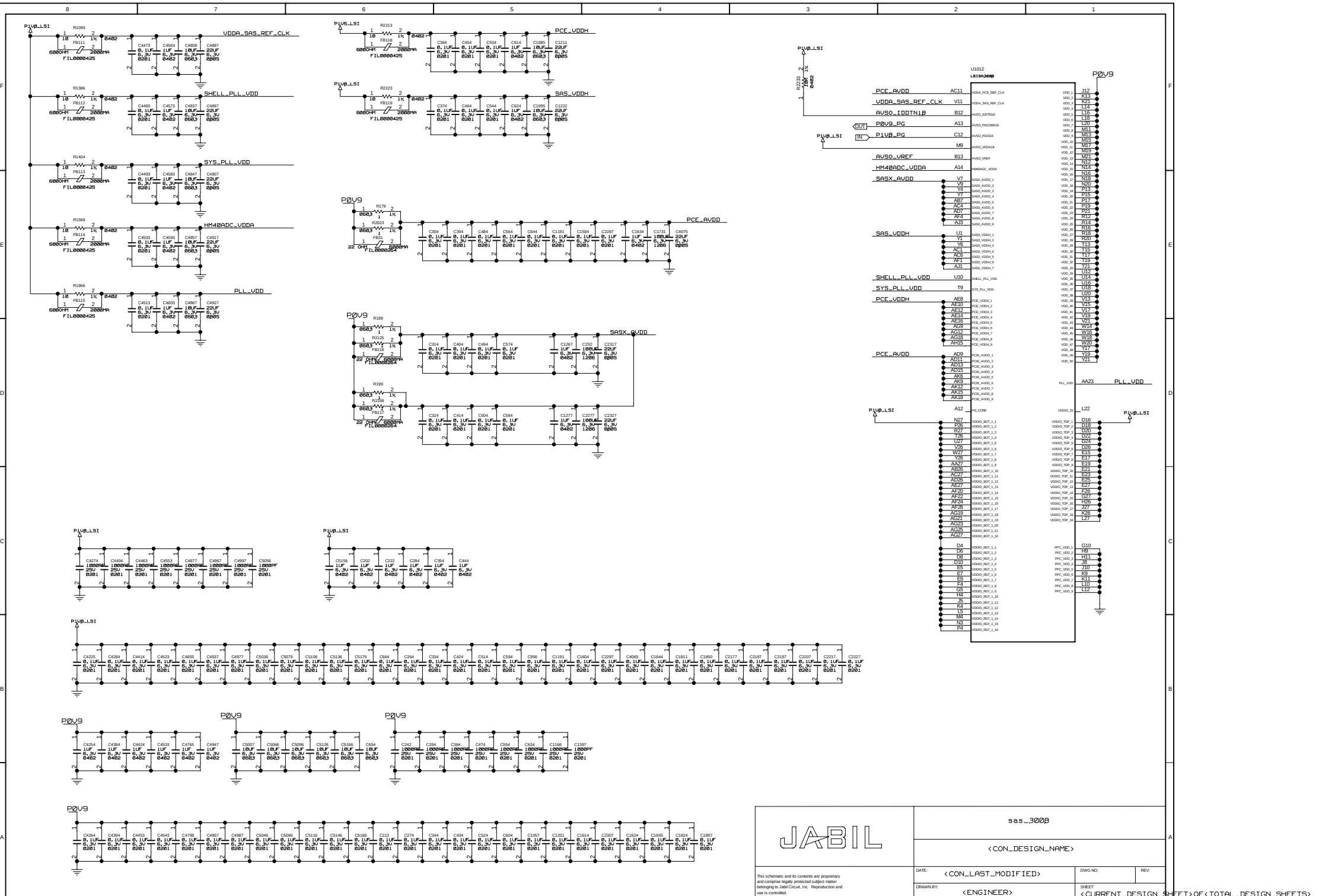
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:
DRAWN BY: <ENGINEER>	REV:
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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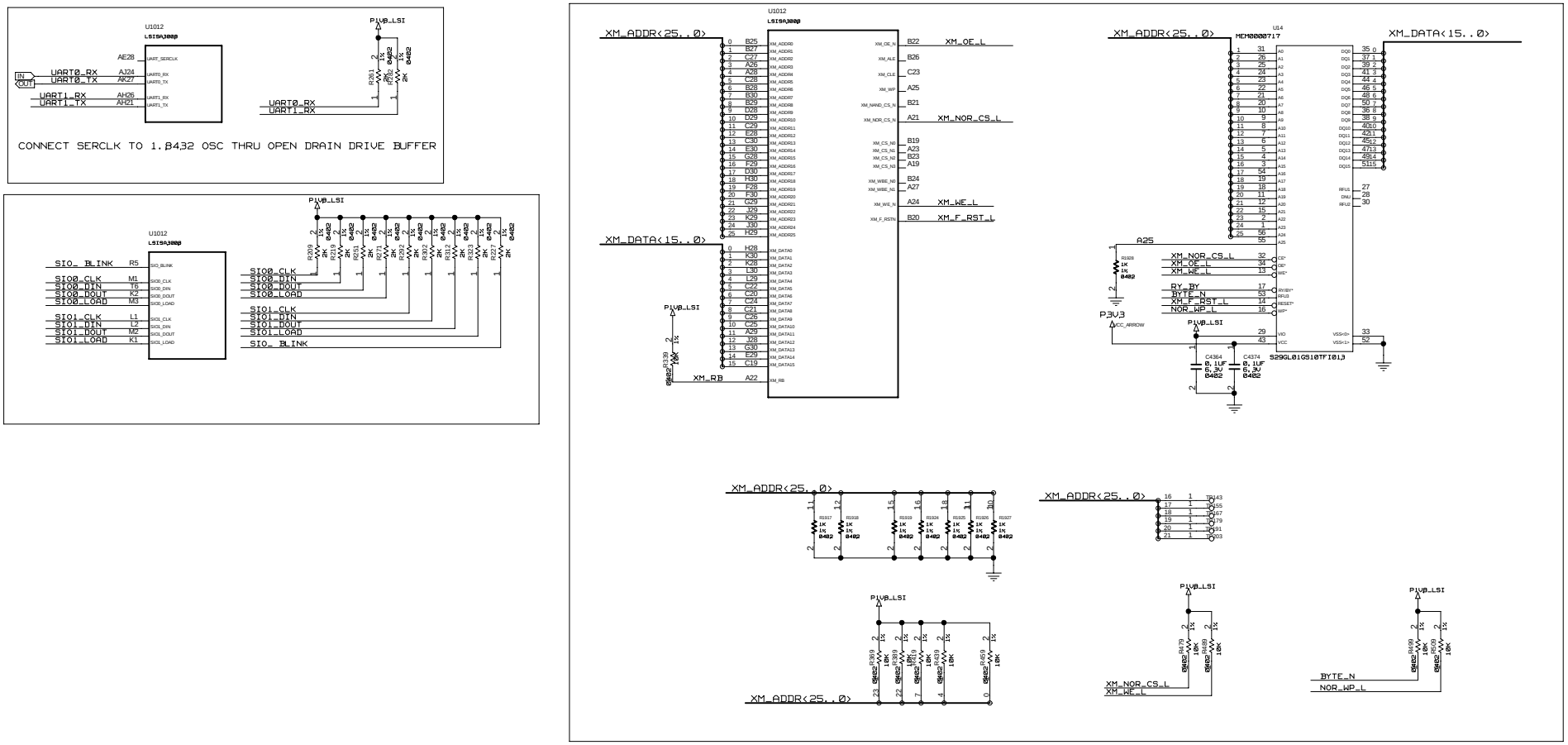
DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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DATE: <CON_LAST_MODIFIED>

DWG NO:

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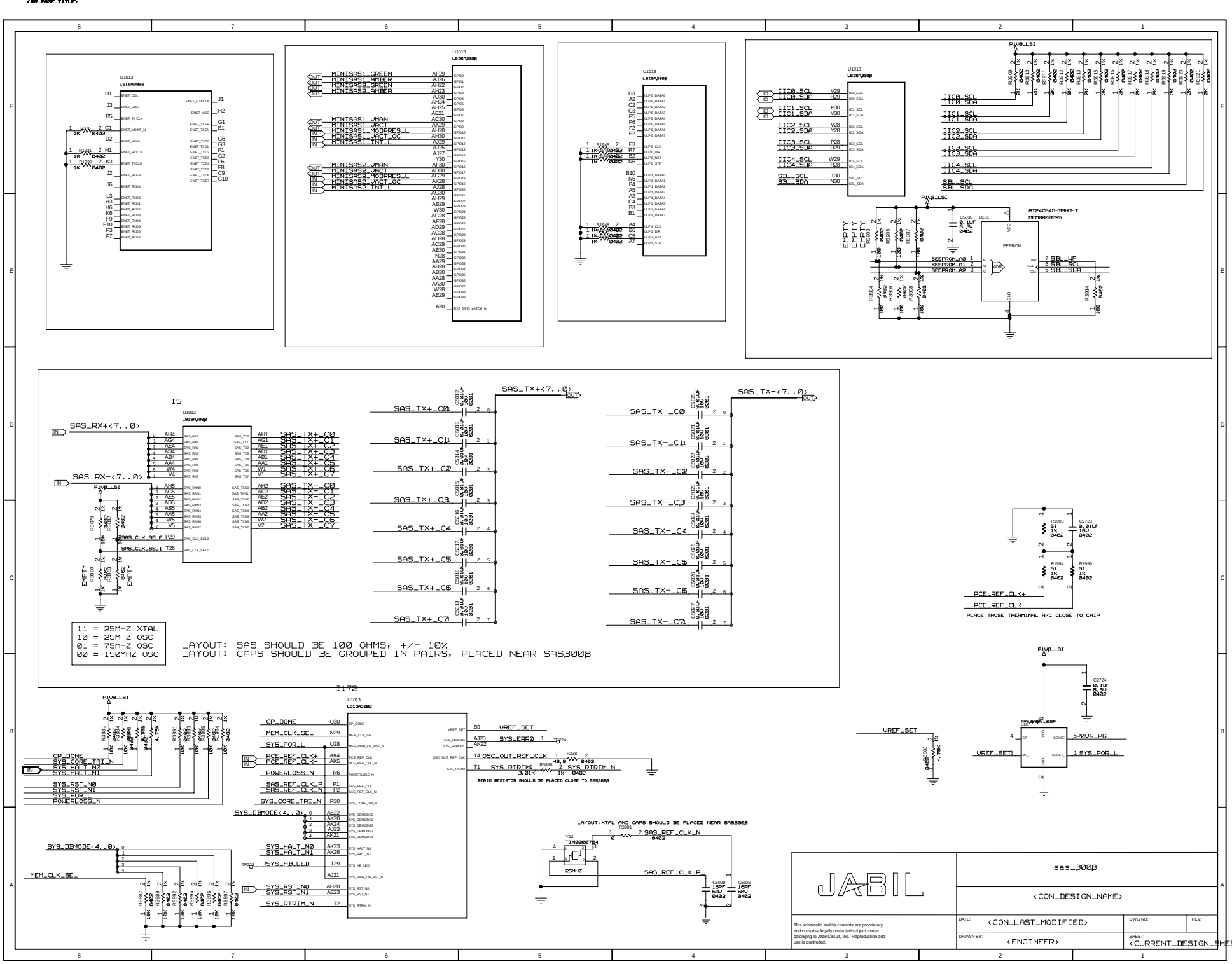
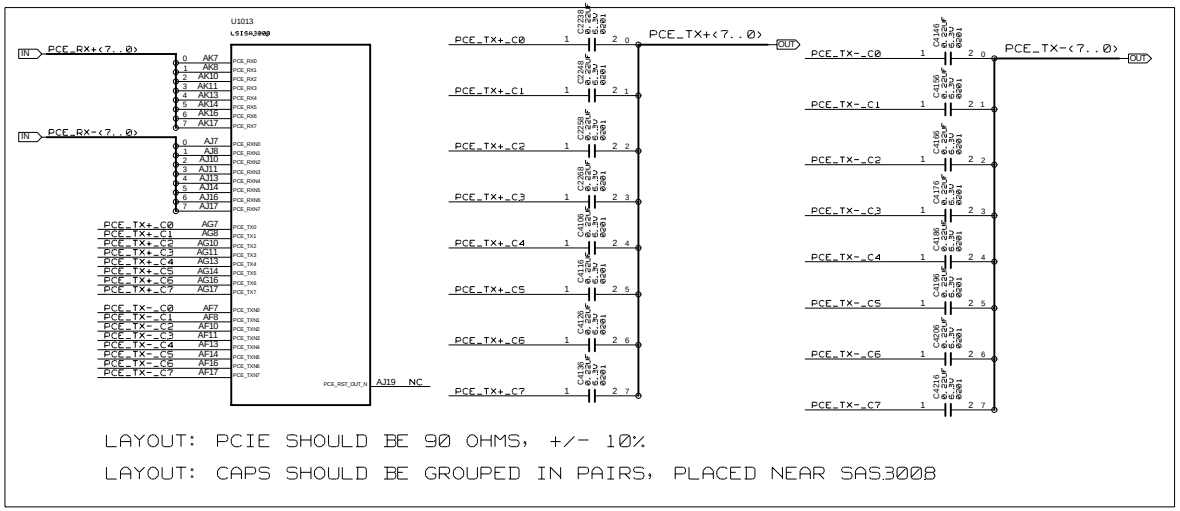
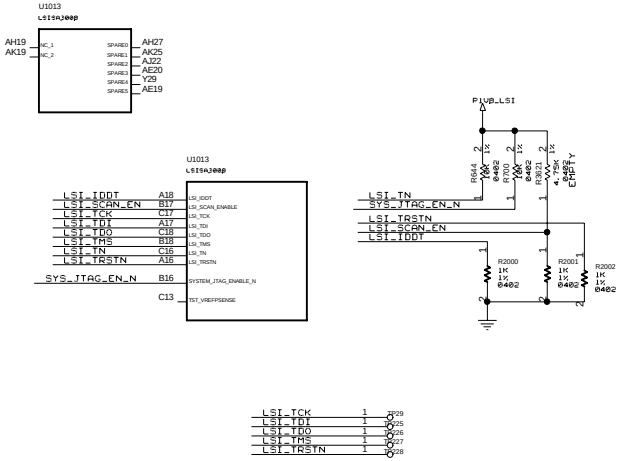
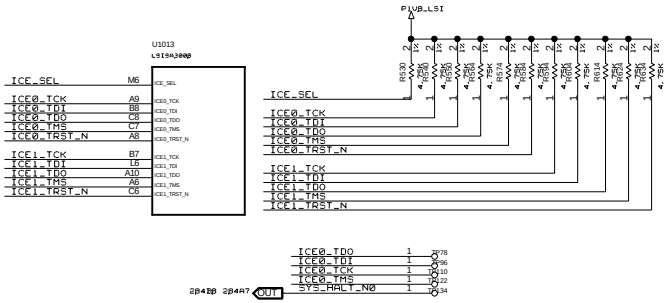
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



DO WE NEED TO CONNECT TESTMUX?







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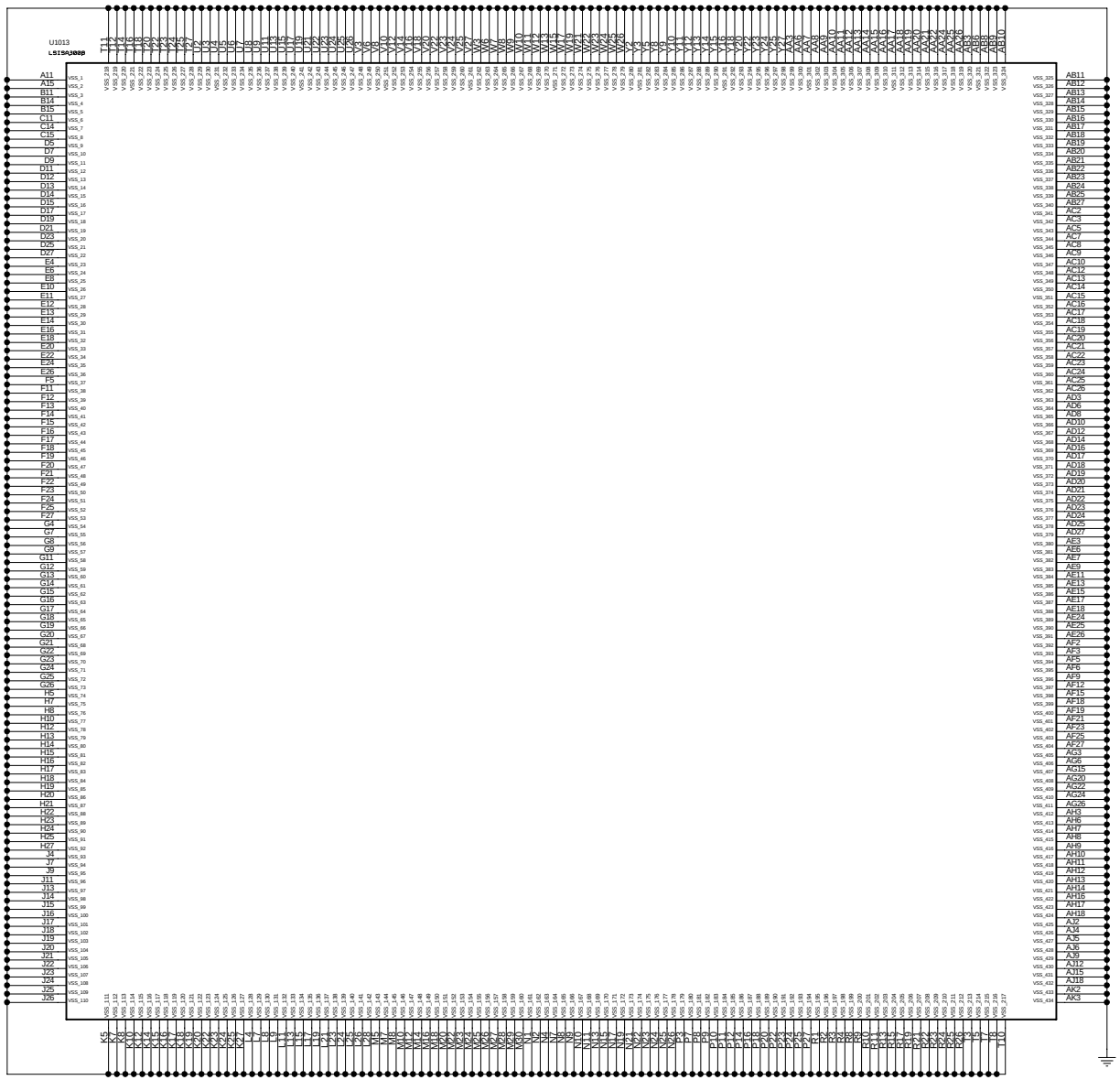
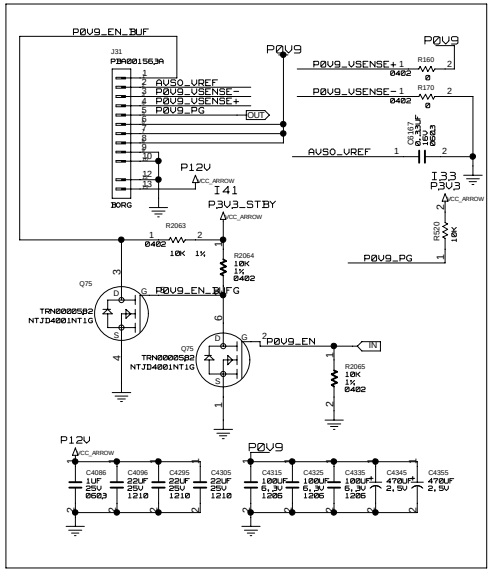
	DRAWN BY: <ENGINEER> SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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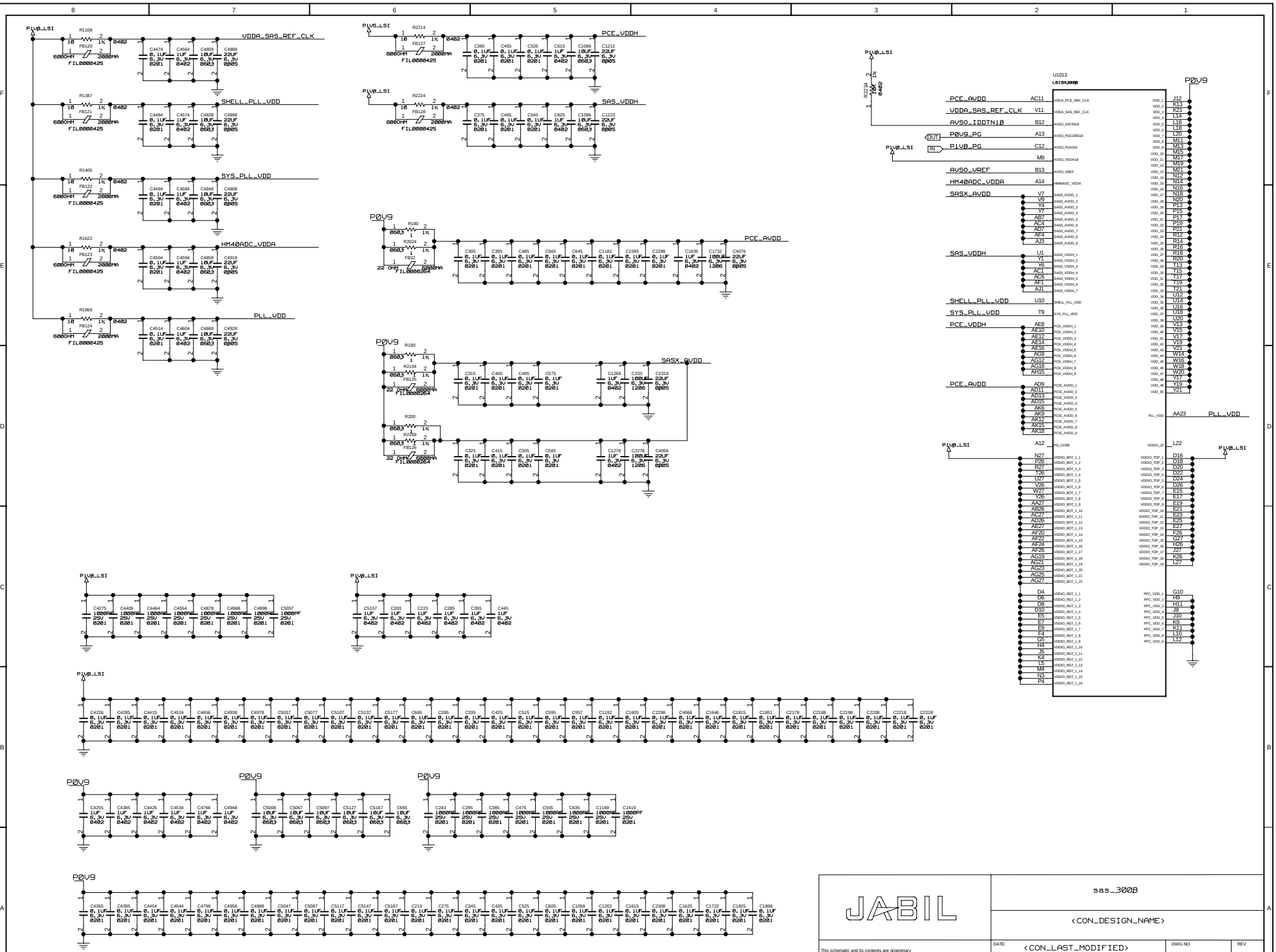
	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



JABIL	sas_300B
	<CON_DESIGN_NAME>
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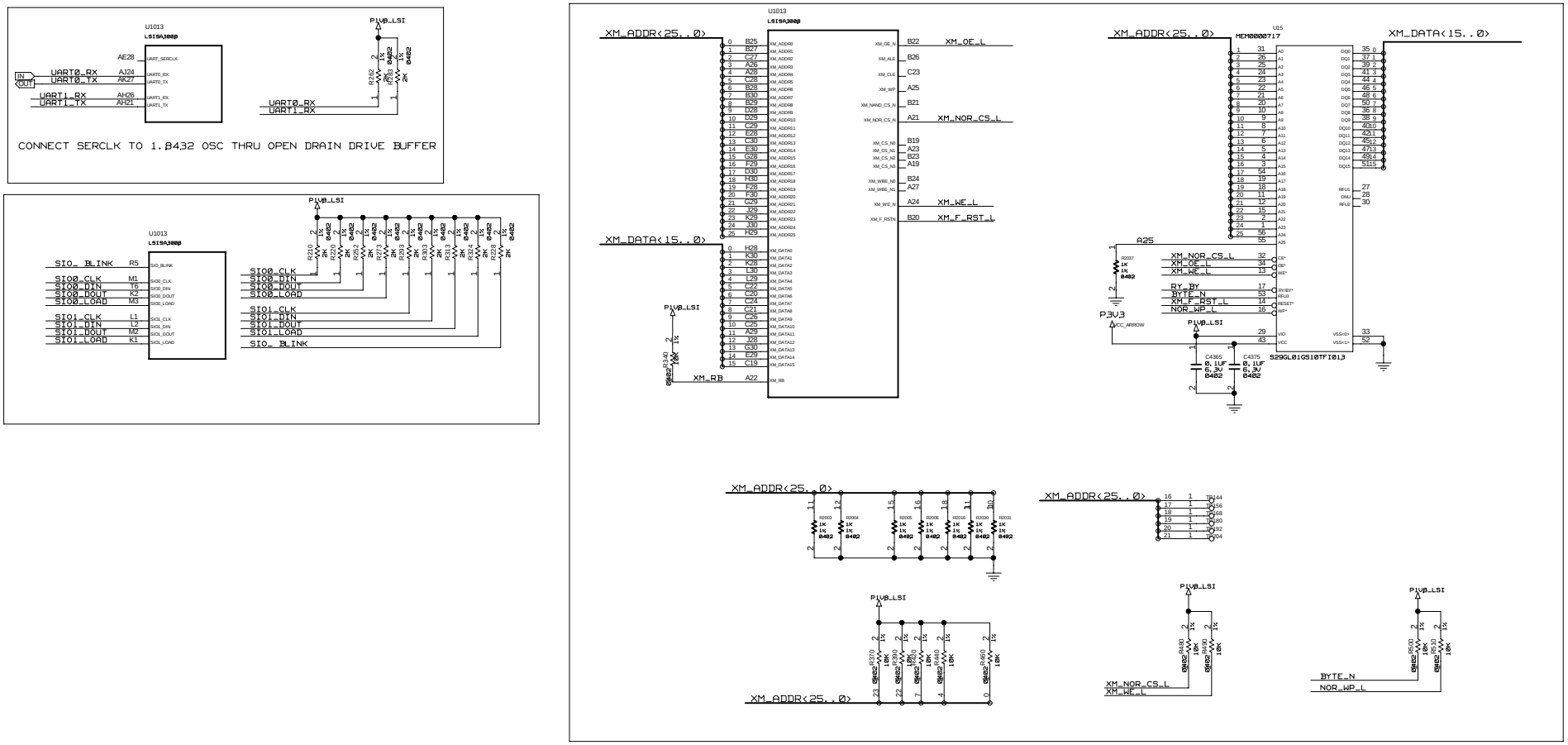
	DRAWN BY: <ENGINEER> SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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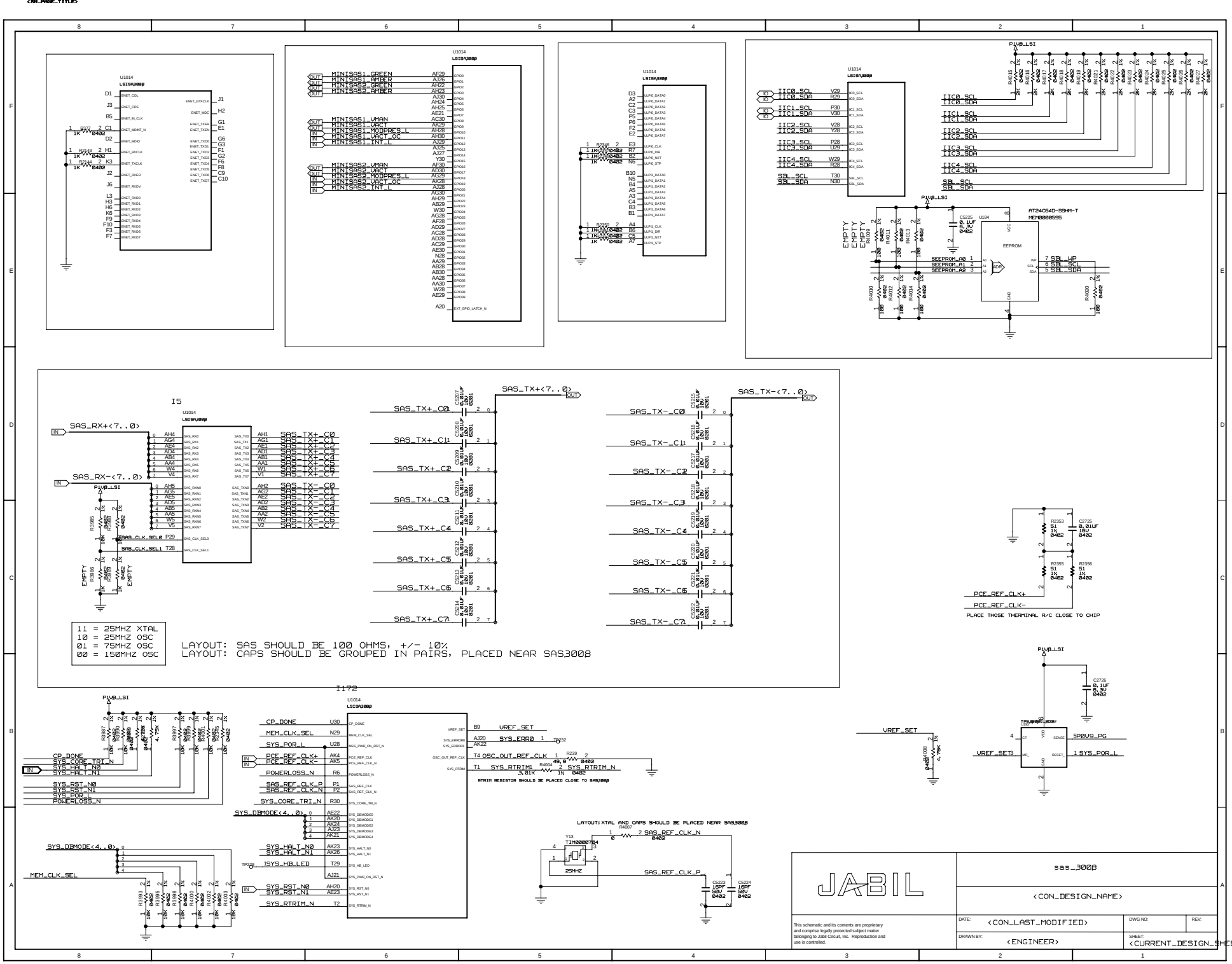
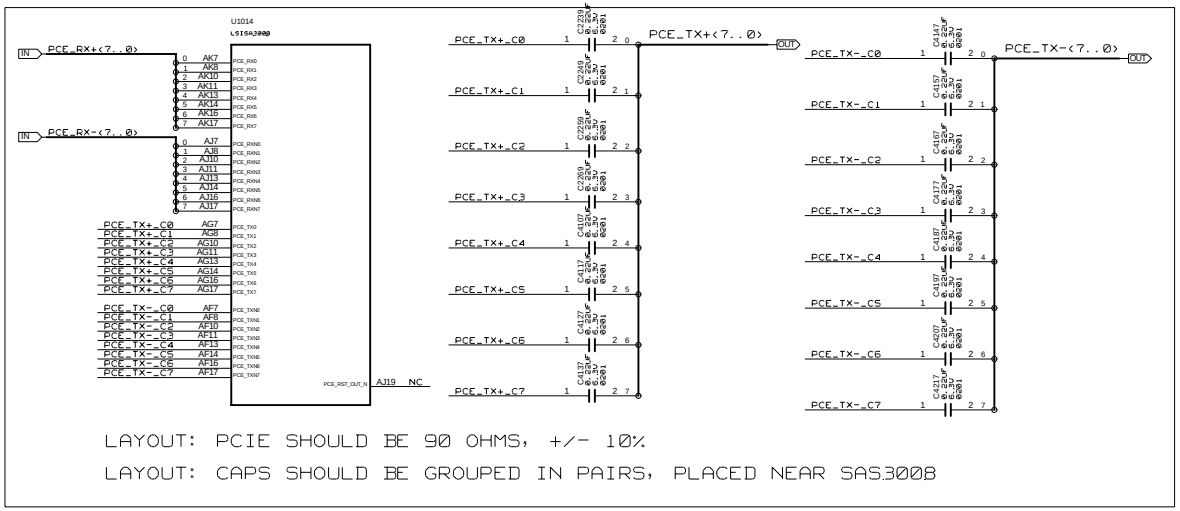
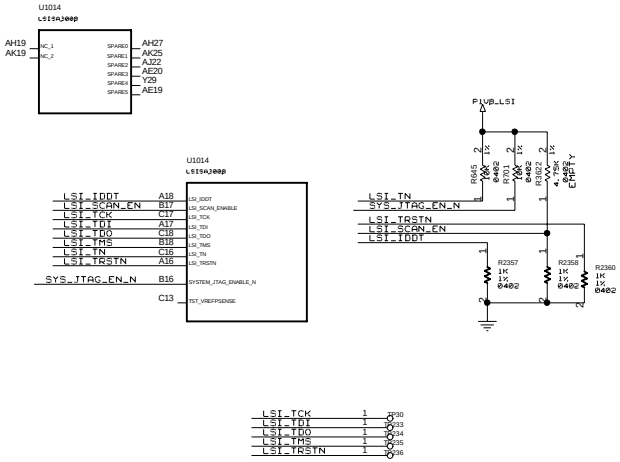
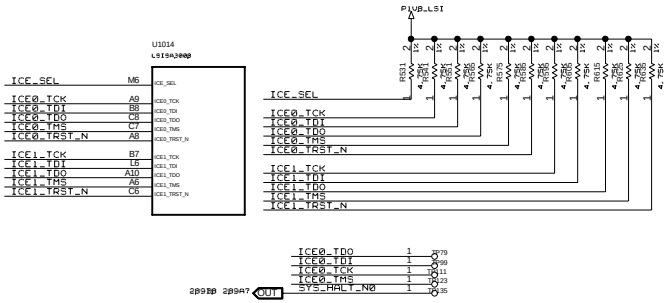
DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



DO WE NEED TO CONNECT TESTMUX?







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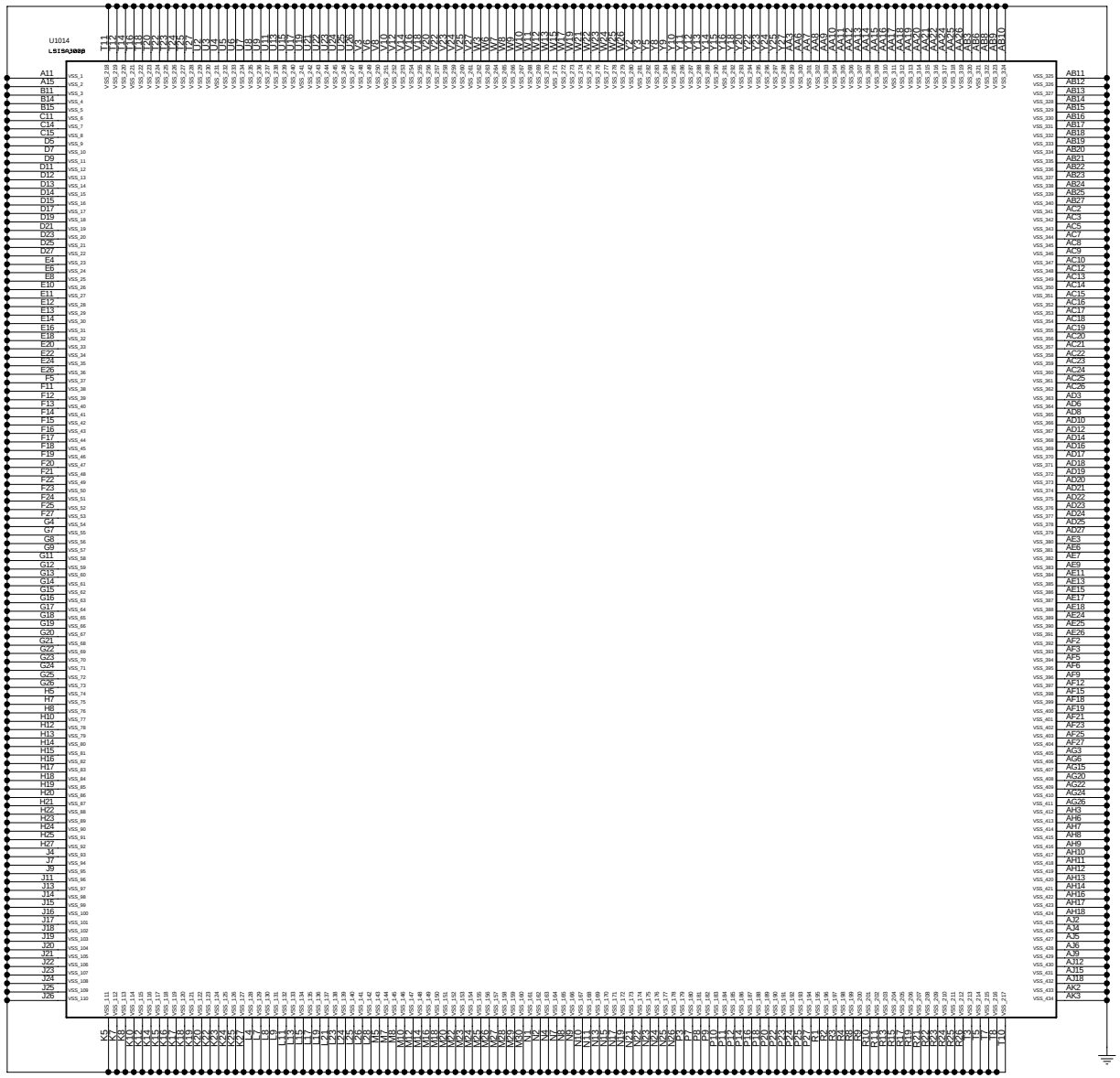
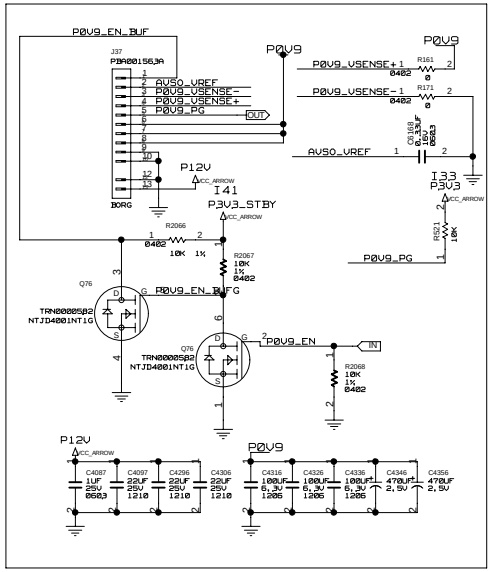
	DRAWN BY: <ENGINEER> / SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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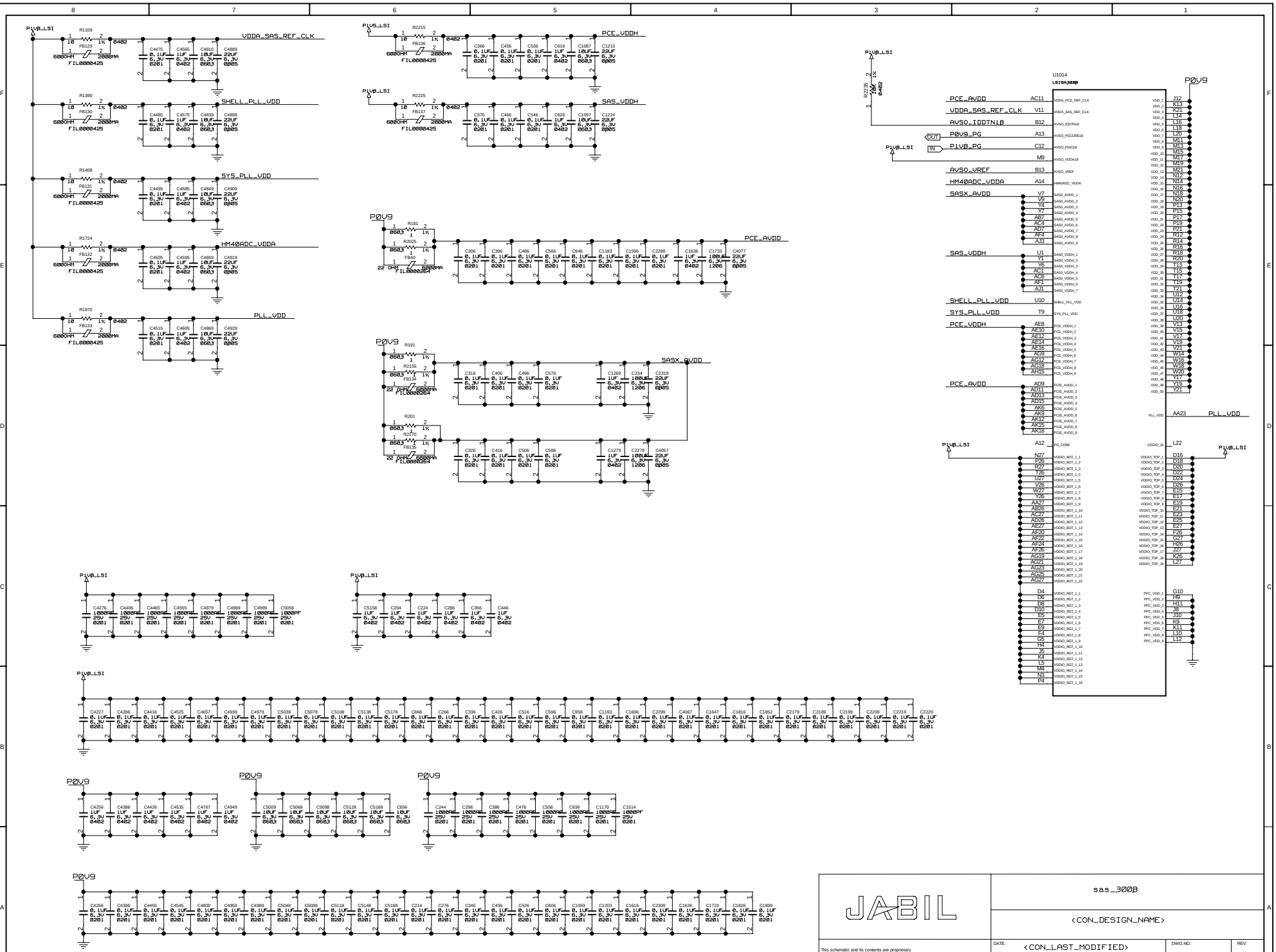
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:
	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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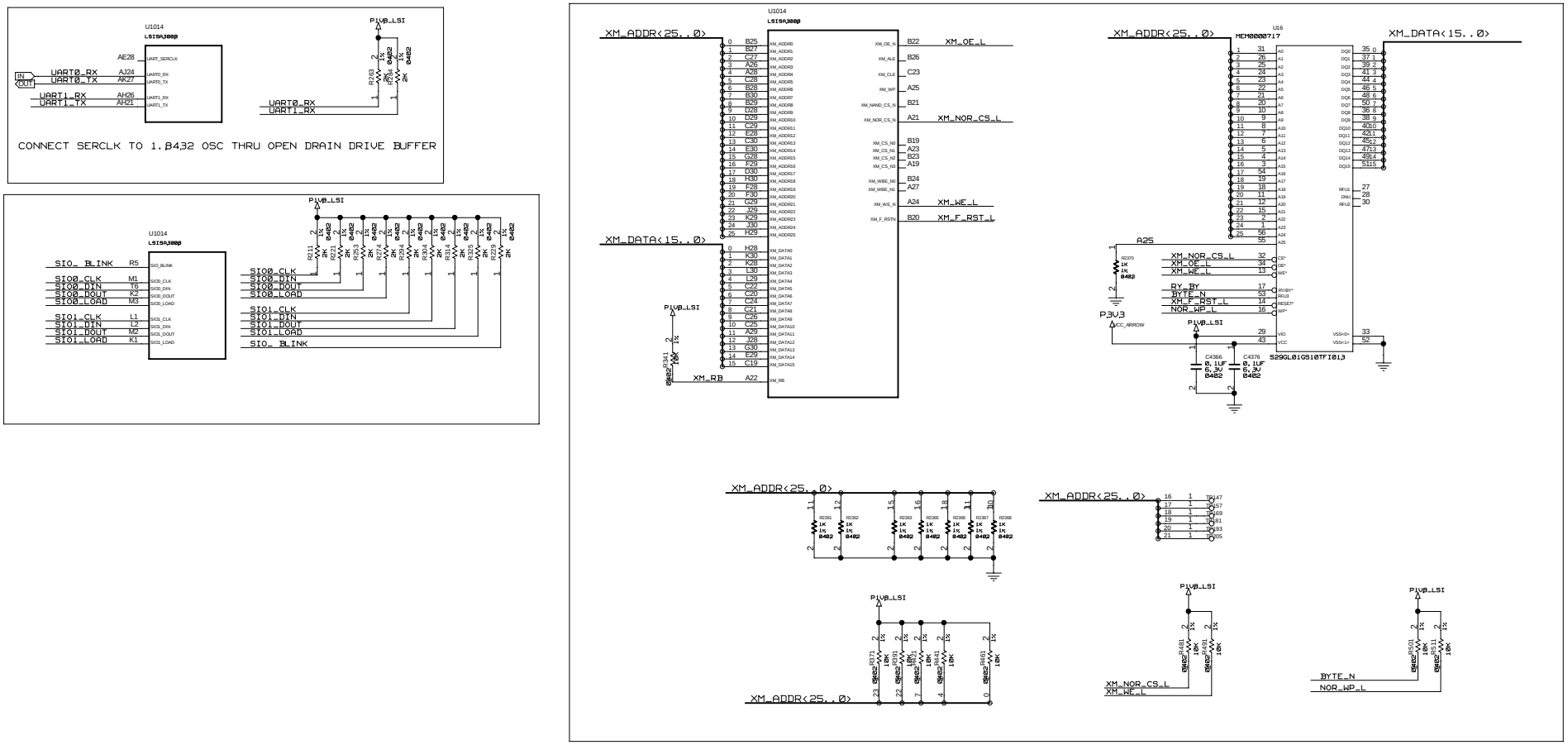
DATE: <CON_LAST_MODIFIED>		DWG NO:	REV:
DRAWN BY: <ENGINEER>		SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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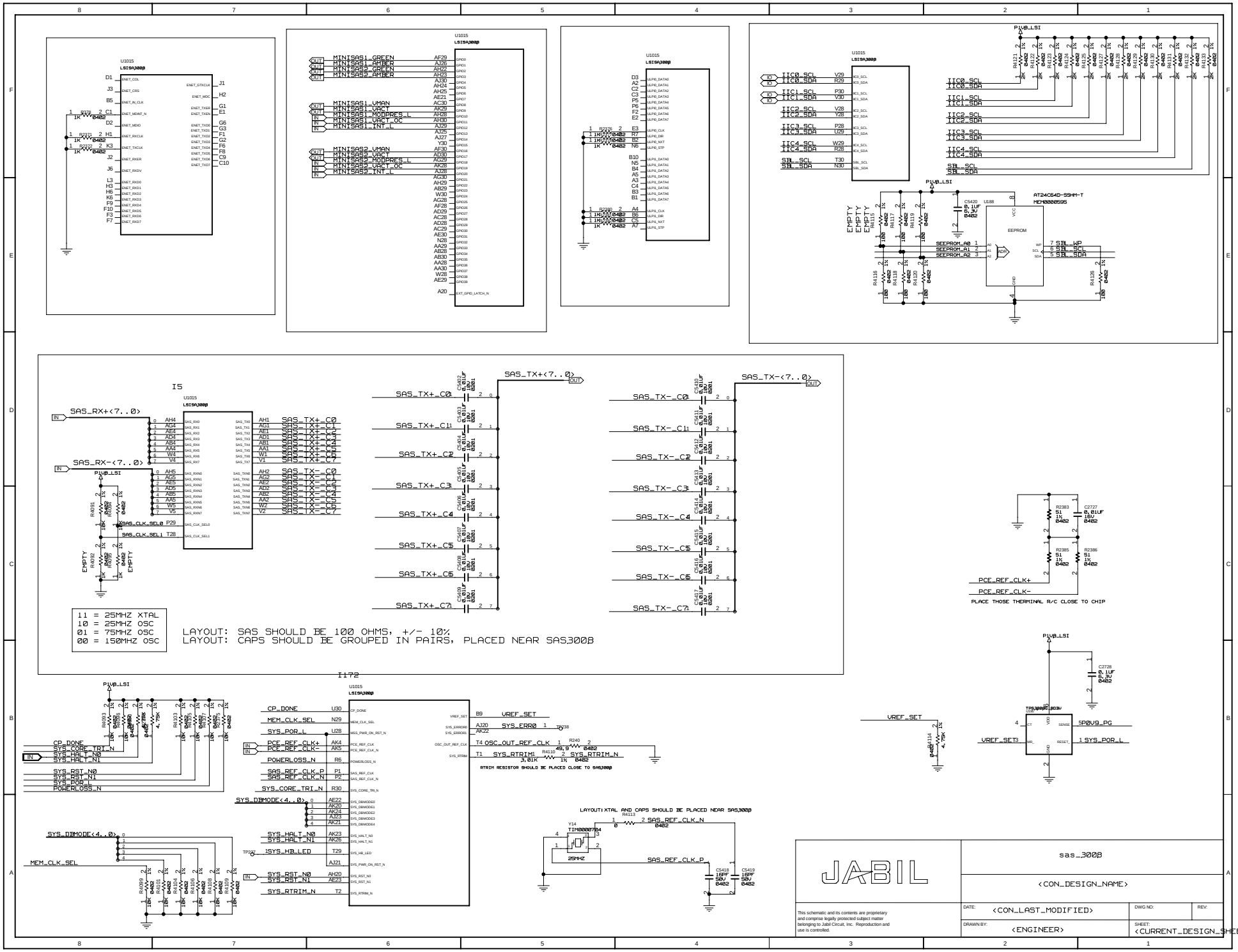
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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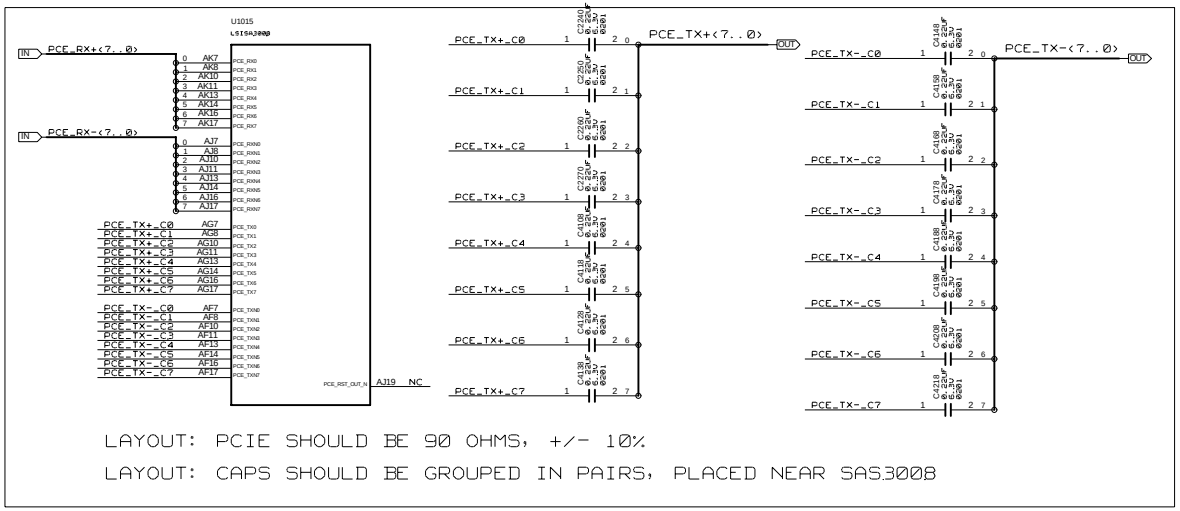

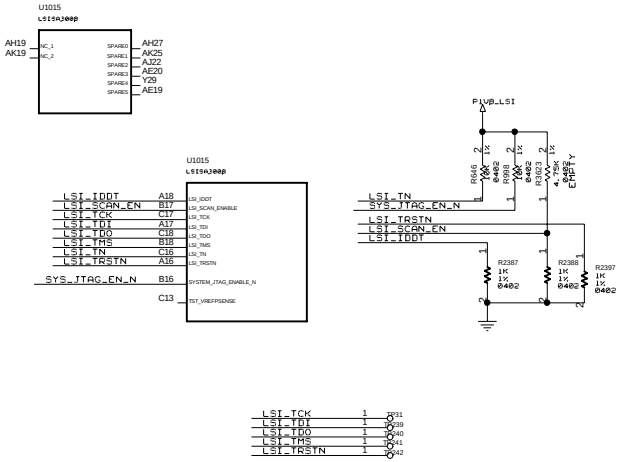

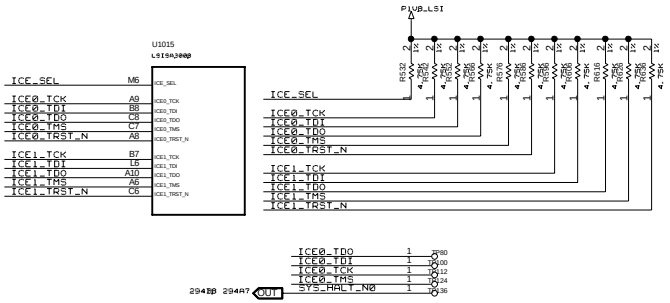

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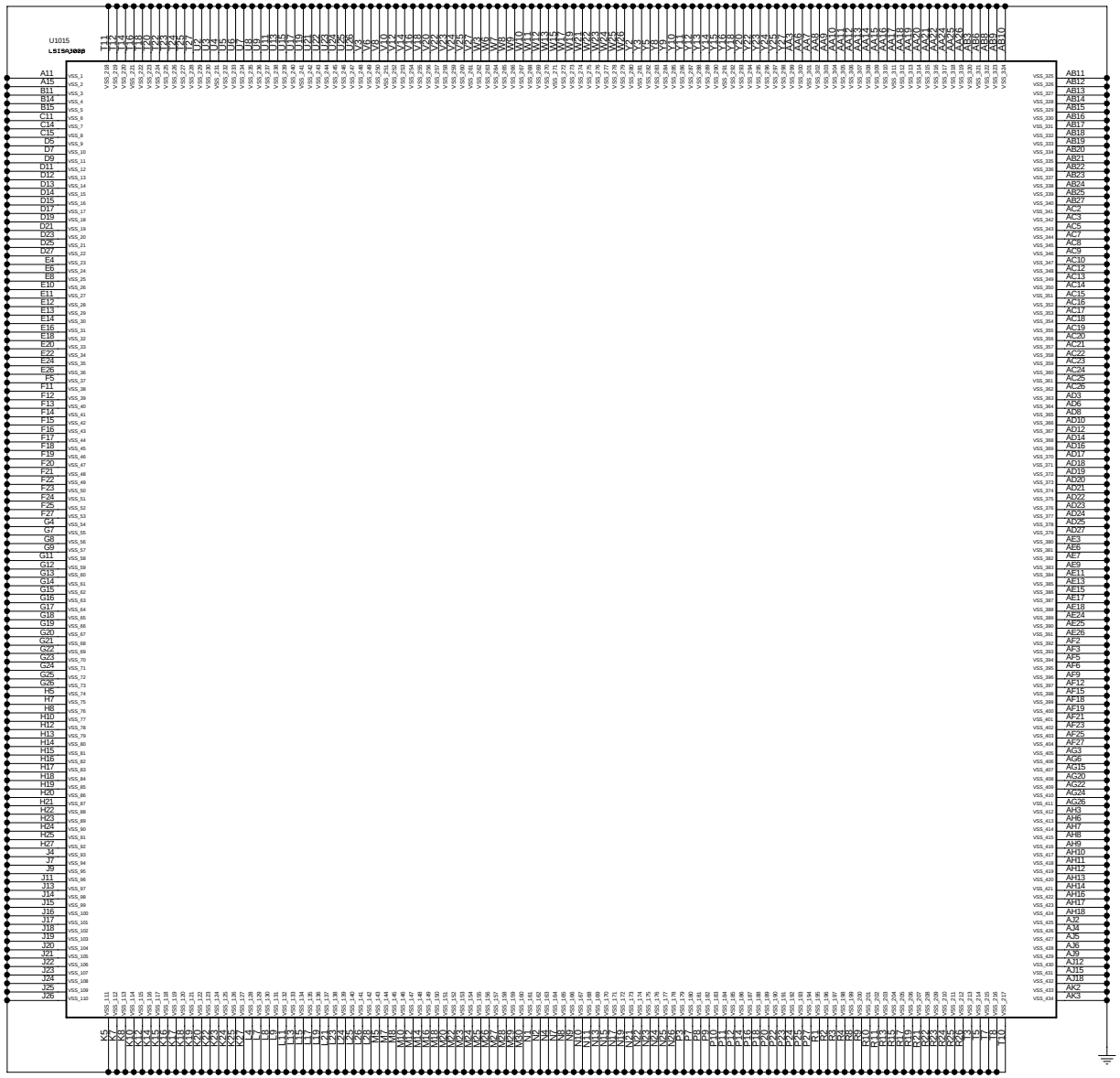
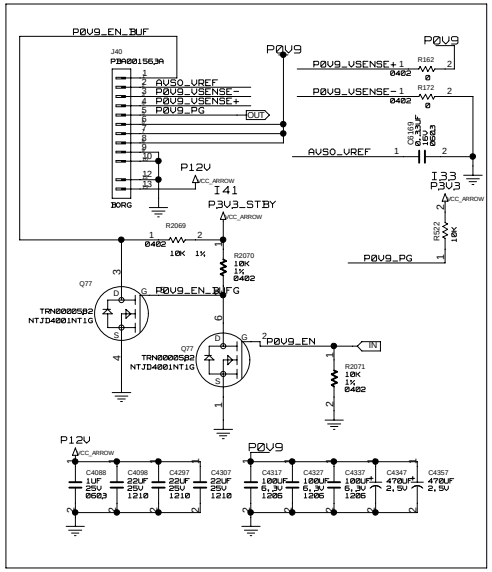
	DRAWN BY: <ENGINEER> / SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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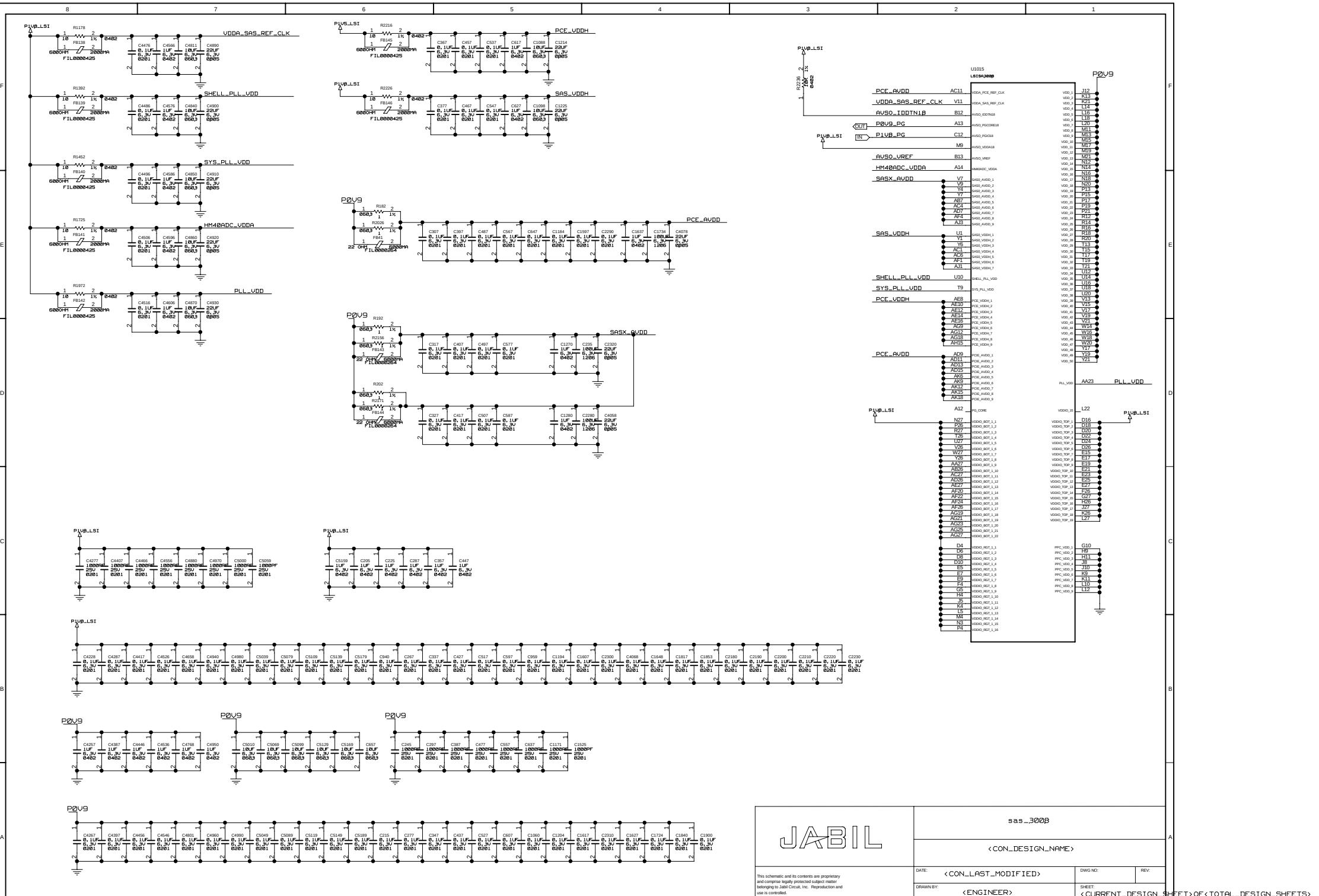
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>		DWG NO:	REV:
DRAWN BY: <ENGINEER>		SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	


P1V8_LSI
R1178
FB138
FIL0000425
VDDA_SAS_REF_CLK
SHELL_PLL_VDD
SYS_PLL_VDD
HM40ADC_VDDA
PLL_VDD
P1V5_LSI
R2216
FB145
PCE_VDDH
R2226
FB146
SAS_VDDH
P0V9
R182
R2026
FB141
PCE_AVDD
R192
R2156
FB143
SASX_QVDD
R202
R2171
FB144
U1015
LSISAJ0MP
P0V9_PG
P1V8_PG
AVSQ_IDDTN18
AVSQ_VREF
SASX_AVDD
SAS_VDDH
SHELL_PLL_VDD
SYS_PLL_VDD
PCE_VDDH
PCE_AVDD
PLL_VDD
VDDIO_15
VDDIO_BOT_1_1
VDDIO_RGT_1_1
PPC_VDD_1
VDDIO_TOP_1
VDD_1
VDD_50
C4277
C4407
C4468
C4556
C4880
C4970
C5000
C5059
C5159
C205
C225
C287
C357
C447
C4228
C4287
C4417
C4526
C4658
C4940
C4980
C5039
C5079
C5109
C5139
C5179
C940
C267
C337
C427
C517
C597
C959
C1194
C1607
C2300
C4068
C1648
C1817
C1853
C2180
C2190
C2200
C2210
C2220
C2230
C4257
C4387
C4446
C4536
C4768
C4950
C5010
C5069
C5099
C5129
C5169
C657
C245
C297
C387
C477
C557
C637
C1171
C1525
C4267
C4397
C4456
C4546
C4801
C4960
C4990
C5049
C5089
C5119
C5149
C5189
C215
C277
C347
C437
C527
C607
C1060
C1204
C1617
C2310
C1627
C1734
C1840
C1900
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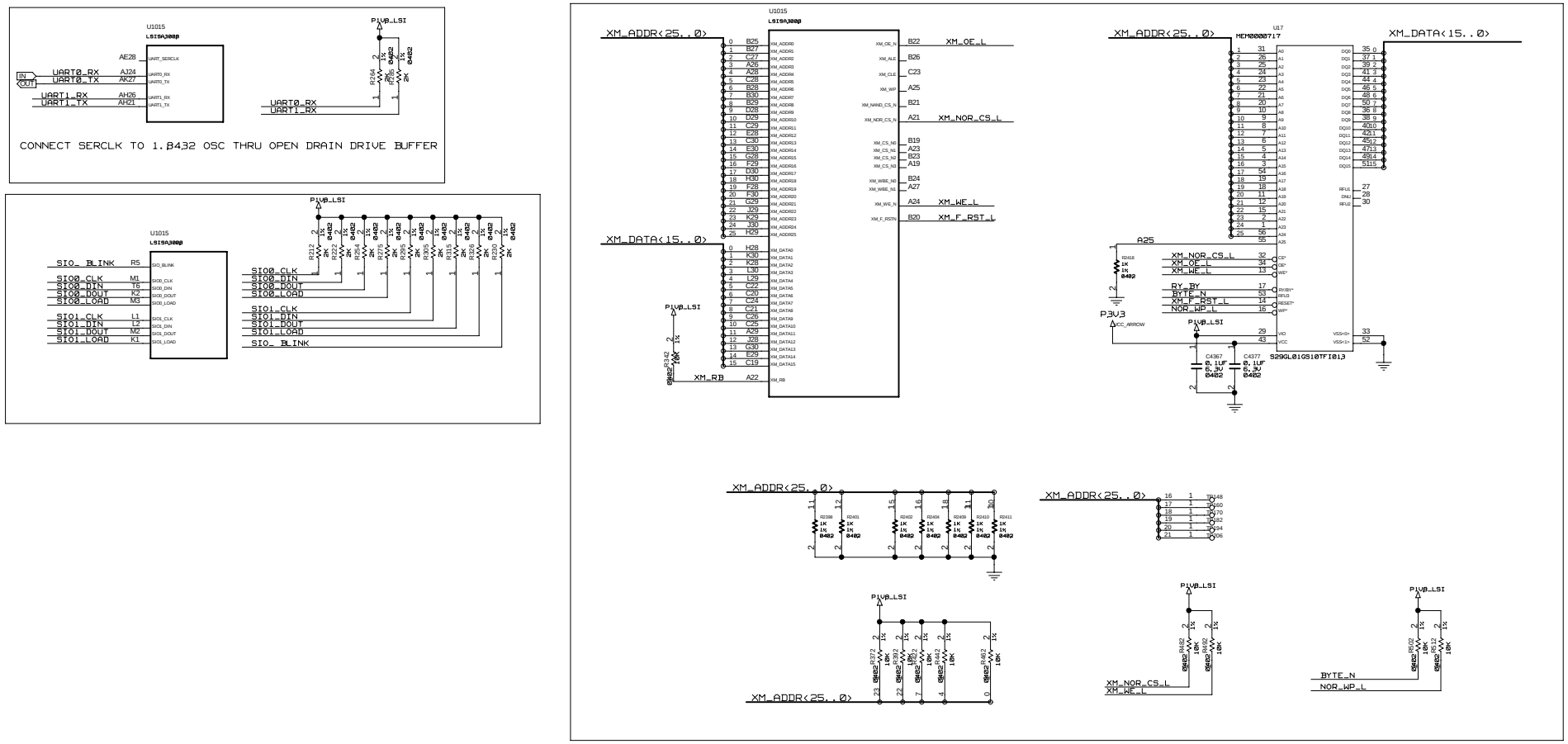
DWG NO:
REV:
DRAWN BY:
<ENGINEER>
SHEET:
<CURRENT_DESIGN_SHEET>OF<TOTAL_DESIGN_SHEETS>



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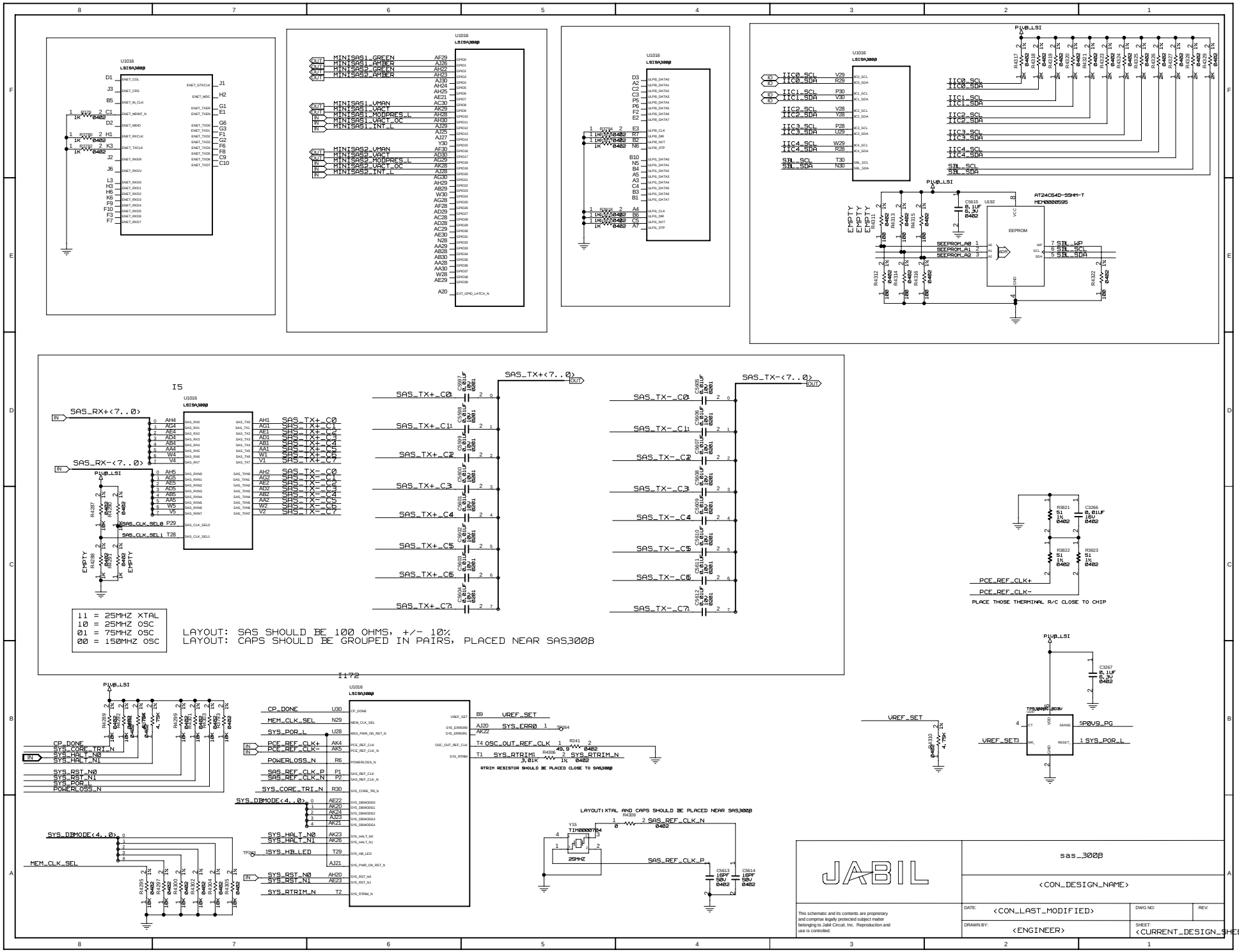
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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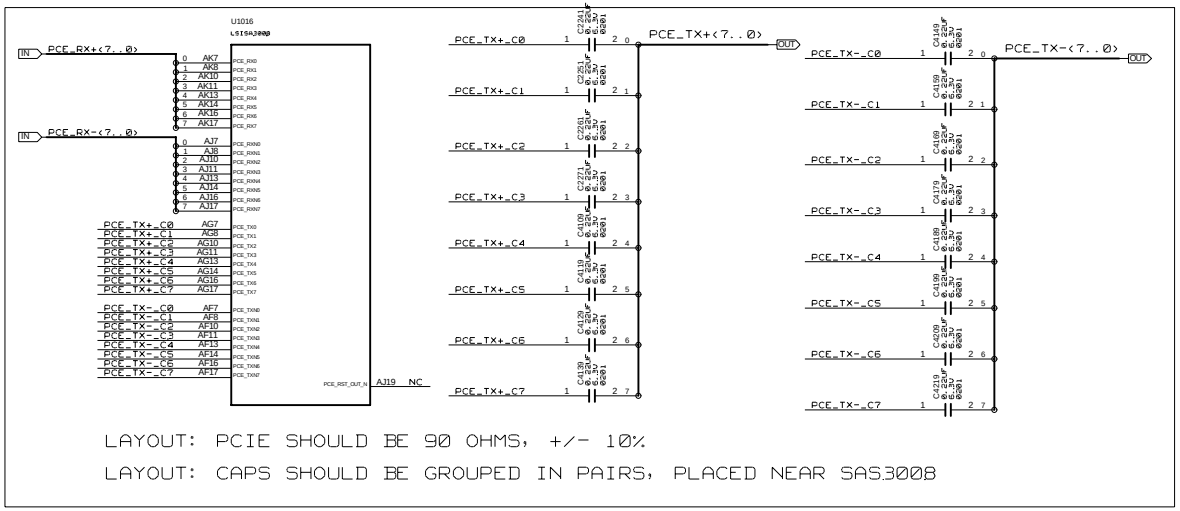

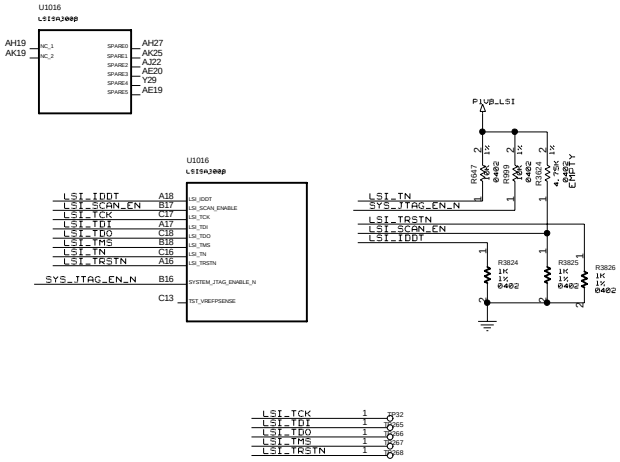

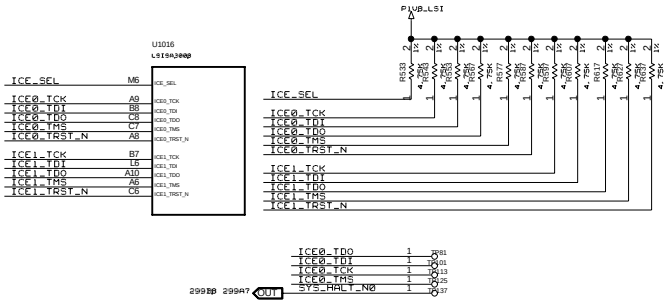

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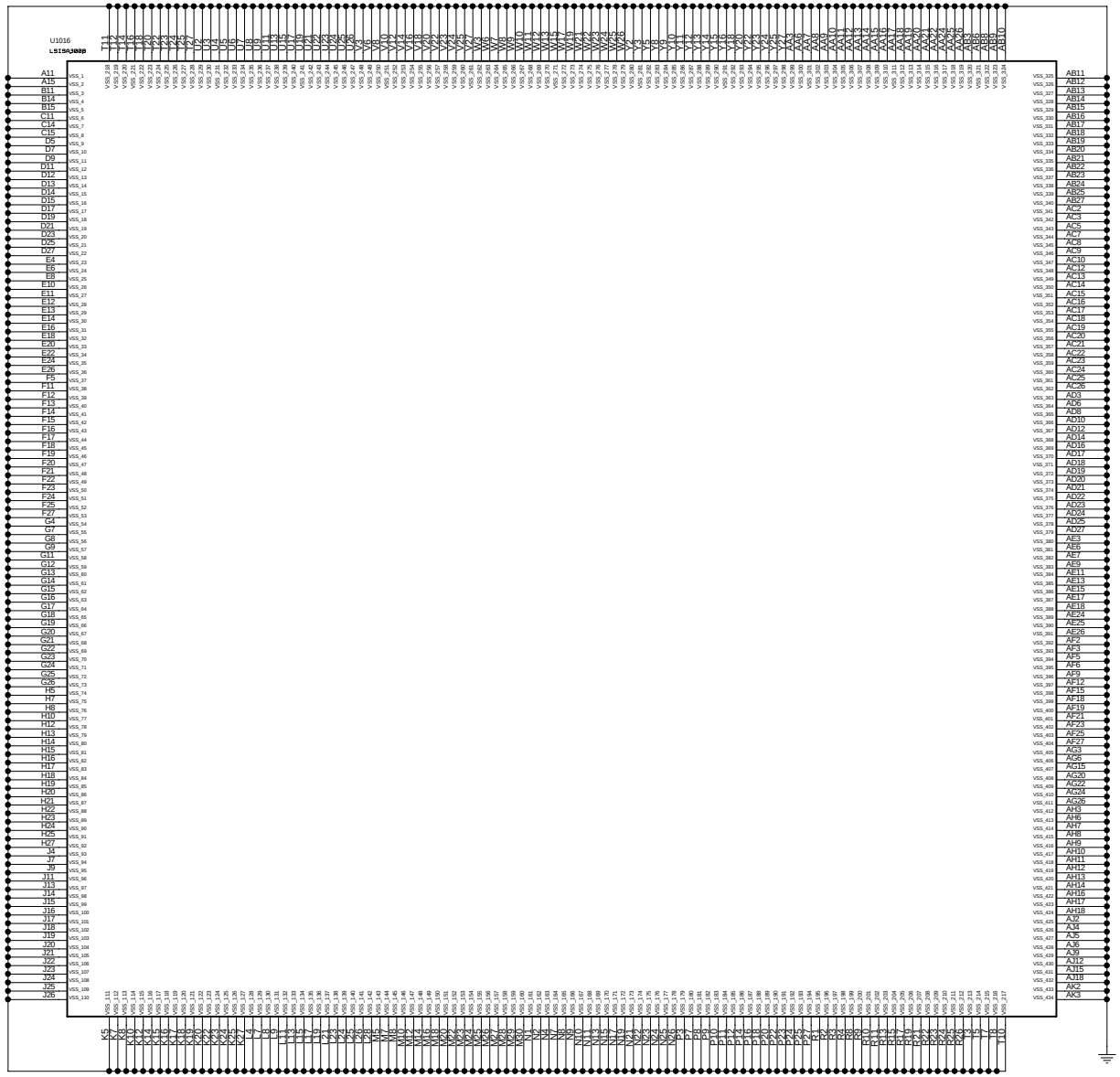
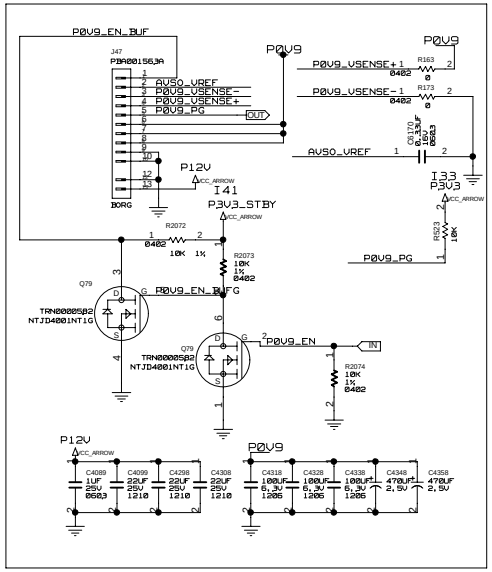
	DRAWN BY: <ENGINEER> / SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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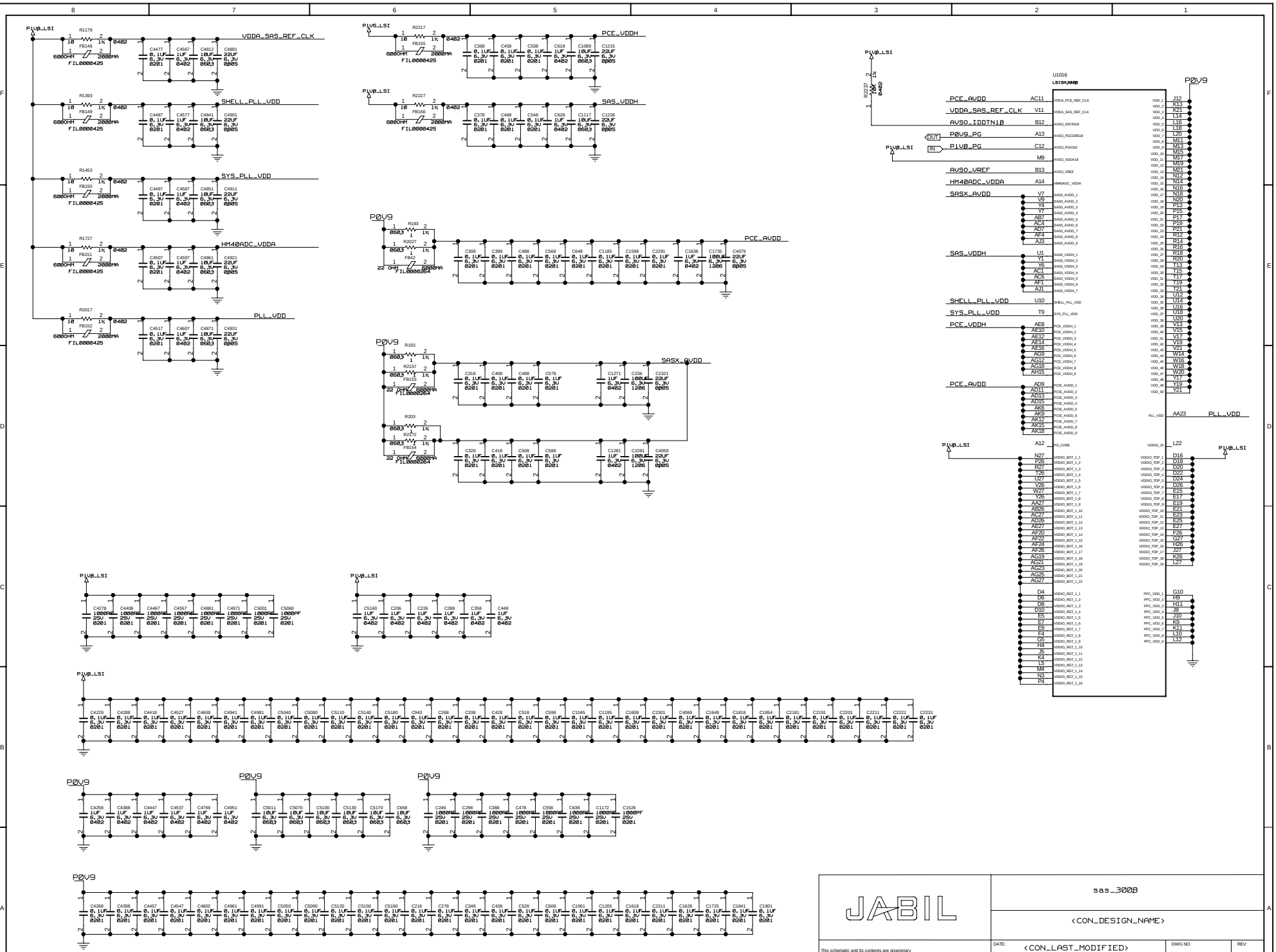
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
	REV:



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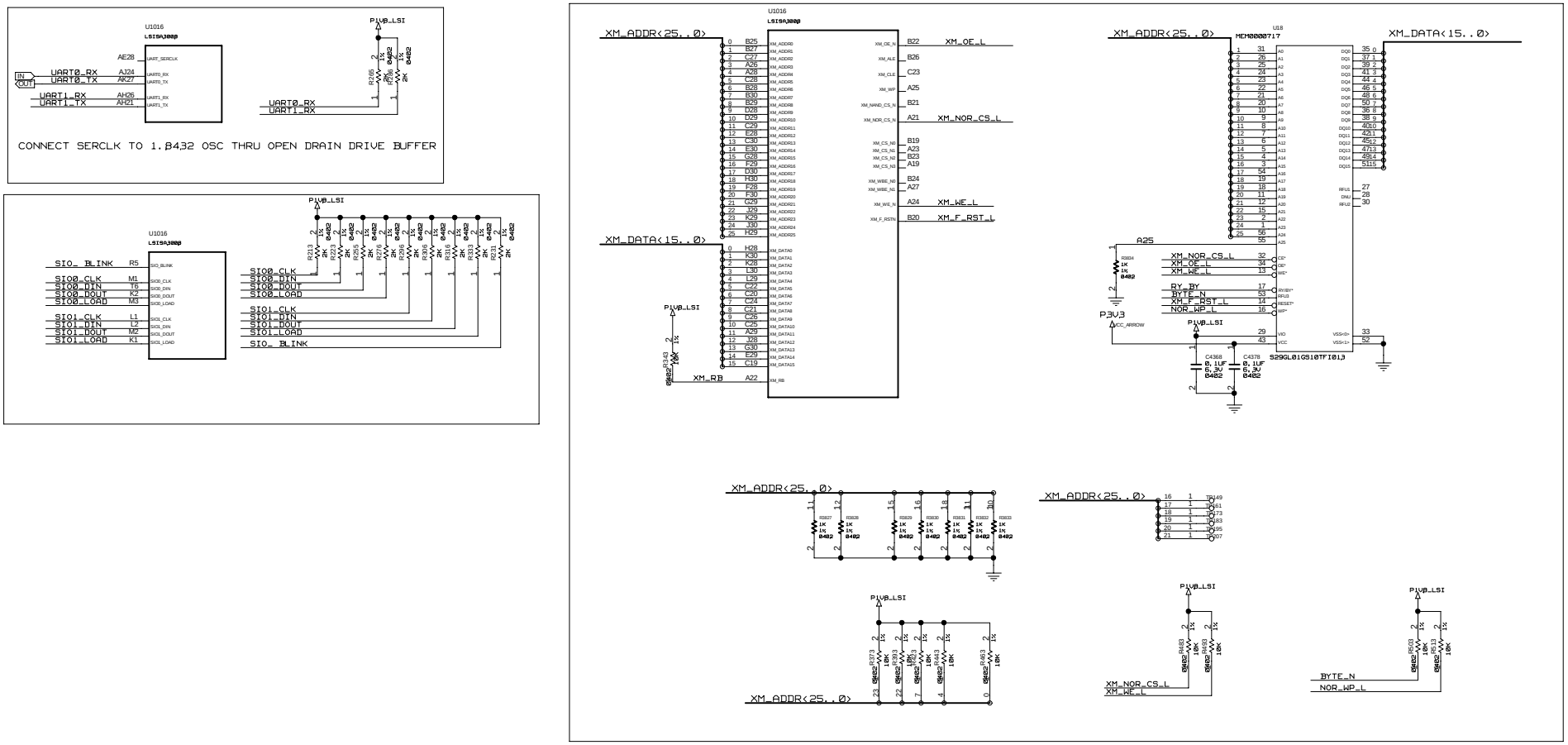

POWER-ON SENSE OPTIONS:

XM_ADDR[0]: SERIAL BOOTSTRAP LOADER ENABLE
  0: DISABLED
  1: ENABLED *

XM_ADDR[1]: SERIAL BOOTSTRAP ROM ADDRESS SELECT
  0: 0XA0 *
  1: 0XAB

XM_ADDR[2]: SERIAL BOOTSTRAP ROM BYTE ADDRESS SELECT
  0: START AT BYTE ADDRESS *
  1: START AT BYTE ADDRESS + 8'H80

XM_ADDR[4]: FUSION MESSAGE UNIT MDE
  0: I20 MODE
  1: FUSION MODE (MPT MODE) *

XM_ADDR[6:5]: PCIE MAXIMUM LINK SPEED
  00: 2.5G *
  01: 5.0G
  10: 8.0G
  11: RESERVED

XM_ADDR[7]: RESERVED FOR FUTURE USED. PULL HIGH

XM_ADDR[8]: RESERVED FOR FUTURE USED. PULL LOW

XM_ADDR[11]: DISABLE PCIE LANE 7 TO 4
  0: ENABLED *
  1: DISABLED AND POWERD DOWN

XM_ADDR[23:16]: AVSO MODE
  11XXXXXX: PASS VALUE FROM E-FUSE WITHOUT ADJUSTMENT *

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sas_300B

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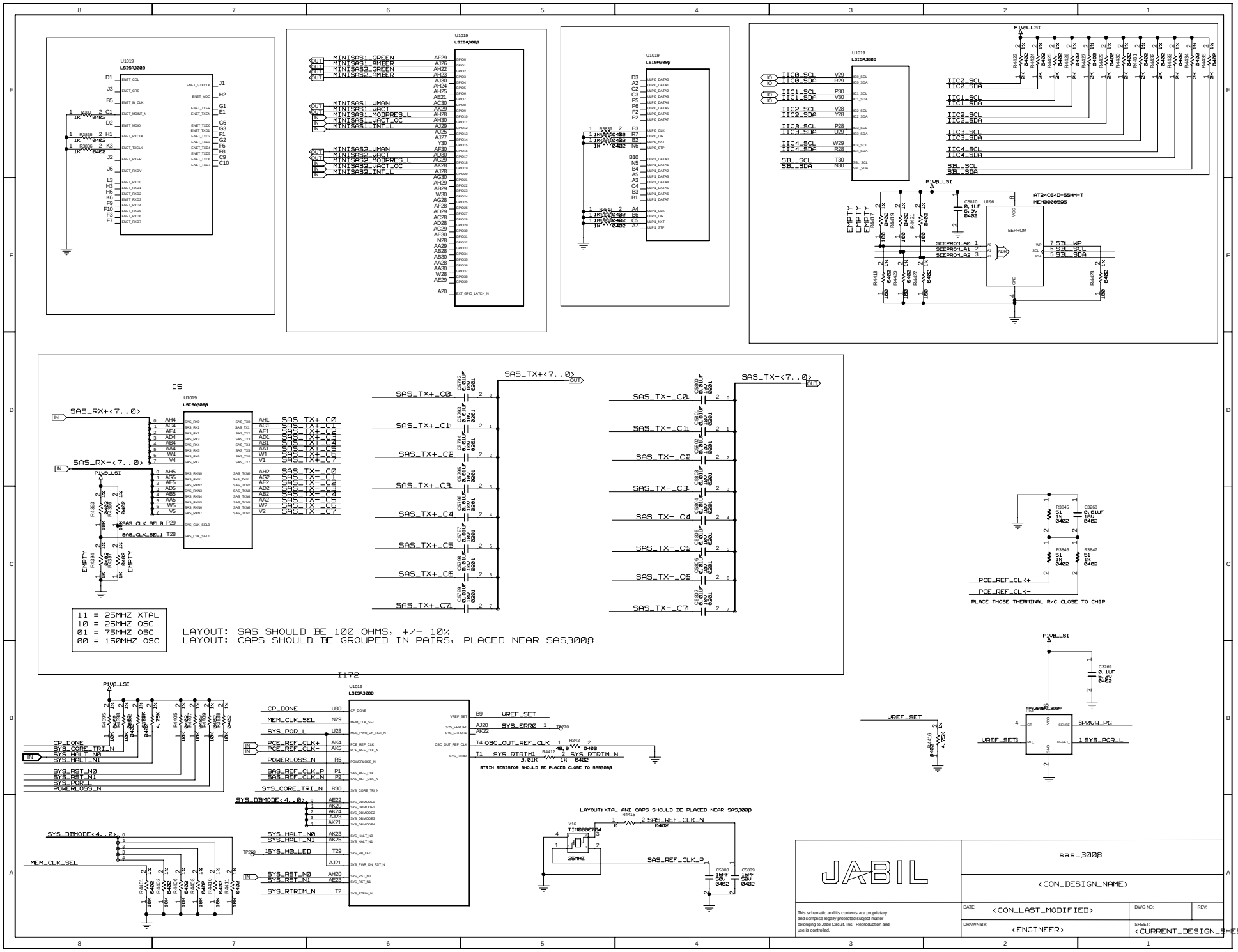
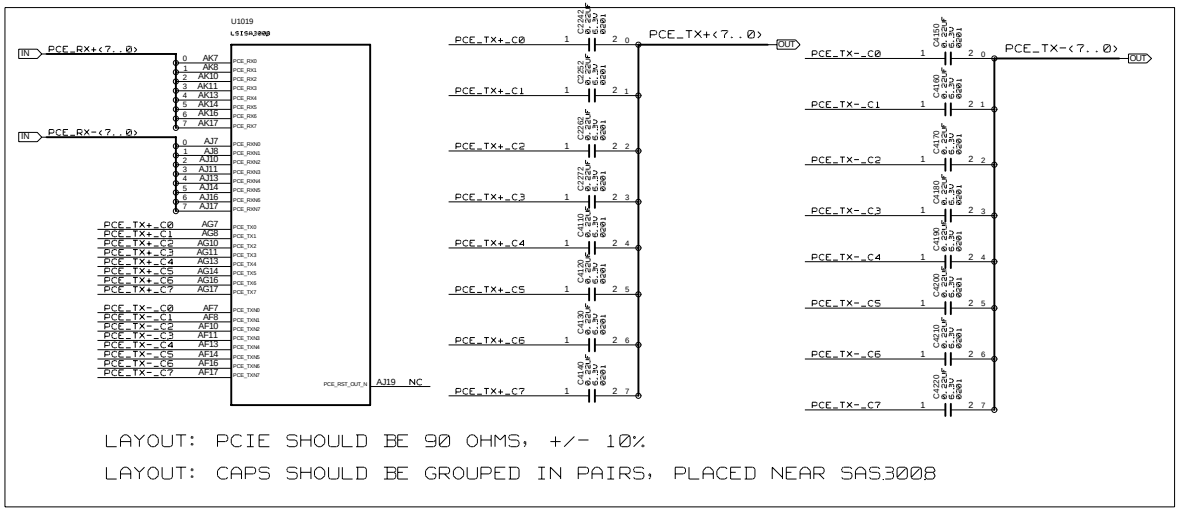
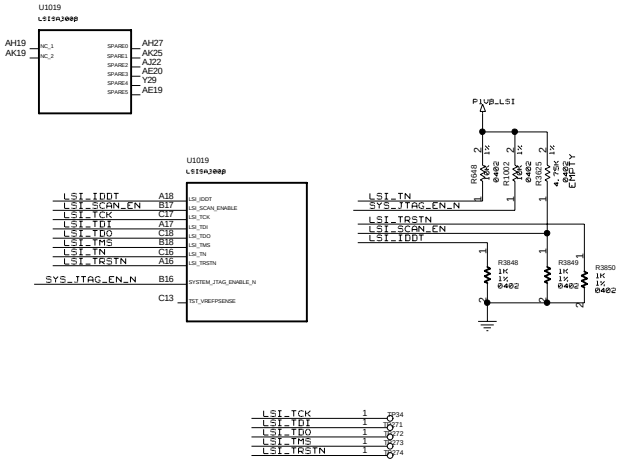
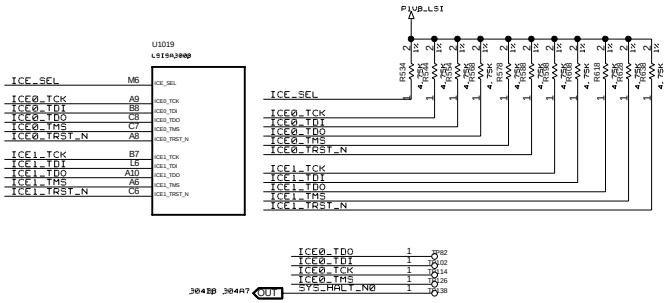
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



DO WE NEED TO CONNECT TESTMUX?







JABIL	sas_3008
	<CON_DESIGN_NAME>
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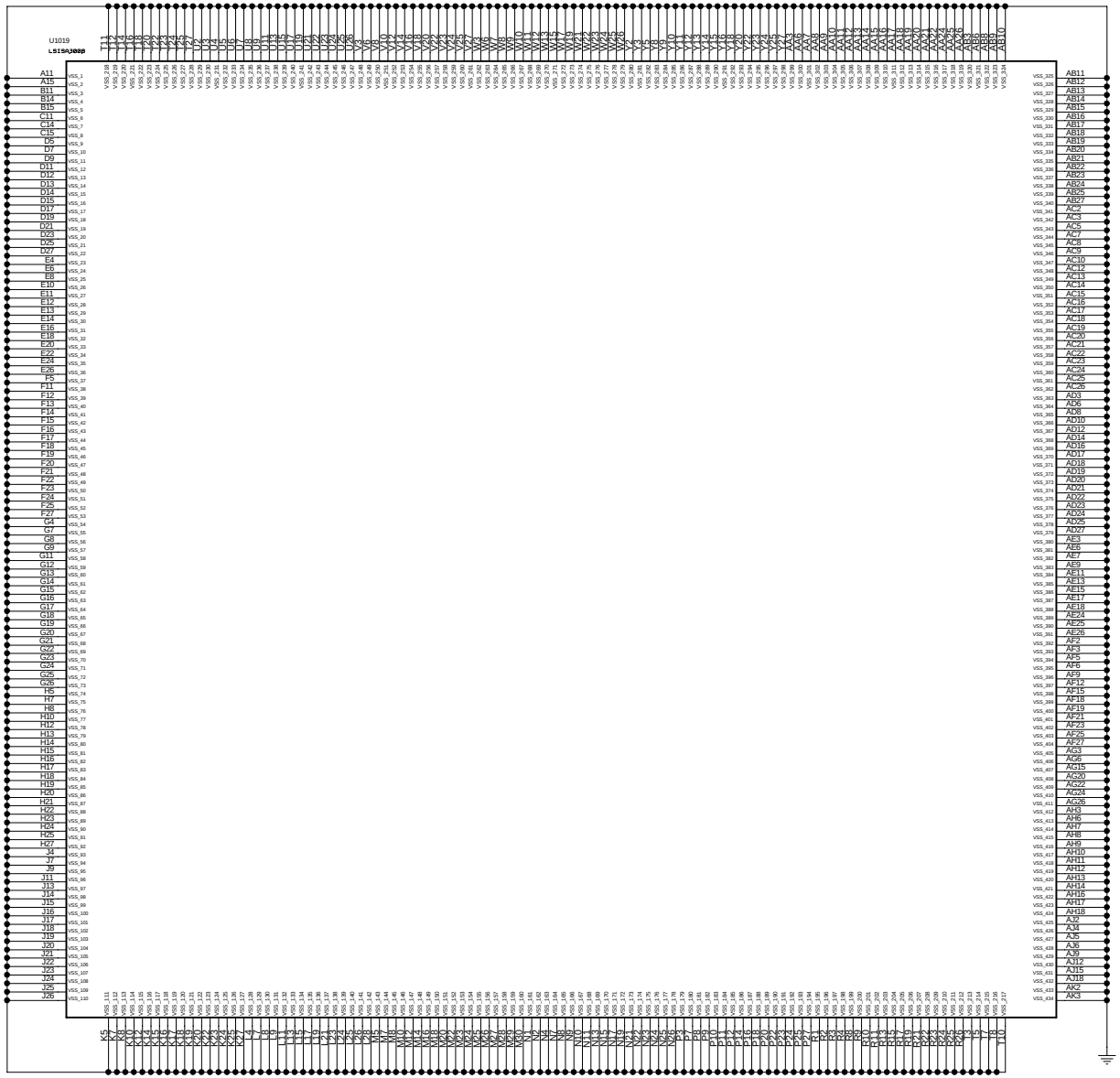
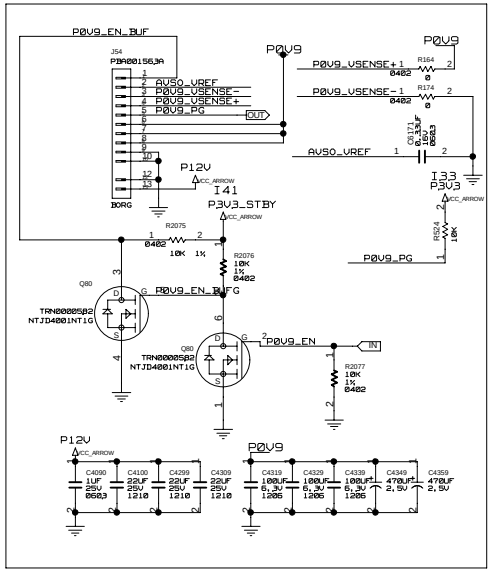
	DRAWN BY: <ENGINEER> / SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





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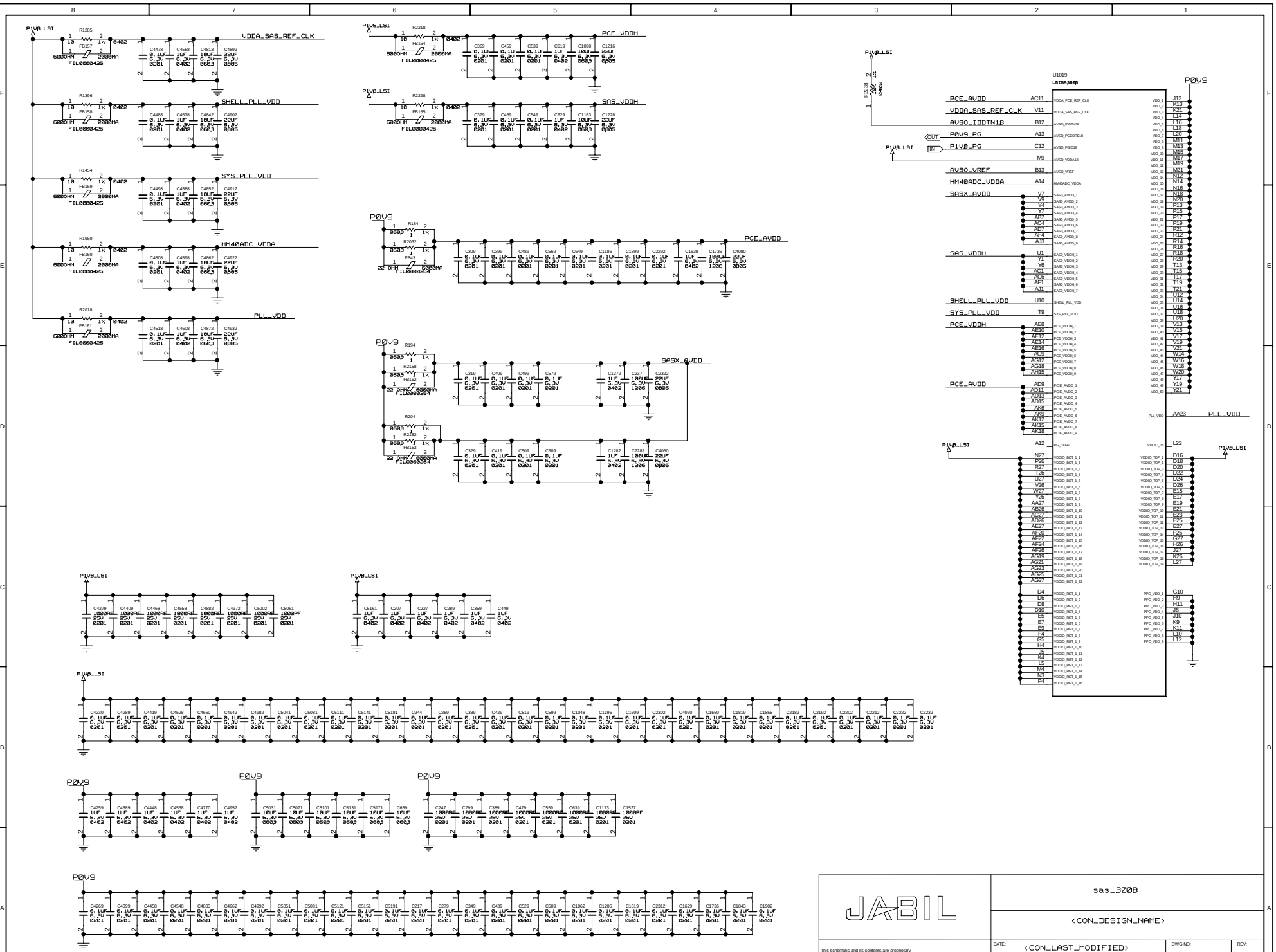
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET>OF<TOTAL_DESIGN_SHEETS>	



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JABIL

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<CON_DESIGN_NAME>

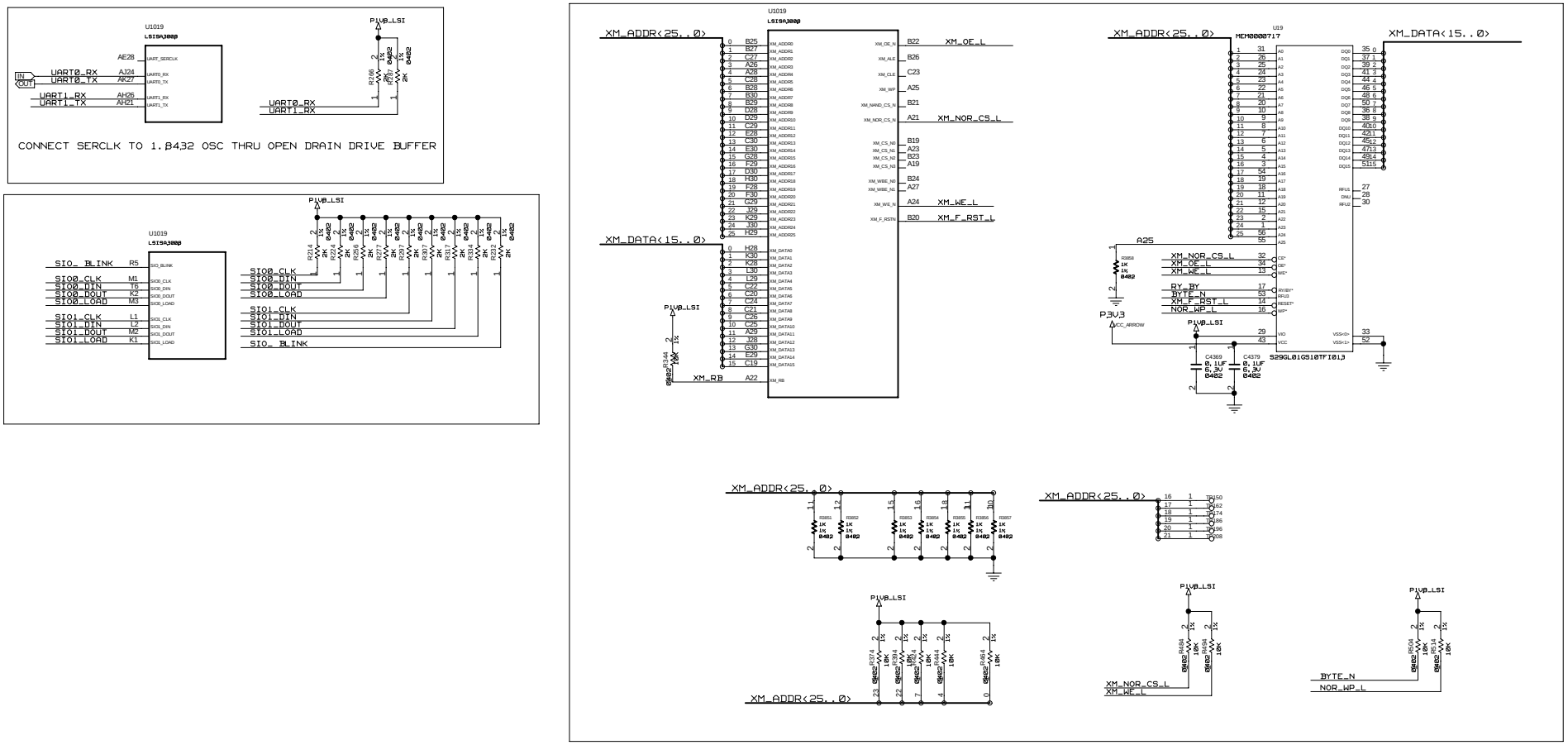
DATE: <CON_LAST_MODIFIED>

DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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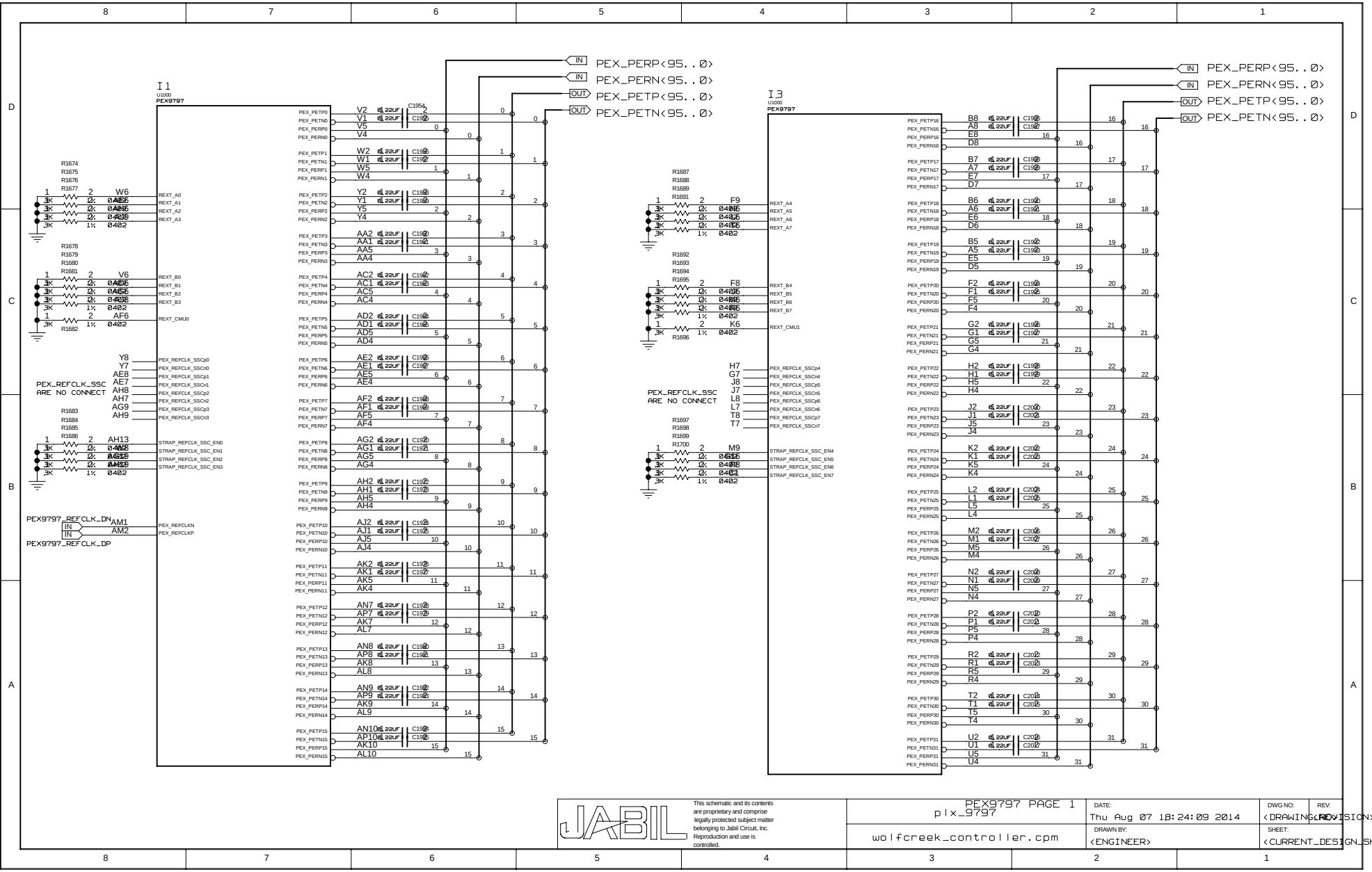
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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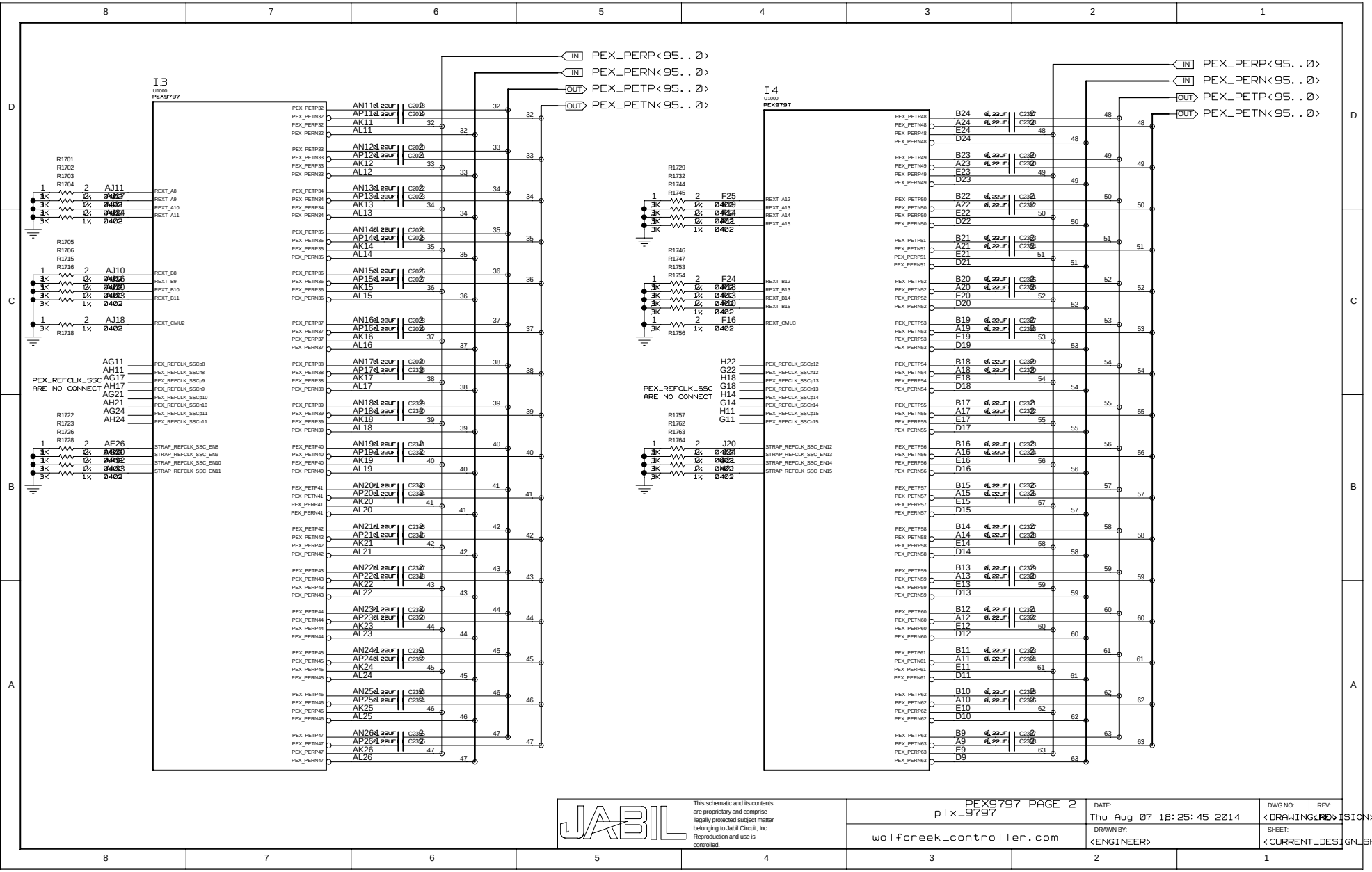
PEX9797 PAGE 1 plx_9797	DATE: Thu Aug 07 18:24:09 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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PEX9797 PAGE 2
plx_9797

wolfcreek_controller.cpm

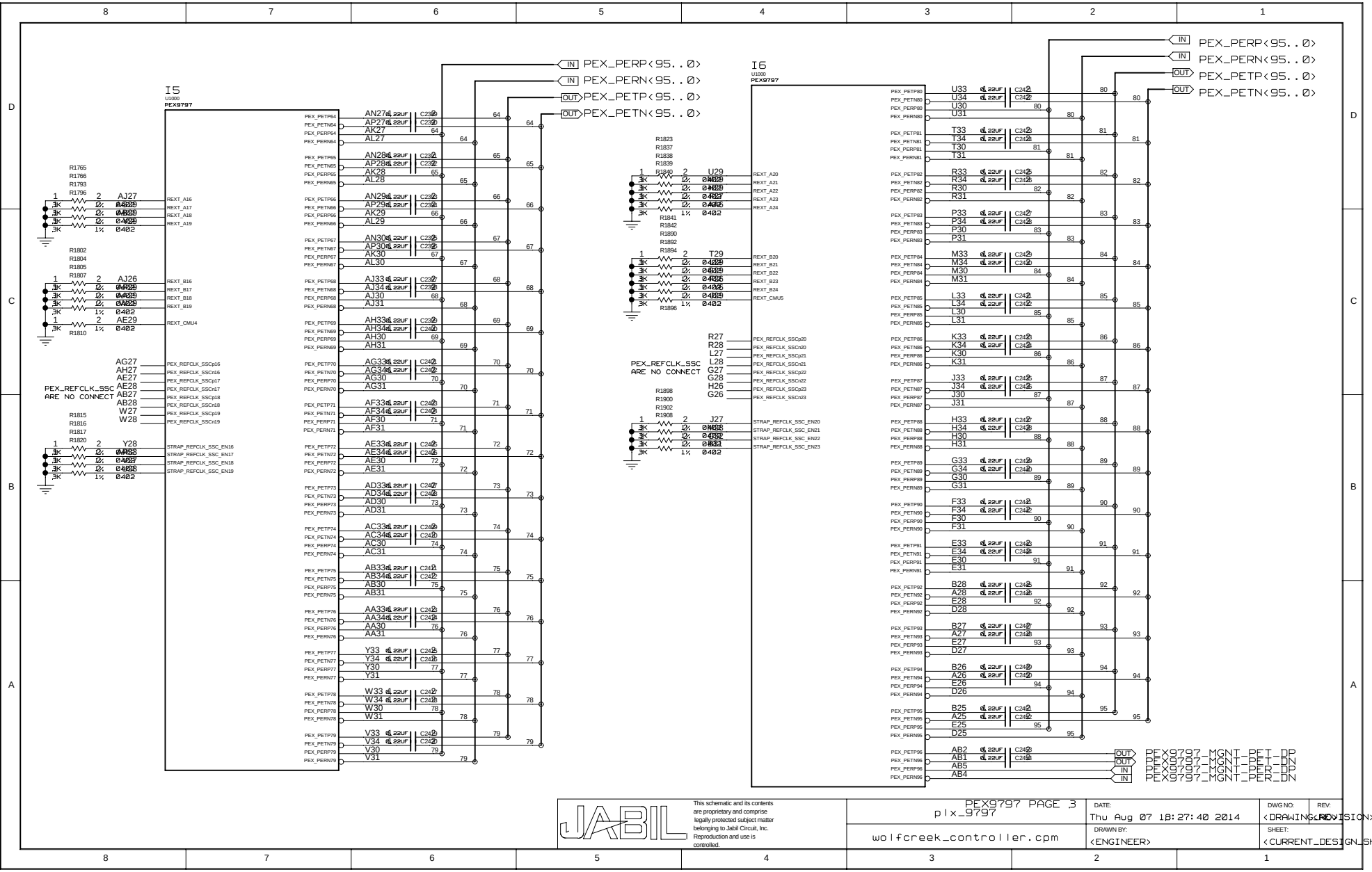
DATE: Thu Aug 07 18:25:45 2014

DRAWN BY: <ENGINEER>

DWG NO: <DRAWING_NO>

REV: <REVISION>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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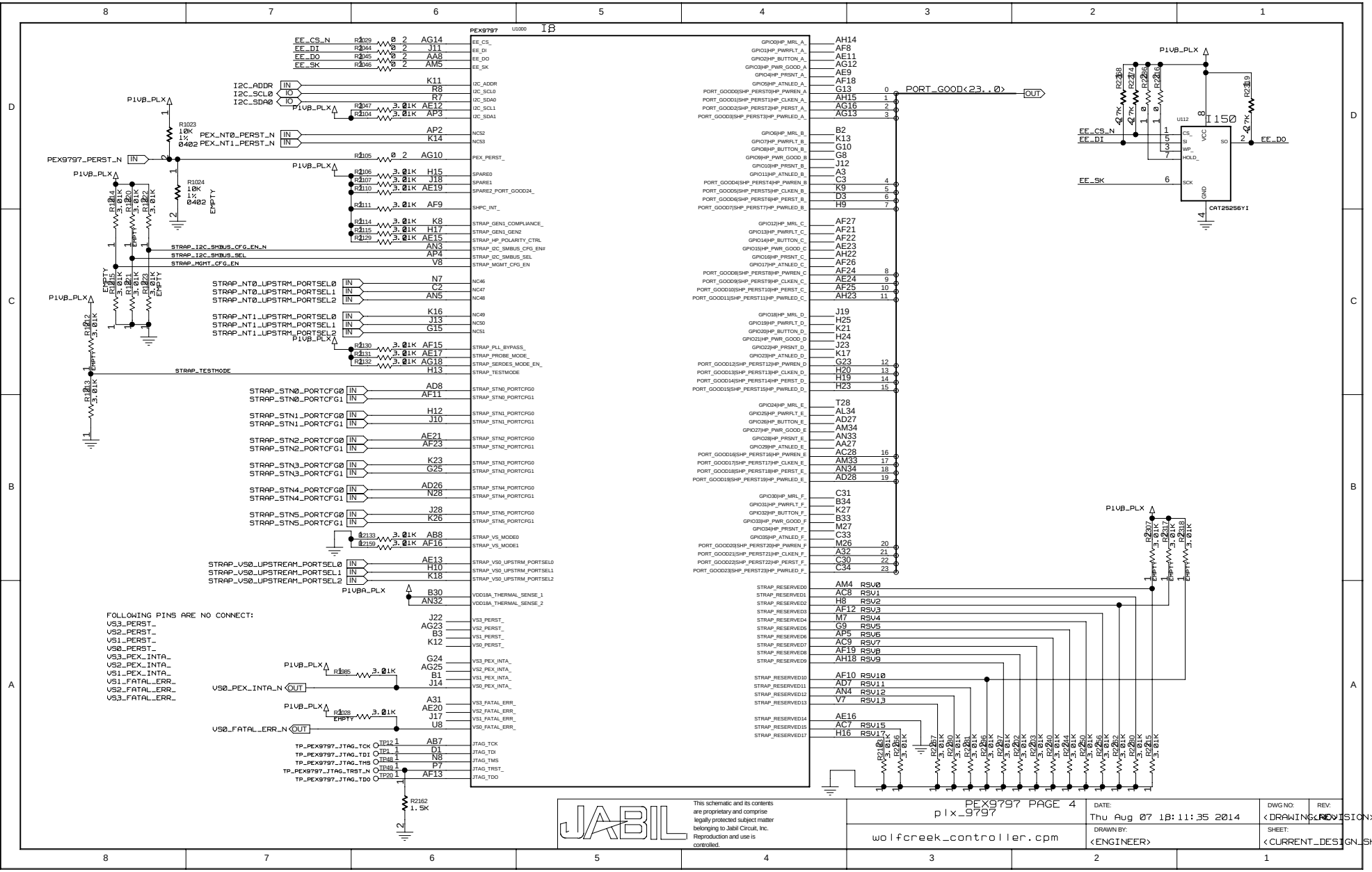
PEX9797 PAGE 3 plx_9797	DATE: Thu Aug 07 18:27:40 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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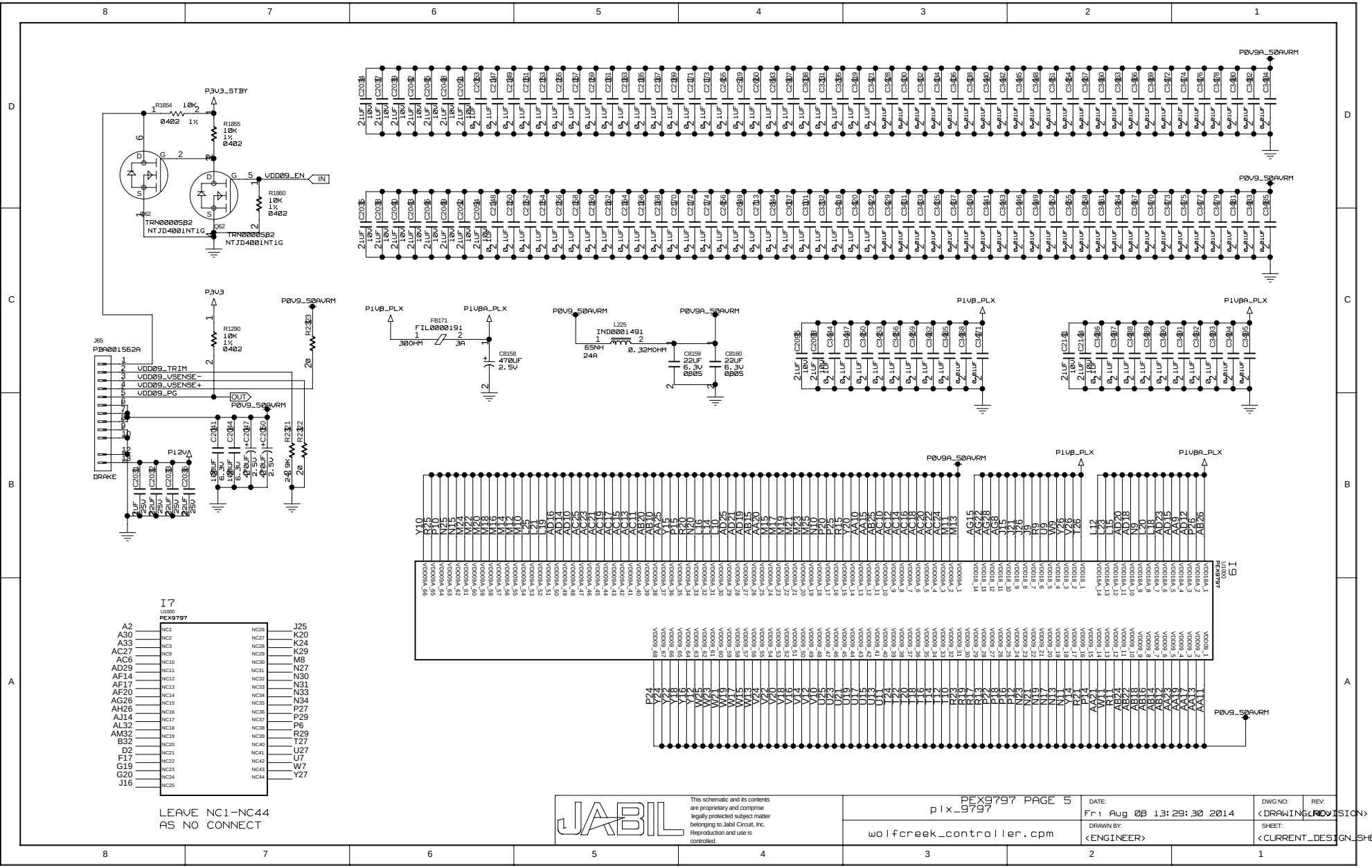
PEX9797 PAGE 4	DATE: Thu Aug 07 18:11:35 2014	DWG NO: <DRAWING>	REV: <REVISION>
plx_9797			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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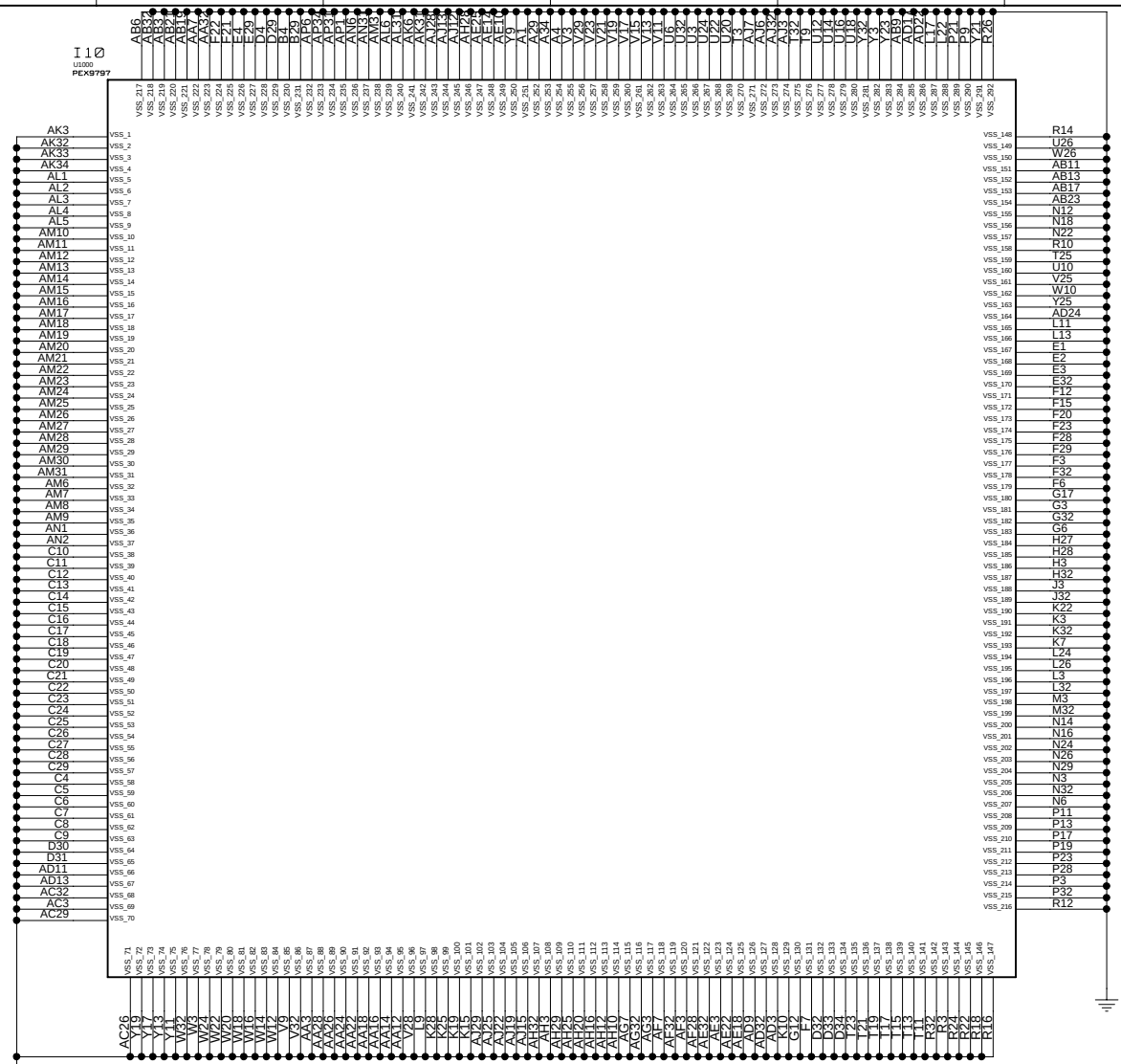
PEX9797 PAGE 5 plx_9797	DATE: Fri Aug 08 13:29:30 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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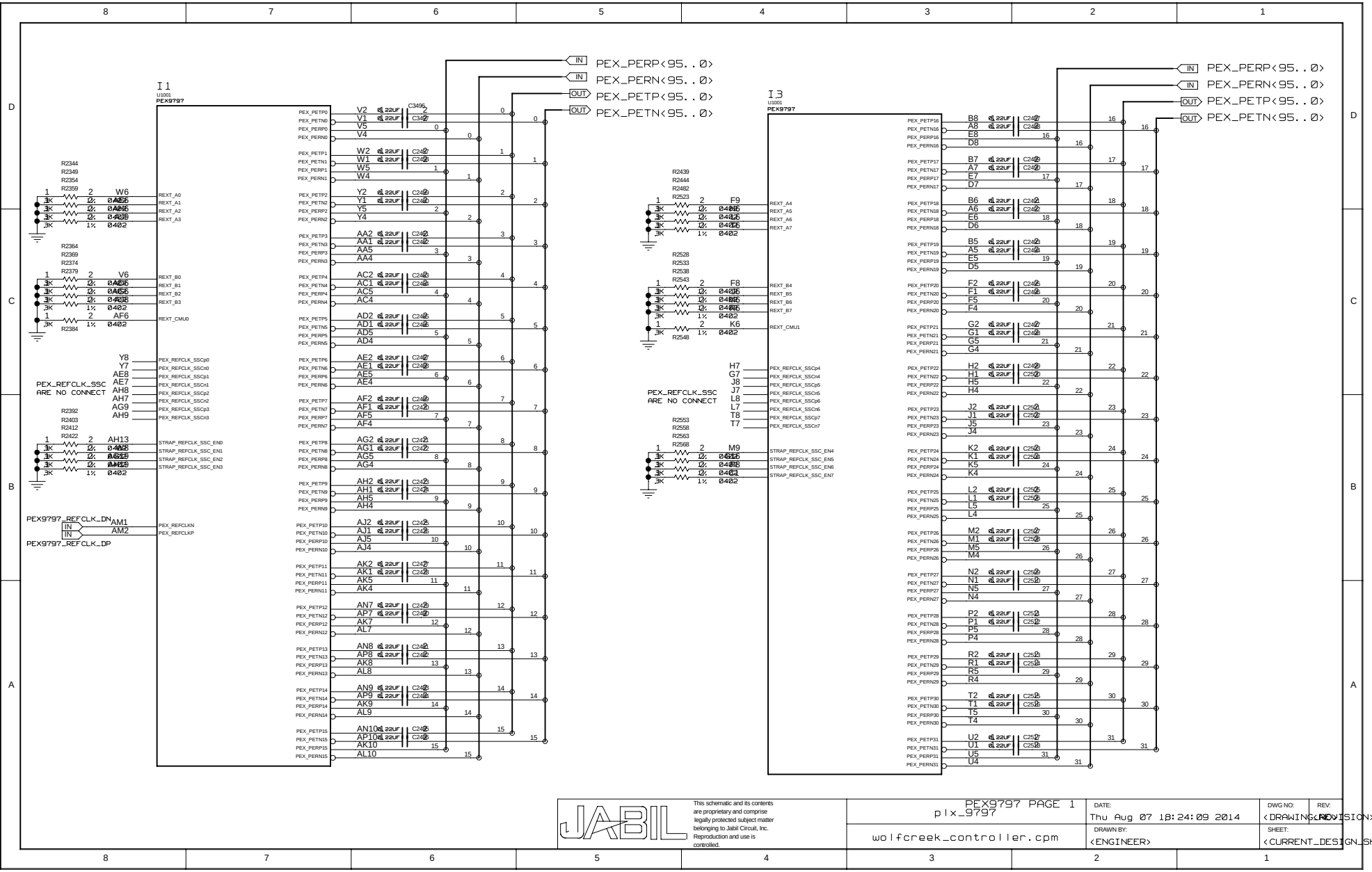
PEX9797 PAGE 6 plx_9797	DATE: Sat Aug 02 14:44:15 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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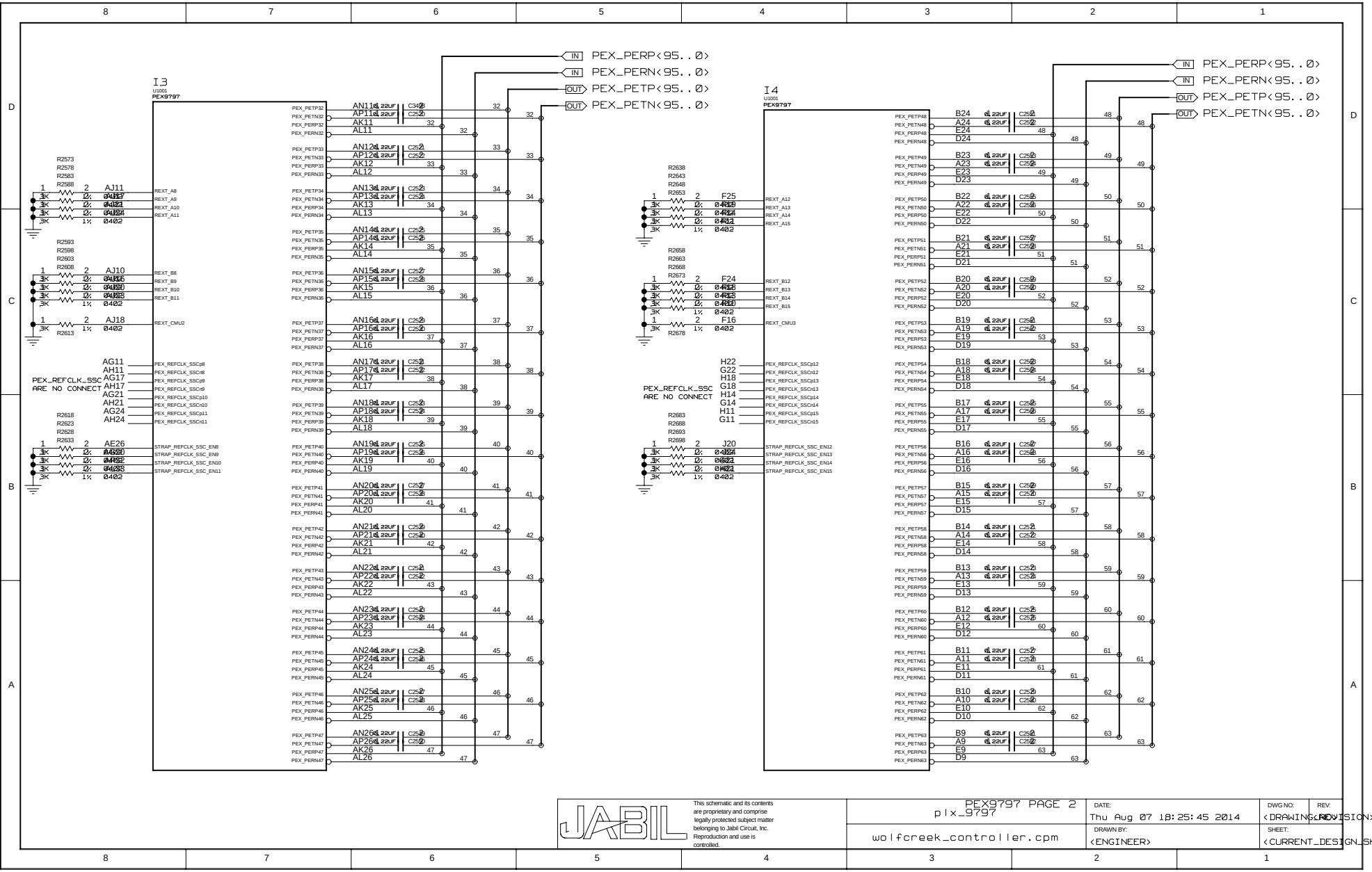
PEX9797 PAGE 1 plx_9797	DATE: Thu Aug 07 18:24:09 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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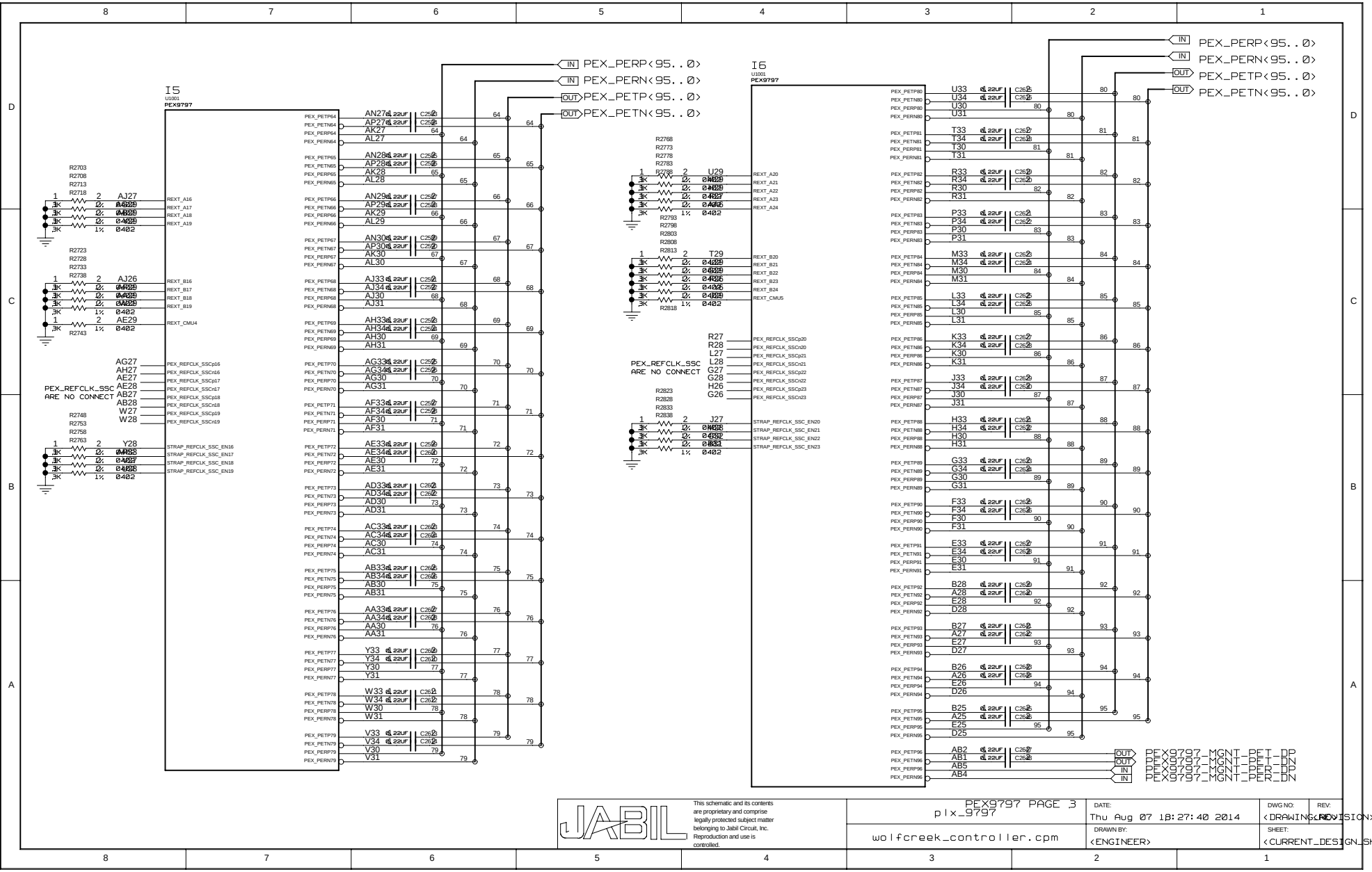
PEX9797 PAGE 2	DATE: Thu Aug 07 18:25:45 2014	DWG NO: <DRAWING>	REV: <REVISION>
plx_9797			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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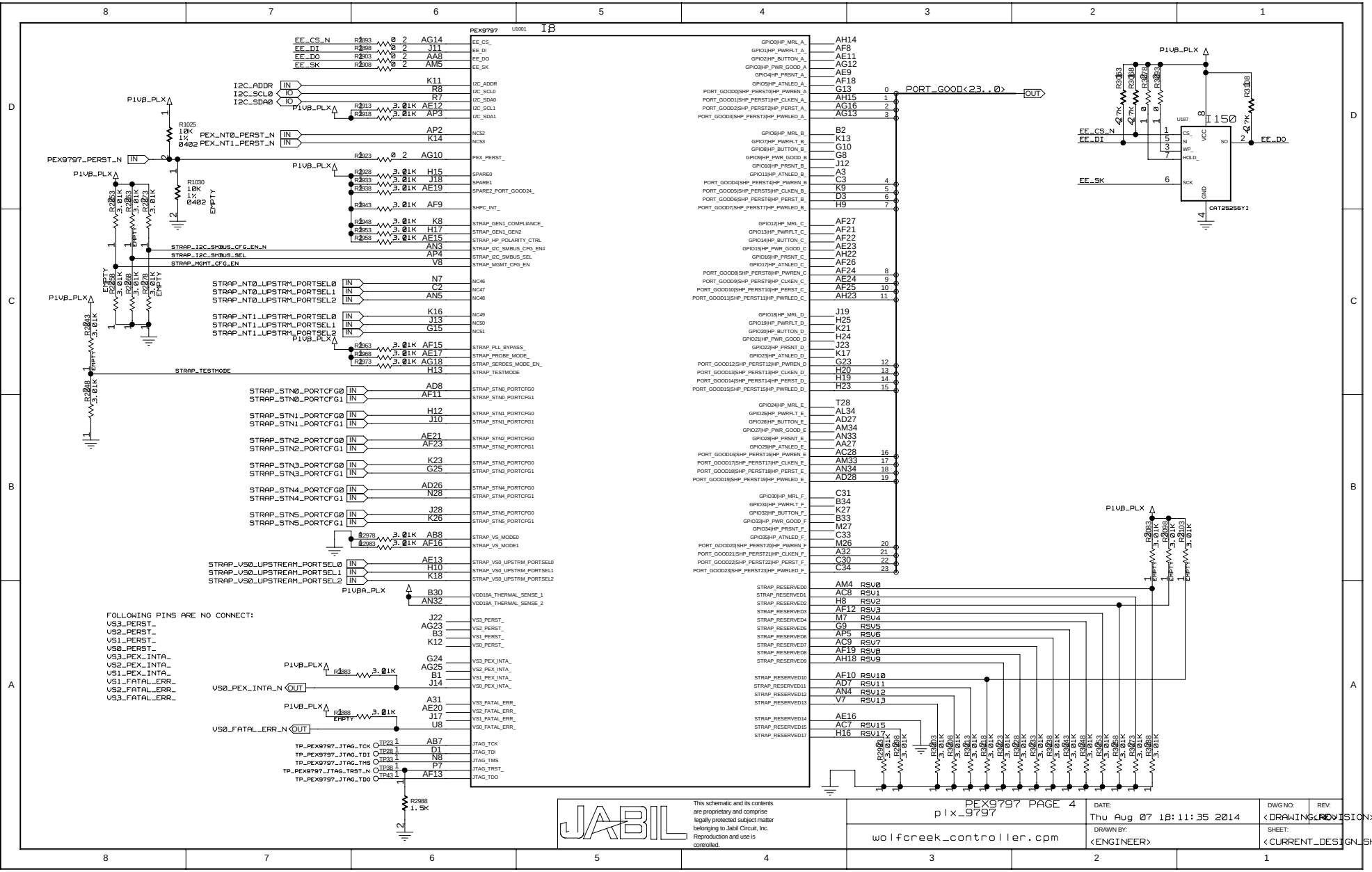
PEX9797 PAGE 3 plx_9797	DATE: Thu Aug 07 18:27:40 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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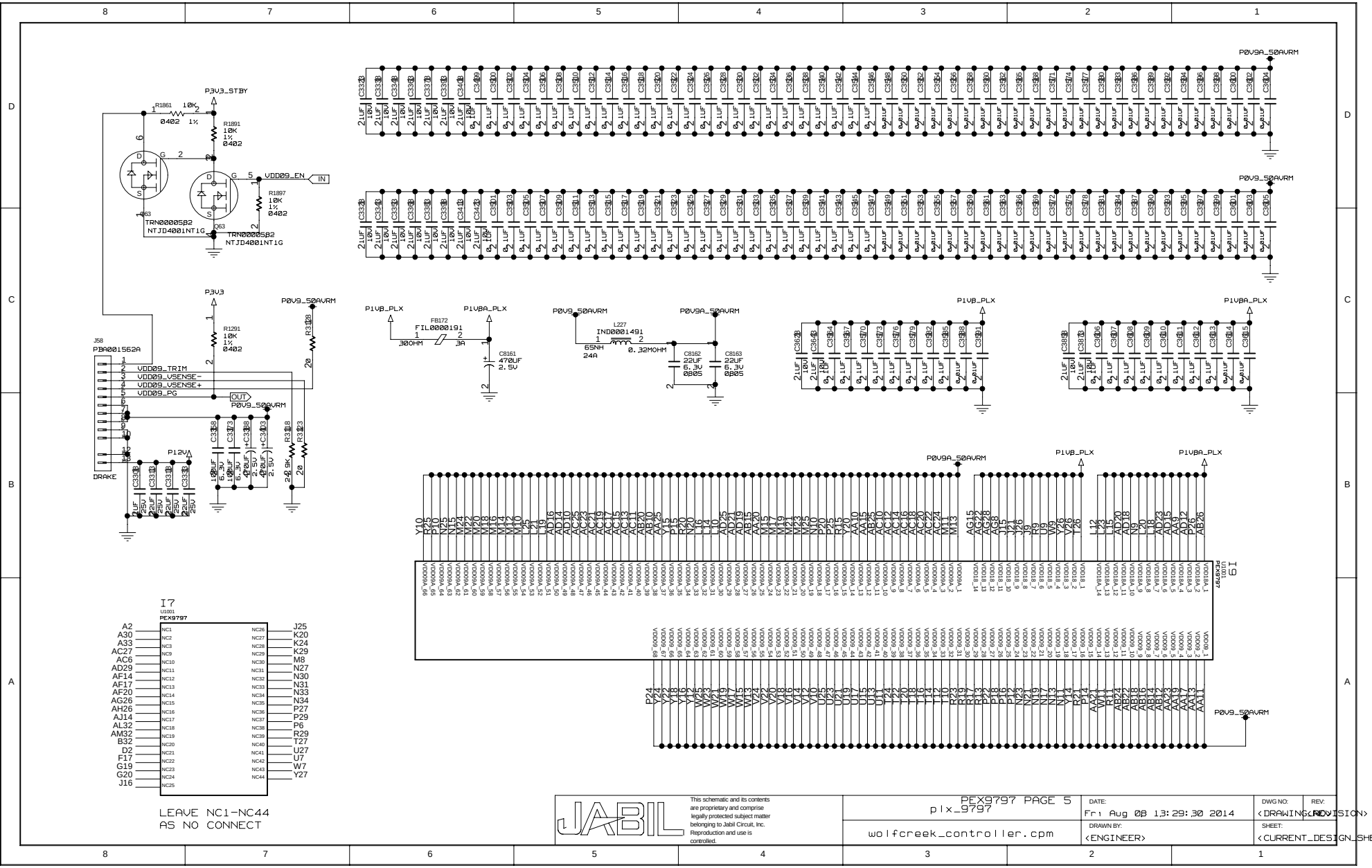
PEX9797 PAGE 4	DATE: Thu Aug 07 18:11:35 2014	DWG NO: <DRAWING>	REV: <REVISION>
plx_9797			
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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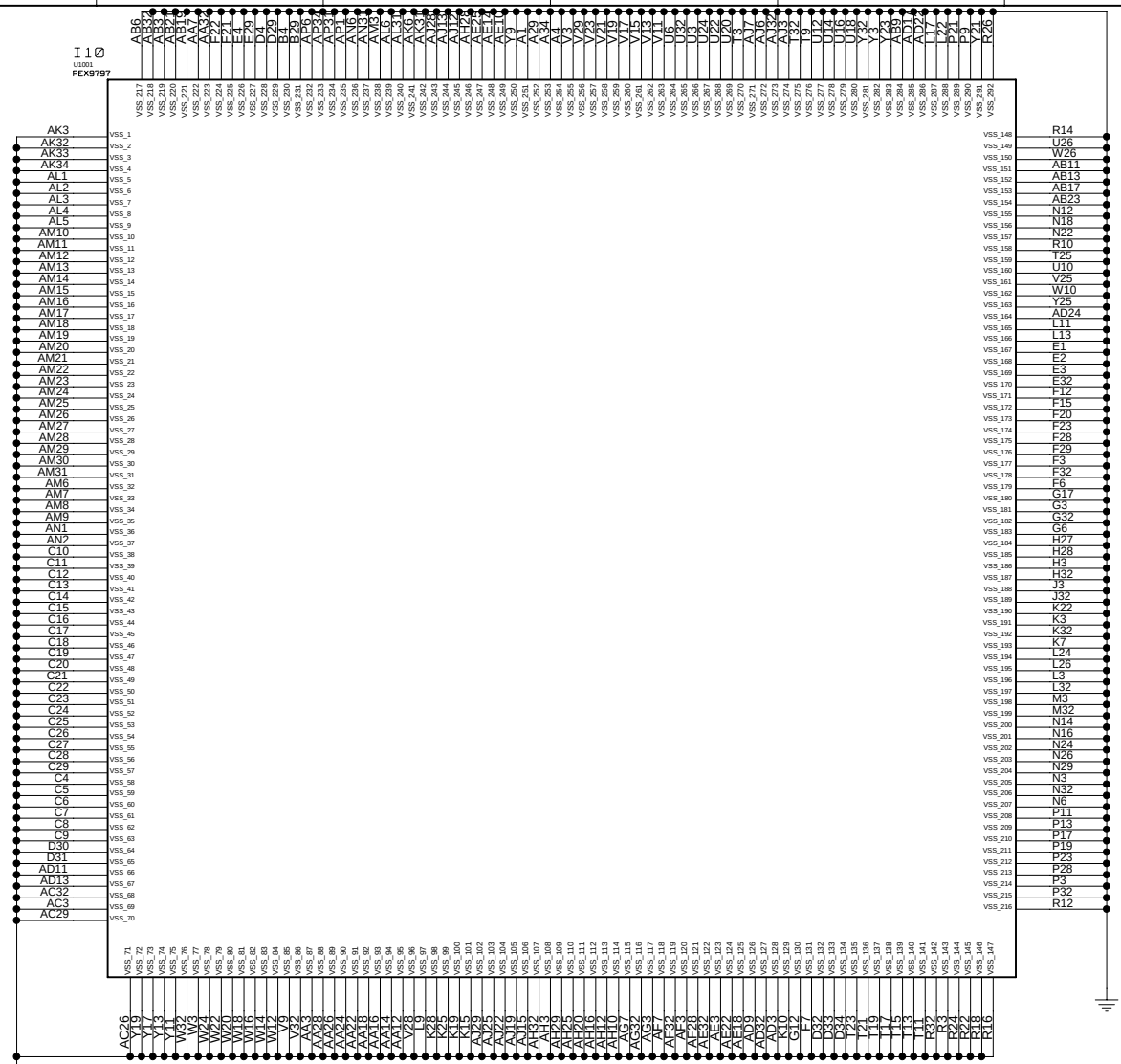
PEX9797 PAGE 5 plx_9797	DATE: Fri Aug 08 13:29:30 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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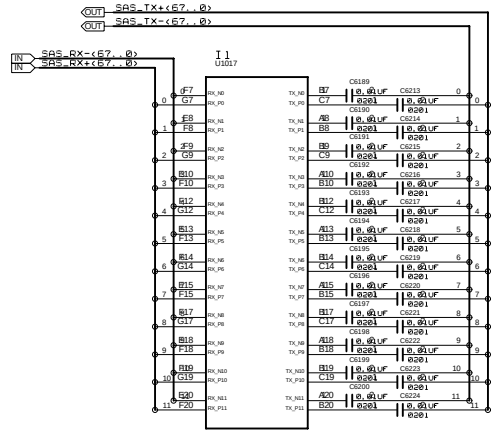
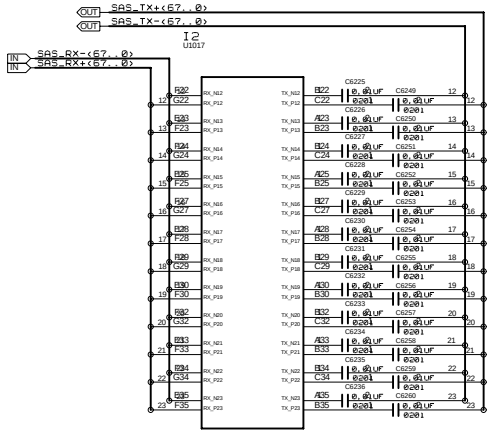
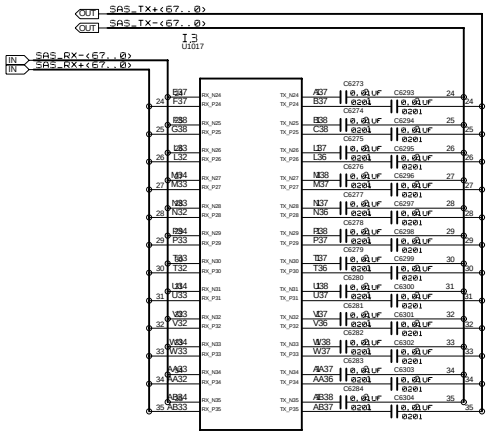
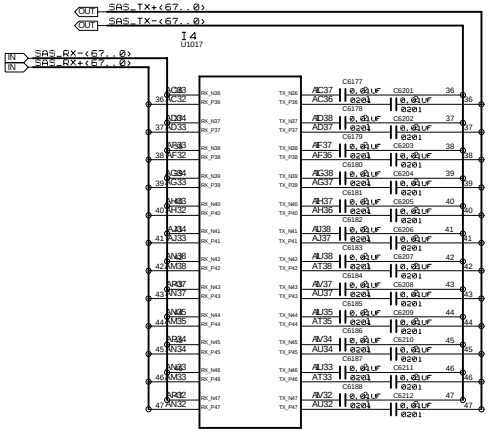
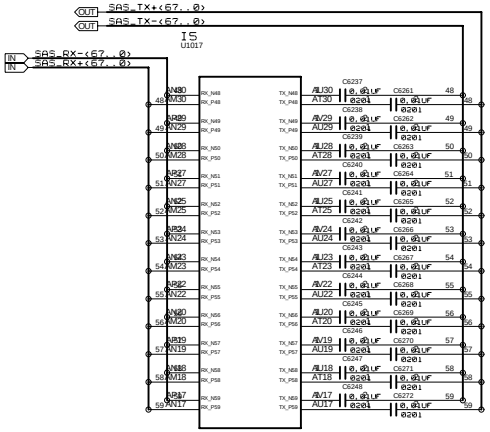
PEX9797 PAGE 6 plx_9797	DATE: Sat Aug 02 14:44:15 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	

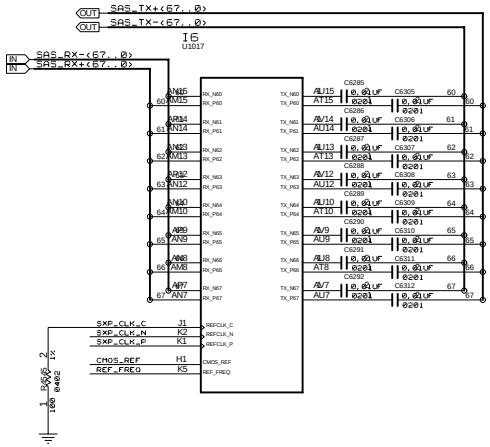


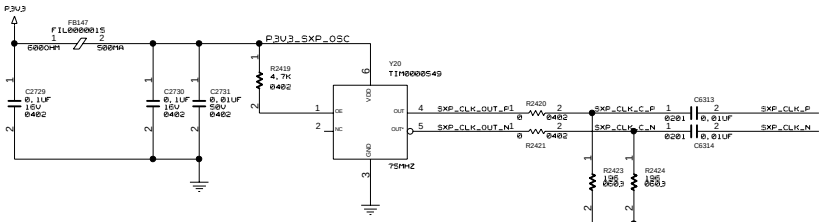


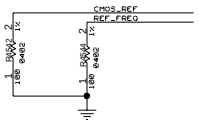












COMS_REF:
LOW: REFCLK_P/N AS CLOCK INPUT *
HIGH: REFCLK_C AS CLOCK INPUT

REF_FREQ:
LOW: 75MHZ *
HIGH: 150MHZ

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pm8056b_block

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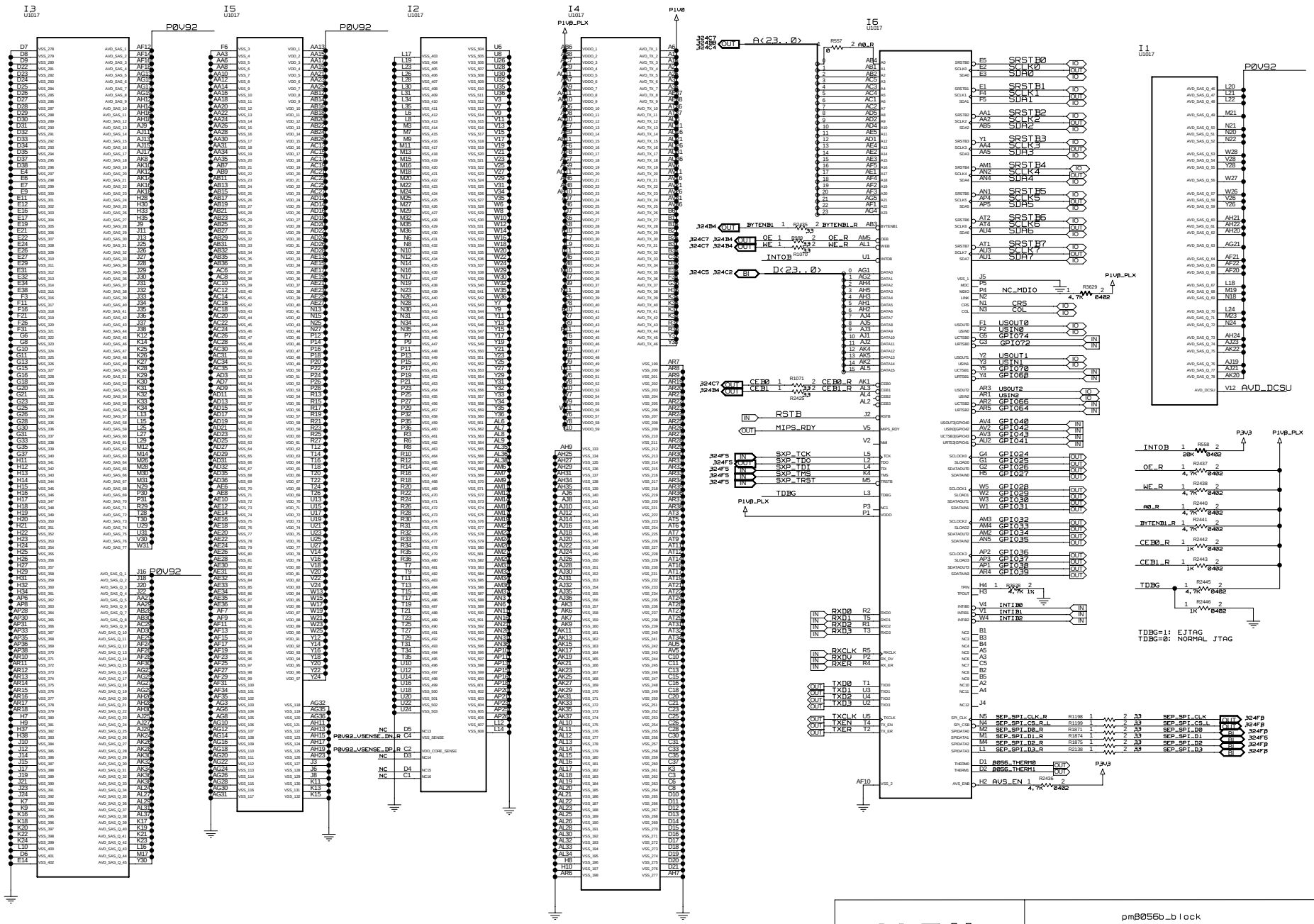
DRAWN BY: <ENGINEER>		SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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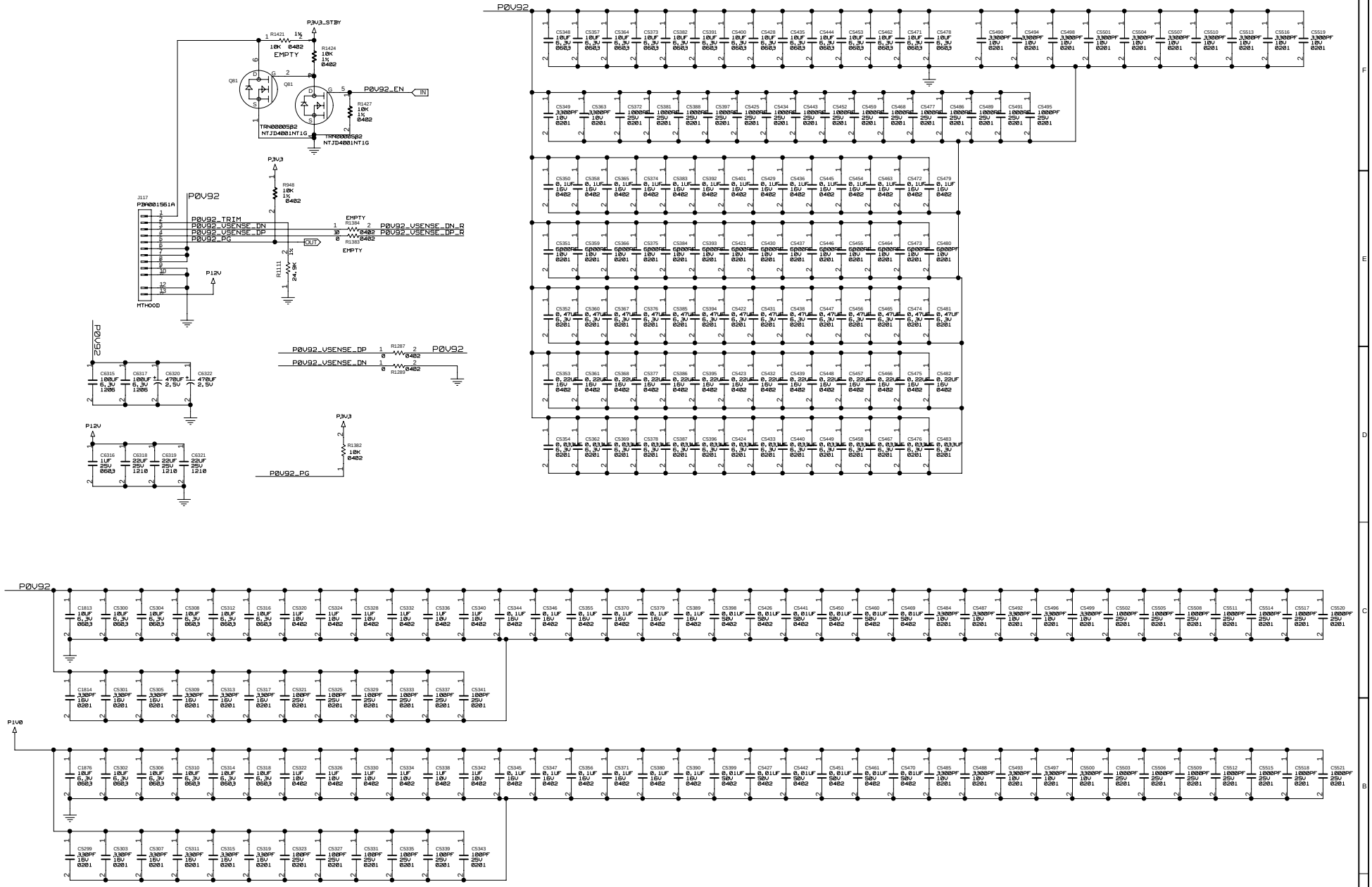
pm8056b_block

<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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pm8056b_block

<CON_DESIGN_NAME>

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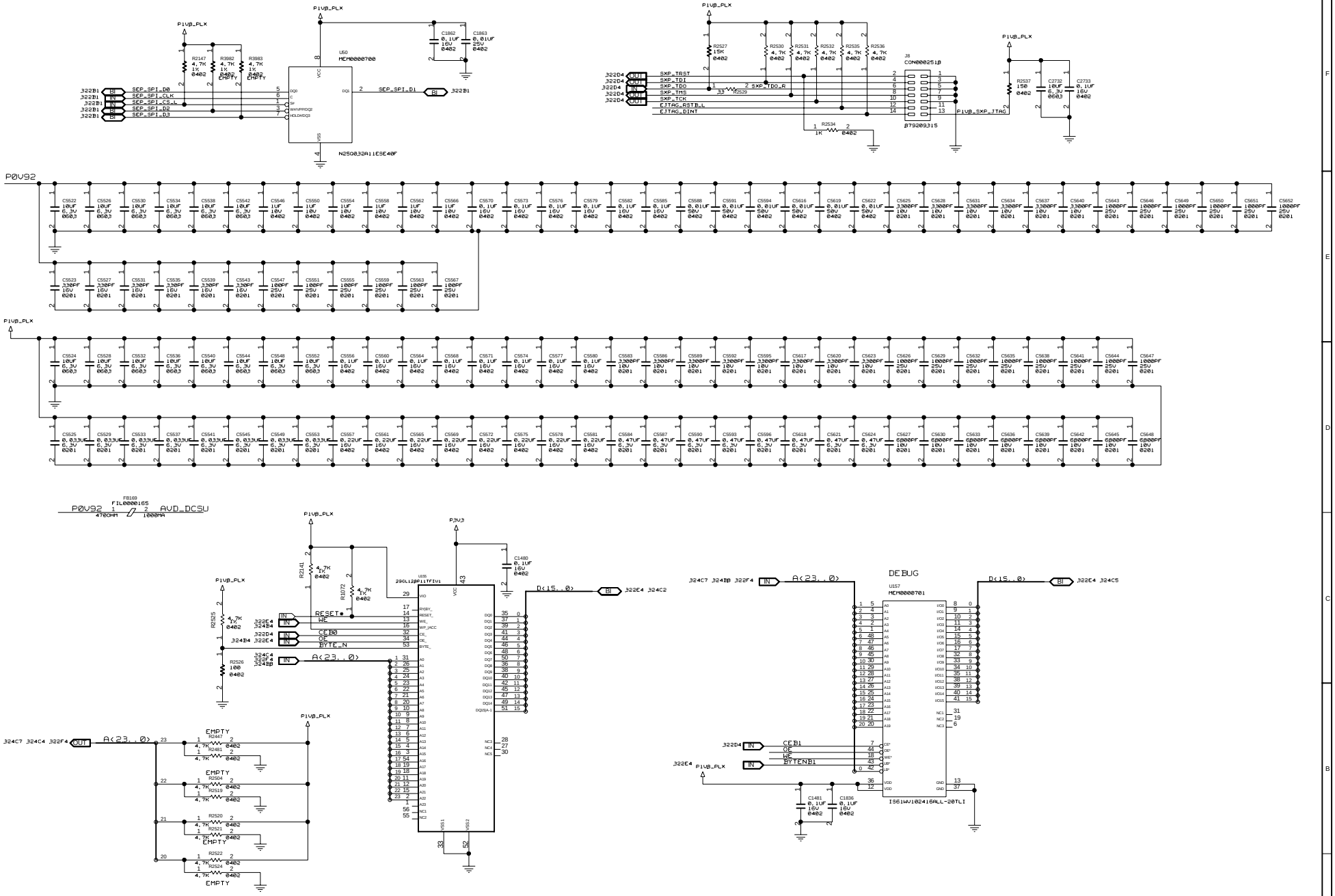
DATE: <CON_LAST_MODIFIED>	DWG NO:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	

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pm8056b_block

<CON_DESIGN_NAME>

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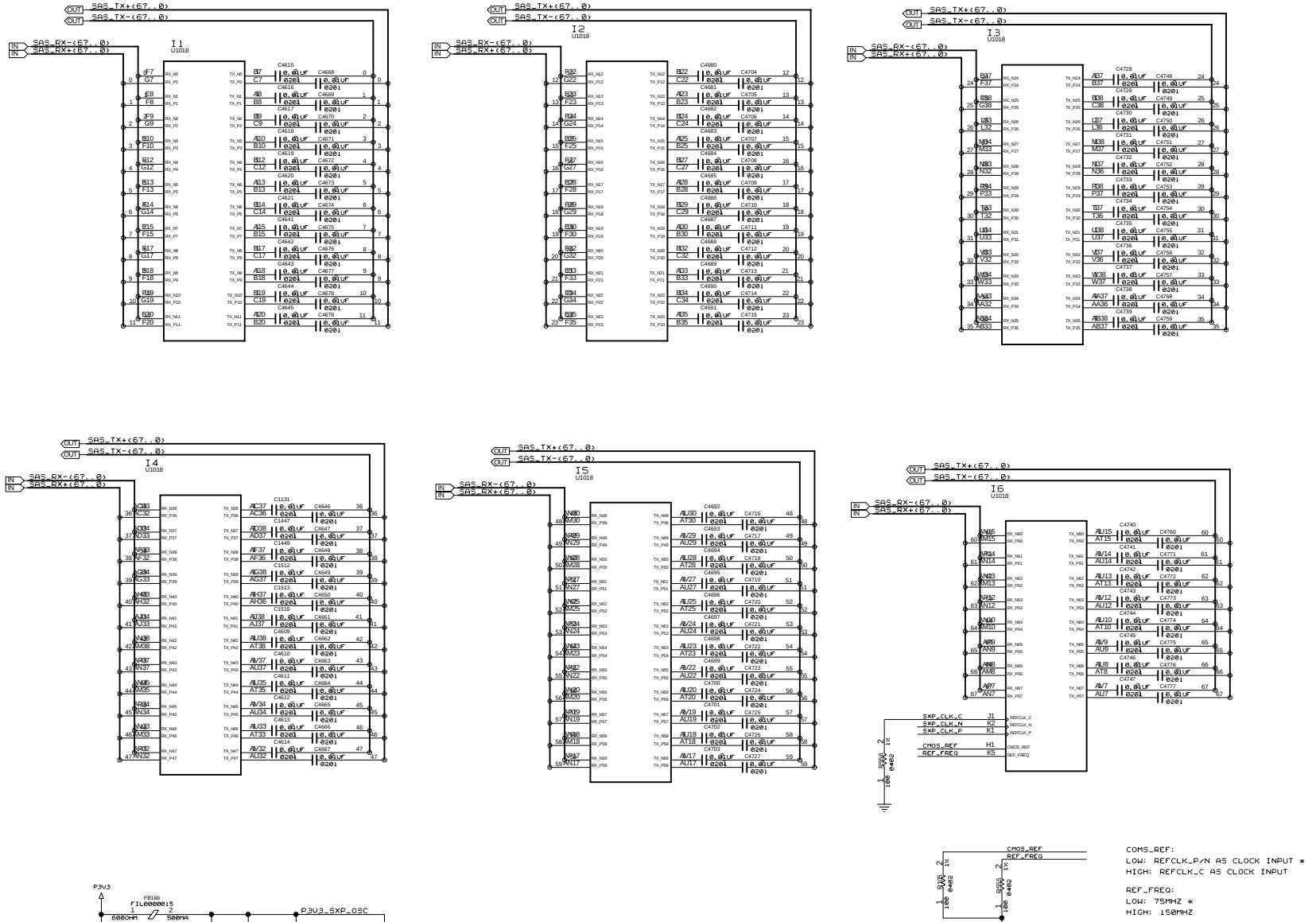
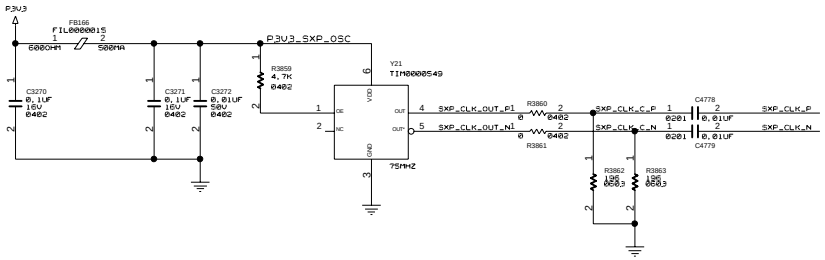
DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET>OF<TOTAL_DESIGN_SHEETS>	





COMS_REF:
LOW: REFCLK_P/N AS CLOCK INPUT *
HIGH: REFCLK_C AS CLOCK INPUT

REF_FREQ:
LOW: 75MHZ *
HIGH: 150MHZ

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<CON_DESIGN_NAME>

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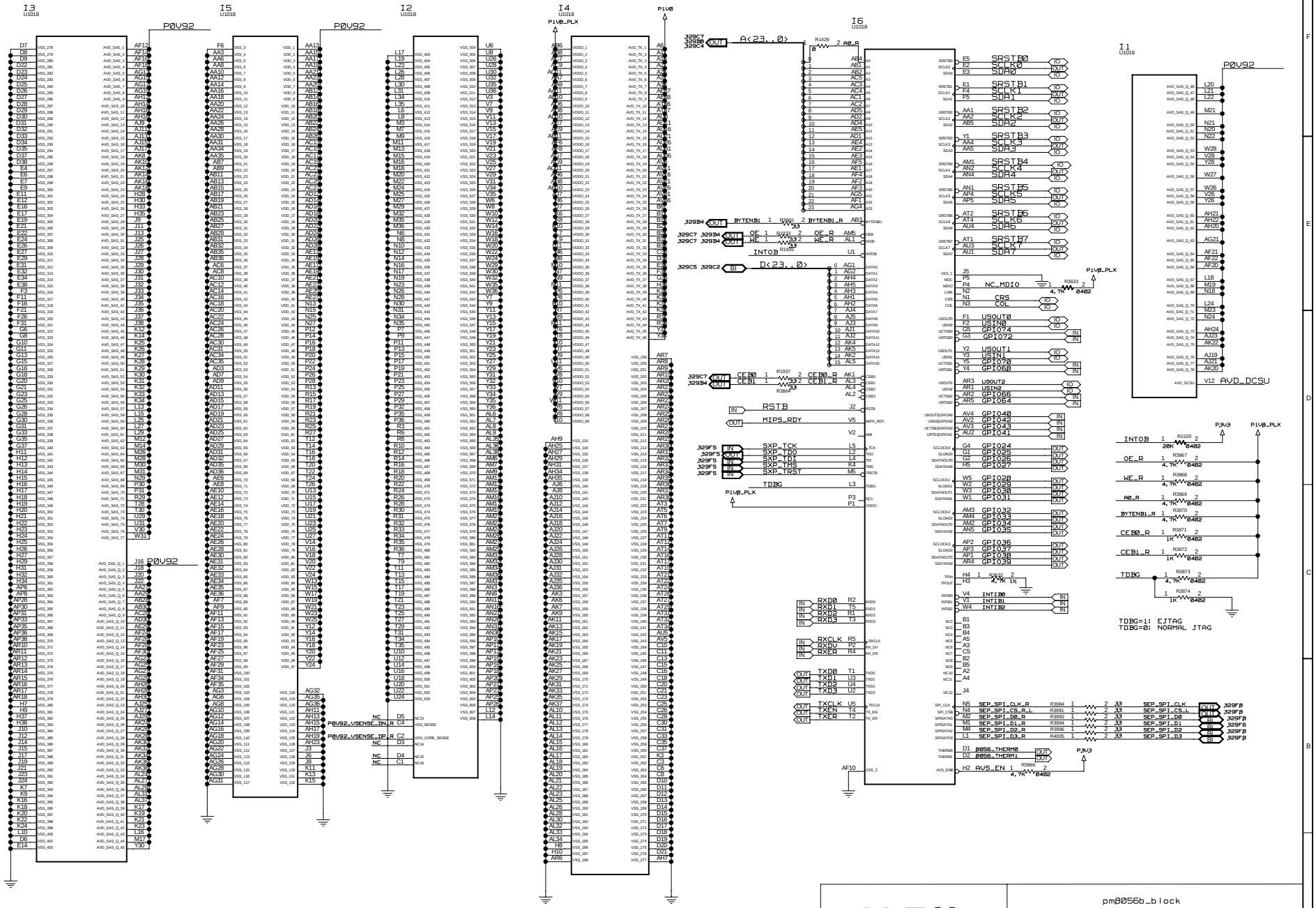
DATE: <CON_LAST_MODIFIED>		DWG NO:	REV:
DRAWN BY: <ENGINEER>		SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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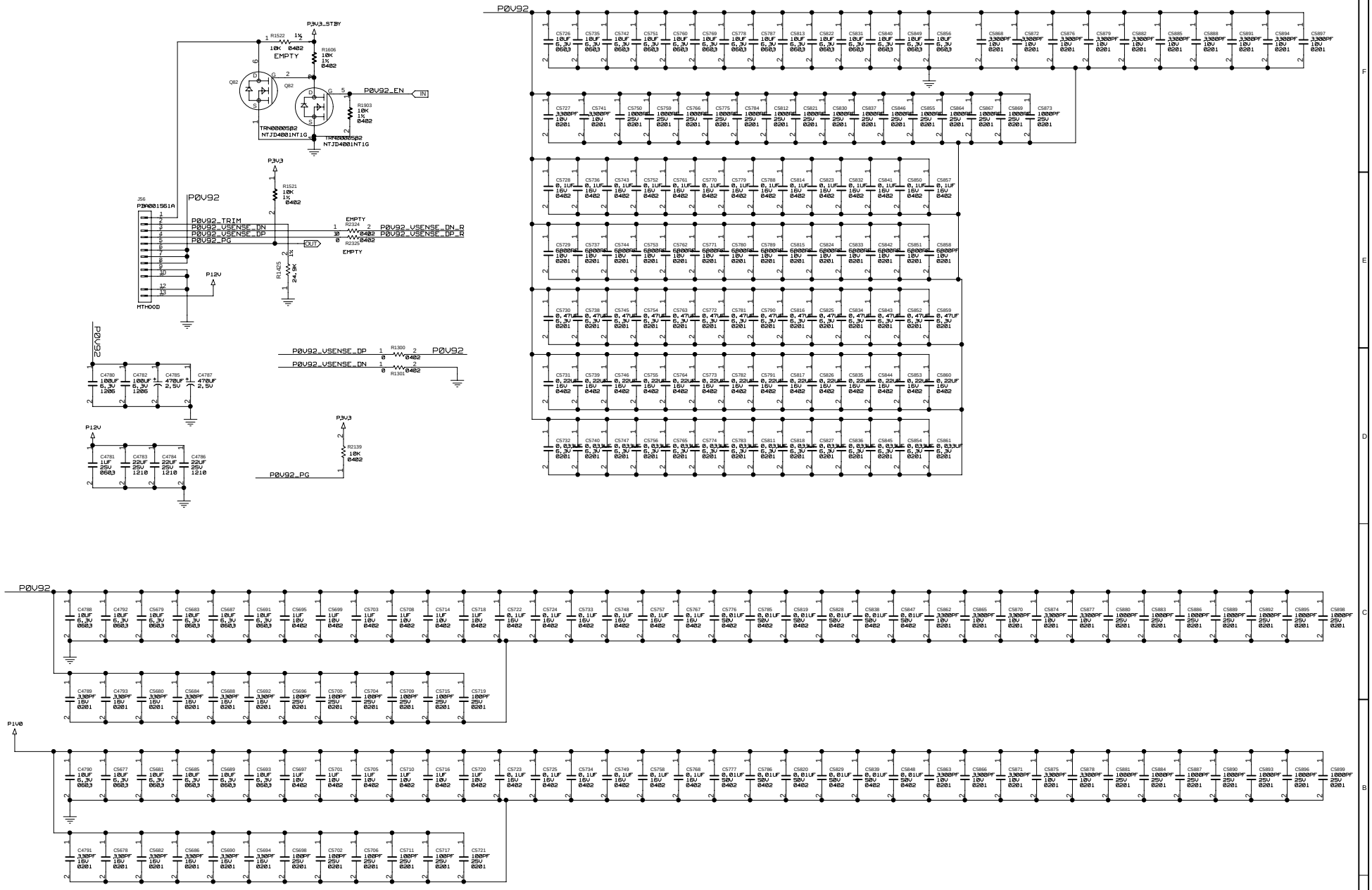
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>		DWG NO:	REV:
DRAWN BY: <ENGINEER>		SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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pm8056b_block

<CON_DESIGN_NAME>

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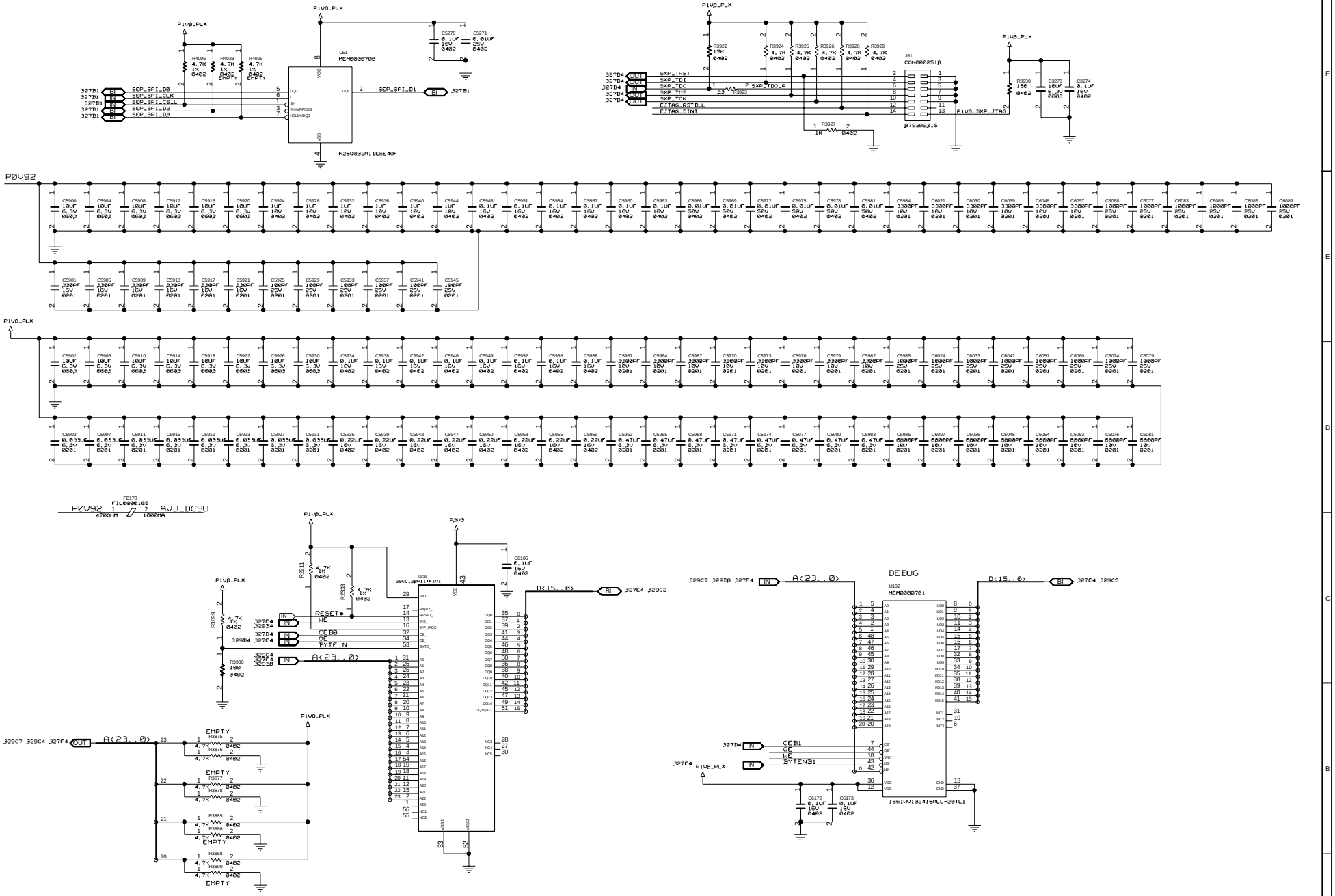
DATE: <CON_LAST_MODIFIED>	DWG NO:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



STRAP OPTIONS:

A23=1: BOOT FROM SPI
A23=0: BOOT FROM LOCAL BUS FLASH *

A22=1: INLINE ECC ENABLE ON BOOT
A22=0: INLINE ECC DISABLE ON BOOT *

A21=1: ENABLE MIPS PROCESSOR BOOT *
A21=0: DISABLE MIPS PROCESSOR BOOT

A20=1: QUAD SPI MODE *
A20=0: SINGLE SPI MODE

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<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	

JABIL

pm8056b_block

<CON_DESIGN_NAME>

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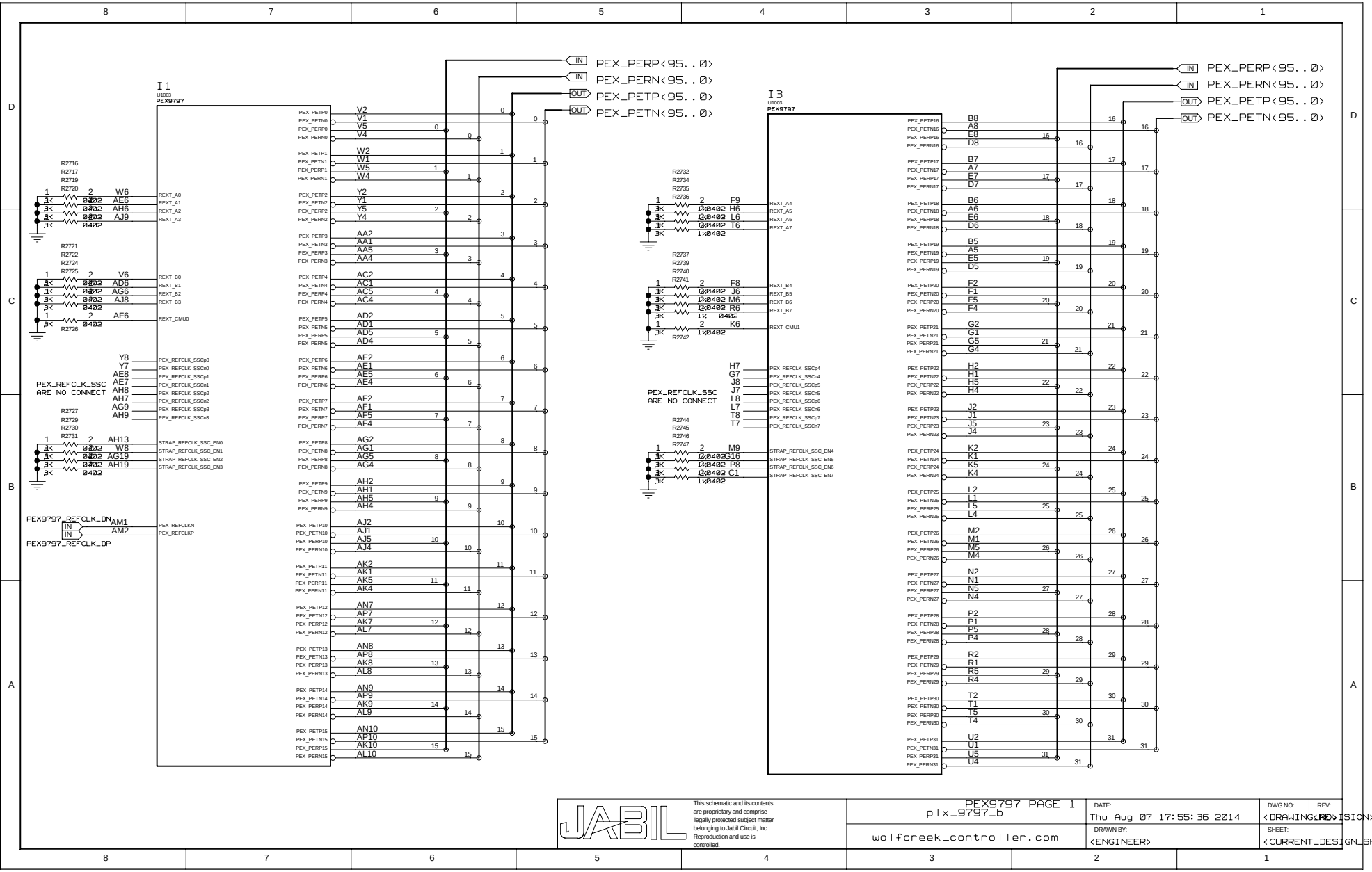
DATE: <CON_LAST_MODIFIED>	DWG NO:	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET>OF<TOTAL_DESIGN_SHEETS>	



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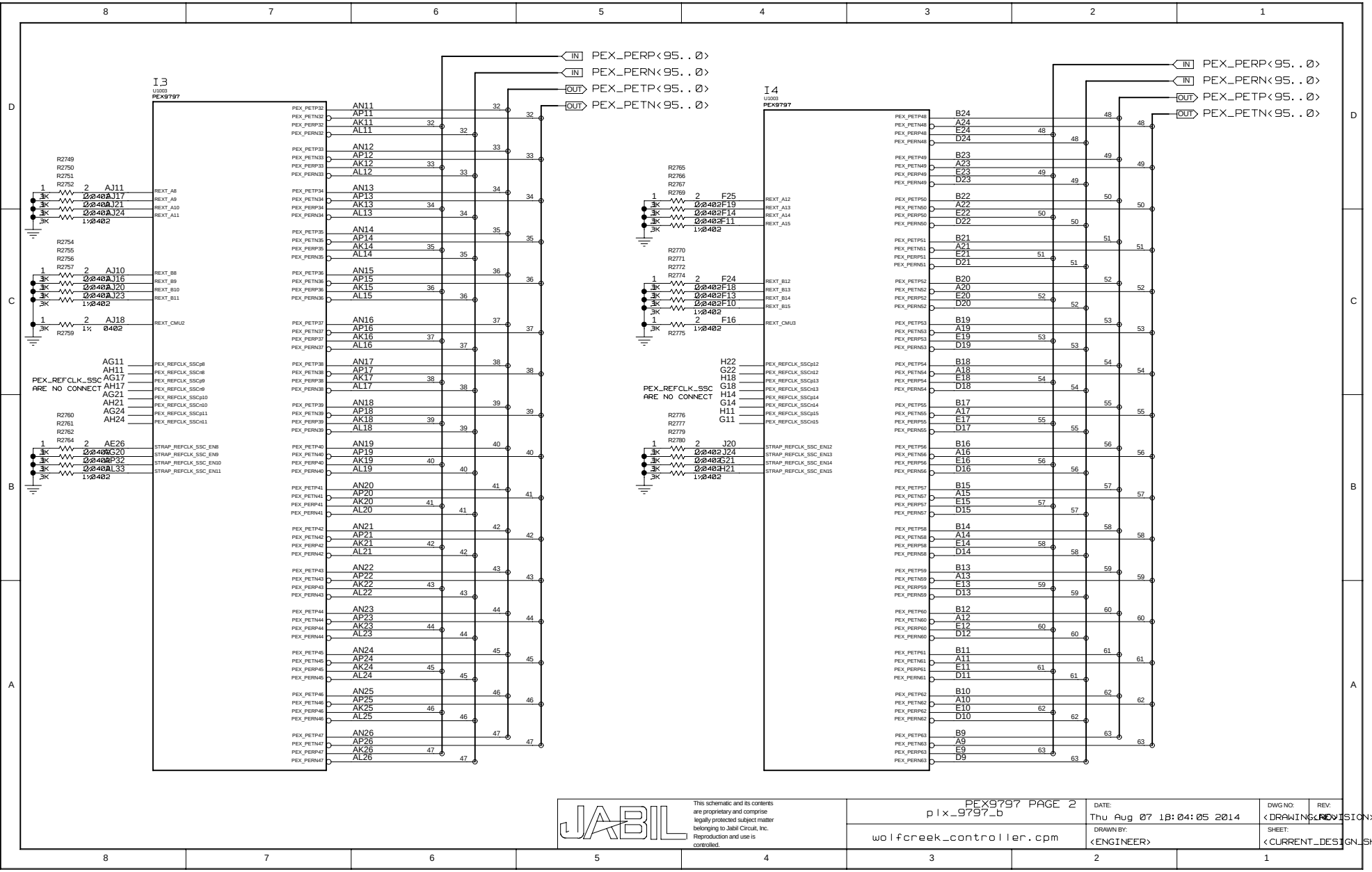
PEX9797 PAGE 1 plx_9797_b	DATE: Thu Aug 07 17:55:36 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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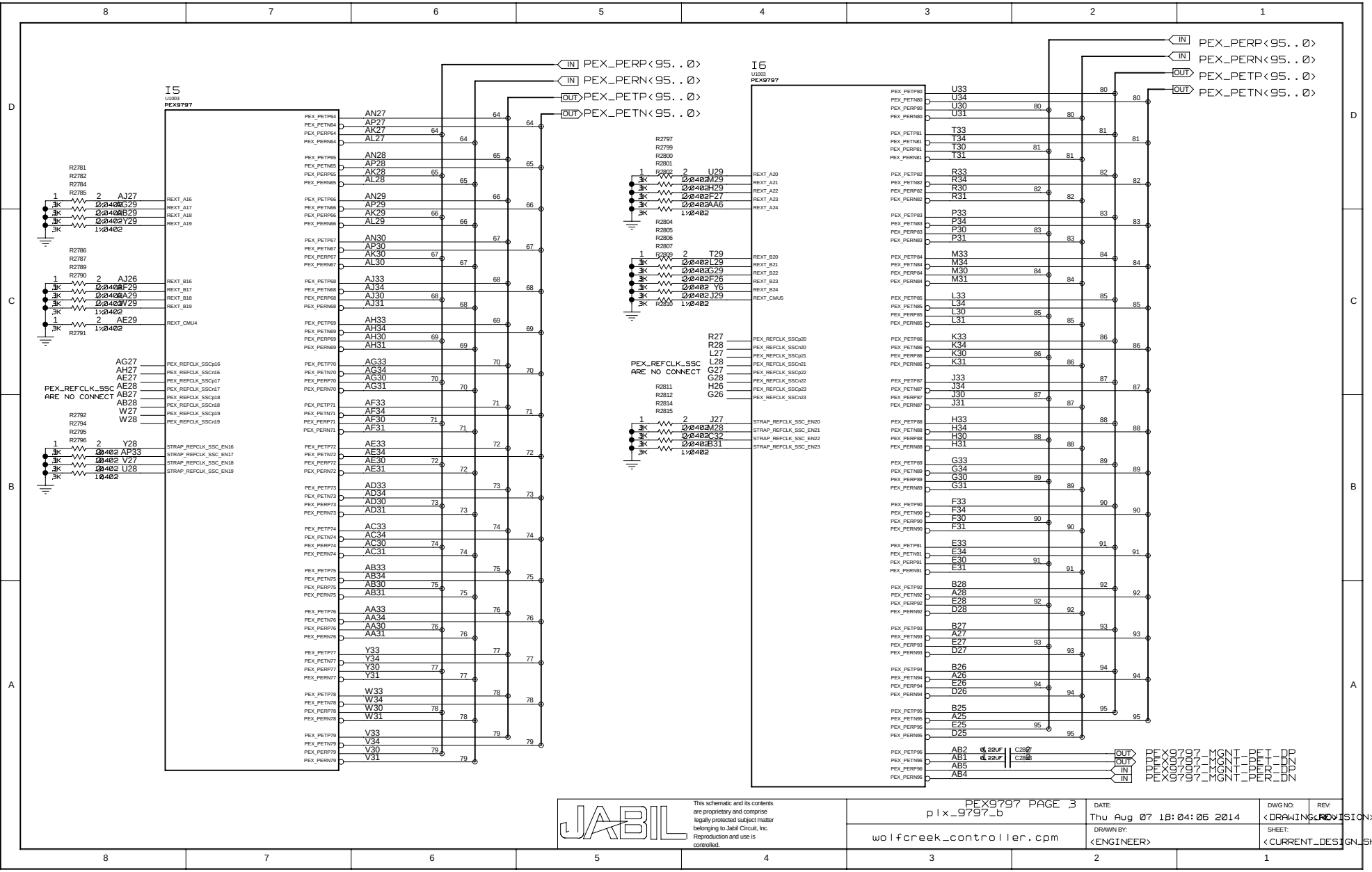
PEX9797 PAGE 2 plx_9797_b	DATE: Thu Aug 07 18:04:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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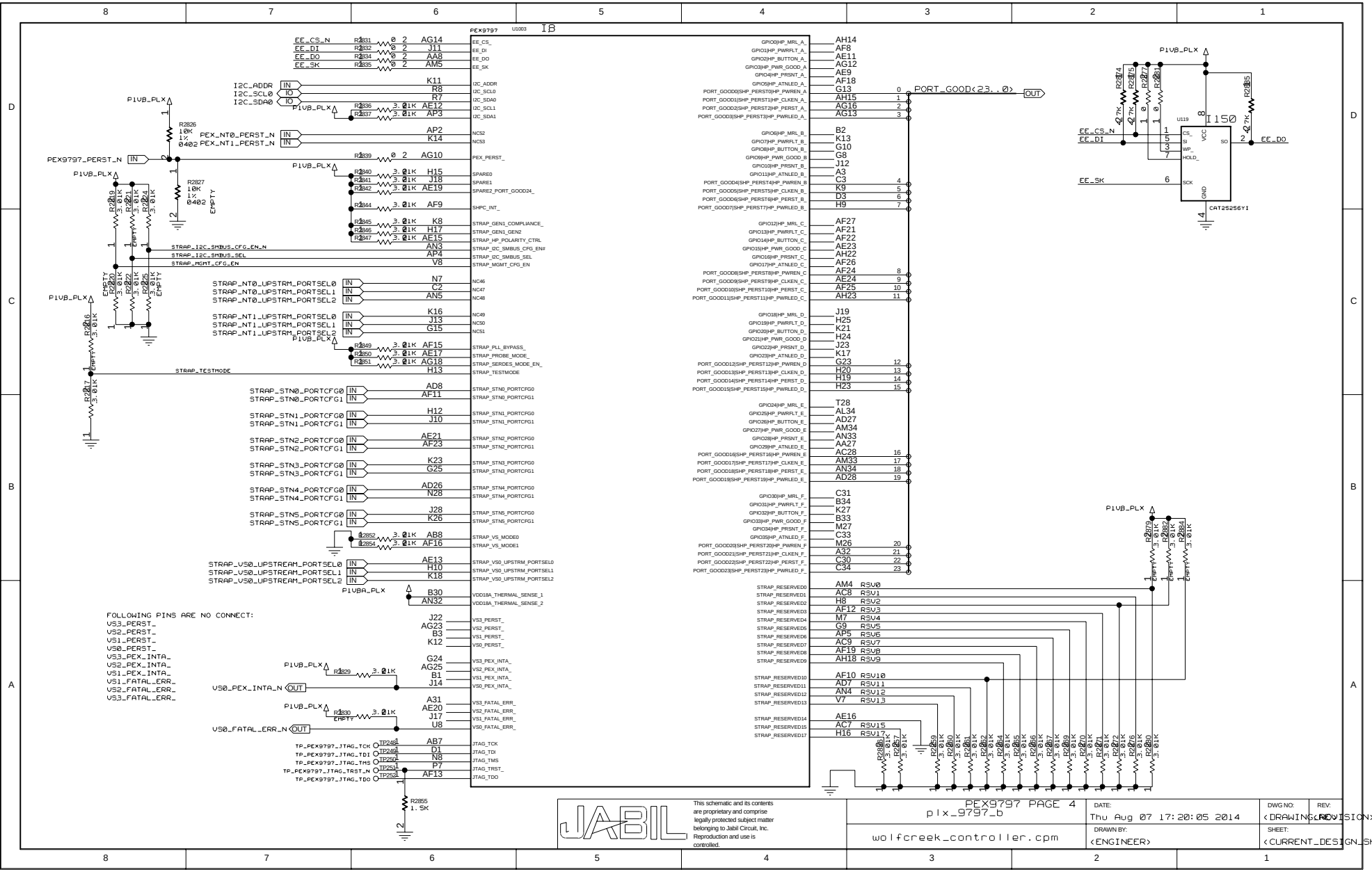
PEX9797 PAGE 3 plx_9797_b	DATE: Thu Aug 07 18:04:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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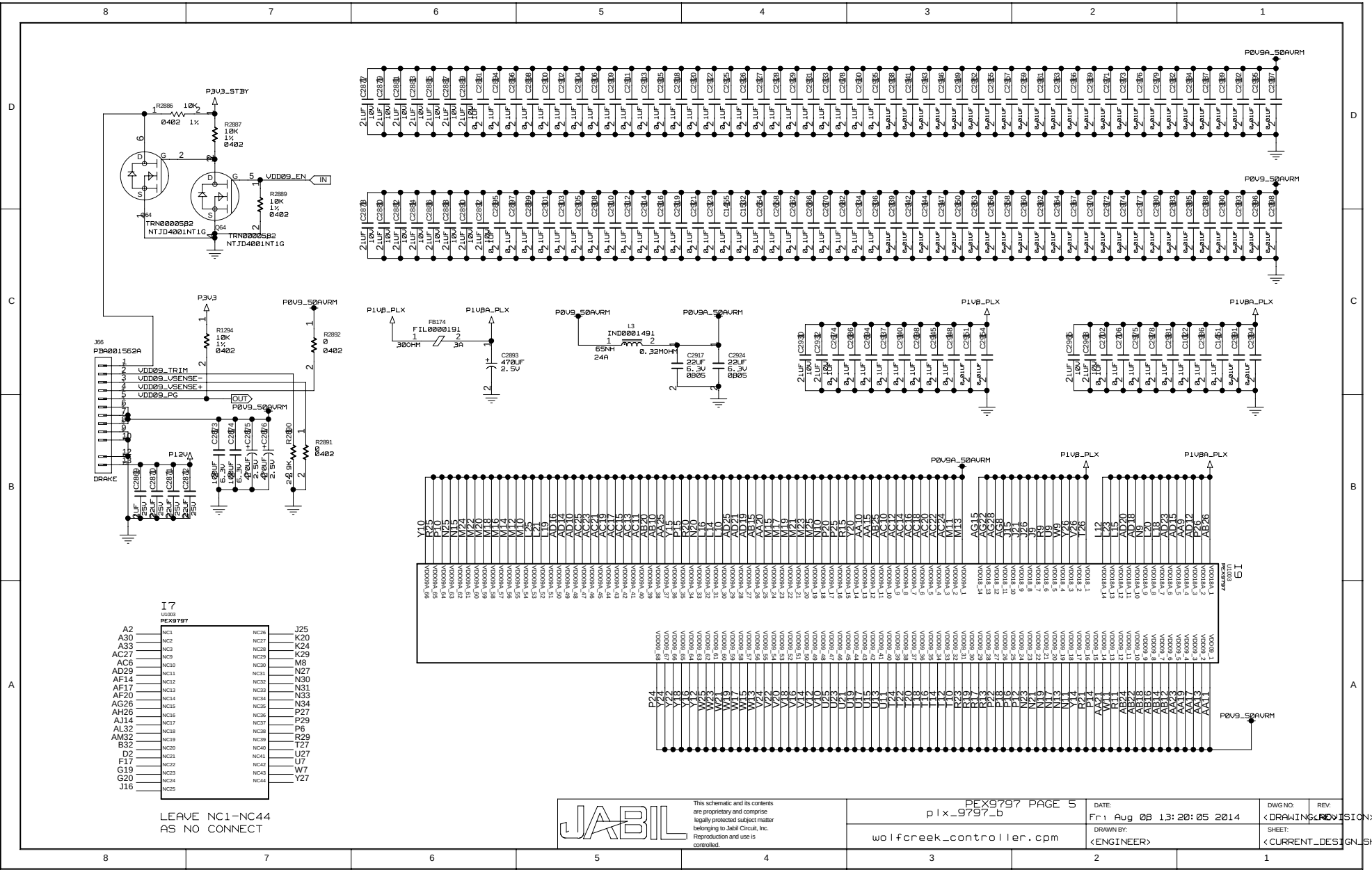
PEX9797 PAGE 4 plx_9797_b	DATE: Thu Aug 07 17:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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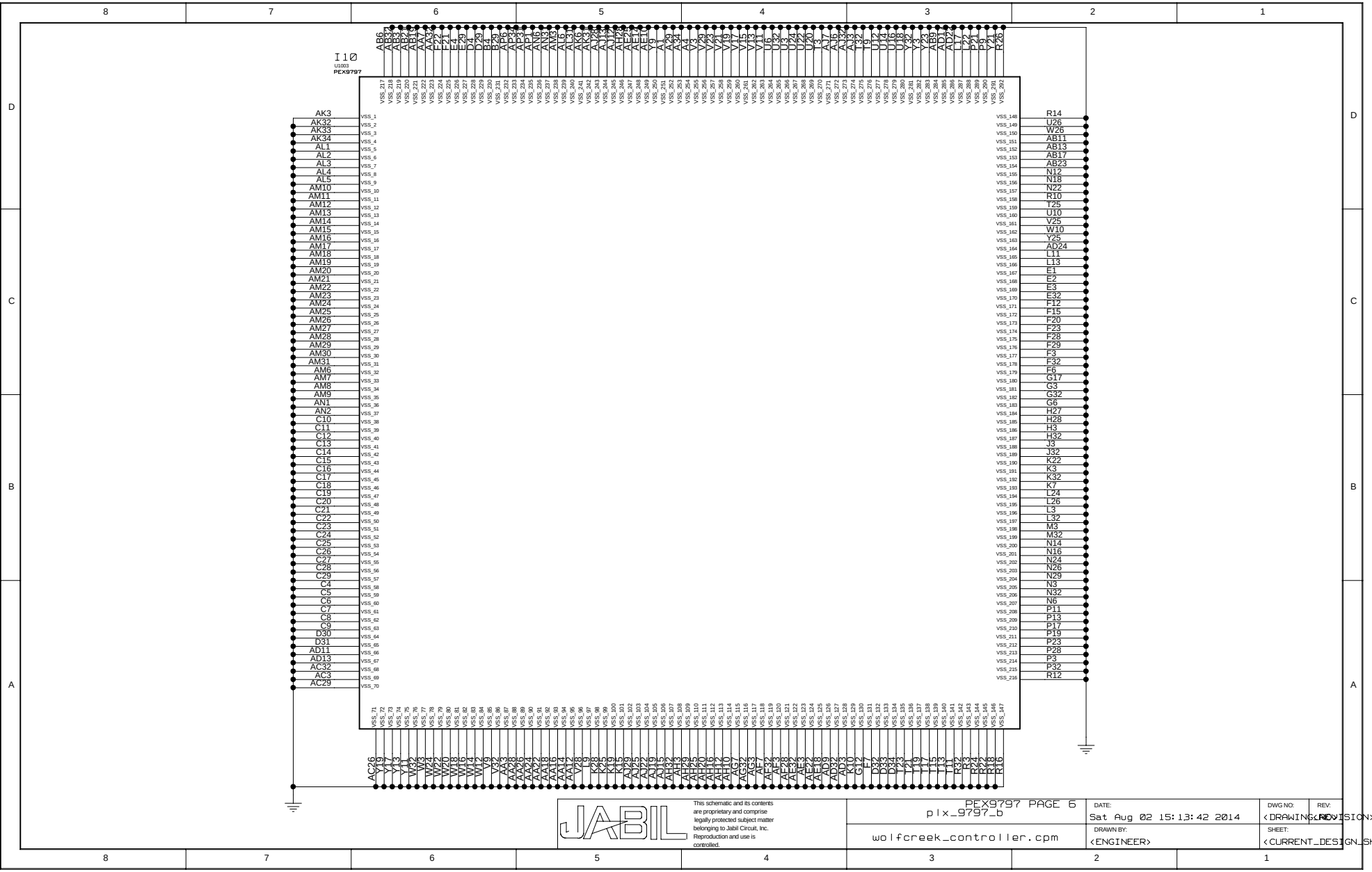
PEX9797 PAGE 5 plx_9797_b	DATE: Fri Aug 08 13:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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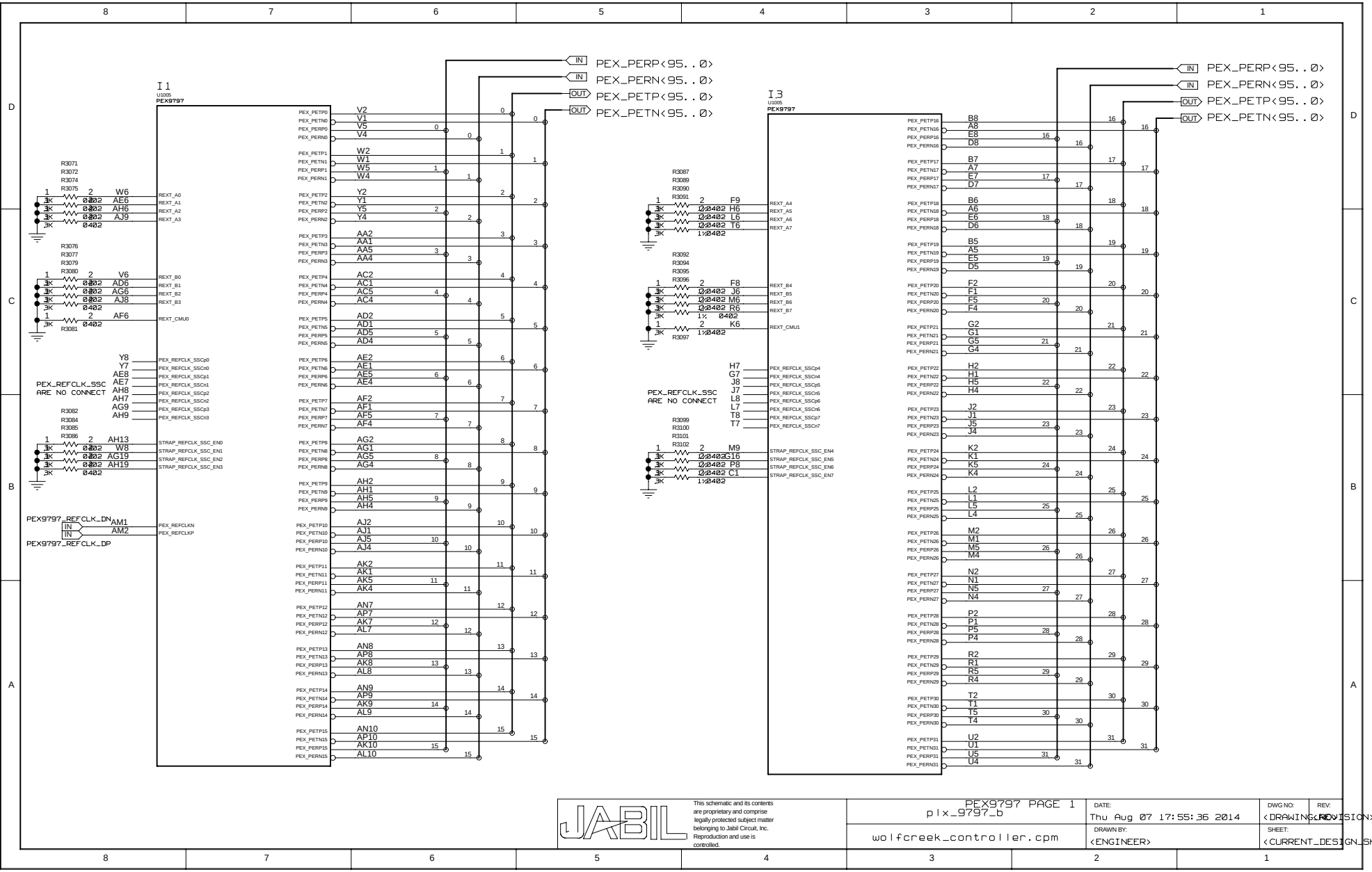
PEX9797 PAGE 6 plx_9797_b	DATE: Sat Aug 02 15:13:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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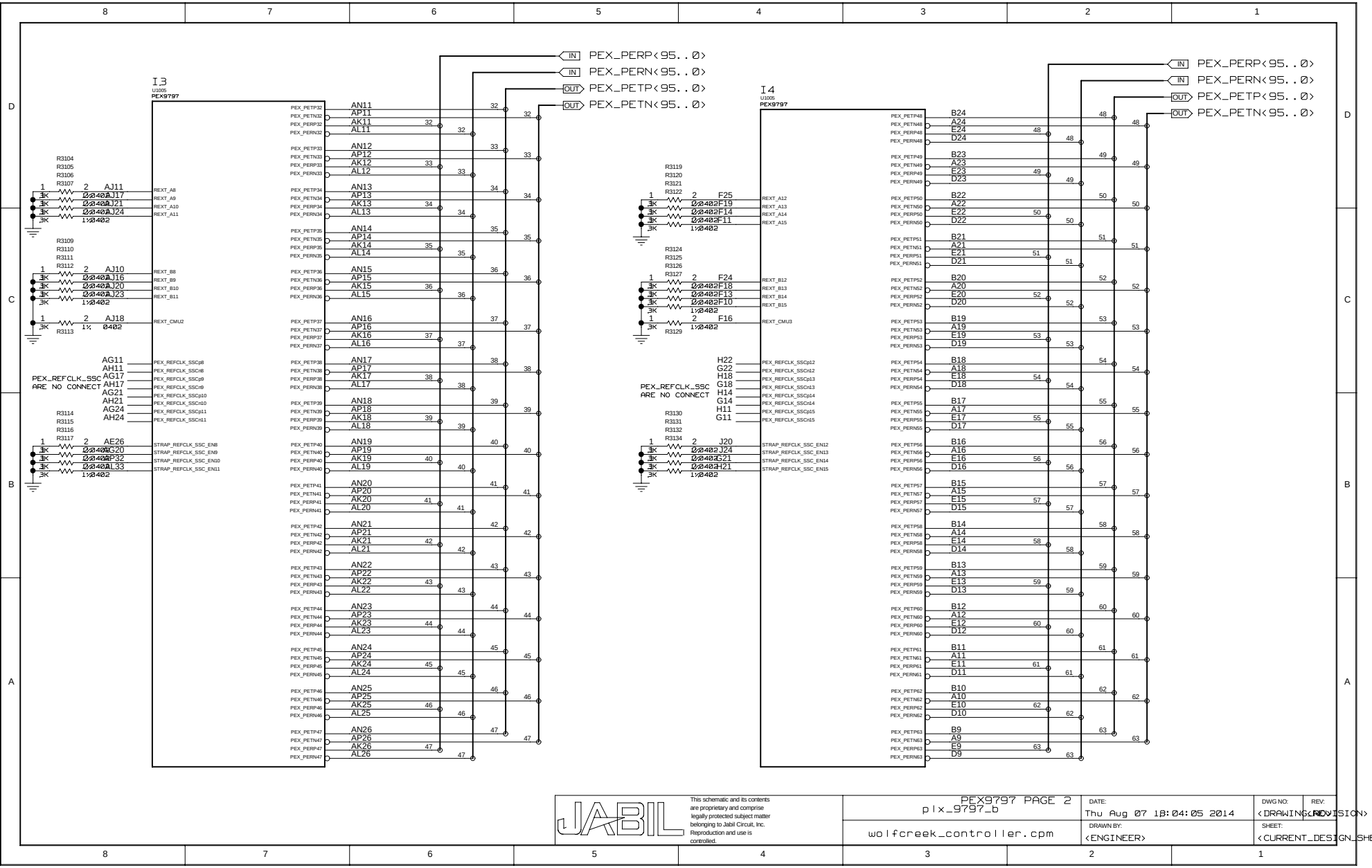
PEX9797 PAGE 1 plx_9797_b	DATE: Thu Aug 07 17:55:36 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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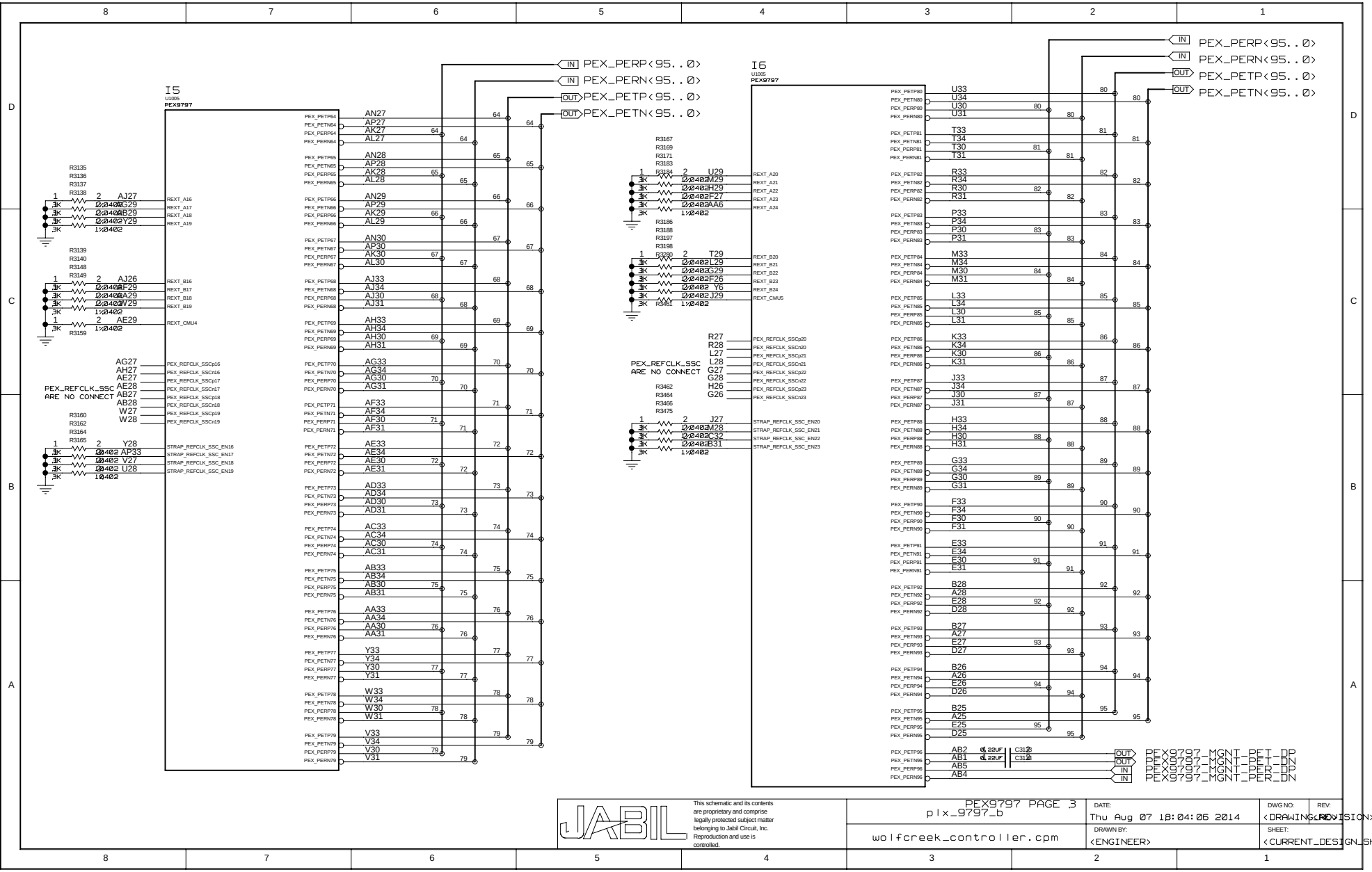
PEX9797 PAGE 2 plx_9797_b	DATE: Thu Aug 07 18:04:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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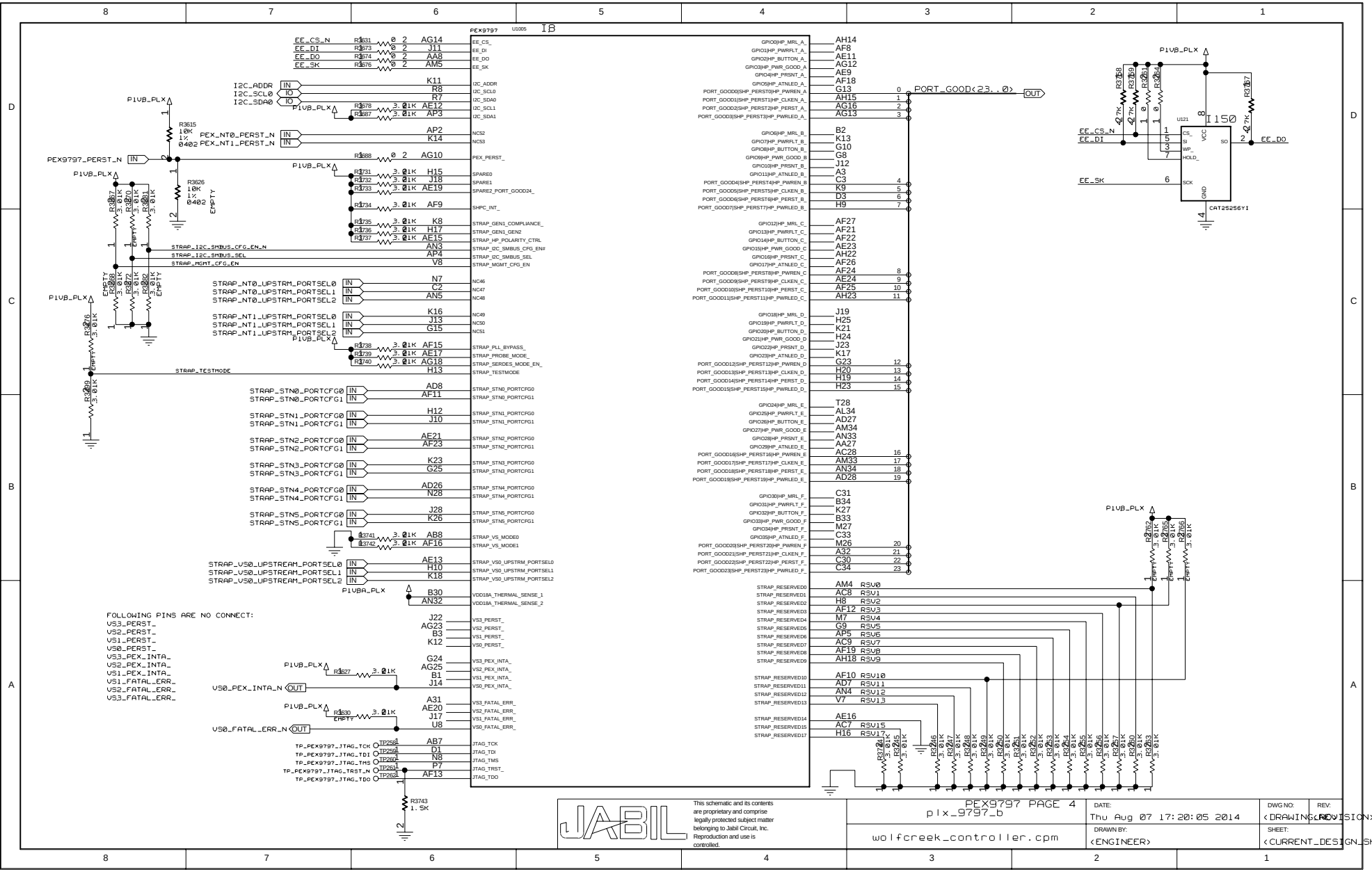
PEX9797 PAGE 3 plx_9797_b	DATE: Thu Aug 07 18:04:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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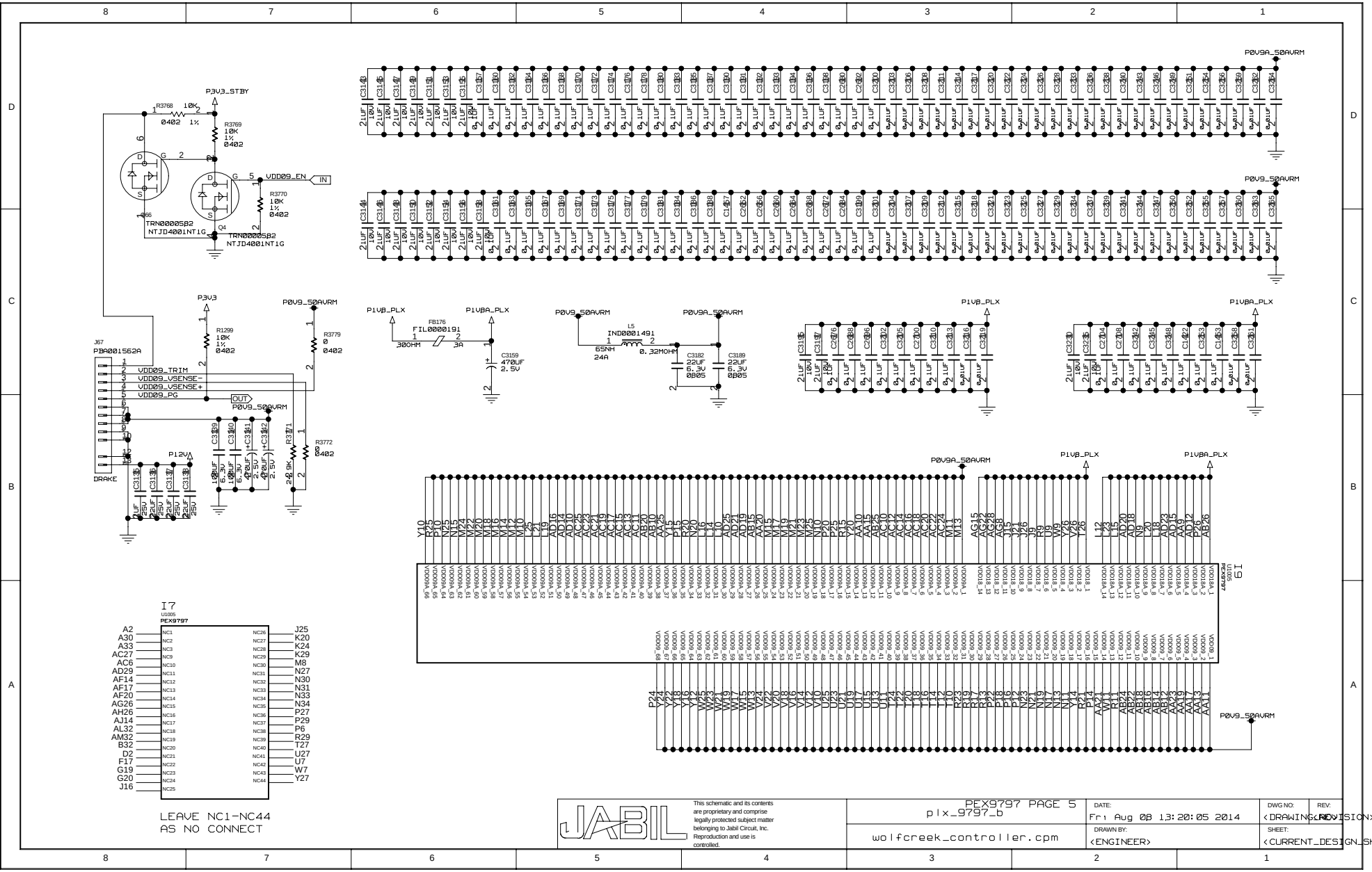
PEX9797 PAGE 4 plx_9797_b	DATE: Thu Aug 07 17:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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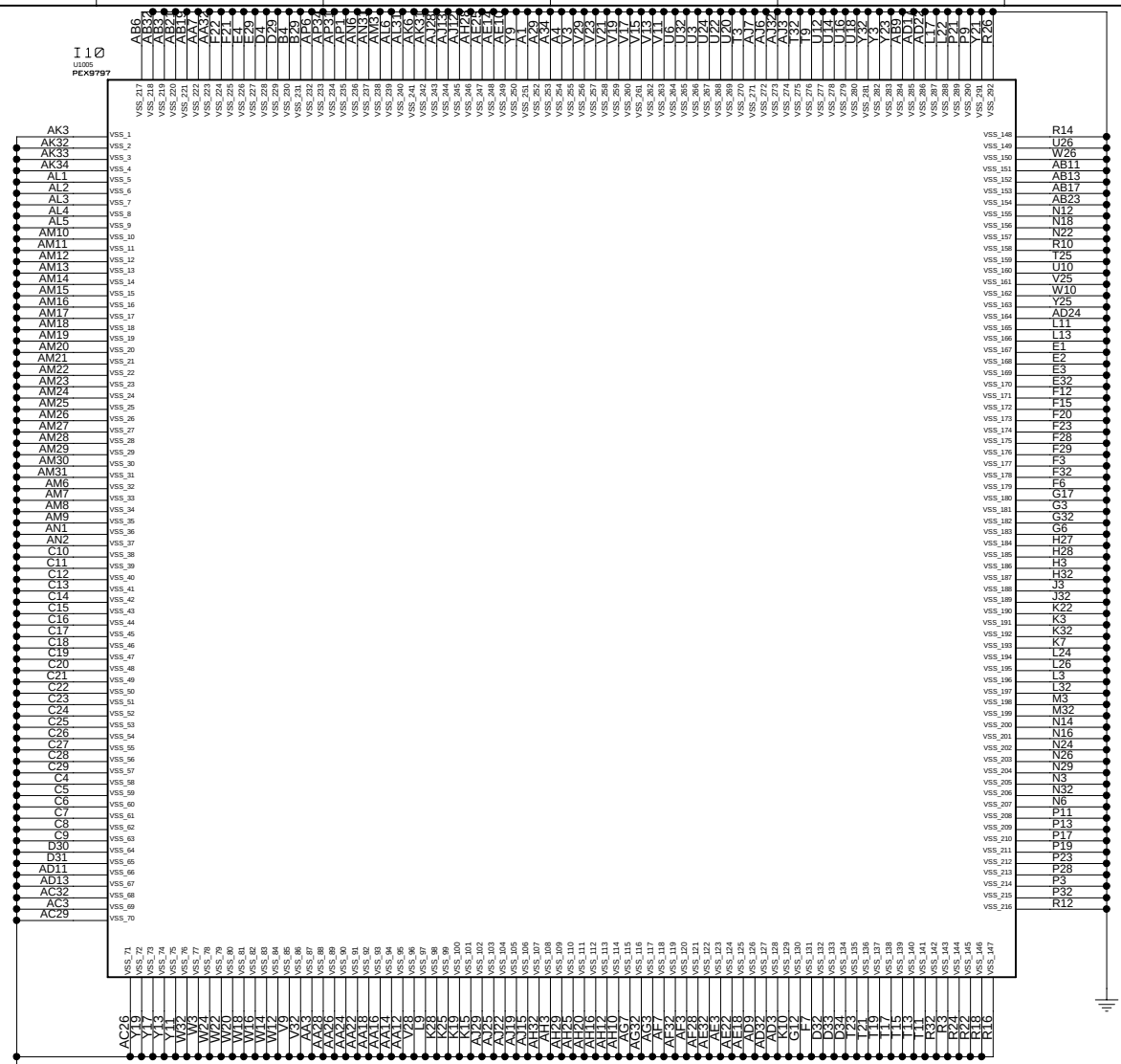
PEX9797 PAGE 5 plx_9797_b	DATE: Fri Aug 08 13:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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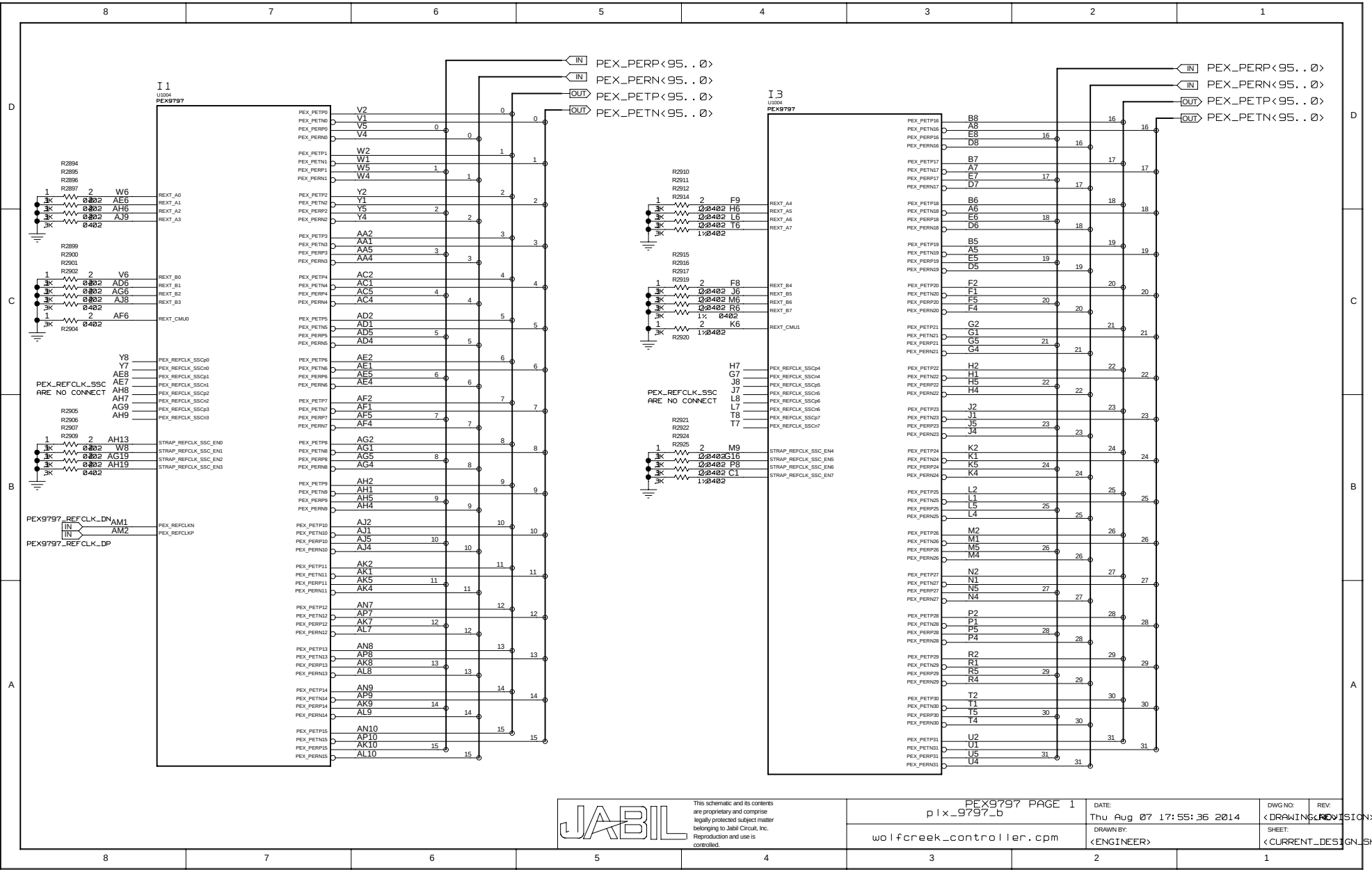
PEX9797 PAGE 6 plx_9797_b	DATE: Sat Aug 02 15:13:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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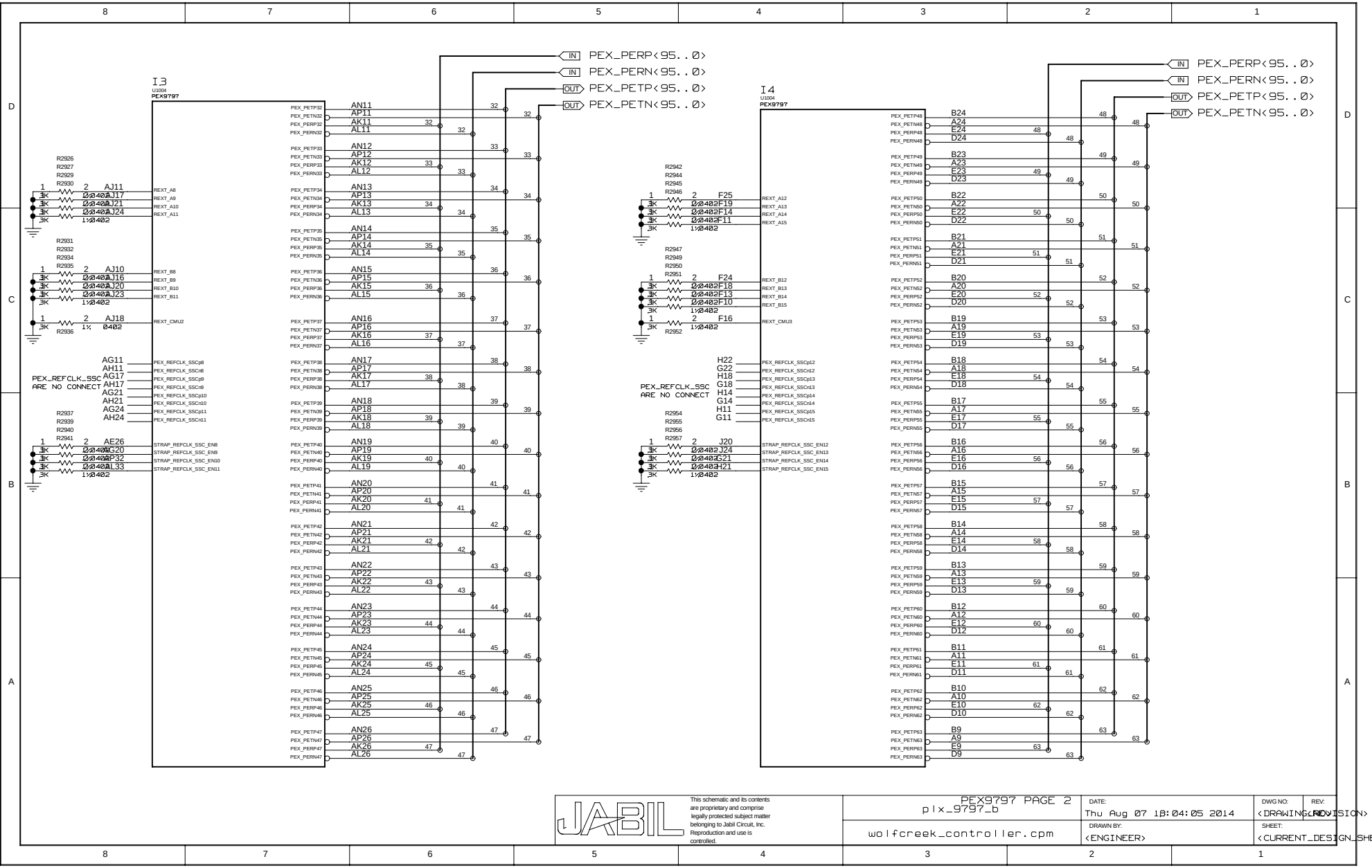
PEX9797 PAGE 1 plx_9797_b	DATE: Thu Aug 07 17:55:36 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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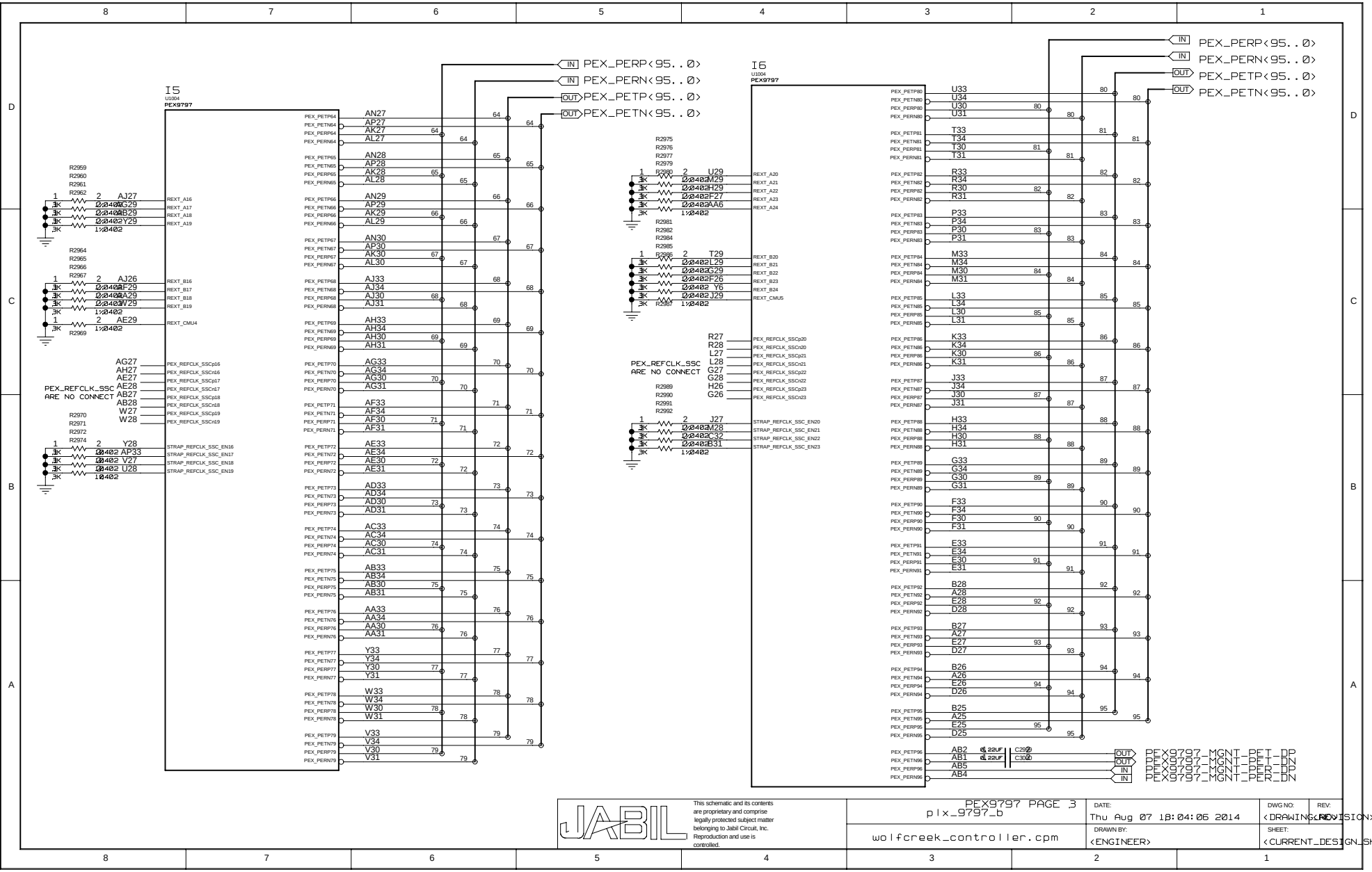
PEX9797 PAGE 2 plx_9797_b	DATE: Thu Aug 07 18:04:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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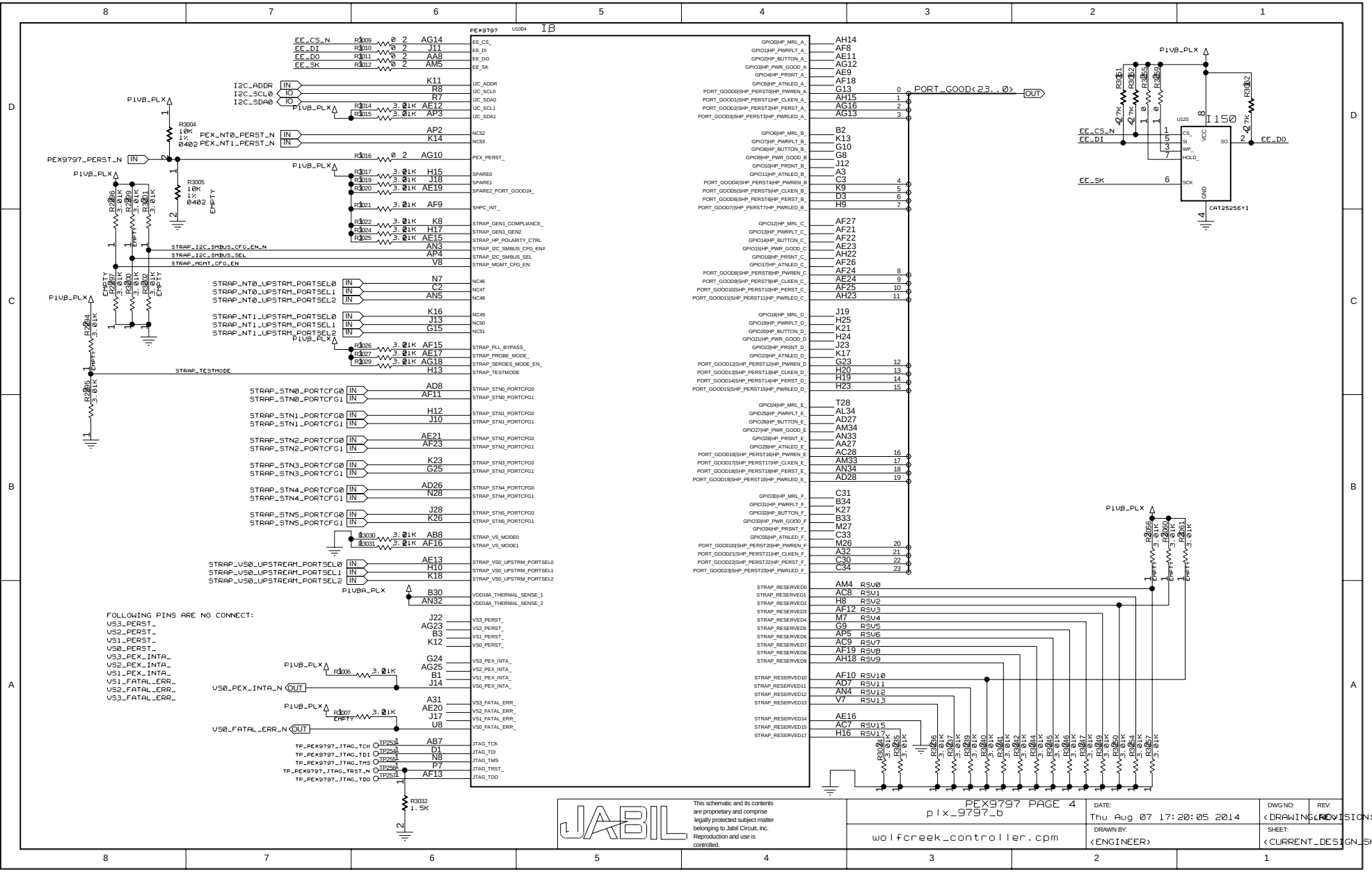
PEX9797 PAGE 3 plx_9797_b	DATE: Thu Aug 07 18:04:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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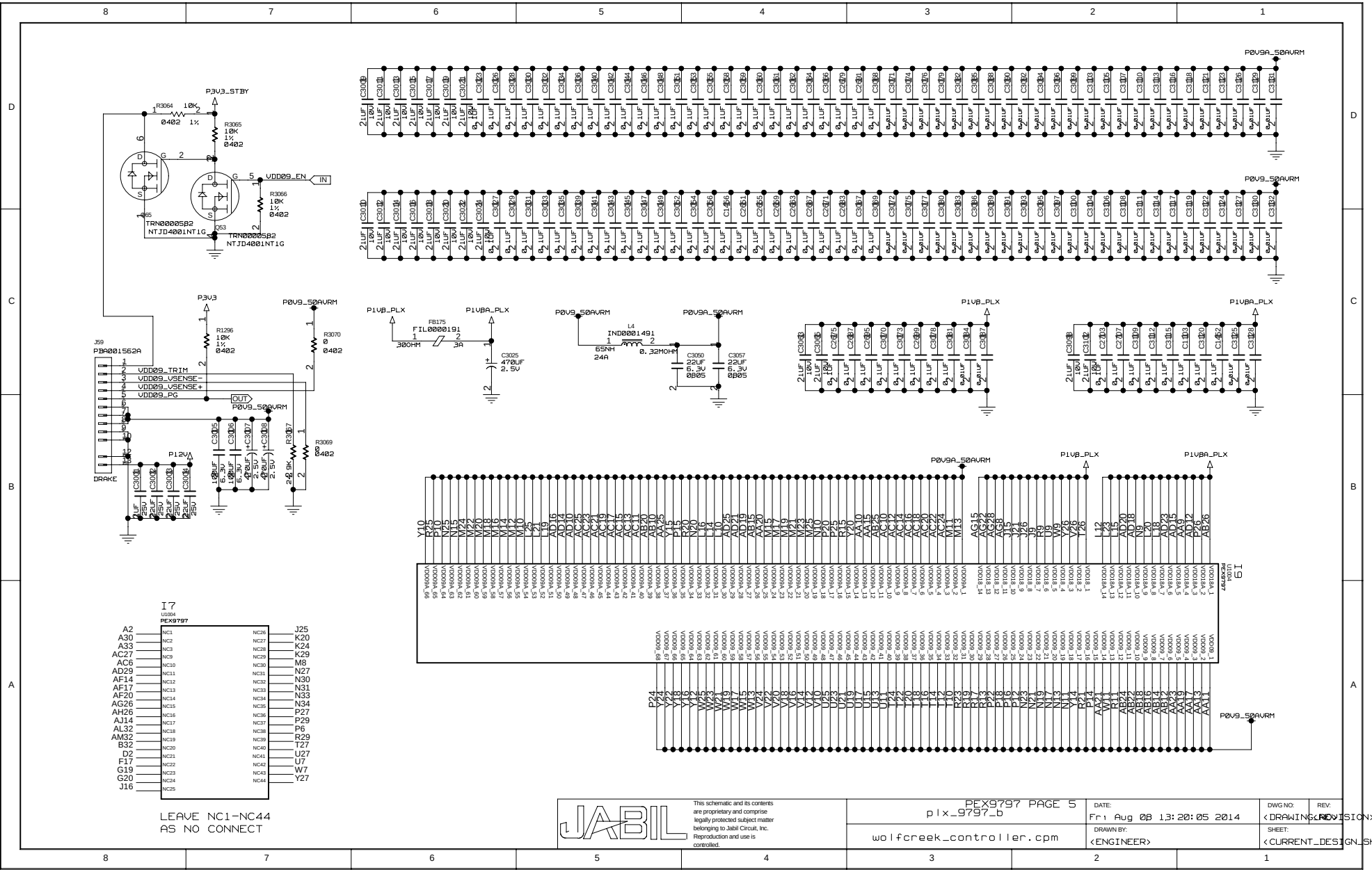
PEX9797 PAGE 4 plx_9797_b	DATE: Thu Aug 07 17:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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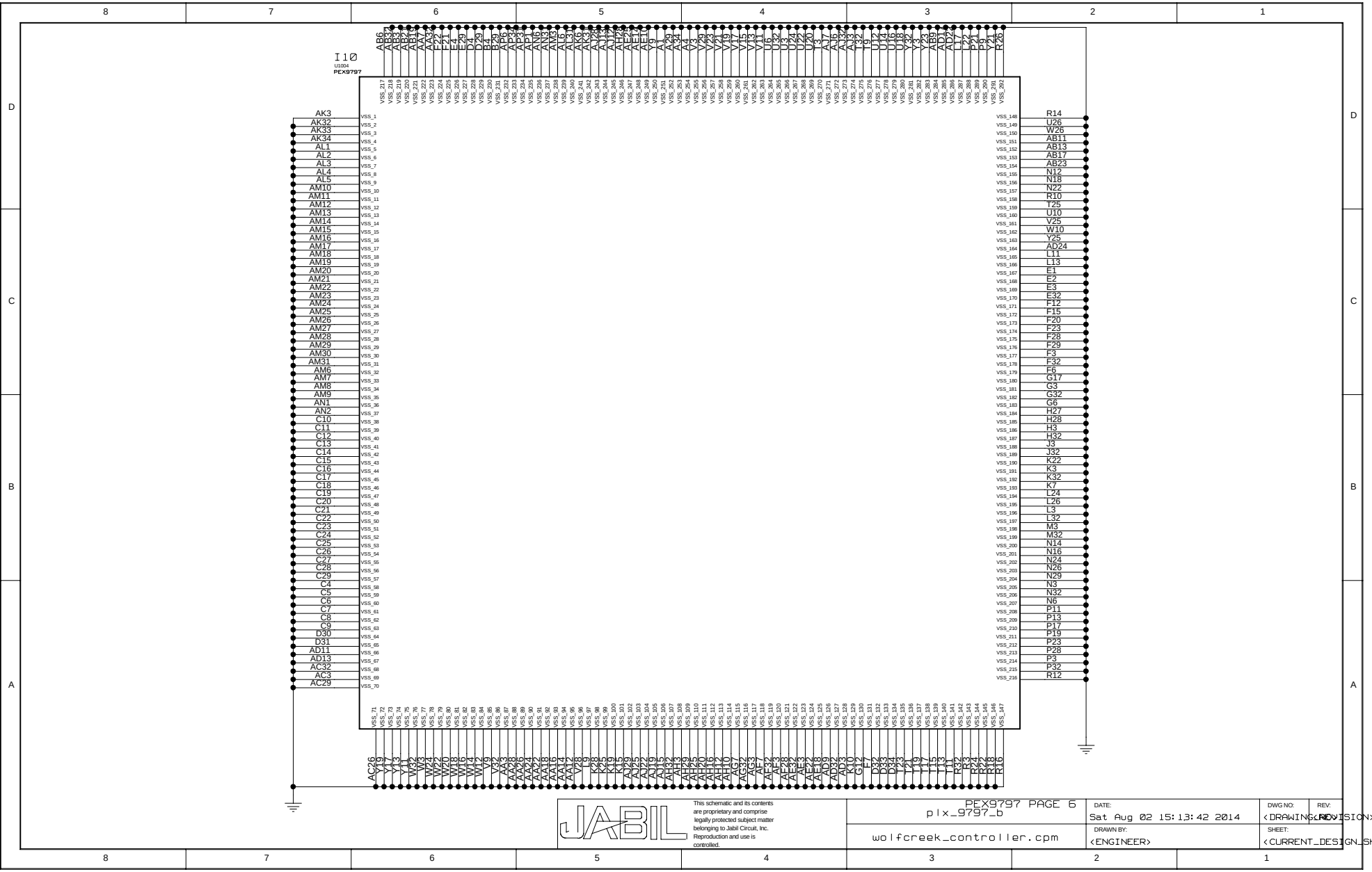
PEX9797 PAGE 5 plx_9797_b	DATE: Fri Aug 08 13:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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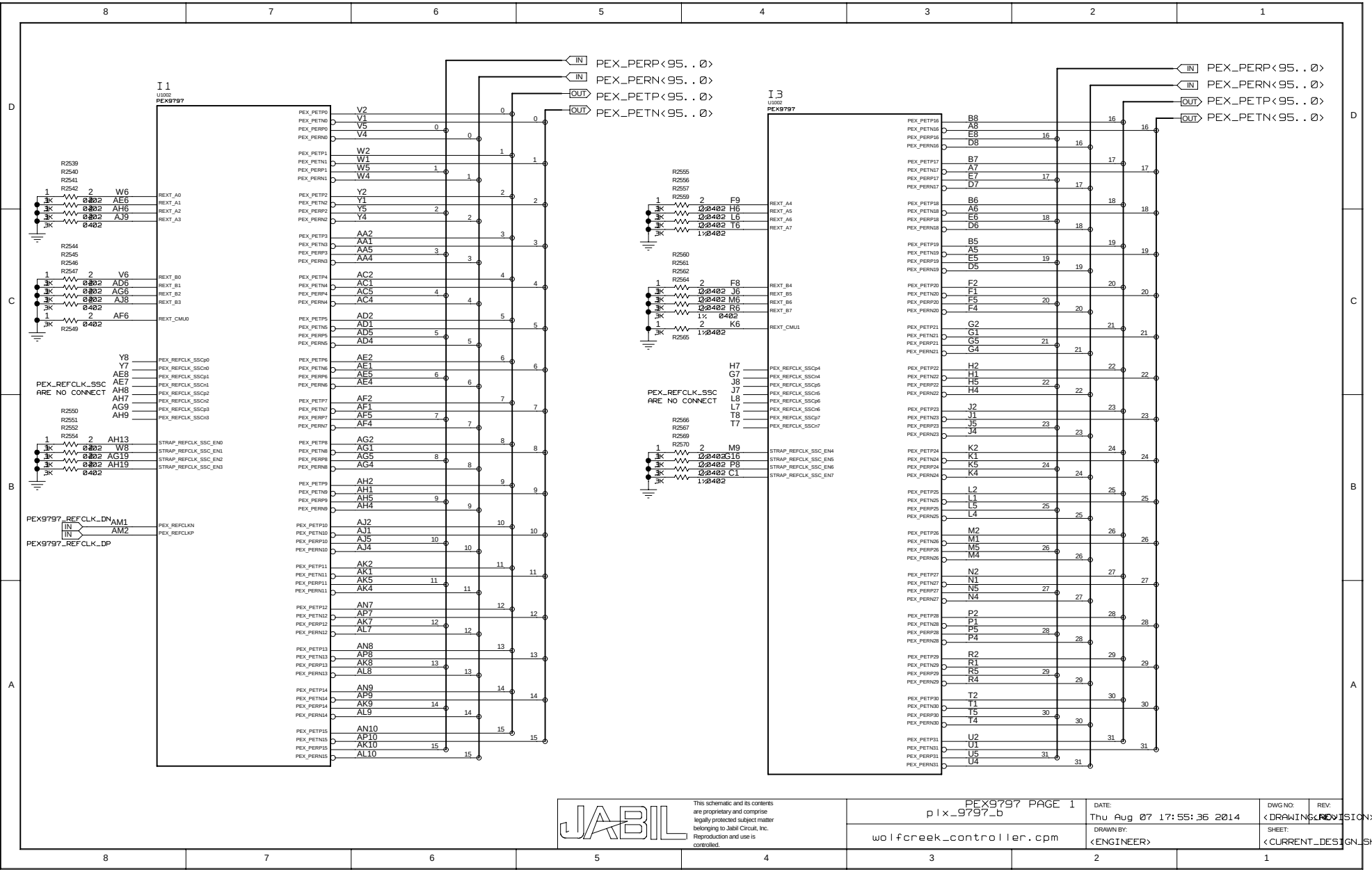
PEX9797 PAGE 6 plx_9797_b	DATE: Sat Aug 02 15:13:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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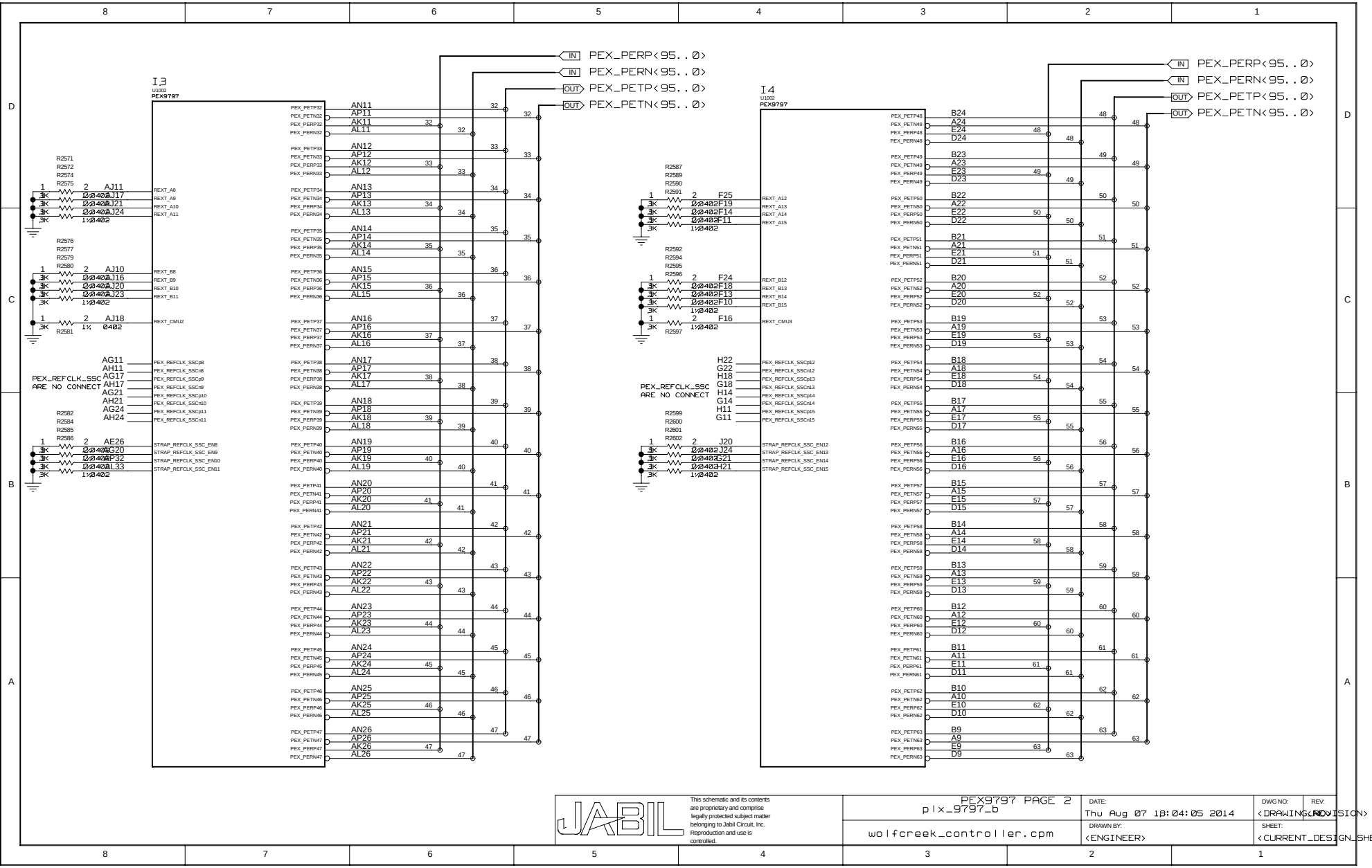
PEX9797 PAGE 1 plx_9797_b	DATE: Thu Aug 07 17:55:36 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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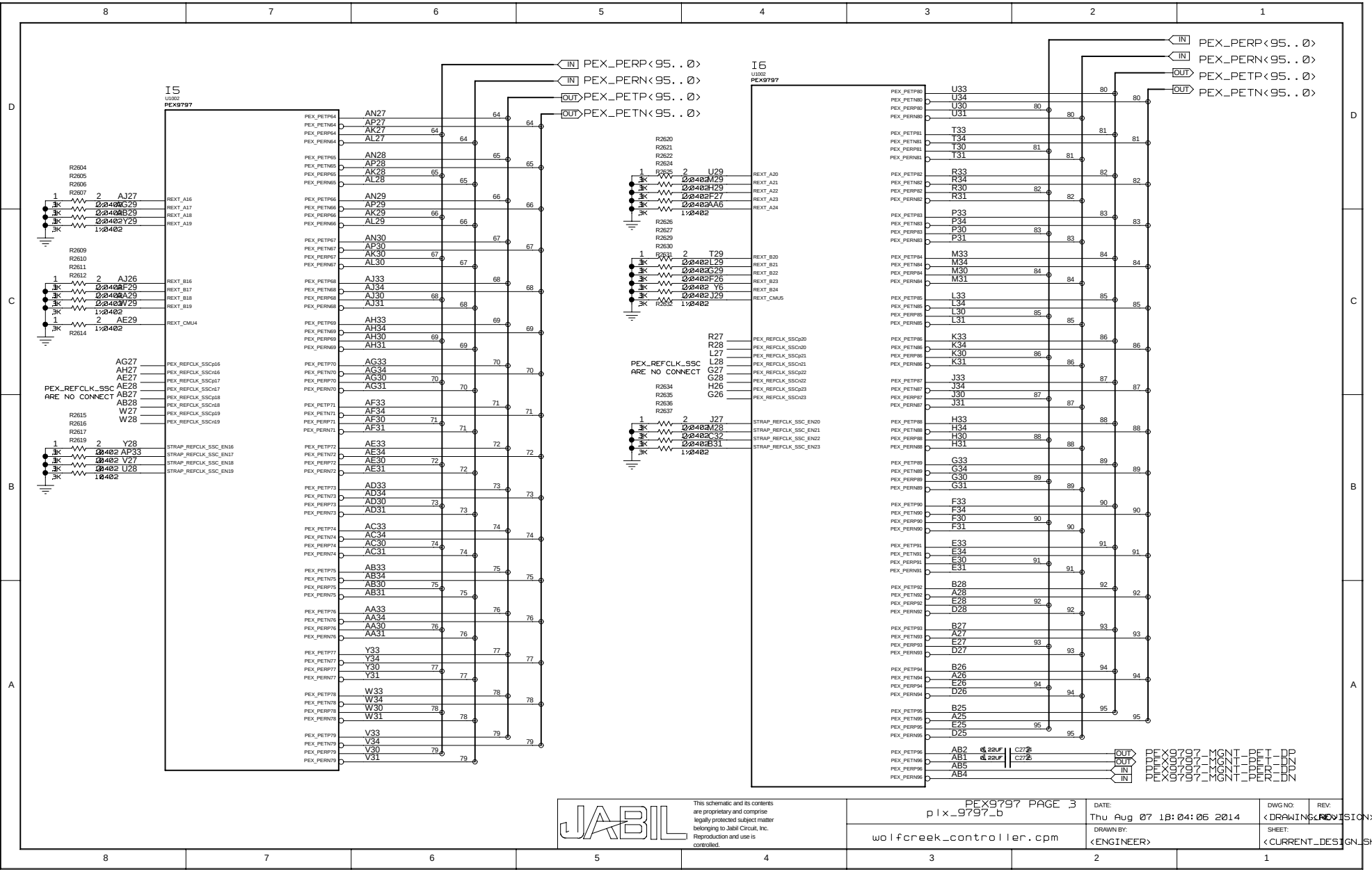
PEX9797 PAGE 2 plx_9797_b	DATE: Thu Aug 07 18:04:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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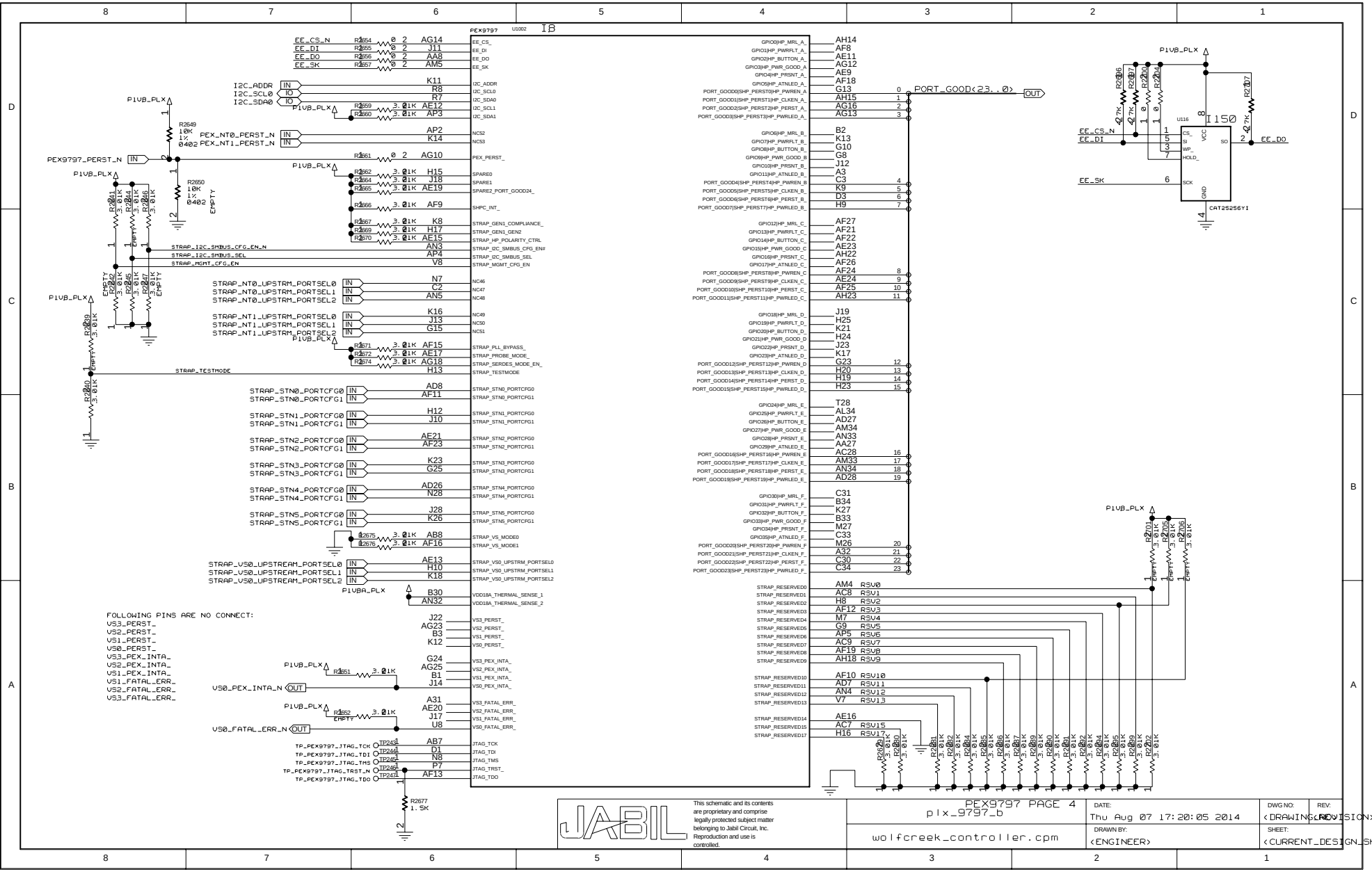
PEX9797 PAGE 3 plx_9797_b	DATE: Thu Aug 07 18:04:06 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	


PEX9797 U1002 18
EE_CS_N AG14
EE_DI J11
EE_DO AA8
EE_SK AM5
I2C_ADDR K11
I2C_SCL0 R8
I2C_SDA0 R7
I2C_SDA1 AP3
PEX_NT0_PERST_N AP2
PEX_NT1_PERST_N K14
PEX9797_PERST_N
PEX_PERST_ AG10
SPARE0 H15
SPARE1 J18
SPARE2_PORT_GOOD24_ AE19
SHPC_INT_ AF9
STRAP_GEN1_COMPLIANCE_ K8
STRAP_GEN1_GEN2 H17
STRAP_HP_POLARITY_CTRL AE15
STRAP_I2C_SMBUS_CFG_EN_N AN3
STRAP_I2C_SMBUS_SEL AP4
STRAP_MGMT_CFG_EN V8
STRAP_NT0_UPSTRM_PORTSEL0 N7
STRAP_NT0_UPSTRM_PORTSEL1 C2
STRAP_NT0_UPSTRM_PORTSEL2 AN5
STRAP_NT1_UPSTRM_PORTSEL0 K16
STRAP_NT1_UPSTRM_PORTSEL1 J13
STRAP_NT1_UPSTRM_PORTSEL2 G15
STRAP_PLL_BYPASS_ AF15
STRAP_PROBE_MODE_ AE17
STRAP_SERDES_MODE_EN_ AG18
STRAP_TESTMODE H13
STRAP_STN0_PORTCFG0 AD8
STRAP_STN0_PORTCFG1 AF11
STRAP_STN1_PORTCFG0 H12
STRAP_STN1_PORTCFG1 J10
STRAP_STN2_PORTCFG0 AE21
STRAP_STN2_PORTCFG1 AF23
STRAP_STN3_PORTCFG0 K23
STRAP_STN3_PORTCFG1 G25
STRAP_STN4_PORTCFG0 AD26
STRAP_STN4_PORTCFG1 N28
STRAP_STN5_PORTCFG0 J28
STRAP_STN5_PORTCFG1 K26
STRAP_VS_MODE0 AB8
STRAP_VS_MODE1 AF16
STRAP_VS0_UPSTREAM_PORTSEL0 AE13
STRAP_VS0_UPSTREAM_PORTSEL1 H10
STRAP_VS0_UPSTREAM_PORTSEL2 K18
VDD18A_THERMAL_SENSE_1 B30
VDD18A_THERMAL_SENSE_2 AN32
FOLLOWING PINS ARE NO CONNECT:
VS3_PERST_
VS2_PERST_
VS1_PERST_
VS0_PERST_
VS3_PEX_INTA_
VS2_PEX_INTA_
VS1_PEX_INTA_
VS1_FATAL_ERR_
VS2_FATAL_ERR_
VS3_FATAL_ERR_
VS3_PERST_ J22
VS2_PERST_ AG23
VS1_PERST_ B3
VS0_PERST_ K12
VS3_PEX_INTA_ G24
VS2_PEX_INTA_ AG25
VS1_PEX_INTA_ B1
VS0_PEX_INTA_ J14
VS3_FATAL_ERR_ A31
VS2_FATAL_ERR_ AE20
VS1_FATAL_ERR_ J17
VS0_FATAL_ERR_ U8
JTAG_TCK AB7
JTAG_TDI D1
JTAG_TMS N8
JTAG_TRST_ P7
JTAG_TDO AF13
TP_PEX9797_JTAG_TCK
TP_PEX9797_JTAG_TDI
TP_PEX9797_JTAG_TMS
TP_PEX9797_JTAG_TRST_N
TP_PEX9797_JTAG_TDO
PORT_GOOD<23..0>
GPIO00|HP_MRL_A_ AH14
GPIO01|HP_PWRFLT_A_ AF8
GPIO02|HP_BUTTON_A_ AE11
GPIO03|HP_PWR_GOOD_A AG12
GPIO04|HP_PRSNT_A_ AE9
GPIO05|HP_ATNLED_A_ AF18
PORT_GOOD0|SHP_PERST0|HP_PWREN_A G13 0
PORT_GOOD1|SHP_PERST1|HP_CLKEN_A_ AH15 1
PORT_GOOD2|SHP_PERST2|HP_PERST_A_ AG16 2
PORT_GOOD3|SHP_PERST3|HP_PWRLED_A_ AG13 3
GPIO06|HP_MRL_B_ B2
GPIO07|HP_PWRFLT_B_ K13
GPIO08|HP_BUTTON_B_ G10
GPIO09|HP_PWR_GOOD_B G8
GPIO10|HP_PRSNT_B_ J12
GPIO11|HP_ATNLED_B_ A3
PORT_GOOD4|SHP_PERST4|HP_PWREN_B C3 4
PORT_GOOD5|SHP_PERST5|HP_CLKEN_B_ K9 5
PORT_GOOD6|SHP_PERST6|HP_PERST_B_ D3 6
PORT_GOOD7|SHP_PERST7|HP_PWRLED_B_ H9 7
GPIO12|HP_MRL_C_ AF27
GPIO13|HP_PWRFLT_C_ AF21
GPIO14|HP_BUTTON_C_ AF22
GPIO15|HP_PWR_GOOD_C AE23
GPIO16|HP_PRSNT_C_ AH22
GPIO17|HP_ATNLED_C_ AF26
PORT_GOOD8|SHP_PERST8|HP_PWREN_C AF24 8
PORT_GOOD9|SHP_PERST9|HP_CLKEN_C_ AE24 9
PORT_GOOD10|SHP_PERST10|HP_PERST_C_ AF25 10
PORT_GOOD11|SHP_PERST11|HP_PWRLED_C_ AH23 11
GPIO18|HP_MRL_D_ J19
GPIO19|HP_PWRFLT_D_ H25
GPIO20|HP_BUTTON_D_ K21
GPIO21|HP_PWR_GOOD_D H24
GPIO22|HP_PRSNT_D_ J23
GPIO23|HP_ATNLED_D_ K17
PORT_GOOD12|SHP_PERST12|HP_PWREN_D G23 12
PORT_GOOD13|SHP_PERST13|HP_CLKEN_D_ H20 13
PORT_GOOD14|SHP_PERST14|HP_PERST_D_ H19 14
PORT_GOOD15|SHP_PERST15|HP_PWRLED_D_ H23 15
GPIO24|HP_MRL_E_ T28
GPIO25|HP_PWRFLT_E_ AL34
GPIO26|HP_BUTTON_E_ AD27
GPIO27|HP_PWR_GOOD_E AM34
GPIO28|HP_PRSNT_E_ AN33
GPIO29|HP_ATNLED_E_ AA27
PORT_GOOD16|SHP_PERST16|HP_PWREN_E AC28 16
PORT_GOOD17|SHP_PERST17|HP_CLKEN_E_ AM33 17
PORT_GOOD18|SHP_PERST18|HP_PERST_E_ AN34 18
PORT_GOOD19|SHP_PERST19|HP_PWRLED_E_ AD28 19
GPIO30|HP_MRL_F_ C31
GPIO31|HP_PWRFLT_F_ B34
GPIO32|HP_BUTTON_F_ K27
GPIO33|HP_PWR_GOOD_F B33
GPIO34|HP_PRSNT_F_ M27
GPIO35|HP_ATNLED_F_ C33
PORT_GOOD20|SHP_PERST20|HP_PWREN_F M26 20
PORT_GOOD21|SHP_PERST21|HP_CLKEN_F_ A32 21
PORT_GOOD22|SHP_PERST22|HP_PERST_F_ C30 22
PORT_GOOD23|SHP_PERST23|HP_PWRLED_F_ C34 23
STRAP_RESERVED0 AM4 RSV0
STRAP_RESERVED1 AC8 RSV1
STRAP_RESERVED2 H8 RSV2
STRAP_RESERVED3 AF12 RSV3
STRAP_RESERVED4 M7 RSV4
STRAP_RESERVED5 G9 RSV5
STRAP_RESERVED6 AP5 RSV6
STRAP_RESERVED7 AC9 RSV7
STRAP_RESERVED8 AF19 RSV8
STRAP_RESERVED9 AH18 RSV9
STRAP_RESERVED10 AF10 RSV10
STRAP_RESERVED11 AD7 RSV11
STRAP_RESERVED12 AN4 RSV12
STRAP_RESERVED13 V7 RSV13
STRAP_RESERVED14 AE16
STRAP_RESERVED15 AC7 RSV15
STRAP_RESERVED17 H16 RSV17
P1V8_PLX
U116 I150
CAT25256YI
EE_CS_N
EE_DI
EE_SK
EE_DO
P1V8A_PLX
R2677 1.5K
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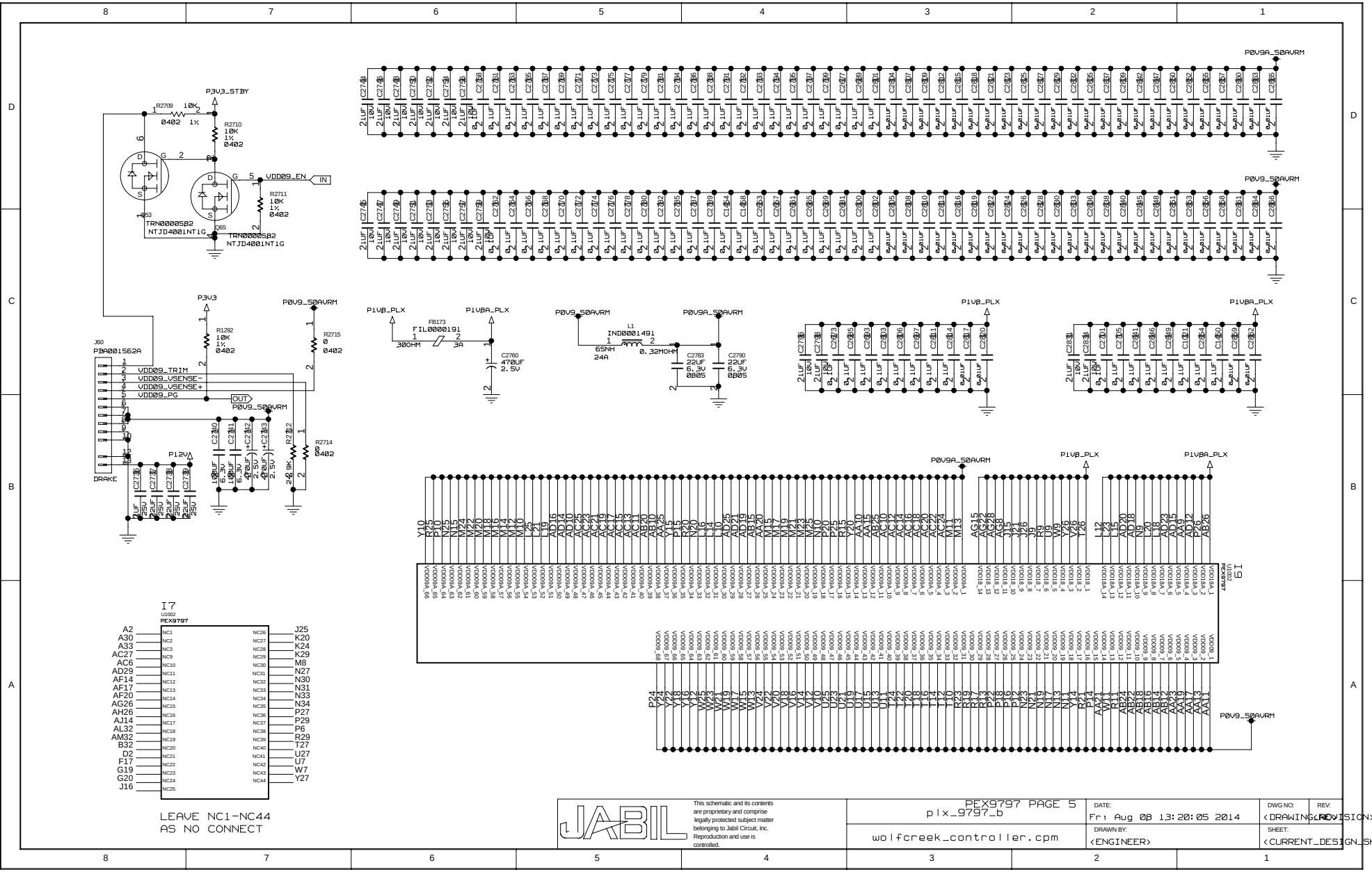
PEX9797 PAGE 4
plx_9797_b
wolfcreek_controller.cpm
DATE: Thu Aug 07 17:20:05 2014
DWG NO: <DRAWING>
REV: <REVISION>
DRAWN BY: <ENGINEER>
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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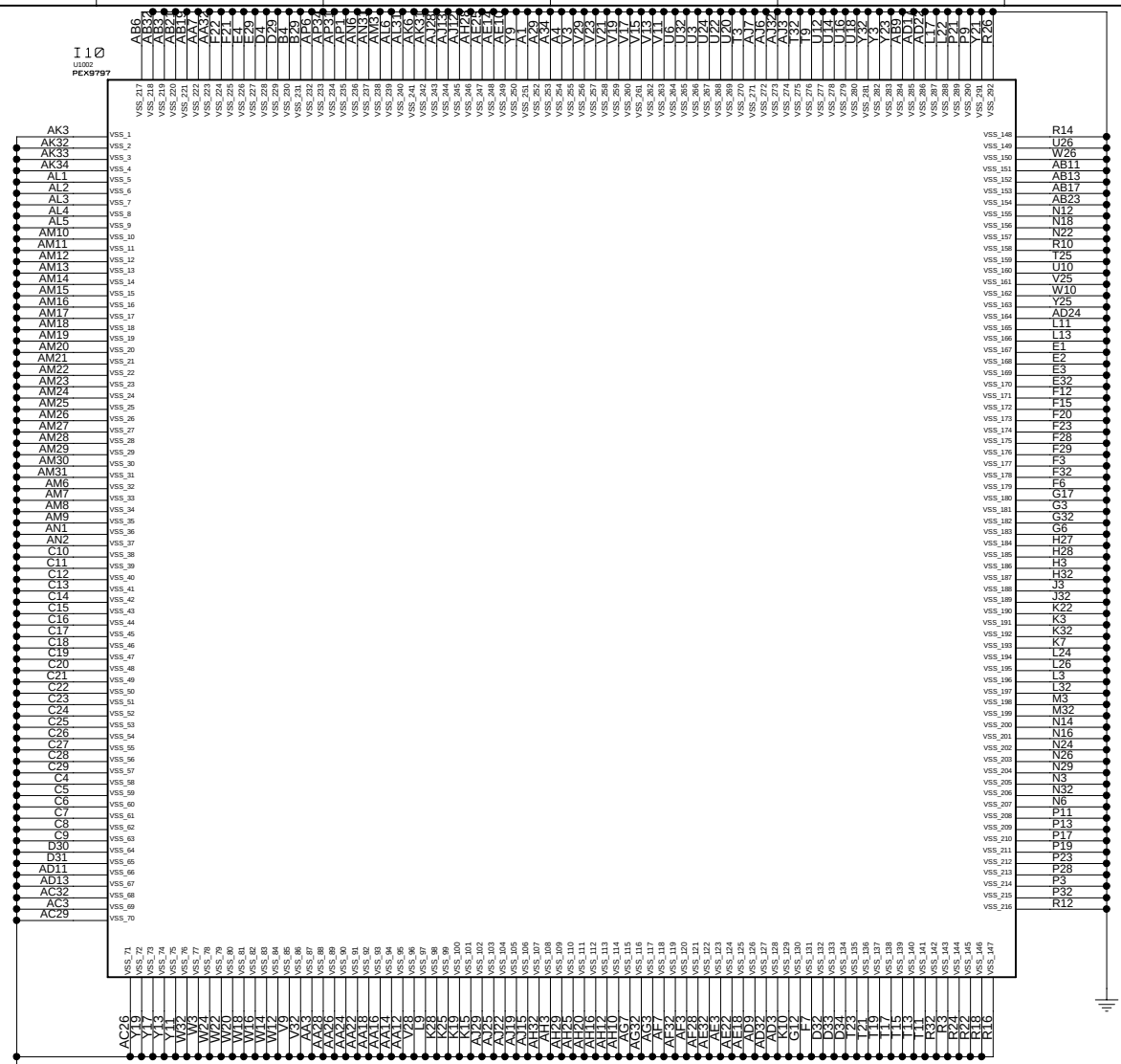
PEX9797 PAGE 5 plx_9797_b	DATE: Fri Aug 08 13:20:05 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



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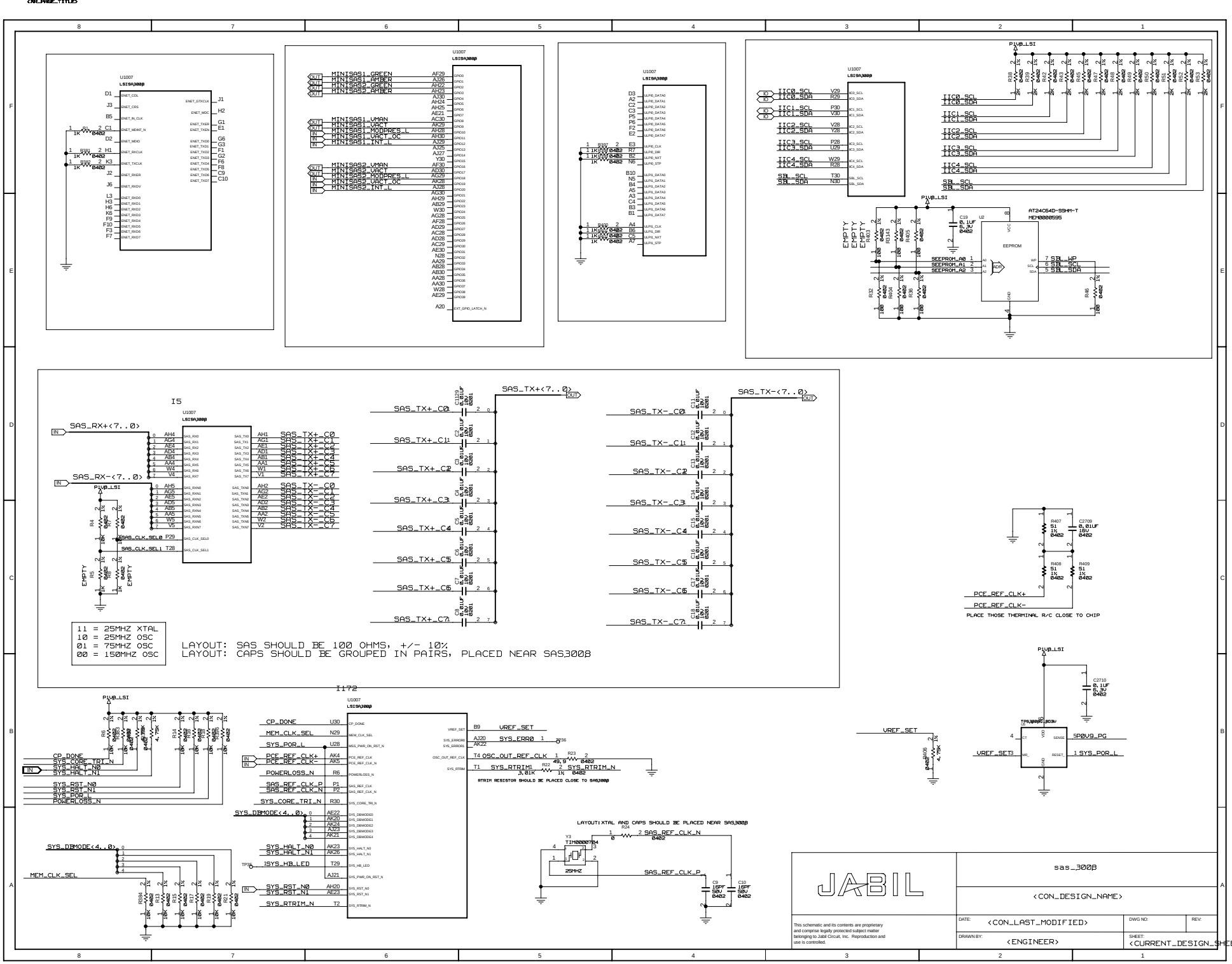
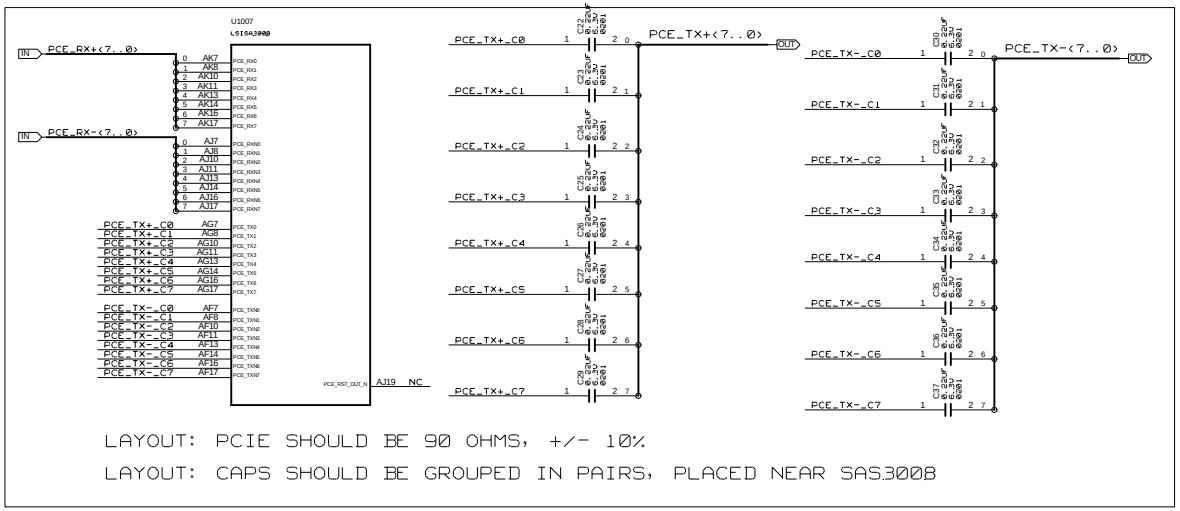
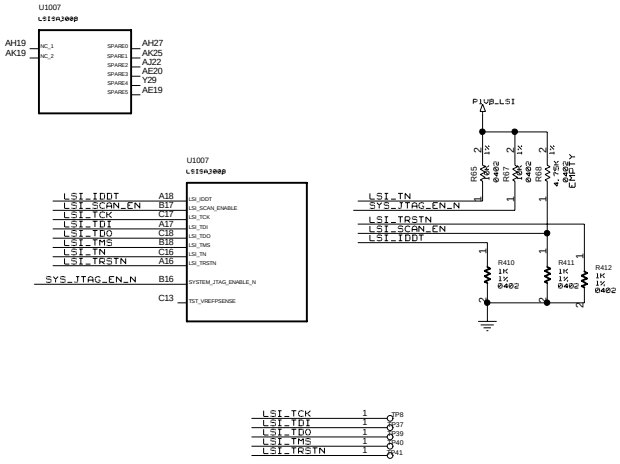
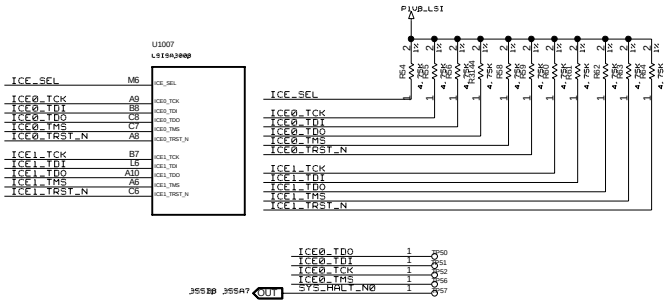
PEX9797 PAGE 6 plx_9797_b	DATE: Sat Aug 02 15:13:42 2014	DWG NO: <DRAWING>	REV: <REVISION>
wolfcreek_controller.cpm	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	



DO WE NEED TO CONNECT TESTMUX?







JABIL	sas_3008		
	<CON_DESIGN_NAME>		
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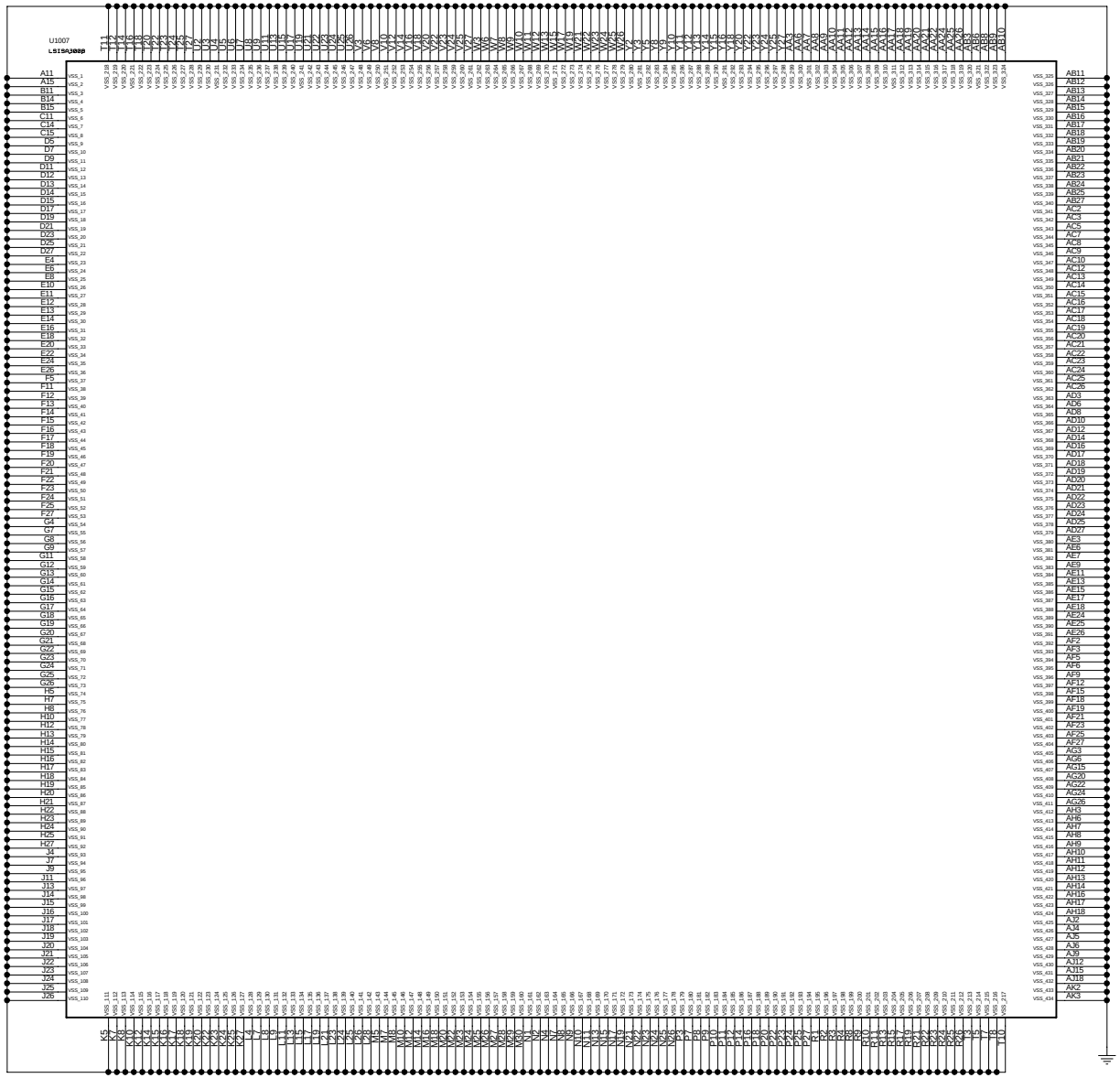
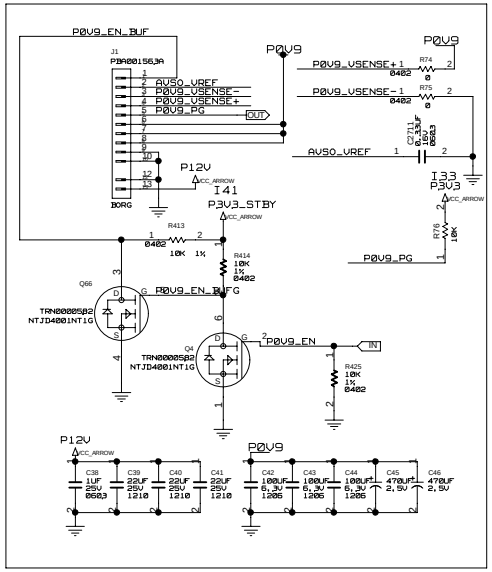
	DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	





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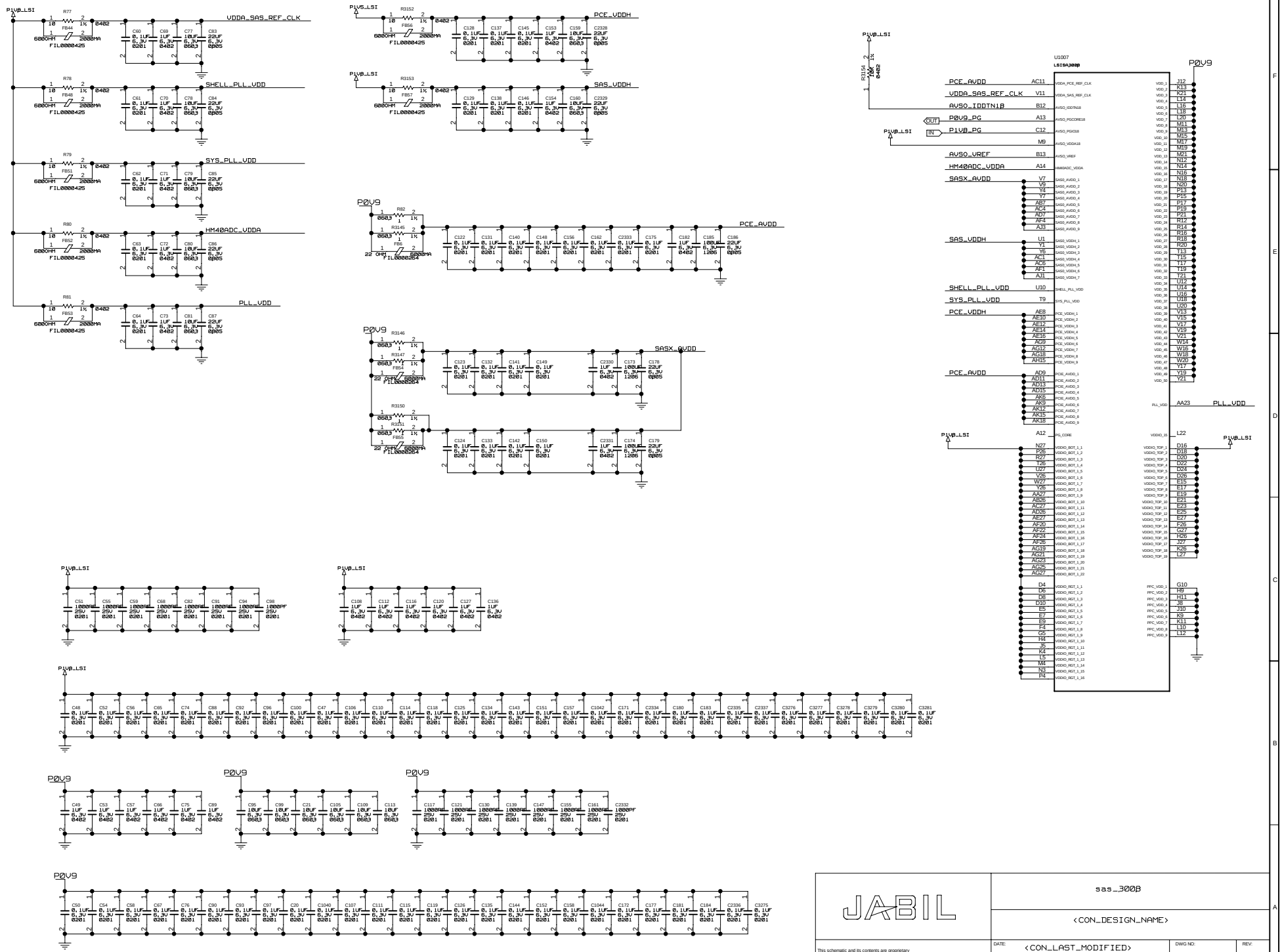
<CON_DESIGN_NAME>

DATE: <CON_LAST_MODIFIED>	DWG NO:
	REV:
DRAWN BY: <ENGINEER>	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



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sas_300B

<CON_DESIGN_NAME>

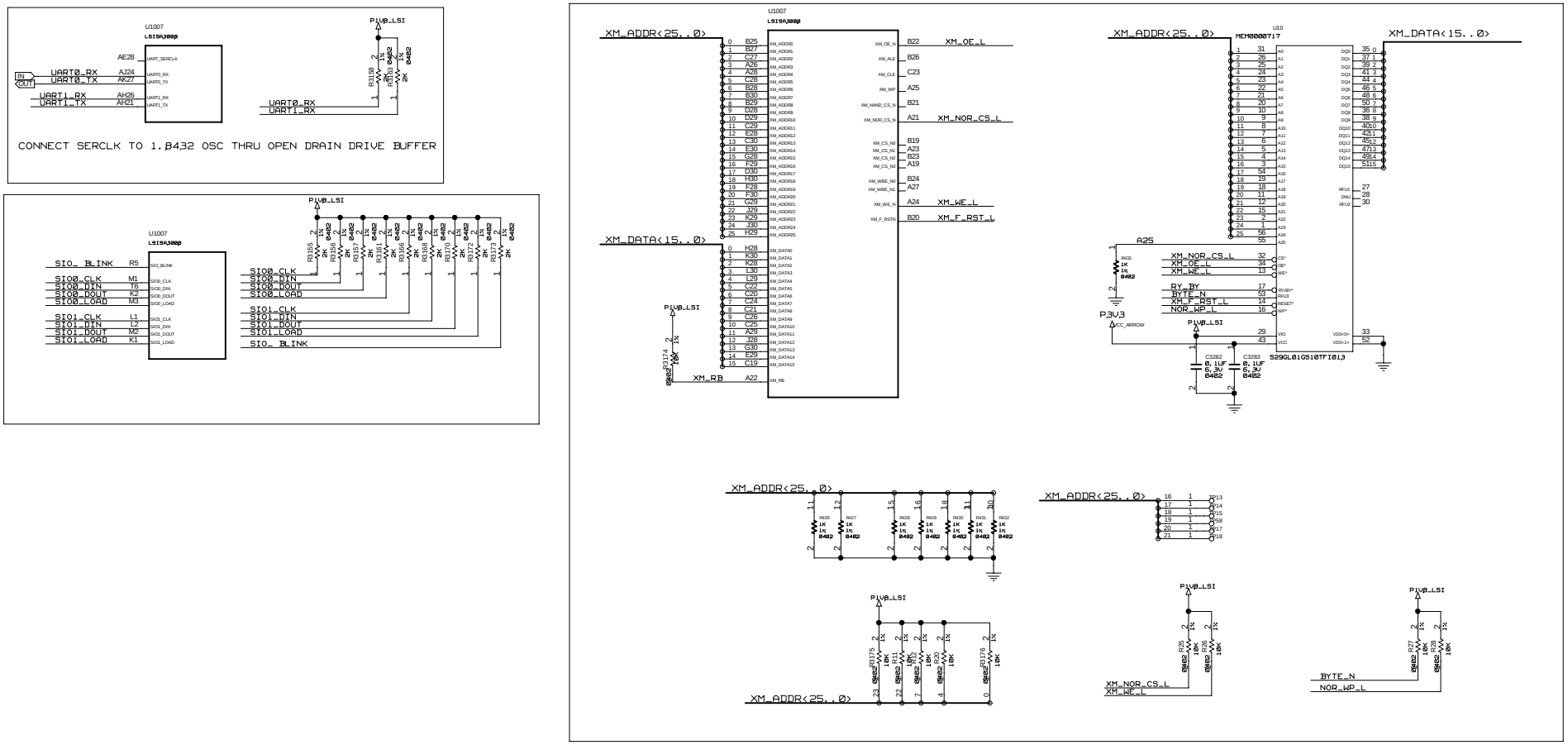
DATE: <CON_LAST_MODIFIED>

DWG NO:

REV:

DRAWN BY: <ENGINEER>

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



POWER-ON SENSE OPTIONS:

XM_ADDR[0]: SERIAL BOOTSTRAP LOADER ENABLE
  0: DISABLED
  1: ENABLED *

XM_ADDR[1]: SERIAL BOOTSTRAP ROM ADDRESS SELECT
  0: 0XA0 *
  1: 0XAB

XM_ADDR[2]: SERIAL BOOTSTRAP ROM BYTE ADDRESS SELECT
  0: START AT BYTE ADDRESS *
  1: START AT BYTE ADDRESS + 8'H80

XM_ADDR[4]: FUSION MESSAGE UNIT MDE
  0: I20 MODE
  1: FUSION MODE (MPT MODE) *

XM_ADDR[6:5]: PCIE MAXIMUM LINK SPEED
  00: 2.5G *
  01: 5.0G
  10: 8.0G
  11: RESERVED

XM_ADDR[7]: RESERVED FOR FUTURE USED. PULL HIGH

XM_ADDR[8]: RESERVED FOR FUTURE USED. PULL LOW

XM_ADDR[11]: DISABLE PCIE LANE 7 TO 4
  0: ENABLED *
  1: DISABLED AND POWERD DOWN

XM_ADDR[23:16]: AVSO MODE
  11XXXXXX: PASS VALUE FROM E-FUSE WITHOUT ADJUSTMENT *

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sas_300B

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<CON_DESIGN_NAME>			
DATE: <CON_LAST_MODIFIED>		DWG NO:	REV:
DRAWN BY: <ENGINEER>		SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	