Hat Trick CPLD Specification

Revision 0.2
12 Jun 2015

Rev	Date	Originator(s)	Change History
0.1	20-May-2015		Preliminary version
0.2	12-Jun-2015		Add Checksum for write Add Interrupt function Correct typo

Reviewed By:	Title	Date:

Table of Contents

1. Introduction

1.1 Document Purpose

This document provides the information needed to implement the functionality required of the Hat Trick CPLD. The information contained in this document, along with information contained in the referenced documents, is intended to provide all the information needed to design and develop the CPLD code.

1.2 Intended Audience

This document is primarily intended for the development team responsible for designing and implementing the CPLD code, and for the test team responsible for validating the operation of the CPLD's operation. Additionally, this document provides the information necessary for those using the CPLD.

1.3 Document Scope

The requirements contained in this document are limited to the code used to program the Lattice LCMXO2 CPLD present on the Hat Trick.

2. References, Definitions, Abbreviations, and Conventions

2.1 References

	Document Name	Version/Date	Author/Issuer
1	*Technical Note TN1204 MachX02 Programming and Configuration Usage Guide*	February 2012	Lattice Semiconductor
2	*UM10204 - I2C-Bus Specification and User Manual*	Rev. 03 19 June 2007	NXP

2.2 Definitions and Abbreviations

TERM	MEANING
CPLD	**C**omplex **P**rogrammable **L**ogic **D**evice
Drive Slot	The opening in a storage enclosure that accepts a drive with paddle.
SGPIO	**S**erial **G**eneral **P**urpose **I**nput/**O**utput
I2C	**I**nter **I**ntegrated **C**ircuit
HDD	**H**ard **D**isk **D**rive
HT CPLD	**H**at**T**rick **C**PLD
ISP	**I**n **S**ystem **P**rogramming
PCBA	**P**rinted **C**ircuit **B**oard **A**ssembly
SAS	**S**erial **A**ttach **S**CSI
SSD	**S**olid-**S**tate **D**rive
PCIe	**P**eripheral **C**omponent **I**nterconnect **E**xpress
NVMe	**N**on-**V**olatile **M**emory **E**xpress

2.3 Keywords

These keywords generally follow the definitions for such terms as outlined in IETF RFC-2119.

expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this specification.

invalid:	A keyword used to describe an illegal or unsupported bit, byte, word, field or code value. Receipt of an invalid bit, byte, word, field or code value shall be reported as an error.
mandatory:	A keyword indicating an item that is required to be implemented as defined in this specification.
may:	A keyword that indicates flexibility of choice with no implied preference (equivalent to "may or may not").
may not:	Keywords that indicates flexibility of choice with no implied preference (equivalent to "may or may not").
obsolete:	A keyword indicating that an item was defined in prior specifications but has been removed from this specification.
optional:	A keyword that describes features that are not required to be implemented to adhere to this specification. However, if an optional feature defined in this specification is implemented, it shall be implemented as defined in this specification.
reserved:	A keyword referring to bits, bytes, words, fields or code values that are set aside for future use. Their use and interpretation may be defined by future revisions of this specification. A reserved bit, byte, word, field or code value shall be set to zero. Recipients are not required to check reserved bits, bytes, words, fields or code values. Receipt of reserved code values in defined fields shall be reported as an error.
shall:	A keyword indication a mandatory requirement (equivalent to "is required to").
should	A keyword indicating flexibility of choice with a strongly preferred alternative; equivalent to the phrase "it is strongly recommended".

2.4 Editorial Conventions

Certain words and terms used in this specification had a specific meaning beyond the normal English meaning. These words or terms are defined in section 2.2 of this document or in the text where they first appear. Names of signals, phases, messages, commands, statuses, and other qualifiers are in all uppercase (e.g., REQUEST SENSE). Names of fields are in low uppercase (e.g., STATE or SPARE). Lower case is used for words having normal English meaning.

Fields that are only one bit are usually referred to as the name bit instead of the name field.

Numbers that are not immediately followed by a lower-case b or h are decimal values.

Numbers immediately followed by lower-case b (e.g., nnb) are binary values.

Numbers immediately followed by lower-case h (e.g., nnh) or are preceded with a 0x (e.g., 0xnn) are hexadecimal values.

Decimals are indicated with a period (e.g., two and one half is represented as 2.5)

Decimal numbers have a value exceeding 999 are represented with a space (e.g., 24 375)

An alphanumeric list (e.g., a,b,c or A,B,C) of items indicate that the items in the list are unordered, while a numeric list (e.g., 1,2,3) items indicate that the items in the list are ordered (i.e., item 1 must occur or complete before item 2)

In the event of conflicting information the precedence for requirements defined in this specification is:

1. text,
2. tables, then
3. figures.

3. Overall Description

3.1 Product Perspective

The HatTrick CPLDs provide I/O signal expansion for Jabil HatTrick product which is a high density storage enclosure for Open Compute Project. It can support 3.5" large form factor (LFF) SAS/SATA drives arranged 3 row x 5 column array.

3.2 Product Functions

The HatTrick CPLDs provide support for increasing I/O capacity:

- 15 drive slots supporting SAS with SFF 8680 connectors contains:
  - HDDn_INSERT_L
  - PWR_EN_HDDn_L
  - P5V_GD_HDDn
  - P12V_GD_HDDn
  - HDDn_Health_LED
  - HDDn_FAULT_LED
- 2 MiniSAS HD Module contains:
  - A/B_MODPRESL
  - A/B_INTL
  - A/B_VMAN_EN_L
  - A/B_VACT _EN_L
  - A/B_VACT_OC_L
  - A/B_Health_LED_L
  - A/B_FAULT_LED
- Enclosure and side plane signals

3.3 Operating Environment

A Lattice Semiconductor MachXO2 FPGA family device shall be used as the CPLD packaged in a 256 BGA.

3.4 Design and Implementation Constraints

There are no design or implementation constraints (such as corporate or regulatory policies, hardware limitations (timing requirements, memory requirements), interfaces to other applications, specific technologies, tools, and databases to be used, parallel operations, language requirements, communications protocols, security considerations, design conventions or programming standards, etc.) other than those imposed by other requirements specified in this document.

3.5 User Documentation

There is no user documentation required to be developed in conjunction with the CPLD code.

3.6 Assumptions and Dependencies

There are no specific assumed factors (as opposed to known facts) that could affect the requirements stated in this document.

4. Interface Requirements

4.1 Hardware Interfaces

The table below listing the signals is for the Hat Trick CPLD.

Pin	I/O Type	Function	Description
	IN	HDD1_INSERT_L	L: Drive insert; H: No Drive Inserted
	OD	PWR_EN_HDD1_L	if HDD#_INSERT_L is Low,set it as Low to enable HDD 12V/5V
	IN	P5V_GD_HDD1	H: HDD 5V is ok
	IN	P12V_GD_HDD1	H: HDD 12V is ok
	OUT	HDD1_Health_LED	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure
	OUT	HDD1_FAULT_LED	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy
	IN	HDD2_INSERT_L	
	OD	PWR_EN_HDD2_L	
	IN	P5V_GD_HDD2	
	IN	P12V_GD_HDD2	
	OUT	HDD2_Health_LED	
	OUT	HDD2_FAULT_LED	
	IN	HDD3_INSERT_L	
	OD	PWR_EN_HDD3_L	
	IN	P5V_GD_HDD3	
	IN	P12V_GD_HDD3	
	OUT	HDD3_Health_LED	
	OUT	HDD3_FAULT_LED	
	IN	HDD4_INSERT_L	
	OD	PWR_EN_HDD4_L	
	IN	P5V_GD_HDD4	
	IN	P12V_GD_HDD4	
	OUT	HDD4_Health_LED	
	OUT	HDD4_FAULT_LED	
	IN	HDD5_INSERT_L	
	OD	PWR_EN_HDD5_L	
	IN	P5V_GD_HDD5	
	IN	P12V_GD_HDD5	
	OUT	HDD5_Health_LED	
	OUT	HDD5_FAULT_LED	
	IN	HDD6_INSERT_L	
	OD	PWR_EN_HDD6_L	
	IN	P5V_GD_HDD6	
	IN	P12V_GD_HDD6	
	OUT	HDD6_Health_LED	

	OUT	HDD6_FAULT_LED	
	IN	HDD7_INSERT_L	
	OD	PWR_EN_HDD7_L	
	IN	P5V_GD_HDD7	
	IN	P12V_GD_HDD7	
	OUT	HDD7_Health_LED	
	OUT	HDD7_FAULT_LED	
	IN	HDD8_INSERT_L	
	OD	PWR_EN_HDD8_L	
	IN	P5V_GD_HDD8	
	IN	P12V_GD_HDD8	
	OUT	HDD8_Health_LED	
	OUT	HDD8_FAULT_LED	
	IN	HDD9_INSERT_L	
	OD	PWR_EN_HDD9_L	
	IN	P5V_GD_HDD9	
	IN	P12V_GD_HDD9	
	OUT	HDD9_Health_LED	
	OUT	HDD9_FAULT_LED	
	IN	HDD10_INSERT_L	
	OD	PWR_EN_HDD10_L	
	IN	P5V_GD_HDD10	
	IN	P12V_GD_HDD10	
	OUT	HDD10_Health_LED	
	OUT	HDD10_FAULT_LED	
	IN	HDD11_INSERT_L	
	OD	PWR_EN_HDD11_L	
	IN	P5V_GD_HDD11	
	IN	P12V_GD_HDD11	
	OUT	HDD11_Health_LED	
	OUT	HDD11_FAULT_LED	
	IN	HDD12_INSERT_L	
	OD	PWR_EN_HDD12_L	
	IN	P5V_GD_HDD12	
	IN	P12V_GD_HDD12	
	OUT	HDD12_Health_LED	
	OUT	HDD12_FAULT_LED	
	IN	HDD13_INSERT_L	
	OD	PWR_EN_HDD13_L	
	IN	P5V_GD_HDD13	

	IN	P12V_GD_HDD13	
	OUT	HDD13_Health_LED	
	OUT	HDD13_FAULT_LED	
	IN	HDD14_INSERT_L	
	OD	PWR_EN_HDD14_L	
	IN	P5V_GD_HDD14	
	IN	P12V_GD_HDD14	
	OUT	HDD14_Health_LED	
	OUT	HDD14_FAULT_LED	
	IN	HDD15_INSERT_L	
	OD	PWR_EN_HDD15_L	
	IN	P5V_GD_HDD15	
	IN	P12V_GD_HDD15	
	OUT	HDD15_Health_LED	
	OUT	HDD15_FAULT_LED	
	IN	A_MODPRESL	L: MiniSAS HD cable module insert; H: No Inserted
	IN	A_INTL	L: An event has occurred that requires interrupt service; H: no interrupt
	OD	A_VMAN_EN_L	L: MiniSAS HD Module power enable for device management
	OD	A_VACT _EN_L	L: MiniSAS HD Module power enable for Active cable
	IN	A_VACT_OC_L	L: MiniSAS HD Module power enable for Active cable over current
	OUT	A_Health_LED_L	L: SAS links (x4) health, H: No link or Loss of SAS links (x1 ~x3)
	OUT	A_FAULT_LED	H: Loss of SAS links (x1 ~x3), L: No SAS links or SAS links (x4) health
	IN	B_MODPRESL	
	IN	B_INTL	
	OD	B_VMAN_EN_L	
	OD	B_VACT _EN_L	
	IN	B_VACT_OC_L	
	OUT	B_Health_LED_L	
	OUT	B_FAULT_LED	
	OUT	Enclosure_Health_LED_L	L: Normal System Operation; PWM: Sled Identify; H: Others
	OUT	Enclosure _Fault_LED	H: Any failure in whole enclosure; PWM: Reserved for future use; L: Others
	IN	I2C_CLK	connect to SAS3x24 Exp I2C bus1
	BI	I2C_DATA	connect to SAS3x24 Exp I2C bus1
	OD	I2C_ALERT_L	connect to SAS3x24 Exp GPIO, L: An event has occurred required Exp to read CPLD status
	IN	RST_CPLD_L	L: Reset CPLD
	IN	sideplane HW reversion bit0	sideplane HW reversion: P0(00)/P1(01)/P2(10)

	IN	sideplane HW reversion bit1	sideplane HW reversion: P0(00)/P1(01)/P2(10)

4.2 Communication Interfaces

4.2.1 I2C Ports

The I2C ports on the CPLD shall provide an I2C-bus interface that is compliant with the *I2C-Bus Specification and User Manual* [REF 2] and operate under the following parameters:

- Only I2C Slave bus operations shall be supported.
- The I2C Slave address shall be:
  - I2C Ports C2/C3h
  - I2C programming Port: 80/81h
- The bus speed shall be Standard-mode (Sm), with a bit rate of 100kbits/s.
- Only 7-bit addressing shall be used. 10-bit addressing shall not be supported.
- General call address shall not be supported.
- Software reset shall not be supported.

5. Functional Requirements

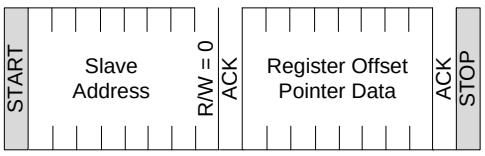
5.1 Access and Control of CPLD Signals

5.1.1 Register Offset Pointer

The CPLD shall maintain a Register Offset Pointer which is used to indicate which CPLD register is to be accessed. This value shall represent an offset into the CPLD register map. The value of the Register Offset Pointer shall be the register offset of the last register accessed incremented by one.

The default value of the Register Offset Pointer following a reset of the CPLD due to power-on or assertion of the CPLD_RESET input signal shall be 00h.

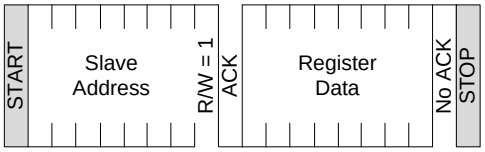
The value of the Register Offset Pointer can be set using an I2C write operation. The first byte received from an I2C Master following the slave address-R/W byte during a write operation (i.e., when the R/W bit is set to 0b) shall replace the current Register Offset Pointer value. This operation is illustrated as follows:



5.1.2 Register Read Operations

5.1.2.1 Current Register Read

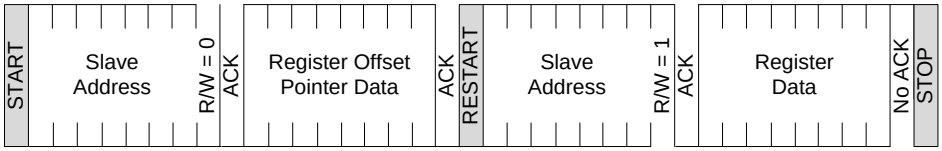
To read the data from the register currently pointed to by the Register Offset Pointer the I2C Master sends a START then Slave address-R/W byte with the R/W bit is set to 1b. The CPLD will acknowledge this and send the data for the register pointed to by the Register Offset Pointer. The Master will then terminate the transfer with a STOP condition as show below without acknowledging the byte.



If the current Register Offset Pointer value points at an invalid CPLD register offset then 00h shall be returned as the register data.

5.1.2.2 Random Register Read

To read the data from the register that is not currently pointed to by the Register Offset Pointer the I2C Master first performs a write operation to set the Register Offset Pointer to the offset of the register to be read. The I2C Master sends a START then Slave address-R/W byte with the R/W bit is set to 0b, which the CPLD will acknowledge. The I2C Master then sends a byte containing the new value for the Register Offset Pointer, which again the CPLD acknowledges. Following this a read operation is preformed using a RE-START. The I2C Master sends a START then Slave address-R/W byte with the R/W bit is set to 1b. The CPLD will acknowledge this and send the data for the register pointed to by the new Register Offset Pointer that was just received. The Master will then terminate the transfer with a STOP condition without acknowledging the byte.

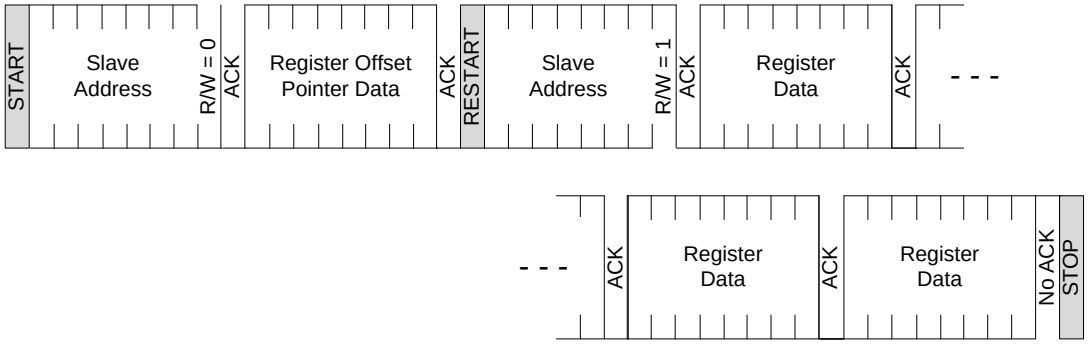


If the new Register Offset Pointer value points at an invalid CPLD register offset then 00h shall be returned as the register data.

5.1.2.3 Sequential Register Read

A sequential register read operation shall operate in a similar fashion as a current register read operation or a random read operation except that the I2C Master will acknowledge the transferred register data byte. In response to this the CPLD shall transfer the data from the next register and continue to transfer data from each sequential register until the I2C terminates the transfer with a STOP condition without acknowledging the byte.

Sequential Current Register Read



Sequential Random Register Read

If at any time during a sequential register read operation the Register Offset Pointer value points at an invalid CPLD register offset then 00h shall be returned as the register data.

5.1.3 Register Write Operations

5.1.3.1 Register Write

A register write operation will by default include setting the value of the Register Offset Pointer. The I2C Master sends a START then Slave address-R/W byte with the R/W bit is set to 0b, which the CPLD will acknowledge. The I2C Master then sends a byte containing the new value for the Register Offset Pointer, which again the CPLD acknowledges. Following this the I2C Master sends a byte that contains the data to be written into the register currently pointed to by the Register Offset Pointer. After the CPLD writes the received data into the register it issues an ACK and the I2C Master then terminates the transfer with a STOP condition.

If the new Register Offset Pointer value points at an invalid CPLD register offset then no data shall be written to any CPLD register and the Register Offset Pointer shall not be incremented.

5.1.3.2 Checksum for write

The write operation should support checksum, and the checksum value should be "0 – write data"

5.2 Interrupt

Once any change occurred on HDD Insert, P5V_GD_HDD and P12V_GD_HDD, the CPLD I2C_ALERT_L will be asserted to interrupt LSI SAS3X24R . The interrupt register (90h) will be set according which signal is changed. After LSI SAS3X24R read the interrupt register (90h), the I2C_ALERT_L should be released and the value of interrupt register should be reset.

5.3 Register Map

Offset	Field	Name	I/O	Description	Default
00h	bit0	HDD1_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit1	HDD2_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit2	HDD3_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit3	HDD4_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit4	HDD5_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit5	HDD6_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit6	HDD7_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit7	HDD8_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
01h	bit0	HDD9_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit1	HDD10_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit2	HDD11_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit3	HDD12_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit4	HDD13_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit5	HDD14_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit6	HDD15_INSERT_L	I	L: Drive insert; H: No Drive Inserted	
	bit7	Reserved		Reserved	
02h	bit0	P5V_GD_HDD1	I	H: HDD 5V is ok	
	bit1	P5V_GD_HDD2	I	H: HDD 5V is ok	
	bit2	P5V_GD_HDD3	I	H: HDD 5V is ok	
	bit3	P5V_GD_HDD4	I	H: HDD 5V is ok	
	bit4	P5V_GD_HDD5	I	H: HDD 5V is ok	
	bit5	P5V_GD_HDD6	I	H: HDD 5V is ok	
	bit6	P5V_GD_HDD7	I	H: HDD 5V is ok	
	bit7	P5V_GD_HDD8	I	H: HDD 5V is ok	
03h	bit0	P5V_GD_HDD9	I	H: HDD 5V is ok	
	bit1	P5V_GD_HDD10	I	H: HDD 5V is ok	
	bit2	P5V_GD_HDD11	I	H: HDD 5V is ok	
	bit3	P5V_GD_HDD12	I	H: HDD 5V is ok	
	bit4	P5V_GD_HDD13	I	H: HDD 5V is ok	
	bit5	P5V_GD_HDD14	I	H: HDD 5V is ok	
	bit6	P5V_GD_HDD15	I	H: HDD 5V is ok	
	bit7	Reserved		Reserved	
04h	bit0	P12V_GD_HDD1	I	HDD 12V is ok	
	bit1	P12V_GD_HDD2	I	HDD 12V is ok	
	bit2	P12V_GD_HDD3	I	HDD 12V is ok	
	bit3	P12V_GD_HDD4	I	HDD 12V is ok	

	bit4	P12V_GD_HDD5	I	HDD 12V is ok	
	bit5	P12V_GD_HDD6	I	HDD 12V is ok	
	bit6	P12V_GD_HDD7	I	HDD 12V is ok	
	bit7	P12V_GD_HDD8	I	HDD 12V is ok	
05h	bit0	P12V_GD_HDD9	I	HDD 12V is ok	
	bit1	P12V_GD_HDD10	I	HDD 12V is ok	
	bit2	P12V_GD_HDD11	I	HDD 12V is ok	
	bit3	P12V_GD_HDD12	I	HDD 12V is ok	
	bit4	P12V_GD_HDD13	I	HDD 12V is ok	
	bit5	P12V_GD_HDD14	I	HDD 12V is ok	
	bit6	P12V_GD_HDD15	I	HDD 12V is ok	
	bit7	Reserved		Reserved	
10h	bit0	PWR_EN_HDD1_L	O	HDD 12V/5V Power Enable	1
	bit1	PWR_EN_HDD2_L	O	HDD 12V/5V Power Enable	1
	bit2	PWR_EN_HDD3_L	O	HDD 12V/5V Power Enable	1
	bit3	PWR_EN_HDD4_L	O	HDD 12V/5V Power Enable	1
	bit4	PWR_EN_HDD5_L	O	HDD 12V/5V Power Enable	1
	bit5	PWR_EN_HDD6_L	O	HDD 12V/5V Power Enable	1
	bit6	PWR_EN_HDD7_L	O	HDD 12V/5V Power Enable	1
	bit7	PWR_EN_HDD8_L	O	HDD 12V/5V Power Enable	1
11h	bit0	PWR_EN_HDD9_L	O	HDD 12V/5V Power Enable	1
	bit1	PWR_EN_HDD10_L	O	HDD 12V/5V Power Enable	1
	bit2	PWR_EN_HDD11_L	O	HDD 12V/5V Power Enable	1
	bit3	PWR_EN_HDD12_L	O	HDD 12V/5V Power Enable	1
	bit4	PWR_EN_HDD13_L	O	HDD 12V/5V Power Enable	1
	bit5	PWR_EN_HDD14_L	O	HDD 12V/5V Power Enable	1
	bit6	PWR_EN_HDD15_L	O	HDD 12V/5V Power Enable	1
	bit7	Reserved		Reserved	1
20h	bit3-0	HDD1_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
	bit7-4	HDD2_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
21h	bit3-0	HDD3_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
	bit7-4	HDD4_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
22h	bit3-0	HDD5_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
	bit7-4	HDD6_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
23h	bit3-0	HDD7_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
	bit7-4	HDD8_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
24h	bit3-0	HDD9_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001

	bit7-4	HDD10_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
25h	bit3-0	HDD11_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
	bit7-4	HDD12_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
26h	bit3-0	HDD13_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
	bit7-4	HDD14_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
27h	bit3-0	HDD15_Health_LED	O	H: Drive Online and Healthy; L: No Drive Inserted or Drive Failure	0001
30h	bit3-0	HDD1_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD2_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
31h	bit3-0	HDD3_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD4_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
32h	bit3-0	HDD5_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD6_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
33h	bit3-0	HDD7_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD8_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
34h	bit3-0	HDD9_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD10_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
35h	bit3-0	HDD11_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD12_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
36h	bit3-0	HDD13_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	HDD14_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
37h	bit3-0	HDD15_FAULT_LED	O	H: Drive Failure; L: No Drive Inserted or Drive Online and Healthy	0001
	bit7-4	Reserved		Reserved	0001
40h	bit0	A_MODPRESL	I	L: MiniSAS HD cable module insert; H: No Inserted	

	bit1	A_INTL	I	L: An event has occurred that requires interrupt service H: no interrupt	
	bit2	A_VACT_OC_L	I	L: MiniSAS HD Module power enable for Active cable over current	
	bit3	B_MODPRESL	I	L: MiniSAS HD cable module insert; H: No Inserted	
	bit4	B_INTL	I	L: An event has occurred that requires interrupt service H: no interrupt	
	bit5	B_VACT_OC_L	I	L: MiniSAS HD Module power enable for Active cable over current	
50h	bit0	A_VMAN_EN_L	O	L: MiniSAS HD Module power enable for device management	1
	bit1	A_VACT _EN_L	O	L: MiniSAS HD Module power enable for Active cable	1
	bit2	B_VMAN_EN_L	O	L: MiniSAS HD Module power enable for device management	1
	bit3	B_VACT _EN_L	O	L: MiniSAS HD Module power enable for Active cable	1
60h	bit3-0	A_Health_LED_L	O	L: SAS links (x4) health H: No link or Loss of SAS links (x1 ~x3)	0001
	bit7-4	A_FAULT_LED	O	H: Loss of SAS links (x1 ~x3) L: No SAS links or SAS links (x4) health	0001
61h	bit3-0	B_Health_LED_L	O	L: SAS links (x4) health H: No link or Loss of SAS links (x1 ~x3)	0001
	bit7-4	B_FAULT_LED	O	H: Loss of SAS links (x1 ~x3) L: No SAS links or SAS links (x4) health	0001
70h	bit3-0	Enclosure_Health_LED_L	O	L: Normal System Operation PWM: Sled Identify H: Reserved	0001
	bit7-4	Enclosure _Fault_LED	O	L: Reserved PWM: Reserved H: Any failure in whole enclosure	0001
80h	bit0	sideplane HW reversion bit0	I	sideplane HW reversion: P0(00)/P1(01)/P2(10)	
	bit1	sideplane HW reversion bit1	I	sideplane HW reversion: P0(00)/P1(01)/P2(10)	
90h	bit0	HDD Insert Interrupt		H: Some HDD have been inserted or unpluged This bit will be reset after I2C read	0
	bit1	P5V_GD_HDD Interrupt		H: Some 5V Power good signal have been changed This bit will be reset after I2C read	0
	bit2	P12V_GD_HDD Interrupt		H: Some 12V Power good signal have been changed This bit will be reset after I2C read	0
F0h	bit7-0	CPLD_MAJ_VER		CPLD Major Version Number Register Identifies the major revision of the Baseboard CPLD	
F1h	bit7-0	CPLD_MIN_VER		bit<7:0> CPLD Minor Version Number Register Identifies the minor revision of the Baseboard CPLD	

F2h	bit7-0	CPLD_HDR_CHK		CPLD Header Information Checksum Register	

5.4 Signal Toggle Rates

The LED of HDD, MiniSAS and Enclosure should follow the standard toggle rate as shown below,

Signal Toggle Rate Code	State	Output Signal State
0000b	SOLID	The indicator is on.
0001b	OFF	The indicator is off.
0010b	1Hz BLINK	The indicator alternates between on and off at a 1Hz rate with a 50% duty cycle.
0011b	2Hz BLINK	The indicator alternates between on and off at a 2Hz rate with a 50% duty cycle.
0100b	4Hz BLINK	The indicator alternates between on and off at a 4Hz rate with a 50% duty cycle.
0101b	0.7S BLINK	Repeated cycle of alternating between 0.7s on and 0.7s off.
0110b	4 Hz BLINK WITH 0.5S	Repeated cycle of alternating between on and off at 4 Hz with a 50% duty cycle twice then on for a period of 500 milliseconds
0111b	4 Hz BLINK WITH 3.5S	Repeated cycle of alternating between on and off at 4 Hz with a 50% duty cycle twice then on for a period of 3.5 seconds
1000b – 1111h	Reserved	Reserved

The toggle rates provided conform to those required by *SFF-8489 Specification for Serial GPIO IBPI (International Blinking Code Pattern Interpretation)*.

6. Other Requirements

6.1 CPLD Programming

The CPLD shall support the following Lattice MachX02 programming and configuration modes (refer to *MachX02 Programming and Configuration Usage Guide* [REF 1]):

- JTAG (using the CPLD ispJTAG port)
- I2C (using the CPLD I2C Update Port)

6.2 ISP (in-system programming) online mode with PC

Before starting to program the CPLD, the user must connect to the CPLD JTAG connector on the board to a PC with ispDOWNLOAD Cable HW-USBN-2A. Power on main board, and enter standby mode or working mode for supply power to CPLD device.

User get ready for compiled JED format image, and programs JED file into HDDS CPLD device via Lattice ispVM system. For more information, refer to the document "UG48 ispDOWNLOAD Cable user's Guide" about ispVM system in lattice website.

The standard JTAG header pin-out and description is shown in the table below.

ispDOWNLOAD Cable Pin Definitions	Name	Pin Type	Description
VCC	Programming Voltage	Input	Connect to VCC plane of the target device. Typical ICC = 10mA. The board design supplies the power for VCC.
TDO	Test Data Output	Input	Used to shift data out via the IEEE1149.1 (JTAG) programming standard.
TDI	Test Data Input	Output	Used to shift data in via the IEEE1149.1 programming standard.
ispEN/PROG	Enable	Output	Enable device to be programmed.
TMS	Test Mode Select Input	Output	Used to control the IEEE1149.1 state machine.
GND	Ground	Input	Connect to ground plane of the target device
TCK	Test Clock Input	Output	Used to clock the IEEE1149.1 state machine
INIT	Initialize	Input	Indicates that ORCA device is ready for configuration.
DONE	Done	Input	An open-collector signal that indicates when configuration is complete.

6.3 ISP (in-system programming) online mode with LSI SAS3X24R

The LSI SAS3X24R can upgrade the Hat Trick CPLD using the I2C bus. The LSI SAS3X24R will support this function only when System is on. To activate the fresh image downloaded into CPLD internal flash, LSI SAS3X24R shall send the REFRESH command by using I2C, after complete to download the entire data into CPLD.