**APB Master VIP**

**Design Specification**

**Revision 0.1**

# REVISION HISTORY

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Author | Date | Description of changes |
| 0.1 | ThinhLe | 03/09/2020 | Update content 8. User Manual |
|  |  |  |  |
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|  |  |  |  |

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# Overview

# Block Diagram

# Class Diagram

# Type Description

|  |  |
| --- | --- |
| APB\_WRITE | Generate write transfer on APB bus |
| APB\_READ | Generate read transfer on APB bus |
| APB\_WRITE\_PROT | Write protection for all register |

# Class Description

## vip\_apb\_master\_transaction

## vip\_apb\_master\_sequencer

## vip\_apb\_master\_driver

**Execution process**



Figure. vip\_apb\_master\_driver execution process

APB

**\_intf.paddr     <= \_item.\_trans\_addr;**

**\_intf.pprot     <= \_item.\_trans\_prot;**

**\_intf.psel      <= '1;**

**\_intf.penable   <= '0;**

**\_intf.pwrite    <=(\_item.\_trans == APB\_WRITE);**

**//     \_intf.pwdata    <= \_item.\_trans\_wdata;**

**\_intf.pstrb     <= \_item.\_trans\_strb;**

foreach (pstrb[i])

if (\_intf.\_pstrb[i] == ‘1) begin

\_intf.\_pwdata[(8i + 7):(8i)] <= \_item.pwdata[(8i + 7):(8i)]

end

**@(posedge \_intf.pclk);**

**\_intf.penable  <= '1;**

**@(posedge \_intf.pclk);**

**while (!\_intf.pready) @(posedge \_intf.pclk);**

**\_item.\_trans\_rdata  = \_intf.prdata  ;**

**\_item.\_trans\_resp   = \_intf.pslverr ;**

## vip\_apb\_master\_agent

## vip\_apb\_master\_write

## vip\_apb\_master\_read

## vip\_apb\_write\_prot\_en

# Message list