Lab 1: Common-Source Amplifiers

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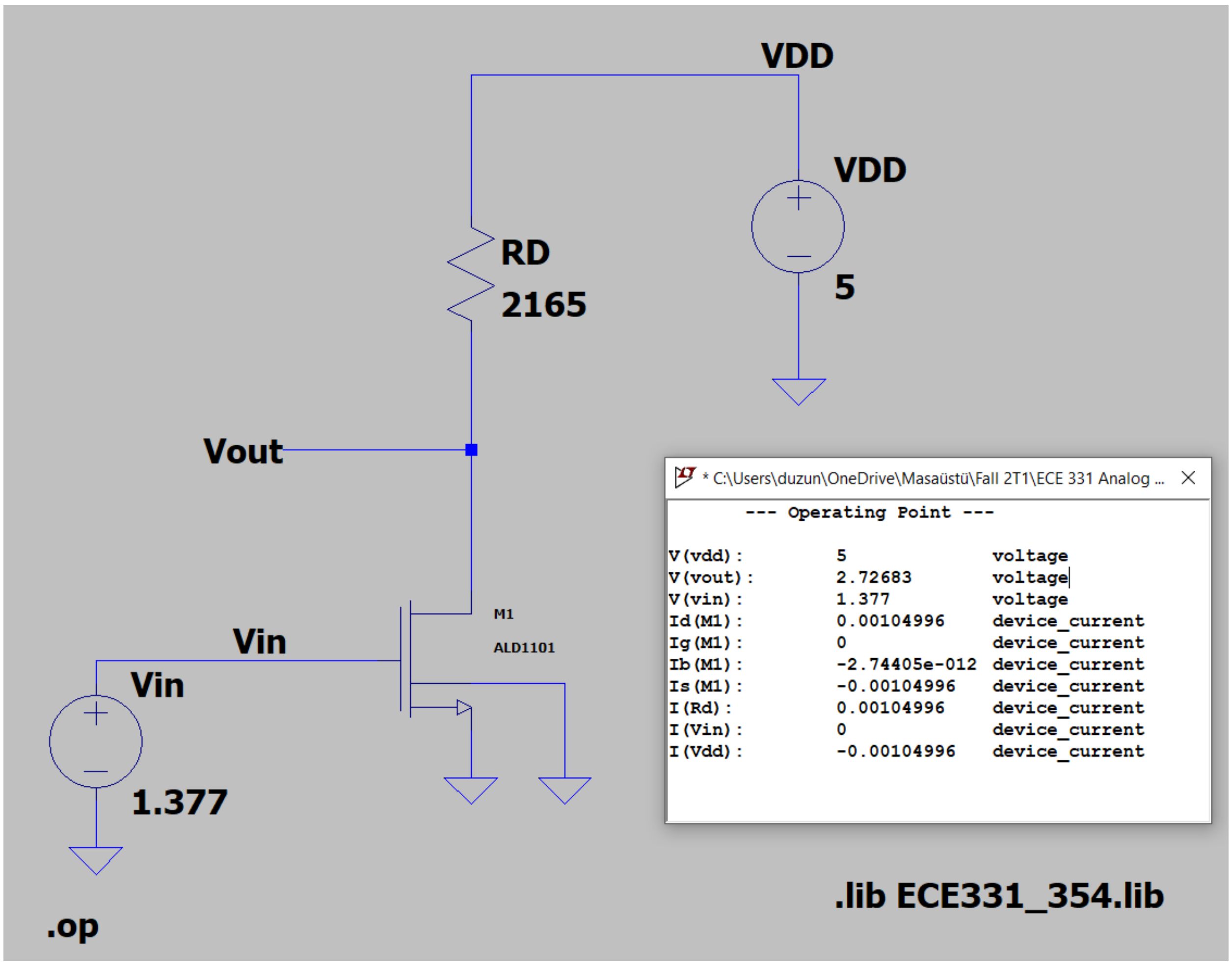
Preparation

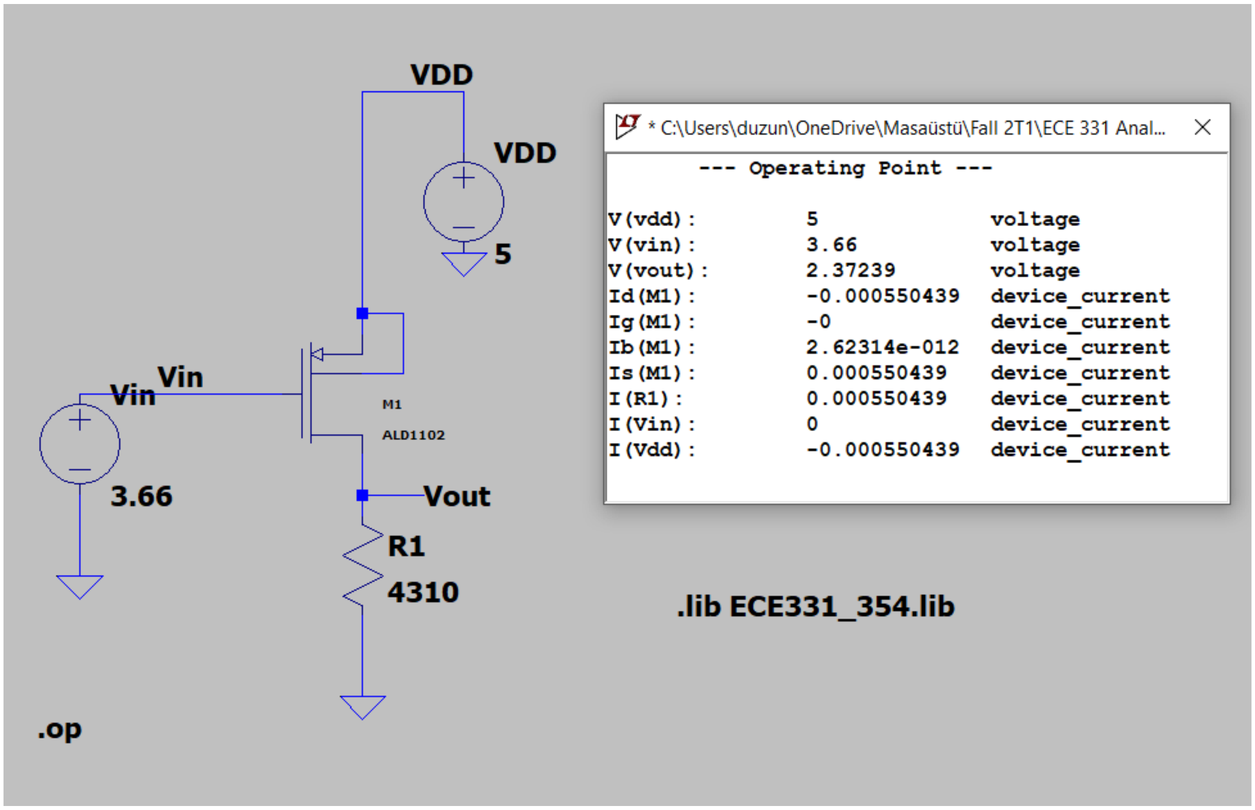
2. Design common-source amplifiers for the criteria shown in Table 1. Perform hand analysis to fill in the blanks in Table 1 using the device parameters shown in Table 2. Be careful the design procedures given above are for NMOS common-source amplifier. You may need some modifications in the equations for the PMOS common-source amplifier.

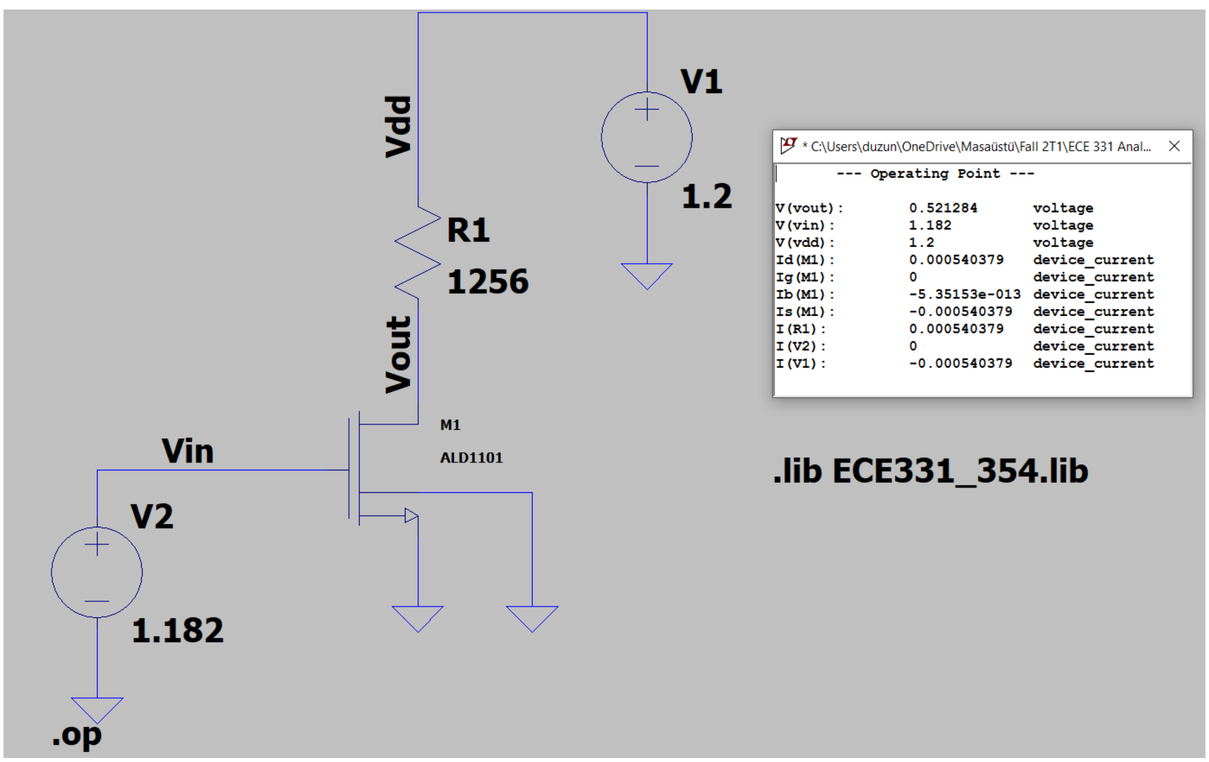
Table 1: Hand analysis table

V_{DD} (V)	Type	Gain	Swing (V_{PP})	V_{OV} (V)	I_D (A)	gm (A/V)	V_o (V)	R_D (Ω)	A_v (V/V)
5.0	NMOS	-	Max	0.667	1m	3m	2.833	2165	-6.46
5.0	PMOS	-	Max	0.69	0.5m	1.45m	2.155	4310	-6.42
1.2	NMOS	Max	0.2	0.472	0.5m	2.119m	0.571	1256	-2.66

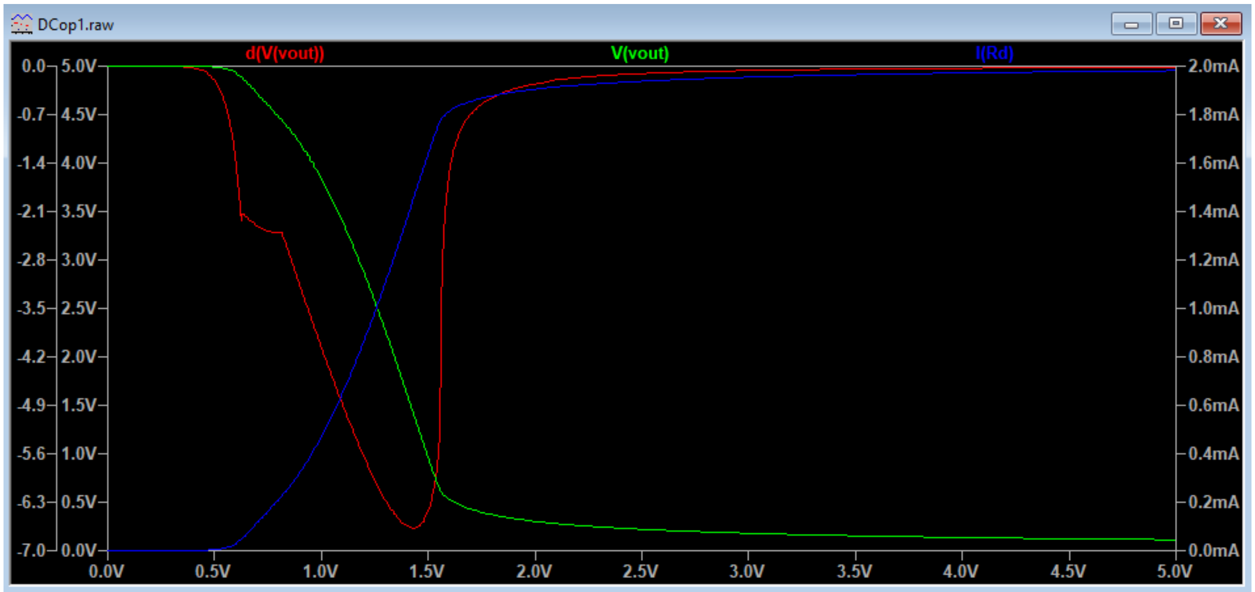
3. Perform a DC operating point simulation for the amplifiers designed above. Note that the transistor models used in simulation are far more complicated and accurate than the simple square law used for hand analysis. Therefore, some deviation from the hand analysis comes with no surprises.

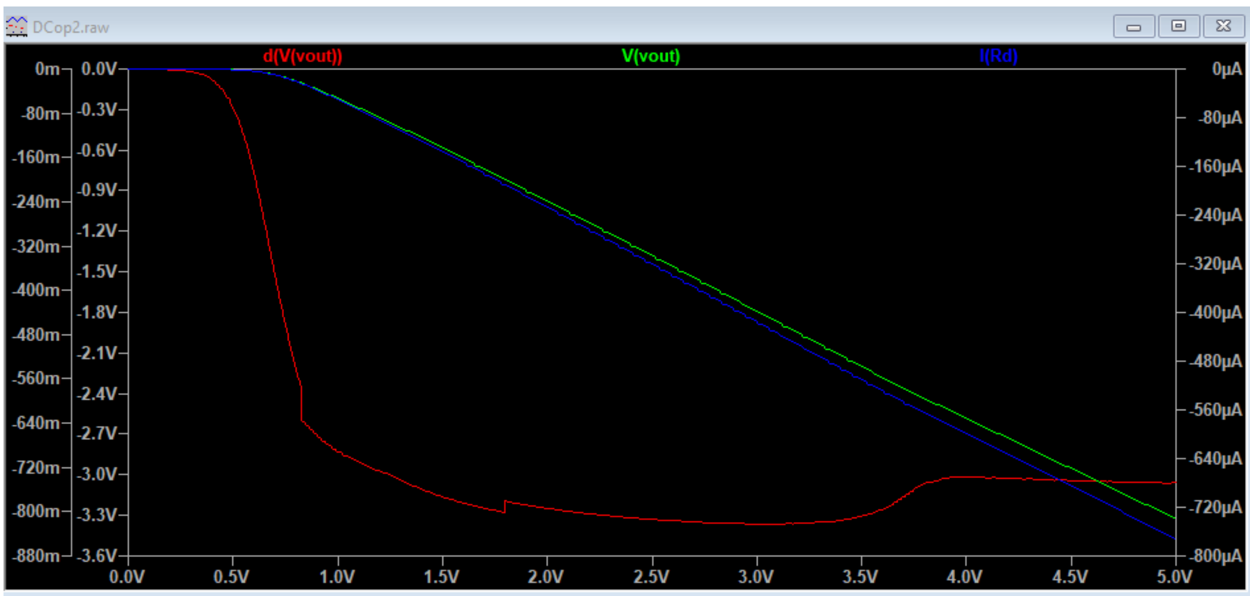


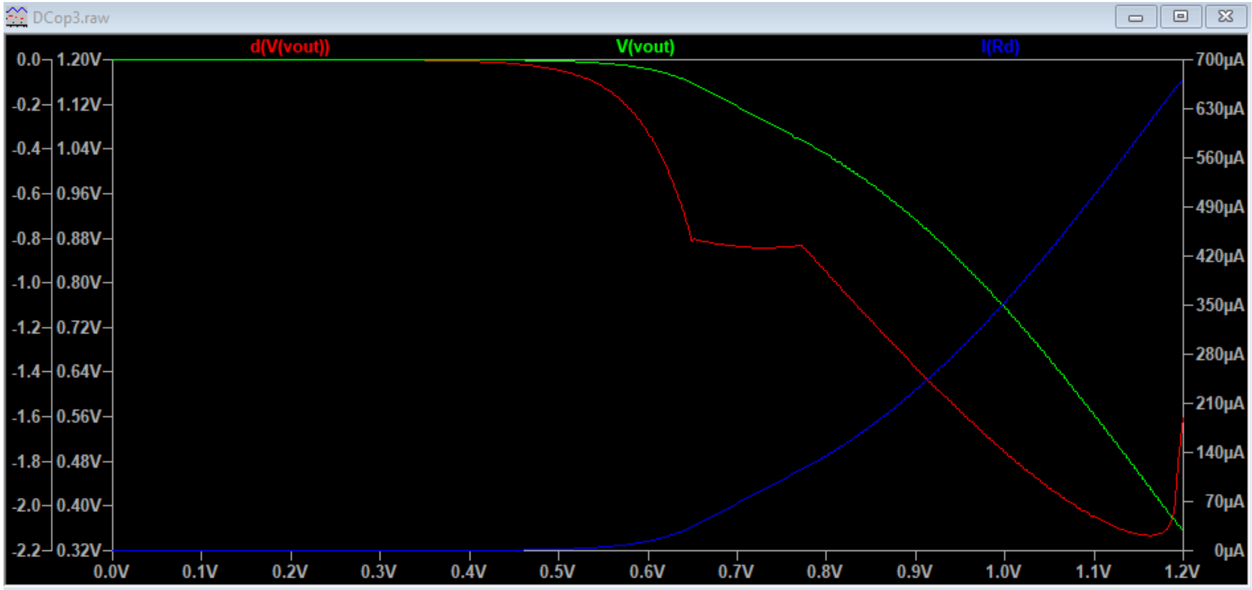




4. Perform a DC sweep to plot Vo, ID, and $dVo/dVi(= Av)$ versus Vi in the same plot window. Vi should be swept from 0 V to VDD.


DCop1.raw
d(V(vout))
V(vout)
I(Rd)
0.0 -0.7 -1.4 -2.1 -2.8 -3.5 -4.2 -4.9 -5.6 -6.3 -7.0
5.0V 4.5V 4.0V 3.5V 3.0V 2.5V 2.0V 1.5V 1.0V 0.5V 0.0V
2.0mA 1.8mA 1.6mA 1.4mA 1.2mA 1.0mA 0.8mA 0.6mA 0.4mA 0.2mA 0.0mA
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V 4.0V 4.5V 5.0V


DCop2.raw
d(V(vout))
V(vout)
I(Rd)
0m -80m -160m -240m -320m -400m -480m -560m -640m -720m -800m -880m
0.0V -0.3V -0.6V -0.9V -1.2V -1.5V -1.8V -2.1V -2.4V -2.7V -3.0V -3.3V -3.6V
0µA -80µA -160µA -240µA -320µA -400µA -480µA -560µA -640µA -720µA -800µA
0.0V 0.5V 1.0V 1.5V 2.0V 2.5V 3.0V 3.5V 4.0V 4.5V 5.0V



5. In the plots green represents Vout, red represents Av = d(Vout)/d(Vin) and blue represents ID.

   Plot 1: (at ID = 1mA)

   Vin = 1.377 V

   Vout = 2.7268 V

   Vswing = Vdd - Vov = Vdd - Vin = 5 - 1.38 = 3.62 V

   Plot 2: (at ID = 0.5mA)

   Vin = 3.66 V

   Vout = 0.653 V

   Vswing = Vdd - Vov = 5 - 0.69 = 4.31 V

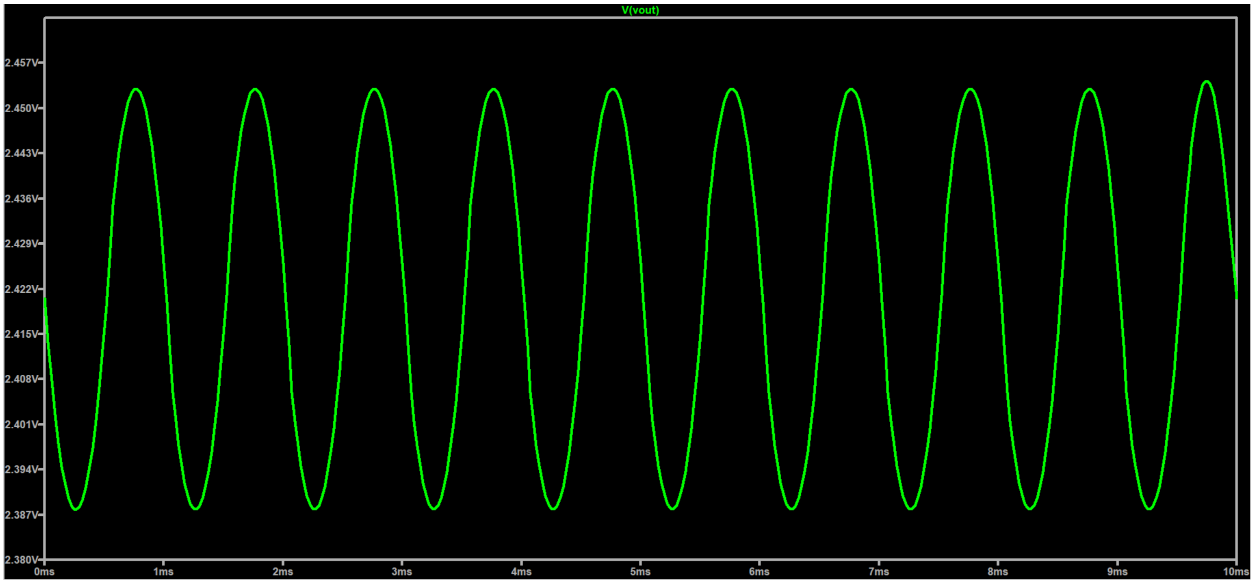
   Plot 3: (at ID = 0.5 mA)

   Vin = 1.182 V

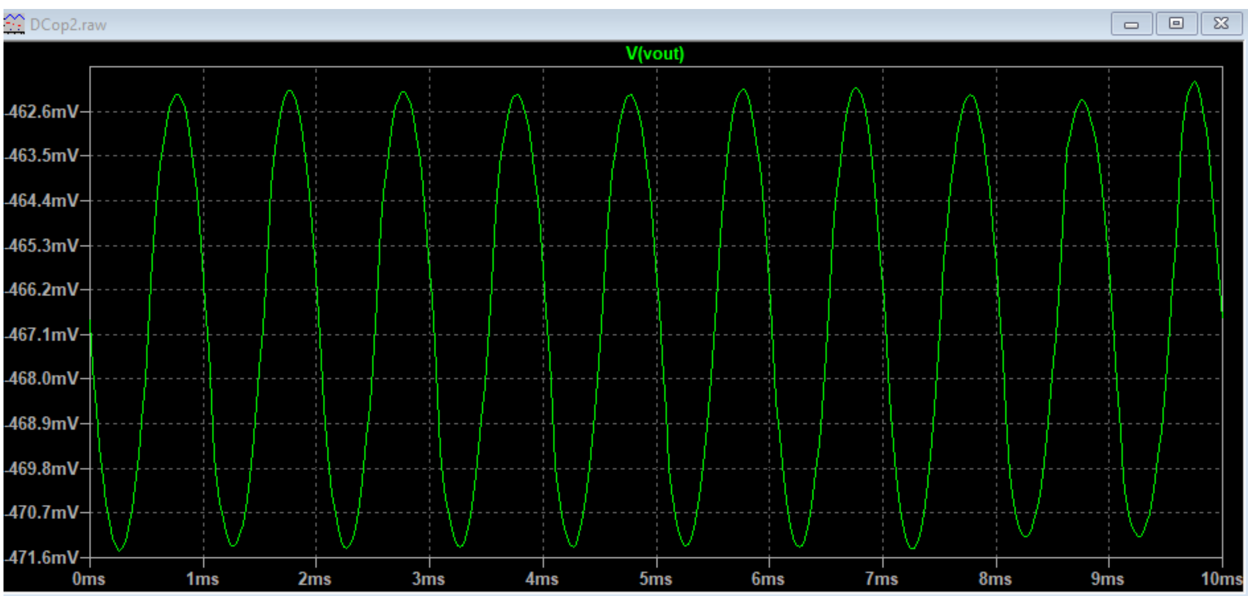
   Vout = 0.52 V

   Vswing = Vdd - Vov = 4.48 V

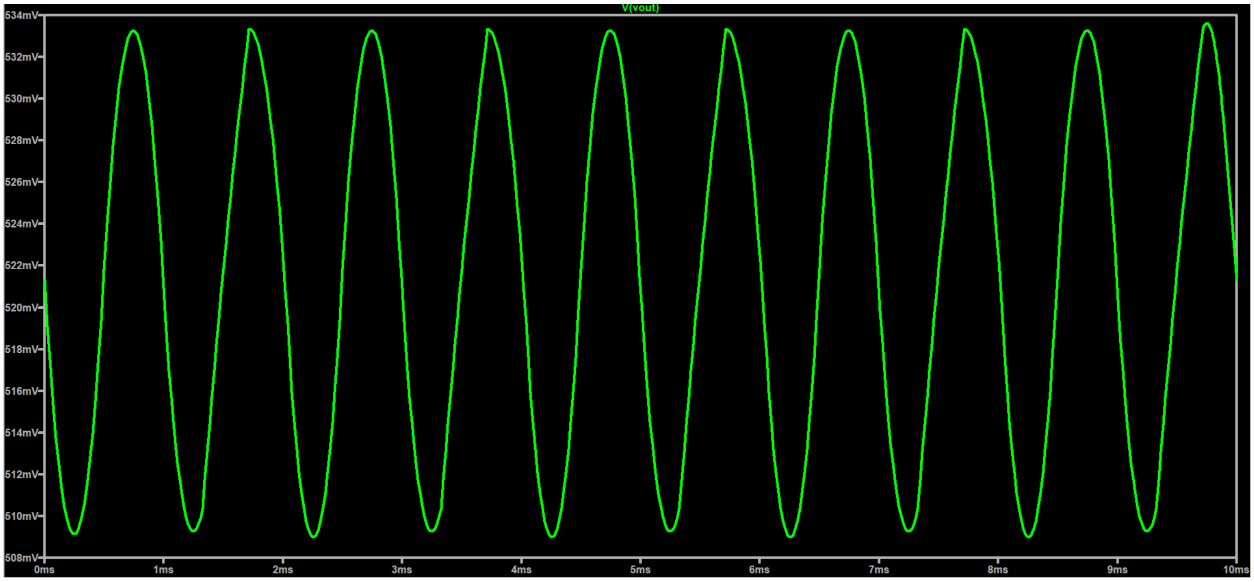
6. Perform a transient simulation to show *Vo* versus time. Use a sinusoidal voltage source at 1 kHz with 10-mVpp amplitude as the input source. Make sure that the input and thus the output are biased at the voltages found in the previous step. Verify the small-signal gain found in the previous step.



Plot 1: Small signal gain Av is approximately -4.837 V/V.



Plot 2: Small signal gain Av is approximately -6.4 V/V.



Plot 3: Small signal gain Av is approximately -2.044 V/V.

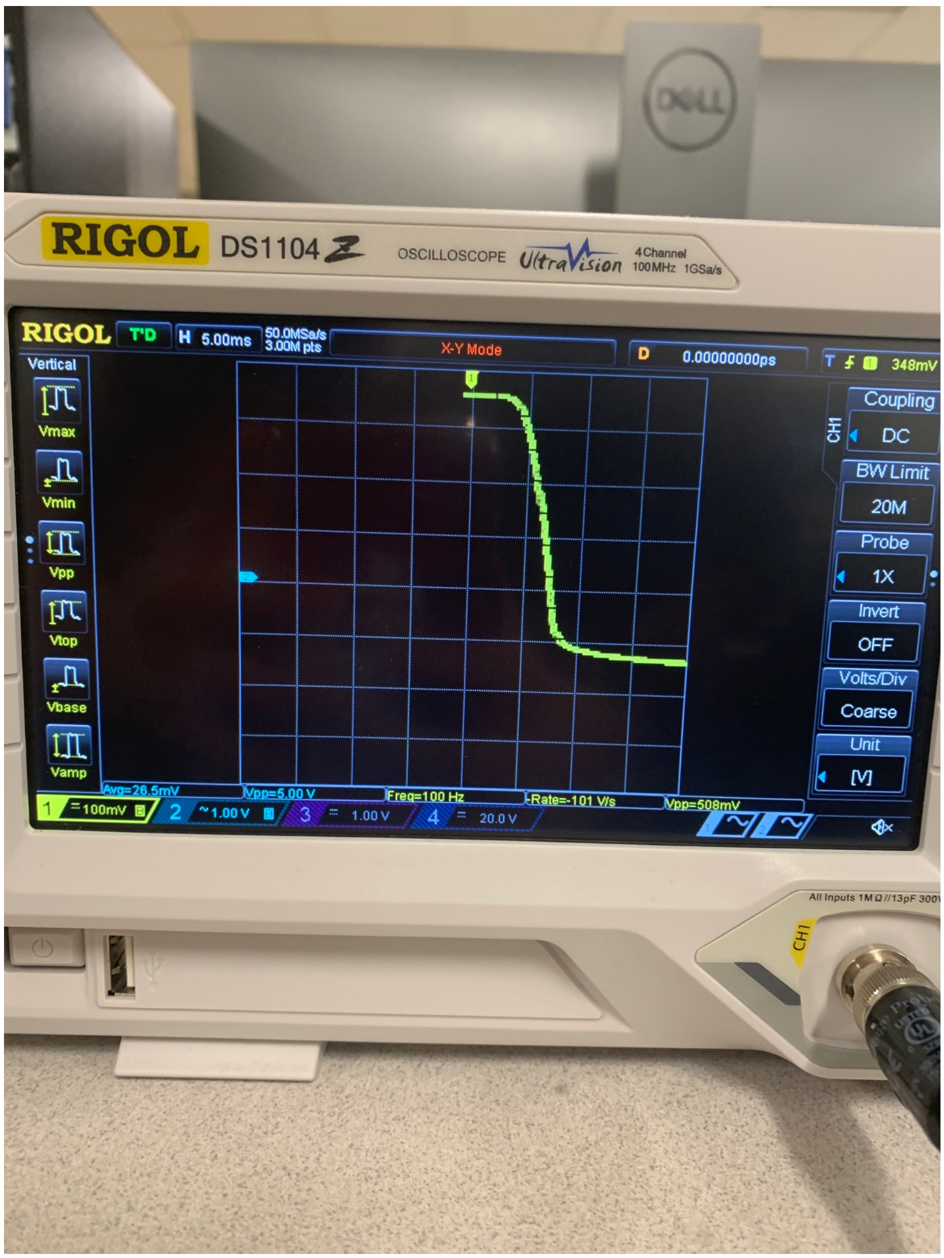
Contents up to this page will be graded within 30 minutes of the start of the lab period.

Lab - Part II: Common-Source Amplifier Implementation

1. Measuring V_o versus V_i

   Sketch a V_o versus V_i curve (or a picture of oscilloscope display) and label important points.

As we increase Vin Vout decreases. For a specific Vin we can find the corresponding Vout by using a cursor and vice versa.



Determine and record the input and output bias voltage that meets the *I_D* requirement in Table 1 and calculate the small-signal gain around that point.

V_{DD} (V)	Type	Gain	Swing (V_{PP})	I_D (A)	V_i (V)	V_o (V)	A_v (V/V)
5.0	NMOS	-	Max	1m	1.41V	2.27 V	-6.04
5.0	PMOS	-	Max	0.5m	-	-	-

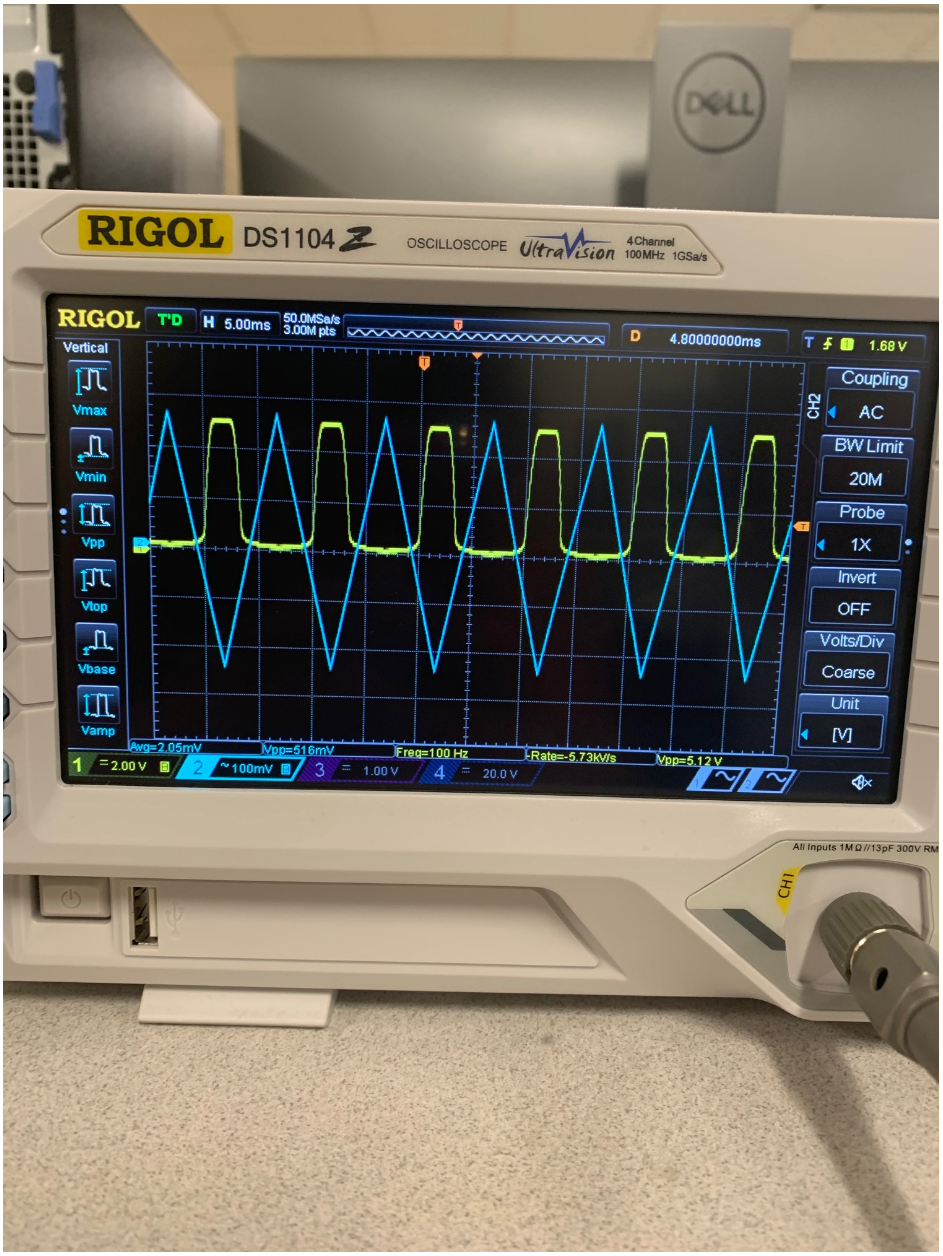
How does this compare with the simulation and hand analysis?

The results follow the finding of the simulation and hand analysis. The small differences could have been caused by approximation errors, noise and device accuracy.

2. Sinusoid testing

Put a picture showing both the input and output on the oscilloscope.

Instead of the triangle wave, we would have observed a sinusoidal waveform in the output. As we did not have enough time we have included our results for the triangular input waveform and its corresponding results.



How does the gain compare with hand analysis and simulation?