Lab 3:   Push-Pull Power Amplifier

Introduction

The common-source amplifiers in Lab 1 and Lab 2 provide a large voltage gain, but they cannot drive a low-impedance load such as an 8-Ω speaker while maintaining the gain because of the high output impedance.

The push-pull power amplifier shown in Figure 1(a) can be used as a buffer because it has a very high input impedance and low output impedance. The push-pull power amplifier is basically a combination of NMOS and PMOS source followers which are responsible for sourcing and sinking current, respectively.

The problem with the push-pull amplifier in Figure 1(a) is the dead zone in which neither of the transistors turn on. This dead zone is caused by the threshold voltages of the transistors and it introduces discontinuity in the transfer characteristics. This mode of operation with a dead zone is called class-B operation.

The dead zone can be cancelled by applying a DC bias voltage (V_{os}) across the gates of the NMOS and PMOS transistors as shown in Figure 1(b). By setting $V_{os} = V_{TN} + |V_{TP}|$, the dead zone is canceled and either NMOS or PMOS transistor is always ON. Setting $V_{os} > V_{TN} + |V_{TP}|$ would also work, but consumes more power because both the PMOS and NMOS transistors can turn on at the same time. The best bias point is where V_{os} is slightly larger than $V_{TN} + |V_{TP}|$ so the dead zone is cancelled while the power consumption is kept low. This mode of operation is called class-AB operation.

The bias voltage V_{os} can be generated with a resistor (R_1) and capacitor (C_1) in parallel as shown in Figure 1(c). The bias voltage V_{os} is simply a product of I_{D4}, which is almost constant, and R_1. The parallel capacitor C_1 provides a small-signal short between the gates of the power transistors.

IRF510 and IRF9510 are used for the push-pull amplifier in this lab because ALD1101/1102 are too weak to drive an 8-Ω load even in the push-pull configuration. ALD1102 is still used for the current mirror. Since the power transistors have a very large threshold voltage (≈ 3.5 V), a 12-V power supply is used in this lab.

Preparation

1. Determine the value of C_s for the cutoff frequency of 50 Hz or less ($f_{3dB} = 1/2\pi R_L C_s$). The power stage can be assumed as a dependent voltage source with zero output impedance.

2. Simulate the class-B push-pull power amplifier in Figure 1(a) with a 1-kHz 12-V_{pp} sinusoid input biased at 6 V and plot V_i, V_x, V_o, and I_{D1}. Simulate the circuit long enough (about
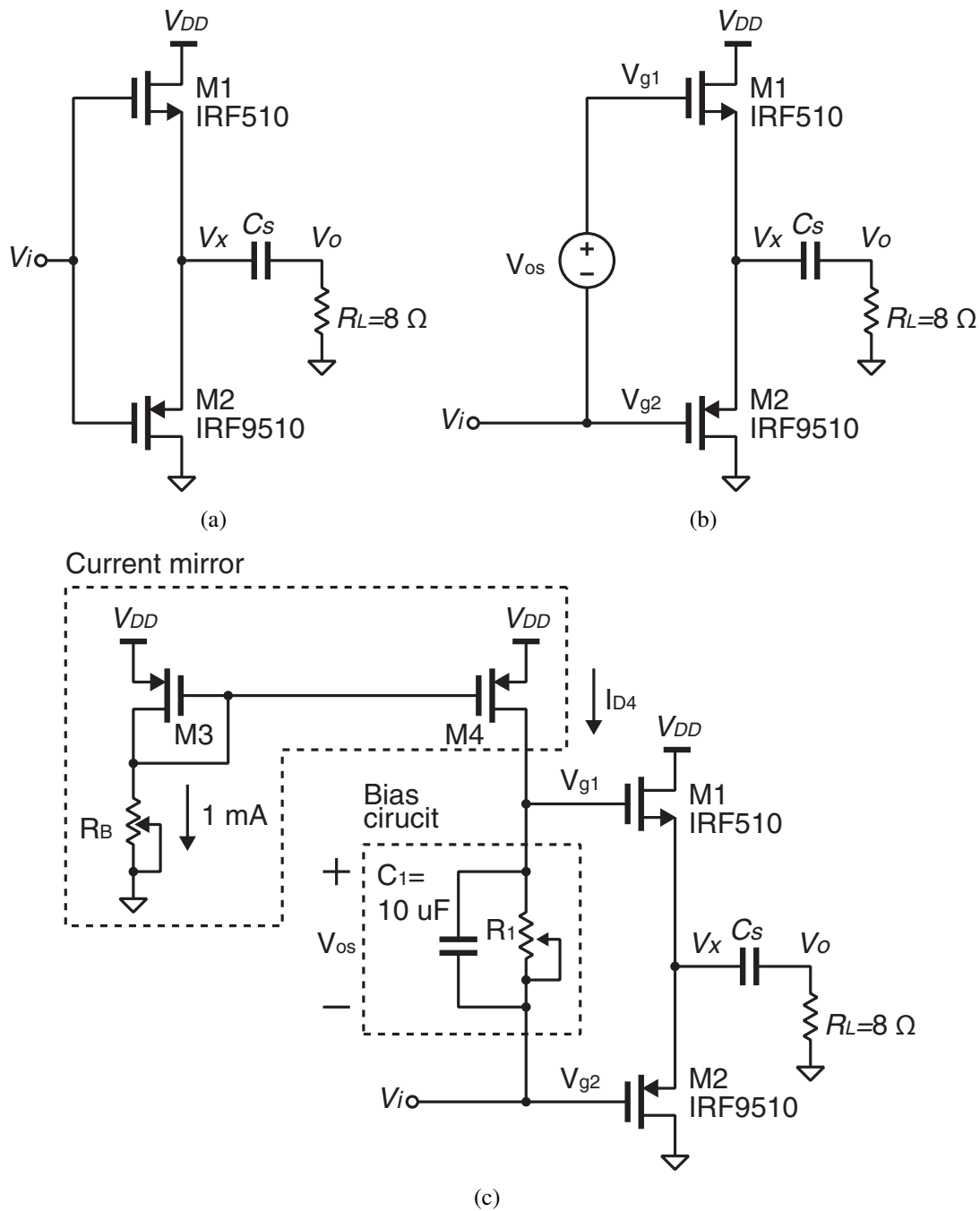
Figure 1: (a) Class B and class AB amplifiers with (b) ideal biasing and (c) bias circuit.

Table 1: Minimum parts list

Part	Description	Quantity
ALD1102	PMOS transistor pair	1
IRF510	NMOS power transistor	1
IRF9510	PMOS power transistor	1
-	C_s in Figure 1	1
-	8-Ω resistor	1
-	10-kΩ multi-turn potentiometer	3

50 ms) to let C_s settle, and zoom in to the portion close to the end of the simulation to show a few cycles of the sinusoid.

3. Determine the value of V_{os} and R_1 in Figure 1(c) required to cancel the dead zone using the plot in the previous step.

4. Simulate the class-AB push-pull amplifier in Figure 1(c) using the value of R_1 found in the previous step. Adjust the input signal source such that the output node, V_x is biased at 6 V with a 2-V$_{pp}$ swing. Plot V_i, V_x, V_o, and I_{D1}. Simulate the circuit long enough (about 50 ms) to let C_s settle, and zoom in to the portion close to the end of the simulation to show a few cycles of the sinusoid. Make sure that the power transistors are biased just in class-AB region so the power consumption is kept minimum while the dead zone is cancelled. This step requires fine tuning of R_1 as well as the input signal source.

5. Determine the voltage gain of the power amplifier.

6. Organize the results for presentation to your TA.

Lab - Part I: LTSpice Simulation Challenge

The first part of this lab will be an LTSpice simulation challenge that will be announced at the beginning of the lab session by your TA. You will work in groups of two and have 50 minutes to finish. Completing the preparation part of the lab and general knowledge of the course should be enough to finalize this part.

Lab - Part II:Class-AB Power Amplifier Implementation

1. Setup the power supply to limit the output current to 250 mA. **This step is very important for your safety** because improper biasing of the power transistors (IRF510 and IRF9510) can cause them to sink amperes of current. In such a condition, **the power transistors**

get extremely hot and they may even burn and/or pop. Set the maximum power supply current as follows:

(a) Disconnect everything from the output port of the power supply except the connection between the '-' and GND terminals.

(b) Turn the current limit to an arbitrary high value.

(c) Set the output voltage to 12 V.

(d) Turn the current limit to zero.

(e) Short the '+' and '-' terminals.

(f) Slowly crank up the current limit until the ammeter reading of the power supply reaches 250 mA.

(g) Turn off the power supply and remove the short.

(h) Turn on the power supply. Do not touch the current limit knob from this point.

If the current limiter trips during your experiment, do not crank up the current limit but fix your circuit. The power amplifier in this lab should not need more than 250 mA if wired and biased properly. **If you are not sure about this step, ask your TA for assistance before turning on the power supply.**

2. Assemble the class-AB amplifier on the breadboard.

3. Adjust R_1 to put the amplifier just in the class-AB mode. This can be done by increasing R_1 and thus V_{os} from its minimum while applying an input signal and monitoring the output on the oscilloscope until the dead zone disappears.

4. Adjust the signal generator for a 1-kHz 2-V_{pp} sinusoid biased at 6 V at the **output**.

5. Determine the voltage gain of the power amplifier.

6. Organize the results for presentation to your TA.