ECE335 Introduction to Electronic Devices

Project 2
Design of a Deep Submicron NMOS

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Introduction

This report examines the simulations of deep submicron NMOS transistors in the Sentaurus TCAD tool in our project. We investigate the relationship between various doping concentrations and their subsequent impact on the device's behavior. For example, we will design an NMOS by testing and selecting appropriate halo and source/drain extension doping concentrations to mitigate short-channel effects inherent to these small devices , 45nm gate length NMOS transistors. Our goal is to refine the design to satisfy specific I_{off} and I_{on} thresholds for two different applied voltages (V_{dd}), and observe plots in linear and saturation regimes. We will also define some key terms, discuss the effect on transistors, and compare the device's parameters against benchmarks from TSMC's paper on 65nm CMOS.

Methodology

A. Background Reading and Getting Started

The initial section of the report defines key concepts like extension doping, halo doping, and spacer. We then plot the 2D doping concentration of the NMOS transistor in Sentaurus with default values. We also integrated insights from the TSMC paper into our background research.

B. Design

We used the Sentaurus 2022 version. We first designed our NMOS transistor to desired $I_{off} \leq 35\ nA/\mu m$ and $I_{on} \geq 700\ \mu A/\mu m$ for $V_{dd} = 1V$ by changing the substrate doping concentration, dopant concentration of the extension region, and dopant concentration of the halo region. Based on the effects of these concentrations on the threshold voltage and currents, we tested various numbers in a systematic method. We plotted the linear and saturation regime currents plots using the visualization tools. Then, we designed another NMOS transistor to desired $I_{off} \leq 0.01\ nA/\mu m$ and $I_{on} \geq 445\ \mu A/\mu m$ for $V_{dd} = 1.2V$ by similarly changing the substrate doping concentration, dopant concentration of the extension region, and dopant concentration of the halo region.

Results and Discussion

A. Background Reading and Getting Started

1. *Extension doping* is created to slightly reduce channel length by extending the source and drain toward each other using low-energy dopant implants of the same dopant type as the source and drain [1]. It results in smaller channel length, increased threshold voltage, and reduced short-channel effects [1] [2].

Halo doping is done by placing the dopants just below the active channel, adjacent to the source and drain regions, in order to avoid the punch-through between the source and drain through the bulk substrate in short-channel devices [3]. The halo limits the downward, and more importantly, the lateral diffusion of the source and drain. The second advantage is that depletion width is reduced without compromising the channel threshold voltage. [1]

Spacers, also called sidewalls, insulate the drain and source metal contacts from the gate of the transistor [4]. Spacers provide a large electric field without allowing large current leakage and reduce the effect of interface traps on carrier population [4]. They enable lateral displacement of heavily doped source/drain regions from the edges of the transistor gate, which is beneficial in reducing short channel effects of submicrons and deep submicron transistors [5].

2.

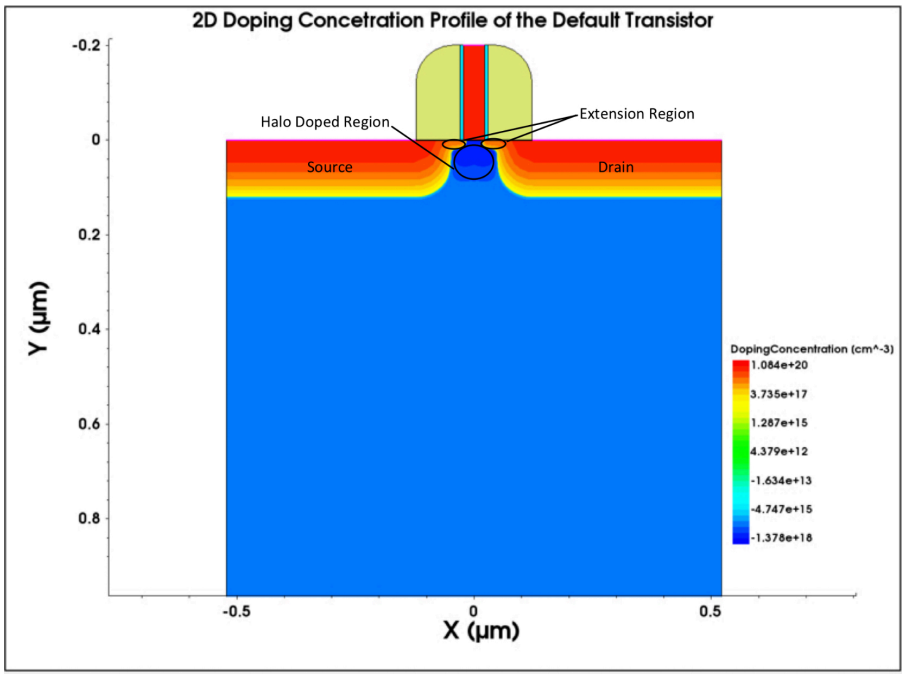

Figure 1: 2D doping concentration profile of the default N-MOSFET

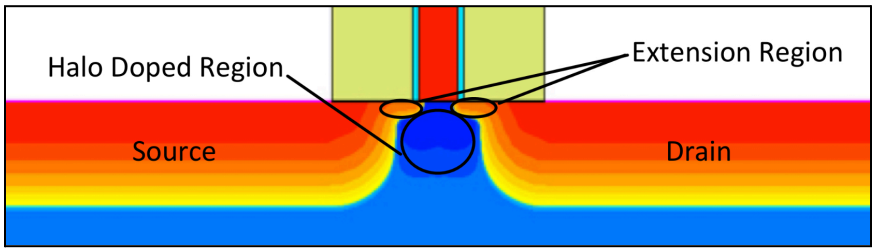

Figure 2: Magnified image of the region near the channel for the default N-MOSFET

3. From the TSMC paper [6] and electronics glossary [7]

i) LP: Low Power **ii)** G: General Purpose **iii)** HS: High Speed

iv) IO: Input/Output **v)** HVT: High Threshold Voltage **vi)** LVT: Low Voltage Threshold

4. Higher I_{on} and lower I_{off} in MOS are desirable. A higher I_{on}, which is the current when the transistor is on, implies that the transistor can deliver more current to the load, which is beneficial for performance as it allows for faster switching and higher drive capabilities. This is especially important in circuits where the transistors' speed directly affects the processing unit's overall speed. As seen in Table 1 of the TSMC paper [6], HS applications have larger I_{on} values (ex: *NMOS I_{on} in HS STD is 1010 $\mu A/\mu m$* vs. G STD is 795 μA/µm vs. in LP STD is 570 µA/µm). Whereas lower I_{off}, the current when the transistor is off, contributes to lower power consumption when the device is in standby mode, especially for high-density integrated circuits to minimize power dissipation and manage thermal issues. As seen in Table 1 of the TSMC paper [6], LP applications have lower I_{off} values (e.g. *NMOS I_{on} in LP STD is 0.2 nA/µm* vs. G STD is 26 nA/µm vs. in HS STD is 80 nA/µm).

B. Design

1. Final Design

The I_{on} and I_{off} values of our final design is I_{on} = 728.7 µA/µm and I_{off} = 29.67 nA/µm. To achieve these results the substrate doping (SubDop) was set to 9 x 10^{17} cm^{-3}, halo doping (HaloDop) was set to 3.3 x 10^{18} cm^{-3} and extension doping (ExtDop) was set to 6 x 10^{19} cm^{-3}. The design specifications, including various geometric parameters and doping parameters are given in Table 1. Labeled 2D doping concentration profile of the designed transistor and its magnified view

near the channels are presented in *Figures 3 and 4.* The Sentaurus Workbench showing the achieved device specification is presented in *Figure 5* and summarized in Table 2.

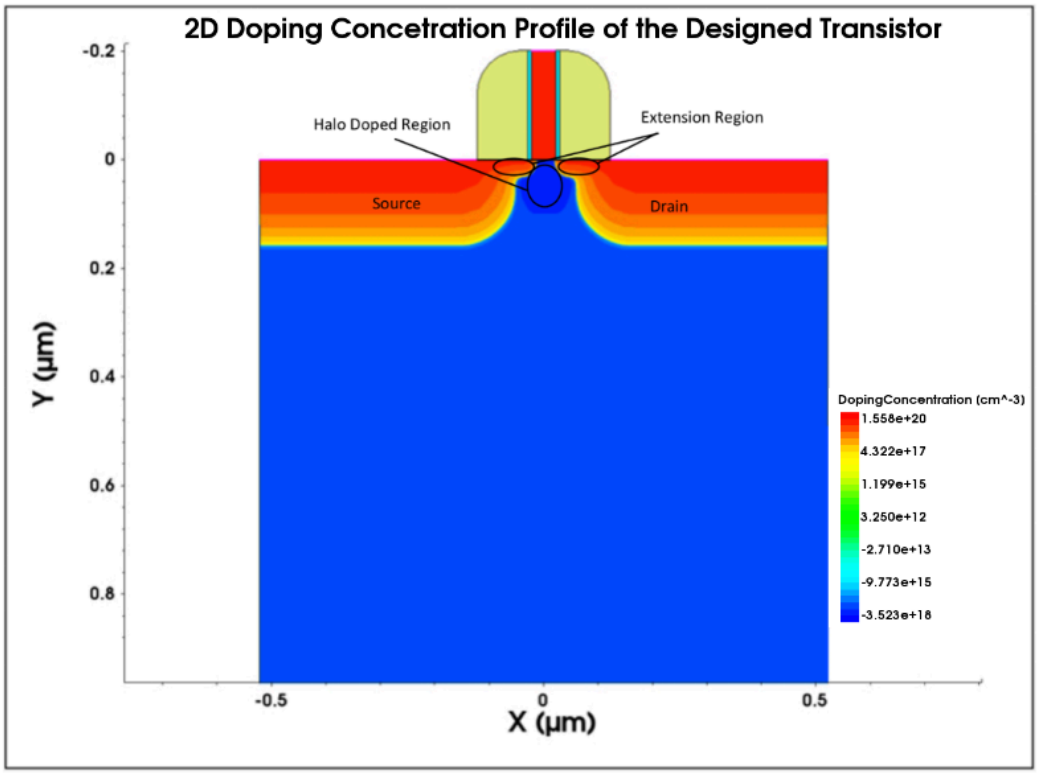

Figure 3: 2D doping concentration profile of the designed N-MOSFET

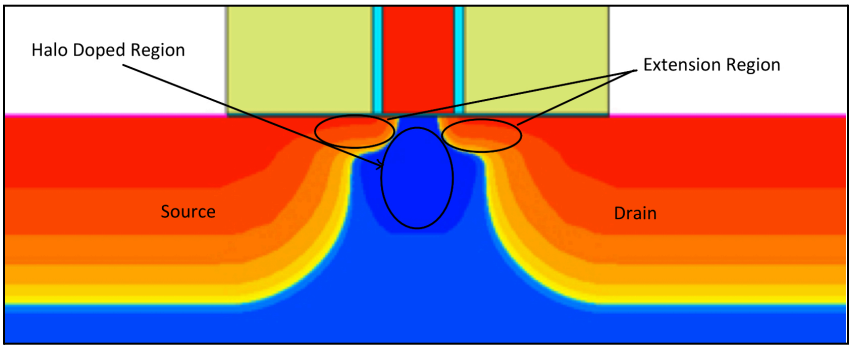

Figure 4: Magnified image of the region near the channel of the designed N-MOSFET

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.440	0.382	9.857e-05	88.525	2.473e-04	7.287e-04	2.967e-09	0.262	87.305	1.320e-03	3488.387

Figure 5: Screenshot of the Sentaurus Workbench, showing the achieved device specifications (I_{off} = 29.67 nA/µm ≤ 35 nA/µm and I_{on} = 728.7 µA/µm ≥ 700 µA/µm for V_{dd} =1V)

Table 1: Summary of transistor parameters of our final design

Parameters (notation)	**Value**
Substrate doping concentration (SubDop)	9.0×10^{17} cm^{-3}
Dopant concentration of the extension region (ExtDop)	6.0×10^{19} cm^{-3}
Dopant concentration of the halo region (HaloDop)	3.3×10^{18} cm^{-3}
Depth of the extension region (XjExt)	0.12 µm
Depth of the halo region (XjHalo)	0.07 µm
Depth of the source and drain (XjSD)	0.12 µm
Spacer Length (Lsp)	0.1 µm
Gate Thickness (Hpol)	0.2 µm
Oxide Thickness (Tox)	1.4 nm

Table 2: Summary of transistor specifications from our final design [8]

Specifications (notation)	**Value**
Threshold voltage defined as the intersection of the tangent at the maximum g_m with the V_{gs} axis (V_{tgm})	0. 440 V
Threshold voltage defined as V_{gs} at which $I_d = 100\ nA/L_g$ for $V_{ds} = V_{dlin}$ (V_{tiLin})	0.382 V
I_d at $V_{ds} = V_{dlin}$ and $V_{gs} = V_{dd}$ (I_{dLin})	9.857×10^{-5} A/µm
Subthreshold voltage swing at $V_{ds} = V_{dlin}$ (SS_{lin})	88.525 mV/decade
Maximum transconductance at $V_{ds} = V_{dlin}$ (g_{mlin})	2.473×10^{-4} S/µm
Saturation current I_d at $V_{ds} = V_{gs} = V_{dd}$ (I_{dSat})	7.287×10^{-4} A/µm
Off-state (drain-leakage) current I_d at $V_{ds} = V_{dd}$ and $V_{gs} = 0$ V (I_{off})	2.967×10^{-9} A/µm
Threshold voltage defined as V_g at which I_d = 100 nA/L g for $V_{ds} = V_{dd}$ (V_{tiSat})	0.262 V
Subthreshold voltage swing at $V_{ds} = V_{dd}$ (SS_{sat})	87.305 mV/decade
Maximum transconductance at $V_{ds} = V_{dd}$ (g_{mSat})	1.320×10^{-3} S/µm
On-state output resistance (R_{on})	3488.387 Ωµm

2. Design Process

In this section we will summarize the impactful changes we have conducted. We began our design process for the NMOS transistor with the default parameters listed in Table 1 with the default values of the substrate, halo, and extension regions.

```
(define SubDop  1e17 ); (define HaloDop 1.5e18 ); (define ExtDop 1e19) ; [1/cm3])
```

The respective transistor specification and their values are seen below:

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.220	0.200	5.265e-05	80.637	1.605e-04	5.163e-04	1.828e-07	0.093	83.261	7.030e-04	4705.770

Figure 6: Screenshot of the Sentaurus Workbench of the default transistor

As seen from the specifications, I_{dsat} was lower than our desired values, and I_{off} was higher than desired values. Hence, increasing or lowering *both* currents simultaneously would not have fixed this issue, that is, I_{on} should increase while I_{off} should decrease. Therefore, in our first iteration we focused on increasing the substrate doping to increase the threshold voltage, thereby reducing I_{off}. Usually, increasing threshold voltage reduces I_{on}, however, during short channel effects, it is possible to see the beneficial increase in I_{on}, as seen from the specifications below. After several iterations and evaluations, we settled on a substrate doping of $9 \times 10^{17}\ cm^{-3}$.

```
(define SubDop  9e17 ); (define HaloDop 1.5e18 ); (define ExtDop 1e19) ; [1/cm3])
```

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.246	0.212	6.850e-05	84.772	1.866e-04	6.157e-04	1.358e-07	0.108	85.889	8.531e-04	4582.454

Figure 7: Screenshot of the Sentaurus Workbench of the 1st iteration

In our second iteration, our focus was on increasing I_{on}. We raised I_{on} by enhancing the extension doping, because increasing the extension doping enhances the electrical conductivity in the source/drain extensions, thereby reducing the series resistance and allowing more current to flow, which increases I_{on}. This indeed increased I_{off} as well, but we will fix that in our next iteration.

```
(define SubDop  9e17 ); (define HaloDop 1.5e18 ); (define ExtDop 6e19) ; [1/cm3])
```

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.236	0.170	1.227e-04	96.169	2.708e-04	1.107e-03	1.917e-06	0.007	111.039	1.455e-03	2025.854

Figure 8: Screenshot of the Sentaurus Workbench of the 2nd iteration

In our third iteration, our focus was on decreasing I_{off}. By increasing the doping concentration of the halo region, we raised the threshold voltage in the lateral direction under the gate edges, which helped to reduce I_{off}. Since this was our last parameter to change, we used a systematic tabular format to test different values for halo doping, reaching the desired current values at a halo doping of $3.3 \times 10^{18}\ cm^{-3}$.

```
(define SubDop  9e17); (define HaloDop 3.3e18); (define ExtDop 6e19) ; [1/cm3])
```

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.440	0.382	9.857e-05	88.525	2.473e-04	7.267e-04	2.967e-09	0.262	87.305	1.320e-03	3488.387

Figure 9: Screenshot of the Sentaurus Workbench of the 3rd and final working iteration

3. Final Design Plots for I_d vs. V_{gs}

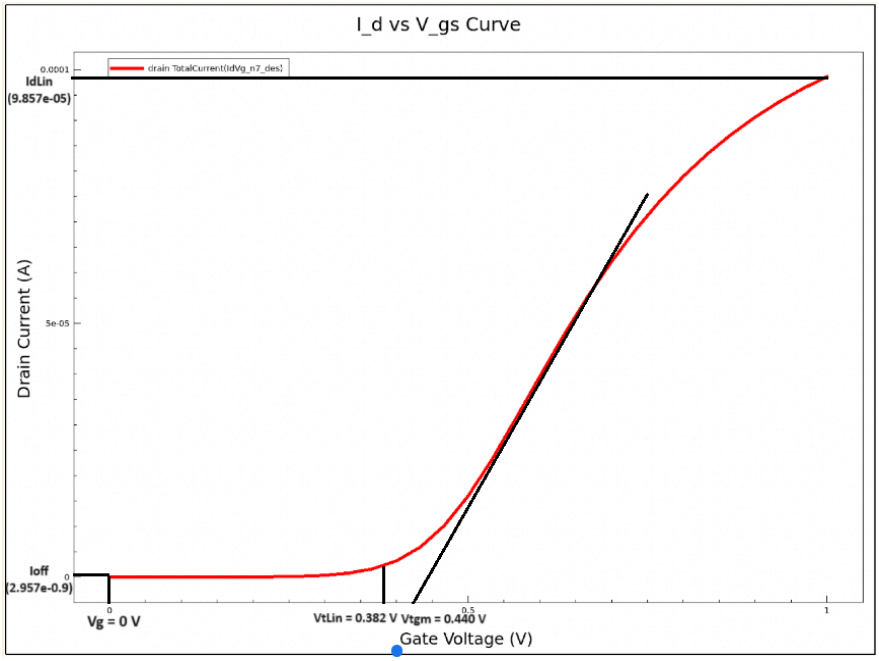

Figure 10: I_d vs. V_{gs} curve where $0 < V_{gs} < V_{dd}$ for V_{ds} = 50 mV (Linear region) V_{tLin} = 0.382 V, I_{off} = 2.967 x 10^{-9} A and I_{dLin} = 9.857 x 10^{-5} A is marked on the plot.

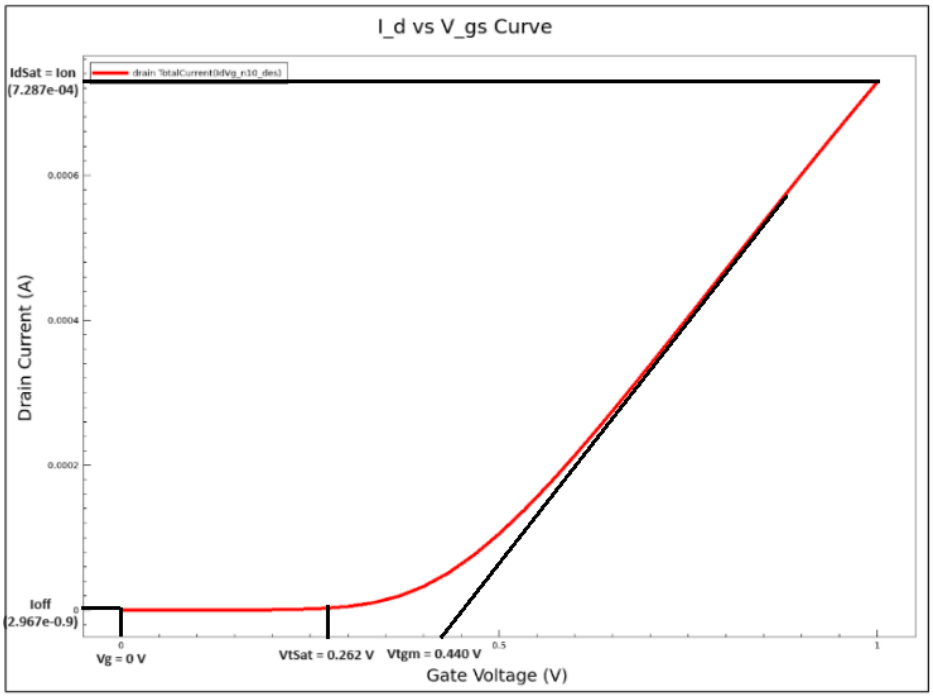

Figure 11: I_d vs. V_{gs} curve where $0 < V_{gs} < V_{dd} = V_{ds} = 1V$ (Saturation) V_{tSat} = 0.262 V, V_{tgm} = 0.440 V, I_{off} = 2.967 x 10^{-9} A (where V_{gs} = 0 V & $V_{ds} = V_{dd}$) and $I_{on} = I_{dSat}$ = 7.287 x 10^{-4} A (where $V_{gs} = V_{ds} = V_{dd}$ = 1V) is marked on the plot.

The threshold voltage in the saturation region (V_{tSat} = 0.262 V) is lower compared to the threshold voltage (V_{tLin} = 0.382 V) in the linear region. This means the transistor enters saturation at a lower V_{gs}. The drain current is significantly higher at the same V_{gs} in saturation compared to the linear region, as shown by values of I_{dSat} *and* I_{dLin}. I_{off}, where the gate voltage is 0, is the same for both regions, whereas I_{on} is determined by I_{dSat}. The threshold voltage V_{tgm} (0.440 V) is at the intersection of the tangent at the maximum g_m with the V_{gs} axis.

4. Comparison to TSMC Paper

Based on the results of our final design in *Figure 9,* the subthreshold swing, SS_{lin} = 88.525 mV/decade, and SS_{sat} = 87.305 mV/decade. As stated in the TSMC paper, these values are below 100 mV/decade. Additionally, based on *Figure 9,* our linear threshold voltage, V_{tiLin} = 0.382 V, and saturation threshold voltage, V_{tiSat} = 0.262 V. In TSMC paper's Figure 4 [6], tracing the 65nm gate length for NFET values we find V_{tLin} = 0.2 V, V_{tSat} = 0.15 V. The trend is of course the same, that is threshold voltage is smaller at saturation than at linear. The values of TSMC are both smaller than ours, this discrepancy may be due to the differences between our ideal simulation setup vs a real physical testing environment of TSMC manufacturing. Physical testing often reveals a lower threshold voltage compared to simulations due to non-idealities and variations that are difficult to capture in simulations.

5. Drain-Induced Barrier Lowering

Drain induced barrier lowering (DIBL) is a short-channel effect in MOSFETs that reduces the threshold voltage of the transistor at higher drain voltages. This effect is negligible in long-channel transistors because the channel formation's 'bottleneck' is sufficiently distant from the drain, ensuring that the drain's electric field does not significantly influence it. In such a scenario, the substrate and gate effectively shield the threshold voltage from any impact of the drain voltage. However, this is no longer true in short-channel devices. The drain is close enough to gate the channel, so a high drain voltage can open the bottleneck and turn on the transistor prematurely [9]. If a high drain voltage is applied, the barrier height can decrease, leading to an increased drain current [10]. We used the equations below to find our design's DIBL [10].

$$DIBL = \frac{\Delta V_{th}}{\Delta V_d} = \frac{|VtiSat - VtiLin|}{\left|Vds_{saturation} - Vds_{linear}\right|} = \frac{|0.262\ V - 0.382\ V|}{|1\ V - 0.05\ V|} = 126\ mV/V$$

A smaller DIBL effect implies that the transistor has better control over the premature turn-on process and is less sensitive to changes in the drain voltage.

6. Final Design Plot for I_{ds} vs. V_{ds}

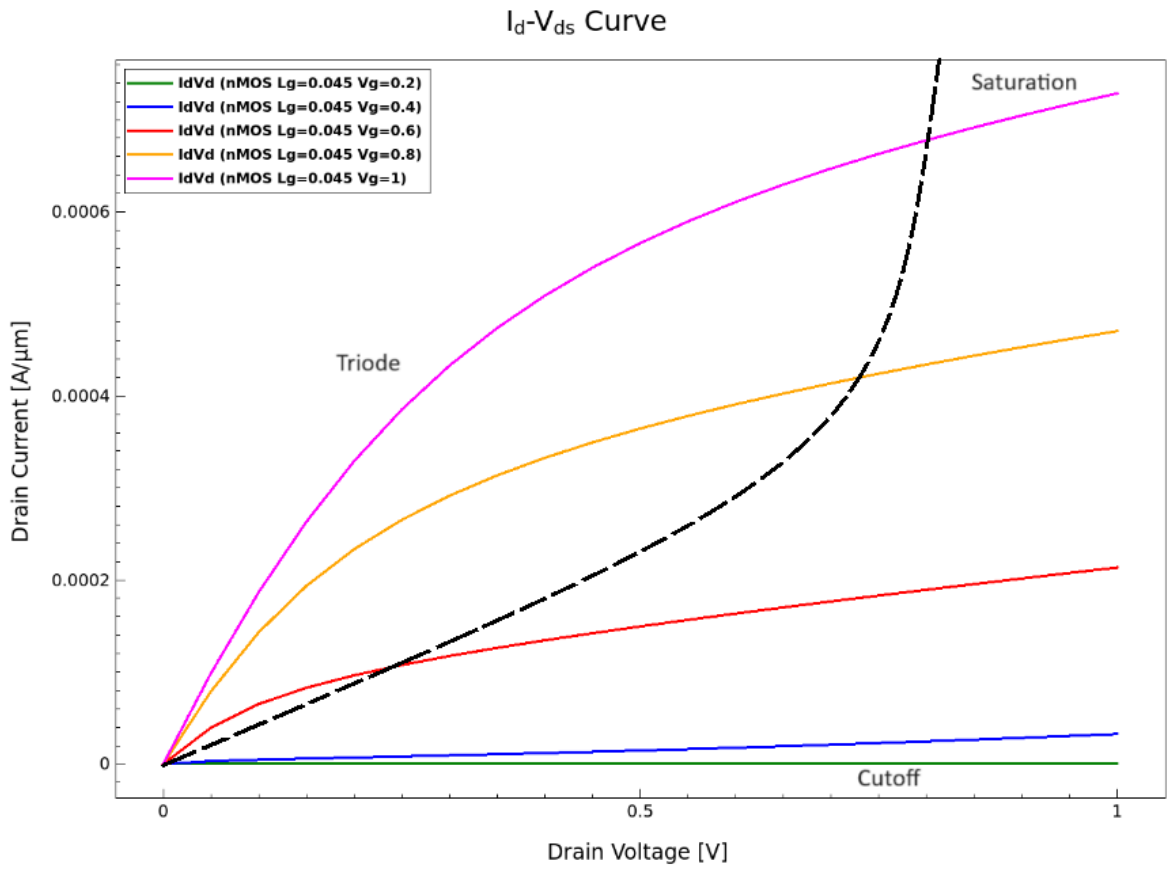

Figure 12: I_{ds} vs. V_{ds} curves for V_{gs} = 0.2, 0.4, 0.6, 0.8 and 1.0 V for $0 \leq V_{ds} \leq V_{dd}$.

The ideal square law dependence for a MOSFET refers to the relationship between the drain current and the gate-to-source voltage in the saturation region. For an ideal MOSFET, where I_{ds} has no dependency on V_{ds}, we would expect the curves to be horizontal in the saturation region (see Appendix A). From *Figure 12,* we observe that the curves are not horizontal as expected, indicating I_{ds} is dependent on V_{ds} even in the saturation region. This deviation could be attributed to the short channel effects of the channel length modulation, which causes the drain current I_{ds} to increase with drain bias V_{ds} in the saturation region [11].

C. Bonus

We started with our previous design parameters from Table 1 but with Vdd=1.2V, instead of 1V.

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.440	0.382	1.078e-04	88.564	2.478e-04	1.018e-03	4.590e-09	0.245	87.442	1.364e-03	4205.359

Figure 13: Screenshot of the Sentaurus Workbench with previous design parameters. Although I_{on} = 1018 µA/µm ≥ 445 µA/µm, the design specifications are not met as I_{off} = 4.59 nA/µm </ 0.01 nA/µm for V_{dd} =1.2V.

As both I_{on} and I_{off} are higher than the specification, we first increase the halo doping iteratively to 6.3 x 10^{18} cm^{-3}. Further increasing the halo doping causes an inverse effect, we therefore keep halo at this value and decrease extension doping iteratively to 3.36 x 10^{19} cm^{-3}. At 3.36 x 10^{19} cm^{-3}, neither I_{on} and I_{off} met the design specifications, although were close, therefore by keeping extension doping at this value, we increased the substrate doping to 9.3 x 10^{17} cm^{-3}. A list of aforementioned iterations and their results, as well as the final design parameters are presented in Appendix B. Achieved design specifications are presented in *Figure 14* below.

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.689	0.651	6.384e-05	91.462	1.756e-04	4.453e-04	9.937e-12	0.569	602.085	9.424e-04	15027.529

Figure 14: Screenshot of the Sentaurus Workbench, showing the achieved device specifications (I_{on} = 445.3 µA/µm ≥ 445 µA/µm and I_{off} = 0.009937 nA/µm ≤ 0.01 nA/µm for V_{dd} =1.2V)

Conclusions

We designed a 45 nm NMOS transistor with a systematic approach observing the effects of reducing or increasing each parameter one at a time. We adjusted physical parameters to meet the desired I_on and I_off criteria and plotted the drain current against the gate-source voltage to observe current trends. Changes in the substrate doping, extension doping and the halo doping concentrations ensured that the final designs met their requirements. We also discussed key terms such as threshold voltages and DIBL along with the readings from TSMC's paper.

References

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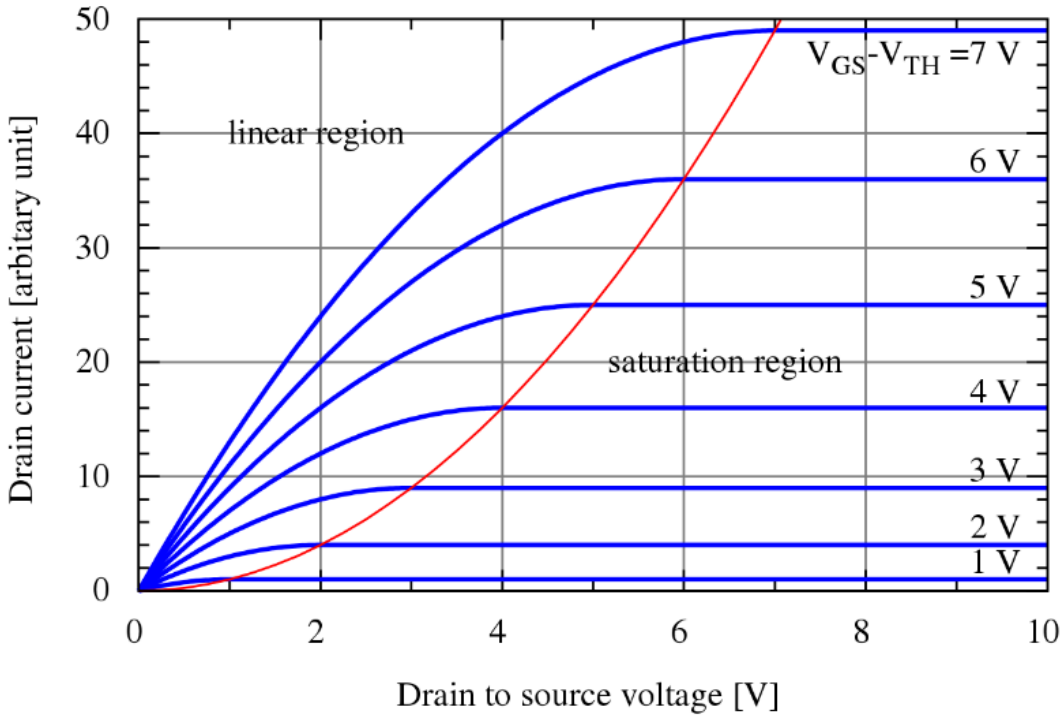
Appendix A



Appendix A - Figure 1: Example I_{ds} vs. V_{ds} curves for an ideal MOSFET, where the curves become horizontal in the saturation region. [12]

Appendix B

Iterations of Changed Parameters & Resulting I_{off} and I_{on} Values for the Bonus Part

Appendix B - Table A: Iterations of doping parameters and resulting Ioff and Ion values. The parameters that were changed for that iteration are bolded. All other parameters were kept the same as the initial design presented in Table 1 of this report.

Halo Doping [cm^{-3}]	**Extension Doping [cm^{-3}]**	**Substrate Doping [cm^{-3}]**	**I_{off} [A]**	**I_{on} [A]**
3.3×10^{18}	6×10^{19}	9×10^{17}	4.59×10^{-9}	1.018×10^{-3}
6×10^{18}	6×10^{19}	9×10^{17}	7.039×10^{-11}	5.689×10^{-4}
6.3×10^{18}	6×10^{19}	9×10^{17}	9.50×10^{-11}	5.285×10^{-4}
6.3×10^{18}	**5×10^{19}**	9×10^{17}	4.226×10^{-11}	5.305×10^{-4}
6.3×10^{18}	**3×10^{19}**	9×10^{17}	0.588×10^{-11}	4.185×10^{-4}
6.3×10^{18}	**3.5×10^{19}**	9×10^{17}	1.184×10^{-11}	4.530×10^{-4}
6.3×10^{18}	**3.3×10^{19}**	9×10^{17}	0.9114×10^{-11}	4.399×10^{-4}
6.3×10^{18}	**3.4×10^{19}**	9×10^{17}	1.050×10^{-11}	4.466×10^{-4}
6.3×10^{18}	**3.35×10^{19}**	9×10^{17}	0.9792×10^{-11}	4.432×10^{-4}
6.3×10^{18}	**3.38×10^{19}**	9×10^{17}	1.036×10^{-11}	4.459×10^{-4}
6.3×10^{18}	**3.37×10^{19}**	9×10^{17}	1.007×10^{-11}	4.446×10^{-4}
6.3×10^{18}	**3.36×10^{19}**	**9.3×10^{17}**	0.9937×10^{-11}	4.453×10^{-4}

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.689	0.649	6.482e-05	91.467	1.777e-04	4.530e-04	1.184e-11	0.566	653.761	9.559e-04	14569.835

Appendix B - Figure 1: Screenshot of the Sentaurus Workbench, with halo doping set to 6.3 x 10^{18} cm^{-3} *and extension doping set to* 3.5 x 10^{19} cm^{-3}. *(6th iteration)*

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.689	0.649	6.482e-05	91.467	1.777e-04	4.530e-04	1.184e-11	0.566	653.761	9.559e-04	14569.835

Appendix B - Figure 2: Screenshot of the Sentaurus Workbench, with halo doping set to 6.3 x 10^{18} cm^{-3} *and extension doping set to* 3.3 x 10^{19} cm^{-3}. *(7th iteration)*

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.689	0.650	6.399e-05	91.452	1.760e-04	4.466e-04	1.050e-11	0.568	635.581	9.443e-04	14979.134

Appendix B - Figure 3: Screenshot of the Sentaurus Workbench, with halo doping set to 6.3 x 10^{18} cm^{-3} *and extension doping set to* 3.4 x 10^{19} cm^{-3}. *(8th iteration)*

Vtgm	VtiLin	IdLin	SSlin	gmLin	IdSat	Ioff	VtiSat	SSsat	gmSat	Ron
0.689	0.650	6.357e-05	91.445	1.752e-04	4.432e-04	9.792e-12	0.569	588.256	9.384e-04	15195.825

Appendix B - Figure 4: Screenshot of the Sentaurus Workbench, with halo doping set to 6.3 x 10^{18} cm^{-3} *and extension doping set to* 3.35 x 10^{19} cm^{-3}. *(9th iteration)*

Appendix B - Changed Final Design Parameters for Bonus Question (sdevice_des.cmd)

```
;   - Substrate doping level
  (define SubDop  9.3e17 )   ; [1/cm3]
  (define HaloDop 6e18 ) ; [1/cm3]
  (define ExtDop 3.36e19) ; [1/cm3]
 )
```