INTEGRATED CIRCUITS

DATA SHEET

PCF8814

65 × 96 pixels matrix LCD driver

Objective specification

2003 Mar 13

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Single-chip LCD controller or driver
- 65 row, 96 column outputs
- Display data RAM 65 × 96 bits
- Selectable 3-line or 4-line serial interfaces, 6.5 MHz and High-speed I^2C-bus
- On-chip:
  - Configurable voltage multiplier generating $V_{LCD;}$ external V_{LCD} also possible
  - Four segment V_{LCD} temperature compensation
  - Generation of intermediate LCD bias voltage
  - Oscillator requires no external components; external clock input also possible
- Temperature read-back via interface
- External reset input pin
- CMOS compatible inputs
- Programmable MUX rate: 1 : 8 to 1 : 65
- Logic supply voltage: 1.7 to 3.3 V
- High voltage generator supply voltage: 2.4 to 4.5 V
- Display supply voltage: 3 to 9 V
- Low power consumption, suitable for battery operated systems
- Programmable row pad mirroring, for compatibility with both Tape Carrier Packages (TCP) and Chip-On-Glass (COG) applications
- Status read which allows for chip recognition
- Start address line, which allows for instance, the scrolling of the displayed image
- Slim chip layout, suited to COG and TCP applications
- Operating temperature: –40 to +85 °C.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF8814[(1)] is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 96 columns. All necessary functions for the display are provided in a single-chip, including on-chip generation of PCF8814 LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The can be interfaced to microcontrollers via a serial bus.

(1) Type PCF8814MU/2DB/2 is sold under a Motif® license agreement. Motif® is a registered trademark of The Open Group in the US and other countries. Type PCF8814U/2DB/2 is not covered by a Philips/Motif License agreement. For further information on Motif licensed and unlicensed LCD drivers from Philips, please contact your local Philips office.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8814U/2DB/2	–	chip with bumps in tray	–
PCF8814MU/2DB/2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

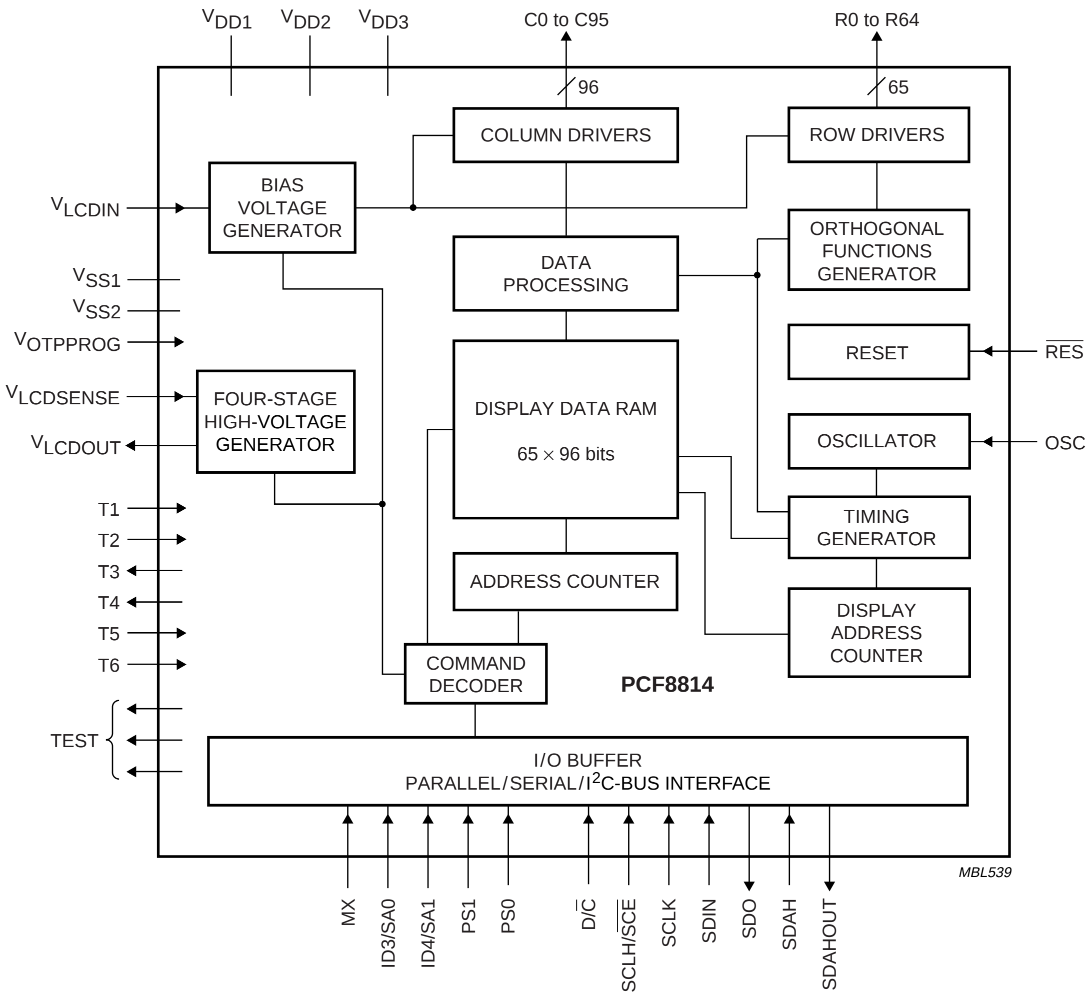


Fig.1 Block diagram.

6 PINNING INFORMATION

SYMBOL	PAD	DESCRIPTION
V_{LCDIN}	5 to 8	LCD supply voltage input; see note 1.
V_{LCDOUT}	9 to 15	Voltage multiplier output; see note 1.
$V_{LCDSENSE}$	16	Voltage multiplier regulation input; see note 1.
T3, T4, v1l_pad, v1h_pad, vc_pad	22, 23, 182 and 148	Test outputs. T3, T4, v1l_pad, v1h_pad and vc_pad must be left open-circuit (these connections are not accessible to the user).
T1, T2, T5 and T6	24, 25, 26 and 27	Test inputs. T1, T2, T5 and T6 must be connected to V_{SS}.
V_{DD1}	41 to 46	Supply voltages 1, 2 and 3 respectively. V_{DD1} is used as the supply voltage for the chip excluding the internal voltage generator. V_{DD2} and V_{DD3} are the supply voltages for the internal voltage generator. Both have the same voltage and should be connected together outside of the chip. V_{DD2} and V_{DD3} must not be applied before V_{DD1}. V_{DD1} can be connected together with V_{DD2} and V_{DD3} but care must be taken to respect the supply voltage range.
V_{DD2}	31 to 40	
V_{DD3}	28 to 30	
SCLK	47	Serial data clock input.
ID3/SA0	48	Module identification inputs. These two inputs may be read back via the Read back instruction. When the I^2C-bus interface is being used, these pins make up the two LSBs of the slave address.
ID4/SA1	49	
OSC	50	Oscillator input for an external clock signal. When the on-chip oscillator is used this input must be connected to V_{DD1}. If the oscillator and external clock are both inhibited by connecting the OSC pad to V_{SS1}, the display is not clocked and may be left in a DC state. To avoid this, the chip should always be put into Power-down mode before stopping the clock.
SDO	51	Serial data output, push-pull type.
SDAHOUT	66	I^2C-bus data output. SDAHOUT is the serial data acknowledge output for the I^2C-bus interface. By connecting SDAHOUT to SDAH externally, the SDAH line becomes fully I^2C-bus compatible. See note 2.
SDAH	67	I^2C-bus serial data input. When not used must be connected to V_{DD1} or V_{SS1}.
SDIN	82	Serial data input.
V_{SS1}	90 to 95	Ground supply voltages 1 and 2 respectively; these ground supply rails must be connected together.
V_{SS2}	83 to 89	
$V_{OTPPROG}$	96 to 98	Supply voltage for the OTP programming. The $V_{OTPPROG}$ pad can be combined with the SCLH/$\overline{\text{SCE}}$ pad in order to reduce the external connections.
SCLH/$\overline{\text{SCE}}$	113	I^2C-bus clock input/$\overline{\text{chip enable}}$: serial clock input when the I^2C-bus interface is selected or the chip enable for non-I^2C-bus interfaces.
D/$\overline{\text{C}}$	114	Data/$\overline{\text{command}}$: this input selects either command/address or data input. Not used in the 3-line serial interface and should be connected to V_{DD1} or V_{SS1} in this situation.
PS1	115	These two logic inputs are used for interface selection.
PS0	117	
MX	118	Horizontal mirroring input.
$\overline{\text{RES}}$	121	External reset input, active LOW. This signal will reset the device and must be applied to initialize the chip.

SYMBOL	PAD	DESCRIPTION
C0 to C95	279 to 232, 230 to 184	LCD column driver outputs
R0 to R64	314 to 283, 149 to 181	LCD row driver outputs
dummy	1 to 4,18 to 21, 52 to 65, 68 to 81, 99 to 112, 119, 120, 123 to 147, 231, 280, 281, 315 to 318	dummy pads

Notes

1. V_{LCDIN} is the positive power supply for the liquid crystal display. If the internal V_{LCD} generator is used, then all three supply lines must be connected together. When the V_{LCD} generator is disabled and an external voltage is to be supplied to V_{LCDIN}, then V_{LCDOUT} must be left open-circuit, $V_{LCDSENSE}$ must be connected to V_{LCDIN}, and V_{DD2} and V_{DD3} should be applied according to the specified voltage range. If the PCF8814 is in power-down mode, the external LCD supply voltage may be switched off.
2. Having the acknowledge output separated from the serial data line is advantageous; in COG applications where the track resistance from the SDAHOUT pad to the system SDAH line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible that during the acknowledge cycle the PCF8814 will not be able to create a valid logic 0 level. By splitting the SDAH input from the SDAHOUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAHOUT pad to the system SDAH line to guarantee a valid LOW level. When not used it must be connected to V_{DD1} or V_{SS1}.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

An on-chip oscillator provides the clock signal for the display system; no external components are required. When the on-chip oscillator is used, the OSC input must be connected to V_{DD1}. An external clock signal, if used, is connected to the OSC input.

7.2 Address counter

The Address Counter (AC) assigns addresses to the display data RAM for writing. The X-address X[6:0] and the Y-address Y[3:0] are set separately.

7.3 Display data RAM

The PCF8814 contains a 65 × 96-bit static RAM which stores the display data. The Display Data RAM (DDRAM) is divided into 9 banks of 96 bytes, although, only one bit of the 9th bank is used. During RAM access, data is transferred to the RAM via the serial interface. There is a direct correspondence between X-address and column output number.

7.4 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

7.5 Display address counter

The display is generated by simultaneously reading out the RAM content for 2 or 4 rows depending on the current display size which is selected. This content will be processed with the corresponding set of 2 or 4 orthogonal functions thus generating the signals for switching the pixels of the display on or off according to the RAM content.

The display status (all dots on/off and normal/inverse video) is set by the bits DON, DAL and E in the command “Display control”; see Table 11.

7.6 LCD row and column drivers

The PCF8814 contains 65 row and 96 column drivers which connect the appropriate LCD bias voltages in sequence to the display, in accordance with the data to be displayed. The number of simultaneously selected rows is represented by the value ‘p’. In the PCF8814, ‘p’ is set to 4 or 2 automatically, depending on the partial display mode selected.

8 ADDRESSING

Data is downloaded in bytes into the DDRAM matrix of the PCF8814 as indicated in Figs 2 and 3. The display RAM has a matrix of 65 × 96 bits. The columns are addressed by the address pointer. The decimal address ranges are: X = 0 to 95 and Y = 0 to 8. The Y address represents the bank number. Addresses outside these ranges are not allowed.

8.1 Display data RAM structure

The mode for storing data into the data RAM is dependent on:

- Horizontal/vertical addressing mode, V
- Data order, DOR
- Mirror the Y-axis, MY.

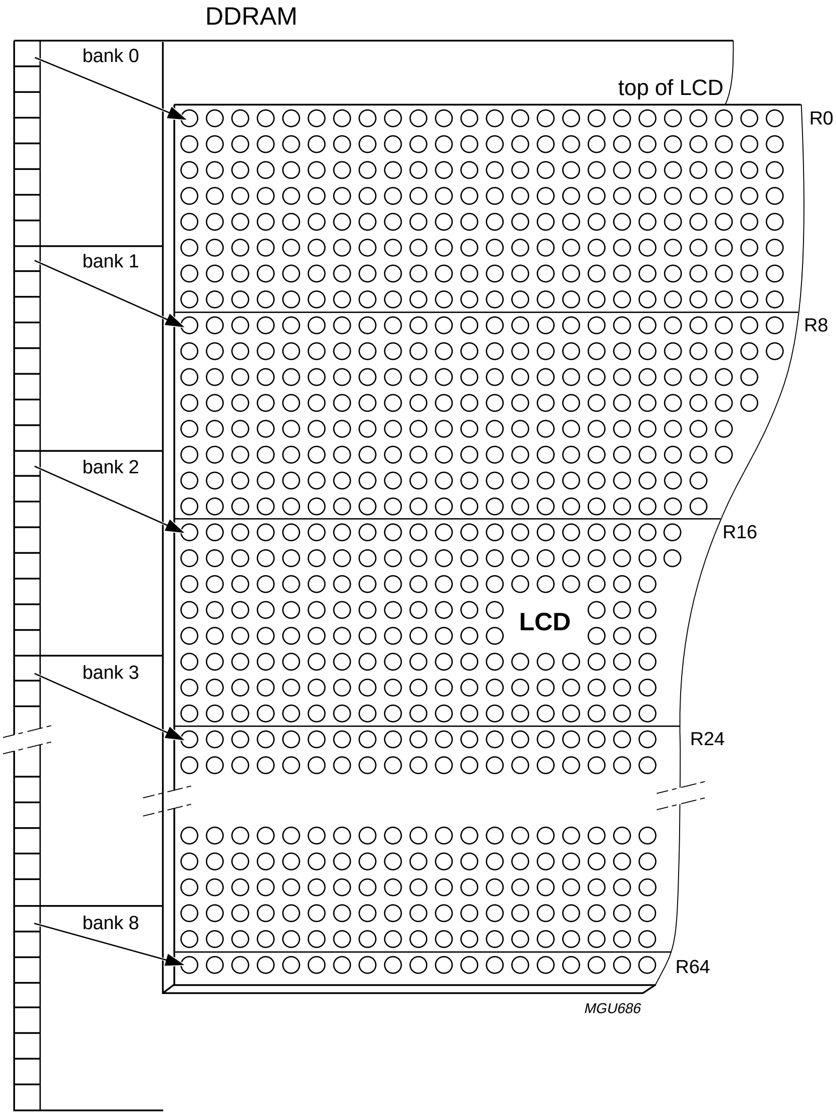


Fig.2 DDRAM to display mapping (MY = 0).

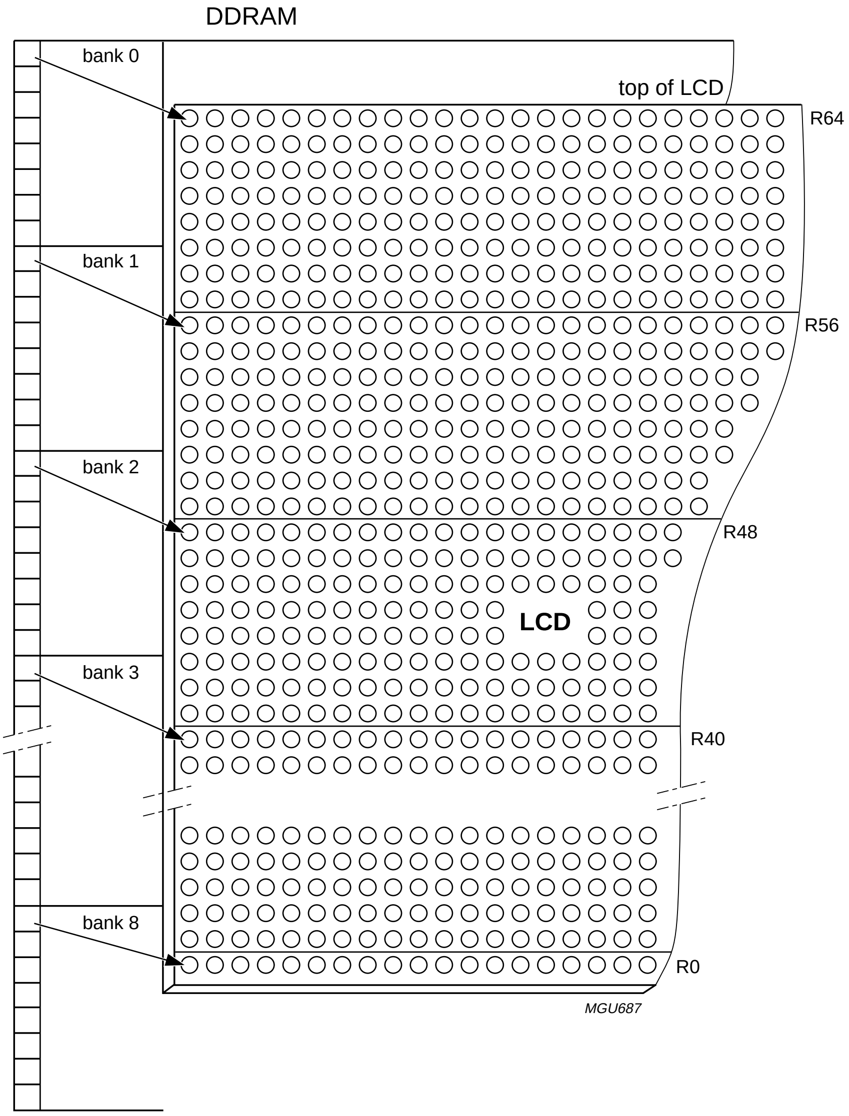


Fig.3 DDRAM to display mapping (MY = 1).

8.1.1 HORIZONTAL/VERTICAL ADDRESSING

Two different addressing modes are possible: horizontal addressing mode and vertical addressing mode.

In the horizontal addressing mode (V = 0), the X address increments after each byte. After the last X address, X wraps around to 0 and Y increments to address the next row (see Fig.4).

In the vertical addressing mode (V = 1), the Y address increments after each byte. After the last Y address (Y = 8), Y wraps around to 0 and X increments to address the next column (see Fig.5).

After the very last address the address pointers wrap around to address X = 0 and Y = 0 in both horizontal and vertical addressing modes.

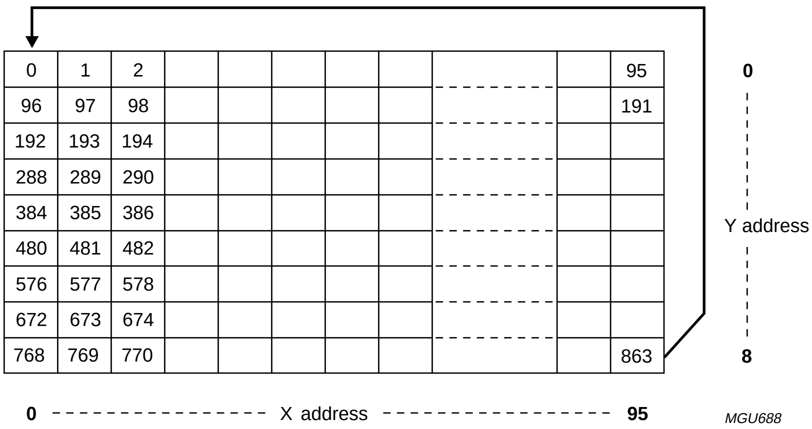


Fig.4 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

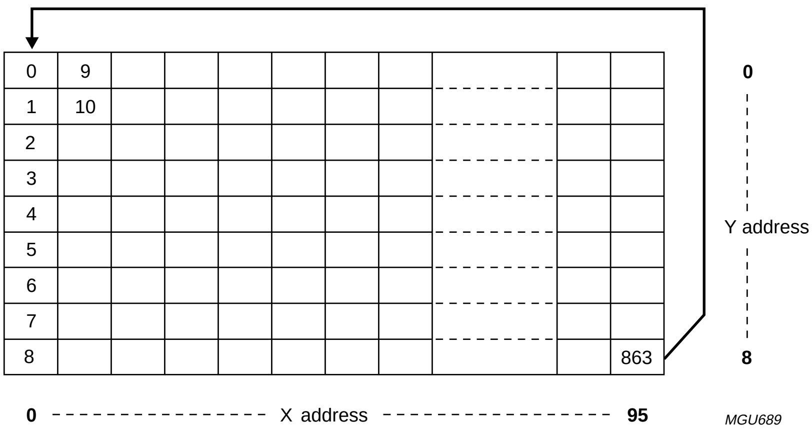


Fig.5 Sequence of writing data bytes into the RAM with vertical addressing (V = 1).

8.1.2 DATA ORDER

The Data Order bit (DOR) defines the bit order (LSB on top or MSB on top) for writing into the RAM (see Figs 6 and 7).

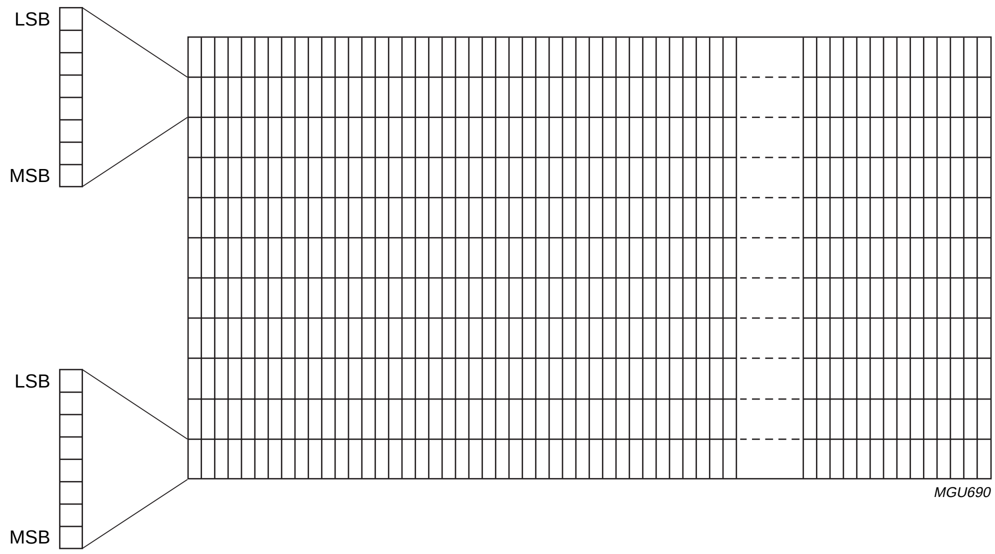


Fig.6 RAM byte organisation (DOR = 0).

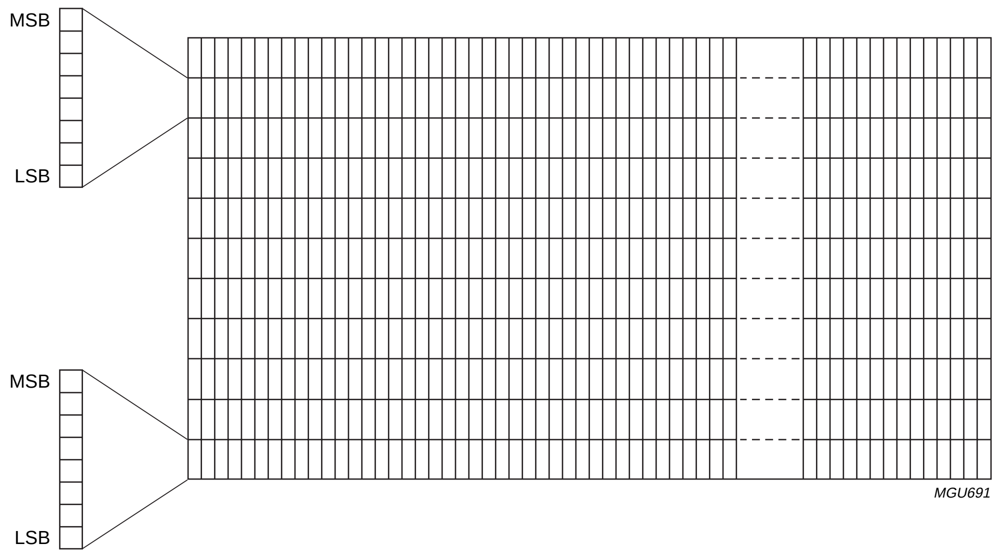


Fig.7 RAM byte organisation (DOR = 1).

8.1.3 MIRROR Y

The MY bit allows vertical mirroring. When MY = 1, the Y address space is mirrored. The address Y = 0 is then located at the bottom of the display (see Fig.8). When MY = 0, the mirroring is disabled and the address Y = 0 is located at the top of the display (see Fig.9).

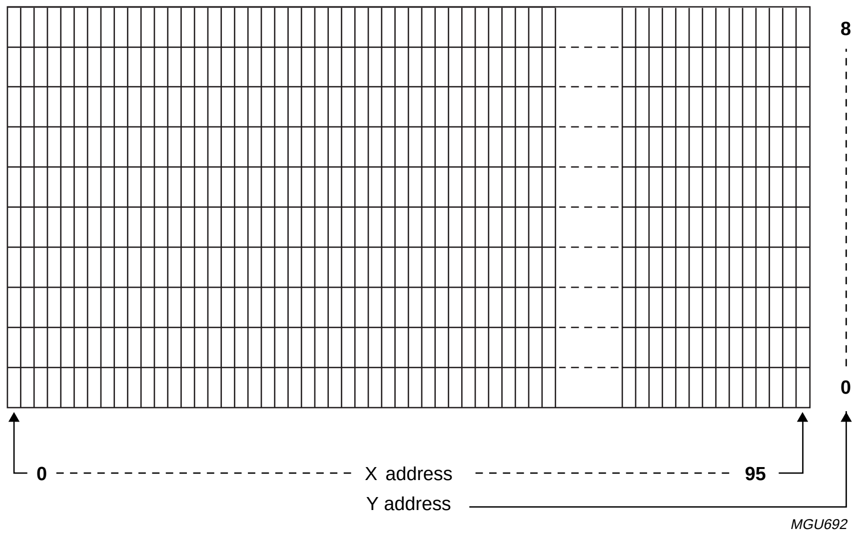


Fig.8 RAM format addressing (MY = 1).

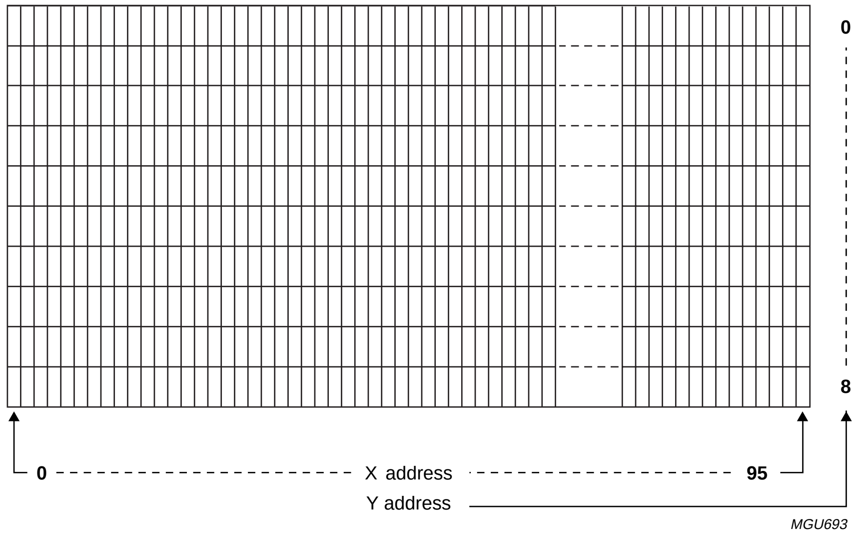


Fig.9 RAM format addressing (MY = 0).

8.1.4 MIRROR X

The MX bit allows horizontal mirroring. When MX = 1, the X address space is mirrored. The address X = 0 is then located at the right side (X-max) of the display (see Fig.10). When MX = 0, the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.11).

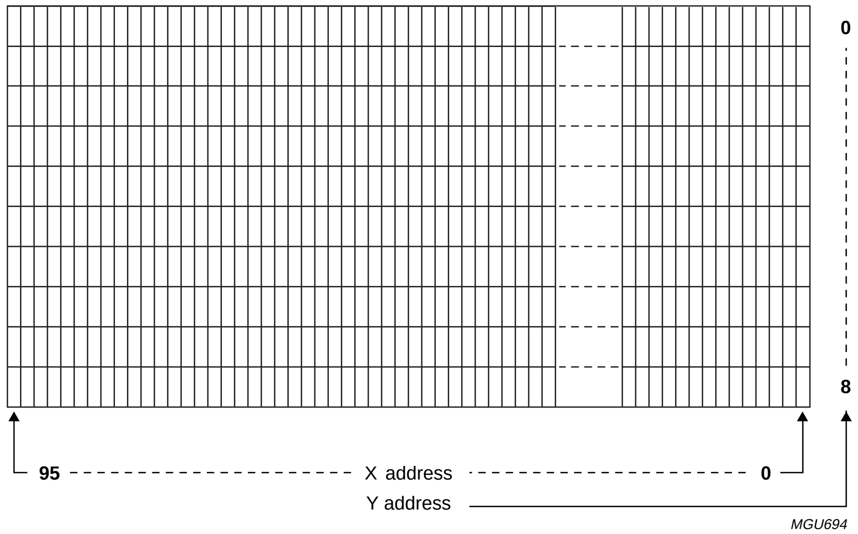


Fig.10 RAM format addressing (MX = 1).

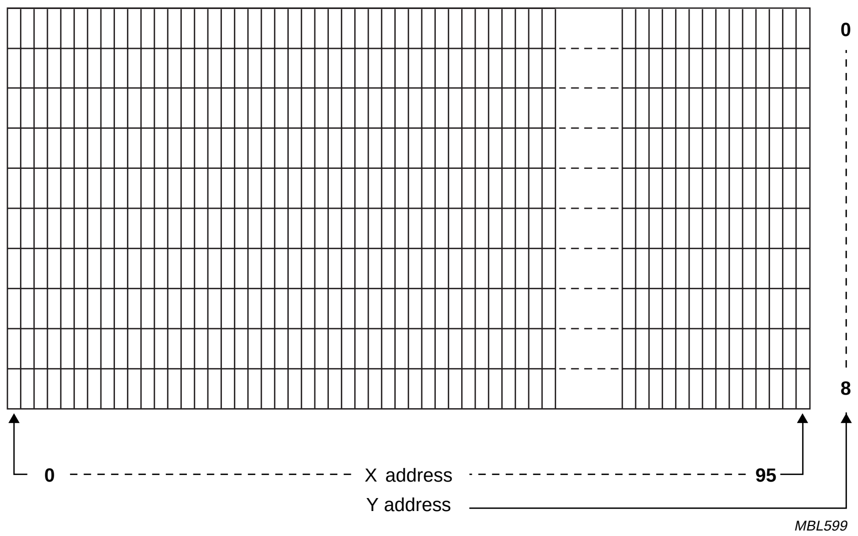


Fig.11 RAM format addressing (MX = 0).

9 SERIAL INTERFACES

Communication with the microcontroller is achieved via a clock-synchronized serial peripheral interface.

One of four different serial interfaces may be selected using the inputs PS1 and PS0; see Table 1.

Table 1 Interface selection

PS1	PS0	INTERFACE
0	0	3-line SPI
0	1	4-line SPI
1	0	I^2C-bus
1	1	3-line serial interface

9.1 Serial peripheral interface

The Serial Peripheral Interface (SPI) is a 3-line or 4-line interface for communication between the microcontroller and the LCD driver chip.

The three lines are: $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDIN (serial data). When the 3-line SPI interface is used the display data/command is controlled by software.

For the 4-line serial interface the D/$\overline{C}$ line is added. The PCF8814 is connected to the serial data I/O of the microcontroller by two pins: SDIN (data input) and SDO (data output) connected together.

The timing diagrams for the 3-line and 4-line SPI are shown in Chapter 15.

9.1.1 WRITE MODE

The display data/command indication may be controlled either via software or using the D/$\overline{C}$ select input. When the D/$\overline{C}$ input is used, display data is transmitted when D/$\overline{C}$ is HIGH, and command data is transmitted when D/$\overline{C}$ is LOW (see Figs 12 and 13). When D/$\overline{C}$ is not used, the Display data length instruction is used to indicate that a specific number of display data bytes (1 to 255) are to be transmitted (see Fig.14). The next byte after the display data string is handled as an instruction command.

If $\overline{SCE}$ is pulled HIGH during a serial display data stream, the interrupted byte is invalid data but all previously transmitted data is valid. The next byte received will be handled as an instruction command. (see Fig.15).

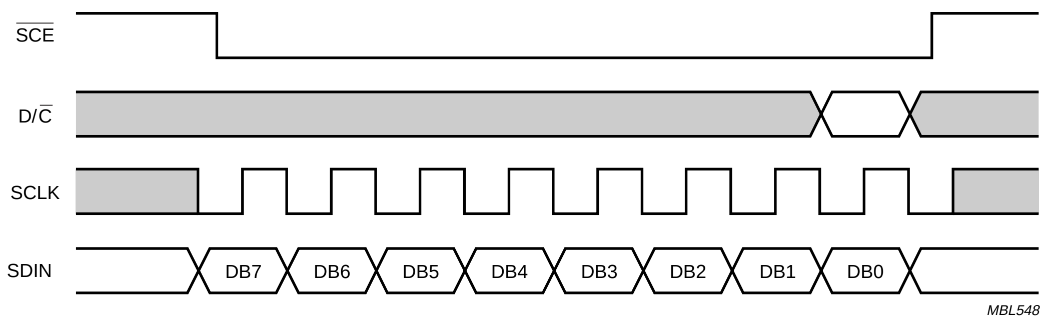


Fig.12 Serial bus protocol: transmission of one byte.

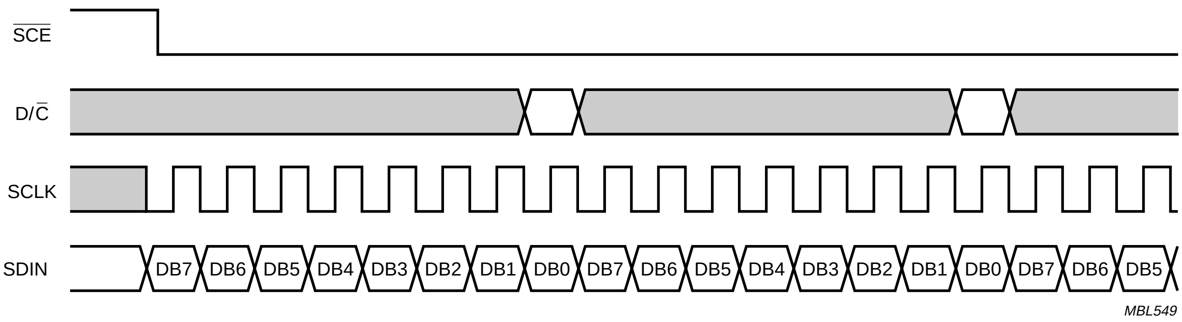


Fig.13 Serial bus protocol: transmission of several bytes.

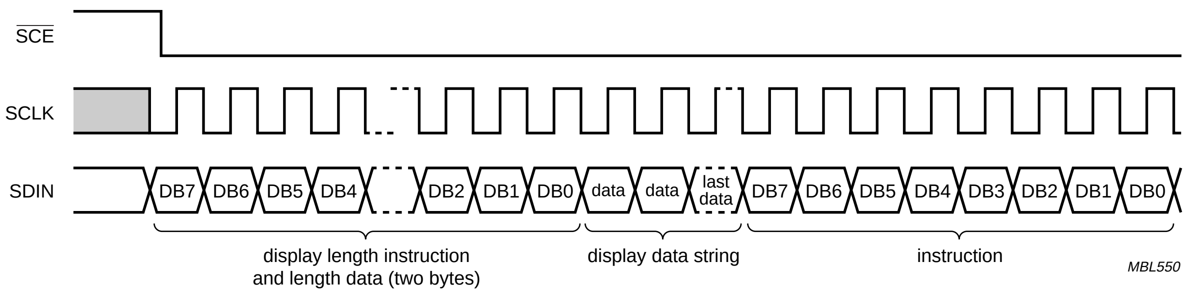


Fig.14 Transmission of several bytes.

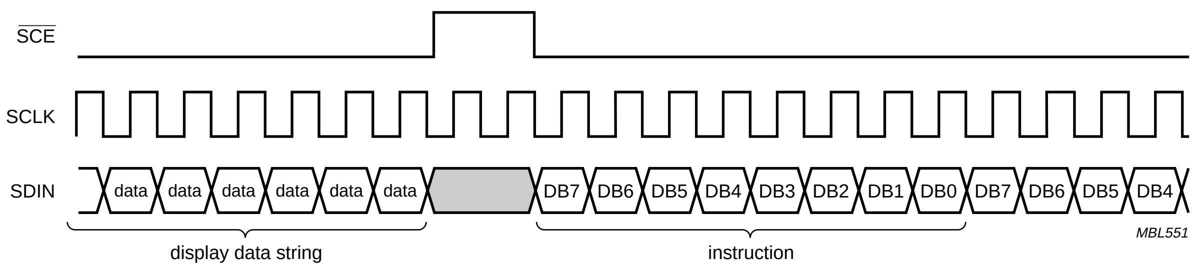


Fig.15 Transmission interrupted by $\overline{SCE}$.

9.1.2 READ MODE

In the read mode of the interface the microcontroller reads data from the PCF8814. To do so the microcontroller first has to send the read status command, then the PCF8814 will respond by transmitting data on the SDO line. After that $\overline{SCE}$ is required to go HIGH, (see Fig.16).

The PCF8814 samples the SDIN data at rising SCLK edges, but shifts SDO data at falling SCLK edges. Thus the microcontroller reads the SDO data at rising SCLK edges.

After the read status command has been sent, the SDIN line must be set to 3-state not later then at the falling SCLK edge of the last bit (see Fig.16).

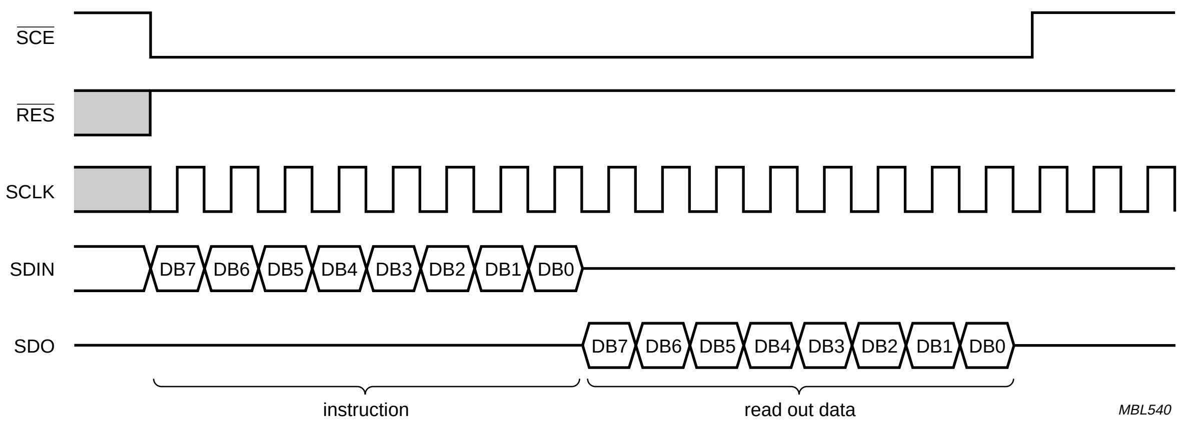


Fig.16 Read mode, SPI 3-line and 4-line.

9.2 3-line serial interface

The serial interface is also a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The three lines are $\overline{\text{SCE}}$ (chip enable), SCLK (serial clock) and SDIN (serial data). The PCF8814 is connected to the SDA line of the microcontroller by two pads, SDIN (data input) and SDO (data output), which are connected together.

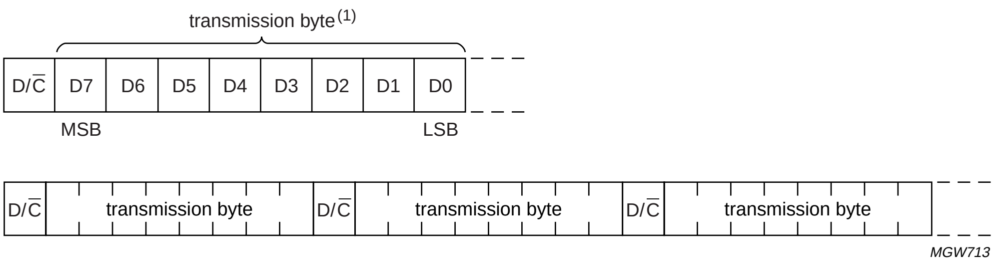
9.2.1 WRITE MODE

In the write mode of the interface the microcontroller writes commands and data to the PCF8814. Each data packet contains a control bit D/$\overline{\text{C}}$ and a transmission byte. If D/$\overline{\text{C}}$ is LOW, the following byte is interpreted as a command byte. The instruction set is given in Table 8. If D/$\overline{\text{C}}$ is HIGH, the following byte is stored in the display data RAM. After every data byte the address counter is incremented automatically. Figure 17 shows the general format of the write mode and the definition of the transmission byte.

Any instruction can be sent in any order to the PCF8814. The MSB is transmitted first. The serial interface is initialized when $\overline{\text{SCE}}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on $\overline{\text{SCE}}$ enables the serial interface and indicates the start of data transmission.

Figures 18, 19 and 20 show the protocol of the write mode:

- When $\overline{\text{SCE}}$ is HIGH, SCLK clocks are ignored. During the HIGH time of $\overline{\text{SCE}}$ the serial interface is initialized
- At the falling $\overline{\text{SCE}}$ edge SCLK must be LOW (see Fig.42)
- SDIN is sampled at the rising edge of SCLK
- D/$\overline{\text{C}}$ indicates whether the byte is a command (D/$\overline{\text{C}}$ = 0) or RAM data (D/$\overline{\text{C}}$ = 1). It is sampled with the first rising SCLK edge
- If $\overline{\text{SCE}}$ stays LOW after the last bit of a command/data byte, the serial interface expects the D/$\overline{\text{C}}$ bit of the next byte at the next rising edge of SCLK (see Fig.19)
- A reset pulse with $\overline{\text{RES}}$ interrupts the transmission. The data being written into the RAM may be corrupted. The registers are cleared. If $\overline{\text{SCE}}$ is LOW after the rising edge of $\overline{\text{RES}}$, the serial interface is ready to receive the D/$\overline{\text{C}}$ bit of a command/data byte (see Fig.20).



(1) A transmission byte may be a command or a data byte.

Fig.17 Serial data stream, write mode.

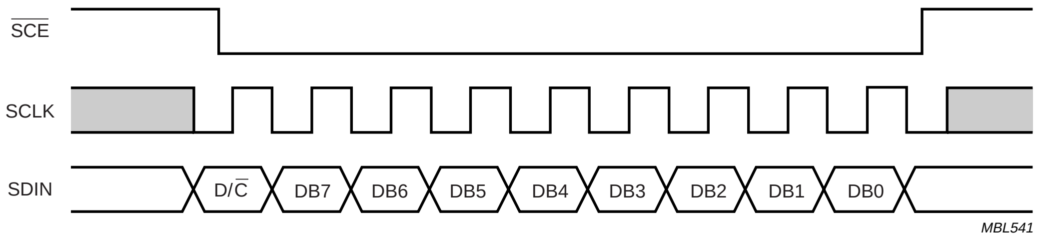


Fig.18 Write mode - a control bit followed by a transmission byte.

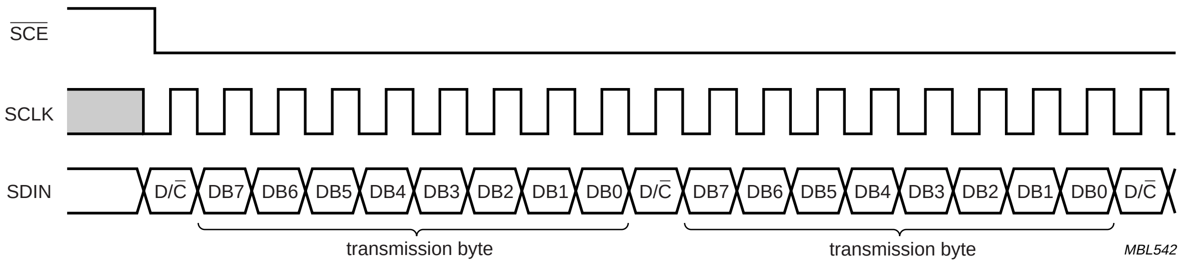


Fig.19 Write mode - transmission of several bytes.

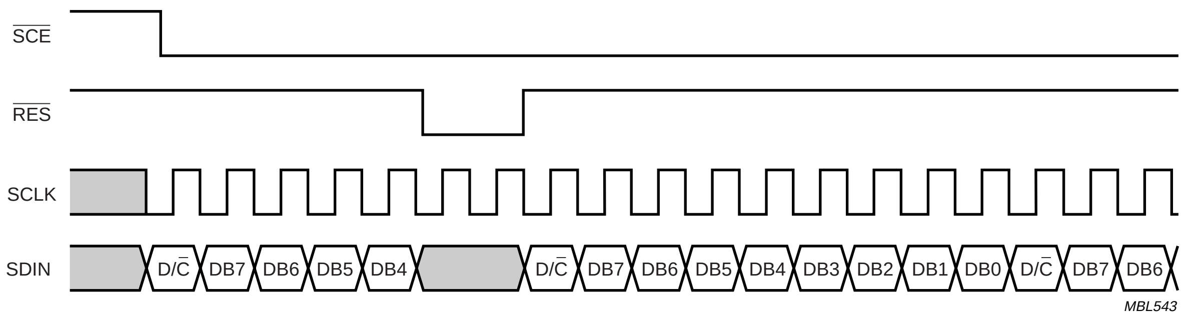


Fig.20 Write mode - interrupted by reset ($\overline{RES}$).

9.2.2 READ MODE

In the read mode of the interface the microcontroller reads data from the PCF8814. To do so, the microcontroller first has to send a command, the read status command, and then the following byte is transmitted in the opposite direction by using SDO (see Fig.21). After that, $\overline{\text{SCE}}$ is required to go HIGH before a new command is sent.

The PCF8814 samples the SDIN data at rising SCLK edges, but shifts SDO data at falling SCLK edges. Thus the microcontroller reads SDO data at rising SCLK edges.

After the read status command has been sent, the SDIN line must be set to 3-state not later then at the falling SCLK edge of the last bit (see Fig.21).

The 8th read bit is shorter than the others because it is terminated by the rising edge of SCLK (see Fig.45). The last rising SCLK edge sets SDO to 3-state after the delay time t_4.

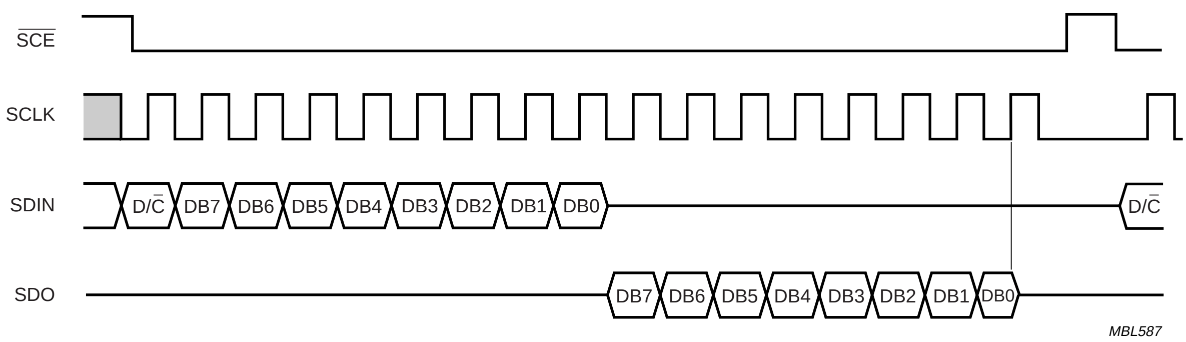


Fig.21 Read mode 3-line serial interface.

9.2.3 READ DATA FORMAT

Regardless of which serial interface is used there are five bits, ID1 to ID4 and VM, that can be read and also one temperature register. For the bits, one bit is transmitted per byte read and is selected by issuing the appropriate Read instruction from the instruction set. The format for the read bit, B, is shown in Table 2.

Sending the instruction to read back the temperature sensor will select the status byte shown in Table 3.

Table 2 Read data format

D7	D6	D5	D4	D3	D2	D1	D0
X	B	B	B	$\overline{B}$	$\overline{B}$	$\overline{B}$	$\overline{B}$

Note

1. X = undefined.

Table 3 Temperature sensor

D7	D6	D5	D4	D3	D2	D1	D0
X	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Note

1. X = undefined.

10 I²C-BUS INTERFACE (HS-MODE)

10.1 Characteristics of the I²C-bus (Hs-mode)

The I²C-bus Hs-mode is for bidirectional, 2-line communication between different ICs or modules with speeds up to 3.4 MHz. The only difference between Hs-mode slave devices and Fast-mode slave devices is the speed at which they operate therefore the buffers on the SLCH and SDAH outputs(1) have an open-drain configuration. This is the same for I²C-bus master devices which have an open-drain SDAH output and a combination of an open-drain pull-down and current source pull-up circuits on the SCLH output. Only the current source of one master is enabled at any one time, and only during Hs-mode. Both lines must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

(1) In Hs-mode, SCL and SDA lines operating at the higher frequency are referred to as SCLH and SDAH.

10.1.1 SYSTEM CONFIGURATION

The system configuration shown in Fig.22 comprises:

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronisation: procedure to synchronize the clock signals of two or more devices.

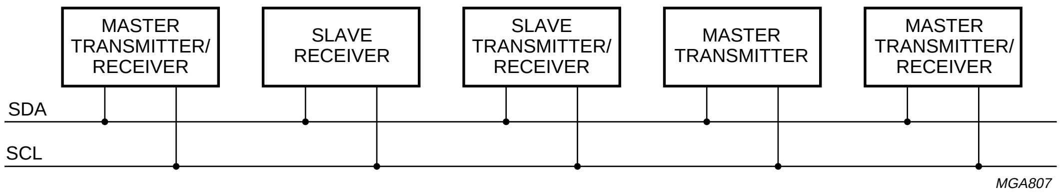


Fig.22 System configuration.

10.1.2 BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDAH line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. See Fig.23.

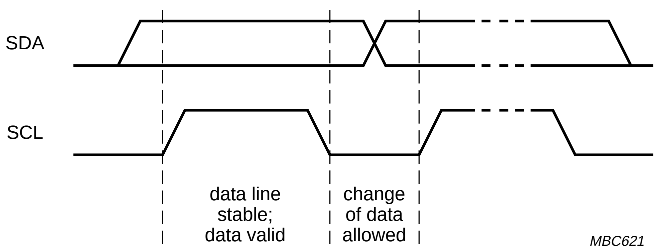


Fig.23 Bit transfer.

10.1.3 START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). See Fig.24.

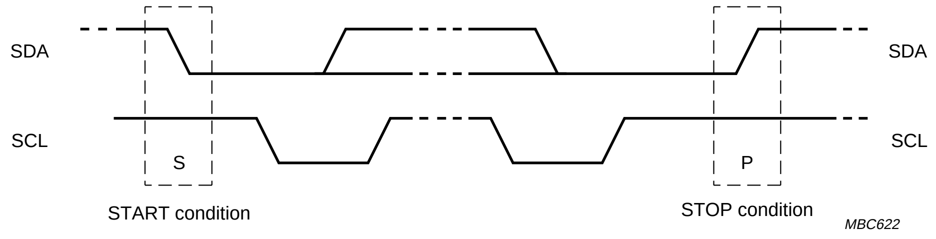


Fig.24 Definition of START and STOP conditions.

10.1.4 ACKNOWLEDGE

Each byte of 8 bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

The acknowledge timing is shown in Fig.25.

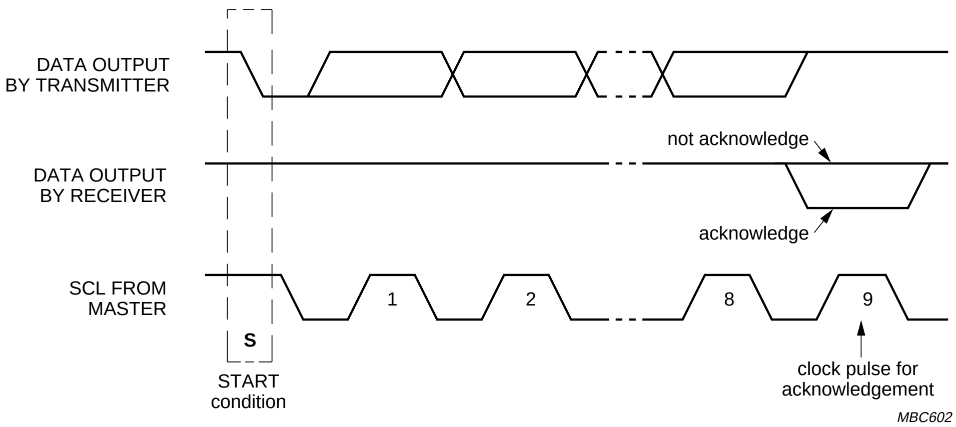


Fig.25 Acknowledge on the I^{2}C-bus.

10.2 I²C-bus Hs-mode protocol

The PCF8814 is a slave receiver/transmitter. If data is to be read from the device the SDAHOUT pad must be connected, otherwise SDAHOUT need not be used.

Hs-mode can only commence after the following conditions:

- START condition (S)
- 8-bit master code (0000 1XXX)
- not-acknowledge bit ($\overline{A}$).

The master code has two functions as shown in Figs 26 and 27. It allows arbitration and synchronization between competing masters at Fast-mode speeds, resulting in one winner.The master code also indicates the beginning of an Hs-mode transfer.

As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge ($\overline{A}$). After this $\overline{A}$ bit, and the SCLH line has been pulled up to a HIGH level, the active master switches to Hs-mode and enables at t_H the current-source pull-up circuit for the SCLH signal (see Fig.27).

The active master will then send a repeated START condition (Sr) followed by a 7-bit slave address with a $R/\overline{W}$ bit, and receives an acknowledge bit (A) from the selected slave. After each acknowledge bit (A) or not-acknowledge bit ($\overline{A}$) the active master disables its current-source pull-up circuit. The active master re-enables its current source again when all devices have released, and the SCLH signal reaches a HIGH level. The rising of the SCLH signal is done by a resistor pull-up and so is slower, the last part of the SCLH rise time is speeded up because the current source is enabled. Data transfer only switches back to Fast-mode after a STOP condition (P).

A write sequence after the Hs-mode is selected is given in Fig.28. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

After the acknowledgement cycle of a write ($\overline{W}$), one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines CO and $D/\overline{C}$, plus a data byte (see Fig.28 and Table 4).

Table 4 Definition of CO

CO	ACTION
0	last control byte to be sent; only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or RE-START condition
1	another control byte will follow this control byte unless a STOP or RE-START condition is received

Table 5 Definition of $D/\overline{C}$

$D/\overline{C}$	$R/\overline{W}$	ACTION
0	0	data byte will be decoded and used to set up the device
	1	data byte will return the status byte
1	0	data byte will be stored in the display RAM
	1	RAM read-back is not supported

The last control byte is tagged with a cleared most significant bit, the continuation bit CO. The control and data bytes are also acknowledged by all addressed slaves on the bus.

After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended PCF8814 device. If the $D/\overline{C}$ bit of the last control byte was set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed PCF8814. At the end of the transmission the I²C-bus master issues a STOP condition (P) and switches back to Fast-mode, however, to reduce the overhead of the master code, it is possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

A read sequence is shown in Fig.29 and again this sequence follows after the Hs-mode is selected. The device will immediately start to output the requested data until a not acknowledge is transmitted by the master. Before the read access, the user has to set the $D/\overline{C}$ bit to the appropriate value by a preceding write access. The write access should be terminated by a RE-START condition so that the Hs-mode is not disabled.

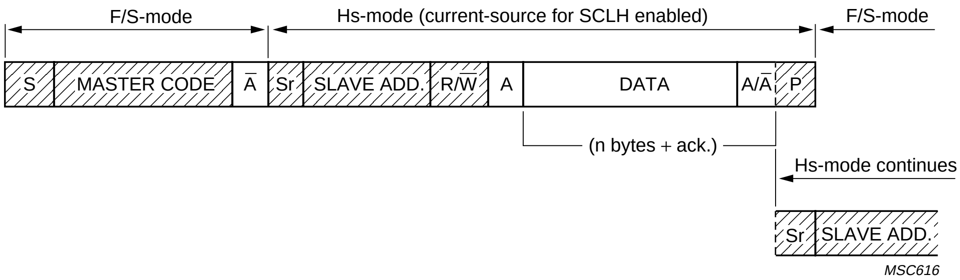


Fig.26 Data transfer format in Hs-mode.

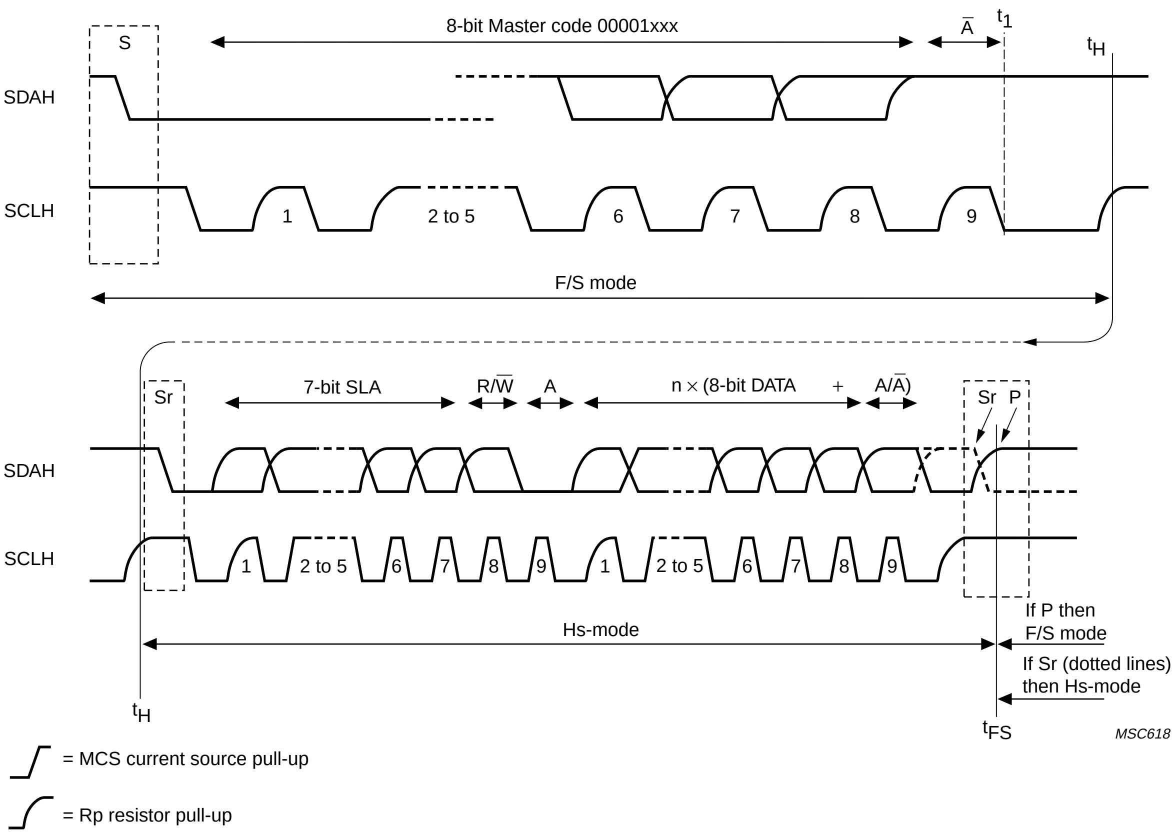


Fig.27 Complete data transfer in Hs-mode.

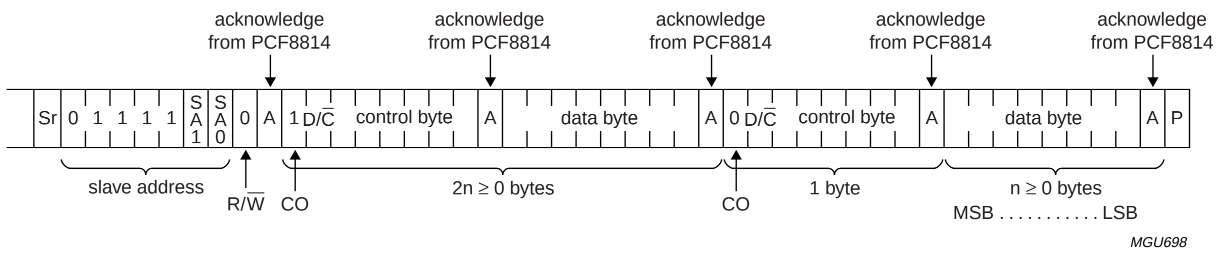


Fig.28 Master transmits in Hs-mode to slave receiver; write mode.

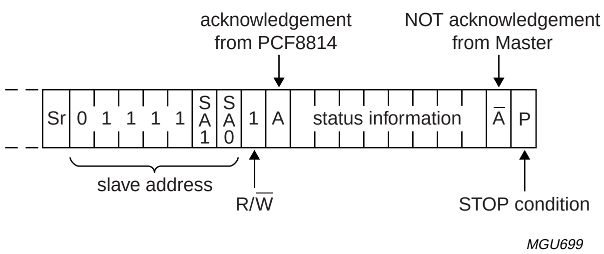


Fig.29 Master receives from slave transmitter (Status Register is read); Read mode.

10.3 Command decoder

The command decoder identifies command words that arrive on the I^2C-bus:

- Pairs of bytes: the first byte determines whether information is display or instruction data; the second byte holds the information
- Stream of information bytes after CO = 0: display or instruction data depending on the last $D/\overline{C}$ state.

The most-significant bit of a control byte is the continuation bit CO. If CO = 1, it indicates that only one data byte, either command or RAM data, will follow. If CO = 0, it indicates that a series of data bytes, either command or RAM data, may follow. The DB6 bit of a control byte is the RAM data/command bit $D/\overline{C}$. When $D/\overline{C}$ = 1, it indicates that a RAM data byte will be transferred next. If $D/\overline{C}$ = 0, it indicates that a command byte will be transferred next.

10.4 Read mode

The I^2C-bus read mode operates differently from the other interfaces. Two different status bytes can be read back and are selected by first sending a Read instruction. A RE-START or STOP-START must then be generated followed by the slave address with the R/W bit set to read in order to read the status register.

Sending the instruction to read ID1, ID2 or VM will select the status byte shown in Table 6.

Sending the instruction to read back the temperature sensor will select the status byte shown in Table 7.

Table 6 ID2, ID1 and VM

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	VM	ID2	ID1

Note

1. X = undefined.

Table 7 Temperature sensor

D7	D6	D5	D4	D3	D2	D1	D0
X	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Note

1. X = undefined.

11 INSTRUCTIONS

The PCF8814 interfaces via two different 3-line serial interfaces, or a 4-line serial interface or an I^2C-bus interface. Processing of the instructions does not require the display clock.

Data accesses to the PCF8814 can be broken-down into two areas, those that define the operating mode of the device, and those that fill the display RAM. For the 4-line SPI interface the distinction is the $D/\overline{C}$ pad. When the $D/\overline{C}$ pad is logic 0, the chip will respond to instructions as defined in Table 8. When the $D/\overline{C}$ bit is logic 1, the chip will send data into the RAM.

When the 3-line SPI or the 3-line serial interface is used, the distinction between instructions which define the operating mode of the device, and those that fill the display RAM is made respectively by the Display data length instruction (3-line SPI) or by the $D/\overline{C}$ bit in the data stream (3-line serial interface).

There are four types of instructions used to perform the following:

- Defining device functions such as display configuration
- Setting internal RAM addresses
- Performing data transfer with internal RAM
- Other instructions.

Note that in the command byte, D7 is the most significant bit.

Table 8 Instruction set

INSTRUCTION	$D/\overline{C}$	COMMAND BYTE								FUNCTION
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	RAM data
Horizontal addressing	0	0	0	0	0	X_3	X_2	X_1	X_0	set X-address, lower 4 bits
	0	0	0	0	1	$x^{(1)}$	X_6	X_5	X_4	set X-address, upper 3 bits
Power control	0	0	0	1	0	1	PC	$x^{(1)}$	$x^{(1)}$	charge pump on/off
Set bias	0	0	0	1	1	0	BS_2	BS_1	BS_0	set bias system
Charge pump control	0	0	0	1	1	1	1	0	1	set multiplication factor
	0	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	S1	S0	
Set initial display line	0	0	1	L_5	L_4	L_3	L_2	L_1	L_0	set start row address
Set V_{OP}	0	0	0	1	0	0	V_{pr7}	V_{pr6}	V_{pr5}	write V_{OP} register
	0	1	0	0	V_{pr4}	V_{pr3}	V_{pr2}	V_{pr1}	V_{pr0}	
Display mode	0	1	0	1	0	0	1	0	DAL	all on/normal display
	0	1	0	1	0	0	1	1	E	normal/inverse display
	0	1	0	1	0	1	1	1	DON	display ON/OFF
Data order	0	1	0	1	0	1	0	0	DOR	swap RAM MSB/LSB order
RAM addressing mode	0	1	0	1	0	1	0	1	V	vertical or horizontal mode
Partial display position	0	1	0	1	0	1	1	0	0	set initial row (R0) of the display
	0	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	C_2	C_1	C_0	
n-line inversion	0	1	0	1	0	1	1	0	1	set n value
	0	F1	$x^{(1)}$	$x^{(1)}$	N_4	N_3	N_2	N_1	N_0	
Vertical addressing	0	1	0	1	1	Y_3	Y_2	Y_1	Y_0	set Y-address
Vertical mirroring	0	1	1	0	0	MY	$x^{(1)}$	$x^{(1)}$	$x^{(1)}$	mirror Y axis (about X axis)
Set partial display	0	1	1	0	1	0	P_2	P_1	P_0	set partial display 1:8 to 1:65
ID read(2)	0	1	1	0	1	1	0	1	0	identification: ID1
	0	1	1	0	1	1	0	1	1	identification: ID2
ID read	0	1	1	0	1	1	1	0	0	identification: ID3

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								FUNCTION
		D7	D6	D5	D4	D3	D2	D1	D0	
ID read	0	1	1	0	1	1	1	0	1	identification: ID4
Temperature sense	0	1	1	0	1	1	1	1	0	temperature read back
VM read	0	1	1	0	1	1	1	1	1	voltage monitor
Row control	0	1	1	1	0	0	0	0	BRS	twist the row blocks
Software reset	0	1	1	1	0	0	0	1	0	internal reset
NOP	0	1	1	1	0	0	0	1	1	no operation
Display data length	0	1	1	1	0	1	0	0	0	display data length for 3-line SPI
	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Temperature compensation	0	0	0	1	1	1	0	0	0	set TC slopes A and B (SLA and SLB)
	0	x[1]	SLB_2	SLB_1	SLB_0	x[1]	SLA_2	SLA_1	SLA_0	
	0	0	0	1	1	1	0	0	1	set TC slopes C and D (SLC and SLD)
	0	x[1]	SLD_2	SLD_1	SLD_0	x[1]	SLC_2	SLC_1	SLC_0	
	0	1	1	1	0	1	0	1	TCE	enable/disable temperature compensation
Oscillator selection	0	0	0	1	1	1	0	1	EC	internal/external oscillator
Set factory defaults[3]	0	0	0	1	1	1	1	1	OTP	enable/disable defaults
Frame frequency	0	1	1	1	0	1	1	1	1	set frame frequency
	0	x[1]	x[1]	x[1]	x[1]	x[1]	x[1]	FR_1	FR_0	
OTP programming	0	1	1	1	1	0	0	OSE	CAL MM	enter calibration mode and control programming
Load 0[4]	0	1	1	0	1	1	0	0	0	write 0 to OTP shift register
Load 1[4]	0	1	1	0	1	1	0	0	1	write 1 to OTP shift register

Notes

1. x = don’t care
2. ID1 will always return 0; ID2 will always return 1.
3. If the factory defaults OTP bit has been programmed to logic 1, then the Set factory defaults instruction is ignored and the device will always use the OTP default data.
4. These bits are used to write data to the OTP shift register when in calibration mode. ID1 = write ‘0’; ID2 = write ‘1’.

Table 9 Special instructions.

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								FUNCTION
		D7	D6	D5	D4	D3	D2	D1	D0	
Set MX	0	1	0	1	0	0	0	0	x	NOP: MX is pad selected
Reserved	0	1	1	1	0	0	1	0	0	reserved
Reserved	0	1	1	1	0	0	1	0	1	reserved

Note

1. x = don’t care

Table 10 Notation used in Table 8

BIT	DESCRIPTION	RESET STATE
DON	0 = display off; 1 = display on	0
E	0 = normal display; 1 = inverse video mode	0
DAL	0 = normal display; 1 = all pixels on	1
MY	0 = no Y mirroring; 1 = Y mirroring	0
PC	0 = charge pump off; 1 = charge pump on	0
DOR	0 = normal data order; 1 = MSB/LSB transposed for RAM data	0
V	0 = horizontal addressing; 1 = vertical addressing	0
BRS	0 = bottom rows are not mirrored; 1 = bottom rows are mirrored	0
TCE	0 = disable temperature compensation; 1 = enable temperature compensation	1
EC	0 = use internal oscillator; 1 = use external oscillator	0
F1	0 = frame inversion disabled and n-line counter runs continuously; 1 = frame inversion enabled and n-line counter reset	0(3)
CALMM	0 = exit OTP calibration mode; 1 = enter OTP calibration mode; see note 1	0
OSE	0 = disable OTP prog. voltage; 1 = enable OTP programming voltage; see note 1	0
SFD(2)	0 = use interface programmed data; 1 = use OTP programmed data	1(3)
N[4:0]	n-line inversion.	01101
FR[1:0]	set frame frequency	00
SLA[2:0]	select slope for segment A	000(3)
SLB[2:0]	select slope for segment B	000(3)
SLC[2:0]	select slope for segment C	000(3)
SLD[2:0]	select slope for segment D	000(3)
BS[2:0]	bias system selection	000(3)
X[6:0]	sets X address (Column) for writing in the RAM.	0000000
Y[3:0]	sets Y address (Bank) for writing in the RAM	0000
C[2:0]	sets the initial R0 of the display.	000
P[2:0]	partial display mode	1:65
S[1:0]	charge pump multiplication factor	00(3)
L[5:0]	sets line address of the display RAM to be displayed on initial R0	000000
Y[3:0]	sets Y address bank for RAM writing	0000000
D[7:0]	display data length for 3-line SPI interface	0000 0000
VPR[7:0]	V_{OP} register	0000 0000(3)

Notes

1. Calibration mode may not be entered if the SEAL bit has been set. Programming is only possible when in calibration mode.
2. If the factory defaults OTP bit has been programmed to 1, then the Set factory defaults instruction is ignored and the device will always use the OTP default data.
3. These values can set by the module maker. If the factory defaults OTP bit has been set, then these values cannot be changed via the interface. Otherwise, the OTP data will only be used if the Set factory defaults instruction OTP bit is set to 1.

Table 11 Display and power mode combinations

DON	DAL	E	FUNCTION
0	0	X	display off, row/col at V_{SS}, oscillator on, HVgen enabled
0	1	X	Power-down mode, display off, row/col at V_{SS}, oscillator off, HVgen disabled
1	0	0	normal display mode
1	0	1	inverse display mode
1	1	X	all pixels on (1)

Note

1. The DAL bit has priority over the E bit.

Table 12 Voltage multiplication factor selection

S1	S0	VOLTAGE MULTIPLIER
0	0	×2
0	1	×3
1	0	×4
1	1	×5

Table 13 Frame frequency selection

FR1	FR0	FRAME FREQUENCY (Hz)
0	0	80
0	1	70
1	0	60
1	1	40

Table 14 Frame frequencies (nominal values) using internal oscillator

MUX RATE	SELECTED FRAME FREQUENCY (Hz)			
	80	70	60	40
1 : 65	80.0	69.7	60.0	40.0
1 : 56	81.4	70.5	61.1	40.7
1 : 48	82.2	71.3	61.4	41.1
1 : 40	82.2	71.0	61.4	41.1
1 : 32	82.2	71.3	61.1	41.1
1 : 24	81.4	71.3	60.9	40.7
1 : 16	80.7	71.3	61.1	40.4
1 : 8	81.4	71.5	60.9	40.7

Table 15 External clock frequencies for given frame rates

MUX RATE	DIVIDER RATIO	EXTERNAL CLOCK FREQUENCY (kHz)
Frame frequency = 80 Hz		
1 : 65	3264	261.1
1 : 56	2688	215.0
1 : 48	3072	245.8
1 : 40	2560	204.8
1 : 32	2560	204.8
1 : 24	2688	215.0
1 : 16	2816	225.3
1 : 8	2688	215.0
Frame frequency = 70 Hz		
1 : 65	3264	228.5
1 : 56	3584	250.9
1 : 48	3072	215.0
1 : 40	3200	224.0
1 : 32	3072	215.0
1 : 24	3072	215.0
1 : 16	3072	215.0
1 : 8	2944	206.1
Frame frequency = 60 Hz		
1 : 65	4352	261.1
1 : 56	3584	215.0
1 : 48	3840	230.4
1 : 40	3840	230.4
1 : 32	3584	215.0
1 : 24	3456	207.4
1 : 16	3584	215.0
1 : 8	3456	207.4
Frame frequency = 40 Hz		
1 : 65	6528	261.1
1 : 56	5376	215.0
1 : 48	6144	245.8
1 : 40	5120	204.8
1 : 32	5120	204.8
1 : 24	5376	215.0
1 : 16	5632	225.3
1 : 8	5376	215.0

Table 16 Partial display control

P2	P1	P0	MUX RATE	p
0	0	0	1 : 65	4
0	0	1	1 : 56	4
0	1	0	1 : 48	4
0	1	1	1 : 40	4
1	0	0	1 : 32	2
1	0	1	1 : 24	2
1	1	0	1 : 16	2
1	1	1	1 : 8	2

11.1 Initialization

Immediately following power-on all internal registers, as well the RAM content, are undefined and the device must be reset.

Reset is accomplished by applying an external pulse (active LOW) at the pad $\overline{RES}$. When reset occurs within the specified time, all internal registers are reset, however the RAM is still undefined. The state of the device after reset is described in Section 11.2. The $\overline{RES}$ input must be $\leq 0.3V_{DD1}$ when V_{DD1} reaches $V_{DD(min)}$ (or higher) within a maximum time t_{VHRL} after V_{DD1} going HIGH (see Fig.41).

A reset can also be achieved by sending a reset command. This command can be used during normal operation but not to initialize the chip after power-on.

11.2 Reset function

After reset the LCD driver has the following state:

- After power-on, RAM data is undefined, the reset signal does not change the content of the RAM
- All LCD outputs at V_{SS} (display off)
- Internal oscillator is off
- Power-down mode is active.

11.3 Power-down mode

Power-down mode gives the following circuit status:

- All LCD outputs at V_{SS} (display off)
- Bias generator and V_{LCD} generator switched off; external V_{LCD} can be disconnected
- Oscillator off (external clock possible)
- RAM contents unchanged; RAM data can be written
- V_{LCD} discharged to V_{SS} in this mode.

Power-down mode is active when the display is OFF (DON = 0) and all the pixels ON (DAL = 1) is set.

11.4 Display control

The bits DON, DAL and E select the display mode (see Table 11).

11.4.1 MIRROR X

When MX = 0, the display RAM is written from left to right (X = 0, is on the left side). When MX = 1, the display RAM is written from right to left (X = 0, is on the right side).

MX has an impact on the way the RAM is written. If horizontal mirroring of the display is desired, the RAM must first be rewritten, after changing MX.

11.4.2 MIRROR Y

When MY = 1, the display is mirrored vertically.

A change of this bit has an immediate effect on the display.

11.5 Set Y address of RAM

Y[3:0] defines the Y address of the display RAM. All undefined states in Table 17 are reserved.

Table 17 X/Y address range

Y3	Y2	Y1	Y0	BANK
0	0	0	0	Bank 0
0	0	0	1	Bank 1
0	0	1	0	Bank 2
0	0	1	1	Bank 3
0	1	0	0	Bank 4
0	1	0	1	Bank 5
0	1	1	0	Bank 6
0	1	1	1	Bank 7
1	0	0	0	Bank 8

11.6 Set X address of RAM

The X address points to the columns. The range of X is from 0 to 95.

11.7 Set display start line

L[5:0] is used to select the display line address of the display RAM to be displayed on the initial row (R0). L[5:0] must not be set higher than the current multiplex system, i.e. if P[2:0] = 010 (MUX 1 : 48), then L[5:0] must be in the range 0 to 47.

The initial row is set by C[2:0] and can only be defined in steps of 8. C[2:0] should not be set such that it causes the visible display area to be wrapped from the bottom of the screen to the top, i.e. $(C[2:0] \times 8) + \text{MUX rate} \leq 65$.

Figure 31 shows the mapping from the RAM content to the display. The content of the RAM is not modified. This allows for screen scrolling, without the need to rewrite the RAM. Figure 32 shows some example screen shots.

Table 18 Initial row selection

C2	C1	C0	ROW
0	0	0	Row 0
0	0	1	Row 8
0	1	0	Row 16
0	1	1	Row 24
1	0	0	Row 32
1	0	1	Row 40
1	1	0	Row 48
1	1	1	Row 56

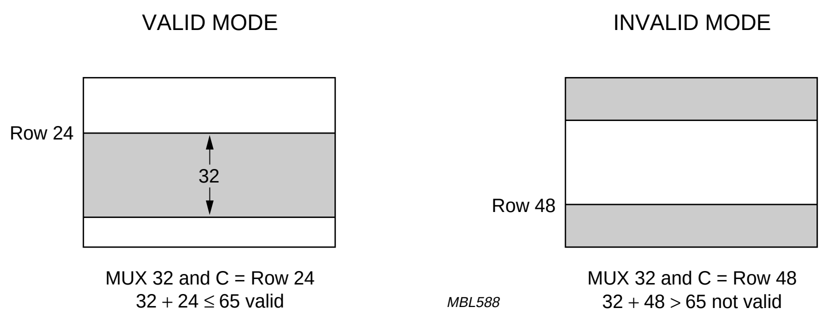


Fig.30 Valid values for ‘p’ (MUX mode) and C (initial row selection).

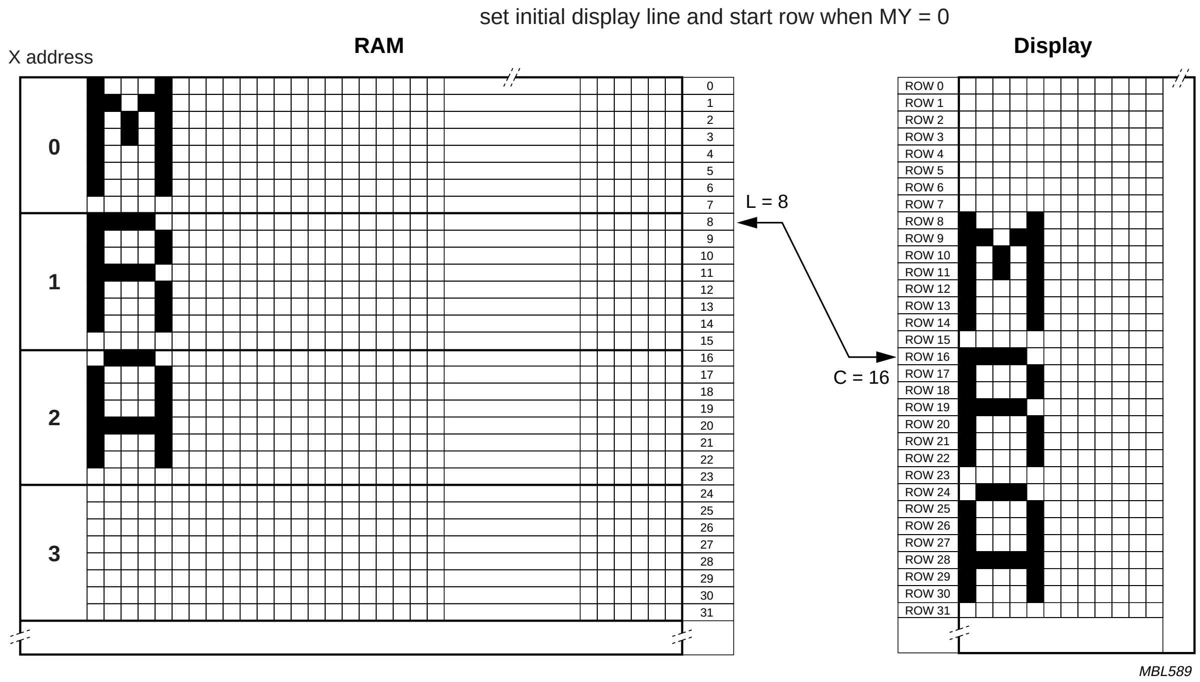


Fig.31 Programming the L address and C address when MY = 0.

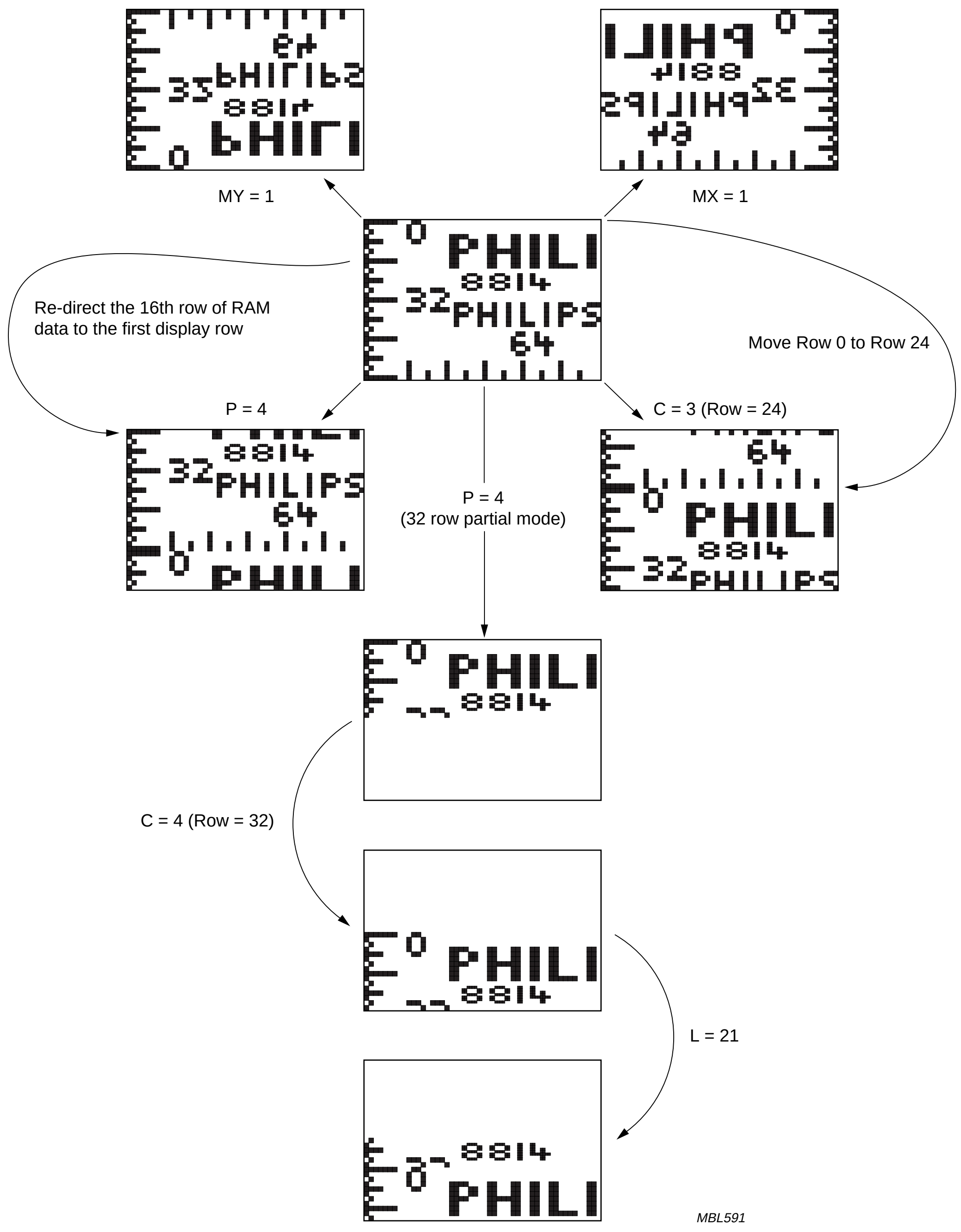


Fig.32 Effects of L and C address, MX, MY and partial displays.

11.8 Bias levels

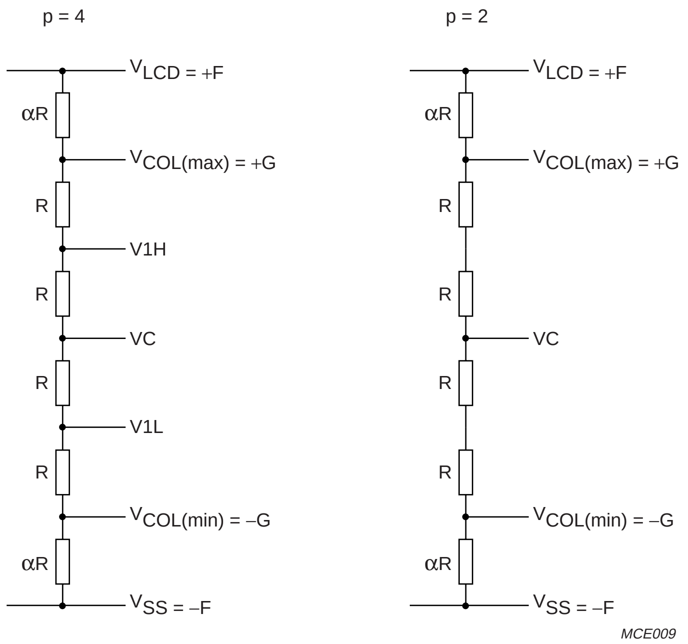


Fig.33 Bias system.

The bias voltage levels (see Fig.33) are a function of the row voltage F and ‘a’ where:

$$F = \frac{V_{LCD}}{2}$$

$$F \geq G$$

$$F = \frac{G \times a}{p}$$

$$\frac{F}{G} = \frac{a}{p}$$

Depending on the value of p, the bias levels are set according to the following ratios:

When p = 2, the bias level is: αR – 2R – 2R – αR

When p = 4, the bias level is: αR – R – R – R – R – αR

The value of α is in the range from 0.15 to 1.35.

The value of F is determined by (2α + 4) × R, and the value of G is determined by 4R.

Also from:

$$\frac{F}{G} = \frac{a}{p} = \frac{(2\alpha + 4) \times R}{4R} = \frac{(2\alpha + 4)}{4} = 1 + \frac{\alpha}{2}$$

or:

$$\alpha = \left(\frac{F}{G} - 1\right) \times 2$$

the relationship between a and α for a given value of p is given by:

$$a = \left(\frac{\alpha}{2} + 1\right) \times p \qquad \alpha = \left(\frac{a}{p} - 1\right) \times 2$$

This leads to the bias settings given in Table 19. The bias can be selected in software and also programmed by OTP.

Table 19 Bias settings

BS[2:0]	F/G	α	a (p = 2)	a (p = 4)
000	1.075	0.15	2.15	4.3
001	1.150	0.30	2.30	4.6
010	1.225	0.45	2.45	4.9
011	1.300	0.60	2.60	5.2
100	1.375	0.75	2.75	5.5
101	1.450	0.90	2.90	5.8
110	1.525	1.05	3.05	6.1
111	1.675	1.35	3.35	6.7

The V_{ON} and V_{OFF} value can be calculated from the following equations:

$$V_{ON} = \frac{F}{a} \times \sqrt{\frac{p \times (a^2 + N + 2a)}{N}}$$

$$V_{OFF} = \frac{F}{a} \times \sqrt{\frac{p \times (a^2 + N - 2a)}{N}}$$

Where V_{ON} is defined by the threshold voltage (V_{TH}) of the liquid crystal display and N is the number of driven lines.

The relationship between selected MUX-rate, the number of simultaneously-selected rows (p) and the number of driven lines is shown in Table 20.

Table 20 Relationship between MUX rate, MUX mode (p) and number of driven lines (N)

MUX RATE	p	N
1:80	2	8
1:16	2	16
1:24	2	24
1:32	2	32
1:40	4	40
1:48	4	48
1:56	4	56
1:65	4	68

When the selected MUX rate, bias system (a) and the threshold voltage (V_{TH}) of the liquid crystal display are defined, LCD supply voltage (V_{LCD}) is determined by:

$$V_{LCD} = 2a \times V_{TH} \times \sqrt{\frac{N}{p(a^2 + N + 2a)}}$$

11.9 LCD drive voltage

11.9.1 LCD DRIVE VOLTAGE GENERATION

V_{LCD} may be supplied externally or generated internally by the on-chip capacitive charge pump.

The Power control instruction may be used to switch V_{LCD} generation on or off. The Charge pump control instruction may be used to select the required voltage multiplication factor. The Set V_{OP} instruction is used for programming the LCD drive voltage V_{LCD}.

The generation of V_{LCD} is illustrated in Fig.34. This shows all factors that effect V_{LCD} generation, including the 6 bits of MMVOPCAL (from OTP) and the 7 bits resulting from the temperature compensation mechanism. Equations summarizing all factors are

$$V_{OP} = V_{PR} + MMVOPCAL + V_T \quad (1)$$

and

$$V_{LCD} = V_{OP} \times b + a \quad (2)$$

Where:

V_{PR}[7:0] is set in the instruction decoder and is the programmed V_{PR} register value as an unsigned number

MMVOPCAL[5:0] is the value of the offset stored in the OTP cells in twos complement format

V_T[7:0] in twos complement format comes from the temperature compensation block (see Table 23)

a and b are fixed constant values (see Table 21).

Table 21 Parameters of V_{LCD}

SYMBOL	VALUE	UNIT
b	0.03	V
a	3	V

CAUTION
As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9 V), the user has to ensure, while setting the V_{PR} register and selecting the temperature compensation, that under all conditions and including all tolerances V_{LCD} remains below 9.0 V. Also, because the programming range for the internally generated V_{LCD} allows values below the minimum allowed V_{LCD} (5 V), the user has to ensure, while setting the V_{PR} register and selecting the temperature compensation, that under all conditions and including all tolerances V_{LCD} remains above 5.0 V.

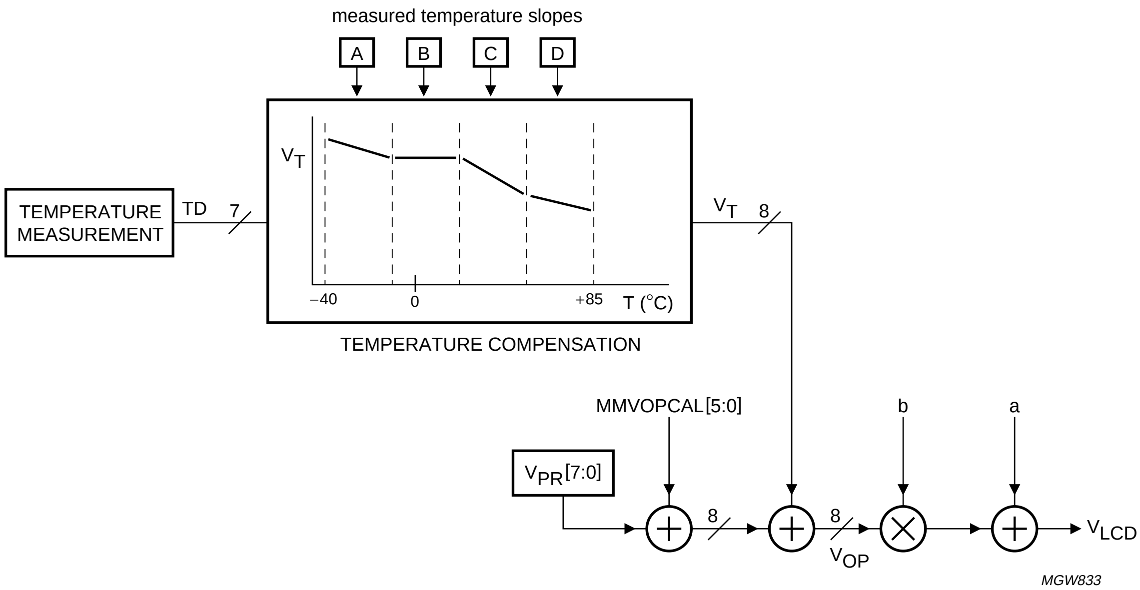
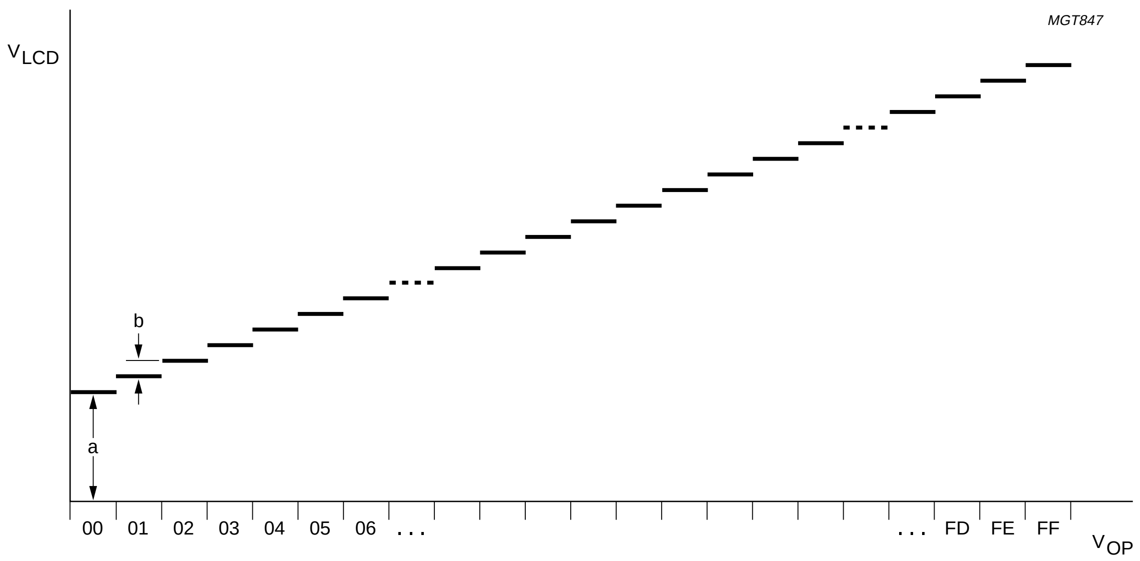


Fig.34 V_{LCD} generation including the temperature compensation and OTP calibration.



V_{PR}[7:0] programming: 00 to FF (HEX).
Assuming MMVOPCAL = 0 and V_T = 0 V.

Fig.35 V_{LCD} programming of PCF8814 shown as plots of equations (1) and (2).

11.9.2 TEMPERATURE MEASUREMENT

The temperature measurement is repeated every 10 seconds. The measured value is provided as a 7-bit digital value TD[6:0] which can be read back via the interface. The temperature can be determined from TD[6:0] using the equation

$$T = (1.875 \times TD - 40)°C \quad (3)$$

11.9.3 TEMPERATURE COMPENSATION

Due to the temperature dependency of the liquid crystal's viscosity, the LCD controlling voltage V_{LCD} may have to be adjusted at different temperatures to maintain optimal contrast.

Internal temperature compensation may be enabled via the Temperature compensation enable instruction. When the internal temperature compensation is applied (TCE bit is set to 1) then according to Equation (1) the V_{LCD} depends also on V_T (the temperature compensation component defined in Table 23), otherwise V_T is considered to be 0 V.

There are four temperature coefficients MA, MB, MC and MD that correspond to four equally spaced temperature regions (see Fig.36 and Table 22). Each coefficient can be selected from a choice of eight different slopes, or multiplication factors. Each one of these coefficients may be independently selected by the user via the Temperature compensation enable instruction. The default for each slope register can be stored in OTP.

Table 22 Temperature coefficients

SLA, SLB, SLC and SLD	MA, MB, MC and MD(1)	SLOPE(1)(2) (mV/K)
111	2.50	–40
110	1.75	–24
101	1.25	–20
100	1.00	–16
011	0.75	–12
010	0.50	–8
001	0.25	–4
000	0.00	0

Notes

1. The relationship between Mn and SLOPE is derived from the ratio of an LSB for TD (1.875 K/LSB) and an LSB for V_{OP} (30 mV/LSB).
2. Slopes of V_{LCD} are calculated from equations (1), (2), (3) and Table 23

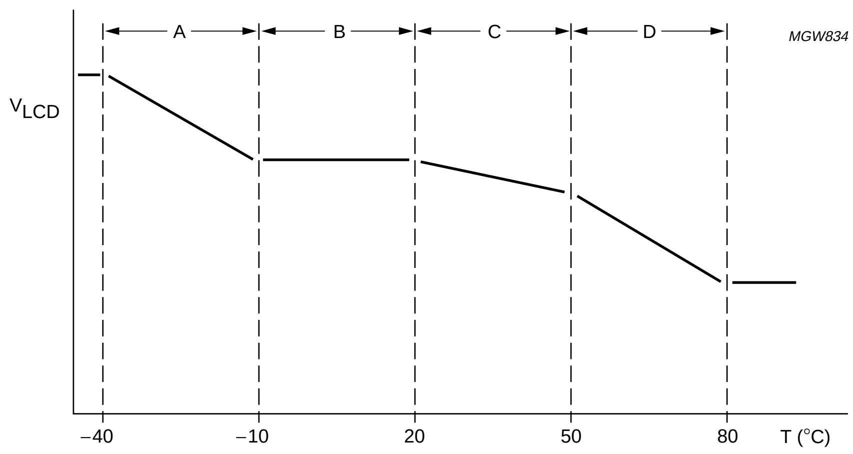


Fig.36 Example of segmented temperature coefficients.

Table 23 Temperature compensation equations

TEMPERATURE RANGE (°C)	TD RANGE	EQUATION
–40 to –11	0 to 15	$V_T = (16 \times MB) + MA \times (16 - TD)$
–10 to +19	16 to 31	$V_T = (32 \times TD) \times MB$
+20 to +49	32 to 47	$V_T = -[(TD \times 32) \times MC]$
+50 to +79	48 to 63	$V_T = -[(16 \times MC) + MD \times (TD - 48)]$

Temperature compensation is implemented by adding an offset V_T to the V_{PR} value (additionally to the OTP calibration offset MMVOPCAL).

The final result for V_{LCD} calculation is an 8-bit positive number as shown in equations (1) and (2). Care must be taken by the user to ensure that the ranges of V_{PR}, MMVOPCAL and V_T do not cause clipping and hence undesired results. The adder stages will not permit overflow or underflow and will clamp results at either end of the range.

The temperature read-out generates a 7-bit result, TD[6:0]. For temperatures below –40 °C, the value of TD is zero. For temperatures above 79 °C, the value of TD is higher than 63, but for V_T calibration the value TD = 63 is used.

The offset value V_T may be calculated from Table 23. The effect on V_{LCD} can be calculated by multiplying the offset value with the value of b (from Table 21).

For example, if T = –10 °C, TD = 16 and MB = 1.25 then $V_{LCD(offset)}$ = 30 mV × (32 – 16) × 1.25 = 600 mV.

11.10 N-line inversion

To improve the optical characteristics of the display, N-line inversion has been implemented with two options:

- When frame inversion is ON, N-line inversion is restarted every frame
- When frame inversion is OFF, the N-line inversion counter runs continuously.

Table 24 N-line inversion

PARAMETER	VALUE	p = 2	p = 4
N[4:0]	00000	no N-line inversion	no N-line inversion
	00001	invert every 2 rows	invert every 4 rows
	:	:	:
	11111	invert every 62 rows	invert every 124 rows
FI	1	frame inversion ON; N-line counter restarted at every frame	
	0	frame inversion OFF; N-line counter runs continuously	

11.11 Orthogonal functions

The orthogonal functions used in the PCF8814 are shown in Tables 25 and 26. SF refers to the sub-frame. All the rows will have the first function applied before the function moves on to its next state. For clarity, no N-line inversion is shown here.

Figure 37 shows the row waveforms and Fig.38 shows the orthogonal function selection for the PCF8814.

Table 25 Orthogonal functions: p = 4

1st FOUR ROWS	NORMAL FRAME				INVERSE FRAME			
	SF0	**SF1**	**SF2**	**SF3**	**SF0**	**SF1**	**SF2**	**SF3**
R0	1	0	0	0	0	1	1	1
R1	0	1	0	0	1	0	1	1
R2	0	0	1	0	1	1	0	1
R3	0	0	0	1	1	1	1	0

Table 26 Orthogonal functions: p = 2

1st TWO ROWS	NORMAL FRAME		INVERSE FRAME	
	SF0	**SF1**	**SF0**	**SF1**
R0	1	0	0	1
R1	1	1	0	0

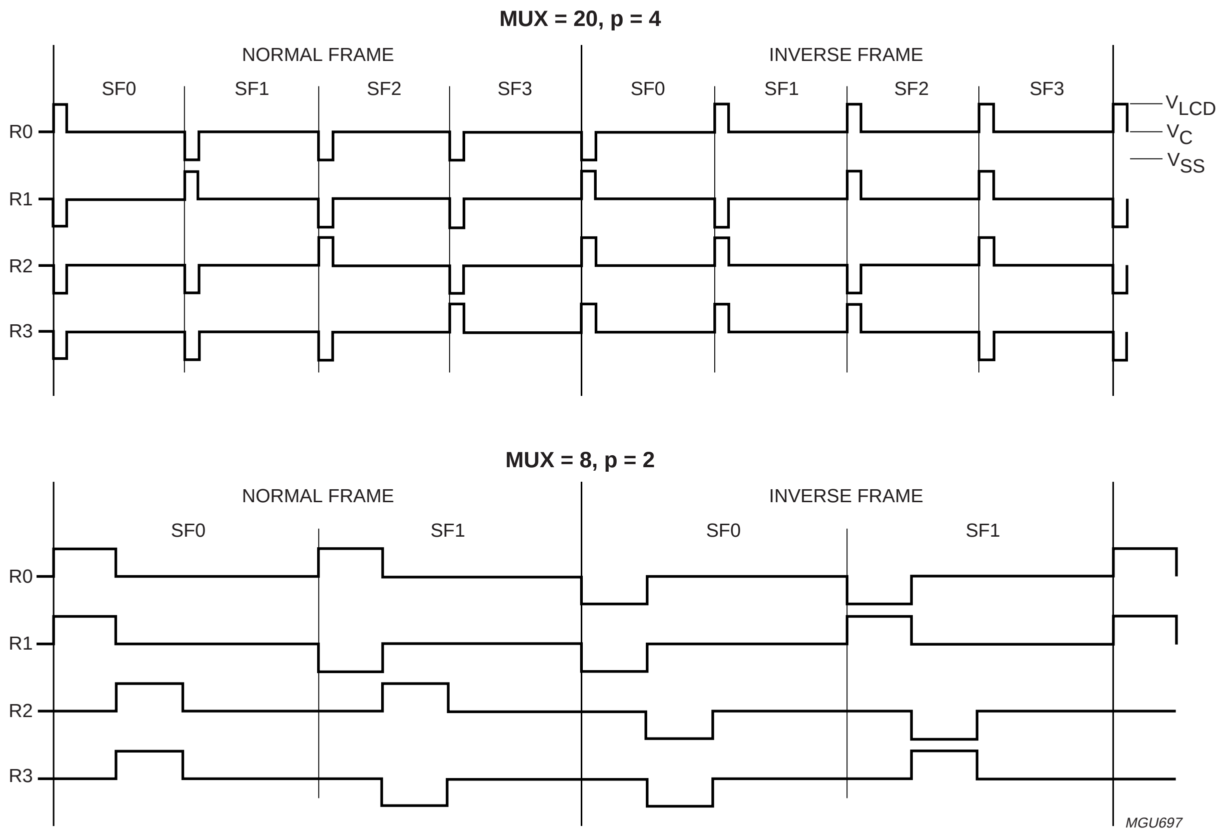


Fig.37 Row waveforms.

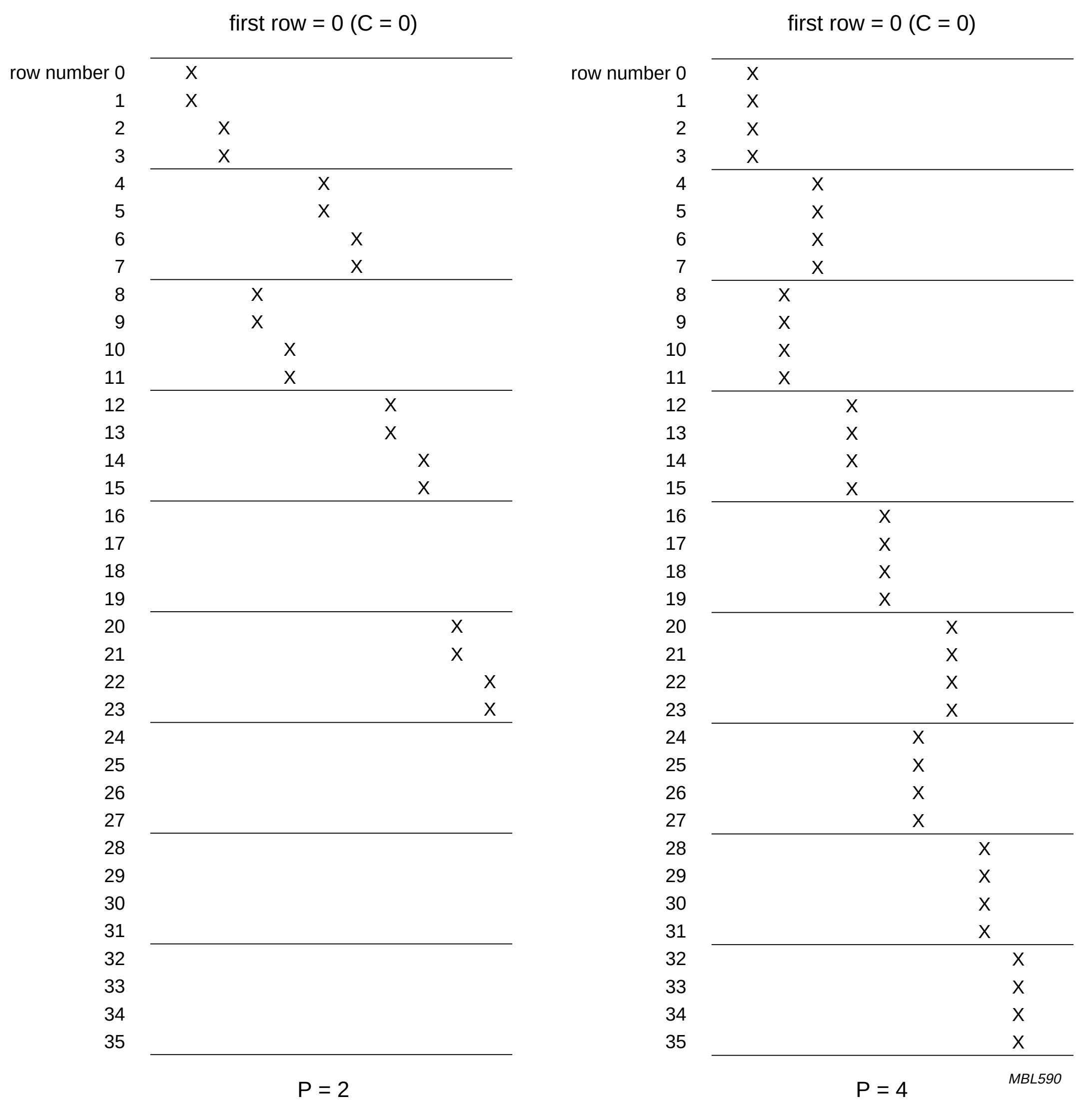


Fig.38 Order of selection of rows for p = 4 and p = 2.

11.12 Voltage monitor

The voltage monitor is an integrated test circuit which indicates the status of the charge pump via the VM bit. In normal operation the charge pump will be switching on and off regularly and it is this operation that is checked each frame. Care must be taken when configuring the charge pump. Setting the number of stages too few, the V_{OP} voltage too high or using a low V_{DD2} can all lead to an incorrectly-operating change pump.

Table 27 Voltage monitor bit VMs

BIT VM	CHARGE PUMP STATUS
0	indicates the charge pump is not working correctly
1	indicates the charge pump is working correctly

11.13 Bottom Row Swap

Bottom Row Swap (BRS) allows for the possibility to route to the module in two different ways as shown by the row count in Figs 39 and 40.

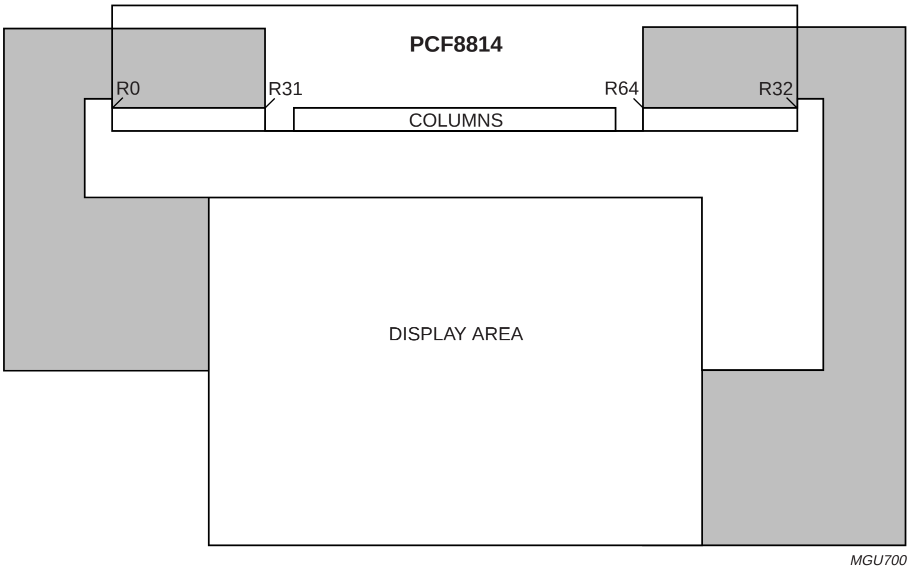


Fig.39 BRS = 0.

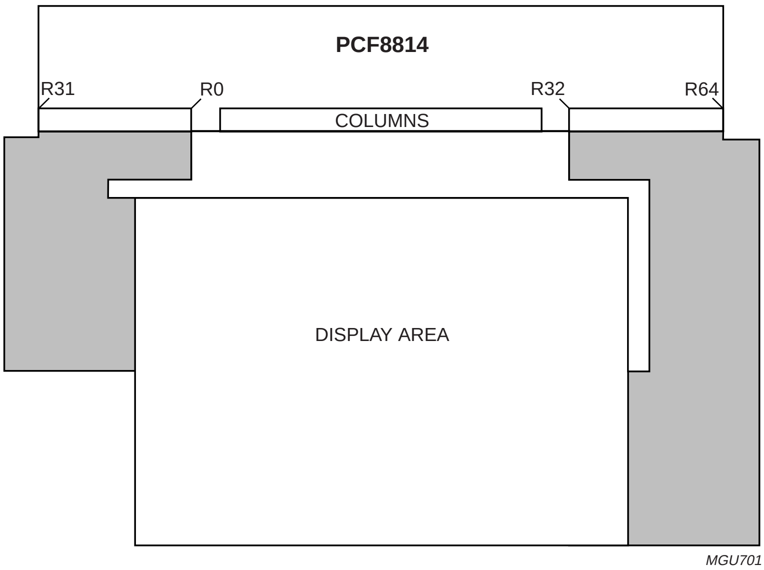


Fig.40 BRS = 1.

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD1}	supply voltage 1	–0.5	+6.5	V
V_{DD2}	supply voltage 2	–0.5	+5.0	V
V_{DD3}	supply voltage 3	–0.5	+5.0	V
V_{LCDIN}	LCD supply voltage input	–0.5	+10.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_{SS}	ground supply current	–50	+50	mA
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	300	mW
P_O	power dissipation per output	–	30	mW
T_{stg}	storage temperature	–65	+150	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise stated.

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

14 DC CHARACTERISTICS

V_{DD1} = 1.7 V to 3.3 V; V_{SS} = 0 V; V_{LCD} = 3 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage 1		1.7	–	3.3	V
$V_{DD2,3}$	supply voltages 2 and 3		2.4	–	4.5	V
V_{LCDIN}	LCD supply voltage input	LCD voltage externally supplied (voltage generator disabled)	–	–	9.0	V
V_{LCDOUT}	generated LCD supply voltage	LCD voltage internally generated (voltage generator enabled); note 1	–	–	9.0	V
$V_{LCD(tol)}$	tolerance of generated V_{LCD}	with calibration; note 2	–70	–	+70	mV
$I_{DD(tot)}$	total supply current (I_{DD1} + I_{DD2} + I_{DD3})	Power-down mode; notes 3 and 4	0.1	1.5	5	μA
I_{DD1}	V_{DD1} supply current	Normal mode; note 4	5	35	50	μA
$I_{DD2,3}$	supply current (I_{DD2} + I_{DD3})	display load = 15 μA; Normal mode; note 4	–	90	140	μA
		display load = 30 μA; Normal mode; note 4	–	150	225	μA
		display load = 50 μA; Normal mode; note 4	–	250	340	μA
		display load = 170 μA; Normal mode; note 4	–	800	1020	μA
Logic circuits						
V_{OL}	LOW-level output voltage	I_{OL} = 0.5 mA	V_{SS}	–	$0.2V_{DD}$	V
V_{OH}	HIGH-level output voltage	$–I_{OH}$ = 0.5 mA	$0.8V_{DD}$	–	V_{DD}	V
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_L	leakage current	V_I = V_{DD} or V_{SS}	–1	–	+1	μA
Column and row outputs						
R_{col}	column output resistance C0 to C95	V_{LCD} = 5 V	–	5	20	kΩ
R_{row}	row output resistance R0 to R64	V_{LCD} = 5 V	–	5	20	kΩ
$V_{col(tol)}$	bias tolerance C0 to C95		–70	0	+70	mV
$V_{row(tol)}$	bias tolerance R0 to R64		–70	0	+70	mV

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Valid for values of temperature, V_{PR} and TC used at the calibration and with temperature calibration disabled.
3. During Power-down all static currents are switched off.
4. Conditions are: V_{DD1} = 1.8 V, V_{DD2} = 2.7 V, V_{LCD} = 7.5 V, voltage multiplier = $4V_{DD2}$, inputs at V_{DD1} or V_{SS}, interface inactive, internal V_{LCD} generation, T_{amb} = +25 °C.

15 AC CHARACTERISTICS

V_{DD1} = 1.8 V to 3.3 V; V_{SS} = 0 V; $V_{LCD(max)}$ = 9.0 V; T_{amb} = –40 to +85 °C; all timings specified are based on 20% and 80% of V_{DD}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{ext}	external clock frequency	see Table 15; MUX rate 1 : 65				
		f_{frame} = 80 kHz; divider ratio = 3264	–	261.1	–	kHz
		f_{frame} = 70 kHz; divider ratio = 3264	–	228.5	–	kHz
		f_{frame} = 40 kHz; divider ratio = 6528	–	261.1	–	kHz
f_{frame}	frame frequency	V_{DD1} = 1.7 V to 3.3 V; T_{amb} = –40 to +85 °C	72	80	88	Hz
		V_{DD1} = 1.8 V; MUX rate 1 : 65; T_{amb} = 27 °C	37	40	43	Hz
Reset; see Fig.41						
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW time	note 1	0	–	1	us
t_{RW}	reset pulse width LOW time		1000	–	–	ns
t_{RWS}	reset pulse width spike suppression		1000	–	–	ns
3-line and 4-line SPI and serial interface; see Figs 42 to 45						
f_{SCLK}	SCLK frequency		–	–	6.5	MHz
T_{cyc}	SCLK cycle time		153	–	–	ns
t_{PWH1}	SCLK pulse width HIGH		60	–	–	ns
t_{PWL1}	SCLK pulse width LOW		60	–	–	ns
t_{S2}	$\overline{SCE}$ set-up time		60	–	–	ns
t_{H2}	$\overline{SCE}$ hold time		55	–	–	ns
t_{PWH2}	$\overline{SCE}$ minimum HIGH time		50	–	–	ns
t_{H5}	$\overline{SCE}$ start hold time	note 2	50	–	–	ns
t_{S4}	SDIN set-up time		60	–	–	ns
t_{H4}	SDIN hold time		60	–	–	ns
t_{S3}	Data/$\overline{\text{Command}}$ set-up time		60	–	–	ns
t_{H3}	Data/$\overline{\text{Command}}$ hold time		60	–	–	ns
t_{S1}	SDIN set-up time		50	–	–	ns
t_{H1}	SDIN hold time		50	–	–	ns
t_1	SDO access time		–	–	100	ns
t_2	SDO disable time	SPI 3-line or 4-line interface	–	–	50	ns
t_3	$\overline{SCE}$ hold time		50	–	–	ns
t_4	SDO disable time	3-line serial interface	25	–	100	ns
C_b	capacitive load for SDO	f_{SCLK} = 6.5 MHz	–	–	50	pF
R_b	series resistance for SDO	including ITO track + connector resistance + PCB	–	–	500	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus interface; see Fig.46						
f_{SCLH}	SCLH clock frequency		0	–	3.4	MHz
$t_{SU;STA}$	set-up time repeated START		160	–	–	ns
$t_{HD;STA}$	hold time repeated START		160	–	–	ns
t_{LOW}	SCLH LOW time		160	–	–	ns
t_{HIGH}	SCLH HIGH time		60	–	–	ns
$t_{SU;DAT}$	data set-up time		10	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	70	ns
t_{rCL}	SCLH rise time		10	–	40	ns
t_{rCL1}	SCLH rise time after acknowledge bit		20	–	80	ns
t_{fCL}	SCLH fall time		10	–	40	ns
t_{rDA}	SDAH rise time		20	–	80	ns
t_{fDA}	SDAH fall time		20	–	80	ns
$t_{SU;STO}$	set-up time STOP condition		160	–	–	ns
C_b	SDAH and SCLH capacitive load	total capacitance for one bus line	–	–	100	pF
C_{b1}	SDAH + SDAHOUT line and SCLH line capacitive load		–	–	400	pF
t_{SW}	tolerable spike width on bus		–	–	5	ns
V_{nL}	noise margin at the LOW level for each connected device (including hysteresis)		$0.1V_{DD}$	–	–	V
V_{nH}	noise margin at the HIGH level for each connected device (including hysteresis)		$0.2V_{DD}$	–	–	V

Notes

1. $\overline{RES}$ may be LOW before V_{DD} goes HIGH.
2. t_{H5} is the time from the previous SCLK rising edge (irrespective of the state of $\overline{SCE}$) to the falling edge of $\overline{SCE}$.

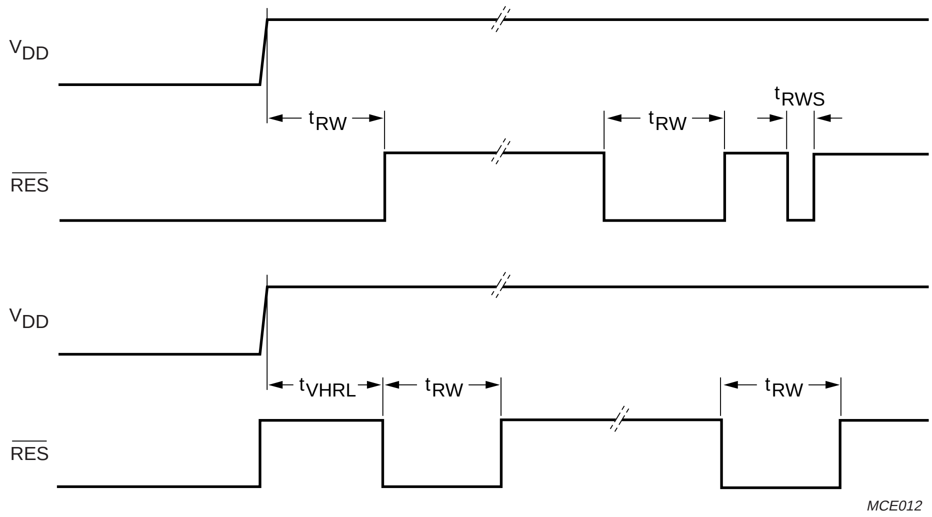


Fig.41 Reset timing.

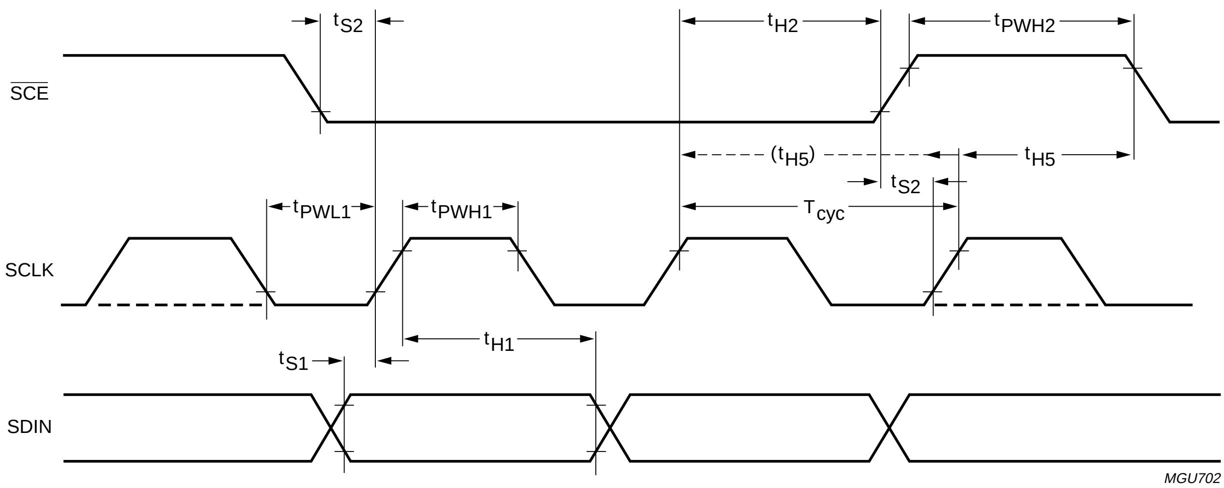


Fig.42 3-line serial interface timing.

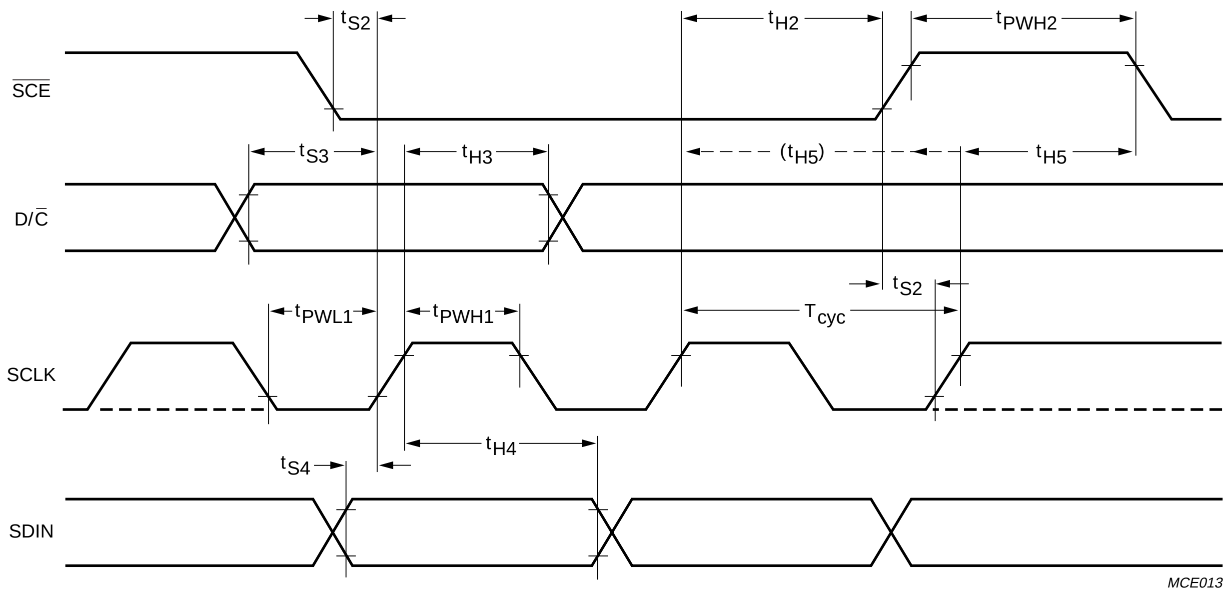


Fig.43 4-line serial interface timing.

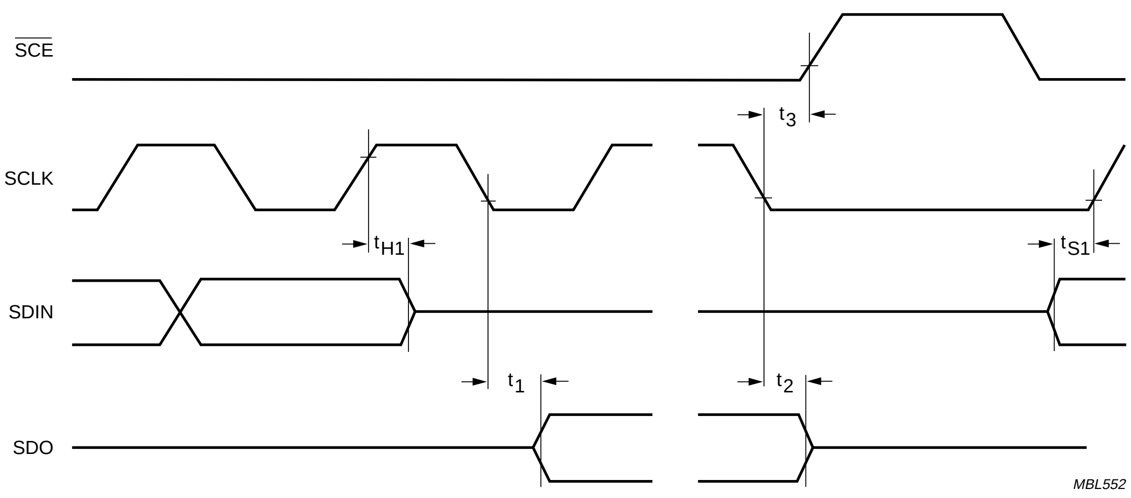


Fig.44 SPI 3-line or 4-line serial interface timing - read mode.

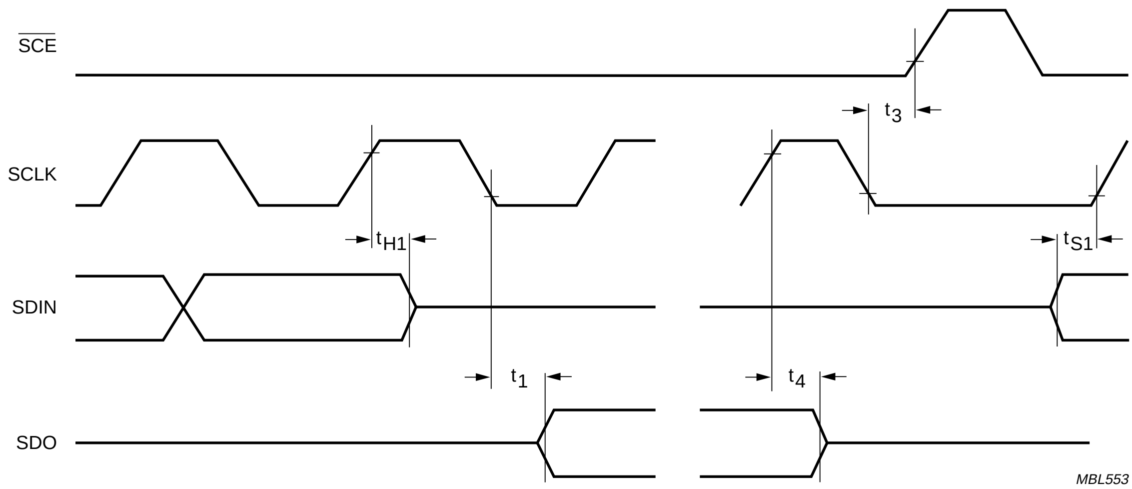
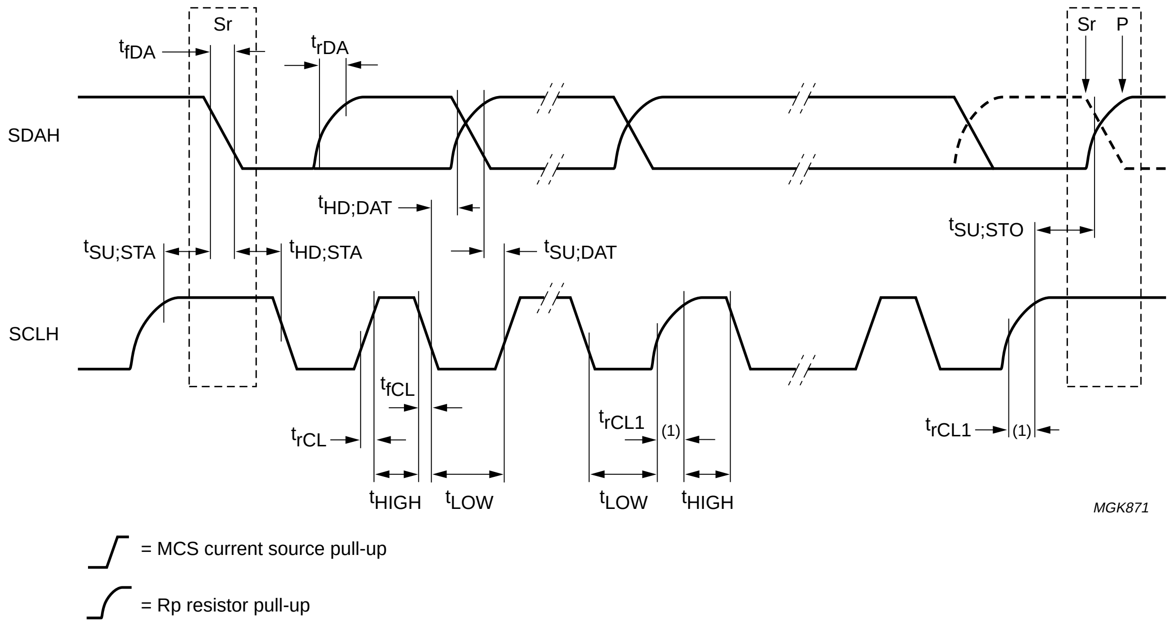


Fig.45 3-line serial interface timing - read mode.



(1) Rising edge of the first SCLH clock pulse after an acknowledge bit.

Fig.46 I^2C-bus timing diagram (Hs-mode).

16 APPLICATION INFORMATION

16.1 Protection from light

Semiconductors are light sensitive. Exposure to light sources can cause malfunction of the IC. In the application it is therefore required to protect the IC from light. The protection must be done on all sides of the IC, i.e. front, rear and all edges.

16.2 Chip-on-glass application

The pinning of the PCF8814 has an optimal design for single-plane wiring e.g. for chip-on-glass display modules. Display size: 65 x 96 pixels.

16.3 Application capacitor values

In the following applications, the required minimum values for the external capacitors are:

- C_{VLCD} = 100 nF (depending on application higher values may give better display performance)
- C_{VDD}, C_{VDD1}, C_{VDD2} = 1 μF
- Higher values can be used for the supply capacitors.

16.4 Supply voltage V_{DD1}

If an external V_{LCD} supply is used, V_{DD1} should not be removed at any time. Power saving should always be achieved using the Power-down mode. With an internal V_{LCD} supply, V_{DD1} should only be removed if entirely necessary by using the following procedure:

1. Discharge the V_{LCD} voltage prior to disconnecting V_{DD1} (this avoids the occurrence of display aberrations). The discharge time depends on the size of C_{VLCD} and how the PCF8814 is shut down; the fastest way to reduce the voltage is:
   a) Switch off the charge pump by setting bit PC of the Power control instruction to logic 0.
   b) Switch off the display by setting bits DON and DAL of the Display mode to logic 0.
2. Follow this action with a short delay (the delay period is application-dependent and must be determined by experimentation).
3. Put the PCF8814 into Power-down mode and remove V_{DD1} (if Power-down mode is entered without going via display-off, the time required to discharge C_{VLCD} may be considerably longer).

16.5 Application examples

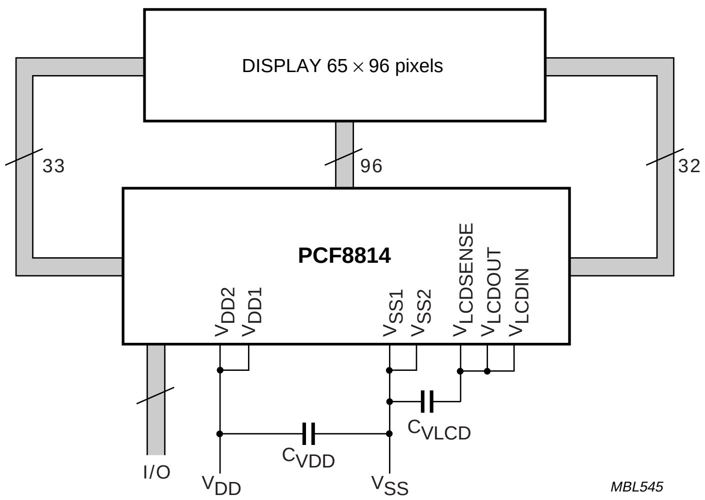


Fig.47 Application example using the internal charge pump and a single V_{DD} source.

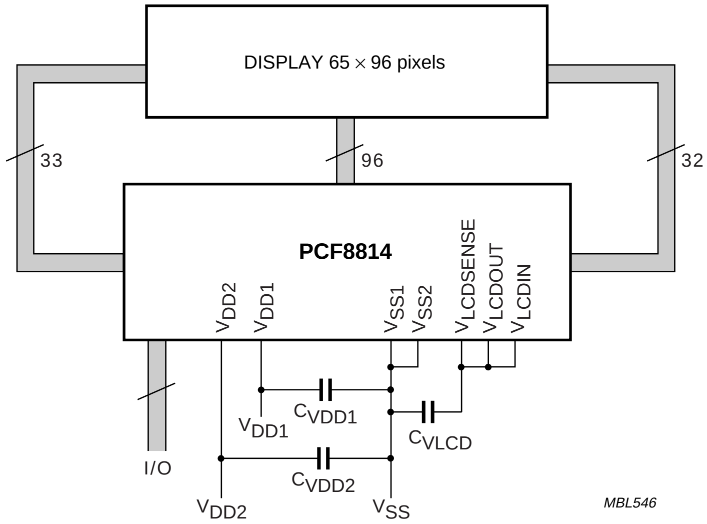


Fig.48 Application example using the internal charge pump and two separate V_{DD} sources (V_{DD1} and V_{DD2}).

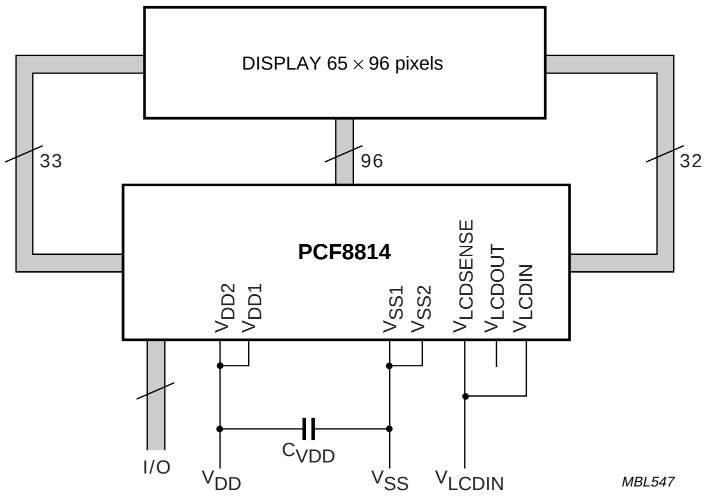


Fig.49 Application example using external high voltage generation.

17 MODULE MAKER PROGRAMMING

One Time Programmable (OTP) technology has been implemented on the PCF8814. It enables the module maker to program some extended features of the PCF8814 after it has been assembled on an LCD module.

Programming is made under the control of the interfaces and the use of one special pad. This pad must be made available on the module glass but needs not to be accessed by the set maker.

The PCF8814 features 6 module maker programmable parameters:

- V_{LCD} calibration
- Default temperature compensation slopes
- Default charge pump multiplication factor
- Default V_{PR} value
- Default bias system
- n-line inversion control
- Enable factory defaults
- Seal bit.

17.1 LCD voltage calibration

The LCD voltage (V_{LCD}) can be tuned with a 6-bit code (MMVOPCAL[5:0]). This code is implemented in twos complement notation giving rise to a positive or negative offset to the V_{PR} register.

The adder in the circuit has underflow and overflow protection. In the event of an overflow, the output will be clamped to 255; whilst during an underflow the output will be clamped to 0.

Examples of possible MMVOPCAL codes are given in Table 28.

Table 28 Possible MMVOPCAL codes

MMVOPCAL[5:0]	DECIMAL EQUIVALENT	V_{LCD} OFFSET (mV)
011111	31	+930
011110	30	+900
011101	29	+870
:	:	:
000010	2	+60
000001	1	+30
000000	0	0
111111	–1	–30
111110	–2	–60
:	:	:
100010	–30	–900
100001	–31	–930
100000	–32	–960

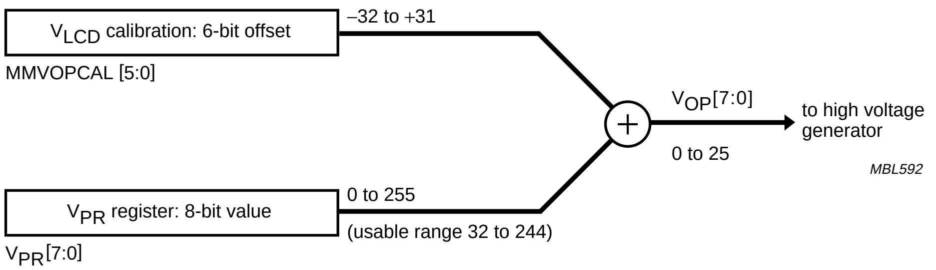


Fig.50 V_{LCD} calibration.

17.2 Factory defaults

In some instances it is desirable that the configuration is derived from OTP cells and not from user configurable registers. It is possible to pre-define the following features:

- Default temperature compensation slopes
- Default charge pump multiplication factor
- Default V_{PR} value
- Default bias system
- n-line inversion control.

The selection of the factory defaults mode is made by setting the factory default OTP cell, as shown in Table 29.

The operation can be thought of as a switch that selects between two sources for the data; see Fig.51. When the factory defaults are selected, changing the values via the interface is not possible (the register contents are updated, but have no effect).

Table 29 Factory default bit

DEFAULT BIT	ACTION
0	configuration data is taken from the interface
1	OTP values are used for configuration

17.2.1 DEFAULT TEMPERATURE SLOPE SELECTION

The values for SLA[2:0], SLB[2:0], SLC[2:0] and SLD[2:0] can be pre-defined.

17.2.2 DEFAULT CHARGE PUMP MULTIPLICATION FACTOR

The value for S[1:0] can be pre-defined.

17.2.3 DEFAULT V_{PR} VALUE

The value for V_{PR}[7:0] can be pre-defined.

17.2.4 DEFAULT BIAS VALUE

The value for BS[2:0] can be pre-defined.

17.3 Seal bit

The module maker programming is performed in a special mode: the calibration mode (CALMM). This mode is entered via a special interface command, CALMM. To prevent wrongful programming, a seal bit has been implemented which prevents the device from entering the calibration mode. This seal bit, once programmed, cannot be reversed, thus further changes in programmed values are not possible. Applying the programming voltages when not in CALMM mode will have no effect on the programmed values.

Table 30 Seal bit definition

SEAL BIT	ACTION
0	possible to enter calibration mode
1	calibration mode disabled

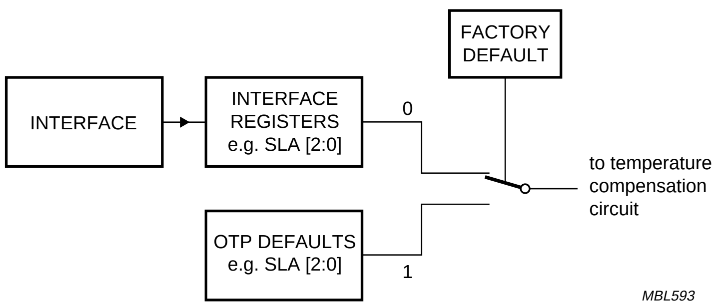


Fig.51 Factory defaults.

17.4 OTP architecture

The OTP circuitry in the PCF8814 contains many bits of data. The circuitry for 1 bit is called an OTP slice. Each OTP slice consists of 2 main parts: the OTP cell (a non-volatile memory cell) and the shift register cell (a flip-flop). The OTP cells are only accessible through their shift register cells: reading from and writing to the OTP cells is performed with the shift register cells, but only the shift register cells are visible to the rest of the circuit. The basic OTP architecture is shown in Fig.52.

The OTP architecture allows the following operations:

- Reading data from the OTP cells. The content of the non-volatile OTP cells is transferred to the shift register where upon it may affect the PCF8814 operation.
- Writing data to the OTP cells. First, all bits of data are shifted into the shift register via the interface. Then the content of the shift register is transferred to the OTP cells (there are some limitations related to storing data in these cells, see Section 17.7).
- Checking calibration without writing to the OTP cells. Shifting data into the shift register allows the effects on the V_{LCD} voltage to be observed.

The reading of data from the OTP cells is initiated by writing to the DON register. The OTP cells will not in fact be updated until the device leaves power-down and the oscillator starts. The reading operation needs up to 5 ms to complete.

The shifting of the data into the shift register is performed in the special mode CALMM. The CALMM mode is entered using the CALMM command. Once in the CALMM mode the data is shifted into the shift register via the interface at the rate of 1 bit per command. After transmitting the last bit and exiting the CALMM mode the serial interface is again in the normal mode and all other commands can be sent. Care should be taken that all bits of data (or a multiple of all bits) are transferred before exiting the CALMM mode, otherwise the bits will be in the wrong positions.

In the shift register the value of the seal bit is, like the others, always zero at reset. To make sure the security feature works correctly, the CALMM command is disabled until power-down has been left. Once a refresh is completed, the seal bit value in the shift register is valid and permission to enter CALMM mode can thus be determined.

The bits are shifted into the shift register in a pre-defined order which is shown in Table 31. For example, the seal bit is the last bit to be loaded into the shift register.

Table 31 OTP bit order.

POSITION	OTP CELL
1	MMVPR[7]
2	MMVPR[6]
3	MMVPR[5]
4	MMVPR[4]
5	MMVPR[3]
6	MMVPR[2]
7	MMVPR[1]
8	MMVPR[0]
9	MMSLD[2]
10	MMSLD[1]
11	MMSLD[0]
12	MMSLC[2]
13	MMSLC[1]
14	MMSLC[0]
15	MMSLB[2]
16	MMSLB[1]
17	MMSLB[0]
18	MMSLA[2]
19	MMSLA[1]
20	MMSLA[0]
21	MMS[1]
22	MMS[0]
23	MMBS[2]
24	MMBS[1]
25	MMBS[0]
26	FI
27	Factory defaults
28	MMVOPCAL[5]
29	MMVOPCAL[4]
30	MMVOPCAL[3]
31	MMVOPCAL[2]
32	MMVOPCAL[1]
33	MMVOPCAL[0]
34	SEAL

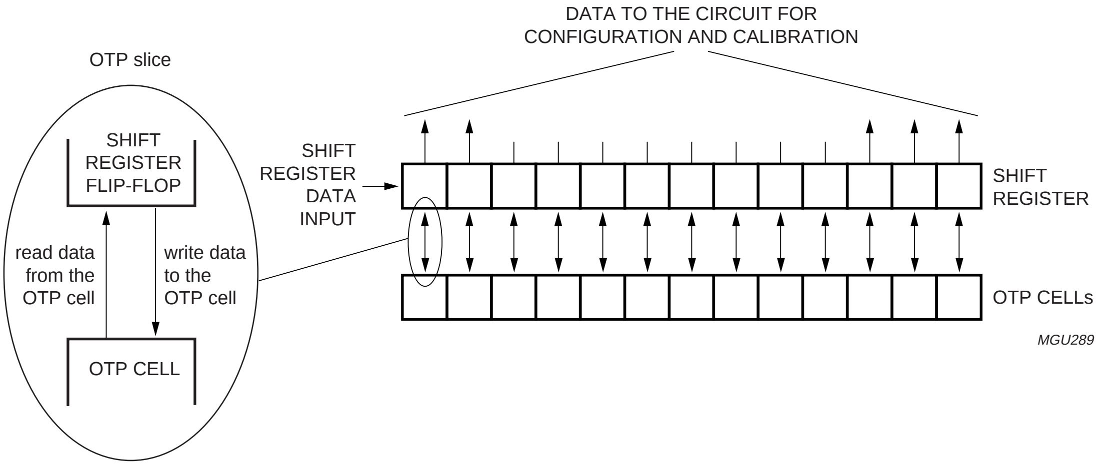


Fig.52 Basic OTP architecture.

17.5 Interface commands

Table 32 OTP instructions

NAME	D/$\overline{C}$	COMMAND BYTE								ACTION
		D7	D6	D5	D4	D3	D2	D1	D0	
OTP programming	0	1	1	1	1	0	0	OSE	CALMM	enter calibration mode and control programming
DON (refresh)	0	1	0	1	0	1	1	1	DON	display ON/OFF
Load 0	0	1	1	0	1	1	0	0	0	write 0 to shift register
Load 1	0	1	1	0	1	1	0	0	1	write 1 to shift register

17.5.1 CALMM

This instruction puts the device into the calibration mode. This mode enables the shift register for loading and allows programming of the non-volatile OTP cells to take place. If the seal bit is set, then this mode can not be accessed and the instruction will be ignored. Once in calibration mode, data may be loaded into the shift register via the ID1 and ID2 instructions (on the falling edge of SCLK).

The CALMM mode may be left by setting the CALMM bit to logic 0. Reset will also clear this mode.

The programming can only take place when OTP Switch Enable (OSE) has been set to logic 1. This enables the $V_{OTPPROG}$ input to be passed to the OTP cells. Since it is common for $V_{OTPPROG}$ to be tied to SCLH/SCE on the module, it is necessary to disconnect $V_{OTPPROG}$ from the OTP cells during normal operation. Reset will also clear this mode

17.5.2 REFRESH

The action of the Refresh instruction is to force the OTP shift register to re-load from the non-volatile OTP cells. This instruction takes up to 5 ms to complete. During this time all other instructions may be sent.

In the PCF8814 the Refresh instruction is associated with the DON instruction such that the shift register is automatically refreshed every time DON is enabled or disabled. Note however, that if this instruction is sent while in power-down mode, the DON bit will be updated but the refreshing is delayed until the device leaves power-down.

17.6 Example of filling the shift register

In Table 33 an example sequence of commands and data is shown. In this example the shift register is filled with the following data: MMVPR = 1101 0000, and the seal bit is logic 0.

It is assumed that the PCF8814 has just been reset. After transmitting the last bit the PCF8814 can exit or remain in CALMM mode (see step 1).

After this sequence has been applied it is possible to observe the impact of the data shifted in. The described sequence is however not useful for OTP programming because the number of bits with the value “1” is greater than that allowed for programming (see Section 17.7). Fig.53 shows the shift register after this action.

Table 33 Example sequence for filling the shift register

STEP	D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	ACTION
1	0	1	0	1	0	1	1	1	1	exit power-down
2										wait 5 ms for refresh to take effect
3	0	1	1	1	1	0	0	0	1	enter CALMM mode
4	0	1	1	0	1	1	0	0	1	shift in data, MMVPR[7] is first bit; see note 1
5	0	1	1	0	1	1	0	0	1	MMVPR[6]
6	0	1	1	0	1	1	0	0	0	MMVPR[5]
7	0	1	1	0	1	1	0	0	1	MMVPR[4]
8	0	1	1	0	1	1	0	0	0	MMVPR[3]
9	0	1	1	0	1	1	0	0	0	MMVPR[2]
:	:	:	:	:	:	:	:	:	:	:
36	0	1	1	0	1	1	0	0	1	MMVOPCAL[0]
37	0	1	1	0	1	1	0	0	0	seal bit
38	0	1	1	1	1	0	0	0	0	exit CALMM mode

Note

1. The data for the bits is not in the correct shift register position until all bits have been sent.

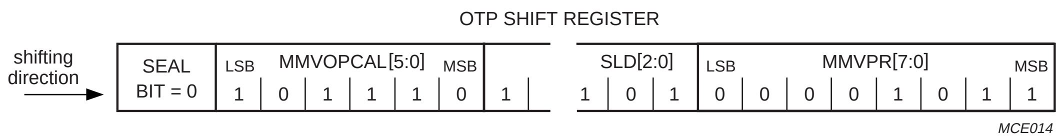


Fig.53 Shift register contents after example sequence of Table 33.

17.7 Programming flow

Programming is achieved whilst in CALMM mode and with the application of the programming voltages. As already stated, the data for programming the OTP cell is contained in the corresponding shift register cell. The shift register cell must be loaded with a logic 1 in order to program the corresponding OTP cell. If the shift register cell contains a logic 0, then no action will take place when the programming voltages are applied.

Once programmed, an OTP cell cannot be un-programmed. A programmed cell, that is an OTP cell containing a logic 1, must not be re-programmed.

During programming a substantial current flows in the V_{LCDIN} pad. For this reason, programming only one OTP cell at a time is recommended. This is achieved by filling all but one shift register cells with logic 0s.

Note that the programming specification refers to the voltages at the chip pads, contact resistance must therefore be considered by the user.

In Table 34 an example sequence of commands and data for OTP programming is shown.

The order for programming cells is not significant, however, it is recommended that the seal bit is programmed last. Once this bit has been programmed it will not be possible to re-enter the CALMM mode.

Prior to the sequence specified in Table 34, it is assumed that the PCF8814 has just been reset.

Table 34 Sequence for OTP programming

STEP	$D/\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	ACTION
1	0	1	0	1	0	1	1	1	1	exit power-down (DON = 1)
2										wait 5 ms for refresh to take effect
3	0	1	1	1	1	0	0	1	1	enter CALMM mode and OSE
4	0	1	1	0	1	1	0	0	1	shift in data. MMVPR[7] is first bit, see note 1
5	0	1	1	0	1	1	0	0	0	MMVPR[6]
6	0	1	1	0	1	1	0	0	0	MMVPR[5]
7	0	1	1	0	1	1	0	0	0	MMVPR[4]
7	0	1	1	0	1	1	0	0	0	MMVPR[3]
9	0	1	1	0	1	1	0	0	0	MMVPR[2]
:	:	:	:	:	:	:	:	:	:	
36	0	1	1	0	1	1	0	0	0	MMVOPCAL[0]
37	0	1	1	0	1	1	0	1	0	seal bit
38										apply programming voltage at pads $V_{OTPPROG}$ and V_{LCDIN}, as specified in according to Section 17.8
Repeat steps 5 to 38 for each bit that should be programmed to logic 1.										
39										apply external reset or exit CALMM

Note

1. The data for the bits is not in the correct shift register position until all the bits have been sent.

17.8 PROGRAMMING SPECIFICATION

Table 35 Programming specification (refer to Fig.54). V_{DD1} = 2.5 V is recommended for programming.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$V_{OTPPROG}$	voltage applied to $V_{OTPPROG}$	with respect to V_{SS1}; note 1				
		programming active	11.0	11.5	12.0	V
		programming inactive	V_{SS} – 0.2	0	0.2	V
V_{LCDIN}	voltage applied to V_{LCDIN}	with respect to V_{SS1}; notes 1 and 2				
		programming active	9.0	9.5	10.0	V
		programming inactive	V_{DD2} – 0.2	V_{DD2}	4.5	V
I_{LCDIN}	current drawn by V_{LCDIN} during programming	when programming a single bit to logic 1	–	850	1000	µA
$I_{VOTPPROG}$	current drawn by $V_{OTPPROG}$ during programming		–	100	200	µA
$t_{su(SCLK)}$	set-up time of internal data after last clock		1	–	–	µs
$t_{hd(SCLK)}$	hold time of internal data before next clock		1	–	–	µs
$t_{su(gate)}$	set-up of $V_{OTPPROG}$ prior to programming		1	–	10	ms
$t_{hd(gate)}$	hold of $V_{OTPPROG}$ after programming		1	–	10	ms
t_{PW}	pulse width of programming voltage		100	120	200	ms
T_{prog}	ambient temperature during programming		0	+25	+40	°C

Notes

1. The voltage drop across the ITO track and any connector must be taken into account to guarantee a sufficient high voltage at the chip pads.
2. The Power-down mode (DON = 0, DAL = 1) and CALMM mode must be active while the V_{LCDIN} pad is being driven.

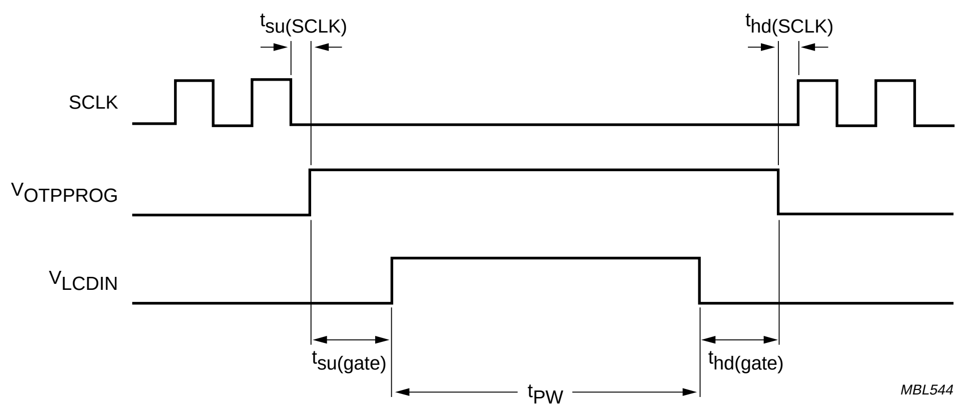


Fig.54 Programming waveforms.

18 CHIP INFORMATION

The PCF8814 is manufactured in n-well CMOS technology.

The substrate is at V_{SS} potential.

Table 36 Bonding pad information

PARAMETER	ROWS/COLS SIDE	INTERFACE SIDE	UNIT
Pad pitch	51.84 (min)	63 (min)	µm
Bump dimensions	30.04 x 99.00 15.0 (±3)	39.94 x 90.00 15.0 (±3)	µm
Wafer thickness (excl. bumps)	381 (±25)		µm

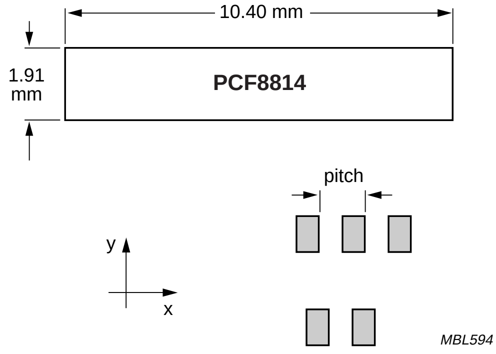
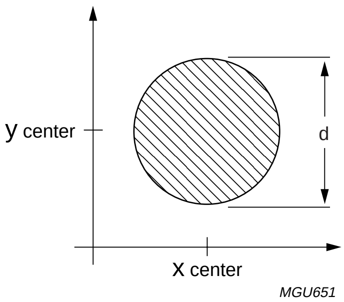
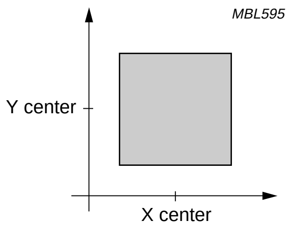


Fig.55 Chip size and pad pitch.



d = 90 µm

Fig.56 Shape of alignment mark.



60 µm square

Fig.57 Shape of bump alignment mark.

Table 37 Pad coordinates X and Y in µm, indicate pad centre and are referenced to the centre of the chip (see Fig.58)

NO.	PAD NAME	X	Y
1	dummy	–5058.0	814.5
2	dummy	–4995.0	814.5
3	dummy	–4932.0	814.5
4	dummy	–4725.0	814.5
5	V_{LCDIN}	–4626.0	814.5
6	V_{LCDIN}	–4563.0	814.5
7	V_{LCDIN}	–4500.0	814.5
8	V_{LCDIN}	–4437.0	814.5
9	V_{LCDOUT}	–4365.0	814.5
10	V_{LCDOUT}	–4302.0	814.5
11	V_{LCDOUT}	–4239.0	814.5
12	V_{LCDOUT}	–4176.0	814.5
13	V_{LCDOUT}	–4113.0	814.5
14	V_{LCDOUT}	–4050.0	814.5
15	V_{LCDOUT}	–3987.0	814.5
16	$V_{LCDSENSE}$	–3924.0	814.5
17	dummy	–3843.0	814.5
18	dummy	–3780.0	814.5
19	dummy	–3717.0	814.5
20	dummy	–3654.0	814.5
21	dummy	–3591.0	814.5
22	T3	–3510.0	814.5
23	T4	–3348.0	814.5
24	T1	–3258.0	814.5
25	T2	–3141.0	814.5
26	T5	–3024.0	814.5
27	T6	–2907.0	814.5
28	V_{DD3}	–2799.0	814.5
29	V_{DD3}	–2736.0	814.5
30	V_{DD3}	–2673.0	814.5
31	V_{DD2}	–2529.0	814.5
32	V_{DD2}	–2466.0	814.5
33	V_{DD2}	–2403.0	814.5
34	V_{DD2}	–2340.0	814.5
35	V_{DD2}	–2277.0	814.5
36	V_{DD2}	–2214.0	814.5
37	V_{DD2}	–2151.0	814.5
38	V_{DD2}	–2088.0	814.5
39	V_{DD2}	–2025.0	814.5
40	V_{DD2}	–1962.0	814.5
41	V_{DD1}	–1836.0	814.5
42	V_{DD1}	–1773.0	814.5
43	V_{DD1}	–1710.0	814.5
44	V_{DD1}	–1647.0	814.5
45	V_{DD1}	–1584.0	814.5
46	V_{DD1}	–1521.0	814.5
47	SCLK	–1422.0	814.5
48	ID3/SA0	–1305.0	814.5
49	ID4/SA1	–1188.0	814.5
50	OSC	–1071.0	814.5
51	SDO	–819.0	814.5
52	dummy	–720.0	814.5
53	dummy	–657.0	814.5
54	dummy	–594.0	814.5
55	dummy	–531.0	814.5
56	dummy	–468.0	814.5
57	dummy	–405.0	814.5
58	dummy	–342.0	814.5
59	dummy	–279.0	814.5
60	dummy	–216.0	814.5
61	dummy	–153.0	814.5
62	dummy	–90.0	814.5
63	dummy	–27.0	814.5
64	dummy	36.0	814.5
65	dummy	99.0	814.5
66	SDAHOUT	198.0	814.5
67	SDAH	306.0	814.5
68	dummy	405.0	814.5
69	dummy	468.0	814.5
70	dummy	531.0	814.5
71	dummy	594.0	814.5
72	dummy	657.0	814.5
73	dummy	720.0	814.5
74	dummy	783.0	814.5
75	dummy	846.0	814.5
76	dummy	909.0	814.5
77	dummy	972.0	814.5
78	dummy	1035.0	814.5
79	dummy	1098.0	814.5

NO.	PAD NAME	X	Y
80	dummy	1161.0	814.5
81	dummy	1224.0	814.5
82	SDIN	1323.0	814.5
83	V_{SS2}	1413.0	814.5
84	V_{SS2}	1476.0	814.5
85	V_{SS2}	1539.0	814.5
86	V_{SS2}	1602.0	814.5
87	V_{SS2}	1665.0	814.5
88	V_{SS2}	1728.0	814.5
89	V_{SS2}	1791.0	814.5
90	V_{SS1}	1854.0	814.5
91	V_{SS1}	1917.0	814.5
92	V_{SS1}	1980.0	814.5
93	V_{SS1}	2043.0	814.5
94	V_{SS1}	2106.0	814.5
95	V_{SS1}	2169.0	814.5
96	$V_{OTPPROG}$	2259.0	814.5
97	$V_{OTPPROG}$	2322.0	814.5
98	$V_{OTPPROG}$	2385.0	814.5
99	dummy	2484.0	814.5
100	dummy	2547.0	814.5
101	dummy	2610.0	814.5
102	dummy	2673.0	814.5
103	dummy	2736.0	814.5
104	dummy	2799.0	814.5
105	dummy	2862.0	814.5
106	dummy	2925.0	814.5
107	dummy	2988.0	814.5
108	dummy	3051.0	814.5
109	dummy	3114.0	814.5
110	dummy	3177.0	814.5
111	dummy	3240.0	814.5
112	dummy	3303.0	814.5
113	SCLH/$\overline{SCE}$	3411.0	814.5
114	D/$\overline{C}$	3564.0	814.5
115	PS1	3699.0	814.5
116	$V_{DD(tie-off)}$	3816.0	814.5
117	PS0	3951.0	814.5
118	MX	4086.0	814.5
119	dummy	4194.0	814.5
120	dummy	4257.0	814.5

NO.	PAD NAME	X	Y
121	$\overline{RES}$	4356.0	814.5
122	dummy	4437.0	814.5
123	dummy	4500.0	814.5
124	dummy	4563.0	814.5
125	dummy	4626.0	814.5
126	dummy	4689.0	814.5
127	dummy	4752.0	814.5
128	dummy	4815.0	814.5
129	dummy	5054.7	–810.0
130	dummy	5002.9	–810.0
131	dummy	4951.1	–810.0
132	dummy	4899.2	–810.0
133	dummy	4847.4	–810.0
134	dummy	4795.6	–810.0
135	dummy	4743.7	–810.0
136	dummy	4691.9	–810.0
137	dummy	4640.0	–810.0
138	dummy	4588.2	–810.0
139	dummy	4536.4	–810.0
140	dummy	4484.5	–810.0
141	dummy	4432.7	–810.0
142	dummy	4380.8	–810.0
143	dummy	4329.0	–810.0
144	dummy	4277.2	–810.0
145	dummy	4225.3	–810.0
146	dummy	4173.5	–810.0
147	dummy	4121.6	–810.0
148	vc_pad	4069.8	–810.0
149	R32	4011.3	–810.0
150	R33	3959.5	–810.0
151	R34	3907.6	–810.0
152	R35	3855.8	–810.0
153	R36	3803.9	–810.0
154	R37	3752.1	–810.0
155	R38	3700.3	–810.0
156	R39	3648.4	–810.0
157	R40	3596.6	–810.0
158	R41	3544.7	–810.0
159	R42	3492.9	–810.0
160	R43	3441.1	–810.0
161	R44	3389.2	–810.0

NO.	PAD NAME	X	Y
162	R45	3337.4	–810.0
163	R46	3285.5	–810.0
164	R47	3233.7	–810.0
165	R48	3181.9	–810.0
166	R49	3130.0	–810.0
167	R50	3078.2	–810.0
168	R51	3026.3	–810.0
169	R52	2974.5	–810.0
170	R53	2922.7	–810.0
171	R54	2870.8	–810.0
172	R55	2819.0	–810.0
173	R56	2767.1	–810.0
174	R57	2715.3	–810.0
175	R58	2663.5	–810.0
176	R59	2611.6	–810.0
177	R60	2559.8	–810.0
178	R61	2507.9	–810.0
179	R62	2456.1	–810.0
180	R63	2404.3	–810.0
181	R64	2352.4	–810.0
182	v1l_pad	2293.9	–810.0
183	C95	2144.3	–810.0
184	C94	2092.5	–810.0
185	C93	2040.7	–810.0
186	C92	1988.8	–810.0
187	C91	1937.0	–810.0
188	C90	1885.1	–810.0
189	C89	1833.3	–810.0
190	C88	1781.5	–810.0
191	C87	1729.6	–810.0
192	C86	1677.8	–810.0
193	C85	1625.9	–810.0
194	C84	1574.1	–810.0
195	C83	1522.3	–810.0
196	C82	1470.4	–810.0
197	C81	1418.6	–810.0
198	C80	1366.7	–810.0
199	C79	1314.9	–810.0
200	C78	1263.1	–810.0
201	C77	1211.2	–810.0
202	C76	1159.4	–810.0

NO.	PAD NAME	X	Y
203	C75	1107.5	–810.0
204	C74	1055.7	–810.0
205	C73	1003.9	–810.0
206	C72	952.0	–810.0
207	C71	848.3	–810.0
208	C70	796.5	–810.0
209	C69	744.7	–810.0
210	C68	692.8	–810.0
211	C67	641.0	–810.0
212	C66	589.1	–810.0
213	C65	537.3	–810.0
214	C64	485.5	–810.0
215	C63	433.6	–810.0
216	C62	381.8	–810.0
217	C61	329.9	–810.0
218	C60	278.1	–810.0
219	C59	226.3	–810.0
220	C58	174.4	–810.0
221	C57	122.6	–810.0
222	C56	70.7	–810.0
223	C55	18.9	–810.0
224	C54	–32.9	–810.0
225	C53	–84.8	–810.0
226	C52	–136.6	–810.0
227	C51	–188.5	–810.0
228	C50	–240.3	–810.0
229	C49	–292.1	–810.0
230	C48	–344.0	–810.0
231	dummy	–447.7	–810.0
232	C47	–499.5	–810.0
233	C46	–551.3	–810.0
234	C45	–603.2	–810.0
235	C44	–655.0	–810.0
236	C43	–706.9	–810.0
237	C42	–758.7	–810.0
238	C41	–810.5	–810.0
239	C40	–862.4	–810.0
240	C39	–914.2	–810.0
241	C38	–966.1	–810.0
242	C37	–1017.9	–810.0
243	C36	–1069.7	–810.0

NO.	PAD NAME	X	Y
244	C35	–1121.6	–810.0
245	C34	–1173.4	–810.0
246	C33	–1225.3	–810.0
247	C32	–1277.1	–810.0
248	C31	–1328.9	–810.0
249	C30	–1380.8	–810.0
250	C29	–1432.6	–810.0
251	C28	–1484.5	–810.0
252	C27	–1536.3	–810.0
253	C26	–1588.1	–810.0
254	C25	–1640.0	–810.0
255	C24	–1691.8	–810.0
256	C23	–1795.5	–810.0
257	C22	–1847.3	–810.0
258	C21	–1899.2	–810.0
259	C20	–1951.0	–810.0
260	C19	–2002.9	–810.0
261	C18	–2054.7	–810.0
262	C17	–2106.5	–810.0
263	C16	–2158.4	–810.0
264	C15	–2210.2	–810.0
265	C14	–2262.1	–810.0
266	C13	–2313.9	–810.0
267	C12	–2365.7	–810.0
268	C11	–2417.6	–810.0
269	C10	–2469.4	–810.0
270	C9	–2521.3	–810.0
271	C8	–2573.1	–810.0
272	C7	–2624.9	–810.0
273	C6	–2676.8	–810.0
274	C5	–2728.6	–810.0
275	C4	–2780.5	–810.0
276	C3	–2832.3	–810.0
277	C2	–2884.1	–810.0
278	C1	–2936.0	–810.0
279	C0	–2987.8	–810.0
280	dummy	–3039.7	–810.0
281	dummy	–3091.5	–810.0
282	v1h_pad	–3188.5	–810.0
283	R31	–3247.0	–810.0
284	R30	–3298.9	–810.0

NO.	PAD NAME	X	Y
285	R29	–3350.7	–810.0
286	R28	–3402.5	–810.0
287	R27	–3454.4	–810.0
288	R26	–3506.2	–810.0
289	R25	–3558.1	–810.0
290	R24	–3609.9	–810.0
291	R23	–3661.7	–810.0
292	R22	–3713.6	–810.0
293	R21	–3765.4	–810.0
294	R20	–3817.3	–810.0
295	R19	–3869.1	–810.0
296	R18	–3920.9	–810.0
297	R17	–3972.8	–810.0
298	R16	–4024.6	–810.0
299	R15	–4076.5	–810.0
300	R14	–4128.3	–810.0
301	R13	–4180.1	–810.0
302	R12	–4232.0	–810.0
303	R11	–4283.8	–810.0
304	R10	–4335.7	–810.0
305	R9	–4387.5	–810.0
306	R8	–4439.3	–810.0
307	R7	–4491.2	–810.0
308	R6	–4543.0	–810.0
309	R5	–4594.9	–810.0
310	R4	–4646.7	–810.0
311	R3	–4698.5	–810.0
312	R2	–4750.4	–810.0
313	R1	–4802.2	–810.0
314	R0	–4854.1	–810.0
315	dummy	–4905.9	–810.0
316	dummy	–4957.7	–810.0
317	dummy	–5009.6	–810.0
318	dummy	–5061.4	–810.0
Recognition mark, left		–4830.8	756.0
Recognition mark, right		4934.5	756.0
Bump alignment mark		5037.4	793.9
Top right corner		5200.0	955.0
Bottom left corner		–5200.0	–955.0

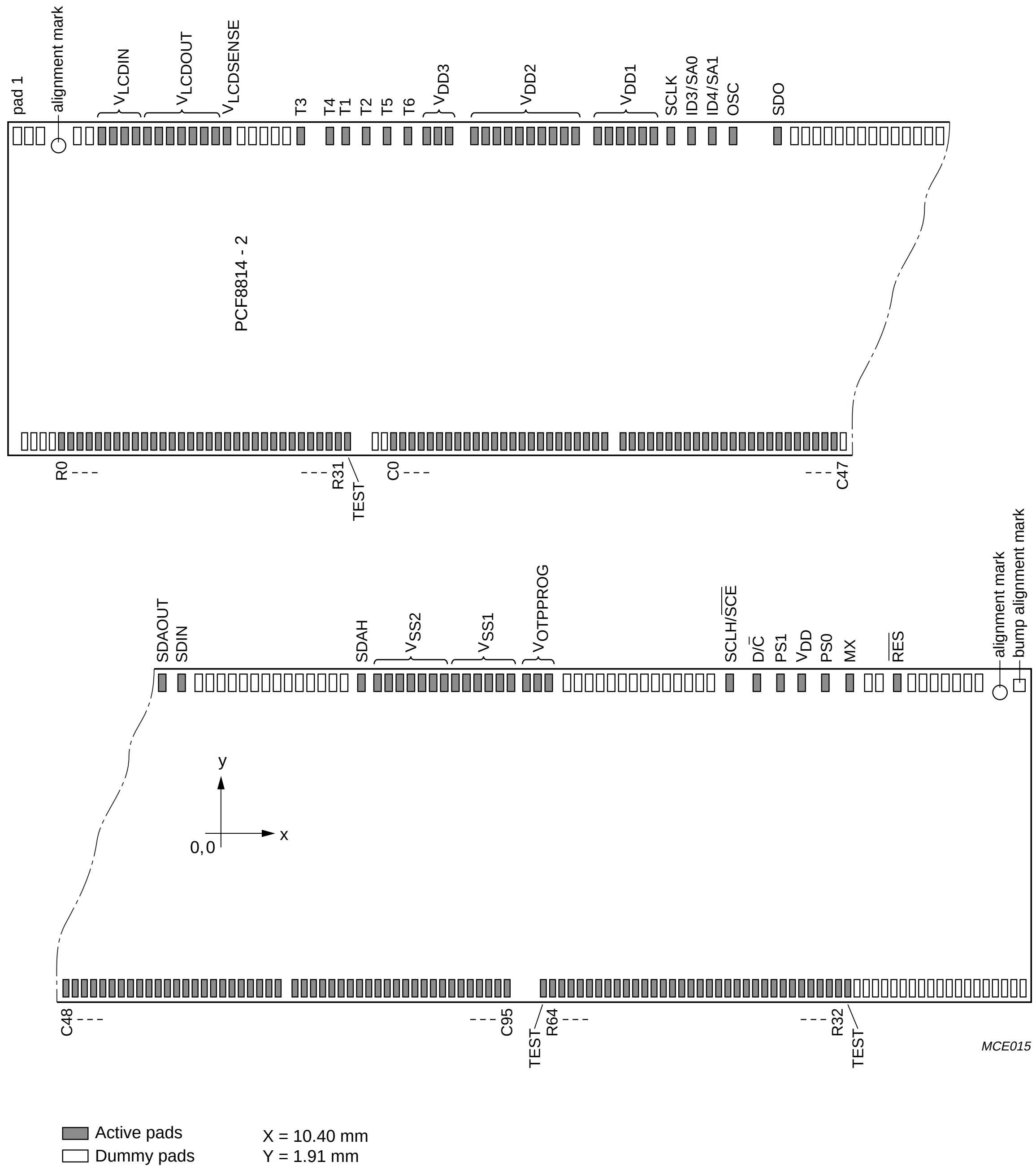
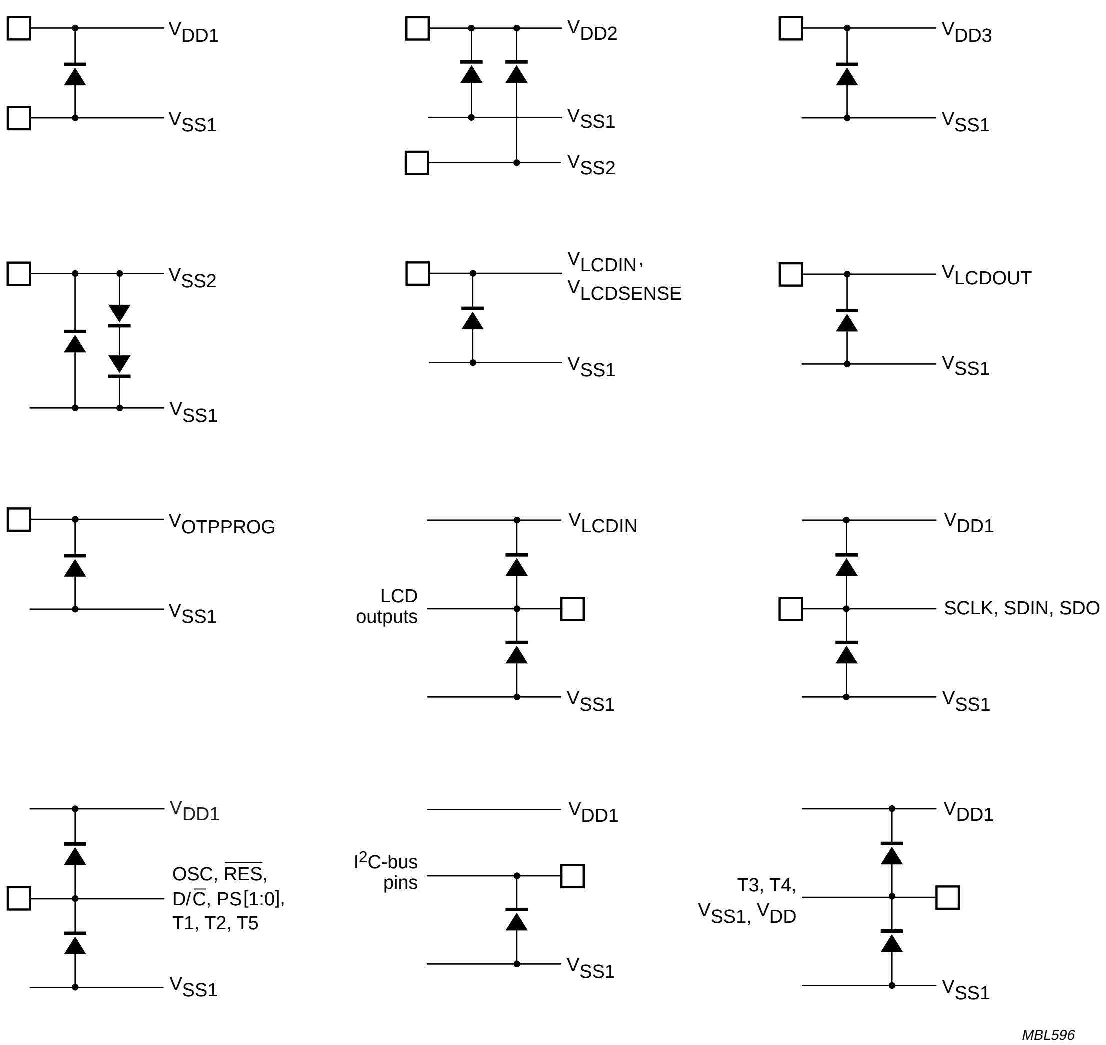


Fig.58 Bonding pad location (viewed from bump side).

19 INTERNAL PROTECTION CIRCUITS



For test purposes only: maximum forward current = 5 mA.

Fig.59 ESD structures

20 TRAY INFORMATION

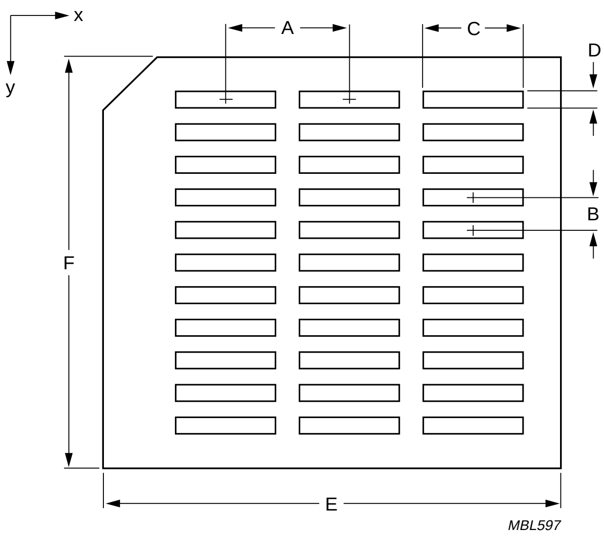
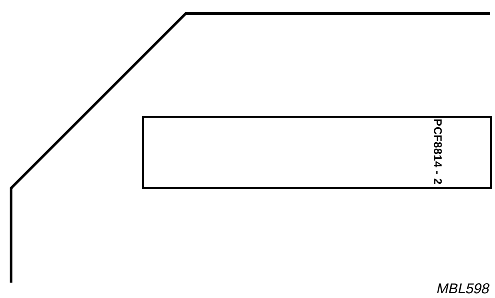


Fig.60 Tray details.

Table 38 Tray dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	14.02 mm
B	pocket pitch, y direction	3.99 mm
C	pocket width, x direction	10.50 mm
D	pocket width, y direction	2.01 mm
E	tray width, x direction	50.80 mm
F	tray width, y direction	50.80 mm
–	pockets in x direction	3
–	pockets in y direction	11



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the die surface.

Fig.61 Tray alignment.

21 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

22 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

23 DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Bare die — All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of Philips' delivery. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post packing tests performed on individual die or wafer. Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

24 PURCHASE OF PHILIPS I^2C COMPONENTS

Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA75

Printed in The Netherlands 403512/01/pp72 Date of release: 2003 Mar 13 Document order number: 9397 750 09664