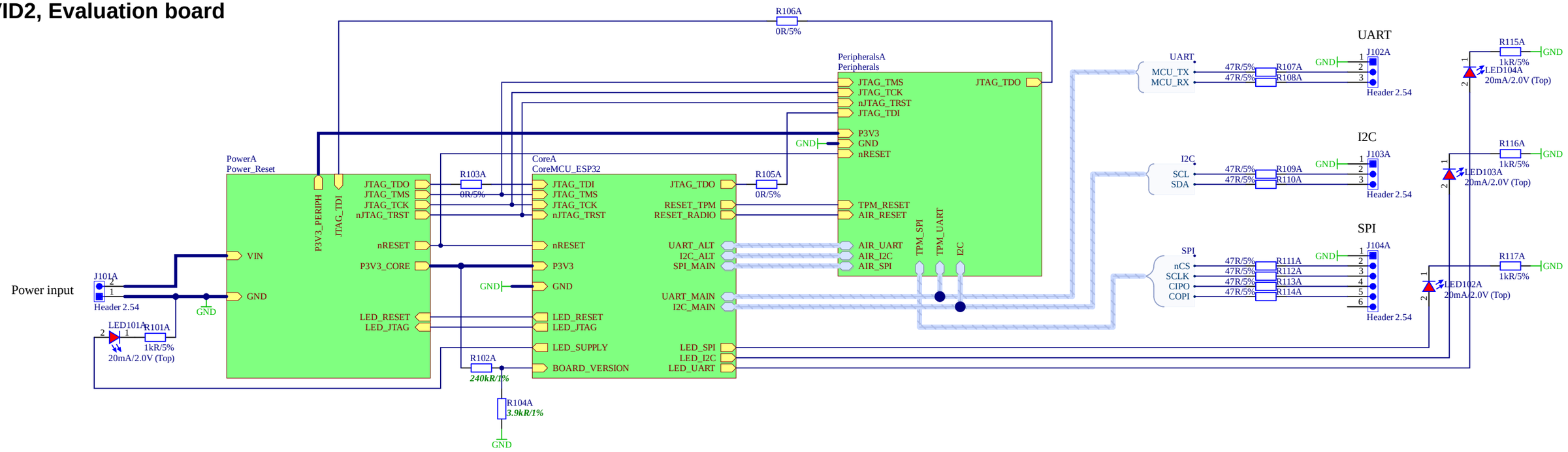
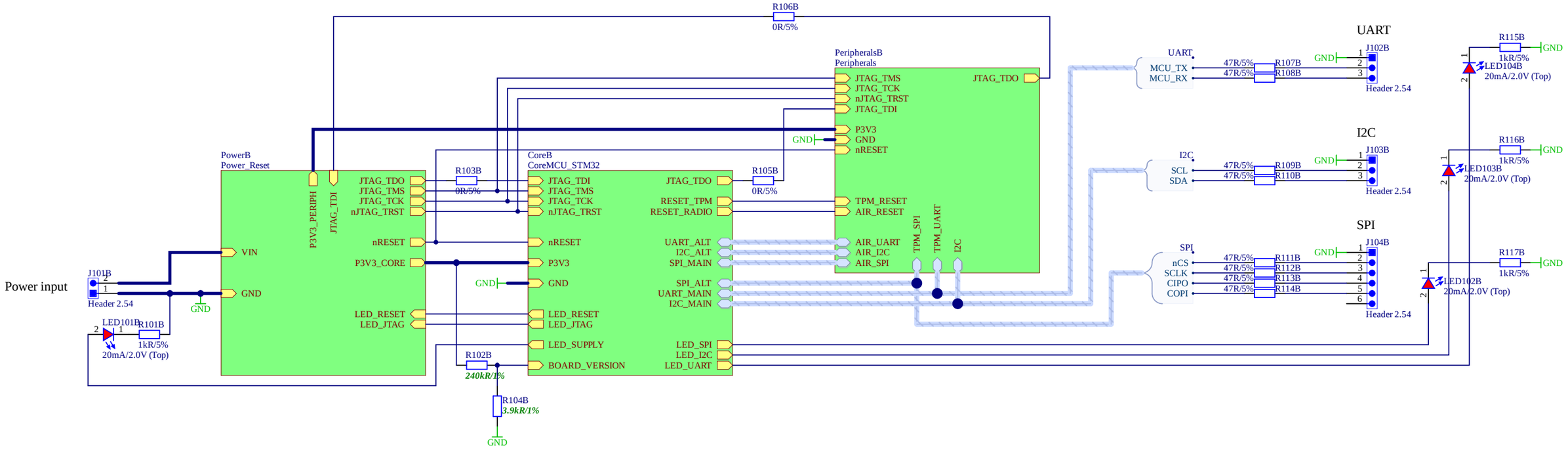
DVID2, Evaluation board



Subsystem A

The two subsystems are electrically independent, except for the shared GND.

Subsystem B

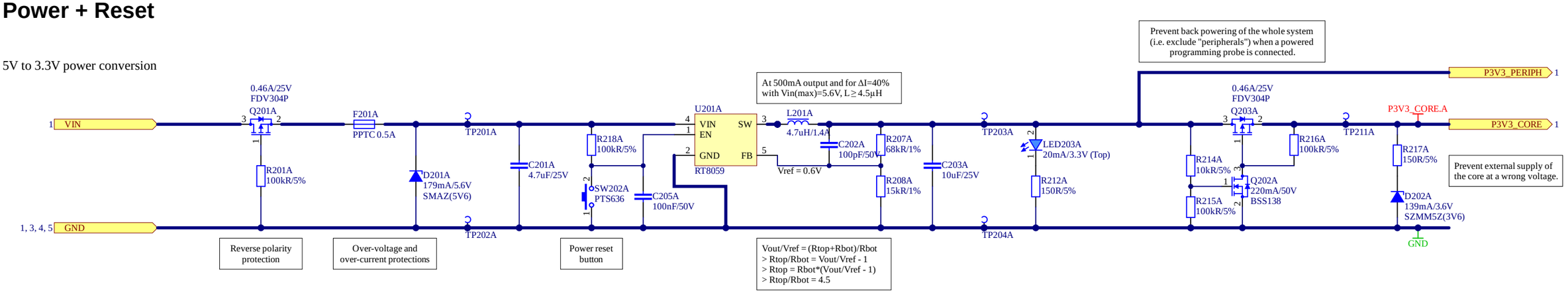


zentek	DVID2_EVB Name of the board (or project)		A Rev. no.	1 BOM no.
	DVID2_EVB.SchDoc Page title (file name)			08/11/2024 Date (D/M/YYYY)
	- Document number	Justin MASSIOT Drawn by	Arnaud COURTY Approved by	1 of 7 Page number

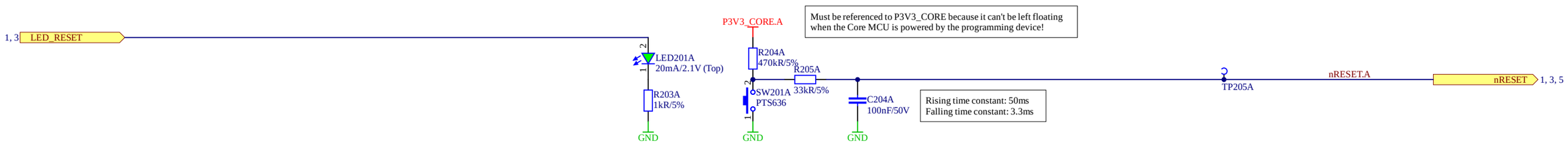
54 56 10/11/2024

Power + Reset

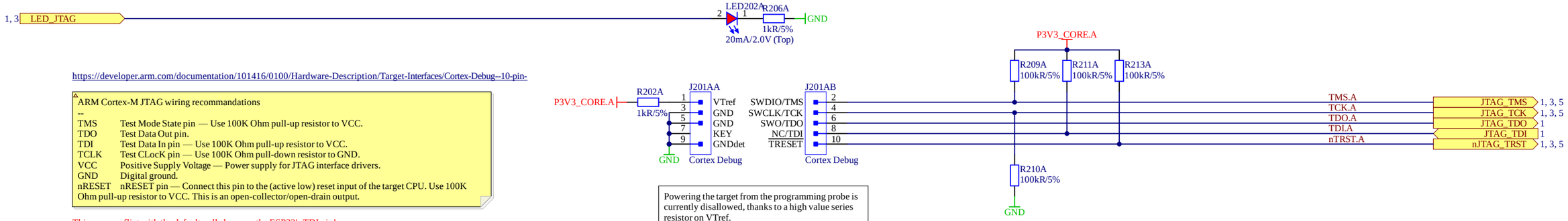
5V to 3.3V power conversion



General Reset control



JTAG prog. connector



https://developer.arm.com/documentation/101416/0100/Hardware-Description/Target-Interfaces/Cortex-Debug--10-pin-

ARM Cortex-M JTAG wiring recommandations
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TMS	Test Mode State pin — Use 100K Ohm pull-up resistor to VCC.
TDO	Test Data Out pin.
TDI	Test Data In pin — Use 100K Ohm pull-up resistor to VCC.
TCLK	Test CLocK pin — Use 100K Ohm pull-down resistor to GND.
VCC	Positive Supply Voltage — Power supply for JTAG interface drivers.
GND	Digital ground.
nRESET	nRESET pin — Connect this pin to the (active low) reset input of the target CPU. Use 100K Ohm pull-up resistor to VCC. This is an open-collector/open-drain output.

This may conflict with the default pull-down on the ESP32's TDI pin!

Powering the target from the programming probe is currently disallowed, thanks to a high value series resistor on VTref.

A 0R resistor could be used instead, resulting in powering only the target core thanks to our "no back power" circuit. BE CAREFUL: In such case, some targets on the JTAG chain may not be powered up!

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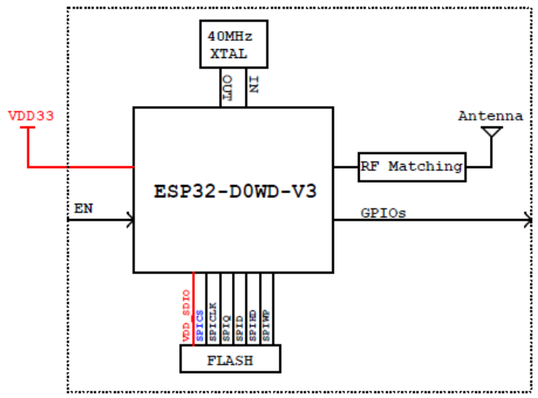
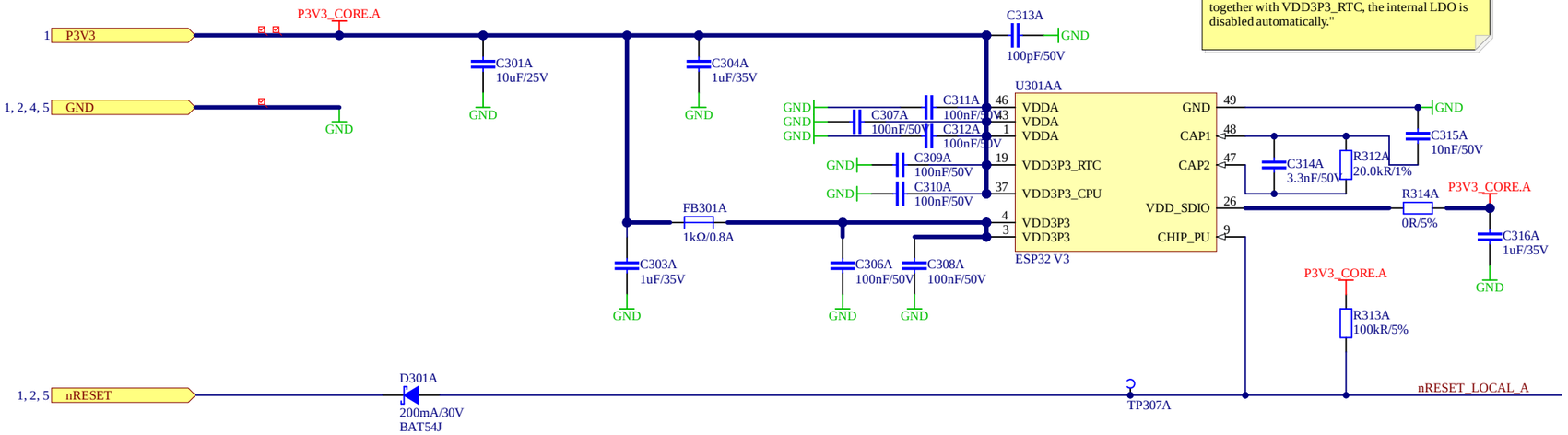
48 56 10/11/2024

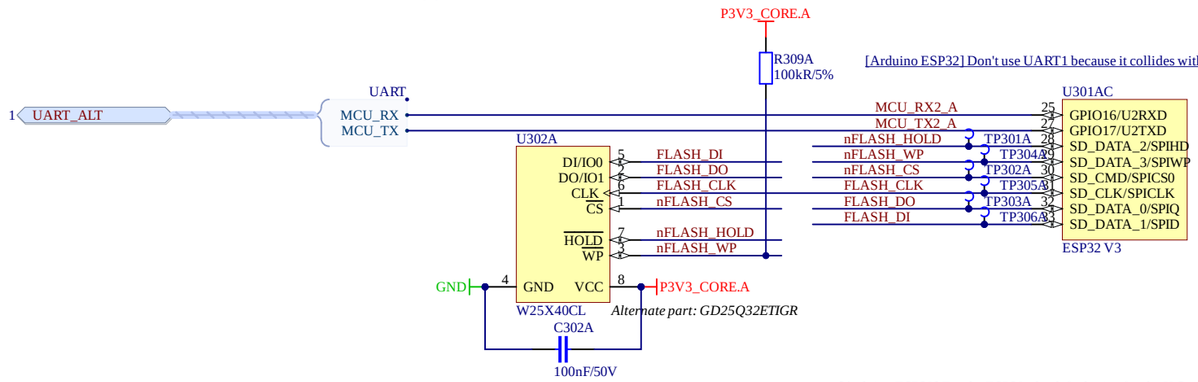
ESP32 core

VDD_SDIO can be an output, but we don't use it as such:
"VDD_SDIO connects to the output of an internal LDO whose input is VDD3P3_RTC. When VDD_SDIO is connected to the same PCB net together with VDD3P3_RTC, the internal LDO is disabled automatically."

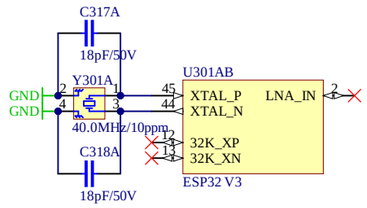
Diagram of a minimal system featuring an ESP32 (external Flash)





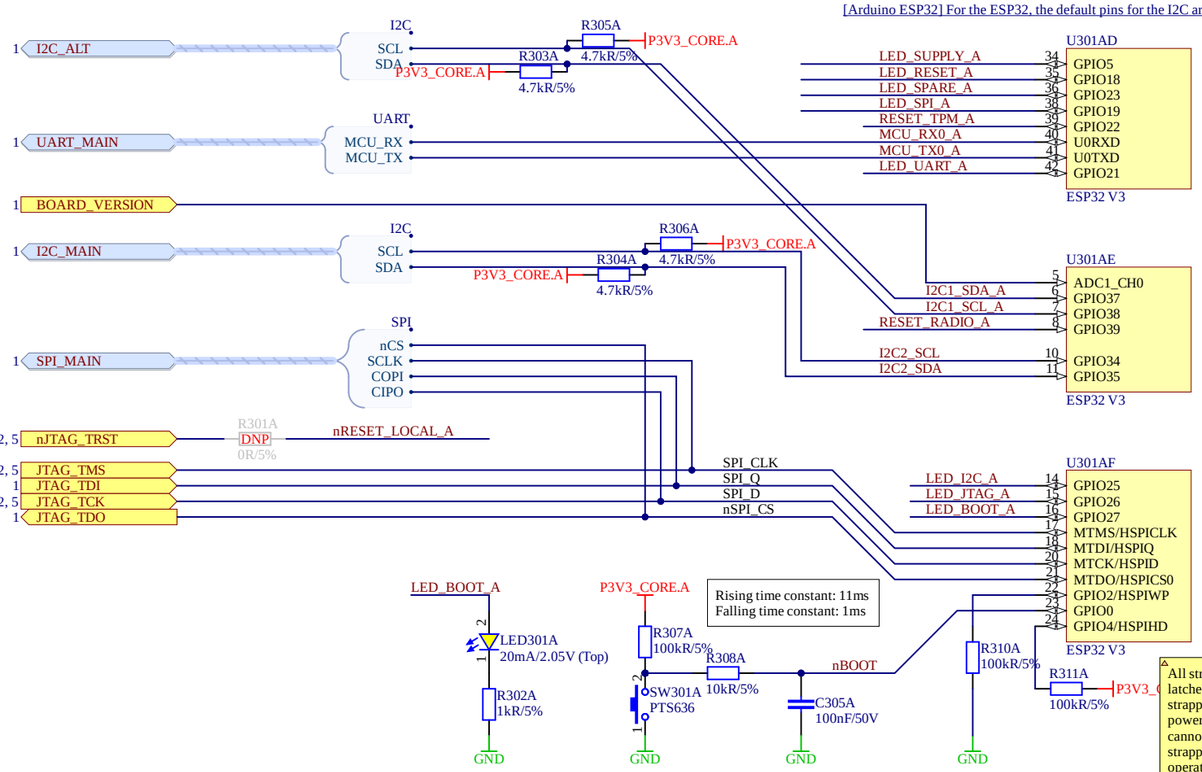


Chip Pin	Off-Package Flash
SD_DATA_1/SPID	IO0/DI
SD_DATA_0/SPIQ	IO1/DO
SD_DATA_3/SPIWP	IO2/WP#
SD_DATA_2/SPIHD	IO3/HOLD#
SD_CLK	CLK
SD_CMD	CS#
GND	VSS
VDD_SDIO	VDD



Alternate part: ABM11AIG-40.000MHZ-4Z-T3
Alternate part: XRCGB40M000F1S1CR0

[Arduino ESP32] For the ESP32, the default pins for the I2C are SDA (GPIO21) and SCL (GPIO22).



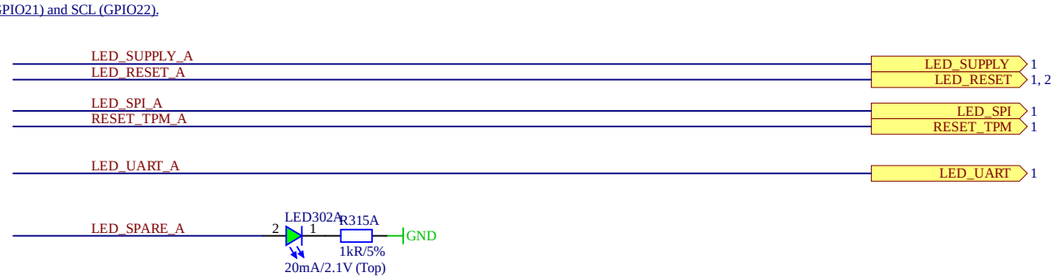


Table 3-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Pull-up	1
GPIO2	Pull-down	0
MTDI	Pull-down	0
MTDO	Pull-up	1
GPIO5	Pull-up	1

Table 3-3. Chip Boot Mode Control

Boot Mode	GPIO0	GPIO2
SPI Boot Mode	1	Any value
Joint Download Boot Mode [2]	0	0

[1] **Bold** marks the default value and configuration.
[2] Joint Download Boot mode supports the following download methods:
- SDIO Download Boot
- UART Download Boot

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

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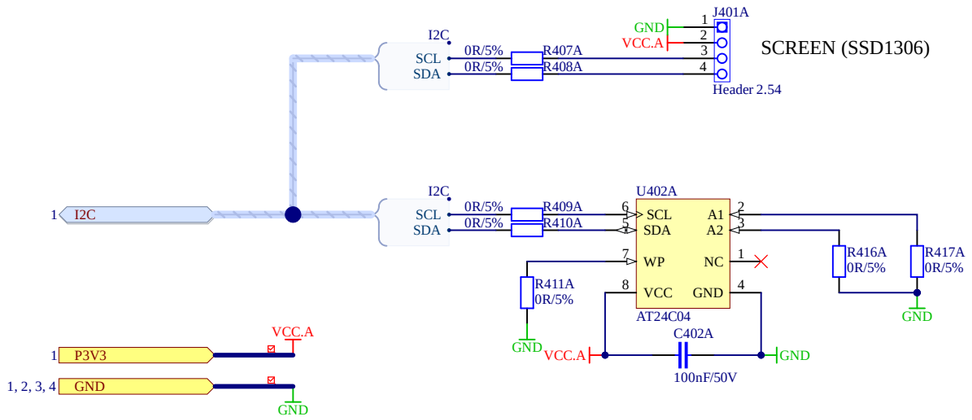
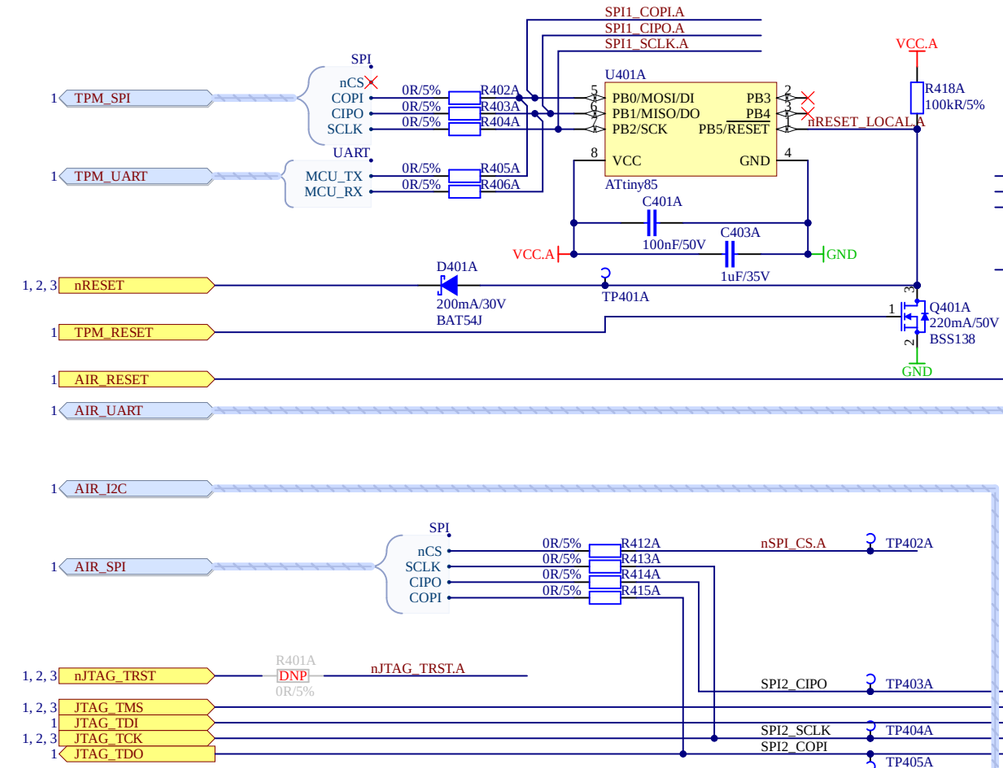
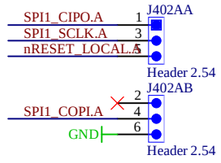
55 56 10/11/2024

Peripherals

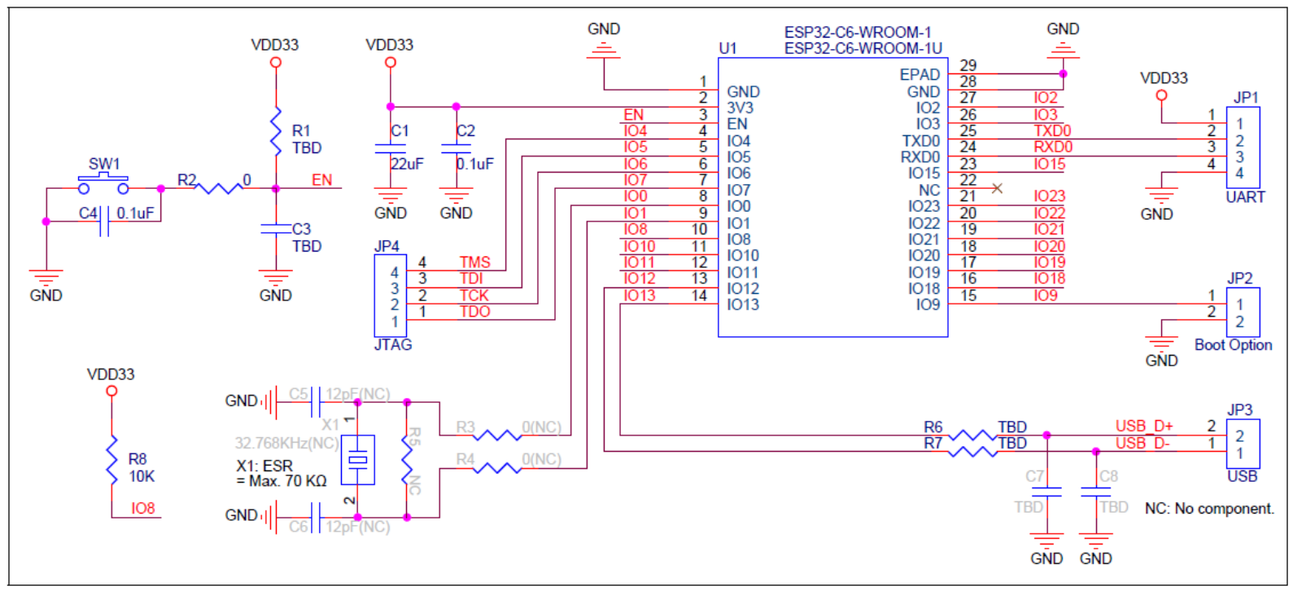






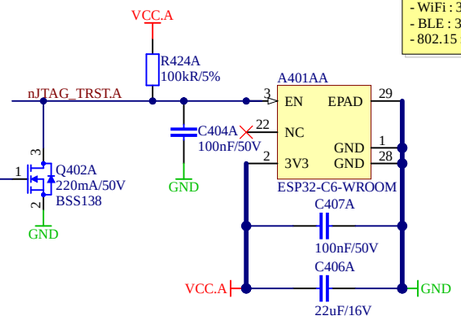
ATtiny ISP prog.

Powering the target through this connector is currently disallowed (VCC not wired).



Typical ESP32-C6-WROOM usage

Maximum current consumption:
- WiFi : 382mA ; transmission (802.11b, 1 Mbps, DSSS @ 20.5 dBm)
- BLE : 309mA ; transmission (LE @ 19.0 dBm)
- 802.15 : 302mA ; transmission (802.15.4 @ 19.0 dBm)



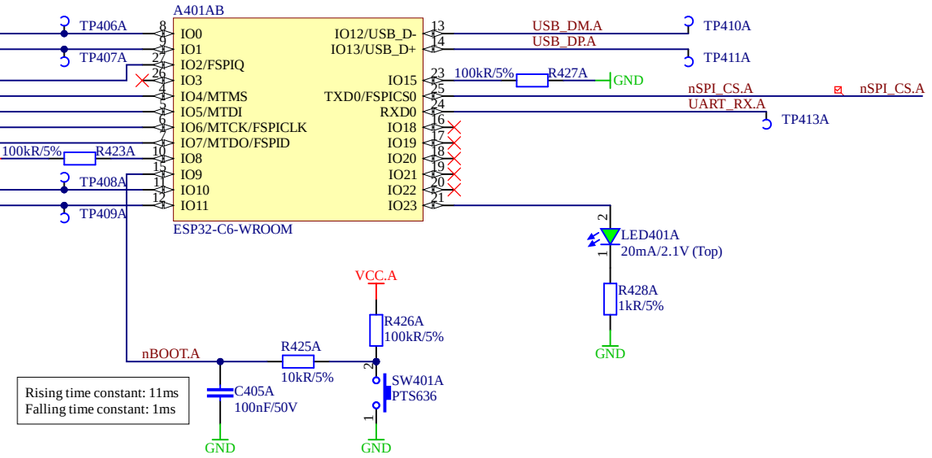


Table 9: JTAG Signal Source Control

eFuse 1[a]	eFuse 2[b]	eFuse 3[c]	GPIO15	JTAG Signal Source
0	0	0	Ignored	USB Serial/JTAG Controller
		1	0	JTAG pins MTDI, MTCK, MTMS, and MTDO
			1	USB Serial/JTAG Controller
0	1	Ignored	Ignored	JTAG pins MTDI, MTCK, MTMS, and MTDO
1	0	Ignored	Ignored	USB Serial/JTAG Controller
1	1	Ignored	Ignored	JTAG is disabled

[a] eFuse 1: EFUSE_DIS_PAD_JTAG
[b] eFuse 2: EFUSE_DIS_USB_JTAG
[c] eFuse 3: EFUSE_JTAG_SEL_ENABLE

Table 7: Boot Mode Control

Boot Mode	GPIO8	GPIO9
Default Configuration	– (Floating)	1 (Pull-up)
SPI Boot (default)	Any value	1
Download Boot	1	0
Invalid combination[1]	0	0

[1] This combination triggers unexpected behavior and should be avoided.

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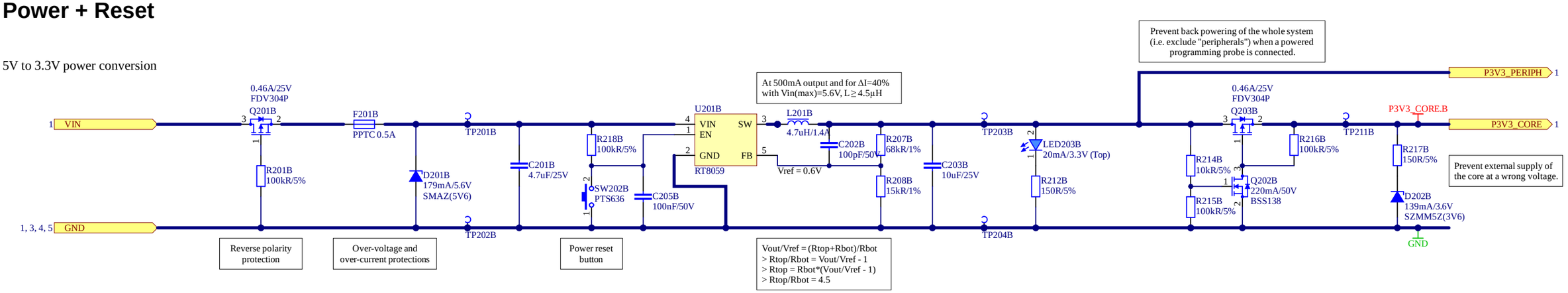
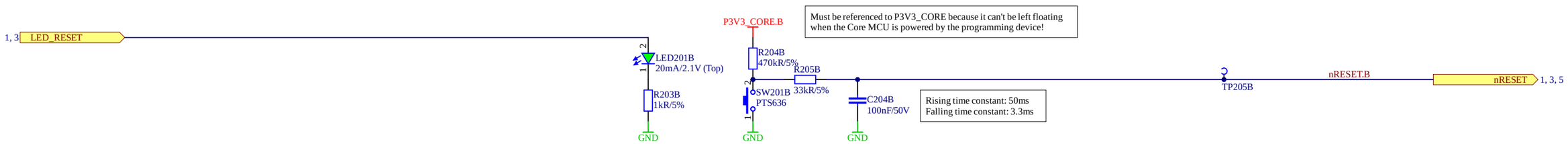
Power + Reset

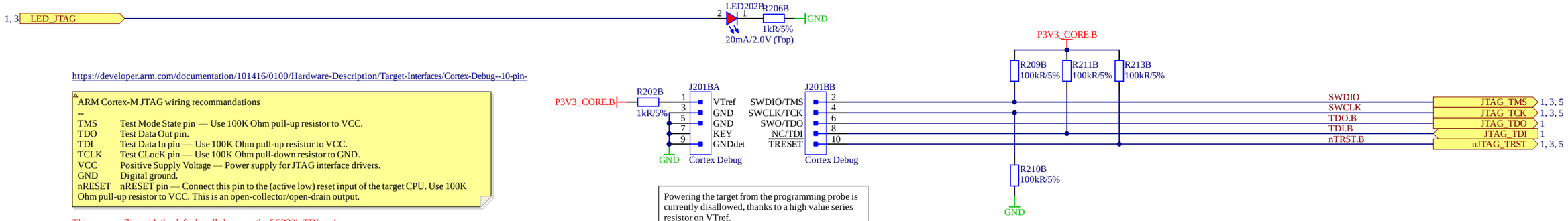
5V to 3.3V power conversion



General Reset control



JTAG prog. connector



https://developer.arm.com/documentation/101416/0100/Hardware-Description/Target-Interfaces/Cortex-Debug--10-pin-

ARM Cortex-M JTAG wiring recommandations
--

TMS	Test Mode State pin — Use 100K Ohm pull-up resistor to VCC.
TDO	Test Data Out pin.
TDI	Test Data In pin — Use 100K Ohm pull-up resistor to VCC.
TCLK	Test CLocK pin — Use 100K Ohm pull-down resistor to GND.
VCC	Positive Supply Voltage — Power supply for JTAG interface drivers.
GND	Digital ground.
nRESET	nRESET pin — Connect this pin to the (active low) reset input of the target CPU. Use 100K Ohm pull-up resistor to VCC. This is an open-collector/open-drain output.

This may conflict with the default pull-down on the ESP32's TDI pin!

Powering the target from the programming probe is currently disallowed, thanks to a high value series resistor on VTref.

A 0R resistor could be used instead, resulting in powering only the target core thanks to our "no back power" circuit. BE CAREFUL: In such case, some targets on the JTAG chain may not be powered up!

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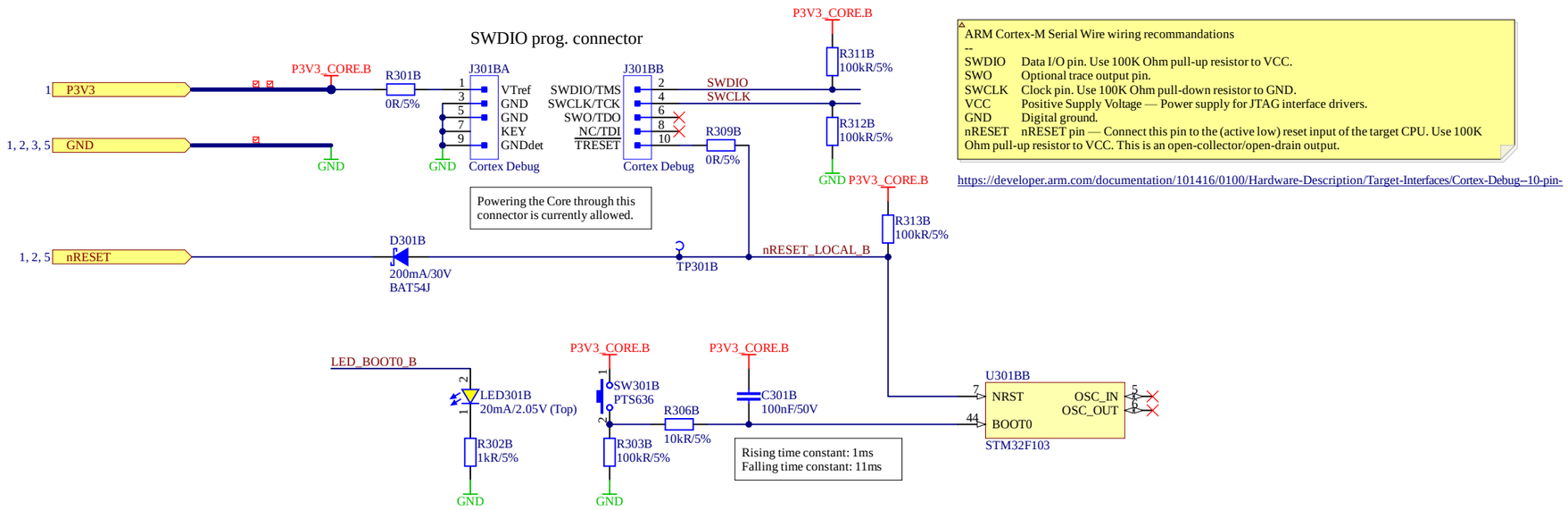
48 56 10/11/2024

STM32 core



ARM Cortex-M Serial Wire wiring recommandations
--

SWDIO	Data I/O pin. Use 100K Ohm pull-up resistor to VCC.
SWO	Optional trace output pin.
SWCLK	Clock pin. Use 100K Ohm pull-down resistor to GND.
VCC	Positive Supply Voltage — Power supply for JTAG interface drivers.
GND	Digital ground.
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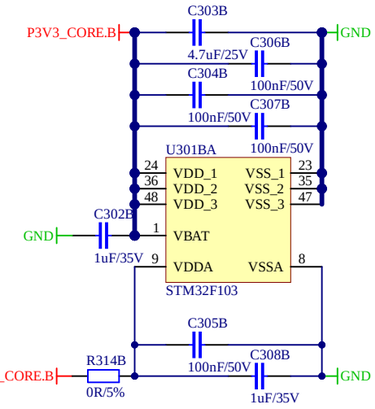

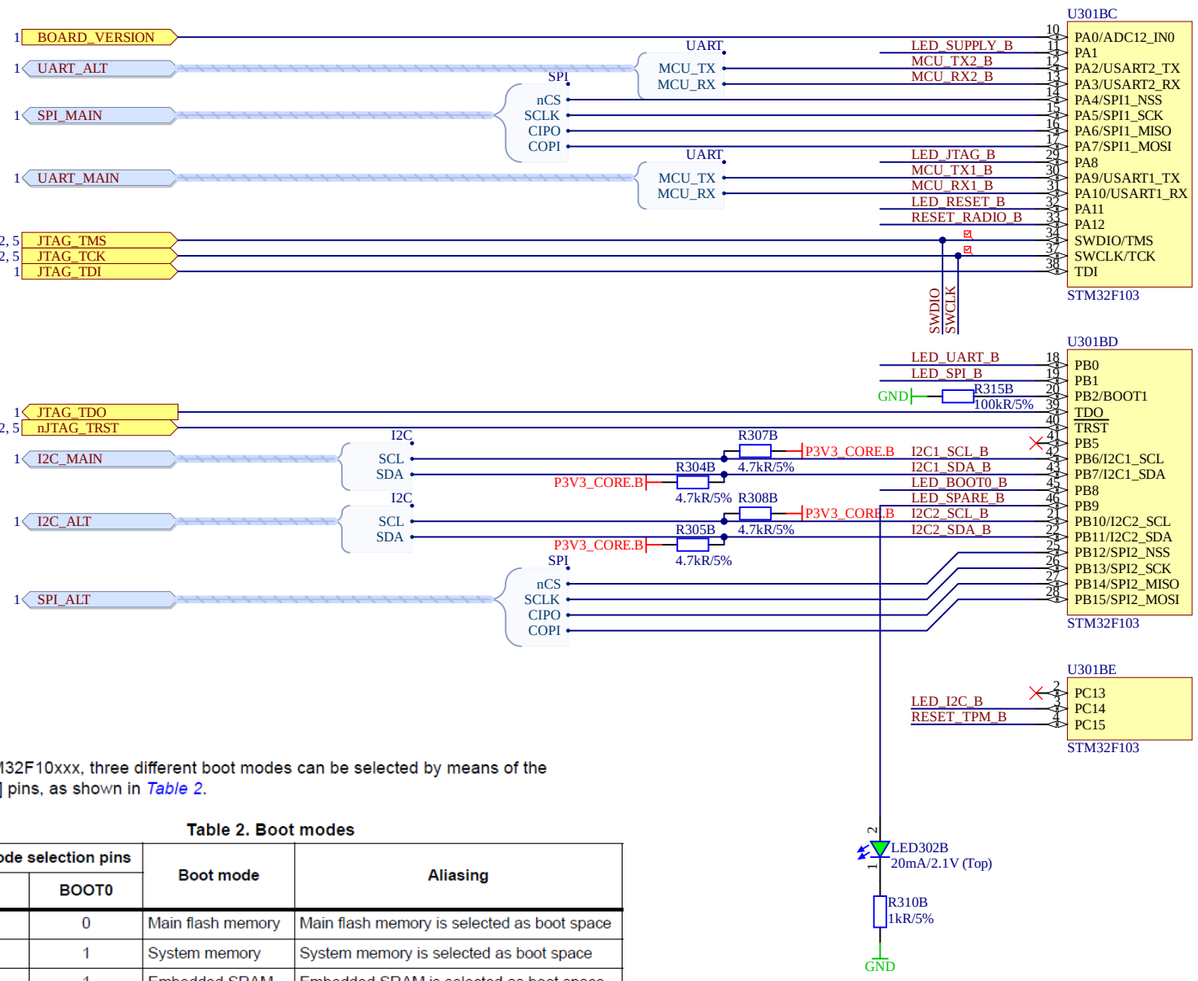

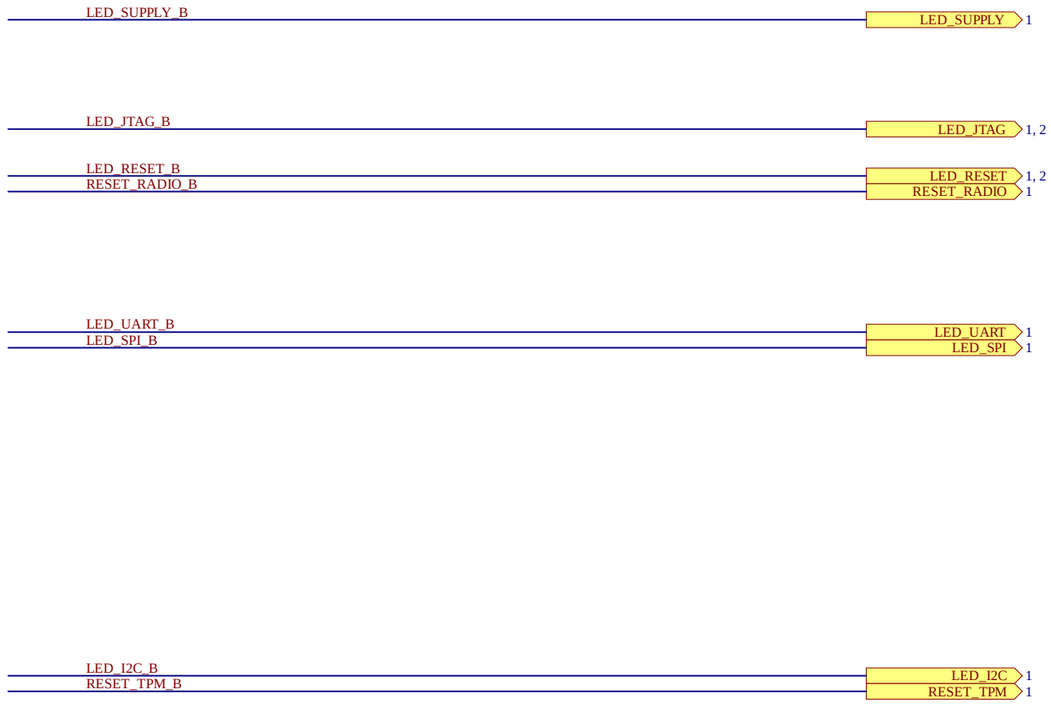

In the STM32F10xxx, three different boot modes can be selected by means of the BOOT[1:0] pins, as shown in *Table 2*.

Table 2. Boot modes

BOOT mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main flash memory	Main flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

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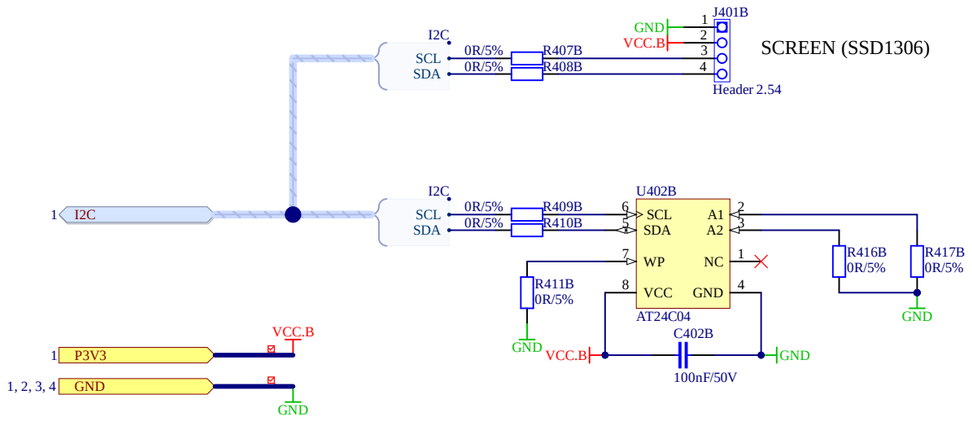

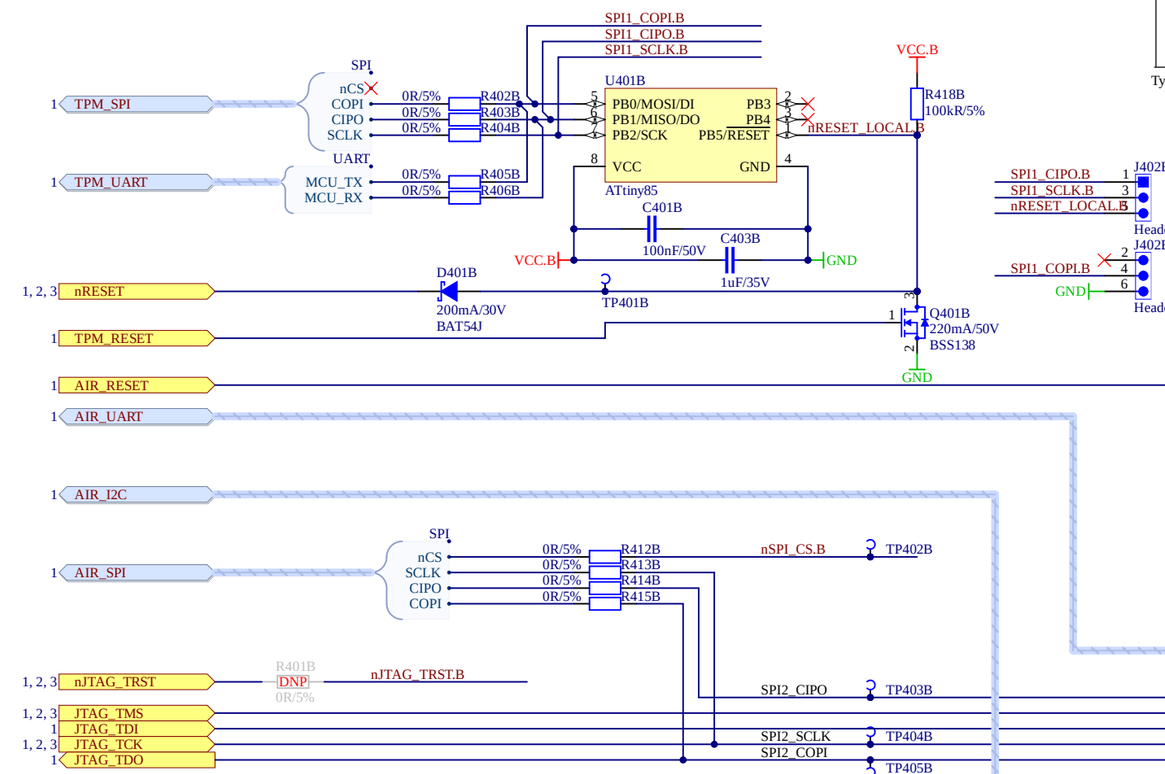

ATtiny ISP prog.

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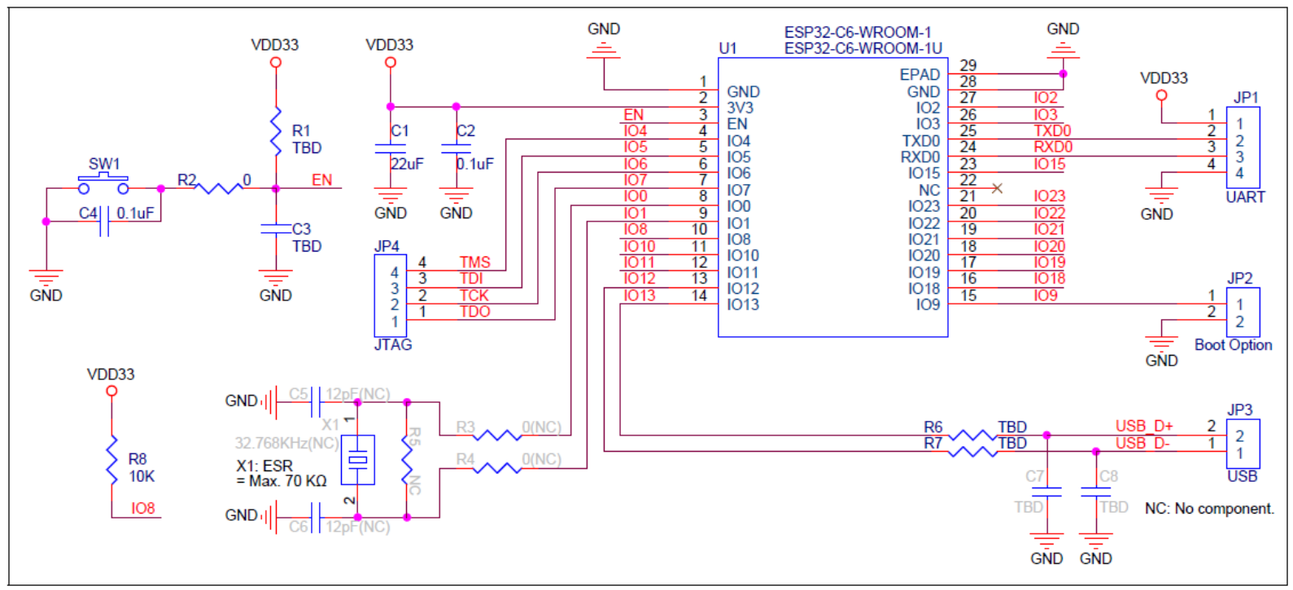
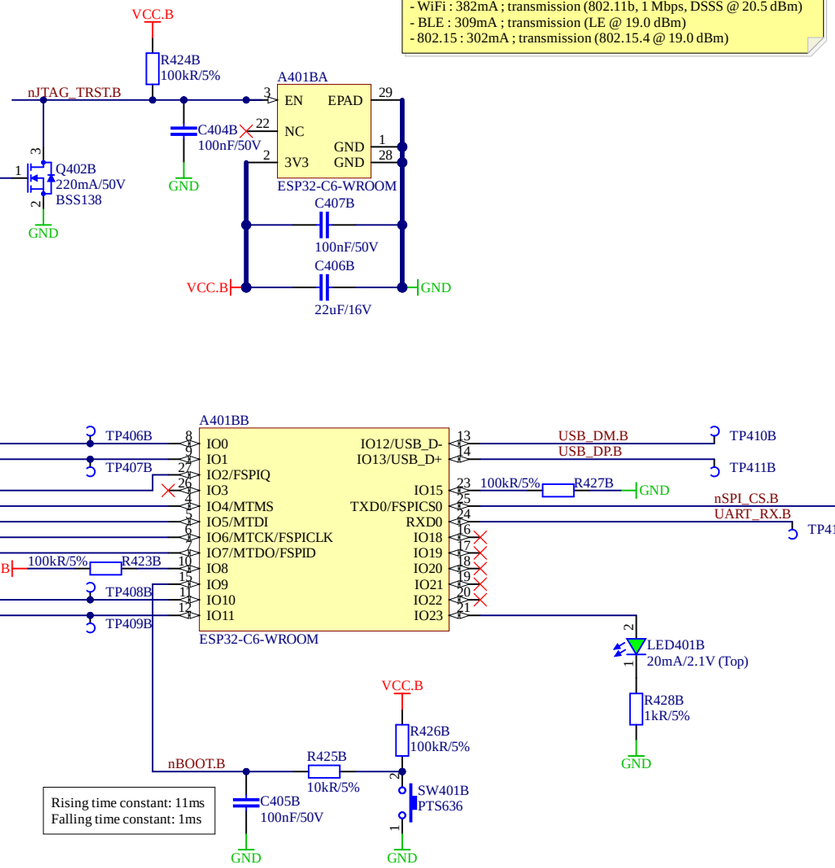


Typical ESP32-C6-WROOM usage



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0	1	Ignored	Ignored	JTAG pins MTDI, MTCK, MTMS, and MTDO
1	0	Ignored	Ignored	USB Serial/JTAG Controller
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[a] eFuse 1: EFUSE_DIS_PAD_JTAG
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48 56 10/11/2024