



# XILINX

ALL PROGRAMMABLE™

## Vivado Simulator Basics

2014.1

# Objectives

**After completing this module, you will be able to:**

- Describe the relationship between the XSim and Vivado tools**
- Using XSim, demonstrate how to**
  - Locate and select signals for simulation
  - Simulate for a fixed period of time
  - Set breakpoints
  - Single step
  - Locate points of interest in the waveform

# Vivado IDE and XSim



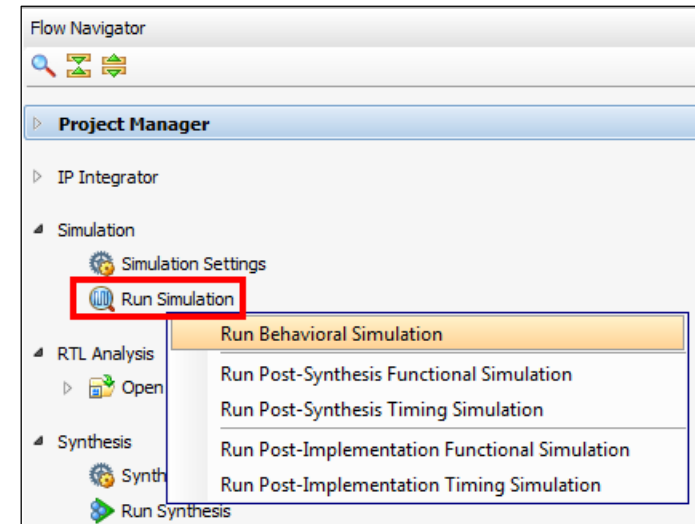
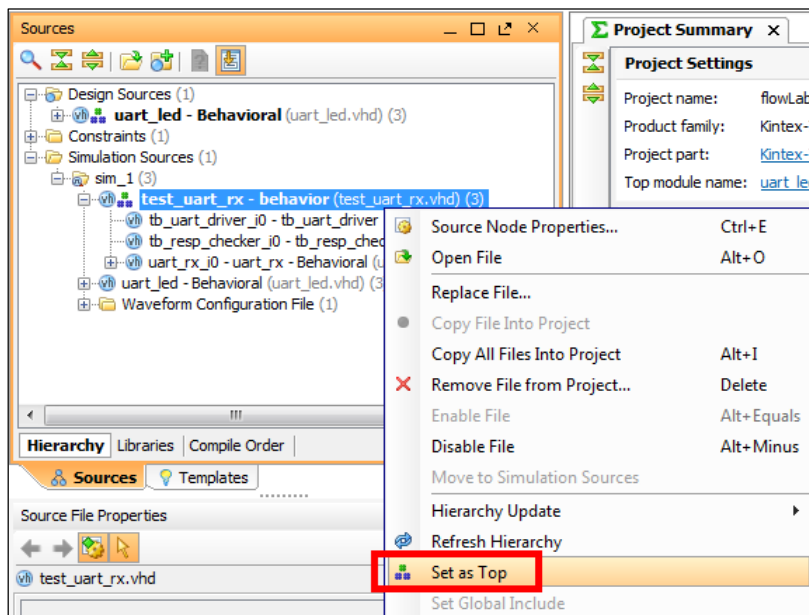
- **Vivado IDE and XSim**
- Navigating XSim
- Summary

# Xilinx and Simulation

- Vivado IDE provides an integrated simulator environment using the Vivado simulator (XSim)
- XSim can now be launched from the Vivado IDE tool environment
- XSim GUI window supports
  - Adding and removing signals
  - Navigating waveforms
  - Running and restarting simulation

# Accessing XSim in the Vivado IDE

- Behavioral simulation (direct simulation of the source code) is accessed via the Project Manager
- Vivado tool requires the top of the hierarchy to be specified



- When selected, all the top-level testbenches are displayed
  - Select the appropriate testbench to simulate
- **Warning:** The process will be applied to any item that is available in the top module list
  - Only simulate testbenches

# Vivado Simulator

The screenshot displays the Vivado Behavioral Simulation interface for a functional simulation named 'sim\_1 - test\_uart\_rx'. The interface is divided into three main sections: Scopes, Objects, and a Waveform window.

**Scopes Window:** This window shows a hierarchical tree of simulation scopes. The 'test\_uart\_rx' scope is selected, revealing its sub-scopes: 'tb\_uart\_driver\_i0', 'tb\_resp\_checker\_i0', 'uart\_rx\_i0', 'meta\_harden...', 'uart\_baud\_ge...', and 'uart\_rx\_ctl\_i0'. Each scope is associated with a specific Design Unit and Block Type (VHDL Entity).

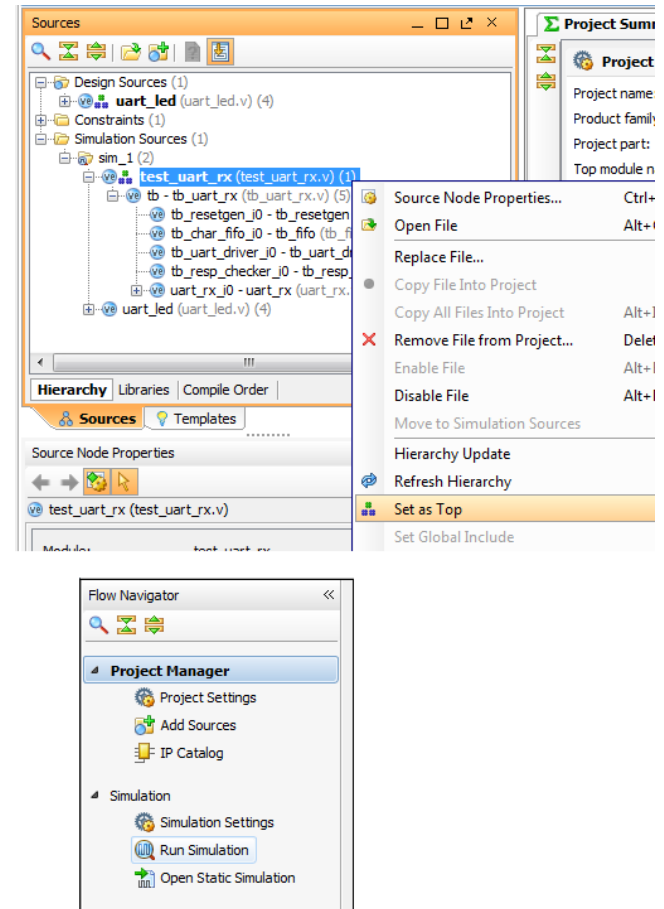
**Objects Window:** This window displays a list of simulation objects and their current values. The objects include:

Name	Value	Data Type
clk_rx	0	Logic
rst_clk_rx	1	Logic
frm_err	U	Logic
data_to_send[...]	00000000	Array
delayed_data_...	UUUUUUUU	Array
data_sent	0	Logic
rx_d_j	1	Logic
rx_data[7:0]	UUUUUUUU	Array
rx_data_rdy	U	Logic
preferred_unit...	"ns "	Array
CLOCK_RATE	1011111010...	Integer
BAUD_RATE	1110000100...	Integer
CLK_RX_PERIOD	5000 ps	Physical ...
BIT_PERIOD	8680555 ps	Physical ...

**Waveform Window:** The waveform window, titled 'Untitled 1', shows a time-based view of the simulation. The time axis ranges from 0 ps to 3 ps. The waveform displays the values of the selected objects over time, with a focus on the 'clk\_rx' signal, which is currently at 0 ps.

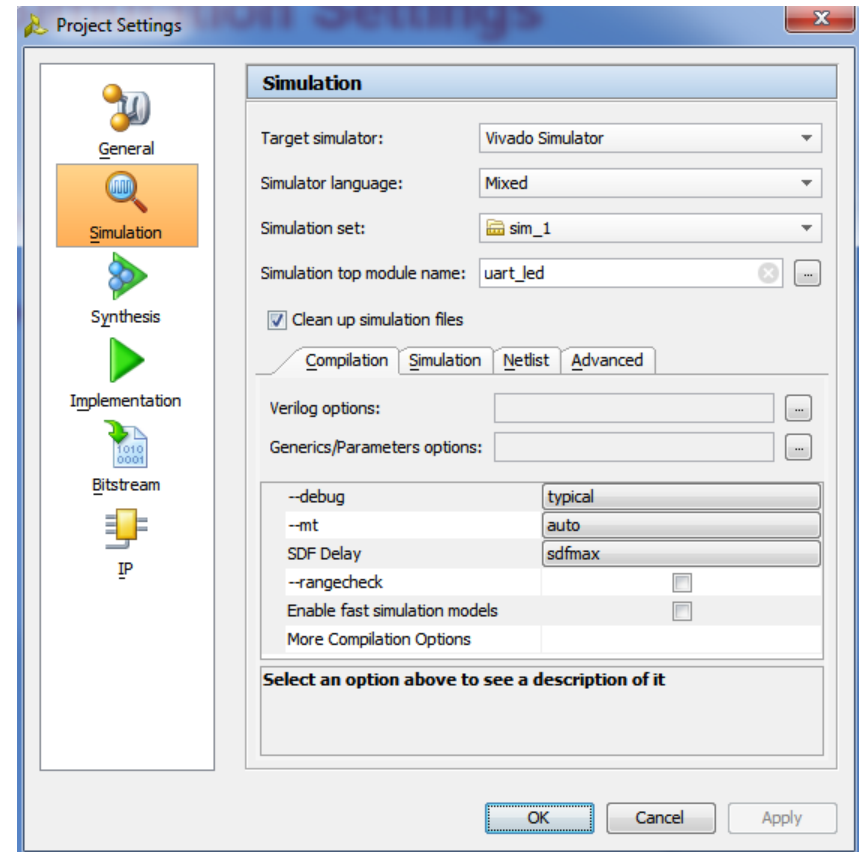
# Running a Simulation

- In the Sources view, expand Simulation Sources > sim\_1
- Select a testbench in the Hierarchy window
- Right-click and select Set as Top
- In the Flow Navigator select Simulation > Run Simulation
- Simulator launches in the Vivado IDE and executes the testbench



# Simulation Settings

- From the Flow Navigator, click Simulation Settings
- Allows selection of compilation and simulation properties
  - Additional options can be entered via more options





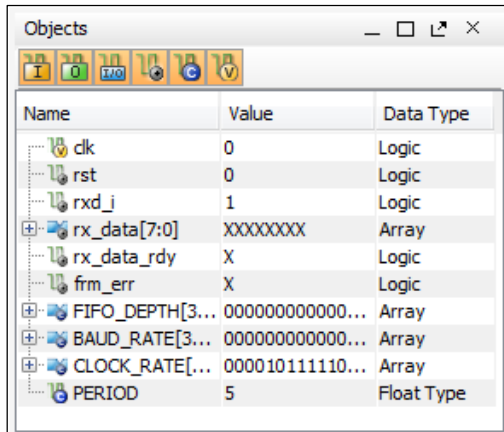
# Navigating ISim



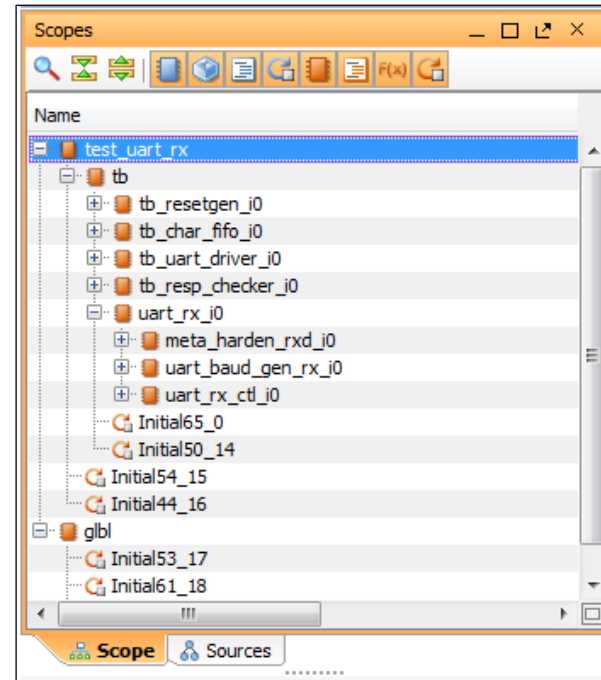
- Vivado IDE and XSim
- **Navigating XSim**
- Summary

# Selecting Signals

- The **Scopes** view supports **hierarchical signal browsing**
  - Entire hierarchical signal collections can be imported into the viewer
- The **Objects** window enables **individual signal selection**



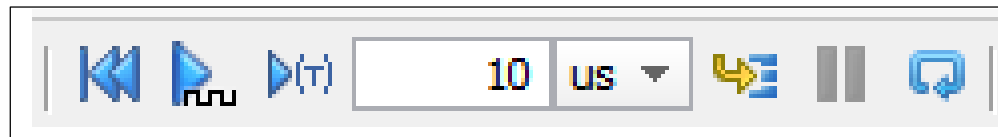
Name	Value	Data Type
clk	0	Logic
rst	0	Logic
rxd_i	1	Logic
rx_data[7:0]	XXXXXXXX	Array
rx_data_rdy	X	Logic
frm_err	X	Logic
FIFO_DEPTH[3...]	000000000000...	Array
BAUD_RATE[3...]	000000000000...	Array
CLOCK_RATE[...]	000010111110...	Array
PERIOD	5	Float Type



# Simulator Simulation Controls

## ► Controlling the simulation

- Restart simulation
- Run all
- Run for specified time
- Single step through source
- Pause simulation (Break)
- Re-launch Simulation



# Simulator Viewing Controls

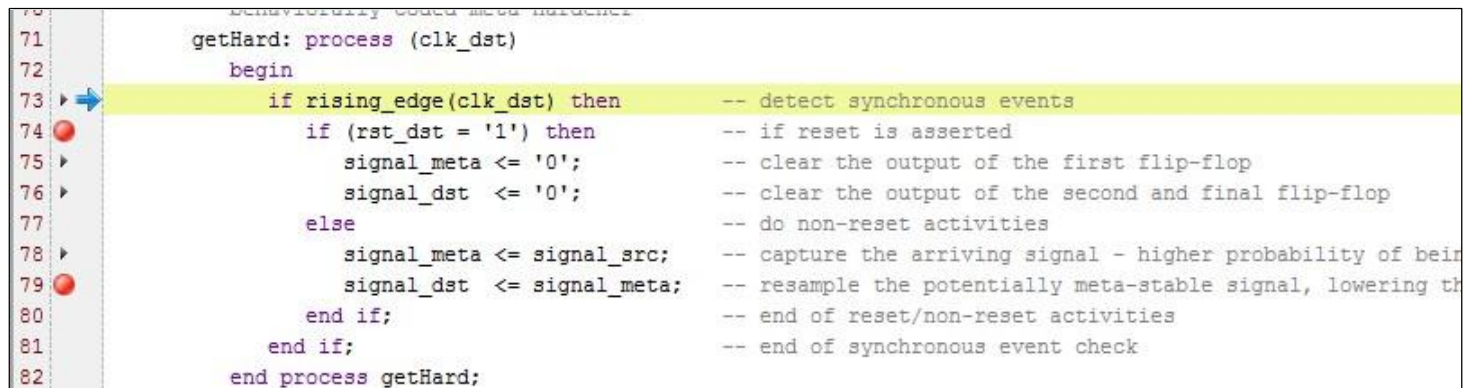
## ► Viewing the results

- Zoom in/out
- Zoom full range
- Zoom to selected
- Jump to time 0 or end
- Jump to previous/next transition on selected signal
- Insert marker
- Jump to previous/next marker
- Swap cursors
- Snap to transitions
- Floating ruler



# Breakpoints

- **Select any level of hierarchy or item from the object window, right-click and select Go to Source Code**
  - Immediately opens the containing file and positions the cursor at the object
- **Breakpoints can be set/cleared by clicking in the region between the line number and the source window**
  - Only lines with executable code are selectable



The screenshot shows a source code window in the Vivado Simulator. The code is a VHDL process named `getHard` with a clock domain `clk_dst`. The code is as follows:

```
70  -- detect synchronous events
71  getHard: process (clk_dst)
72      begin
73      if rising_edge(clk_dst) then
74          if (rst_dst = '1') then
75              signal_meta <= '0';
76              signal_dst <= '0';
77          else
78              signal_meta <= signal_src;
79              signal_dst <= signal_meta;
80          end if;
81      end if;
82  end process getHard;
```

Line 73 is highlighted in yellow, and a blue arrow points to it, indicating a breakpoint is set. Red circles are visible next to lines 74, 75, 76, 78, and 79, indicating they are also selectable for breakpoints. The line numbers are on the left, and the code is on the right.

# Summary

- Vivado IDE and XSim
- Navigating XSim
- **Summary**



# Summary

- The XSim tool is integrated with the Vivado IDE
- The simulation executable is created within the Vivado IDE
- The XSim waveform viewer "runs" the simulation and supports
  - Customization of the waveform
  - Zoom/pan controls
  - Marker
  - Single stepping the source code
  - Breakpoints

# What's Next?

## ➤ Now you know

- How to build a basic testbench (from the previous module)
- The basics of how to run the Vivado simulator

## ➤ What do you do now?

- Simulate a design