Describe the basics of dynamic RAM

# BASICS OF DYNAMIC RAM

2024.1

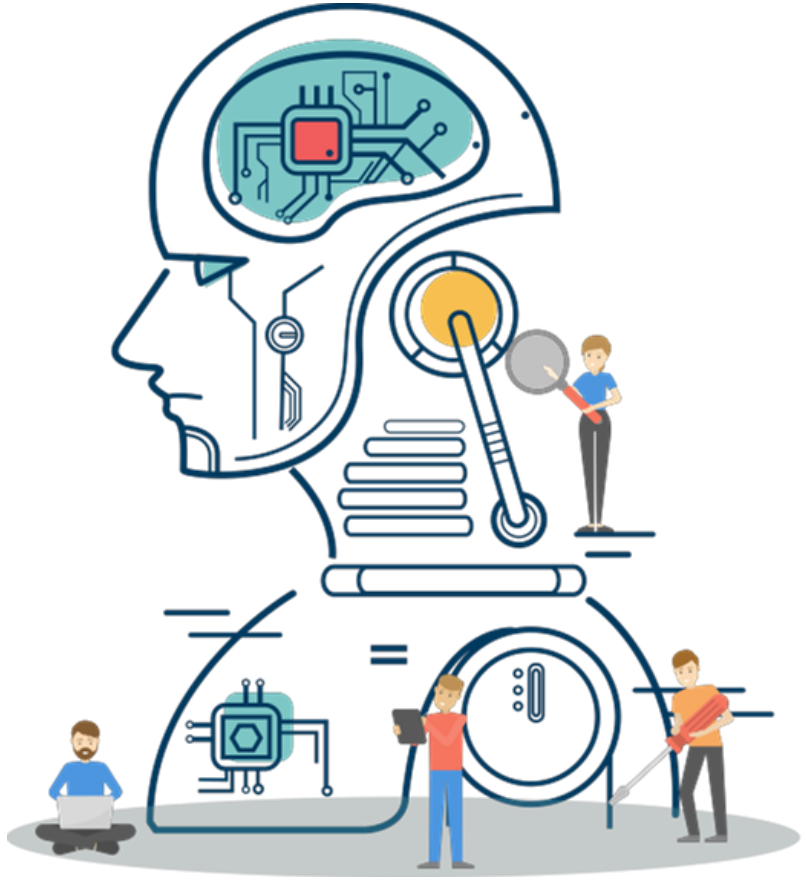
AMD
together we advance_

# Objectives

After completing this module, you will be able to:

**OBJECTIVE 01**

Describe the basics of dynamic RAM



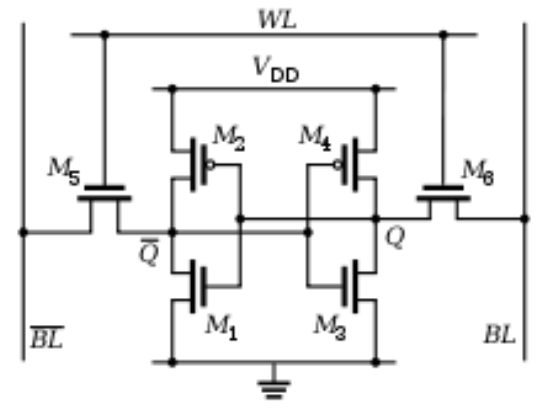
# Dynamic RAM

DDR – double data rate

Transfers data on rising and falling clock edges

# Dynamic RAM

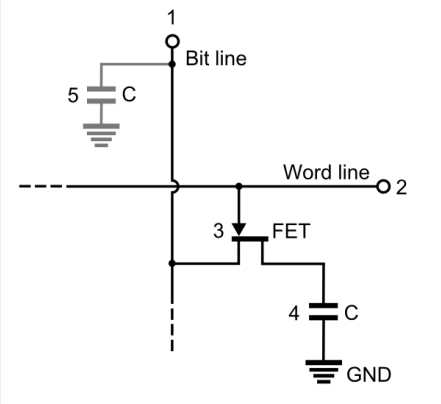
## Static Memory




SRAM Memory Cell

- Built from multiple logic gates
- Value lost on power removal
- One bit stored in a ‘D’ flip-flop
- 4-6 transistors to store one bit

## Dynamic Memory

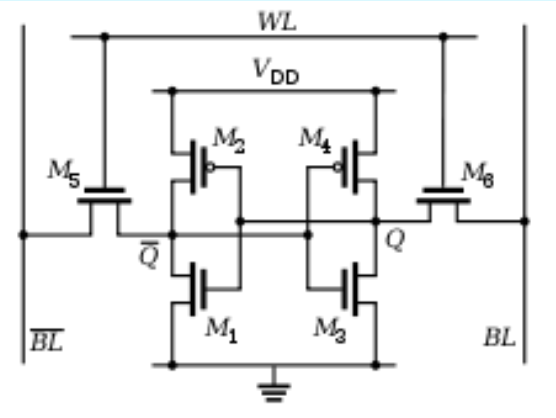



DRAM Memory Cell

- Requires transistor and small capacitor
- Value “refreshed” periodically
- Always external to the device
- Scalable controllers included in the devices

# Dynamic RAM

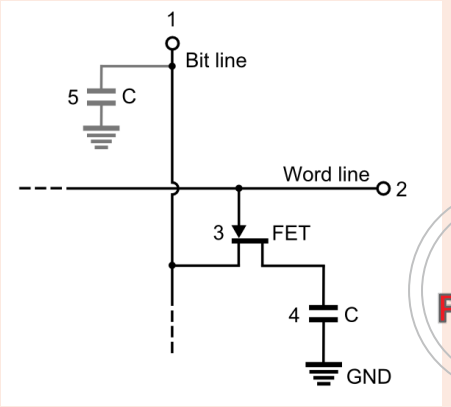
## Static Memory




SRAM Memory Cell

- Directly accessible
- Faster transistor switching
- More expensive than DDR – silicon space

## Dynamic Memory



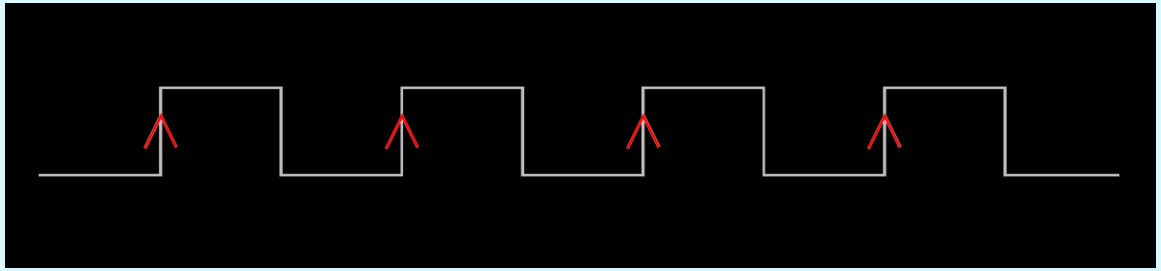

Most Popular

DRAM Memory Cell

- Controller required due to complexity
- Slower charging/discharging capacitors

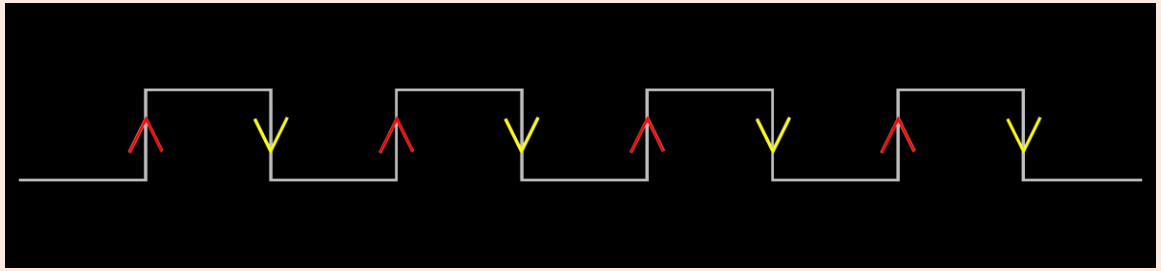
# Dynamic RAM

## Single Data Rate



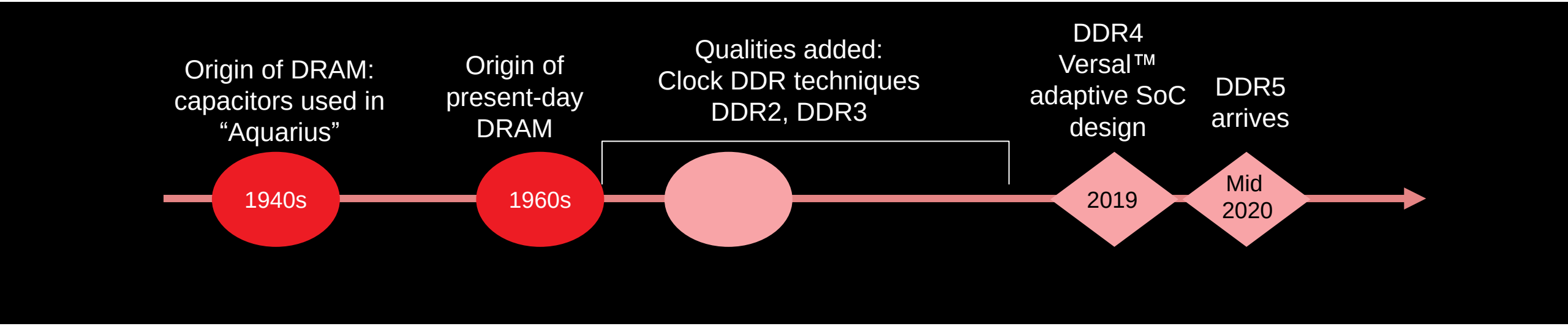
- Data moves on rising clock edge
- More high-frequency components
- Power and noise compliance implications

## Double Data Rate



- Data moves on rising and falling clock edges
- Two moves per clock
- Tricky for single datum reads/writes
  - Handled by the DDR controller
  - Irrelevant – bulk data transfer mechanism

# Dynamic RAM



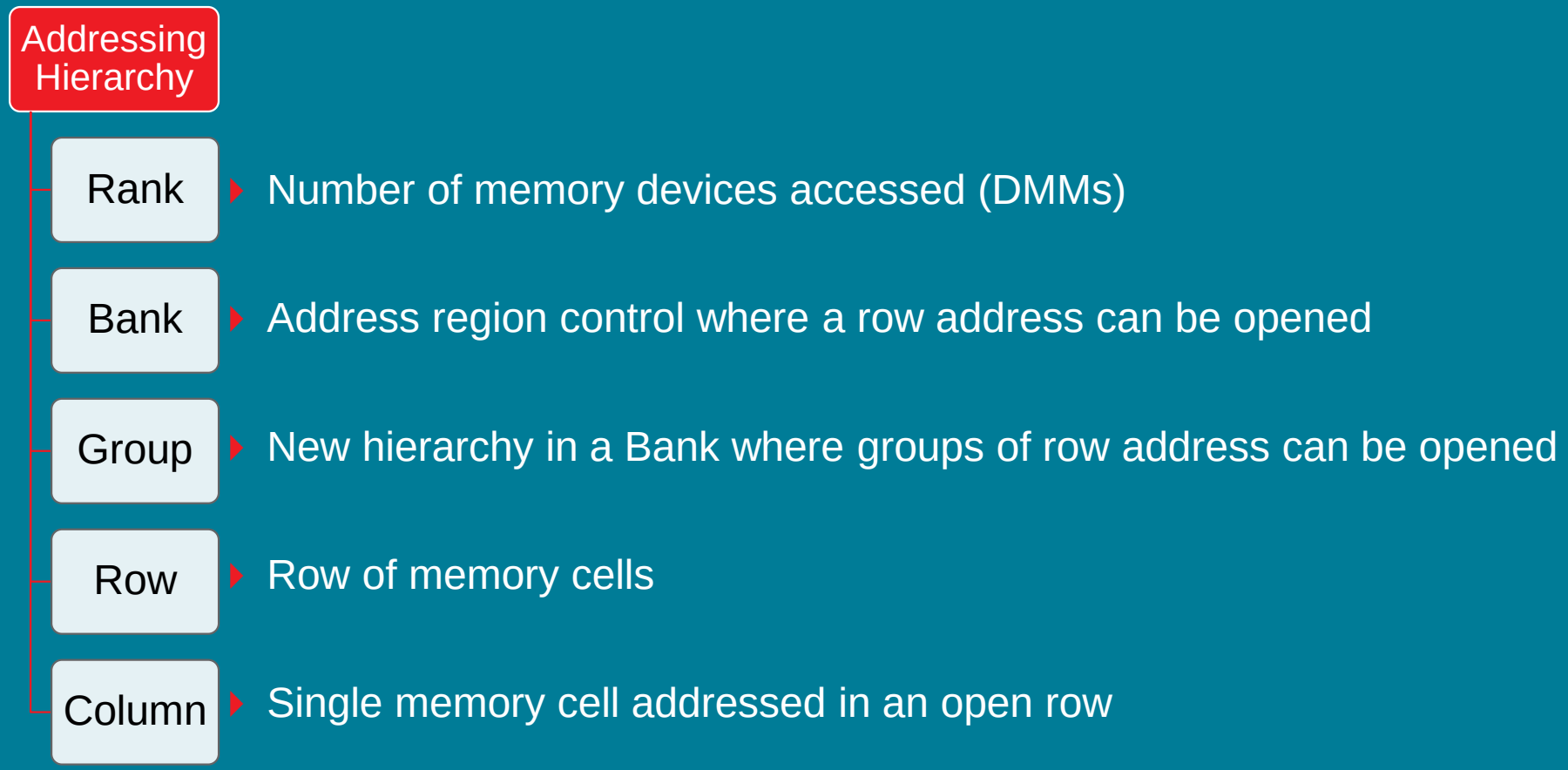

Versal adaptive SoC uses DDR4

Does not use DDR5

| DDR SDRAM Standard | Internal rate (MHz) | Bus clock (MHz) | Prefetch | Data rate (MT/s) | Transfer rate (GB/s) | Voltage (V) |
|---|---|---|---|---|---|---|
| SDRAM | 100-166 | 100-166 | 1n | 100-166 | 0.8-1.3 | 3.3 |
| DDR | 133-200 | 133-200 | 2n | 266-400 | 2.1-3.2 | 2.5/2.6 |
| DDR2 | 133-200 | 266-400 | 4n | 533-800 | 4.2-6.4 | 1.8 |
| DDR3 | 133-200 | 533-800 | 8n | 1066-1600 | 8.5-14.9 | 1.35/1.5 |
| DDR4 | 133-200 | 1066-1600 | 8n | 2133-3200 | 17-21.3 | 1.2 |
| DDR5 | — | — | >8ns | 4000-8000 | 32-64 | 1.1 |

# Dynamic RAM Basics

Controller manages complex address-data access



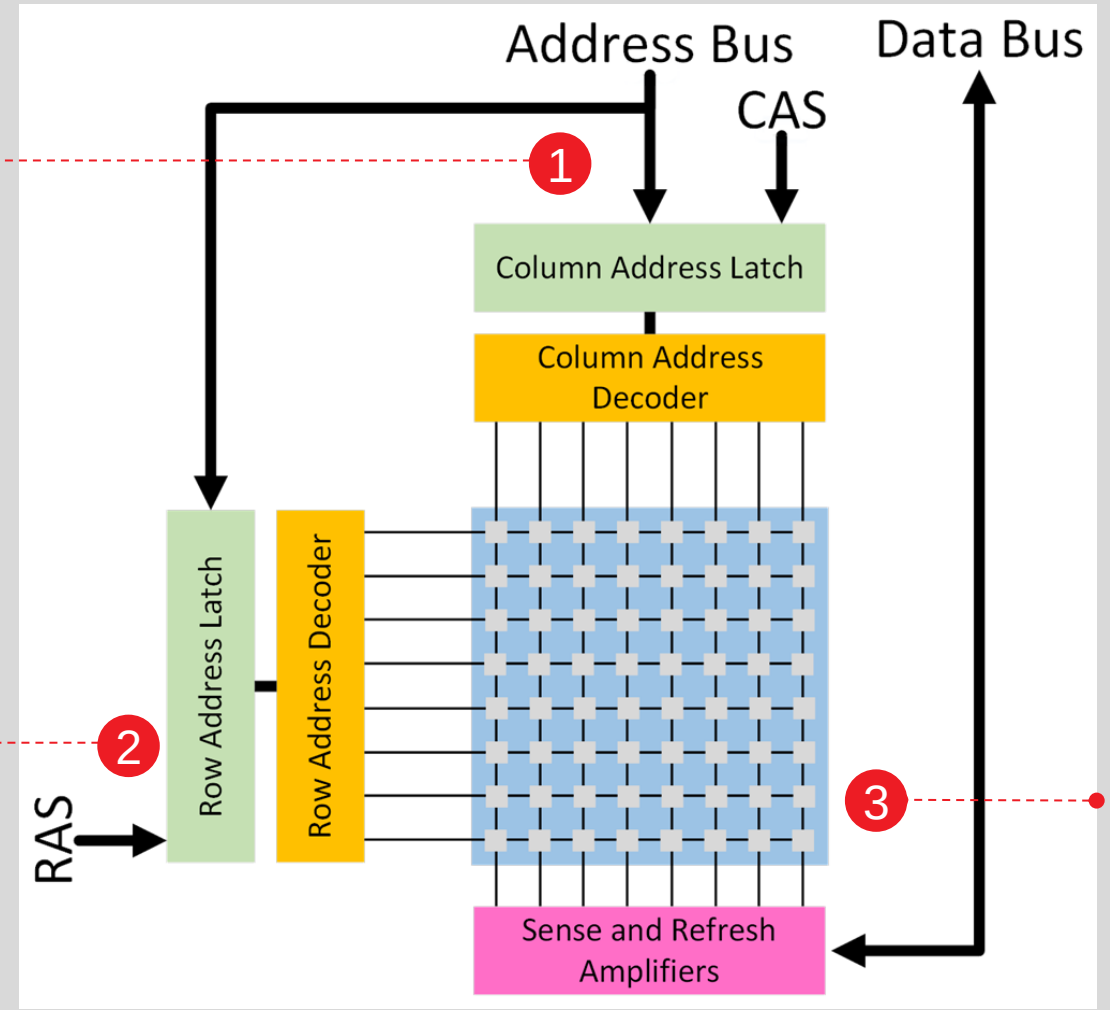
# Dynamic RAM Basics

- Data accessed on a row/column basis
- Row/column driven by system address lines
- Row/column addresses share package pins
- Two device pin RAS and CAS indicate the address on package pins

# Dynamic RAM Basics

Row addresses placed on the device address pins

RAS signal asserted




Row is open

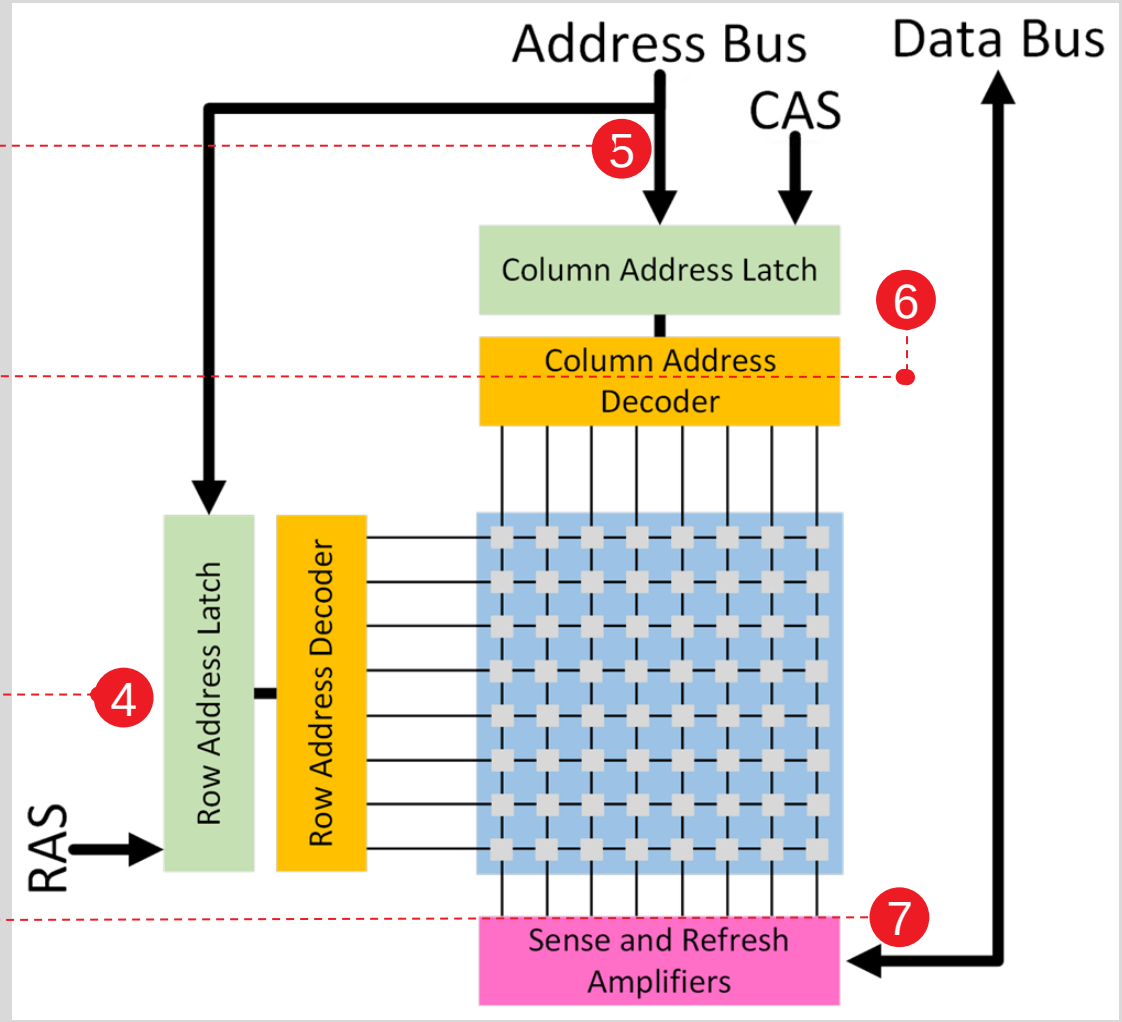
# Dynamic RAM Basics

Column addresses placed on device address pins

CAS signal asserted

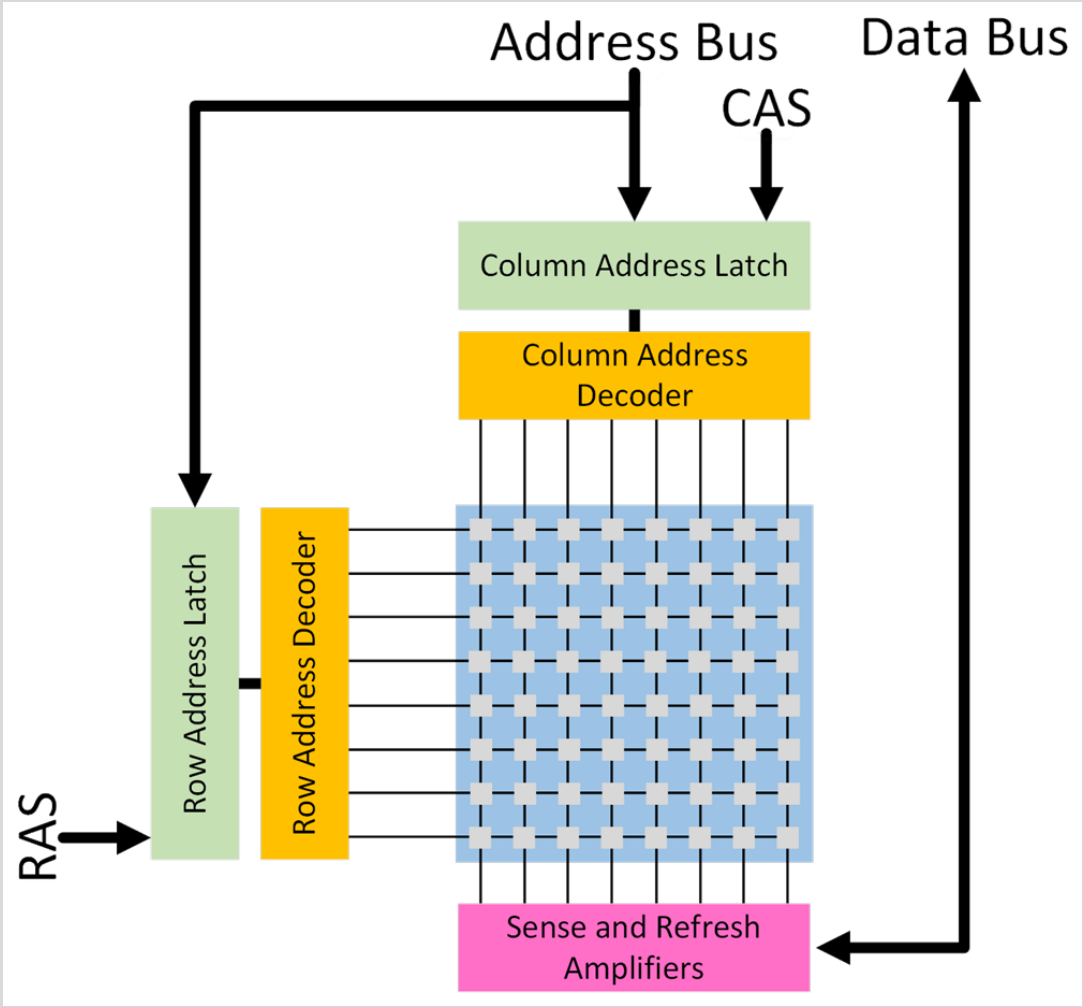
Dynamic RAM controller multiplexes from row to column addresses

After access time, data read/write



# Dynamic RAM Basics

- Row opening: Slowest operation
- Opened rows can remain open
- Latch new column addresses
- Access to an open row is faster



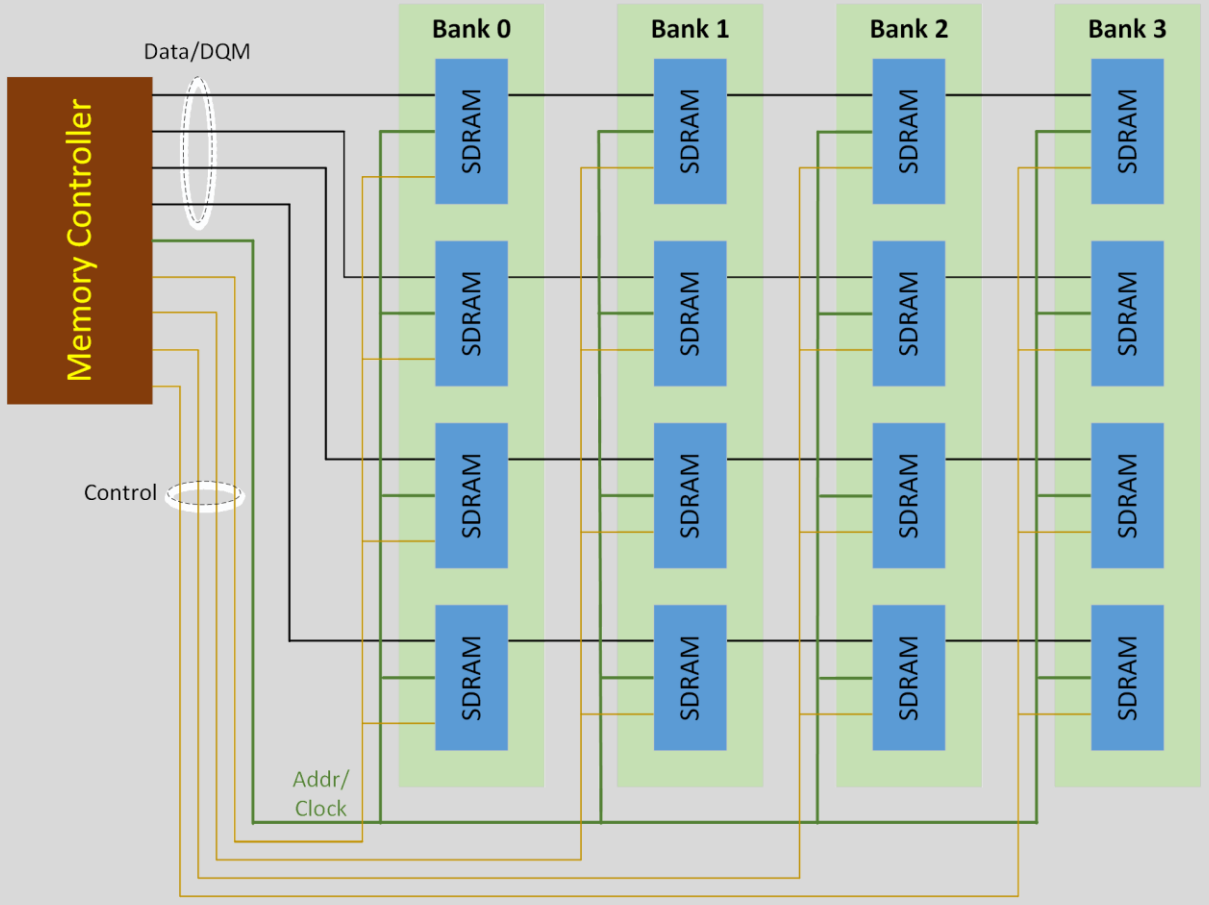
# Apply Your Knowledge

**Q** Match each address hierarchy to its appropriate description.

| Address Hierarchy | Descriptions |
| --- | --- |
| Ranks | Address region controls |
| Banks | Row of memory cells |
| Group | Single memory cell addressed |
| ROW | New hierarchy |
| COLUMN | Number of memory devices accessed |

# DDR4 Synchronous Dynamic RAM

- 1.2V operation
- Auto/self-refresh
- Separate data I/O by bank groups
- Enhanced DQ training
- Command/address parity
- Data bus write CRC
- Boundary scan
- Programmable timing
- Power-down mode
- Data rate: 1600 – 3200 MHz
- Density: 2Gb – 16 Gb



# DDR4 SDRAM Command Basics

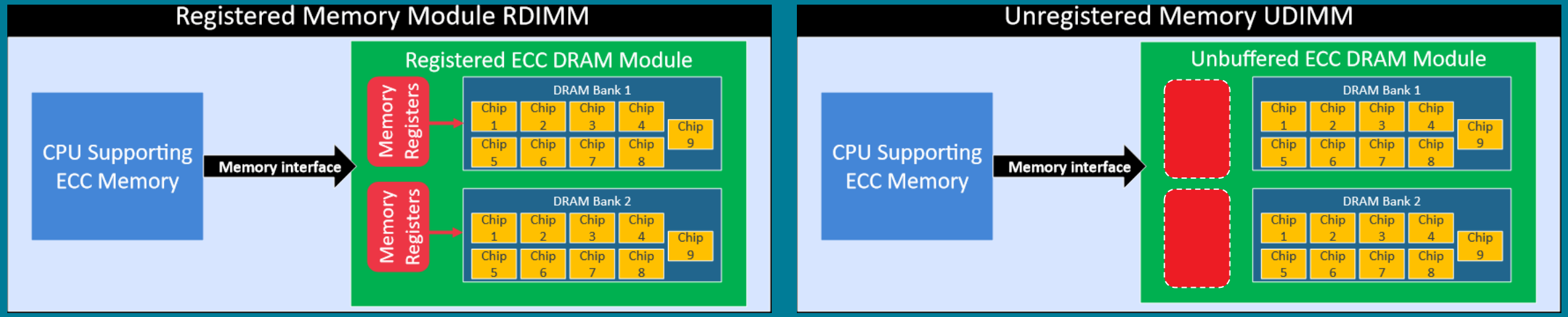
DDR commands:

- CS – Chip enable
- RAS – Open a row
- CAS – Access a memory cell in the open row
- WE – Write enable
- BA – Bank address
- BG – Bank group
- BC – Burst chop for data burst operations
- AP – Auto-precharge
  - Close row after read/write and ready another row
- ACT – Activation command input
  - Mux input between RAS, CAS, WE, and A16, A15, A1

| Command | $\overline{CS}$ | BG1–0, BA1–0 | $\overline{ACT}$ | A17 | A16 $\overline{RAS}$ | A15 $\overline{CAS}$ | A14 $\overline{WE}$ | A13 | A12 BC | A11 | A10 AP | A9–0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselect (no operation) | H | X | | | | | | | | | | |
| Active (activate): open a row | L | Bank | L | Row address | | | | | | | | |
| No operation | L | V | H | V | H | H | H | V | | | | |
| ZQ calibration | L | V | H | V | H | H | L | V | | | Long | V |
| Read (BC, burst chop) | L | Bank | H | V | H | L | H | V | BC | V | AP | Column |
| Write (AP, auto-precharge) | L | Bank | H | V | H | L | L | V | BC | V | AP | Column |
| Unassigned, reserved | L | V | v | V | L | H | H | V | | | | |
| Precharge all banks | L | V | H | V | L | H | L | V | | | H | V |
| Precharge one bank | L | Bank | H | V | L | H | L | V | | | L | V |
| Refresh | L | V | H | V | L | L | H | V | | | | |
| Mode register set (MR0–MR6) | L | Register | H | L | L | L | L | L | Data | | | |

Signal level (H, high • L, low • V, either low or high, a valid signal • X, irrelevant) • Logic level ( Active • Inactive • Not interpreted)

# DDR4 SDRAM Packaging



# DDR4 SDRAM Packaging

SODIMM | UDIMM | RDIMM | LRDIMM

Single Components

Raw memory devices

Assembled into modules

Used directly on boards

Not upgradable or expandable


# DDR4 SDRAM Packaging

## SODIMM

- Small outline dual in-line memory module
- Smaller footprint alternatives to a DIMM
- Used when space limited
- DDR4 SODIMMs have 260 pins


## UDIMM

- Unregistered version of a SODIMM
- Used in desktop and laptop computers
- Called unbuffered memory
- Run faster than RDIMM
- Packaged on 288-pin PCB cards

## RDIMM

- Registered memory version of the DDR
- Used in servers
- Provides better stability and scalability
- Lowers workload on MC
- Packaged on 288-pin PCB cards

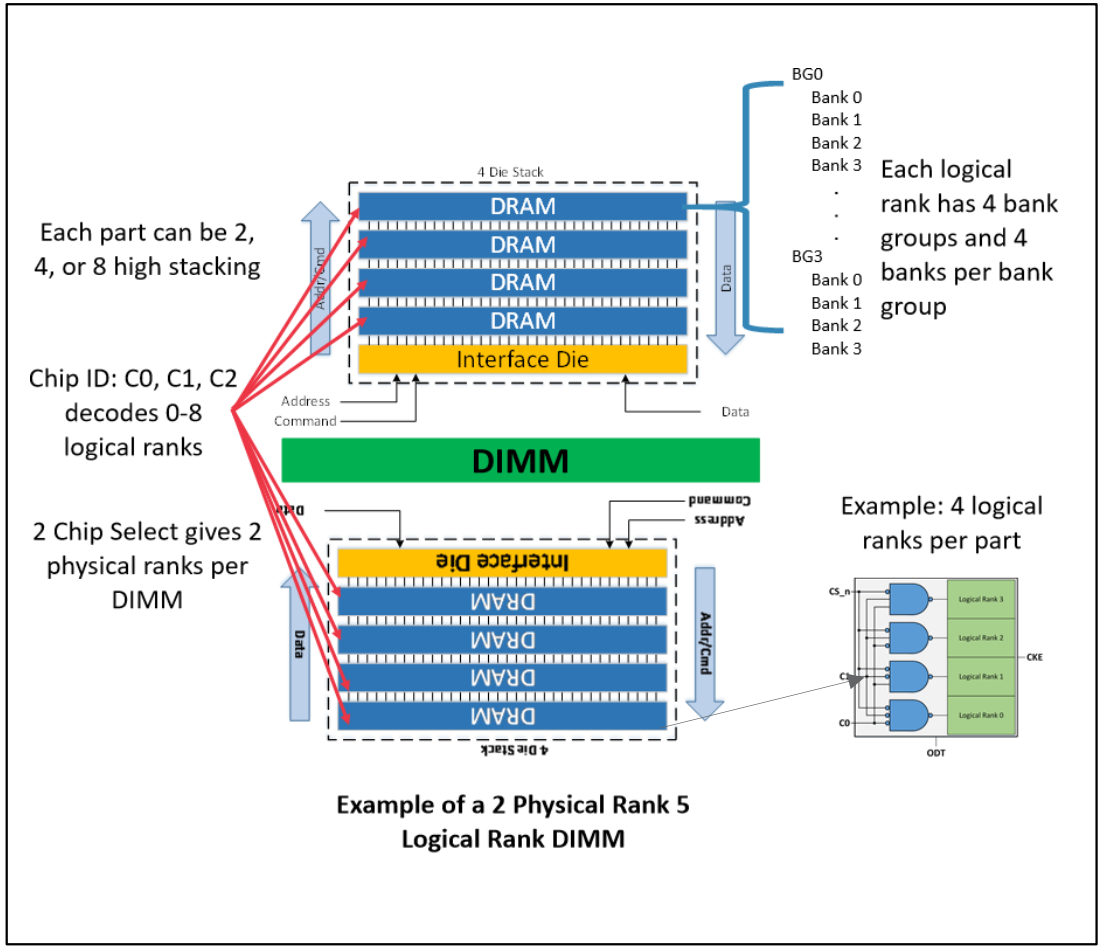
## LRDIMM

- Load-reduction DIMM
- Used in servers
- Supports higher densities than RDIMMS
- Contains a memory buffer chip
- Very expensive
- Packaged on 288-pin PCB cards

# DDR4 SDRAM Packaging

3DS DDR4 SDRAM

- High-speed, CMOS DRAM
- 2-high or 4-high 3DS component
- 2-high device has 1 master die and 1 slave die
- 4-high device has 1 master die and 3 slave dies
  - Bottom die always the master
- 3DS stack: device and dies use the same addressing
- 2-high stack: 2 independent selectable logical ranks
- 4-high stack: 4 independent selectable logical ranks
- 3DS stacks only have one CSn pin
- Master/slave logic sharing
  - Varied impact – all ranks or single rank




**Example of a 2 Physical Rank 5 Logical Rank DIMM**

# Apply Your Knowledge

**Q** Which memory component is used to provide better scalability for systems running on a server?

- SODIMMs
- UDIMMs
- RDIMMs
- LRDIMMs

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