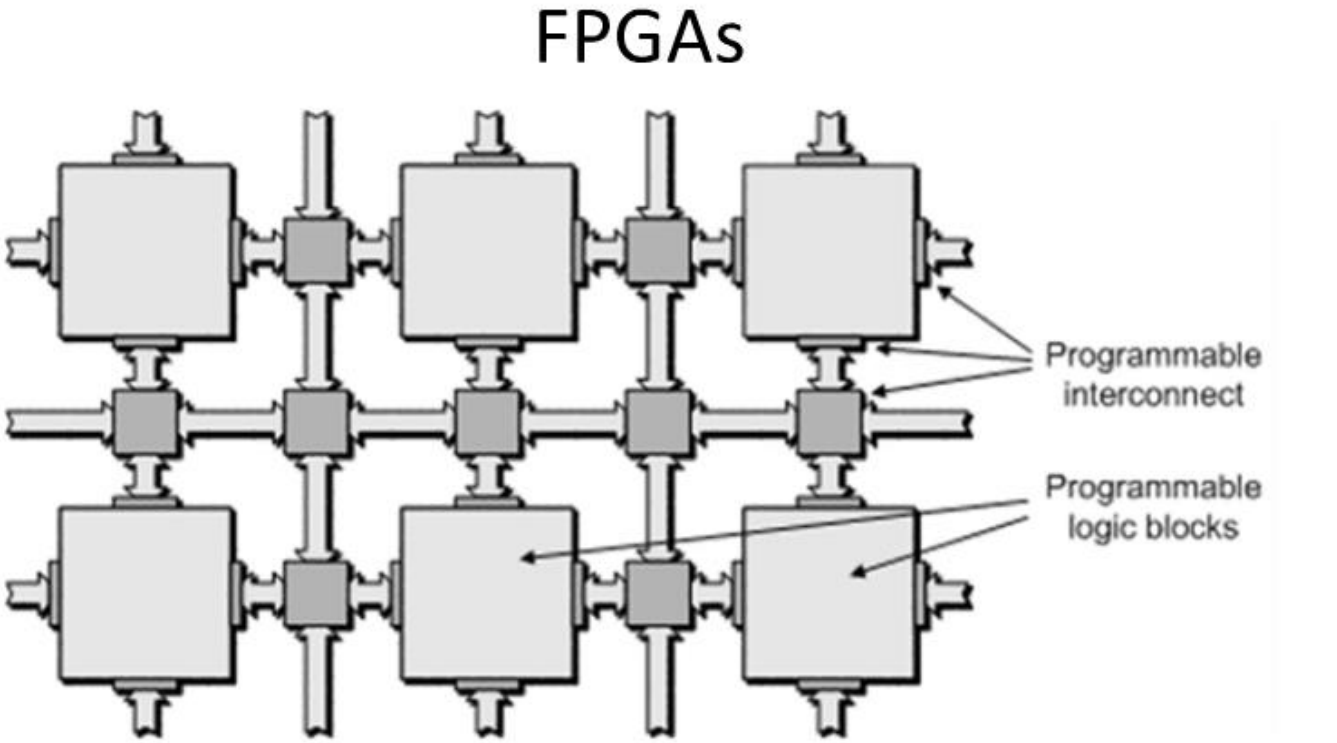
FPGA BASIC PRINCIPLES & VHDL INTRODUCTION

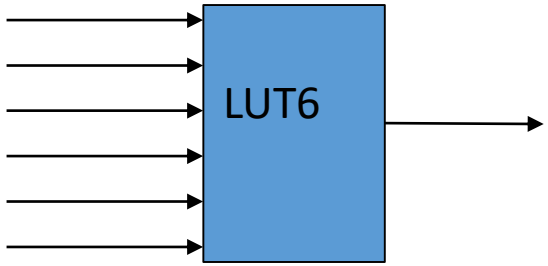
- What is FPGA?
- FPGA basic components
- FPGA Design Flow.
- RTL-register transfer level.
- Parallel processing verse serial processing.
- **Lab 1: VIVADO-using the tools-creating a new project.**

FPGA-introduction

***FPGA**-filed programmed gate array*

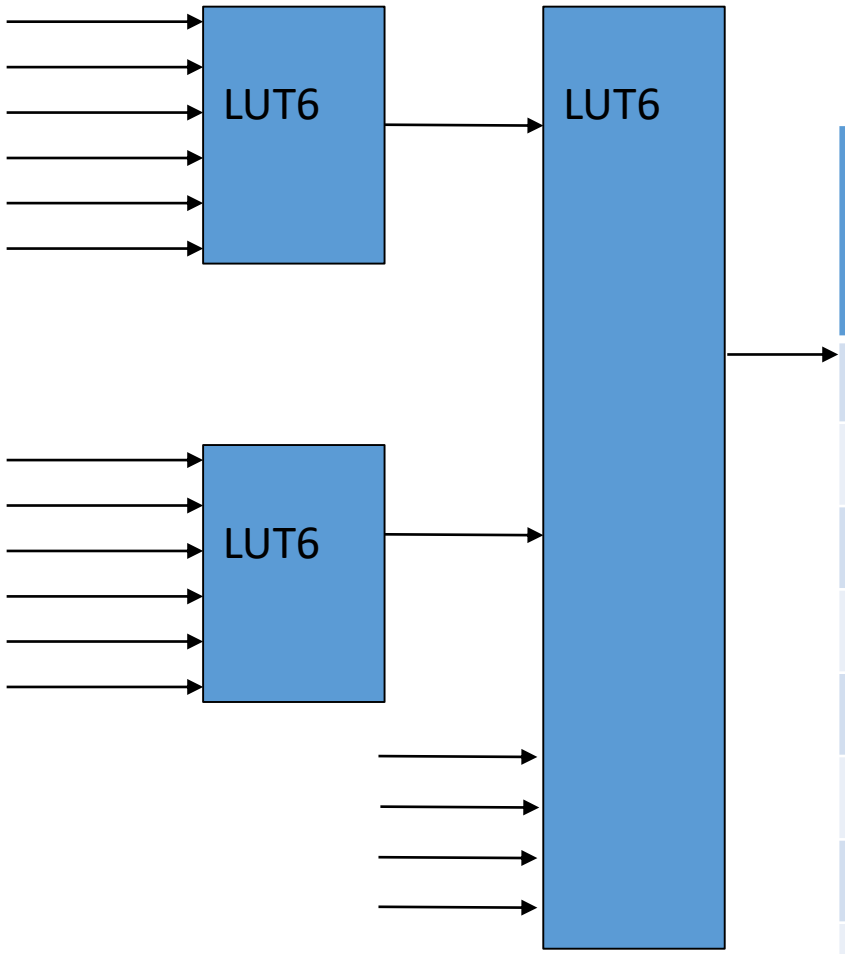


LUT –comparator example



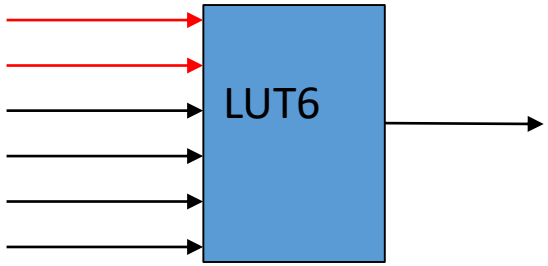
IO	I1	I2	I3	I4	I5	OUT
0	0	0	0	0	0	1
0	0	0	0	0	1	0
0	1	0	0	1	0	1
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	1

LUT- COMPARATOR "LEGO”-



IO	I1	I2	I3	I4	I5	OUT
0	0	x	x	x	x	0
0	1	x	x	x	x	0
1	0	x	x	x	x	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	x	x	x	x	1
1	1	x	x	x	x	1
1	1	x	x	x	x	1

LUT- MULTIPLEXER EXMAPLE

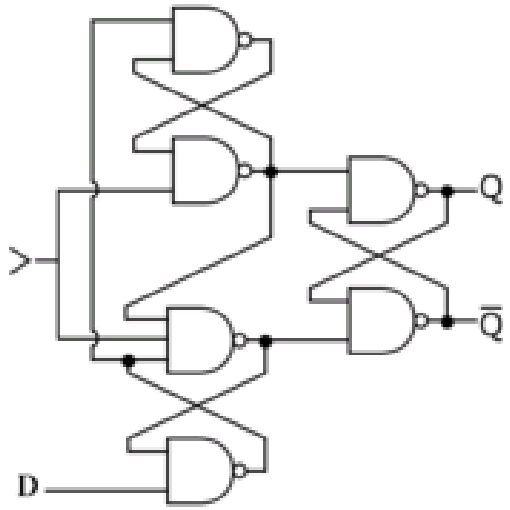


IO(sel1)	I1(sel0)	I2	I3	I4	I5	OUT
0	0	0	0	0	0	0
0	1	0	0	1	0	1
1	0	0	1	1	0	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	0	1	0	1	0
1	1	0	1	1	0	0
1	1	1	1	1	1	1

FLIP-FLOP

flip-flop has two stable states and thereby is capable of serving as one bit of memory.

A flip-flop is usually controlled by one or two control signals and/or a gate or clock signal

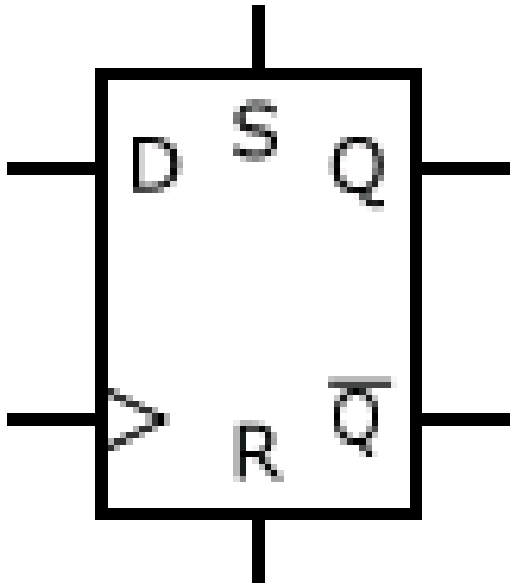


D-FLIP FLOP

The Q output always takes on the state of the D input at the moment of a rising clock edge (or falling edge if the clock input is active low).. The D flip-flop can be interpreted as a primitive memory cell, delay line.

Truth table:

Clock	D	Q
Rising edge	0	0
Rising edge	1	1
Non-Rising	X	Q_{prev}



VHDL

What is Vhdl?

VHDL-**VHSIC** *hardware description language*

VHSIC-Very *High-Speed Integrated Circuit*

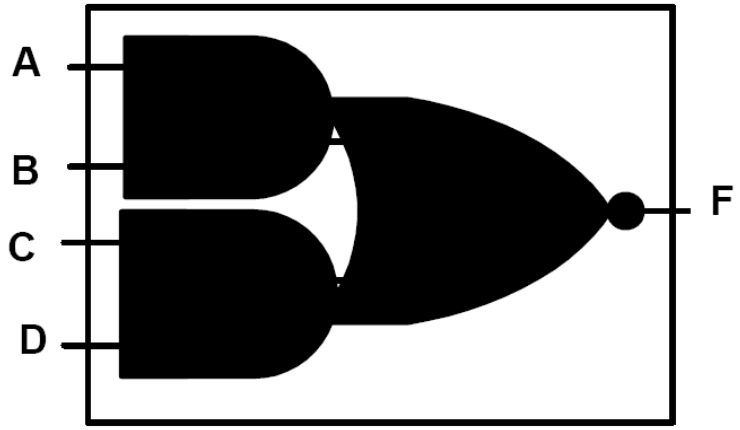
ENTITY.

The *entity declaration* represents the external interface to the design entity.

ARCHITECTURE

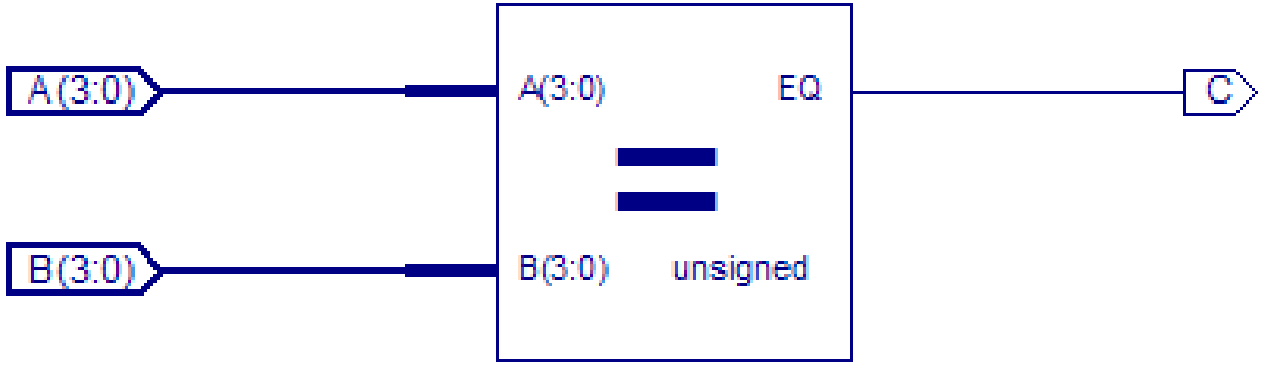
The *architecture body* represents the internal description of the design

entity - its behavior, its structure, or a mixture of both. In this example, we want to describe an and-or-invert (**AND_OR_INV**) gate in VHDL. If we consider the **AND_OR_INV** gate as a single chip package, it will have four input pins and one output pin.



ENTITY

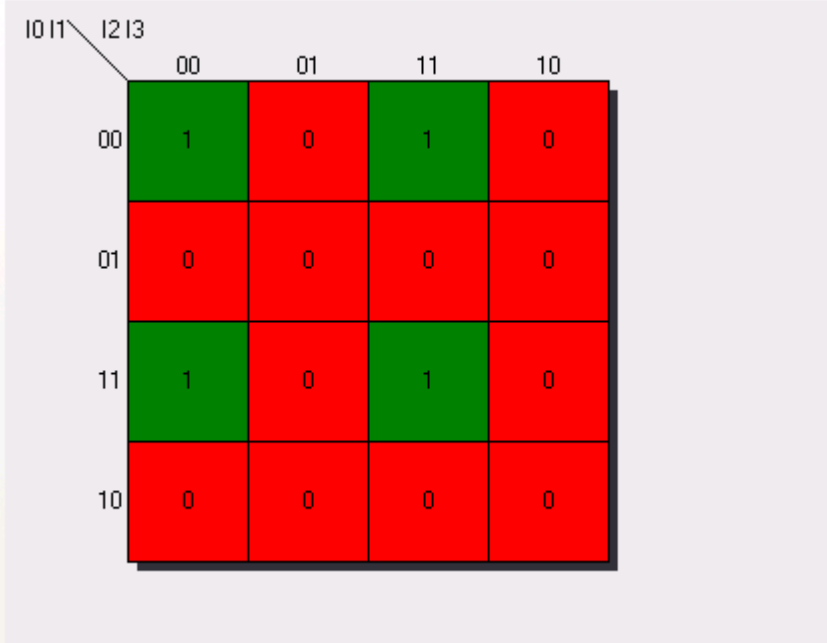
```
entity my_comp is
    Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
           B : in  STD_LOGIC_VECTOR (3 downto 0);
           C : out  STD_LOGIC);
end my_comp;
```



Process

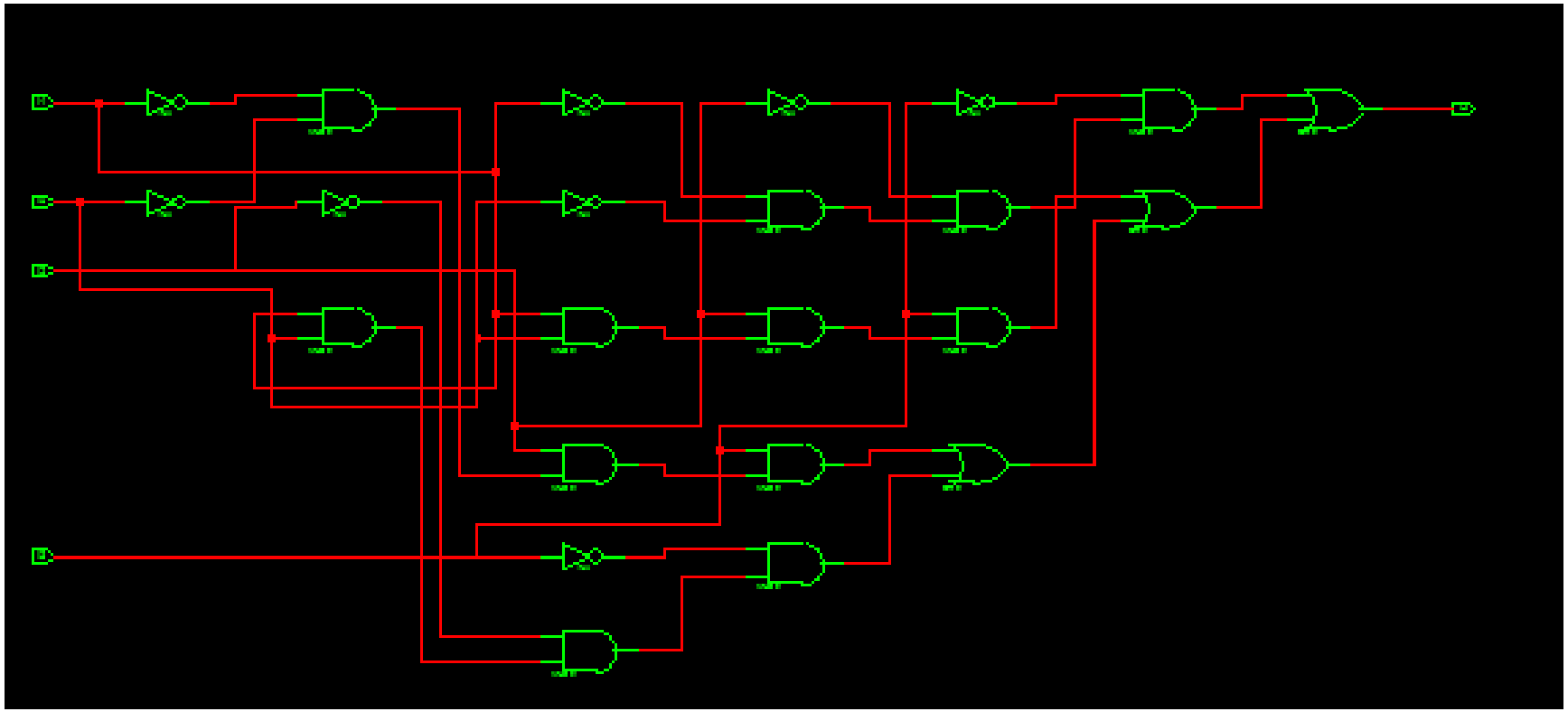
```
architecture my_comp of my_comp is

begin

        Process (A,B)
        begin
        if (A=B) then
            C<='1';
        else
           C<= '0';
        end if ;
        end process;
end my_comp;
```

Kranugh map-*synthesis*



((i0 * i1 * !i2 * !i3) + (!i0 * !i1 * i2 * i3) + (i0 * i1 * i2 * i3) + (!i0 * !i1 * !i2 * !i3))

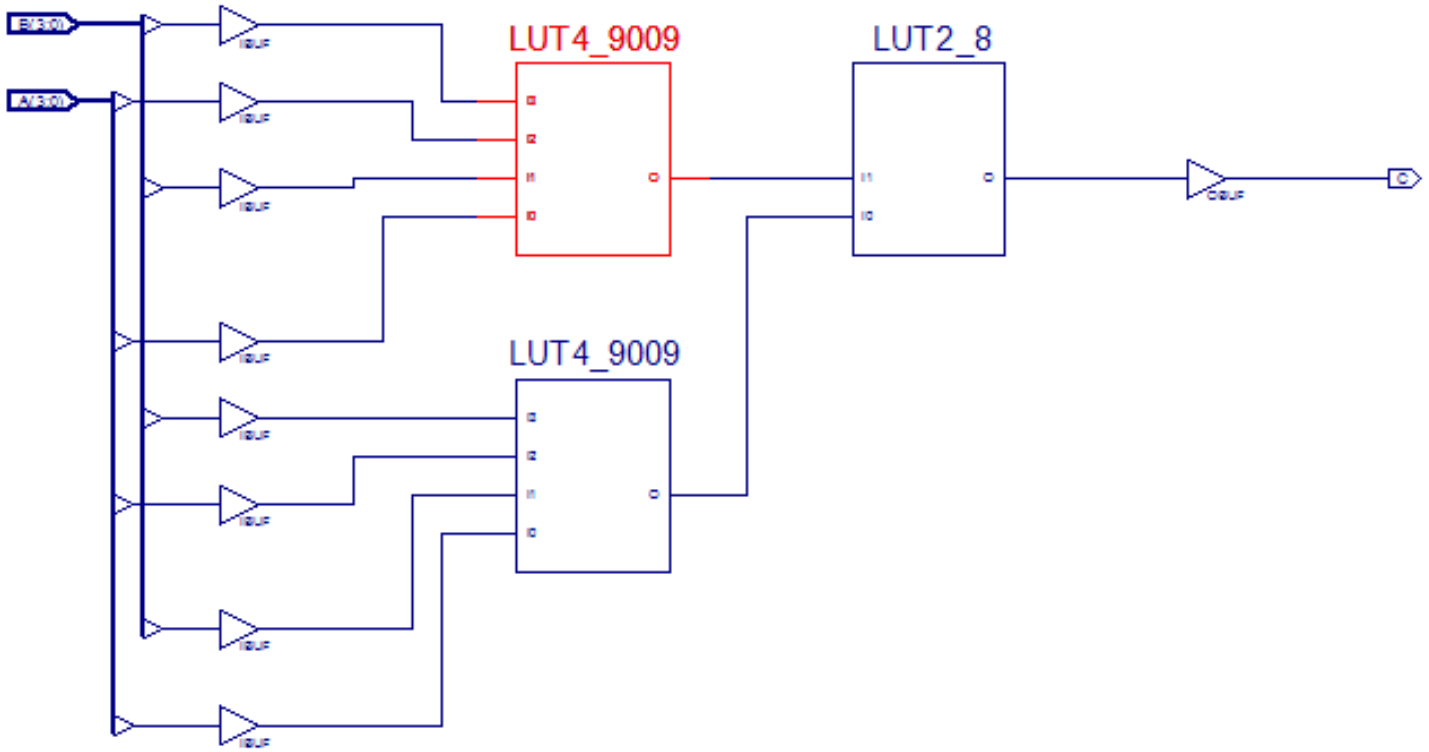
Kranugh map-*synthesis*



FPGA-ram based-*synthesis*

I3	I2	I1	I0	O
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

FPGA-ram based -*synthesis*



Device utilization –*Synthesis report*

Device utilization summary:

Selected Device : 3s1600efg320-5

Number of Slices:	2	out of 14752	0%
Number of 4 input LUTs:	3	out of 29504	0%
Number of bonded IOBs:	9	out of 250	3%

Timing -*Synthesis report*

Timing Summary:

Delay: 7.587ns (Levels of Logic = 4)

Source: A<1> (PAD)

Destination: C (PAD)

Data Path: A<1> to C

Cell:in->out	fan-out	**Delay**	**Gate Delay**	Logical	Name (Net Name)
IBUF:I->O	1	1.106	0.833		A_1_IBUF (A_1_IBUF)
LUT4:I0->O	1	0.612	0.833		C426 (C4_map33)
LUT2:I0->O	1	0.612	0.681		C454 (C_OBUF)
OBUF:I->O		2.910			C_OBUF (C)

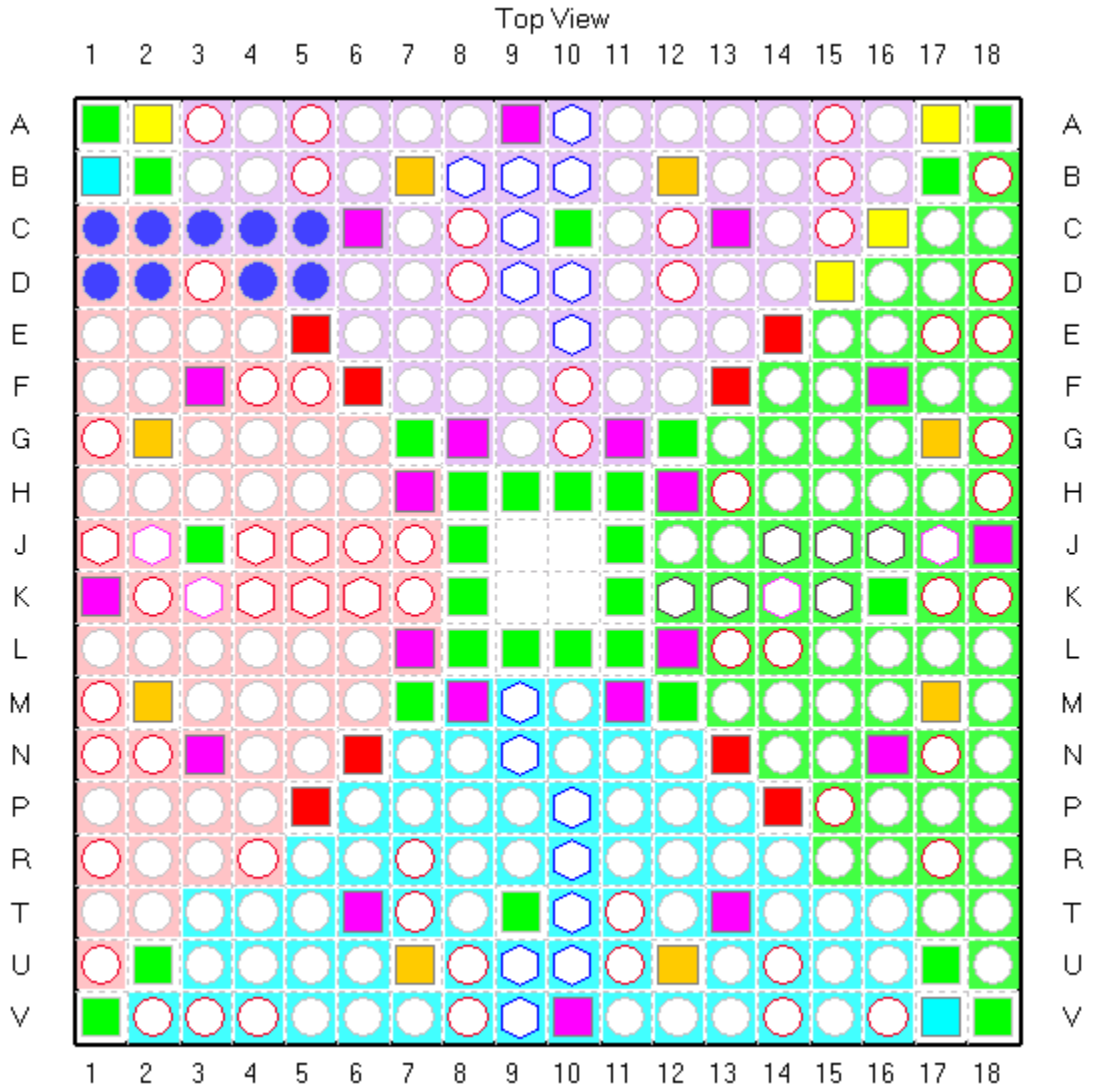
Total **7.587ns (5.240ns logic, 2.347ns route)**

69.1% logic, **30.9%** route

Assign package pin-*user constrains*

	I/O Name	I/O Direction	Loc
	A<0>	Input	C4
	A<1>	Input	D4
	A<2>	Input	C5
	A<3>	Input	D5
	B<0>	Input	C1
	B<1>	Input	D1
	B<2>	Input	C2
	B<3>	Input	D2
	C	Output	C3

Assign package pin-*user constrains*



mapping

Design Summary

Number of errors: 0

Number of warnings: 0

Logic Utilization:

Number of 4 input LUTs: 3 out of 29,504 1%

Logic Distribution:

Number of occupied Slices: 2 out of 14,752 1%

Number of Slices containing only related logic: 2 out of 2 100%

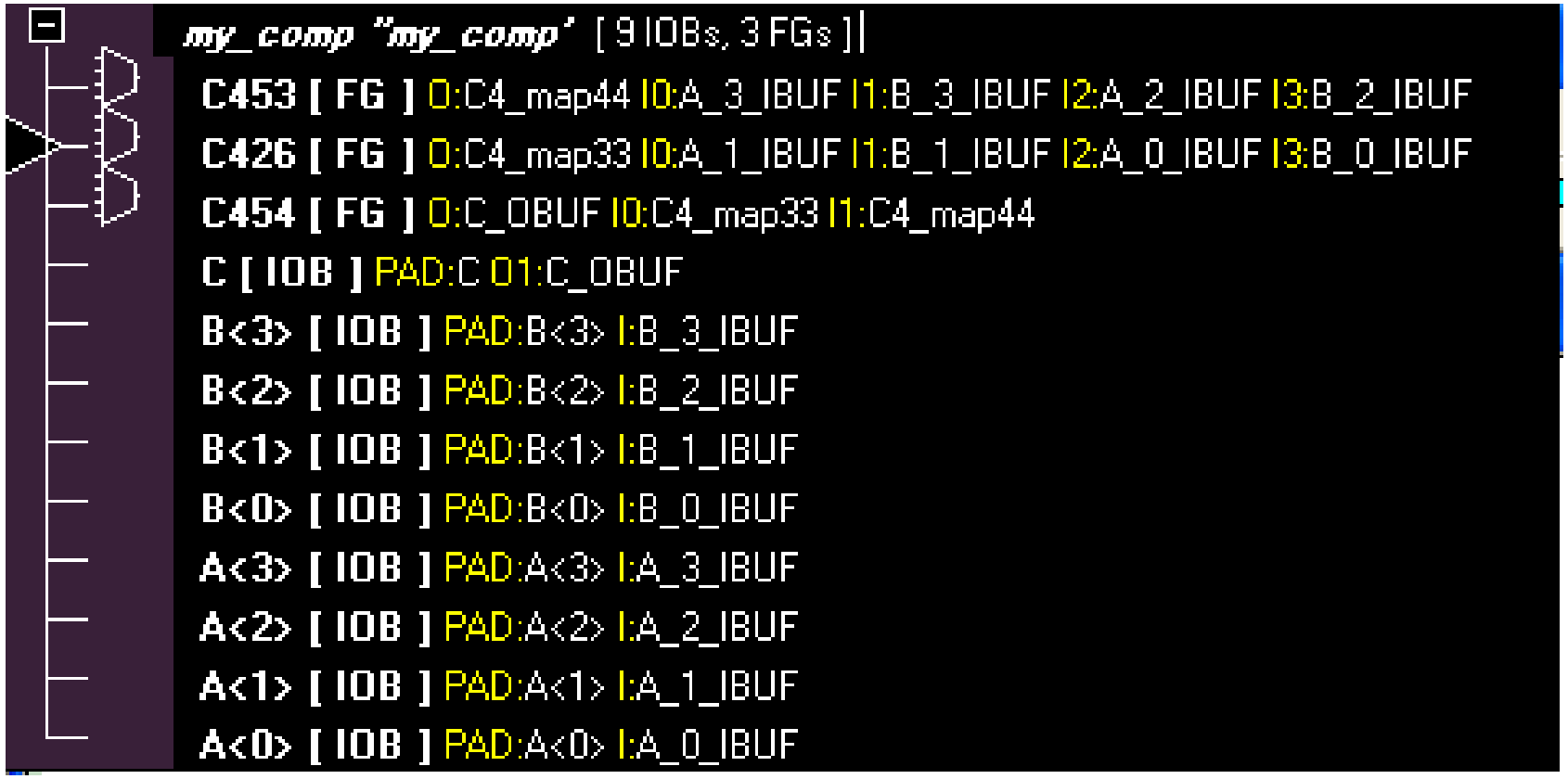
Number of Slices containing unrelated logic: 0 out of 2 0%

* See NOTES below for an explanation of the effects of unrelated logic

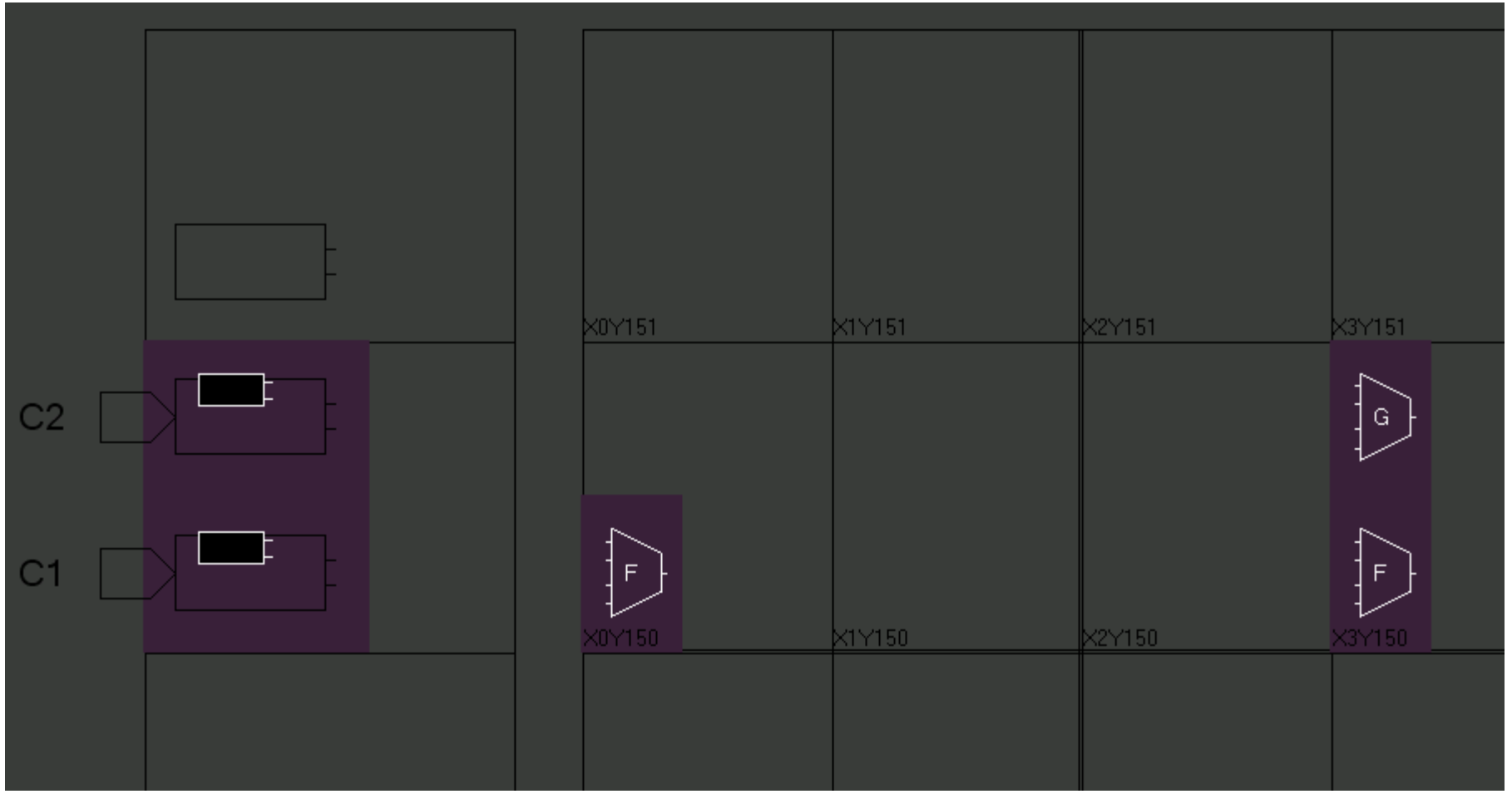
Total Number of 4 input LUTs: 3 out of 29,504 1%

Number of bonded IOBs: 9 out of 250 3%

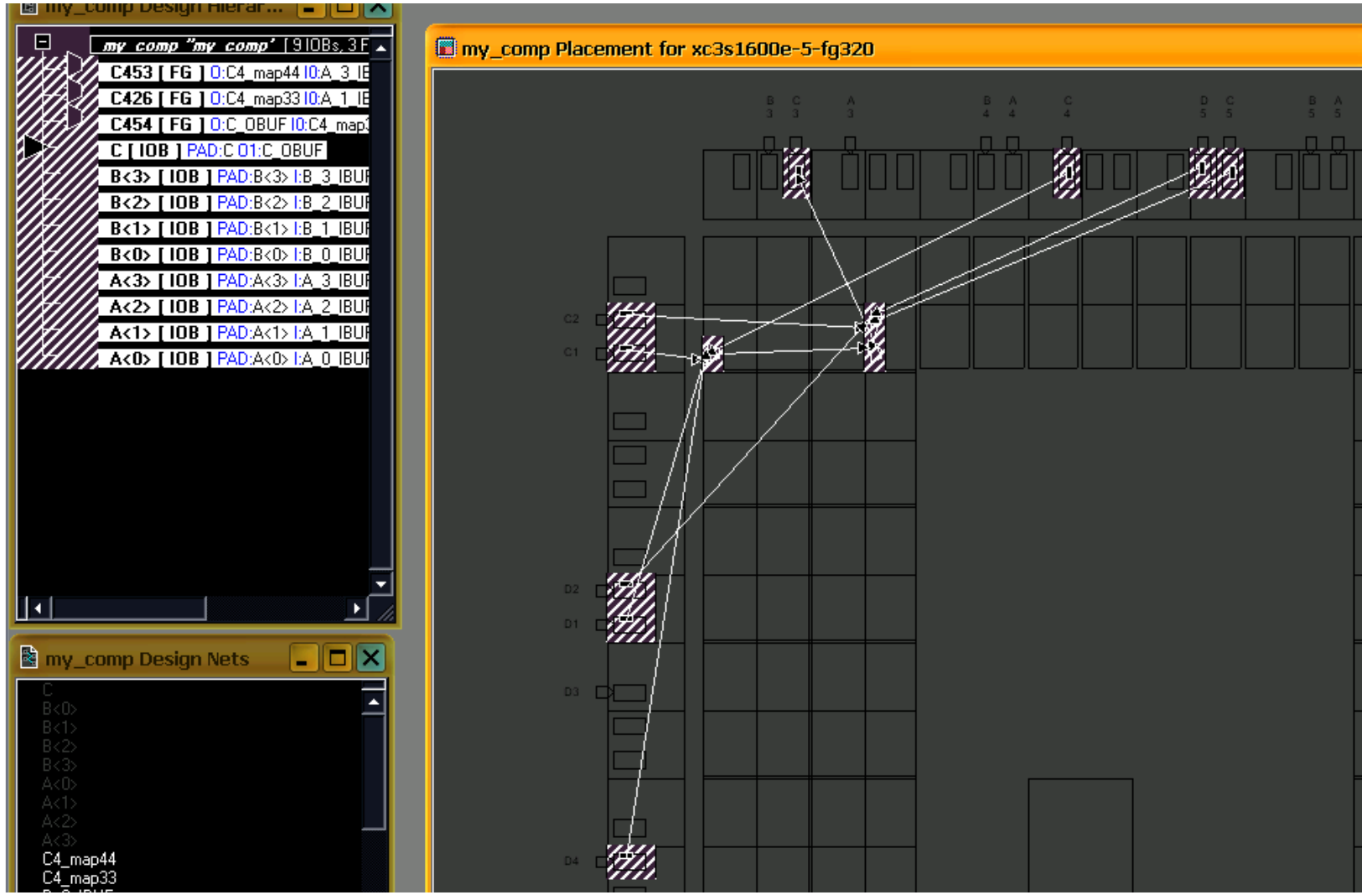
mapping


my_comp "my_comp" [9 IOBs, 3 FGs]
C453 [FG] O:C4_map44 I0:A_3_IBUF I1:B_3_IBUF I2:A_2_IBUF I3:B_2_IBUF
C426 [FG] O:C4_map33 I0:A_1_IBUF I1:B_1_IBUF I2:A_0_IBUF I3:B_0_IBUF
C454 [FG] O:C_OBUF I0:C4_map33 I1:C4_map44
C [IOB] PAD:C O1:C_OBUF
B<3> [IOB] PAD:B<3> I:B_3_IBUF
B<2> [IOB] PAD:B<2> I:B_2_IBUF
B<1> [IOB] PAD:B<1> I:B_1_IBUF
B<0> [IOB] PAD:B<0> I:B_0_IBUF
A<3> [IOB] PAD:A<3> I:A_3_IBUF
A<2> [IOB] PAD:A<2> I:A_2_IBUF
A<1> [IOB] PAD:A<1> I:A_1_IBUF
A<0> [IOB] PAD:A<0> I:A_0_IBUF

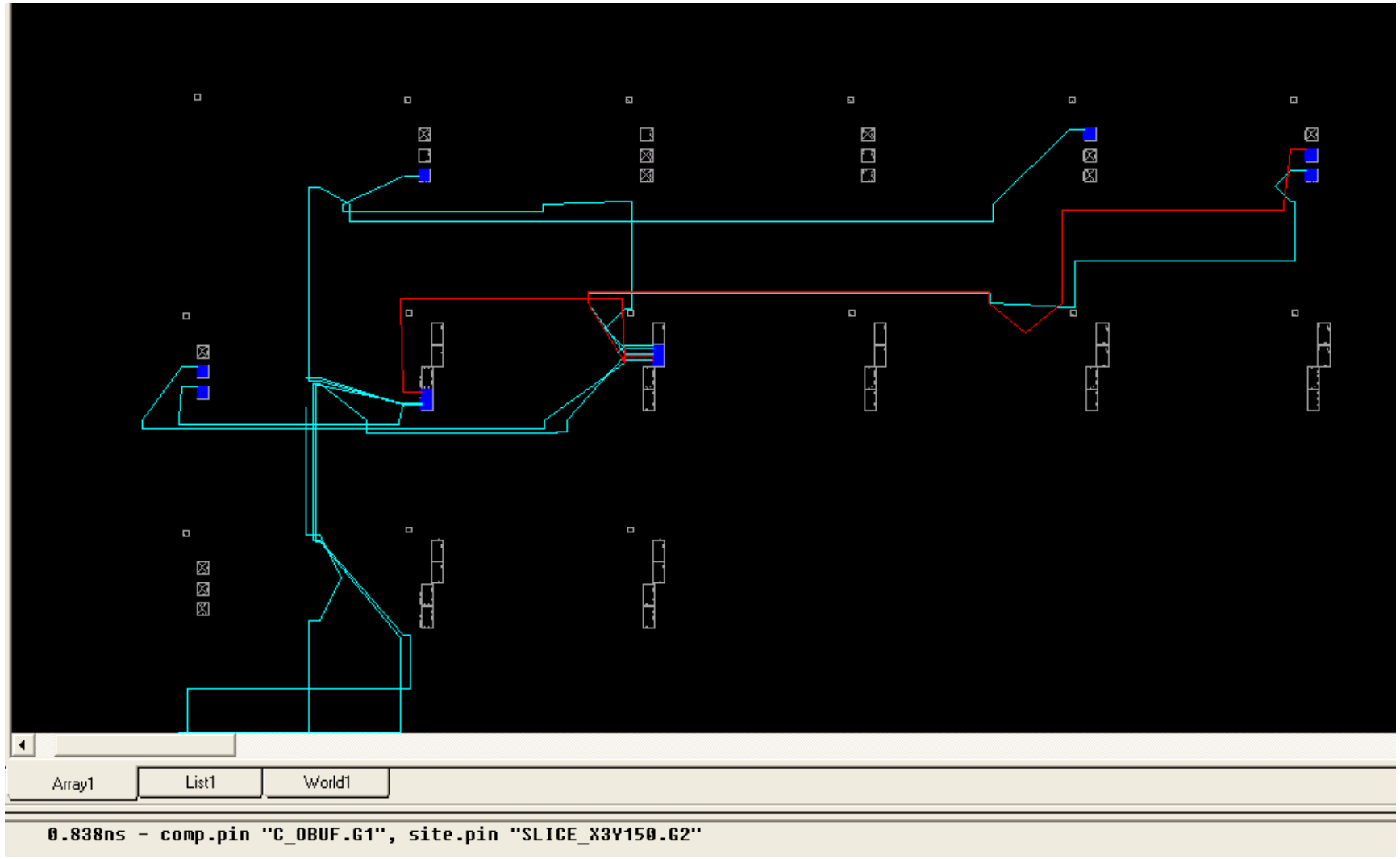
Placing


C2
C1
X0Y151
X1Y151
X2Y151
X3Y151
G
F
F
X0Y150
X1Y150
X2Y150
X3Y150

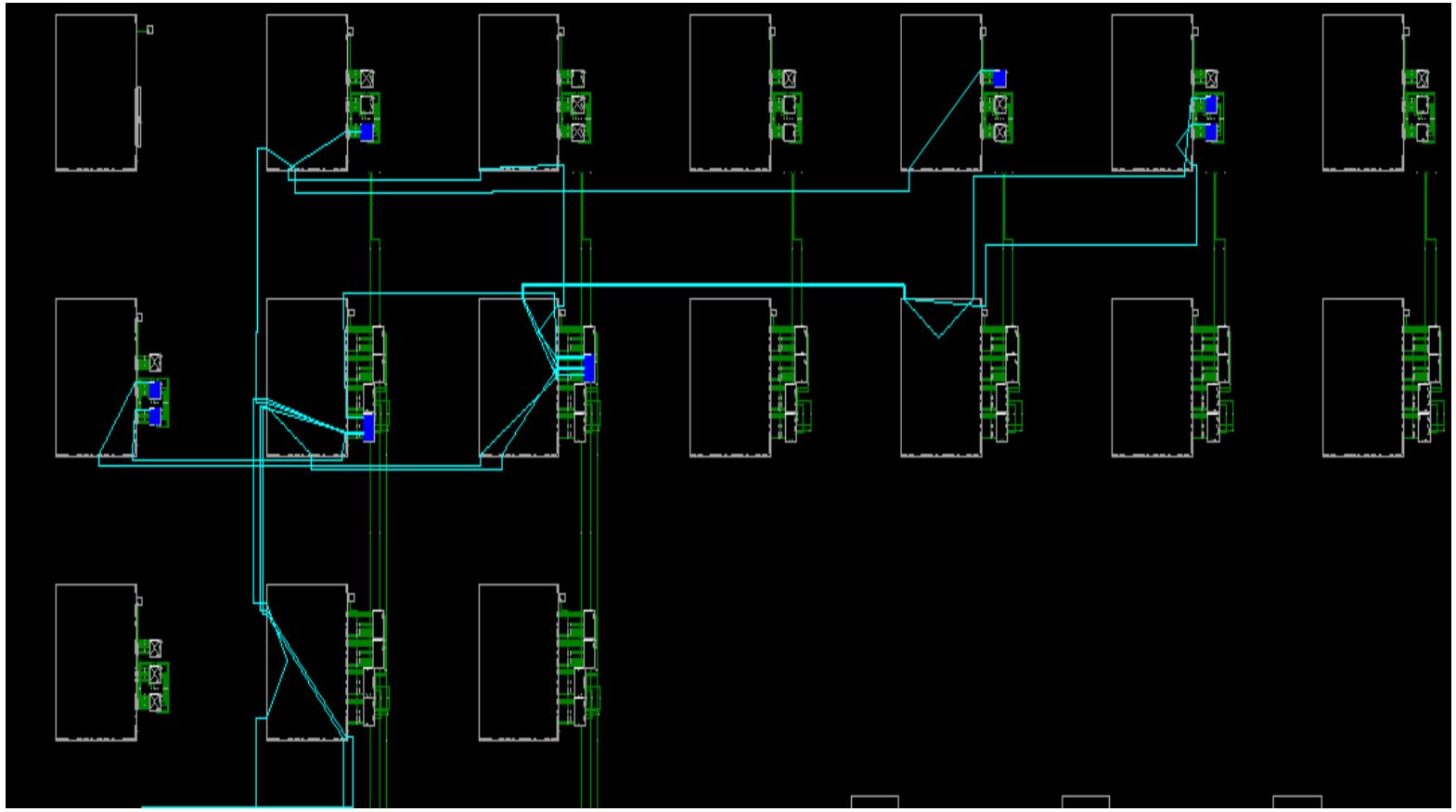
Placing


my_comp "my_comp" [9 IOBs, 3 F
C453 [FG] O:C4_map44 I0:A_3_IB
C426 [FG] O:C4_map33 I0:A_1_IB
C454 [FG] O:C_OBUF I0:C4_map
C [IOB] PAD:C O1:C_OBUF
B<3> [IOB] PAD:B<3> I:B_3_IBUF
B<2> [IOB] PAD:B<2> I:B_2_IBUF
B<1> [IOB] PAD:B<1> I:B_1_IBUF
B<0> [IOB] PAD:B<0> I:B_0_IBUF
A<3> [IOB] PAD:A<3> I:A_3_IBUF
A<2> [IOB] PAD:A<2> I:A_2_IBUF
A<1> [IOB] PAD:A<1> I:A_1_IBUF
A<0> [IOB] PAD:A<0> I:A_0_IBUF
my_comp Design Nets
C
B<0>
B<1>
B<2>
B<3>
A<0>
A<1>
A<2>
A<3>
C4_map44
C4_map33
my_comp Placement for xc3s1600e-5-fg320
C2
C1
D2
D1
D3
D4

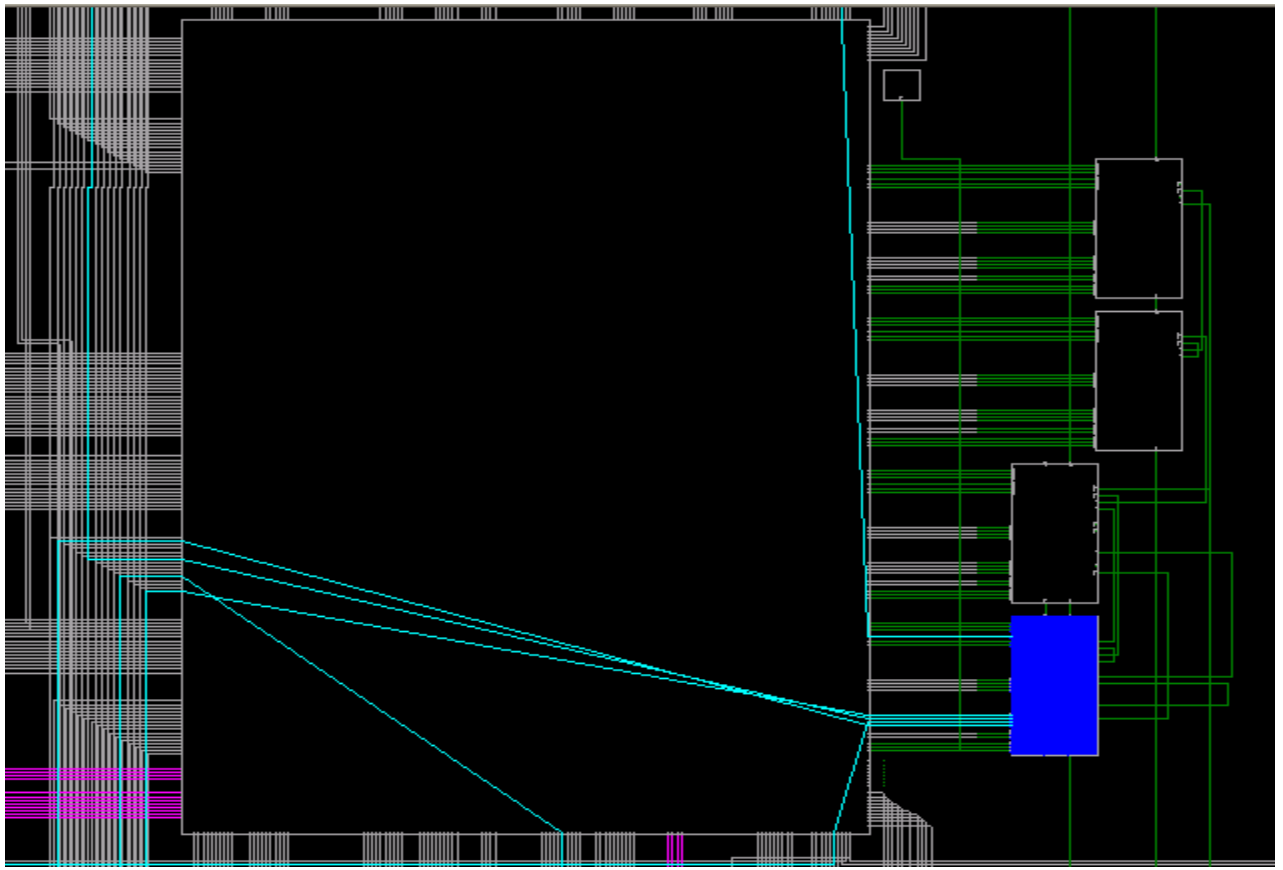
routing


Array1
List1
World1
0.838ns - comp.pin "C_OBUF.G1", site.pin "SLICE_X3Y150.G2"

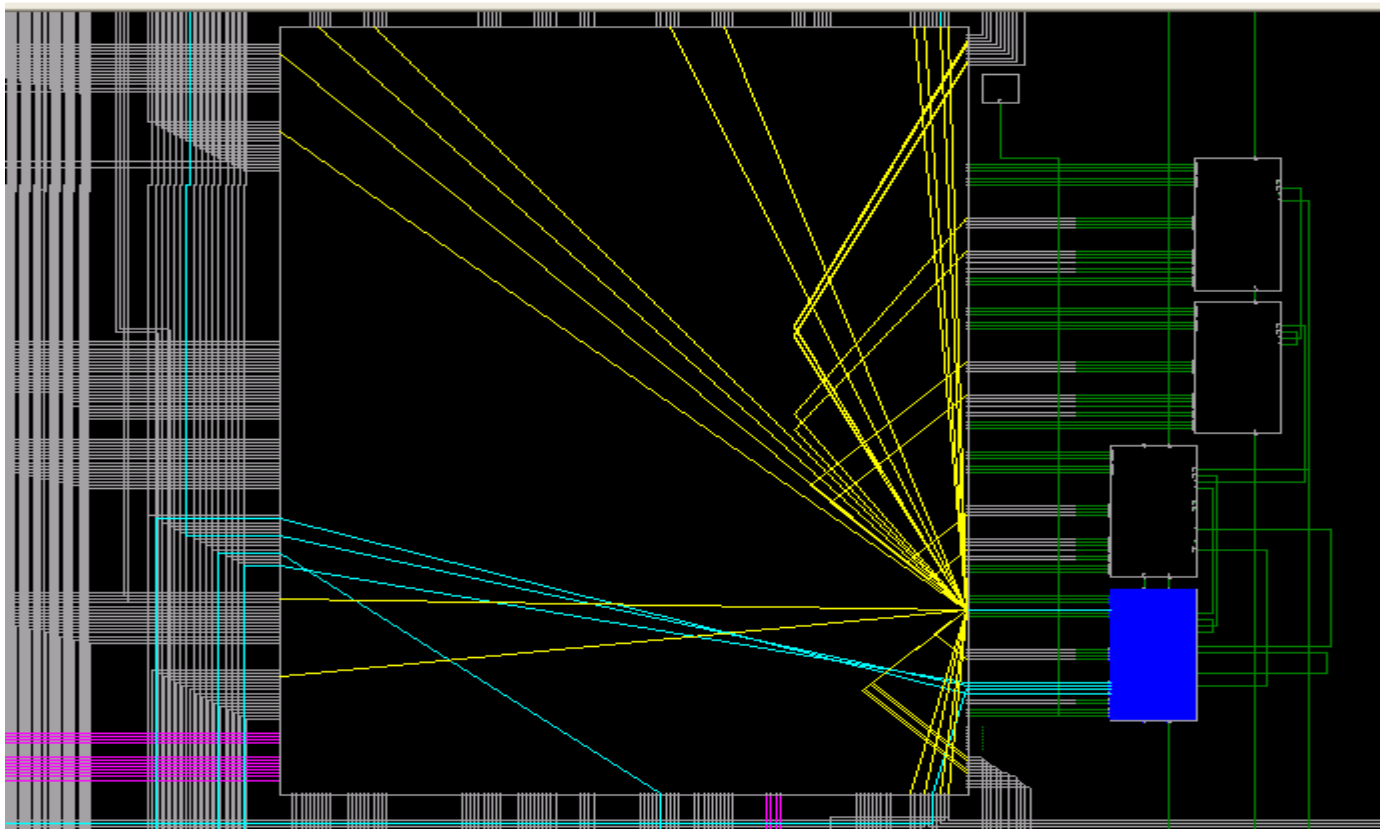
routing



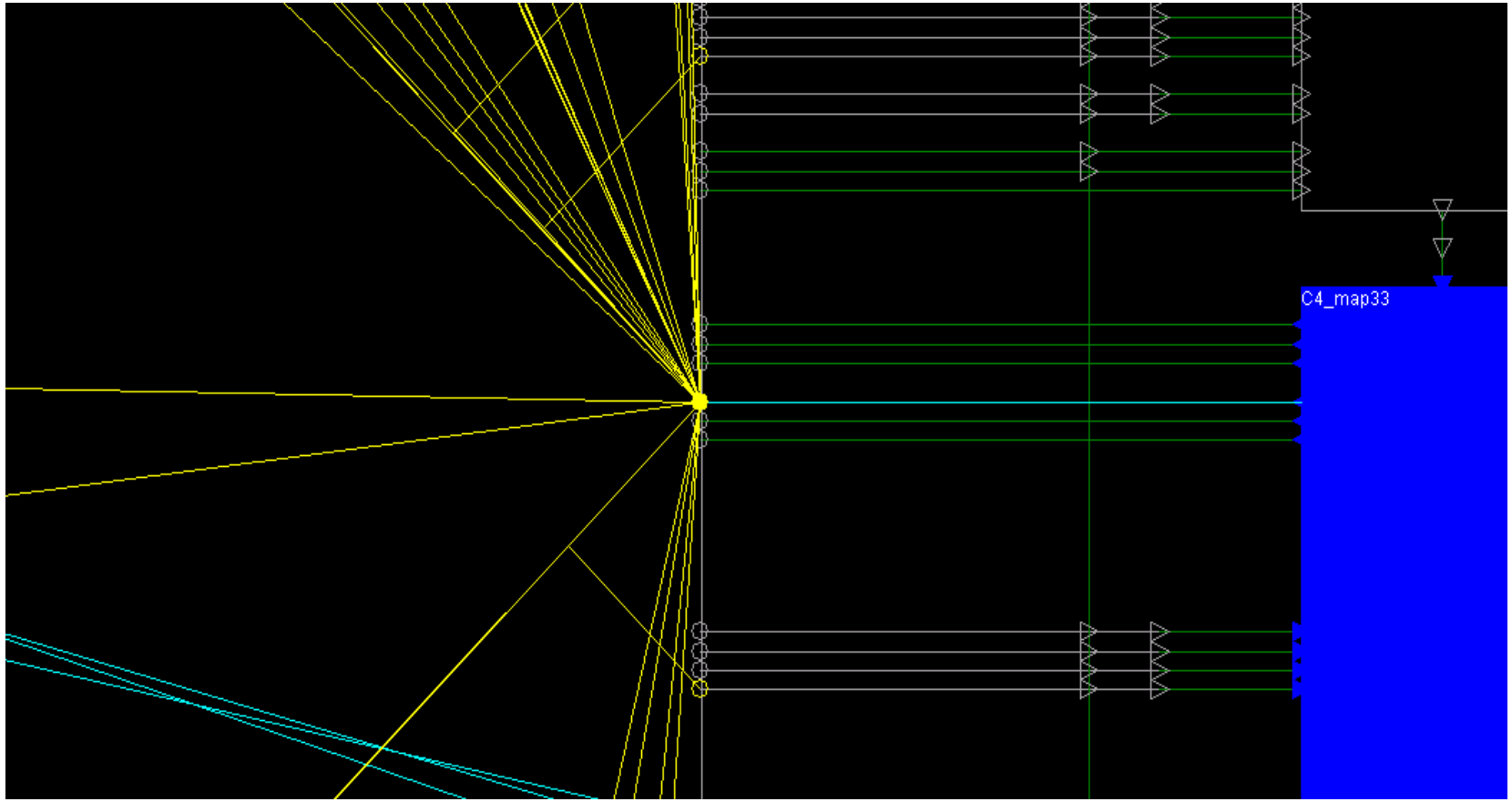
Switching matrix



Switching matrix-optional connections



Switching matrix-optional connections zoom in

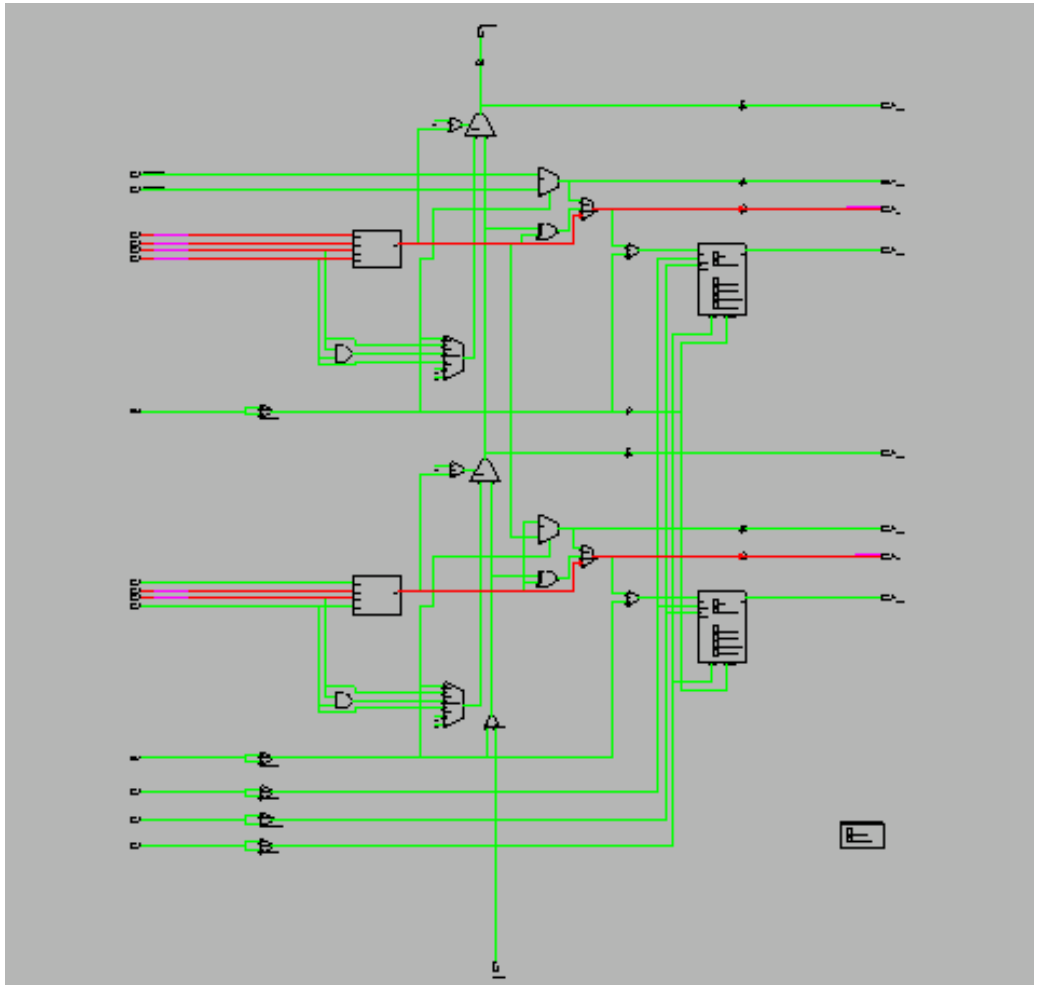


Delay report

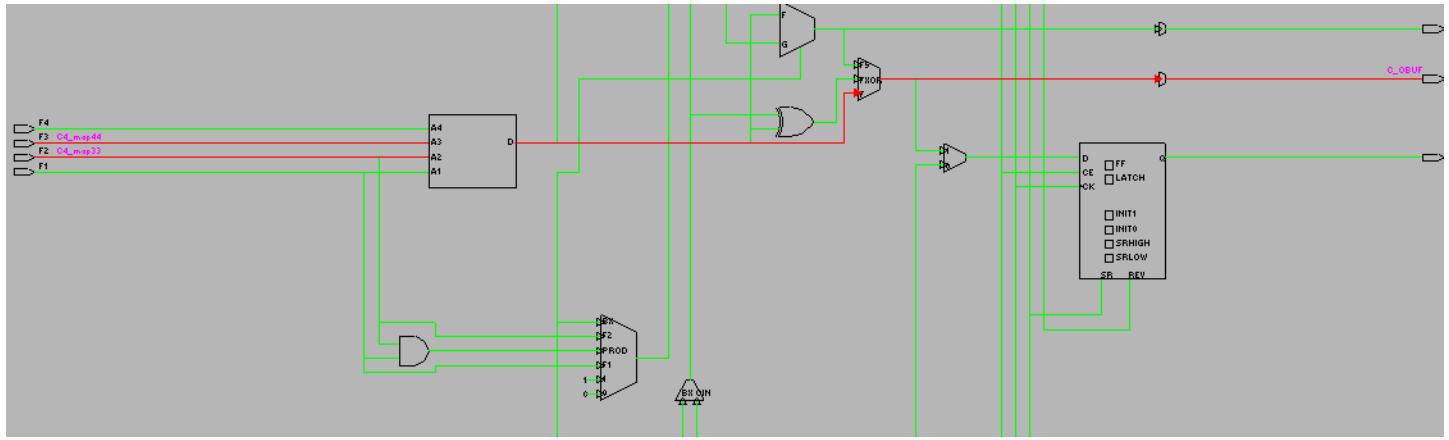
The 20 worst nets by delay are:

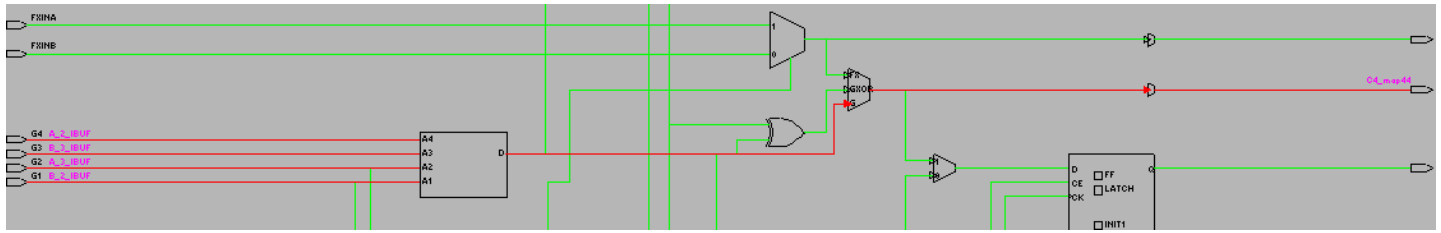
Max Delay	Net name
0.838	A_3_IBUF
0.794	A_1_IBUF
0.770	B_3_IBUF
0.653	B_2_IBUF
0.551	A_2_IBUF
0.538	A_0_IBUF
0.513	C_OBUF
0.491	B_1_IBUF
0.372	C4_map33
0.328	B_0_IBUF
0.020	C4_map44

Routing-zoom in



Routing-zoom in





RTL CODE

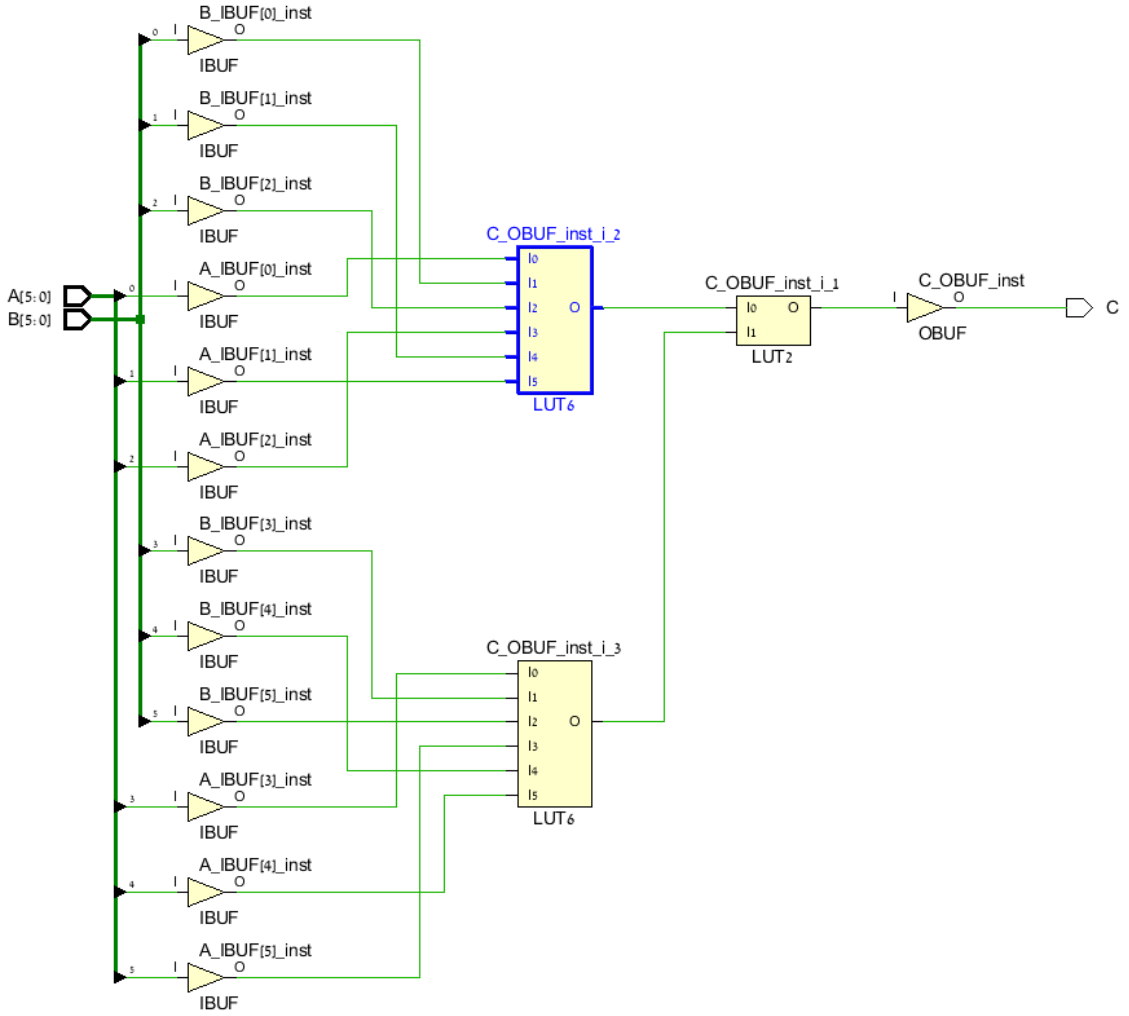
```
entity BH_MUX is
    Port ( A : in STD_LOGIC_VECTOR (5 downto 0);
           B : in STD_LOGIC_VECTOR (5 downto 0);
           C : out STD_LOGIC);
end BH_MUX;

architecture Behavioral of BH_MUX is

begin
process(a,b)
  begin
      if a=b then
           c<='1';
      else
          c <='0';
      end if ;
end process;

end Behavioral;
```

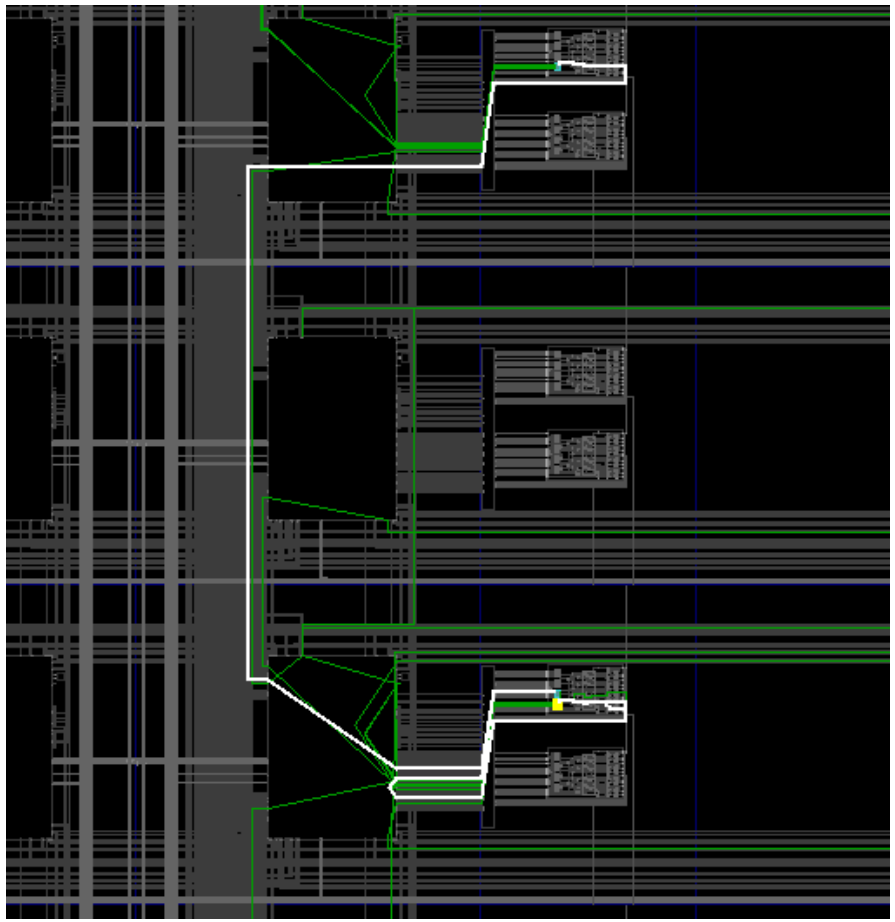
Synthesis

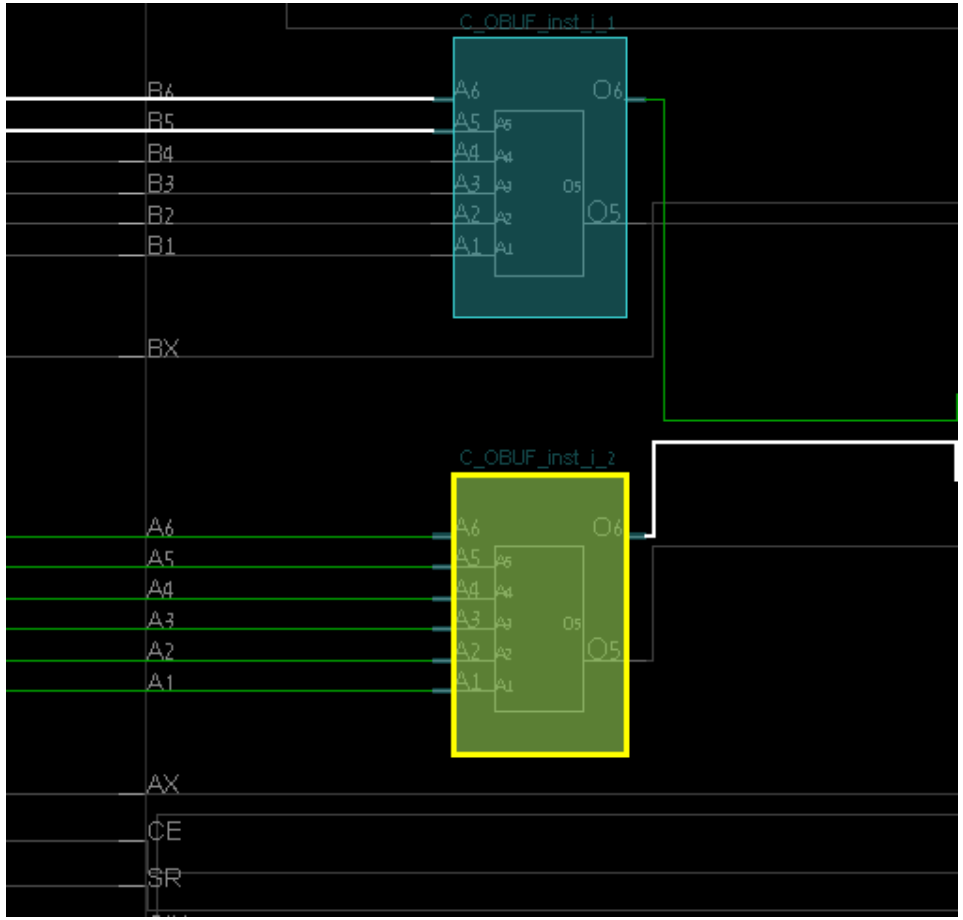
I5	I4	I3	I2	I1	I0	O=!I0 & !I1 & !I2 & !
0	0	0	0	0	0	1
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	1
0	0	1	1	0	1	0
0	0	1	1	1	0	0
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	0
0	1	0	1	0	1	0
0	1	0	1	1	0	0
0	1	0	1	1	1	0
0	1	1	0	0	0	0
0	1	1	0	0	1	0
0	1	1	0	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	0

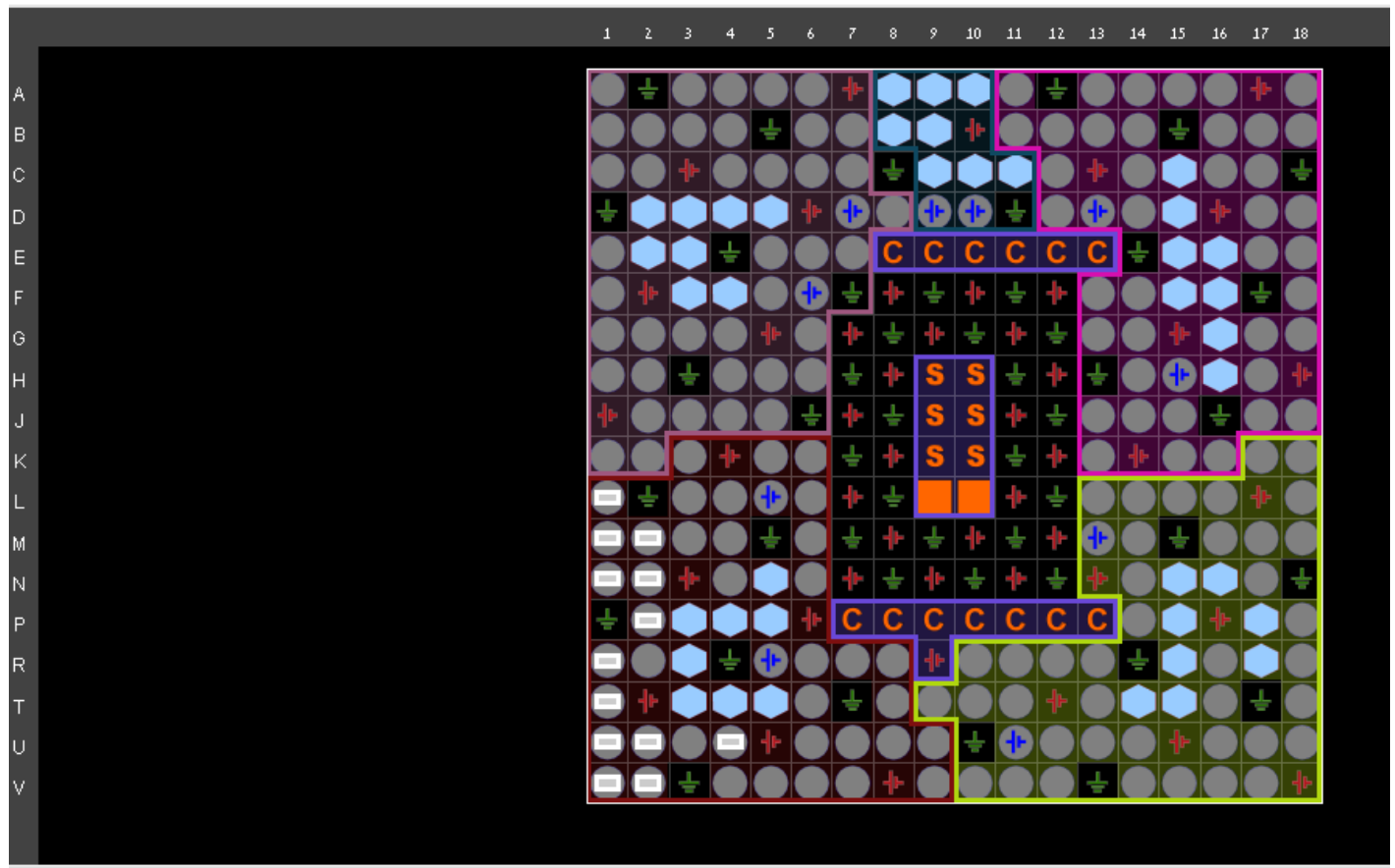
Edit LUT Equation...

ver Nets Cell Pins **Truth Table**

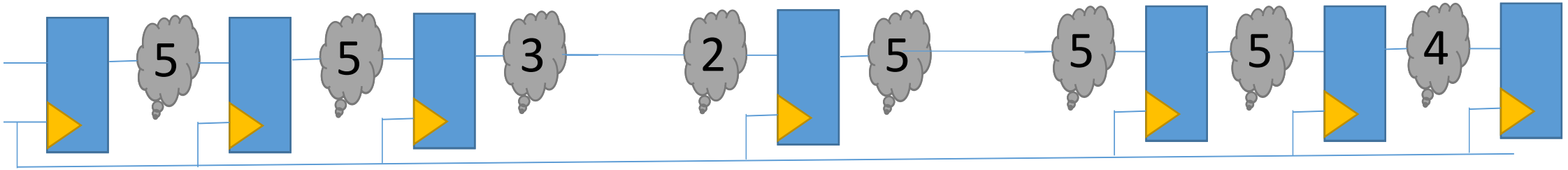





C_OBUF_inst_i_1
B6
B5
B4
B3
B2
B1
BX
A6
O6
A5
A4
A3
O5
A2
A1
C_OBUF_inst_i_2
A6
A5
A4
A3
A2
A1
AX
CE
SR

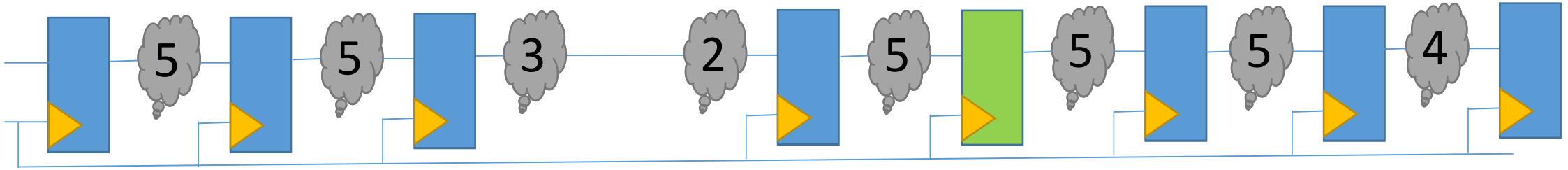

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
A B C D E F G H J K L M N P R T U V
C C C C C C
S S
S S
S S
C C C C C C C

RTL –Register Transfer Level

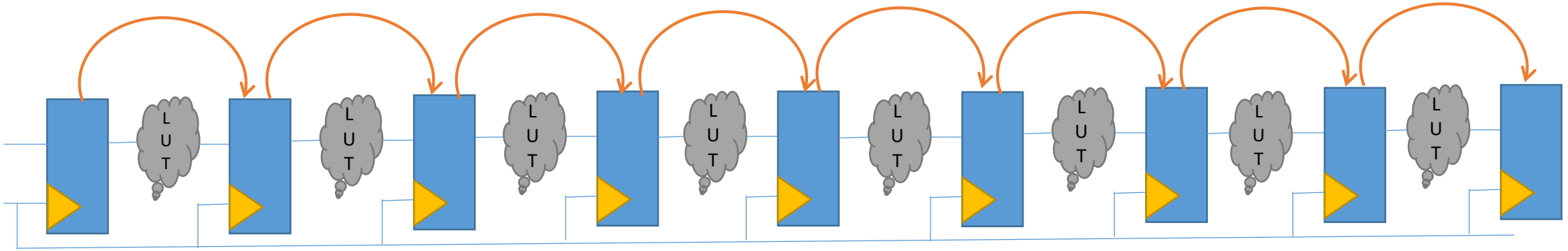


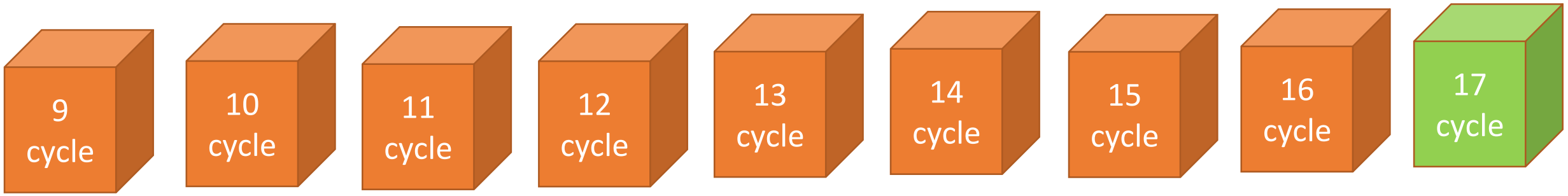
FMAX=1/ MAX DELAY=100 MHZ

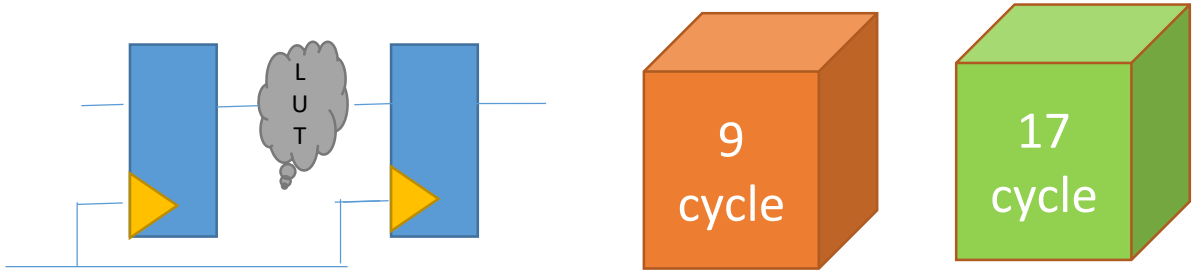
FMAX=1/ MAX DELAY=200 MHZ



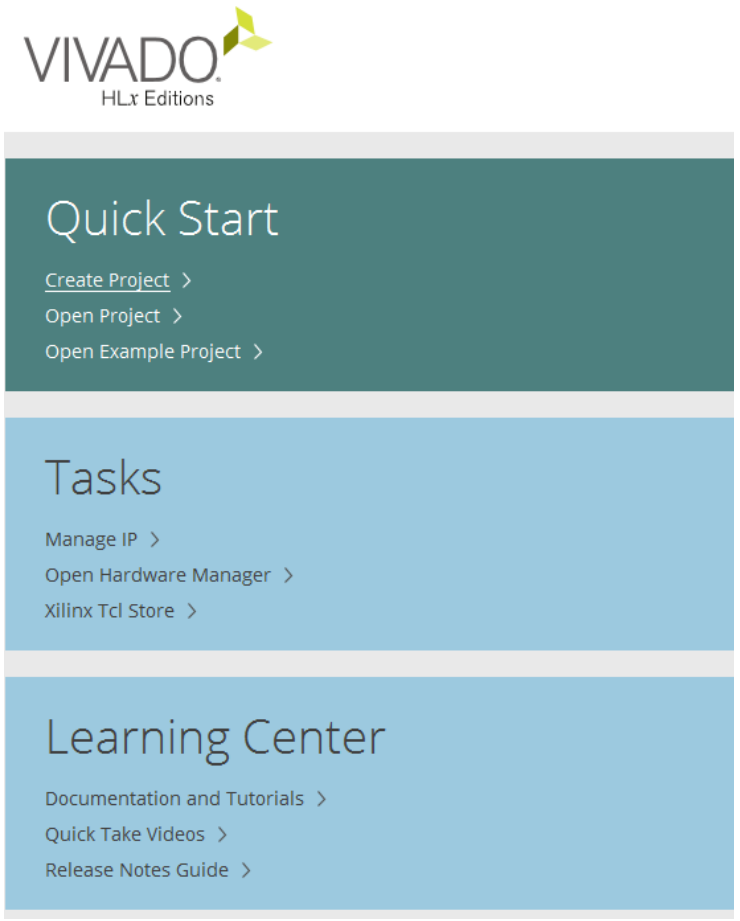
PARALLEL PROCESSING VERSUS SERIAL PROCESSING



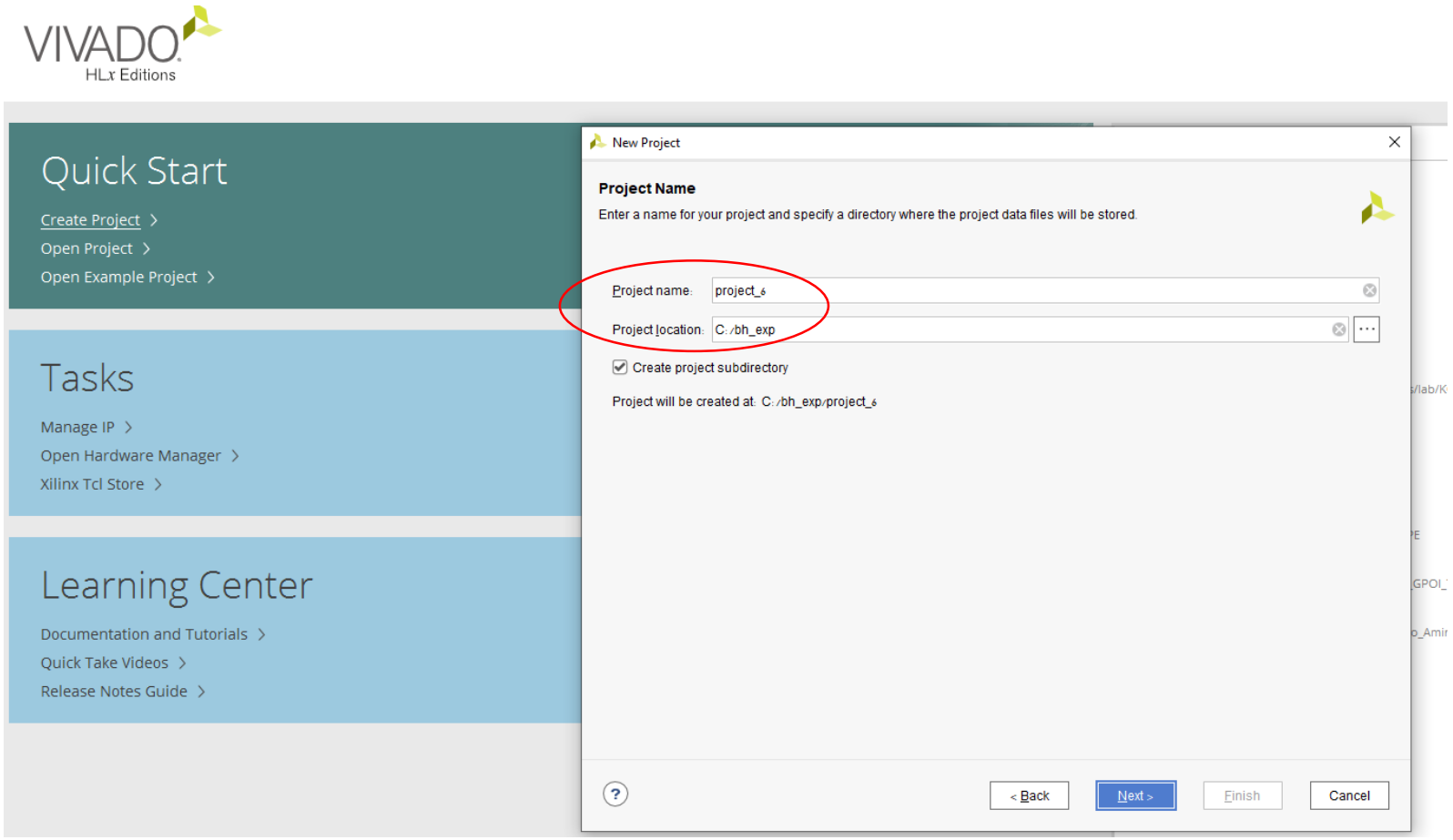




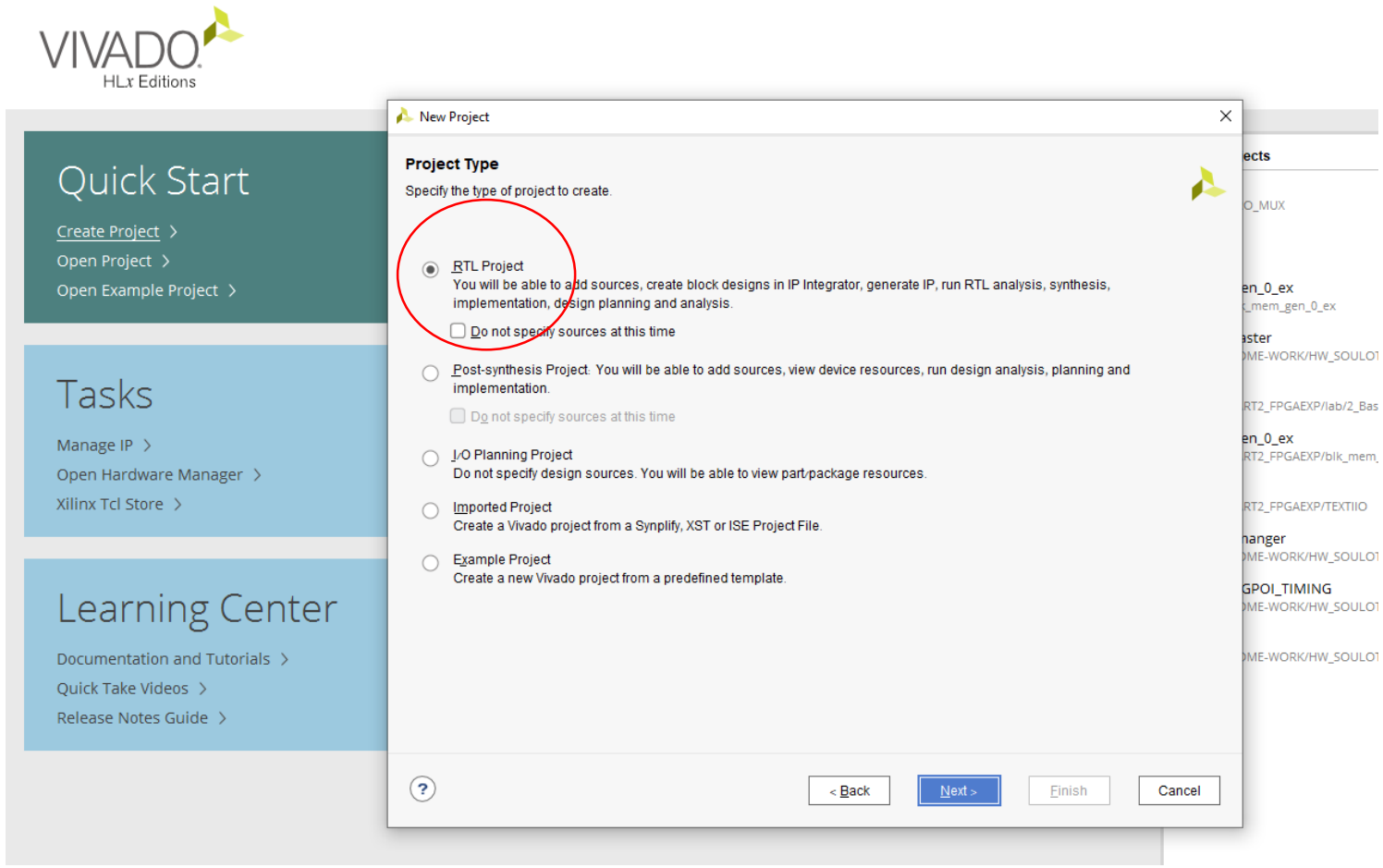
Create project



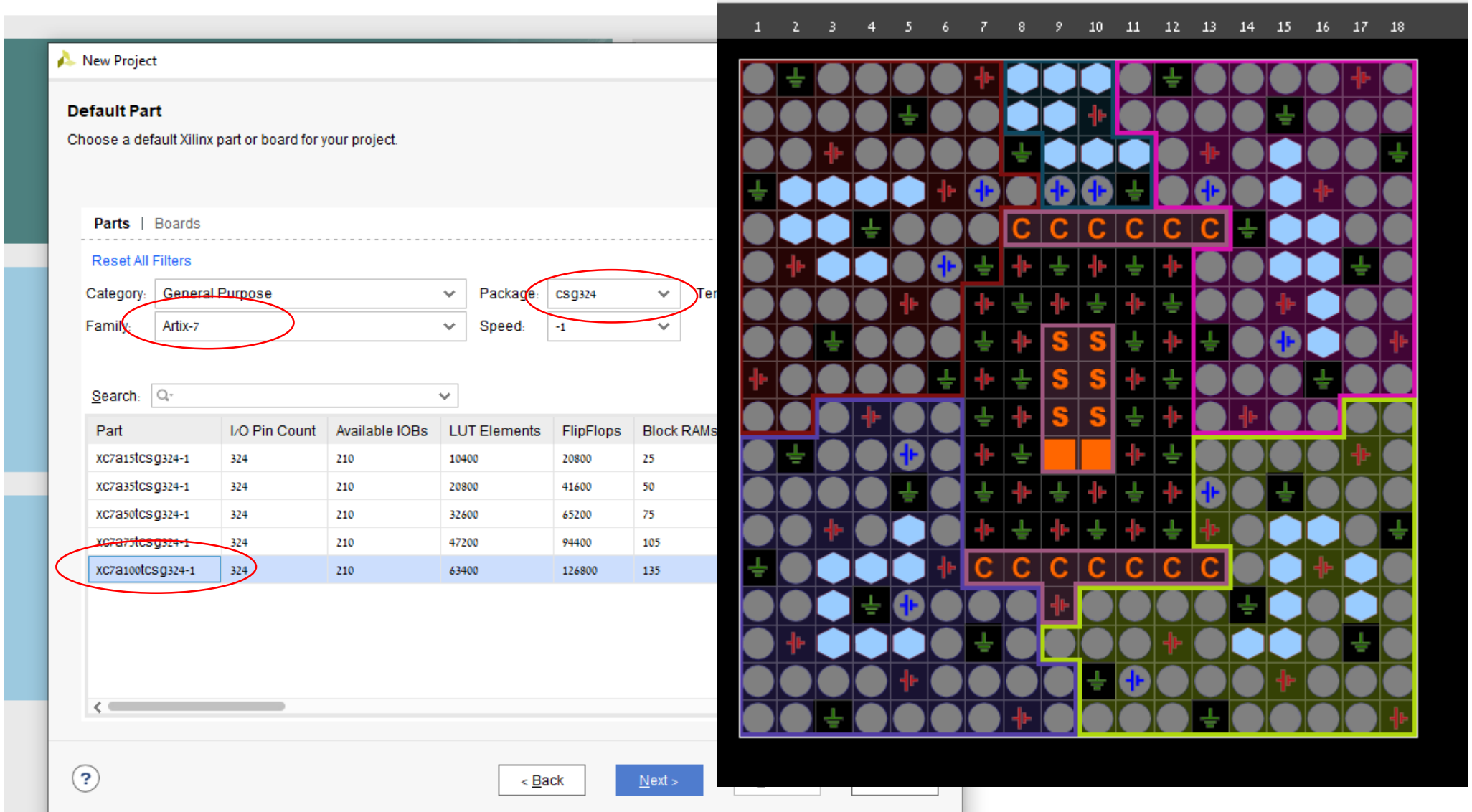
Create project –name & path not in Hebrew!!



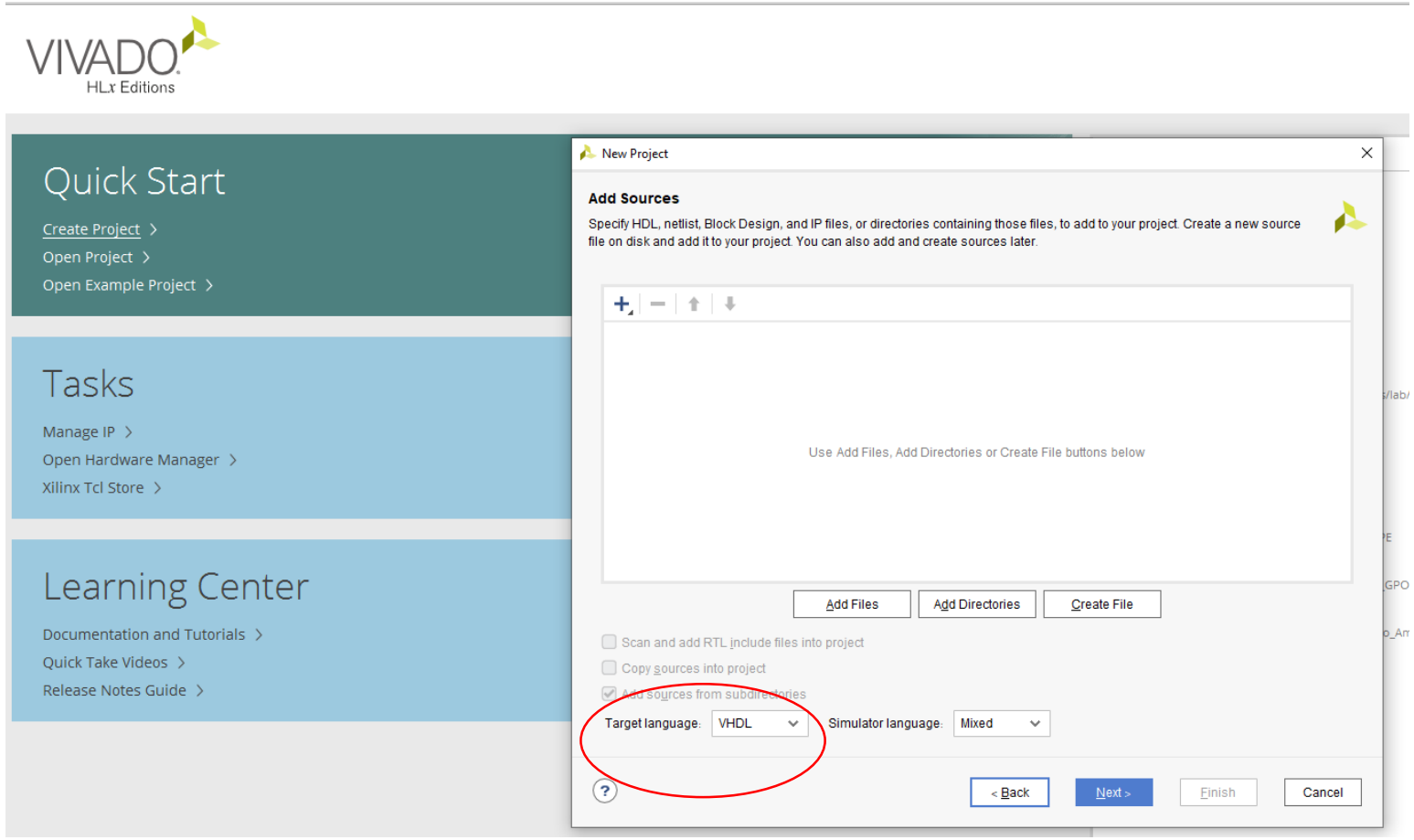
Create project –RTL project



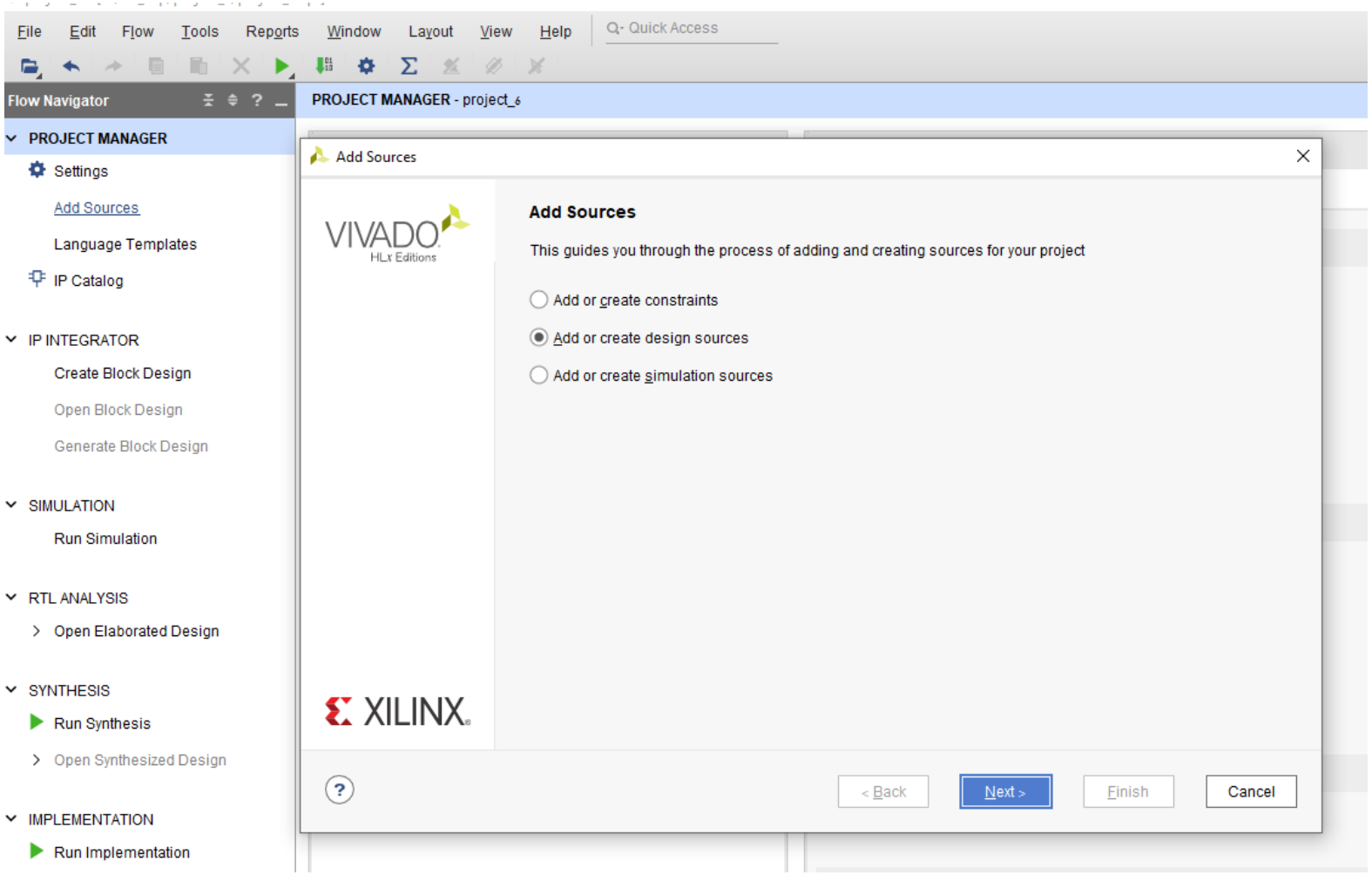
Create project –FPGA choosing



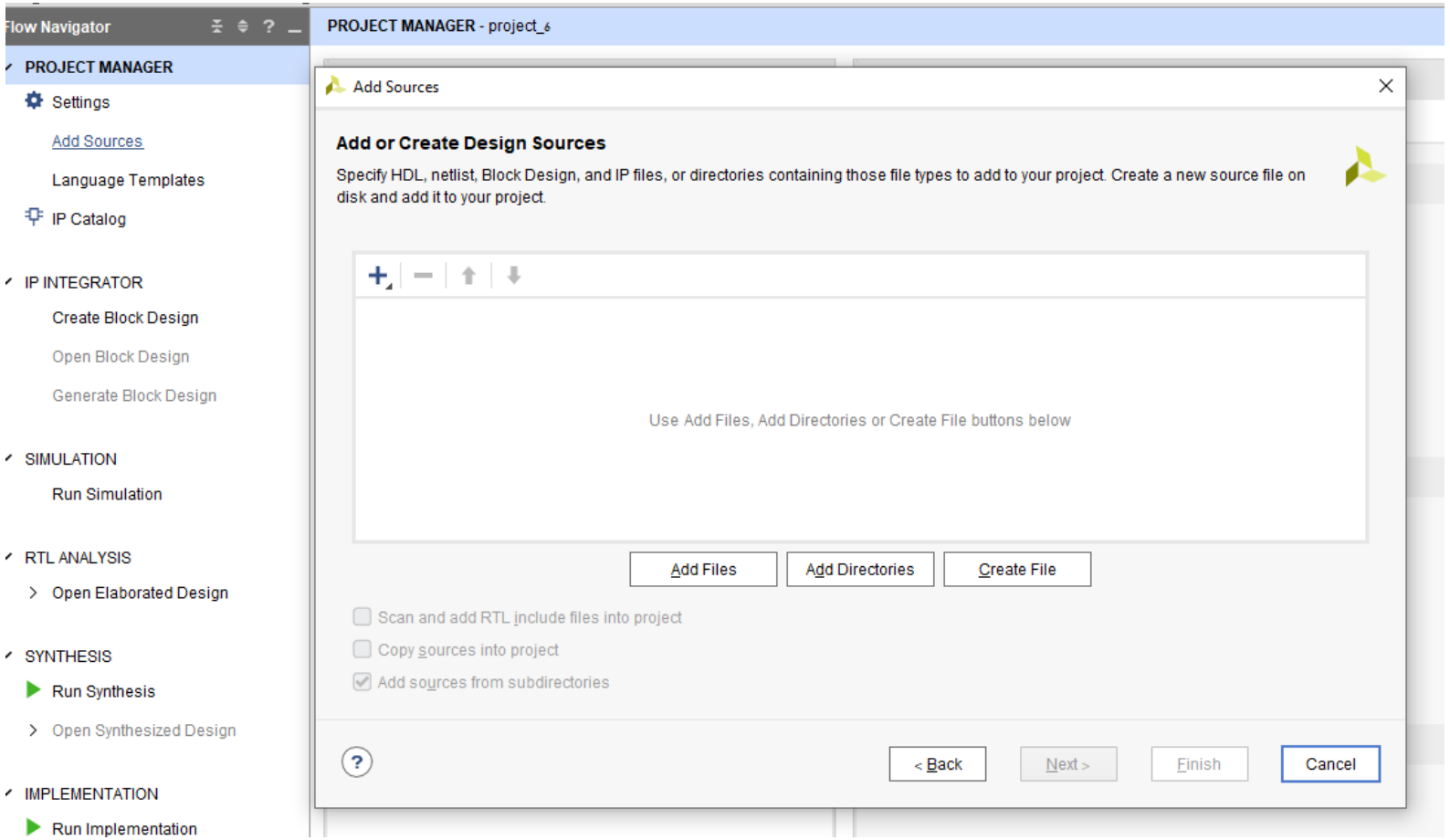
Create project –next …next .next…



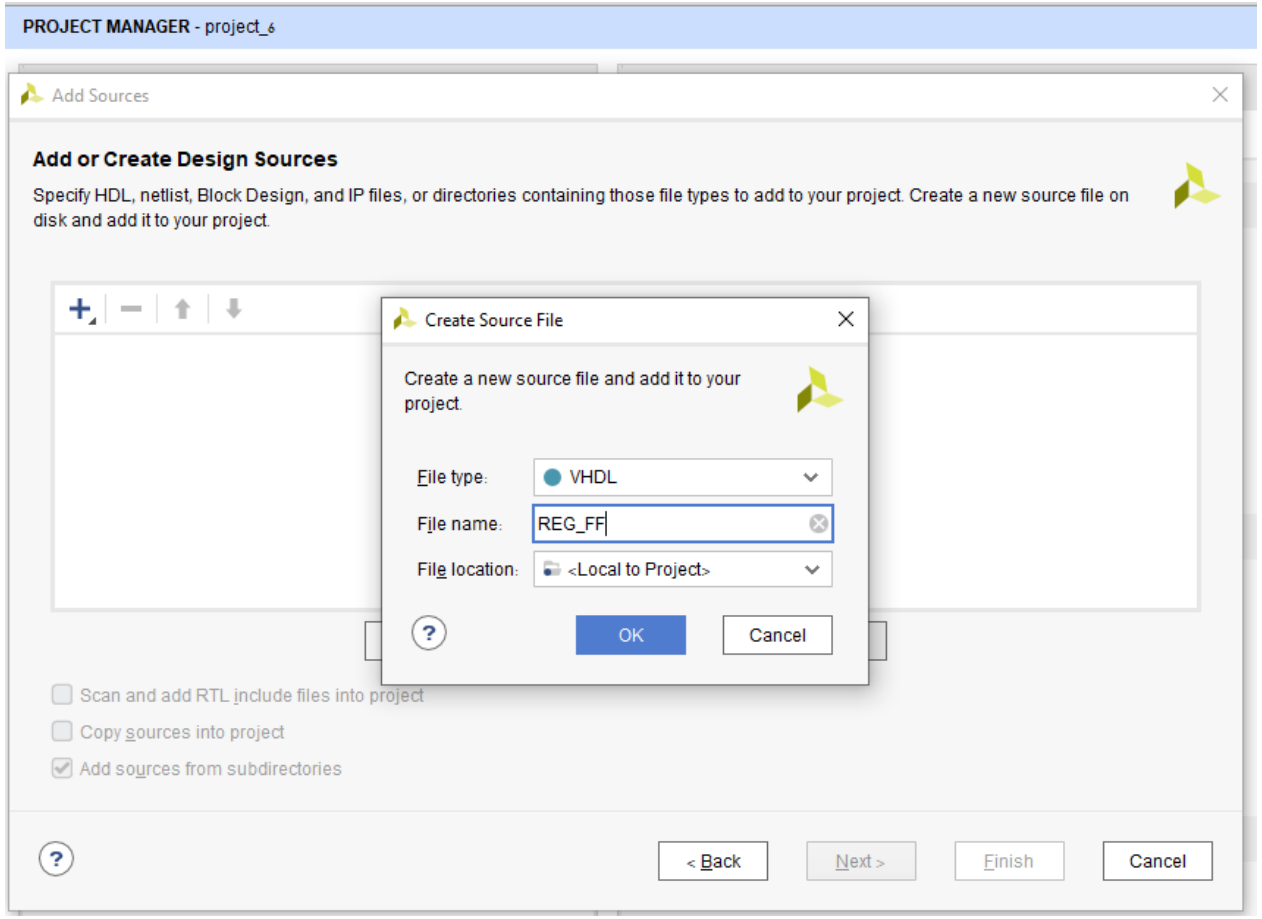
Adding source



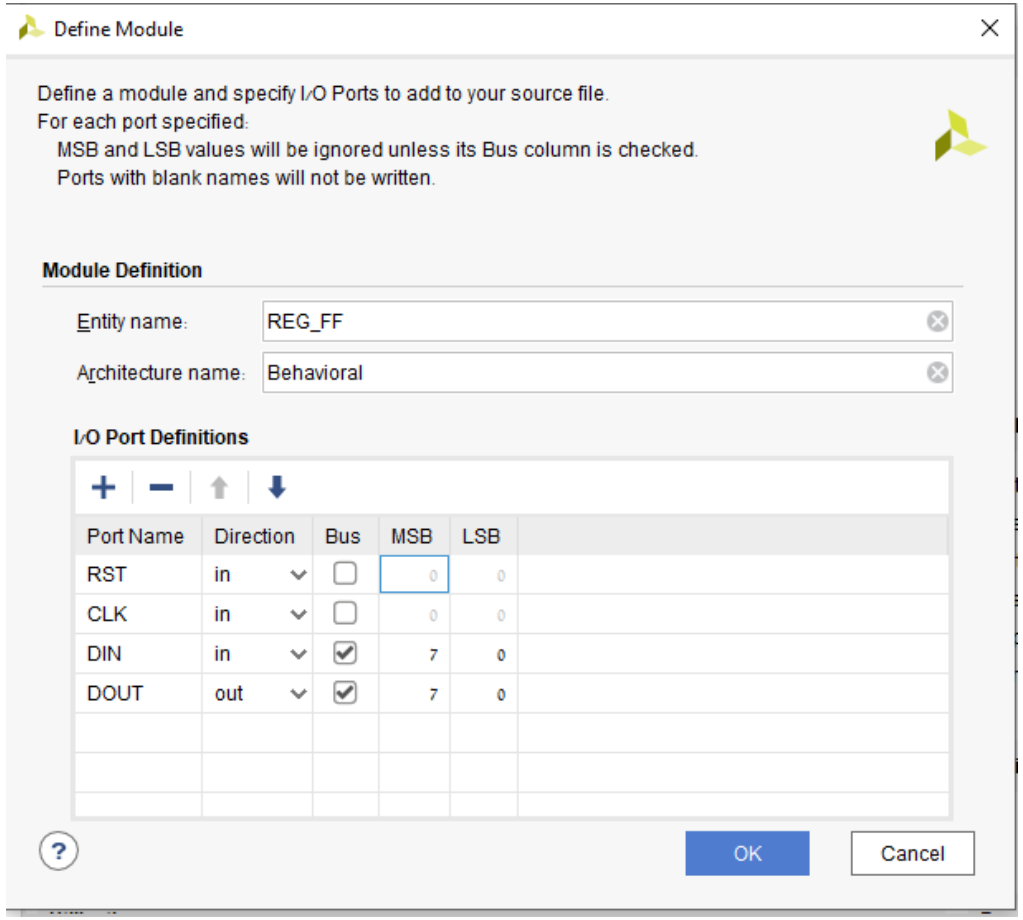
Create files



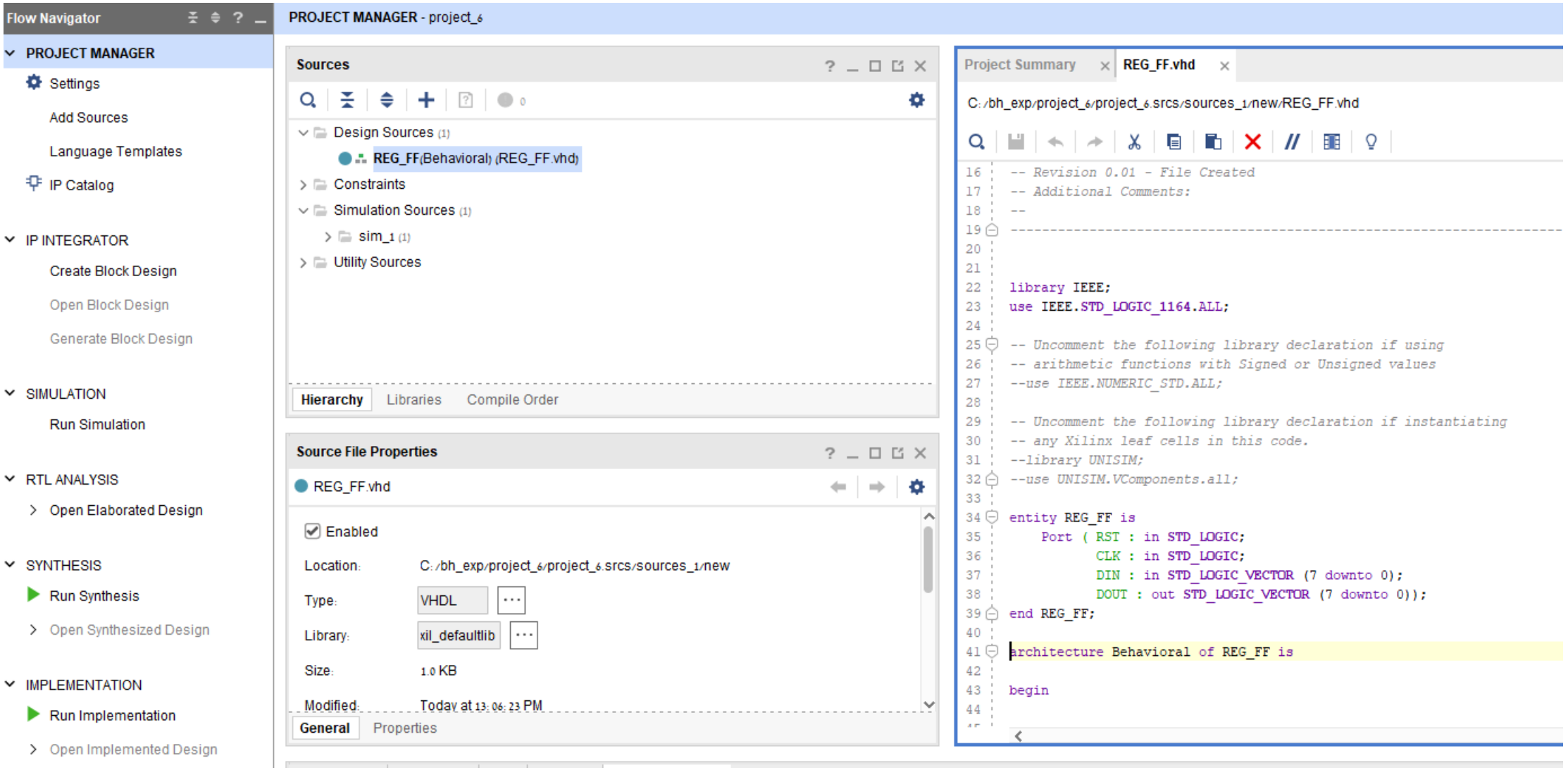
Create sources files



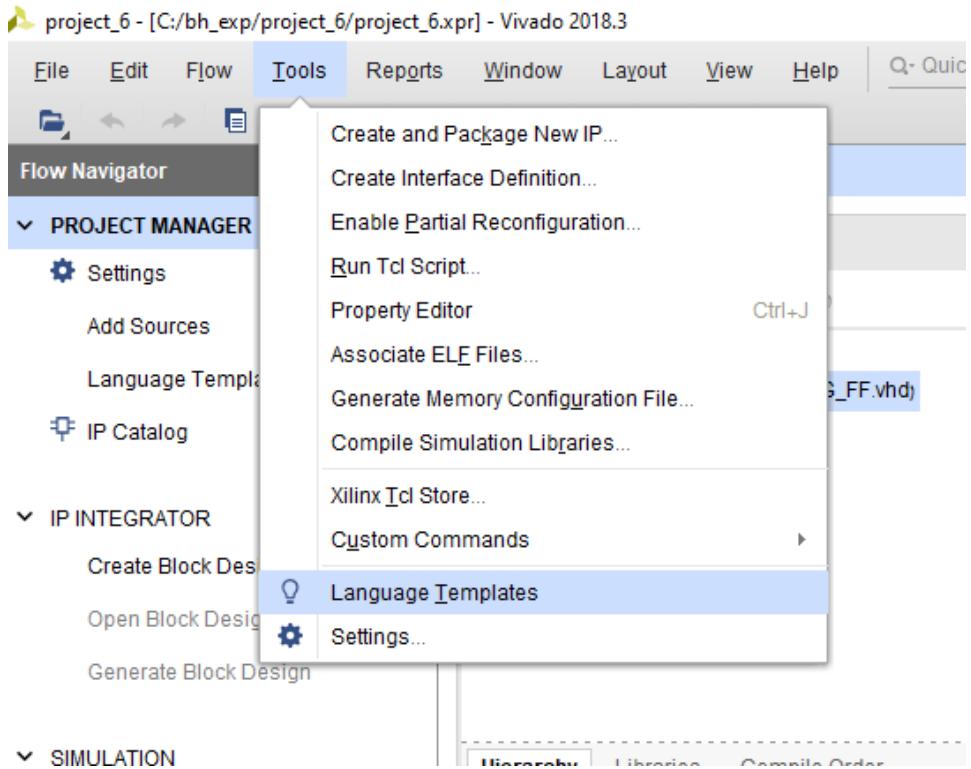
Create sources files –Entity Definition

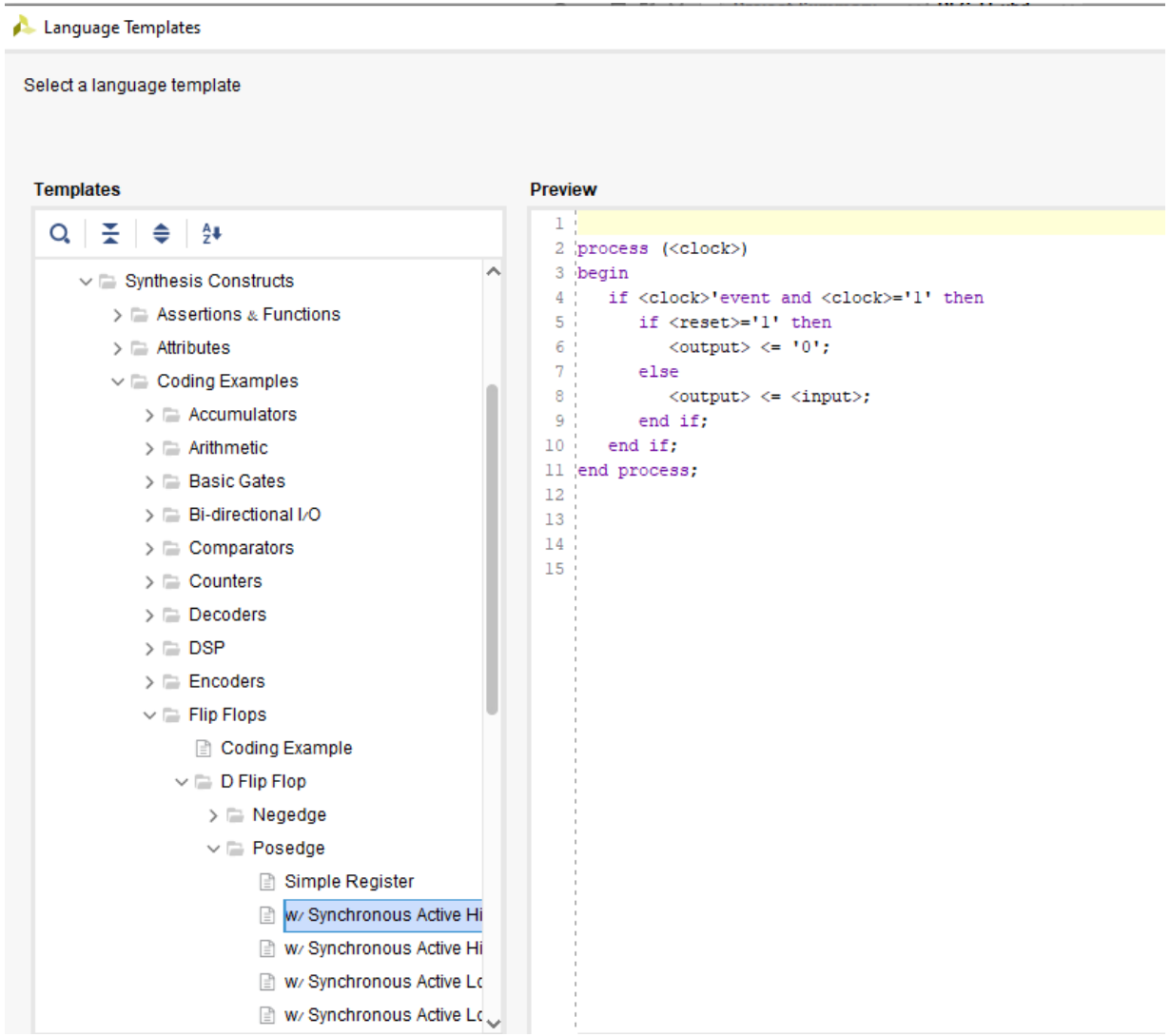


Create sources files –Entity

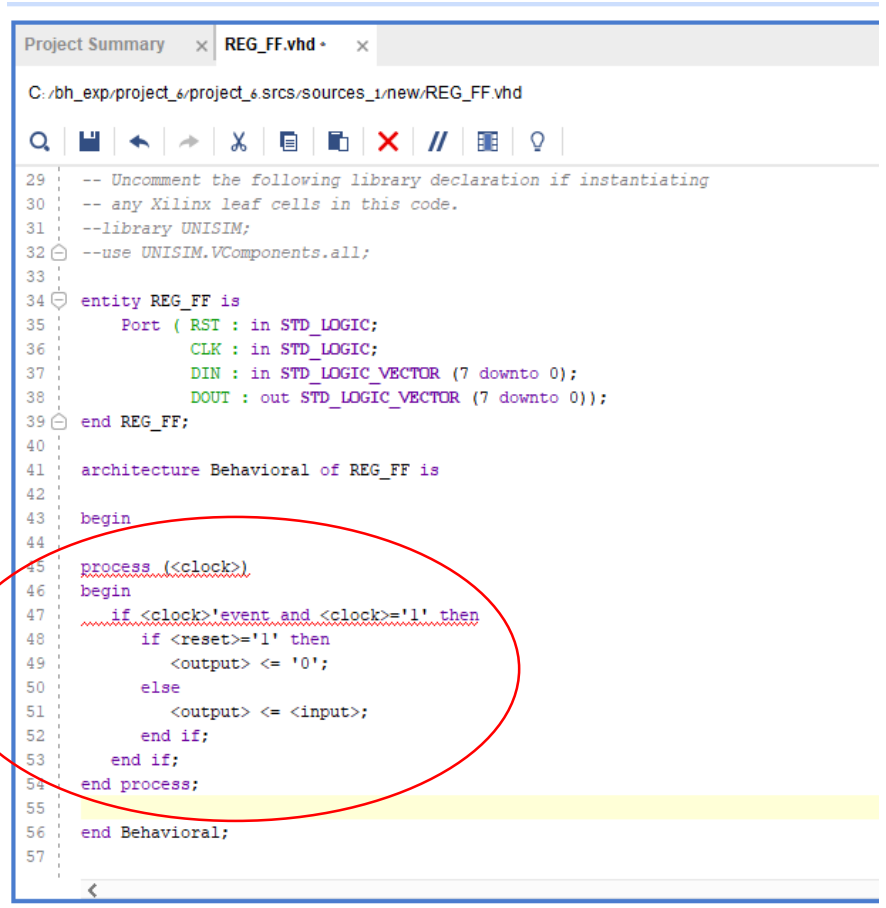


Using Language templates –stage 1

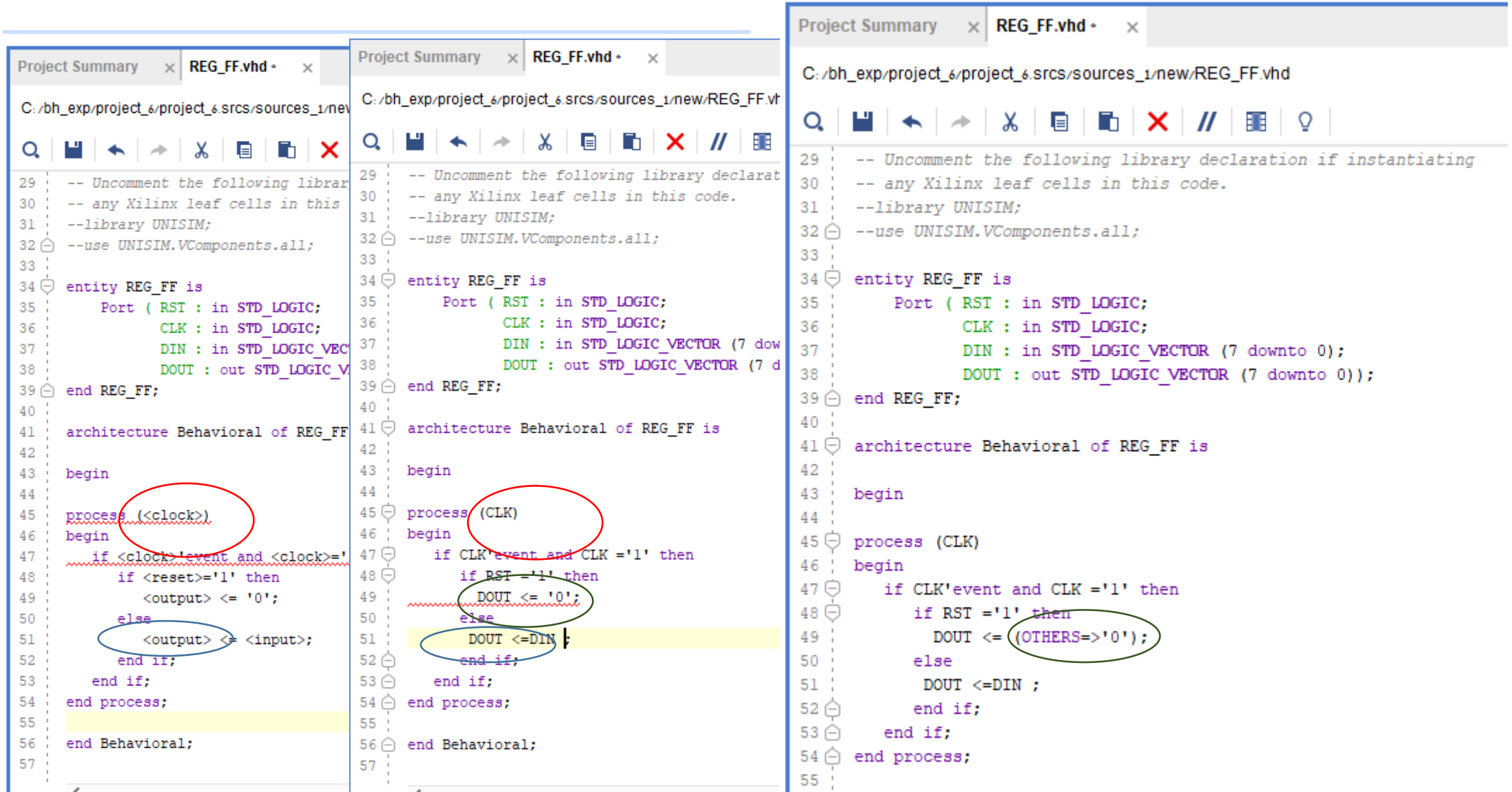




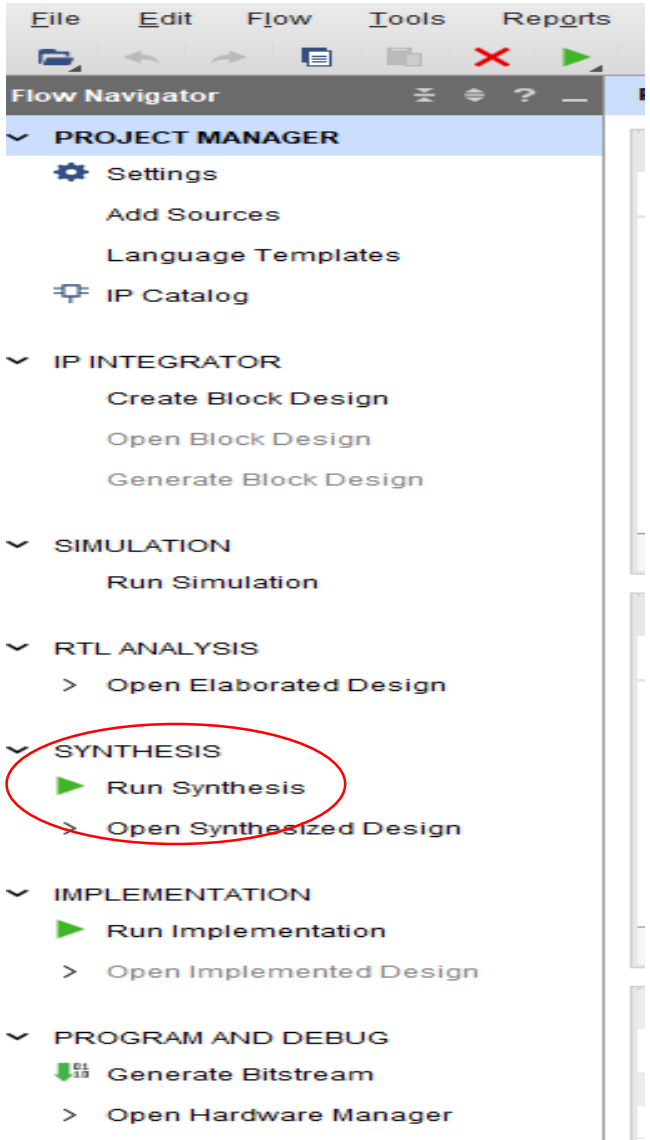
Using Language templates –stage 2

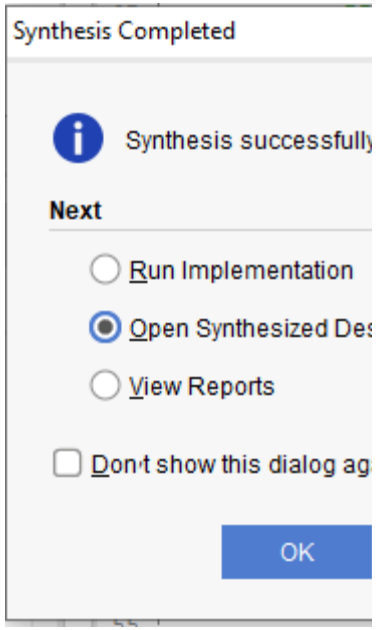


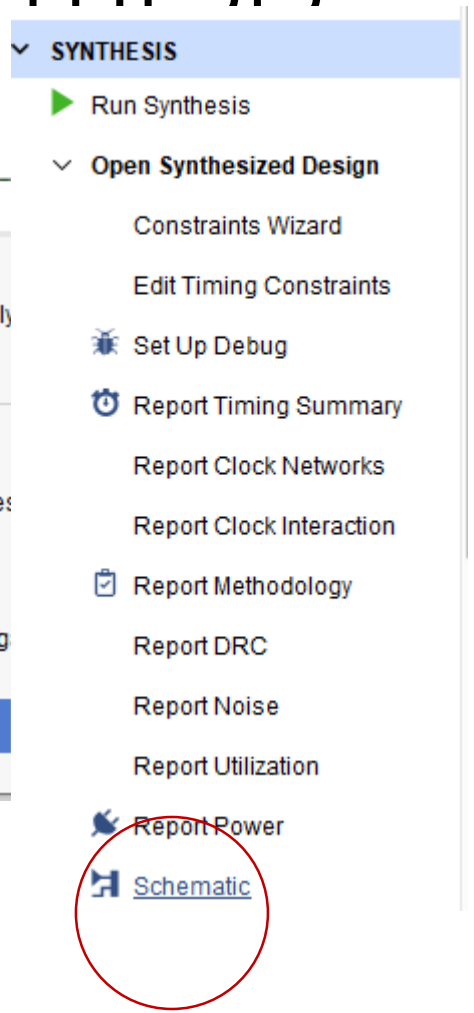
Using Language templates –stage 3



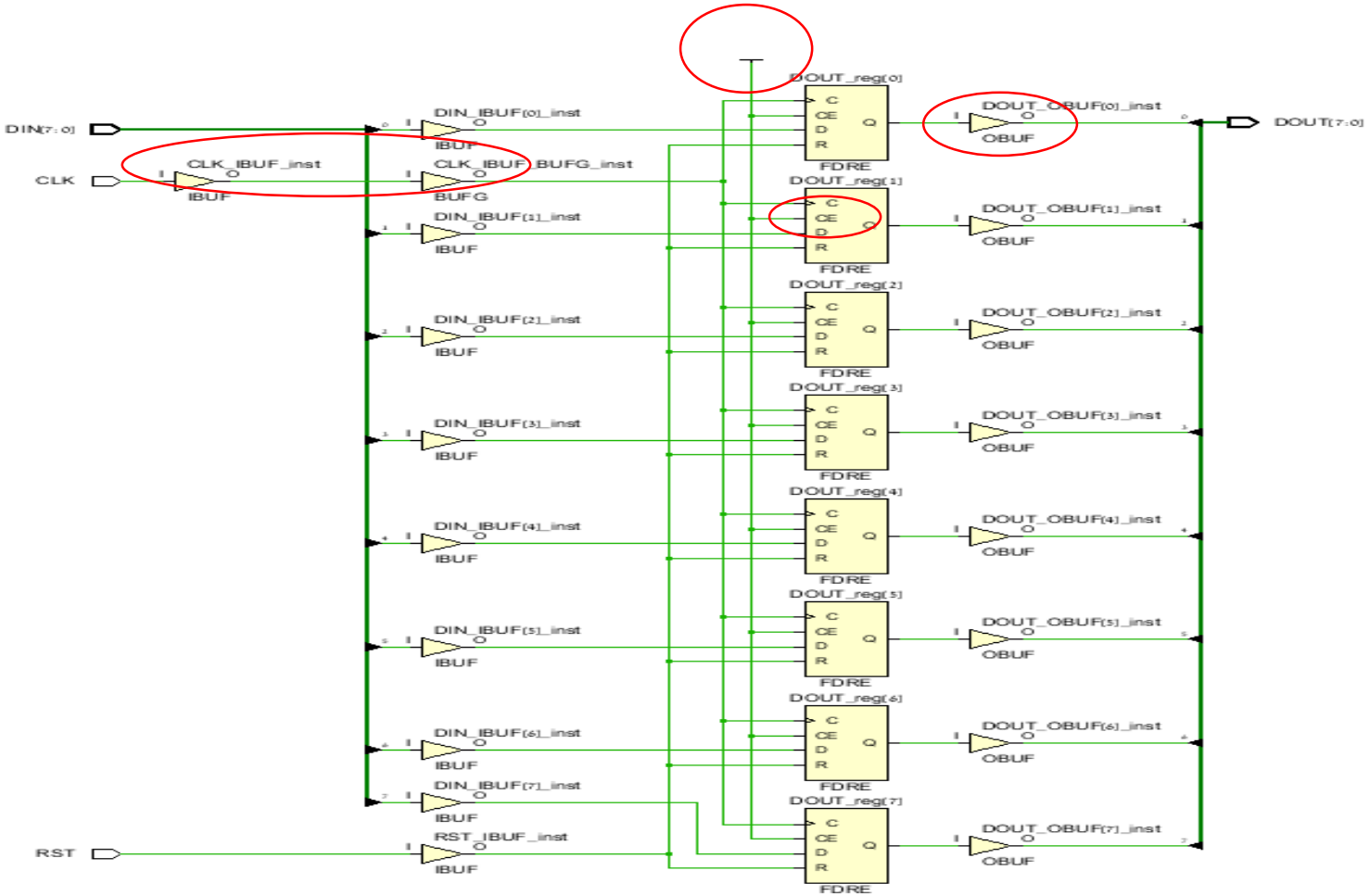
RUN SYNTHESIS



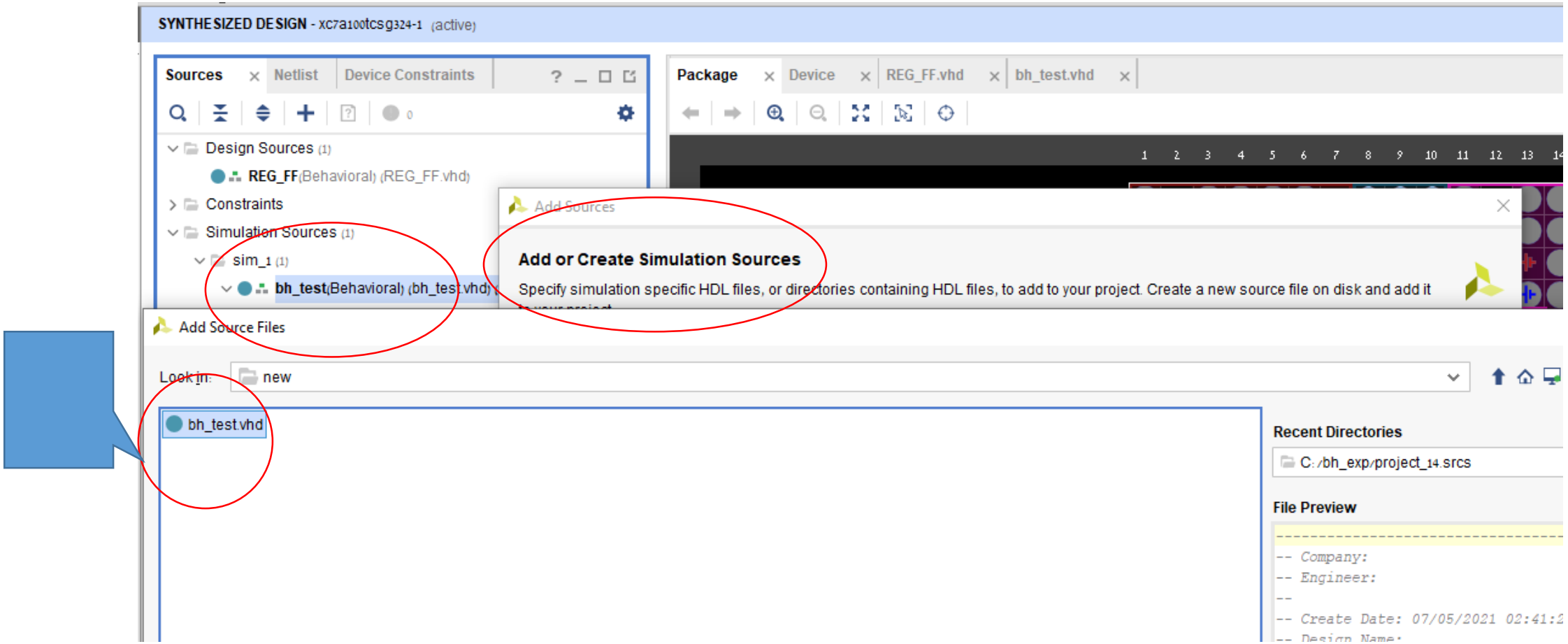




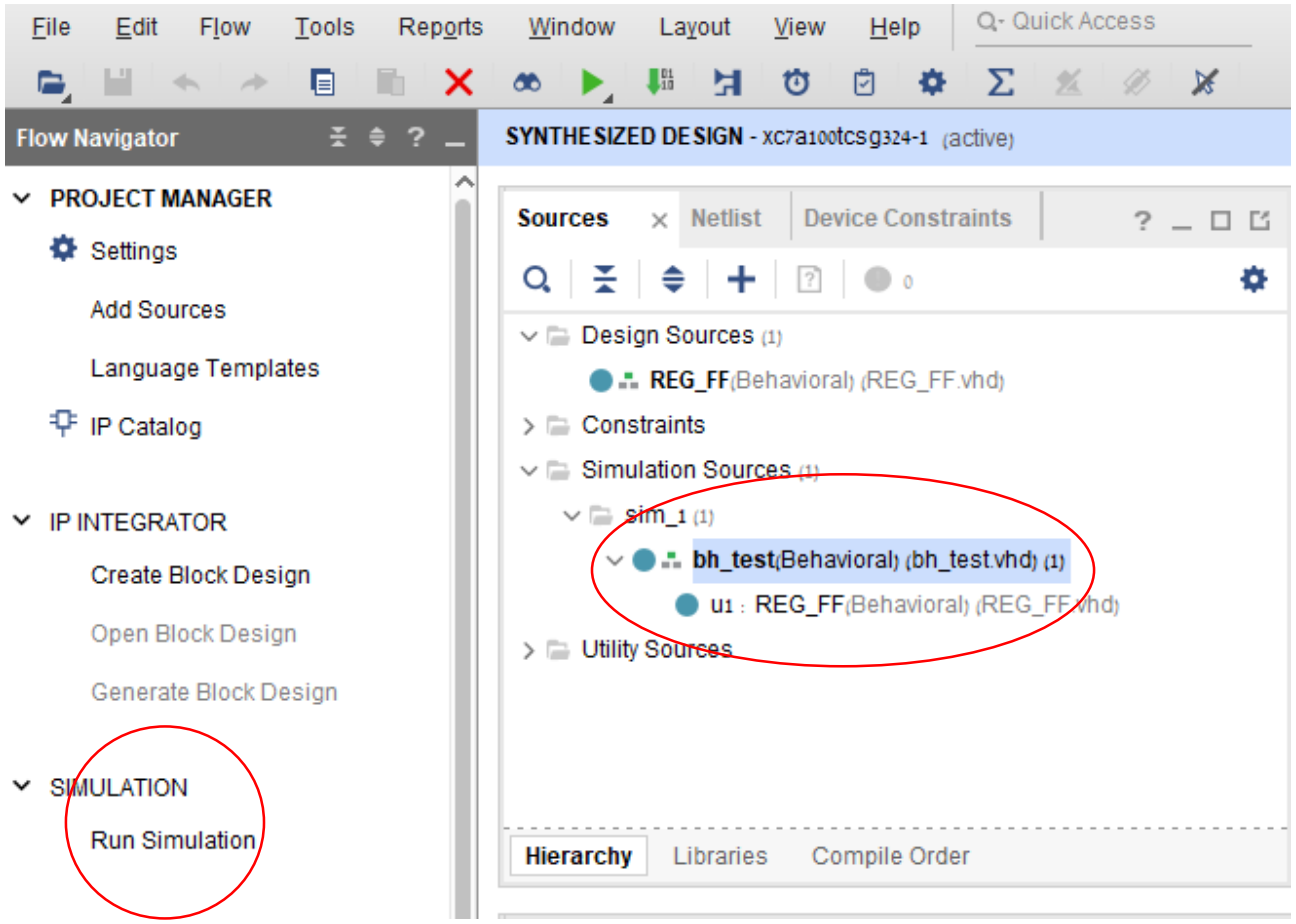
Schematic


DIN[7:0]
CLK
RST
CLK_IBUF_inst
IBUF
CLK_IBUF_BUFG_inst
BUFG
DIN_IBUF[0]_inst
DIN_IBUF[1]_inst
DIN_IBUF[2]_inst
DIN_IBUF[3]_inst
DIN_IBUF[4]_inst
DIN_IBUF[5]_inst
DIN_IBUF[6]_inst
DIN_IBUF[7]_inst
RST_IBUF_inst
DOUT_reg[0]
DOUT_reg[1]
DOUT_reg[2]
DOUT_reg[3]
DOUT_reg[4]
DOUT_reg[5]
DOUT_reg[6]
DOUT_reg[7]
C
CE
D
R
Q
FDRE
DOUT_OBUF[0]_inst
DOUT_OBUF[1]_inst
DOUT_OBUF[2]_inst
DOUT_OBUF[3]_inst
DOUT_OBUF[4]_inst
DOUT_OBUF[5]_inst
DOUT_OBUF[6]_inst
DOUT_OBUF[7]_inst
OBUF
DOUT[7:0]

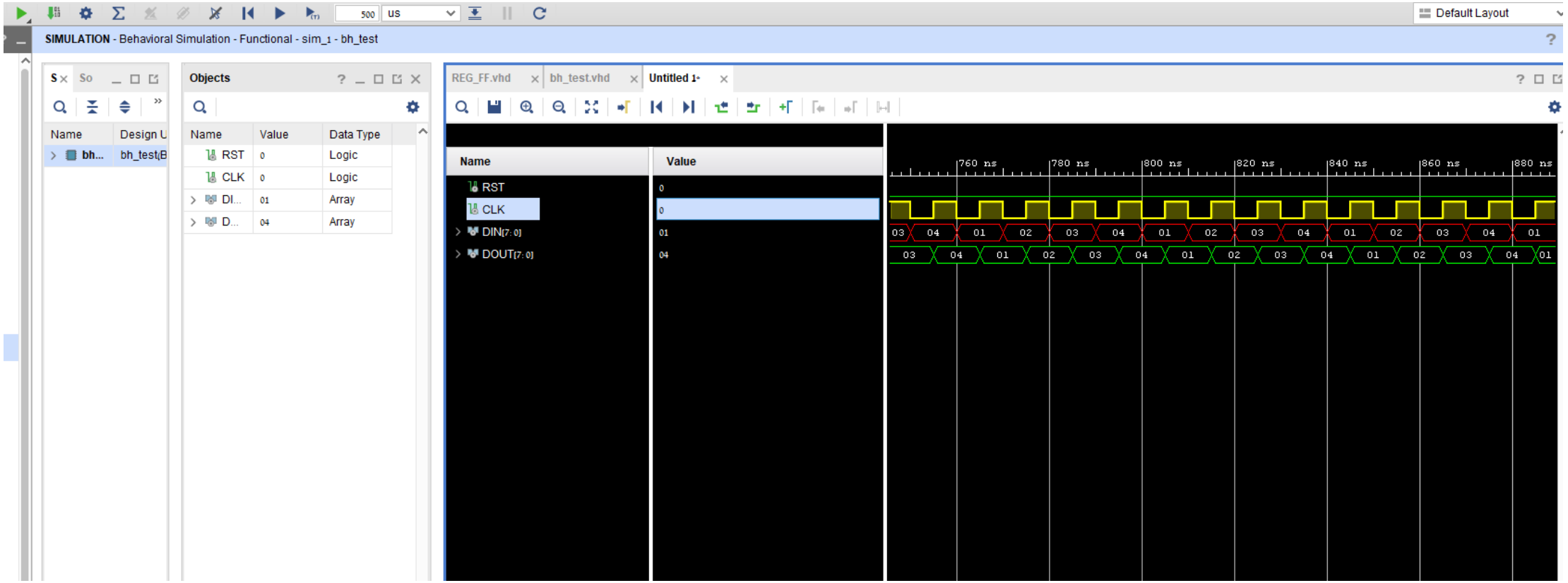
add source simulation



Simulation


File
Edit
Flow
Tools
Reports
Window
Layout
View
Help
Quick Access
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
SYNTHESIZED DESIGN - xc7a100tcsg324-1 (active)
Sources
Netlist
Device Constraints
Design Sources (1)
REG_FF(Behavioral) (REG_FF.vhd)
Constraints
Simulation Sources (1)
sim_1 (1)
bh_test(Behavioral) (bh_test.vhd) (1)
u1 : REG_FF(Behavioral) (REG_FF.vhd)
Utility Sources
Hierarchy
Libraries
Compile Order

Simulation


SIMULATION - Behavioral Simulation - Functional - sim_1 - bh_test
Default Layout
Objects
Name
Value
Data Type
RST
CLK
DI...
D...
REG_FF.vhd
bh_test.vhd
Untitled 1
DIN[7:0]
DOUT[7:0]
760 ns
780 ns
800 ns
820 ns
840 ns
860 ns
880 ns