Small Scale High Frequency Broadband NMR Preamplifier Project Proposal

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Contents

Acronyms **2**

Variable Conventions **2**

1 Introduction **3**

2 Scope **5**
2.1 Justification . . . 5

3 Design & Theory **7**
3.1 Component Selection . . . 7
3.1.1 High Frequency Low-Noise Amplifiers . . . 7
3.1.2 Transistors . . . 7
3.2 The Common-Emitter/Source Amplifier . . . 8
3.2.1 DC Biasing . . . 8
3.2.2 AC Output Impedance Analysis . . . 10
3.2.3 Q-Point Design Finalization . . . 11
3.2.4 Small Signal Voltage Gain . . . 11
3.2.5 AC Input Impedance Analysis . . . 12
3.2.6 LTspice Simulation Results . . . 12
3.2.7 Potential Multi-Stage Designs . . . 13
3.3 Noise . . . 14
3.3.1 Noise Figure . . . 15
3.3.2 Noise Reduction Techniques . . . 15
3.4 Transmission Lines . . . 16
3.4.1 Voltage Reflections . . . 16
3.4.2 Impedance Matching . . . 17
3.5 Circuit Protection . . . 17

4 Deliverables **17**

5 Testing & Validation Plan **18**
5.1 Magnetic Properties . . . 18
5.1.1 The Magnetic Field's Effect On The Circuit . . . 18
5.1.2 The Circuit's Effect on the Uniformity of the Magnetic Field . . . 19
5.2 Amplifier Parameters . . . 19
5.2.1 Gain . . . 19
5.2.2 Output Impedance . . . 19
5.2.3 Saturation Recovery Time . . . 19
5.3 Noise Performance . . . 20

6 Risk Analysis **20**

7 Workflow Diagram **22**

A Appendix **25**

A.1 BJT Hybrid-Pi 25
A.2 Common Emitter Amplifier Gain Calculations 27
A.3 Single Transistor Amplifier Topologies 28
A.4 The Junction Field Effect Transistor 30
A.4.1 Common Source Amplifier Gain 31
A.5 Transmission Line 32
A.5.1 Impedance 32
A.5.2 Smith Chart 32
A.6 Testing and Validation 34

Acronyms

BJT	Bipolar Junction Transistor
JFET	Junction Field Effect Transistor
LNA	Low Noise Amplifier
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NF	Noise Figure
NMR	Nuclear Magnetic Resonance
PCB	Printed Circuit Board
RF	Radio Frequency
SMT	Surface Mount Technology
SNR	Signal to Noise Ratio
VNA	Vector Network Analyzer

Variable Conventions

When referring to signals as voltages, this paper follows this convention:

i_B, v_{BE}	Total instantaneous values
I_B, V_{BE}	DC Values
i_b, v_{be}	Instantaneous AC values (not RMS)

1 Introduction

Signal amplification is a topic that has been widely researched and continually revised over the past few decades. However, there are always new areas within this field that present the opportunity to be explored, as such is the nature of our ENPH 459 capstone project.

For this project, we are working with UBC Physicist Dr. Carl Michal [1] to develop a Nuclear Magnetic Resonance (NMR) receiver coil preamplifier circuit. Dr. Michal is an associate professor for the Department of Physics and Astronomy at UBC, who has research interests in NMR application techniques and instrumentation. In this case, he is interested in creating a preamplifier circuit that will be used to amplify small signals (in the μV range) resulting from the NMR to an extent where they can be used for analysis later on.

NMR is a phenomenon where a particle generates an electromagnetic signal when placed in a strong magnetic field (B-field) with a smaller oscillating B-field. The strong B-field causes the particle's magnetic moment to line up with it, then a weak B-field perpendicular to the strong B-field causes it to precess. Eventually, if the field oscillation matches the particle's resonant frequency, the magnetic moment of the particle precesses horizontal to the strong field, producing a changing B-Field that can be detected with a probe. This phenomenon is often used to determine the presence of various particles in a sample by observing the resonant frequencies [2].

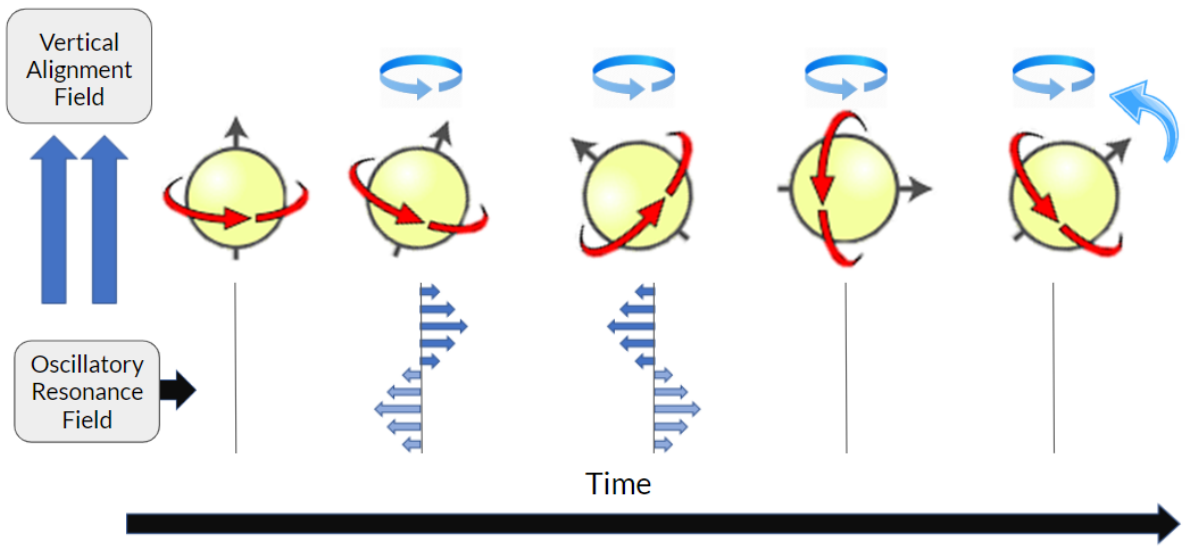

Figure 1: NMR Visualization.

Our project lies within a greater scope for NMR applications - Dr. Michal is currently working with Dr. Andre Simpson's research group, from the University of Toronto, to develop a NMR-spectroscopy-based assay capable of performing NMR on living organisms. This will allow them to monitor, at the molecular level, the impact of pollution on organisms throughout their life cycle, rather than simply measuring broad end-points like reproduction and death. According to The Andre Simpson's Research Group, no other techniques come close to providing the level of detail of molecular information *in-vivo* ("within the living") as NMR [3], furthering the cause for this research topic. In the larger picture of the research endeavour, our role is to develop preamplifier that will be used for NMR experiments within a traditional high-resolution NMR spectrometer.

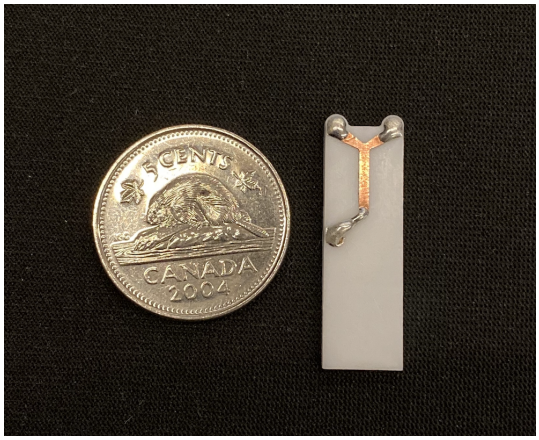

Figure 2: NMR probe beside nickel coin for scale (1.5 x 8.3 x 27 mm^3).

What makes our project unique is perhaps the environment of which the circuit will be placed in. Our amplifier needs to operate in a 8-12 Tesla magnetic field without perturbing it. This increases the complexity of our project as along with designing for specific requirements (bandwidth, gain, noise), we need to ensure our circuit satisfies those requirements in the magnetic field. Moreover, the setup of our project adds another layer of difficulty - the NMR probe will be placed inside the oscillating magnetic field, which in itself is a relatively strong RF signal compared to the NMR signal we want to analyze.

In terms of signal analysis, some NMR amplification techniques already exist for high magnetic field environments. A recent example of this is the work done by the *American Chemical Society*, where they experimented with the Signal Amplification by Reversible Exchange (SABRE) method to amplify NMR signals in a 9.4 Tesla field [4]. However, most techniques/applications are for a specific, predetermined frequency. The circuit that we are designing must be broadband (operation between 125MHz - 500MHz), which not only makes our capstone more challenging, but also a specific-case design project that has yet to be taken on by any other organization or group.

2 Scope

This section describes the scale and major dimensions of the project. Most of the project dimensions come directly from the original project description. Minimum requirements for each dimension, also written as 'must haves' in the Scope Table, are resulted from research and discussions with the sponsor. Individual requirements and their justification are provided after the scope table.

Dimension	**Must have**	**Should have**	**Nice to have**
Gain	Around 30dB	Around 33dB	40dB
Magnetic Properties	Circuit functions in 8-12 T with correctable disturbances to the uniform field	60 million^{-1} variation of the field over the sample volume	No disturbance to the uniform field
Operating Frequency	125 - 500 MHz ±10%	125 - 500 MHz	50 - 500 MHz
Output Impedance	50 Ω ± 20%	50 Ω	
Noise Figure	Less than 1.6 dB	Less than 1 dB	
Size	5 x 8.3 x ∞ mm^3	Minimum z-axis length	
Testing and Validation	Simulations and research data to prove schematic validity	Performance tested in the magnetic field with simulated signal	
Power	DC Power Supply (12V max)		Phantom power from 50 Ω transmission line
Saturation Recovery Time	1ms	Less than 1ms	
Total Cost	Under $1000	Under $600	Under $400

Table 1: Scope Table

2.1 Justification

1. Gain: The main goal of the preamplifier is to amplify the original signal so that the amplified noise amplitude of the original signal is greater than the thermal noise of the 50 Ω transmission line and the noise created by the preamplifier circuit combined. 30dB is a conservative estimate from the ratio of the resistances of the transmission line over the estimated minimum resistance of the NMR probe.

$$A = 20\log_{10}\left(\sqrt{\frac{R_o}{R_i}}\right) = 20\log_{10}\left(\sqrt{\frac{50}{0.1}}\right) \approx 27 \text{ dB} \tag{1}$$

2. Magnetic Properties: The circuit will be placed inside a strong magnetic field (8-12 T) so the minimum requirement is that the circuit is functional in the field. The uniformity of the external field is important for NMR, so the circuit itself cannot disturb the field. However, correctable disturbances will be tolerated, such as a linear gradient.

3. Operating Frequency: Some of the most important particles of interest have resonant frequencies in the range of 125 to 500 MHz. It is acceptable to have ±10% tolerance since it will still be distinguishable with the drop off.

4. Impedance: At high frequencies, transmission line effects may appear. To minimize voltage wave reflections, the output impedance from the preamplifier circuit must be as close to the impedance of the connecting transmission line as possible. Detailed theory is in section 3.4.2.

5. Noise figure: Since the input signal is already small, we wish to minimize the noise introduced by the preamplifier. It would be acceptable to have the circuit produce noise 2/3 the thermal noise of the NMR probe at the input. The thermal noise per square root of the bandwidth is [5]:

$$\frac{v}{\sqrt{\Delta f}} = \sqrt{4kTR} \approx 0.29 \text{ nV}/\sqrt{\text{Hz}} \tag{2}$$

   where k is the Boltzmann constant, T is the temperature in Kelvins, and R is the resistance in Ohms. For the NMR probe, T = 313.5 K and R = 5 Ω were used as upper bounds. If our circuit produces 2/3 of this, we can calculate an upper limit of the Noise Figure (NF). Using the formulas derived in Section 3.3.1, we compute a noise figure of 1.6 dB. A good amplifier has a noise performance lower than 1 dB [2].

6. Size: The circuit will be placed inside a cylindrical coil approximately the size of the NMR probe (1.5 x 8.3 x 27 mm^3). As a conservative approximation, a 5mm height for circuit components was chosen and the z-axis length (axial direction of the coil) does not have limits. However, it would be ideal to minimize the overall circuit volume.

7. Testing and validation: The minimum deliverable is a schematic for the preamplifier circuit. To show that the schematic is valid for the project, analytical proofs, simulation data on LTSpice and additional research data addressing each of the dimensions of the scope table will have to be provided. The precise requirements and methods to prove circuit functionality are written in sections 4 and 5.

8. Power: A DC power supply can be provided (12V is an arbitrary value based on commercially available power supplies). For minimum noise, a battery source can be provided. Otherwise, a linear regulator can be placed after the power supply. An ideal case would be 'phantom power', which doesn't require any additional power lines to the circuit other than the transmission line that the preamplifier connects to [6]. Power consumption should be minimized to reduce temperature variations.

9. Saturation Recovery Time: There will be a strong signal from the oscillating B-field with the same frequencies as the NMR signal, lasting ~10μs. Therefore, the preamplifier must recover from saturation before the NMR signal dissipates. NMR signal lasts about 100ms with exponential decay.

10. Cost: The sponsor has expressed that he can match the amount provided by the ENPH Project Lab, although he can contribute up to a few thousand dollars as part of his grant for the project. This cost includes any costs related to PCB manufacturing, sourcing components, consulting any possible external sources, or buying test equipment. It is not likely that we would need external expertise that require a payment, or to purchase new equipment since there are alternatives to various measurement techniques. The budget does not include labour costs for circuit maintenance.

Environmental factors such as temperature and humidity will be ignored since the sponsor has specified that we can assume that a source of constant air flow could be provided to keep the environment ideal for the circuit.

3 Design & Theory

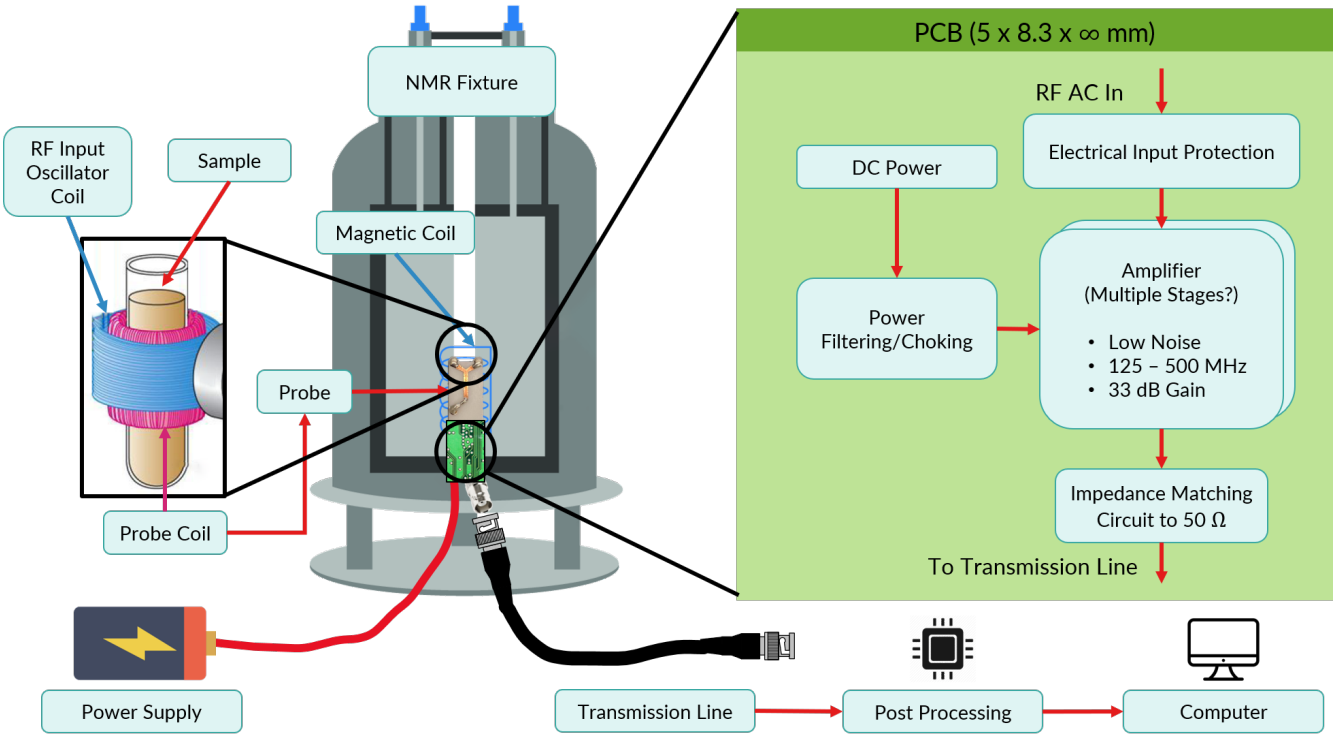

Figure 3: System overview of the proposed design of our preamplifier circuit as well as its operational environment. The NMR probe will be placed alongside the preamplifier and a sample inside a magnetic coil that presides in a fixture. This coil produces a stable field of 8-12 T. The coil that surrounds the sample is sent a RF signal from an external source which perturbs the sample, which in turn sends its NMR signal. The probe's coil observes the change in the field as a voltage signal to the preamplifier. After amplification the signal is sent over a coaxial cable for further processing.

3.1 Component Selection

There are a variety of options for amplifier circuit configurations. The following describes our decision-making process regarding component selections for LNAs, BJTs, JFETs, and MOSFETs.

3.1.1 High Frequency Low-Noise Amplifiers

We experienced difficulty sourcing Op-Amps that fit the requirements. After a discussion with Texas Instruments, we were discouraged to pursue this design due to insufficient noise performance. Therefore, we are investigating Low-Noise Amplifiers (LNAs) based on their low current consumption, wide bandwidth, and excellent noise performance. Lower current LNAs were preferred as they would generate smaller disturbances on the uniform B-field. We are parallelizing the design work with transistor-based circuits since LNAs' behaviour inside the B-field is less predictable compared to discrete transistors.

3.1.2 Transistors

To select transistors for the amplifier, we considered the following characteristics:

- Transistor terminal capacitance on the order of a pico-farad. High capacitance will limit the gain-bandwidth product of our transistor via the Miller Effect (described in 3.2.5).
- A noise figure (NF) ≈ 1 dB (since we also need to consider noise produced by other components)
- Small packaging (within design constraints)
- Power, voltage, and current ratings that do not constrain our design
- Higher priority to components available on Digikey

The Infineon 7th and 8th generation RF all fit the above requirements and were promising candidates for the BJT design. All transistors in the series had similar performance for our constraints: transistor terminal capacitance 0.5pF, ideal NF 0.5 dB, 2mm max dimension, sufficient max power ratings, and available on Digikey.

For JFETs, after satisfying the above list, we selected transistors that reached the saturation region within a volt, which allows us to reach the saturation current with a smaller power supply. JFETs typically have good noise performance than BJTs and MOSFETs due to their physical design so they are good candidates (see section A.4). The NXP BF861B is one sample transistor we sourced.

Due to their physical properties, MOSFETs have a higher input impedance than BJTs which result in a higher gain (~ 20dB - 26 dB on DigiKey components). However, this is only beneficial assuming low noise presence in the signal; in reality, this is the opposite. Imperfections and defects in MOSFET components can lead to high 1/f noise figures [7], hence adding additional noise and making the NMR signal more difficult to analyze.

3.2 The Common-Emitter/Source Amplifier

We started with a single-transistor circuit as to design for the smallest size and lowest NF (see section 3.3) design. Due to inability of other topologies to provide sufficient gain performance as a single stage, we chose to use a common emitter amplifier design (detail of transistor amplifier topologies in section A.3). This section outlines a common-emitter amplifier based on BJTs. The same concepts apply to other transistors.

3.2.1 DC Biasing

In designing a BJT amplifier, ensuring that the transistor remains forward biased avoids non-linear output due to rectification from the swinging AC source signal. To remedy this, we apply the principle of superposition. The AC signal can be offset by some DC signal, keeping the transistor in its linear active region. Additionally, the DC and AC response of the circuit can be analyzed separately. The DC operational state of the amplifier (all DC steady state currents and voltages with no small signal input) is called the Quiescent Operation Point, or Q-Point.

We require a few restrictions on the design:

- Collector current I_C of around 5 mA to reduce magnetic interference from Ampere's Law. Even with a very conservative estimate of a 1 cm current loop radius, and assuming the probe is approximately 1 cm away from the current loop, there would be a 27 nT magnetic field disturbance. Further testing of effects to magnetic field uniformity may change this strictness in the future.
- Z_o of 50Ω to match the transmission line at the output of the amplifier

- Start design with a low voltage power supply to reduce power consumption
- Components must be available in 0201 packaging on Digikey to meet size requirement. Setting this sizing standard allows to easily swap components on the PCB.

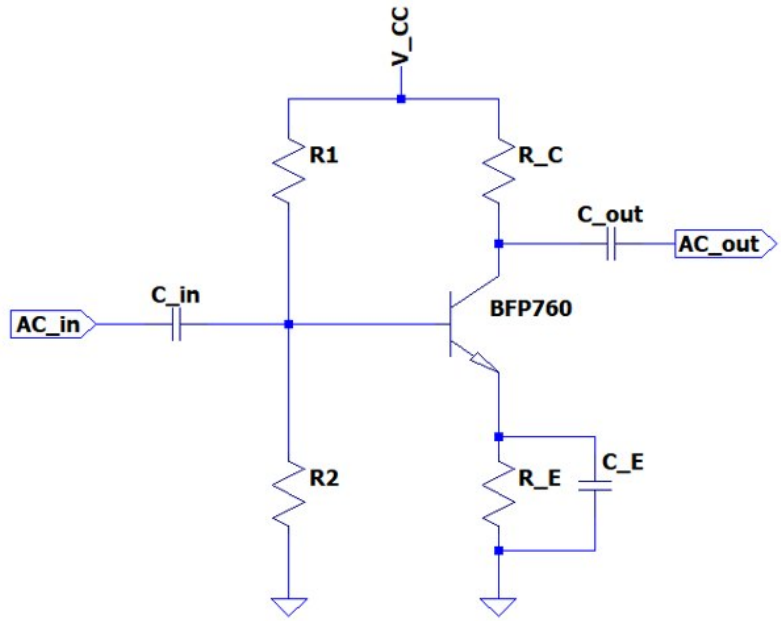

Figure 4: The common-emitter BJT amplifier design used in our analysis.

The common-emitter design (shown in Figure 4) uses a voltage divider at the base to add a degree of freedom on the biasing, an emitter resistor to improve bias stability, and an emitter bypass capacitor to short AC signals to ground [8]. Using the variables in Figure 4, we find how the resistor values in the circuit affect the emitter current (I_E). To do this, we apply Kirchhoff's Voltage Law (KVL) starting from V_{cc} through the b-e junction to ground, shown in equation 3.

$$V_{cc} - I_{R1}R_1 - V_{BE} = I_E R_E \tag{3}$$

Here, I_{R1} is the current through R_1 and V_{BE} is the voltage drop across the base-emitter PN-junction (0.76V at I_C = 5mA) [9]. Next, we find I_{R1} via nodal analysis at the base with label V_1 and the current amplification factor of the BJT as β. Note that $(\beta + 1)I_B = I_E$ is the characteristic relationships for the current gain of a BJT.

$$I_{R1} = \frac{V_{cc} - V_1}{R_1} = I_{R2} + I_B = \frac{V_1}{R_2} + I_B = \frac{V_1}{R_2} + \frac{I_E}{\beta + 1} \tag{4}$$

Plugging in $V_1 = V_{cc} - I_{R1}R_1$ and rearranging for I_E:

$$I_E = \frac{\frac{V_{CC}R_2}{R_1+R_2} - V_{BE}}{\frac{R_1 \| R_2}{\beta+1} + R_E} \tag{5}$$

Equation 5 shows that without the emitter resistor, I_E is proportional to β which could potentially vary with temperature as well as the magnetic field [10]. If the resistor values are chosen such that $\frac{R_1 \| R_2}{\beta+1} << R_E$, then I_E is practically independent of β and will be stable against any effects from the magnetic field. This allows us to get two equations to constrain our design, expressed in equations 5 and 6:

$$\left(\frac{R_1 \parallel R_2}{\beta+1} << R_E\right) \sim \left(\frac{R_1 \parallel R_2}{\beta+1} \simeq 0.1R_E\right) \sim (R_1 \parallel R_2 \simeq R_E) \tag{6}$$

3.2.2 AC Output Impedance Analysis

Since the output impedance (Z_o) of our amplifier is one of the most crucial parameters in the design, we decided to calculate which parameters of our design affect Z_o the most and constrain them accordingly. To analyze the AC Z_o of our circuit, we first short all DC supplies to ground (since DC sources act as shorts for AC signals) [8], short all large capacitors (C_E, C_{in}, and C_{out}), and replace the BJT with the Hybrid Pi model equivalent circuit (detailed derivation of the Hybrid Pi model is given in the appendix in section A.1), shown in Figure 5.

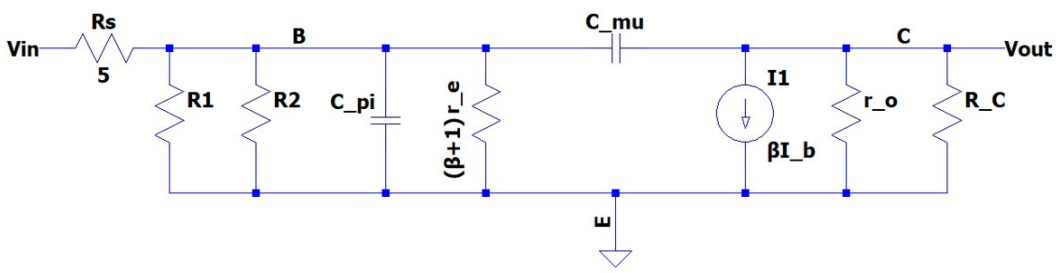

Figure 5: The AC equivalent circuit of the common-emitter amplifier with a Hybrid-Pi BJT model.

Z_o is defined as the equivalent impedance of the circuit when the source is shorted. If $v_i = 0$, then there is no current through the base and the dependent current source (I_1 in Figure 5) is also 0. Thus, Z_o can be found by an equivalent impedance calculation of all the resistors and capacitors in the circuit. To do this, we calculate the values of all Hybrid-Pi parameters. The results are summarized in Table 2.

Parameter	Calculation	Researched Data	Design Data	Value
C_π	-	$C_\pi = 0.595$ pF	-	0.595
$(\beta+1)r_e$	$(\beta+1)\frac{V_T}{I_E}$	$\beta = 350$, $V_T = 27$ mV	$I_E = 5$mA	1895 Ω
C_μ	-	$C_\mu = 0.147$ pF	-	0.147 pF
r_o	$\frac{V_A}{I_E}$	$V_A = 482.4$ V	$I_E = 5$ mA	96.48 kΩ

Table 2: Hybrid-Pi Model Parameters. Values indicated under "Researched Data" were sourced from the Infineon BFP760 spice model parameters [11] with the exception of the thermal voltage V_T [12].

Z_o of the amplifier is given in equation 7. Since parasitic capacitances will pose challenges at higher frequencies, we decided to conduct all analyses at the maximum frequency of 500 MHz. At that frequency, C_μ has an impedance of $Z_{c\mu} = \frac{1}{j\omega c_\mu} = -2165.4j\ \Omega$.

$$Z_o = R_C \parallel r_o \parallel (Z_{c\mu} + R_1 \parallel R_2 \parallel Z_{c\pi} \parallel (\beta+1)r_e \parallel R_s) \tag{7}$$

Notice that the two parallel components to R_C are much larger than 50 Ω, and that making $R_C = 50\Omega$ will cause it to dominate the parallel combination. We simplify by conservatively assuming that the parallel branch containing C_μ has the minimum possible impedance of $-2165.4j\ \Omega$ (shorting elements in series with C_μ). The equation for Z_o can then be further simplified by noting that r_o is at least 3 orders of

magnitude above the parallel combination Under this assumption, if $R_C = 50\ \Omega$,

$$Z_o = R_C \parallel Z_{c\mu} = \frac{(-2165.4j)(50)}{50 - 2165.4j} = 49.97 - 1.15j\Omega,\ f = 500\text{MHz} \tag{8}$$

Following the results of equation 8, we decided against designing an additional impedance matching stage at this point since we are still unsure whether such a small deviation would produce a noticeable effect, and that it would be better to first test the effects of the small mismatch.

3.2.3 Q-Point Design Finalization

After constraining R_C, we can nearly solve for all other resistors in the circuit. To complete the design, we constrain $V_{CE} > V_{BE}$ to keep the base-collector junction reverse biased. Setting V_{CE} to a conservative value of 1V (recall that $V_{BE} \simeq 0.8V$), we then constrain R_E with equation 9. Digikey does not have the calculated value in 0201, but there is a 412Ω resistor as an alternative.

$$V_{cc} - I_C R_C - V_C E - I_E R_E = 0 \rightarrow R_E = \frac{V_{cc} - I_C R_C - V_C E}{I_E} = 410\Omega \simeq 412\Omega \tag{9}$$

We then solve for the two biasing resistors using equations 5 and 6, simplifying equation 6 to require $R_1 \parallel R_2 = R_E$. Solving the equations yields $R_1 = 482\ \Omega$ and $R_2 = 2832\ \Omega$, fully constraining all parameters of the amplifier. The closest resistor values available in 0201 packaging were $R_1 = 487\ \Omega$ and $R_2 = 2.87\ \text{k}\Omega$. The final single-stage design with values is shown in Figure 6.

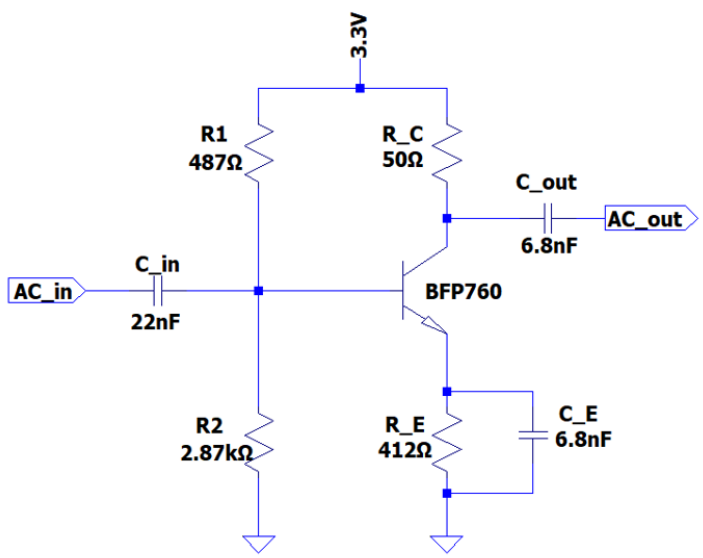

Figure 6: Complete Common-Emitter single-stage BJT amplifier design for the NMR preamplifier.

3.2.4 Small Signal Voltage Gain

The gain of the amplifier, $G = \frac{v_{\text{out}}}{v_{\text{in}}}$, is given by equation 10 (detailed derivations of the amplifier gain in section A.2).

$$G = \frac{v_{\text{out}}}{v_{\text{in}}} = -R_C \parallel Z_{c\mu}\left(\frac{I_E}{V_T} - \frac{1}{Z_{c\mu}}\right) = -9.254 + 0.190j,\ |G| = 9.256 = 19.328\text{dB} \tag{10}$$

It is evident that a single-stage amplification is insufficient as it is approximately 10-20 dB lower than the requirement. Note that this is the open circuit gain, and impedance matching at the output will decrease it by at least 6dB (shown in section A.2).

3.2.5 AC Input Impedance Analysis

Another important characteristic of the amplifier is the input impedance, Z_i, since a low Z_i will result in a reduced effective gain (if interested, detailed derivation provided in section A.2). We can simplify Z_i calculation by using Miller's theorem on C_μ, replacing it with two parallel capacitors, one each at the input and output [8] (Figure 7). This decouples the input and output. Z_i can then be easily calculated as a combination of all parallel elements at the input, as shown in equation 11. Note that increasing the gain will increase the Miller capacitance, thereby decreasing our effective gain at higher frequencies.

$$Z_i = Z_{\text{eq,in}} \parallel Z_{\text{CMi}} = 56.2 - 126.4j\Omega,\ |Z_i| = 138.3\ \Omega,\ \phi_{zi} = -66^\circ,\ f = 500\ \text{MHz} \tag{11}$$

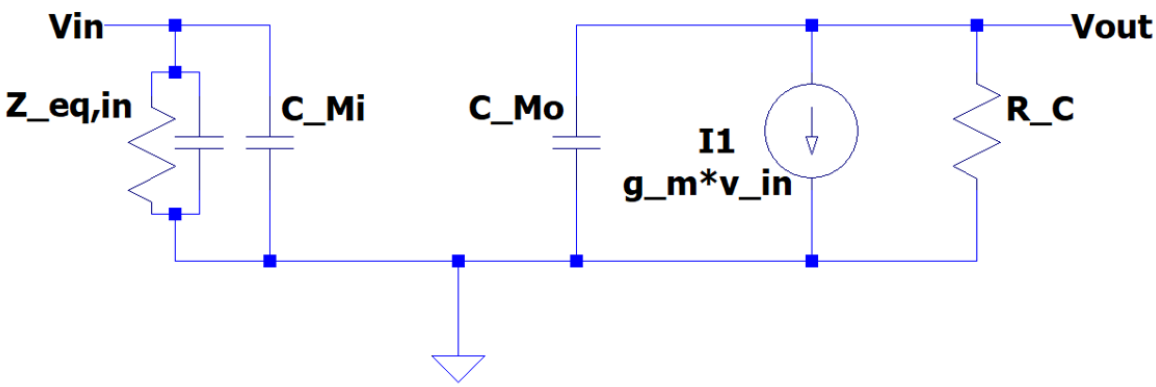

Figure 7: The Miller Effect allows decoupling of the input and output of our circuit All output components are now ignored by replacing the C_μ with two parallel capacitances. Here, $C_{\text{Mi}} = (1 + |G|)C_\mu$ and $C_{Mi} = \left(1 + \frac{1}{|G|}\right) C_\mu$.

3.2.6 LTspice Simulation Results

To confirm our model and our result, we simulated our circuit on LTspice. Infineon provides models for their RF BJTs to allow accurate component simulation. The resulting bode plot of G is shown in Figure 8. The simulated gain is slightly lower than what was predicted in our model (~18.5 dB vs. ~ 19.3dB). Although the cause of the discrepancy is unknown at the moment, the difference is small enough to validate our model as a preliminary design tool. The circuit can then be verified on LTspice and tested on a PCB.

To measure Z_o with LTspice, the open circuit gain was first measured (G = 18.5 dB). Then, the source and load resistors were varied independently until a decrease of 6dB was observed, which indicated impedance

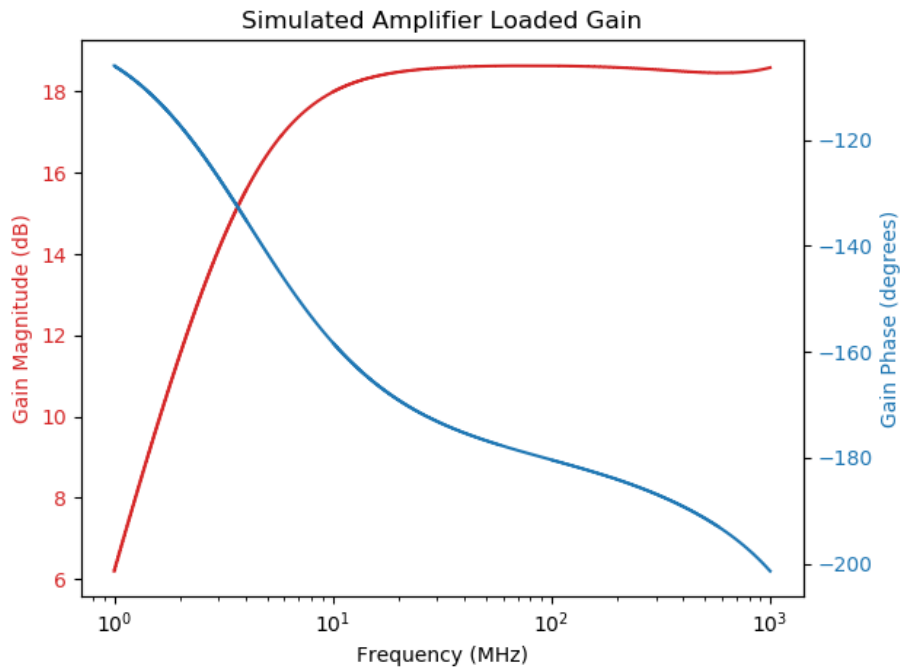

Figure 8: A Bode Plot of the amplifier gain.

matching at the input and output. This test yielded $|Z_i| = 140.3\ \Omega$ and $|Z_o| = 49.8\ \Omega$, which is extremely close to the calculated values for Z_i and Z_o from our model.

3.2.7 Potential Multi-Stage Designs

Although a single-stage common-emitter design was insufficient, this design can be extended to meet the gain requirements.

As shown in equation 10, the gain of the circuit is almost directly proportional to the current through the branch or to the collector resistance. These are constrained by our design requirements, but could be loosened under a couple conditions:

1. A buffer is placed at the output of the circuit to allow to match impedance with a higher R_C.
2. we discover that the effects of 5 mA of current on the magnetic field are sufficiently low such that we can raise the collector current.

Even then, we are limited by the Miller Effect on Z_i. Increasing the open circuit gain would also decrease our Z_i, which would in turn decrease our effective gain (as derived in section A.2). As mentioned in section A.3, the common-base topology bypasses the Miller Effect by having the input at the emitter. Thus, a setup that can achieve high gain while reducing the Miller Effect employs a low-gain common-emitter topology for high Z_i followed by a high gain common-base topology (which would then have to be impedance matched using an emitter follower buffer). This configuration is called a cascoded amplifier and is pictured in Figure 9.

Considering all BJT amplifier topologies and the fact that we can also include off the shelf LNAs in the design, there are many configurations together that could, in theory, meet the design specifications. However, all of those configurations are combinations of 4 distinct circuit designs:

- Common-Emitter/Source
- Cascoded Common-Emitter/Source + Common-Base/Gate
- Emitter-Follower to use as a buffer for output impedance matching
- Off the shelf LNA

We decided the best approach would be to design and characterize each configuration, test each configuration to see if our predicted performance is correct, and then based on test results decide how to best combine them to achieve the goals of the project.

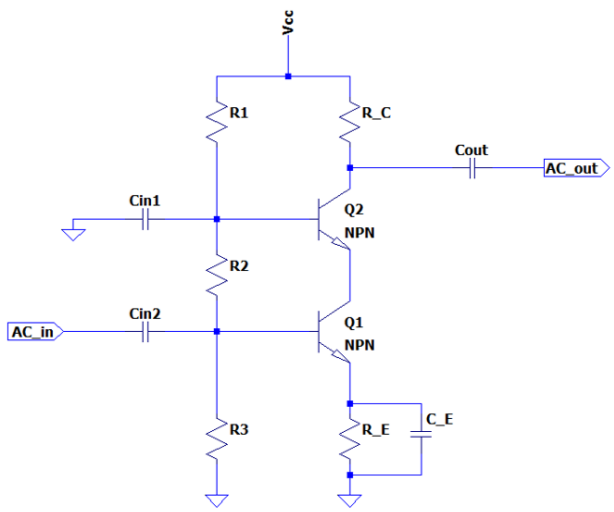

Figure 9: A Cascoded amplifier consisting of a common-emitter followed by a common-base.

3.3 Noise

Reducing the noise from our preamplifier is one of the major goals and difficulties with this project. The applicable noise sources are Johnson-Nyquist (thermal) noise, noise from active components (such as shot and flicker noise), noise from the surrounding environment, and noise from natural quantization fluctuation. From these, the ones in our focus are the thermal and amplifier noise, which are to be minimized [13].

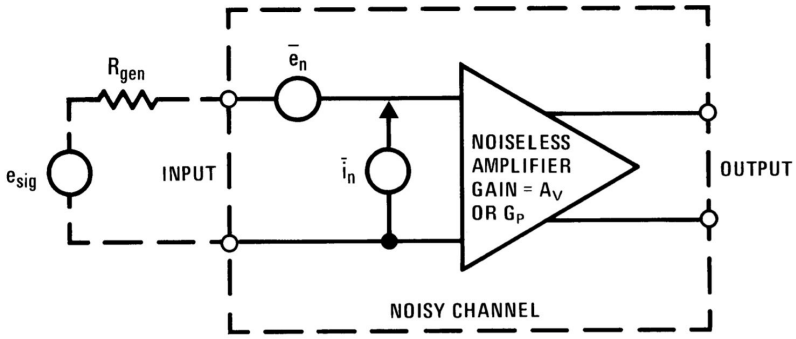

Figure 10: Noise Characterization of an Amplifier [14]

The noise performance of our system can be analyzed by using the model in Figure 10. The probe is modeled as an input to our amplifier with some signal source e_{sig} and impedance R_{gen}. Our noisy amplifier is separated into a noiseless amplifier, an equivalent amplifier noise current generator $\bar{i}_n$, and an equivalent amplifier noise voltage generator $\bar{e}_n$. The equivalent noise voltage $\bar{e}_n$ is the noise seen at the input of our amplifier if we simply short the input terminal(s). The equivalent noise current $\bar{i}_n$ typically occurs from shunting capacitors or resistors across the terminals as $\bar{i}_n R_{\text{in}}$ (or X_{in}). These are RMS values and have units of $\text{V}/\sqrt{\text{Hz}}$ or $\text{A}/\sqrt{\text{Hz}}$. These values are specified at certain frequencies and are not constant over the range of a specified bandwidth (typically increases at lower frequencies) [14].

Caused by the thermal agitation of electrons inside conductors, thermal noise can be modeled using a noiseless resistor R_p in series with its noise voltage e_p:

$$e_p = \sqrt{4k_B RT\Delta f} \tag{12}$$

where we have the Boltzmann constant k_B, the absolute temperature T, and the bandwidth Δf. On the other hand, shot noise and flicker noise are considered electronic noise sources and arise commonly from active devices. Flicker noise is more prominent at low frequencies (0-100 Hz) [13].

3.3.1 Noise Figure

The noise performance of our circuit can be modelled by the noise figure of the amplifier. If we suppose the Signal to Noise Ratio (SNR) at the input is:

$$\text{SNR}_{\text{input}} = \left(\frac{v_i}{N_{\text{probe}}}\right)^2 \tag{13}$$

where v_i is the input signal and N_{probe} is the noise voltage of the probe (the ratio is expressed as a square as noise is added in terms of power). Then, the output signal-to-noise ratio $\text{SNR}_{\text{output}}$ is:

$$\text{SNR}_{\text{output}} = \left(\frac{A_v v_i}{\sqrt{(A_v N_{\text{probe}})^2 + (A_v \bar{e}_n)^2}}\right)^2 \tag{14}$$

where A_v is the voltage gain of the amplifier. We can then calculate the noise figure as [15]:

$$\text{NF} = 10\log_{10}\left(\frac{\text{SNR}_{\text{input}}}{\text{SNR}_{\text{output}}}\right) \tag{15}$$

If we assume that $\bar{e}_n = N_{\text{probe}}$, then the noise figure is 3 dB. As mentioned earlier, a good preamplifier has a noise figure of below 1 dB [2].

3.3.2 Noise Reduction Techniques

From the above equations it can be seen that a reduction in temperature can significantly improve noise performance, which is why many NMR spectrometers run at cryogenic temperatures. Although the environment will be at room temperature, constant airflow will be provided to maintain some steady temperature. Additionally, we can aim for low power dissipation to reduce such variations.

To minimize electronic noise, we can source components with low equivalent noise voltages while reducing the number of active components we use. This is one of the reasons a single-transistor amplifier

would be ideal, while a multi-stage cascading/cascoding amplifier would be preferable to achieve other requirements such as gain. Applying additional low or very high frequency filters can exclude unwanted bandwidth from the signal. In the design of the PCBs, it will be important to avoid ground loops, adding physical space between analog signals, reducing trace lengths, adding decoupling capacitors and more.

Minimizing external noise sources through voltage smoothing and current choking on the power supply will be investigated once a functional circuit is obtained if significant ripple is observed.

3.4 Transmission Lines

Transmission line refers to a system designed to transfer electrical energy in the form of voltage wave from the source to the load. In standard circuit analysis, the time difference for the finite speed voltage wave is ignored because the length scale of the circuit is well below the wavelength of the wave [16]. As the transmission line gets longer, signal wavelength gets shorter, and the difference in the time of arrival of the signal becomes more significant.

3.4.1 Voltage Reflections

Voltage waves, as any other forms of waves, can be reflected back. The end condition of the mechanical wave is analogous to the load impedance for a voltage wave. A 'fixed' end is like a short circuit since the voltage is forced to ground and a 'free' end is like an open circuit since nothing is connected. Similarly, if a rope is connected to another rope with a different weight, hence a different mechanical impedance, then a fraction of the wave will be reflected back.

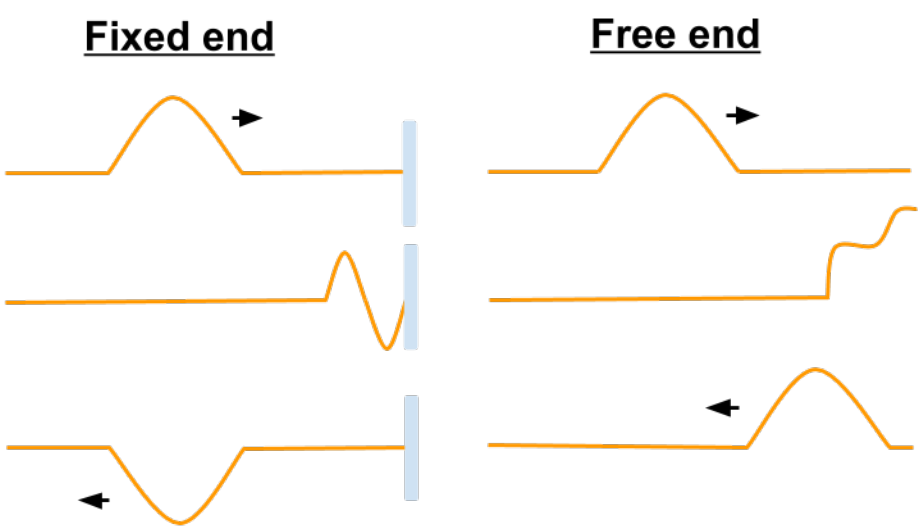

Figure 11: Depending on the ending condition(mechanical impedance), the wave is reflected in different orientations(phase). This figure specifically compares a fixed end to a free end [17].

If voltage waves are reflected back, the transmitted power is decreased. If the length of the transmission line is significantly smaller than the wavelength of the signal, the nodes of the standing wave are outside the circuit, making the issue negligible. For this project, $f_{\max}$= 500 MHz, so we would see significant reflection issues when the traces on our PCB reaches around 60cm:

$$\lambda = \frac{c}{f_{\max}} = 60 \text{ cm} \tag{16}$$

However, this is assuming that the voltage wave travels at the speed of light. A conservative estimation is $\lambda/10 = 6$ cm as a threshold at which we ignore voltage reflections on our PCB according to the PHAS Elab. Since the preamplifier will be attached directly to the NMR probe, we will not consider transmission line effects at the input of the preamplifier.

3.4.2 Impedance Matching

Voltage reflections can be avoided by impedance matching. If a transmission line has its characteristic impedance Z_0, the reflection coefficient, Γ, is described by citetransmissionLine:

$$\Gamma = |\Gamma|e^{i\phi} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{17}$$

where Z_L is the load impedance, or the characteristic impedance of the connected transmission line. If the load impedance is equal to the characteristic impedance of the transmission line, the signal will be transmitted entirely. Derivation of Z_0 can be found in section A.5.1

The 50 Ω transmission line must be matched at the output of the preamplifier. Since impedance is a function of frequency and influences the gain, trade-offs will need to be considered. A useful tool for this is a graphical method called the Smith chart shown in section A.5.2. Section A.2 details this impact on amplifier gain. In general, higher output impedance relates to higher gain.

3.5 Circuit Protection

There are several risks that need to be addressed regarding circuit protection. Due to the nature of NMR, the circuit needs to endure high magnetic fields and occasional blasts of strong RF signals. These RF signals cannot be filtered since they are in the same frequency as the input signal. One of the common solutions to this problem is using a positive/negative diode clipper as shown in Figure 12. Further investigation of effectiveness is required after the development of the preamplifier circuit, but there are existing designs for RF input protection circuits [18].

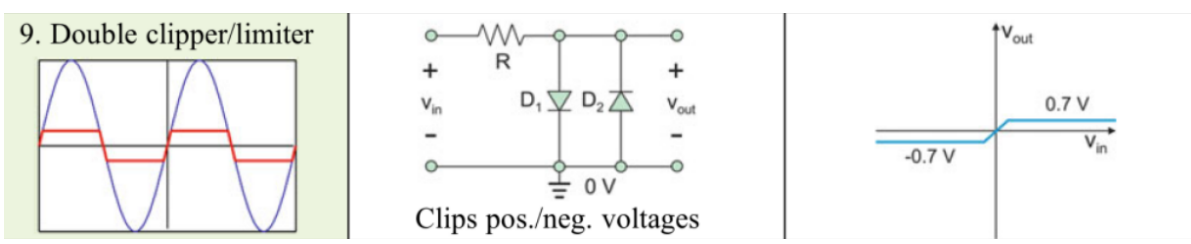

Figure 12: Parallel positive/negative diode clipper configuration to cut off voltages higher than the voltage drop across the diode (0.7 V in this case) symmetrically on an AC signal. This voltage level can be altered by using germanium diodes, where the voltage drop is 0.3 V instead [19].

4 Deliverables

The main goal of our project is to deliver a working NMR preamplifier circuit to our sponsor by April 2020. Now as mentioned in the scope table, this can either be a circuit schematic or a physical circuit. As such, we have two main deliverable options with the following criteria:

1. **Option 1: Circuit Schematic** - we present a complete circuit diagram with transistor models, resistor/capacitor values, and wiring. To validate the design, we will provide proofs for the equations we used in our circuit design along with simulation results.
2. **Option 2: Physical Circuit** - we submit a physical version of our design with all components soldered on and placed on the PCB. In this option, it is not required for our team to provide a special report justifying our decisions as long as the circuit is operational.

In addition, the following elements will also be submitted as deliverables upon the completion of this project, mostly to support our main deliverable element:

- Circuit diagram detailing the components used, along with the layout/orientation of the circuit.
- BOM of the components and where to source them from.
- Manual for operating the circuit.
- Documentation detailing relationships between the electrical characteristics of the circuit, such as:
    1. Gain vs frequency.
    2. Noise performance vs frequency.
    3. Input/output characteristics vs frequency.
    4. Maximum input/output signal & amplitude/power.
    5. Performance vs temperature.
    6. Power supply requirements & power consumption.
- Final proposal document that provides a comprehensive overview on the NMR preamplifier circuit.

5 Testing & Validation Plan

The following are tests we can perform to ensure our prototype circuit designs meet the requirements in the scope table.

5.1 Magnetic Properties

5.1.1 The Magnetic Field's Effect On The Circuit

Steps to prove circuit functionality in the B-field:

1. Use a coin-sized neodymium magnet, which can exert a B-field of a Tesla to check if circuit components are magnetic [20]. If they are ferromagnetic, they will react to the stable magnetic field and disrupt its uniformity, thus disallowing their candidacy.
2. Compare DC characteristics of the circuit inside and outside the field. Presence of ferromagnetic or magnetoresistive materials can be affected. Also, a strong B-field can affect the diffusion of charge carriers [10], so it can directly affect the characteristics of a transistor. This can be probed with a protoboard-circuit and a standard oscilloscope.

3. Compare AC characteristics of the circuit inside vs outside the field. This requires a carefully planned out PCB to connect to a Vector Network Analyzer (VNA) due to the high frequency signals. The PCB design and the testing equipment is outlined in sections 5.2.1 and 5.2.2.

5.1.2 The Circuit's Effect on the Uniformity of the Magnetic Field

Steps to characterize whether the current through the circuit itself will affect the uniformity of the external field:

1. Analytical model of the traces estimated as a magnetic monopole. This estimates the scale of the magnetic distortions on a theoretical level.
2. Performing NMR with the probe. If the circuit impacts the external field, NMR signals will be distorted. Placement of tuned correction coils around the magnet based on the theoretical model can isolate the type of distortion on the field.

5.2 Amplifier Parameters

5.2.1 Gain

Gain measurement is not trivial since the input signal is very small (which is why we need a preamplifier). Validation can be done as follows:

1. To avoid impedance matching at the input (as discussed in section 3.4.1), we will connect the VNA probe to a voltage divider consisted of a 50 Ω and a 0.1 Ω resistor, then using the signal across the smaller resistor as the input to the preamplifier. This makes the impedance to the VNA close enough to avoid reflections and the signal into the circuit will be of similar magnitude as a real NMR signal. The amplitude across the 0.1 Ω resistor can be calculated from the voltage divider, therefore the gain can be measured by comparing it with the output amplitude.
2. Using an RF synthesizer to characterize gain between 50-300 MHz. This setup does not require a voltage divider, but we may not be able to perform the full frequency sweep.

5.2.2 Output Impedance

1. LTspice and online Smith Chart simulated output impedance calculations
2. Single port measurement on the VNA. This may lead to constant modification of various passive components at the output of the circuit since impedance is a function of frequency. We will design a modifiable PCB using the structure in Figure 13.

5.2.3 Saturation Recovery Time

Saturation recovery time from an RF blast:

Connecting the source of the RF signal to an oscilloscope while the circuit is saturated and measuring the time it takes the output of the preamplifier to return back to its normal state. We may have to add a Schottky diode to improve the recovery time [21].

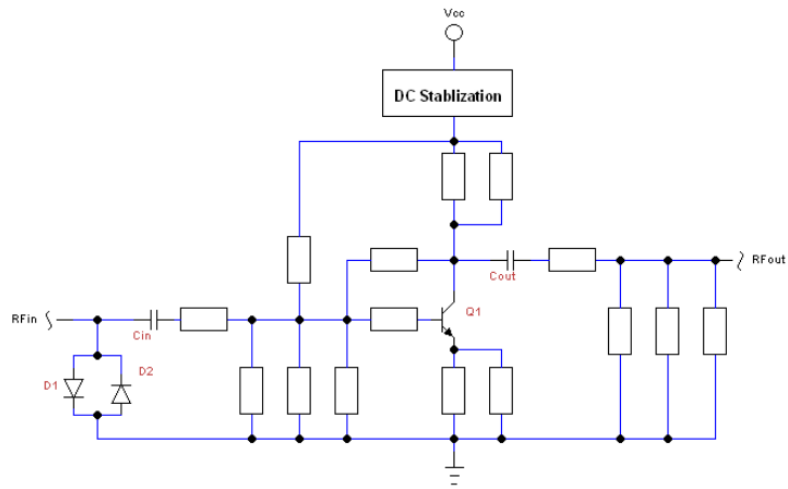

Figure 13: Structure of the modifiable PCB. All rectangular boxes are places that are available for potential passive components. If the passive components are not required, 0Ω resistors will be placed for boxes in series, and all parallel pads will remain unpopulated. Although there were concerns regarding antenna effects for unpopulated pads branching off of the main trace, guidelines from Altium and consulting the electronics lab from the UBC Physics department has eliminated this risk.

5.3 Noise Performance

Generally, the noise figure of a circuit can be measured with a spectrum analyzer. However, due to the lack of an accessible spectrum analyzer, we have developed alternative methods to quantify the noise performance:

1. Measuring the output signal of the preamplifier when there is no input signal. This will give us an idea of the "white noise" present in the amplifier itself, which is directly related to the equivalent noise performance [14].
2. Comparing the output signal of a 50 Ω source at room temperature vs after dipping it into liquid nitrogen. As the thermal noise is a function of temperature, comparing the two results will enable us to calculate the thermal noise that is present in the circuit.
3. Plotting the RMS value of a known sine wave, then attenuating the sine wave until the RMS plot dips from the signal being flooded into the noise level.

6 Risk Analysis

In terms of the scope, most of the risks revolve around the functionality of the circuit - it's physical/electrical characteristics, operational limits, and ability to produce an amplified signal while achieving minimal noise figures. Thus, these factors become the foundation for our risk analysis as we must ensure that our circuit adheres to the requirements set out in the scope table.

Table 3: Risk Analysis Table

Risk	Probability	Severity	Mitigation	Score	Comments
Magnetic field affects component functionality	High	High	Early testing and sourcing a variety of components	**High**	Currently testing components using in magnetic field with DC signals.
Pre-amp causes noticeable disturbances to the magnetic field	Medium	High	Early testing to ensure disturbances to and from magnetic field are acceptable	**High**	
Noise coming from preamplifier itself is overwhelming	Medium	High	Spend significant time researching noise sources and noise reduction techniques. Source low noise components	**High**	Current ratio we are aiming for is less than 1.0.
Input and output impedance & gain not all attainable with single transistor circuit	Medium	Medium	Cascade or cascode transistor designs or use alternative amplifier designs	**Medium**	
RF pulse causes damage to the circuit	Medium	Medium	Use input protection circuits, such as cross or pin diodes	**High**	This needs to be researched further to determine a solution.
Design unrealizable on small space constraint	Low	Medium	Simplify & reorganize design, choose smaller components	**Medium**	
Inconsistent PCB procurement time	Medium	Low	Design testing PCBs to be customizable and modular. Order early and communicate with vendors about schedules.	**Medium**	Main concern is holiday season - submit initial PCBs for manufacturing before then.
Heat from the preamp influences probe receptance from thermal expansion	Low	Low	Spend significant time researching noise sources and noise reduction techniques; source low noise components	**Low**	

Table 4: Risk matrix colour legend

Colour	Legend
	Not Acceptable - Risk reduction required. These risks should be addressed as soon as possible.
	Acceptable as long as scope requirements are satisfied. Consider risk reduction after high priority risks have been addressed.
	Acceptable.

7 Workflow Diagram

To address the challenges and risks in this project, we have developed a workflow diagram which shows our planned actions and progress for each major milestone. The workflow diagram is broken down into five major sections:

1. Define Project (September/October) → we clearly define the project, scope, and requirements with our sponsor during this time.
2. Initial Simulations/Testing (November/December) → run simulations to determine circuit components, develop prototype PCBs for simple magnetic tests.
3. Select Circuit (January/February) → perform extensive testing on circuits that have passed the first screening rounds in the step before and select the most promising circuit design to progress onwards with.
4. Tune Circuit (March) → optimize and validate chosen circuit to satisfy project requirements.
5. Submit Project (April) → finalize design, document all aspect of our work, and submit final report.

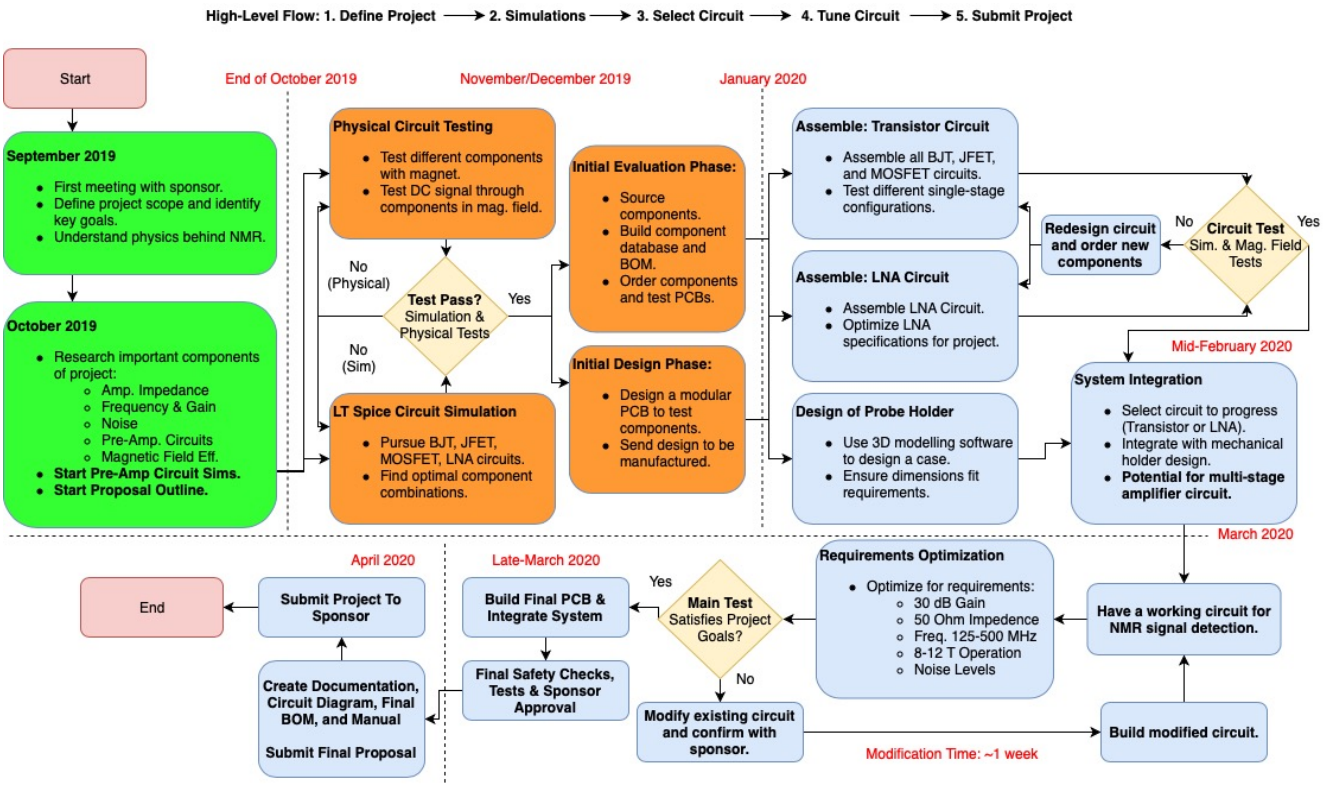

Figure 14: Workflow Diagram

In our workflow diagram, green indicates tasks that have been completed, orange indicates current tasks, and blue indicates tasks that will be done in the future.

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A Appendix

A.1 BJT Hybrid-Pi

One of the biggest difficulties in analyzing transistor circuits is that they are non-linear devices. To counter this, we can keep them within a region which they behave almost linearly. To take full advantage of this, the transistor is replaced with a linear, small AC signal equivalent circuit. For our application, the transistor is best modelled by the Hybrid-Pi Model. The steps for constructing this model are [8]:

1. Create the most basic equivalent model by accounting for current amplification and V_{BE} drop
2. Account for the Early Effect [22]
3. Account for junction capacitances

The most basic model can be constructed by replacing the transistor with a current controlled current source at the collector (having a value of β multiplied by the base current) and a diode at the emitter (representative of the p-n junction between the base and emitter), as shown in Figure 15. However, the diode itself is a non-linear device, and must be replaced with a linear model as well. This is done by linearizing the diode's voltage-current relationship around the Q-point, since it acts approximately linear under small AC perturbations. This results in first order Taylor approximation of the relationship. The method involves examining how infinitesimal changes in current cause changes in voltage ($\frac{dV_D}{dI_D}$) and replaces the diode with a resistor with R = this rate of change [8].

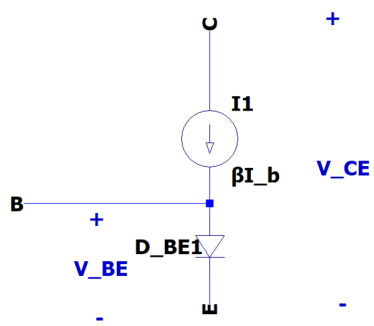


Figure 15: The BJT modeled as a current controlled current source and a base-emitter diode.

To calculate the dynamic resistance, we differentiate the current-voltage relationship of the diode:

$$I_E = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \tag{18}$$

$$\frac{dI_E}{dV_{BE}} = \frac{1}{r_e} = \frac{I_S e^{\frac{V_{BE}}{V_T}}}{V_T} = \frac{I_E + I_S}{V_T} \tag{19}$$

where I_E is the emitter current, I_S is the reverse saturation current of the pn-junction ($\sim 10^{-12}$ from the transistor datasheet), V_T is the junction's thermal voltage and is typically 25mV, V_{BE} is the base-emitter potential difference, and r_e is the dynamic resistance. Since $I_S << I_E$, we can write the dynamic resistance as [8]:

$$r_e = \frac{V_T}{I_E} \tag{20}$$

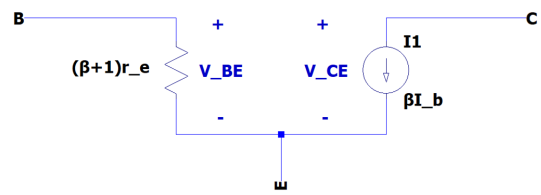


Figure 16: The linear equivalent version of the model. The location of r_e only affects the base and not the collector since the collector has a constant current source. r_e in the figure has been adjusted with a correction factor, since its current is now I_B and not I_E. This placement makes the circuit analysis much simpler as the base and collector are decoupled from each other.

Once the diode is replaced, we can decouple the base and collector as shown in Figure 16.

To improve the accuracy of the model in Figure 16, we next need to model the Early Effect. While it is generally assumed that the current through the collector is only dependent on the base current, there is a slight dependence on the voltage between the collector and emitter. Higher V_{CE} increases the width of the junction depletion region, which in turn causes the effective base layer to become thinner [12]. With a smaller effective base layer, more e^- diffuse into the base-collector depletion region, which increases the current, as shown in Figure 17. The I_C in the active region can be calculated in terms of the Early Voltage by finding the slope of the line and adding the linear contribution to the constant amplified base current.

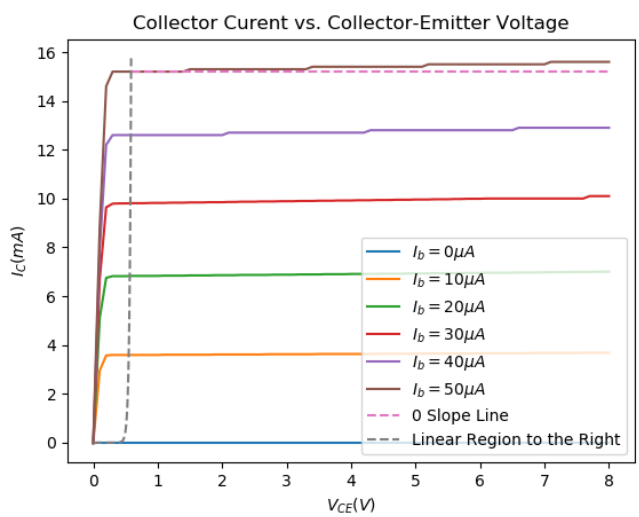


Figure 17: A plot showing the I_C as a function of V_{CE}(for different I_b). The plot was made using data pulled from an LTspice simulation of the Infineon BFP760 transistor. It is clear from this plot that the current is not constant in the saturation region, and instead has a slight positive slope due to the Early Effect.

$$I_C = \beta I_b + \frac{I_C}{V_A + V_{CE}} V_{CE} \simeq \beta I_b + \frac{I_C}{V_A} V_{CE} \tag{21}$$

The relationship in equation 21 can be described as a sum of two currents, one being the current source already in the model, the other being a current across a parallel resistor, with value $r_o = \frac{V_A}{I_C}$. So, we simply add a resistor of value r_o in parallel with the current source, as shown in Figure 18.

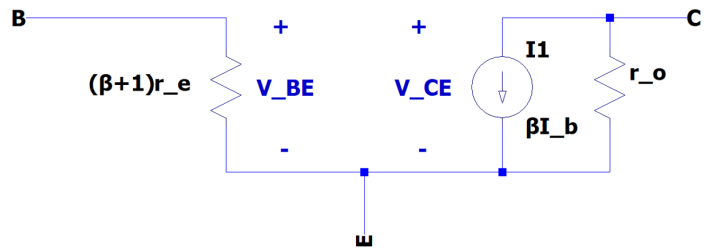


Figure 18: The full dynamic resistance model with the parallel resistor to account for the Early Effect. This model is quite accurate for small signal applications in lower frequencies.

While the model in Figure 18 works well for low frequencies, it fails in high frequencies since it does not account for capacitive effects between the semiconductor layers of the transistor [8]. To fix this, we add a capacitor between each semiconductor junction (b-e and c-b) to form the complete Hybrid-Pi Model (pictured in Figure 19).

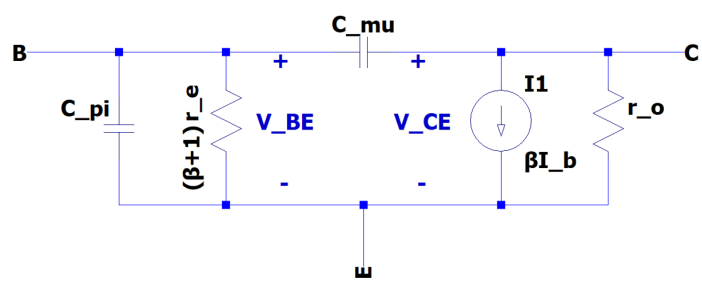


Figure 19: The Hybrid-Pi model with parasitic BJT capacitances. This is the model we used for our BJT small signal analysis.

A.2 Common Emitter Amplifier Gain Calculations

Before analyzing the open circuit gain of the amplifier ($G = \frac{V_{out}}{V_{in}}$), we first simplify the AC equivalent model. Expressing the current source dependence in terms of the voltage across $(\beta + 1)r_e$,

$$\beta i_b = \beta \frac{v_{\text{in}}}{(\beta + 1)r_e} \simeq \frac{v_{\text{in}}}{r_e} = v_{in} g_m, \qquad g_m = \frac{1}{r_e} = \frac{I_E}{V_T} \tag{22}$$

where g_m is the transconductance of the transistor, describing how small changes in input voltage cause changes in the output. This simplification decouples the current source dependence on the current through $(\beta + 1)r_e$, allowing to group impedances together for an easier nodal analysis calculation. The equivalent impedance calculations are shown in equations 23 and 24.

$$Z_{\text{eq,in}} = R_1 \parallel R_2 \parallel \frac{1}{j\omega C_\pi} \parallel (\beta + 1)r_e = 242.5 - 154.5j\,\Omega, \;\; f = 500\text{MHz} \tag{23}$$

$$Z_{\text{eq,out}} = R_C \parallel r_o \simeq R_C = 50\,\Omega,\ \forall f \tag{24}$$

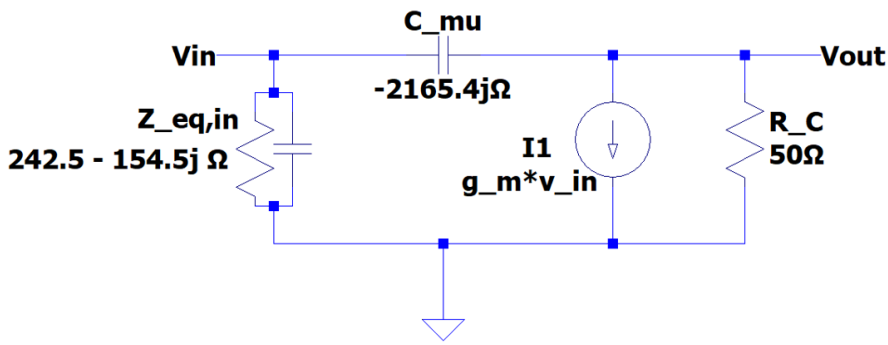


Figure 20: The Simplified AC equivalent circuit with all parallel impedances combined.

v_{out} is given by a nodal analysis on the v_{out} node (note that since this is the open circuit gain, there is no current flowing out of the amplifier) as shown in equation 25. Rearranging, the expression for the gain is given in equation 10.

$$\frac{v_{\text{out}} - v_{\text{in}}}{Z_{c\mu}} + g_m v_{in} + \frac{v_{\text{out}}}{R_C} = 0 \ \rightarrow\ \frac{v_{\text{out}}}{R_C \parallel Z_{c\mu}} = -v_{\text{in}}\left(g_m - \frac{1}{Z_{c\mu}}\right) \tag{25}$$

$$G = \frac{v_{\text{out}}}{v_{\text{in}}} = -R_C \parallel Z_{c\mu}\left(g_m - \frac{1}{Z_{c\mu}}\right) = -9.254 + 0.190j,\ f = 500\text{ MHz} \tag{26}$$

Next, we explore how loading the amplifier affects the effective gain. Figure 21 presents the models of both the input and the output. For the input, the effective input voltage ($v_{\text{in}}^{\text{eff}}$ is calculated as a function of the source and input impedance in equation 27. Note that if $R_S << Z_i$, then $v_{\text{in}}^{\text{eff}} \simeq v_{\text{in}}$. For the output, the effective output voltage ($v_{\text{out}}^{\text{eff}}$) is calculated as a function of the load and output impedance in equation 28. Note that since $R_L = Z_o$ due to the impedance matching criteria, then $v_{\text{out}}^{\text{eff}} = 0.5 v_{\text{out}}$. This means that having to match impedances at the output effectively reduces our gain by a factor of 2 (6dB). Our loaded amplifier gain is finally given in equation 29.

$$v_{\text{in}}^{\text{eff}} = \frac{v_{\text{in}} Z_i}{Z_i + R_s} \tag{27}$$

$$v_{\text{out}}^{\text{eff}} = \frac{v_{\text{out}} R_L}{R_L + Z_o} \tag{28}$$

$$G_{\text{eff}} = \left(\frac{Z_i}{Z_i + R_s}\right)\left(\frac{v_{\text{out}} R_L}{R_L + Z_o}\right) G \ \rightarrow\ |G_{\text{eff}}| = (0.985)(0.5)|G| = 4.558 = 13.17\text{ dB} \tag{29}$$

A.3 Single Transistor Amplifier Topologies

There are three main topologies of single stage amplifiers for both BJTs and FETs. The characteristics of the different topologies are summarized in Table 5. Each topology is displayed in Figure 22.

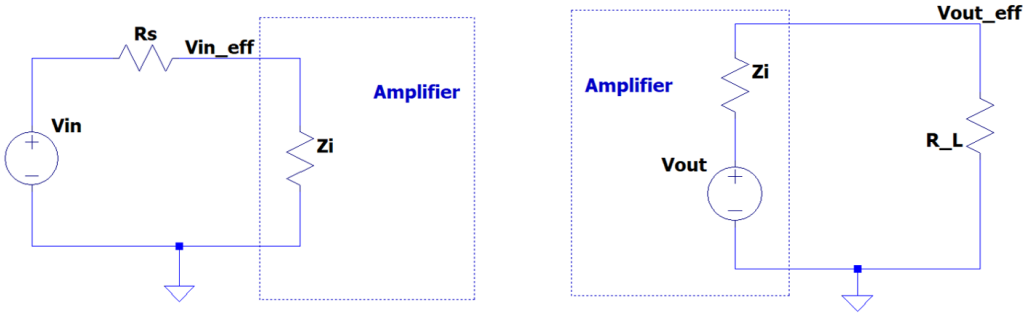


Figure 21: Left: The input portion of the amplifier circuit can be modelled effectively as a voltage divider. A low input impedance will result in loading the source and having a smaller voltage at the input of the amplifier than what is delivered by the source. Right: The output portion of the circuit can also be modelled as a voltage divider, this time with the source being the amplifier itself. Thus, a low output impedance is desirable so that there is a negligible voltage drop due to the load.

Topology	Voltage Gain	Current Gain	Input Resistance	Output Resistance
Common Source/Collector	$A_v > 1$	$A_i > 1$	Moderate	Moderate
Source/Emitter Follower	$A_v \approx 1$	$A_i > 1$	Moderate to high	Low
Common Gate/Base	$A_v > 1$	$A_i \approx 1$	Low	Moderate to high

Table 5: Characteristics for three common single transistor amplifiers [8]

The emitter follower configuration provides voltage gain ≤1 and is ineffective as a single stage [8]. One possible use for this topology is a voltage buffer at the final stage of amplification to aid in impedance matching at the output. The common base configuration has low input impedance and therefore will result in poor gain performance for a single stage (as shown by equation 29. However, this topology is particularly good for high frequency applications since it bypasses the parasitic feedback capacitance between the base and collector that is present in the other two topologies [8]. Thus, this configuration performs well as a second, high gain stage in a multi-transistor amplifier for improved frequency response. The common emitter amplifier provides a compromise between all amplifier characteristics, and therefore is the most effective of the three topologies as a single stage.

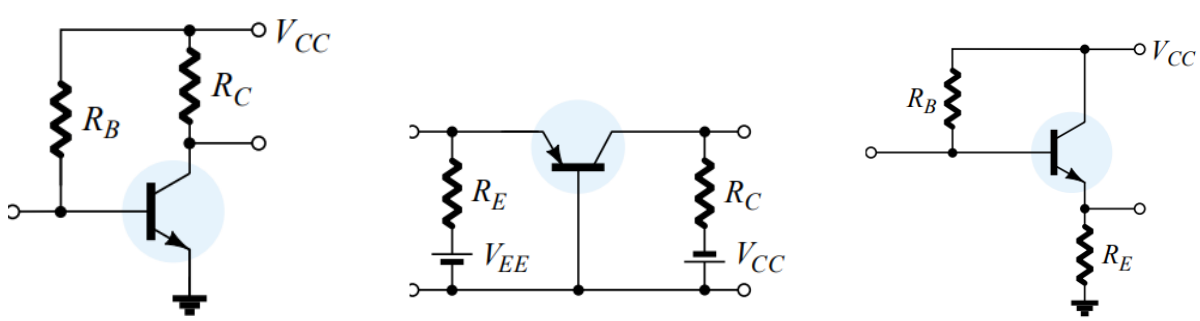


Figure 22: Left: A basic common emitter topology. Middle: A basic common base topology. Right: A basic emitter follower topology [8].

A.4 The Junction Field Effect Transistor

The n-channel JFET is comprised of the n-type channel between the drain and the source with p-type surrounding the sides of the cylindrical n-channel. Its operation is based on reverse-biasing the PN-junction at the gate and behaves similarly to that of a hose faucet.

When there is a positive drain-source voltage v_{DS}, the source is set to ground and the total instantaneous gate-source voltage $v_{GS} = 0$, the applied voltage at the drain will cause current to flow from the drain to source. N-channel JFETs are normally active with $v_{GS} = 0$. If we apply a negative v_{GS}, the PN-junction will become reverse biased and the depletion region will widen.

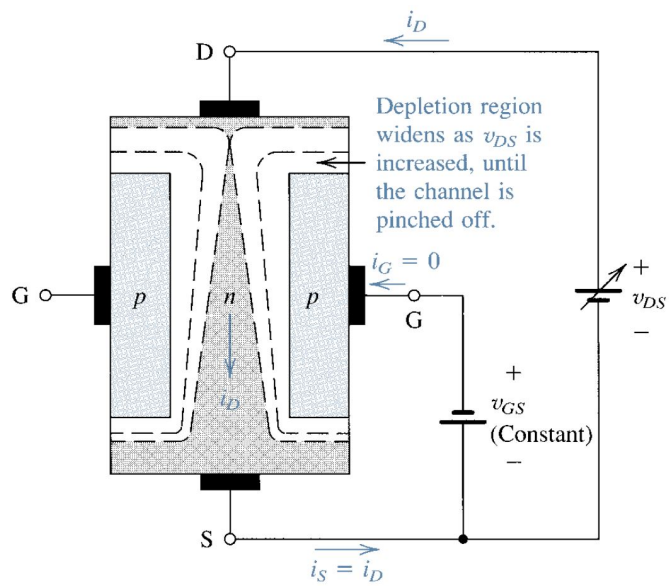


Figure 23: Physical operation of a JFET [23].

As the v_{GS} becomes more negative, the electric field from the drain to the gate will increase and e^- from the gate will be pushed towards the drain, widening the depletion region. At some critical point the depletion region increases to obstruct the entire channel, so no current can flow. This is called the pinchoff voltage (in reality the width of the channel is non-zero but is very small).

But, the JFET suffers from channel width modulation. At larger v_{DS}, there is a noticeable difference in widths of the depletion region. We can model the n-type channel as a series of resistors, with the voltage the greatest at the top. The electric field pointing from the drain to the gate is larger than that near the bottom due to the resistor voltage drops, which causes the narrowness of the channel near the top. With a constant v_{GS} below the pinchoff voltage and a large v_{DS}, the reverse-bias at the drain end v_{GD} falls beneath the pinchoff voltage. The depletion region widens to a maximum and the drain current saturates. Although the depletion region has "pinched off" the channel, the electric field from the drain to source is very high, and conduction continues.

If we attempt to apply a positive V_{GS}, the PN-junction becomes forward biased and the gate ceases to have control over the channel. The maximum V_{GS} of an n-channel JFET is typically 0V.

For the characteristics above, JFETS typically have better noise performance than BJTs because charge carriers in the BJT must travel across two PN junctions, so the possibility of additional thermal noise due to collisions is higher. The gate current of the JFET is very small compared to the BJT as it is a

voltage-controlled device. In fact, due to the reverse-biased PN-junction, n-channel JFETs experience reverse gate current.

For the purposes of our JFET will always be biased in the saturation region of operation to serve as an amplifier. In the linear region, the drain current will have a dependence on the drain voltage, which is unwanted. Under ideal conditions, JFET is modelled by the following equation for its drain current:

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 \tag{30}$$

where V_P is the pinchoff voltage (the value v_{GS} at which $i_D = 0$) and I_{DSS} is the saturation drain current when $V_{GS} = 0$. This equation allows us to derive the transconductance for the JFET (an ohmic relationship between the input voltage signal v_{gs} and the output current i_d) as:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GSQ}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{31}$$

A.4.1 Common Source Amplifier Gain

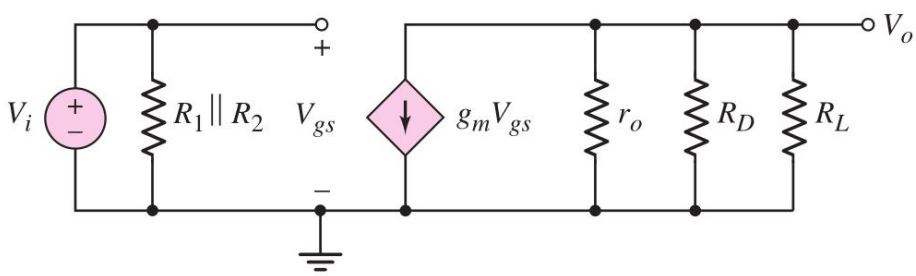


Figure 24: Common source JFET amplifier small signal equivalent model

Applying Kirchoff's Voltage Law around the output loop, we obtain $v_o = -g_m v_{gs}(r_o \parallel R_D \parallel R_L)$ (negative sign from reversed current flow). Since $v_{gs} = v_i$ we compute the gain:

$$\frac{v_o}{v_i} = A_v = -g_m(r_o \parallel R_D \parallel R_L) \tag{32}$$

where r_o is the output resistance of the JFET defined as:

$$r_o = \left.\left(\frac{\partial i_D}{\partial v_{GS}}\right)^{-1}\right|_{v_{GS}=\text{const}} = \left[\lambda I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]^{-1} = \frac{1}{\lambda I_{DQ}} \tag{33}$$

We see that the gain is linearly related to the JFET's transconductance. In the design, we control V_{GS} and the other parameters are specified by the datasheets. Although this model ignores the transistor capacitances, it describes the relationship between the transconductance and the load resistors. If we assume r_o is much larger than R_D and R_L, then the gain is dependent on the minimum of R_D and R_L. If we wish to use a single transistor design, then R_D must match the impedance of the transmission cable at 50Ω. The transconductance of a low-noise JFET (LSK170A) is approximately 20 mS, so the gain would be approximately 1, which fails to meet the design requirements. This supports the pursuit of a multi-stage design.

A.5 Transmission Line

A.5.1 Impedance

A transmission line can be modelled with an equivalent circuit as shown in Figure 25.

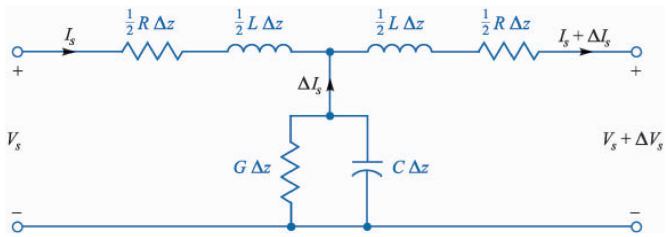


Figure 25: A unit length of a transmission line can be modelled as an equivalent circuit like this, where Δz is the distance along the transmission line (horizontally) [16].

Any transmission line has a characteristic impedance, described by the equation:
[16]

$$Z_0 = \sqrt{\frac{R + jwL}{G + jwC}} = \frac{1}{Y_0} \tag{34}$$

where Y_0 is the characteristic admittance.

A.5.2 Smith Chart

A Smith chart is a graphical tool to show how the impedance of the transmission line changes as various components are added/removed, or when the frequency is varied. It then relates the impedance values to the reflection coefficient, Γ. We define z_L, the normalized load impedance:

$$z_L = \frac{Z_L}{Z_0} = r + jx \tag{35}$$

where r and x are the real(resistance) and imaginary(reactance) components of z_L. Rearranging equations 17 and 35, we obtain:

$$\Gamma = \frac{z_L - 1}{z_L + 1} \tag{36}$$

The basis of the Smith chart is the polar representation of Γ. Breaking Γ into real and imaginary components:

$$\Gamma = \Gamma_r + j\Gamma_i \tag{37}$$

Rearranging equations 35, 36, and 37 results in:

$$\left(\Gamma_r - \frac{r}{1+r}\right)^2 + \Gamma_i^2 = \left(\frac{1}{1+r}\right)^2 \tag{38}$$

and

$$(\Gamma_r - 1)^2 + \left(\Gamma_i - \frac{1}{x}\right)^2 = \left(\frac{1}{x}\right)^2 \tag{39}$$

These equations produce a set of lines on the Γ plane as shown in the figures below.

Together, they make the Smith Chart. The steps to use the Smith Chart is the following.

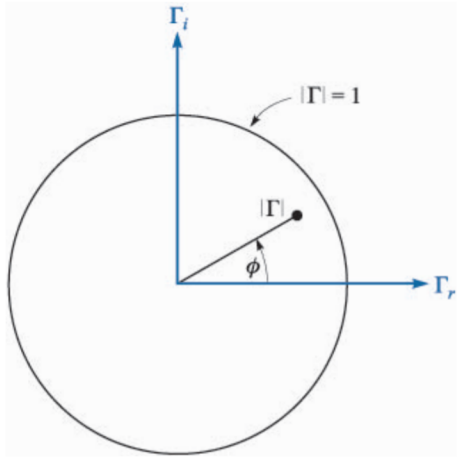
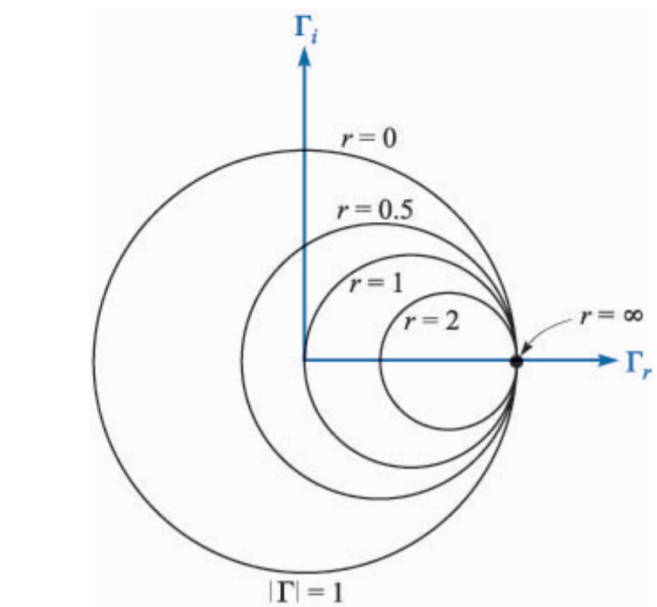
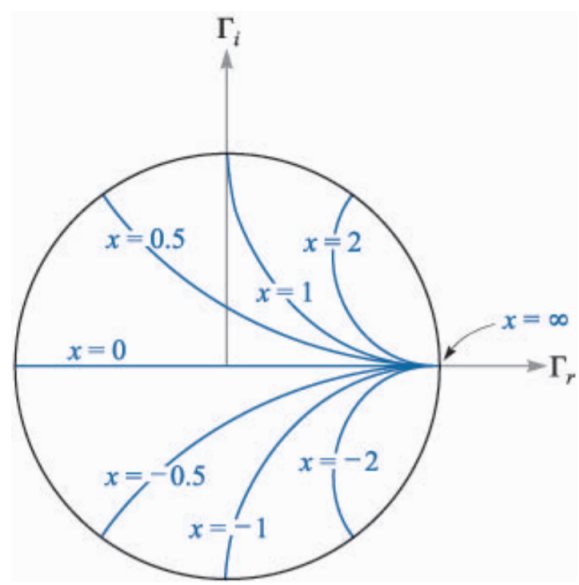


Figure 26: Γ in polar coordinates, where the unit circle is when $|\Gamma| = 1$, meaning all of the voltage wave is reflected back [16].



(a) A set of lines produced by equation 38 [16].



(b) A set of lines produced by equation 39 [16].

Figure 27

1. Normalize Z_L by equation 35
2. Plot z_L by finding the intersection point of r and x
3. Check how adding various components move z_L along the chart to get it closest to the center point, which means the impedance has been matched.

The following are some of the general guidelines on how the various circuit components affect movement on the Smith Chart.

1. If adding things in series: Series inductor/capacitor components move the point along constant r circles (L clockwise, and C counterclockwise)

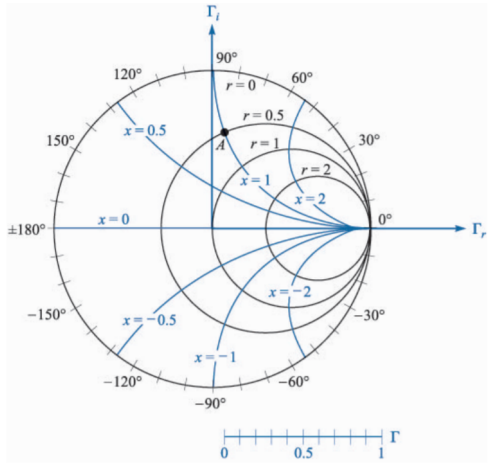


Figure 28: Smith Chart. $x = 0$ (left most point) representing a short circuit and $x = \infty$ (right most point) representing an open circuit [16].

2. If adding things in parallel: You first have to convert z_L to y_L (admittance) by drawing a circle which the center is the center of the Γ plot, and z_L is on the circumference. When you draw a straight line from z_L, passing the center point, to the opposite end of the circle, that is y_L. We can convert the entire chart to show admittance by mirroring it along the y-axis. Parallel inductor/capacitor components move y_L along constant conductance circles (L counterclockwise, and C clockwise)

A.6 Testing and Validation

While the AC characteristics of a transistor need to be tested with a more carefully designed PCB, the DC characteristics can be tested with protoboards. A simple PCB simply to interface between SMT and through-hole components (Figure 29) was ordered, and the rest of the circuit was designed based on LTspice simulations.

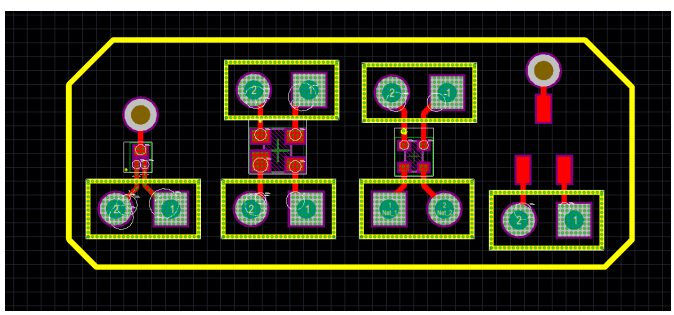


Figure 29: Testing PCB schematic for interfacing between SMT transistors of varying package types and through-hole components on a protoboard.