

ADVANCED CPU ARCHITECTURE AND HARDWARE ACCELERATORS LABRATORY

Preparation Report LAB 4

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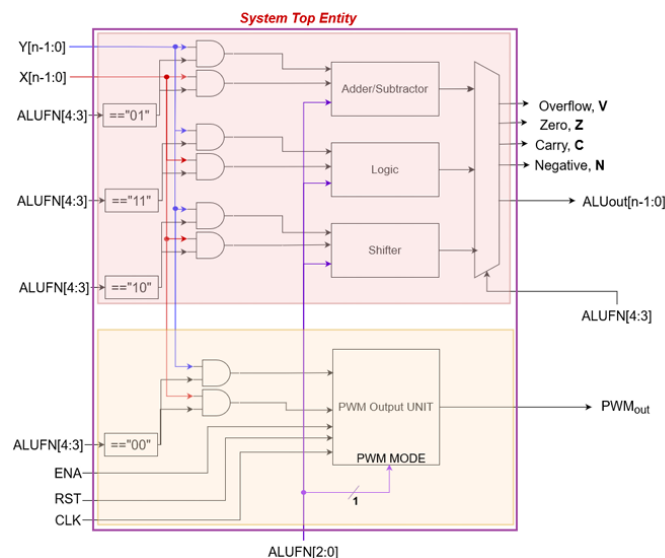
רקע

מטרות המעבדה הן הבנה של סינטזה דיגיטלית והתנסות עם FPGA. במעבדה זו, לקחנו את הקבצים של מעבדה 1 ומה שמימשנו בהם והוספנו להם מימוש נוסף של הוצאת תדר PWM, עטפנו את המימוש החדש כיחידה אחת וצרבנו ל FPGA, ניתחנו נתונים ובדקנו ביצועים.

פירוט ה-Modules הקיימים במערכת

- Top envelope
- Top
- Pwm envelope
- רכיבי מימוש פנימיים

על כל הקומפוננטות קיים הסבר מפורט בקובץ readme.txt



צילומי מסך עבור מימוש המערכת לפני חיבורה ל-FPGA:

The screenshot displays the Quartus Prime IDE interface during the compilation of an FPGA project. The Project Navigator on the left shows the file structure with VHDL files for the Design Under Test (DUT). The Tasks window in the center lists the compilation steps, all of which are marked as successful. The Compilation Report - top window provides a detailed summary of the compilation flow, including the status, version, and various resource utilization metrics. The Messages window at the bottom shows the real-time output of the compilation process, including the completion of post-fitting delay annotations and the successful execution of the Fitter and Assembler.

איור 1: תיאור מעבר קומפילציה תקינה של המערכת

Project Navigator Files

- ../DUT/top.vhd
- ../DUT/Shifter.vhd
- ../DUT/PWMEV.vhd
- ../DUT/PWM.vhd
- ../DUT/Logic.vhd
- ../DUT/FA.vhd
- ../DUT/counter.vhd

Tasks Compilation

- Task
- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings

Compilation Report - top

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Flow Messages
- Flow Suppressed Messages

Flow Summary

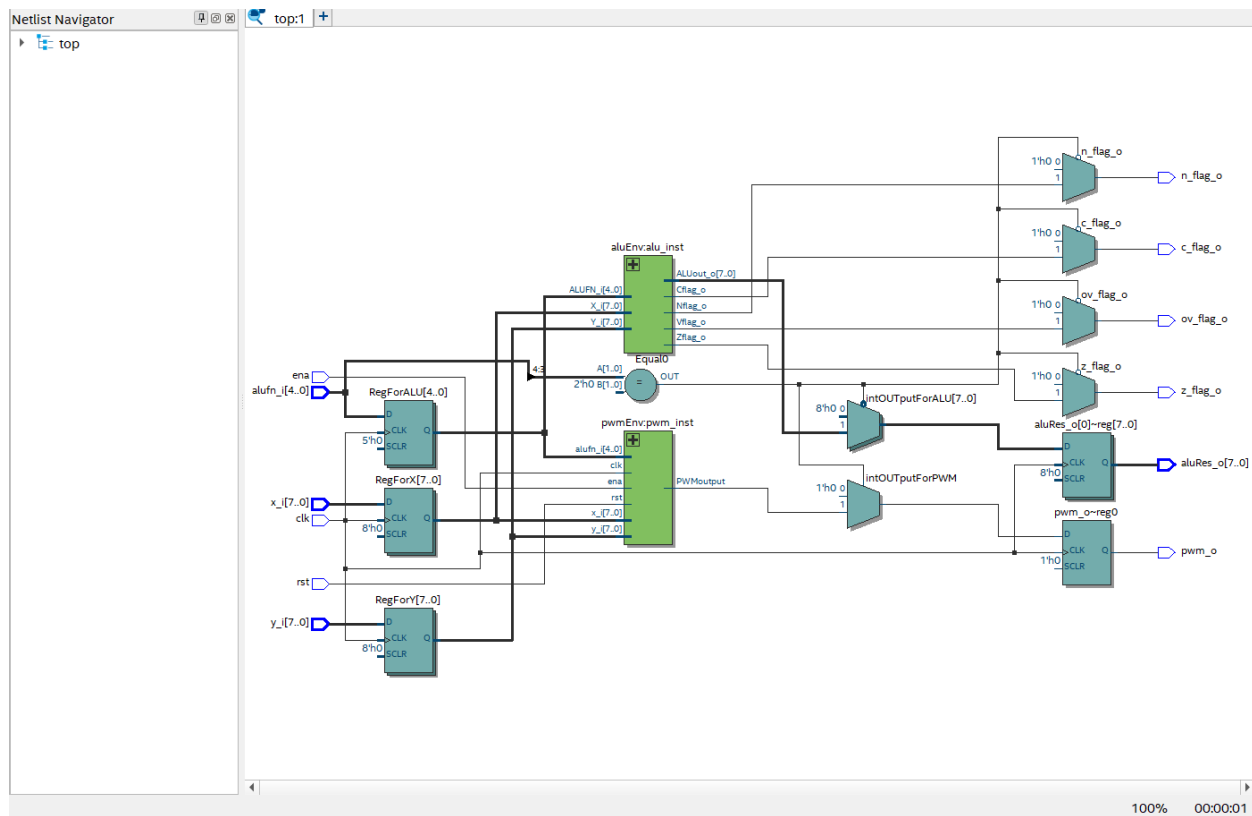
<<Filter>>

Flow Status	Successful
Quartus Prime Version	21.1.0 Build
Revision Name	top
Top-level Entity Name	top
Family	Cyclone V
Device	5CSXFC6D
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	39
Total pins	37
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0

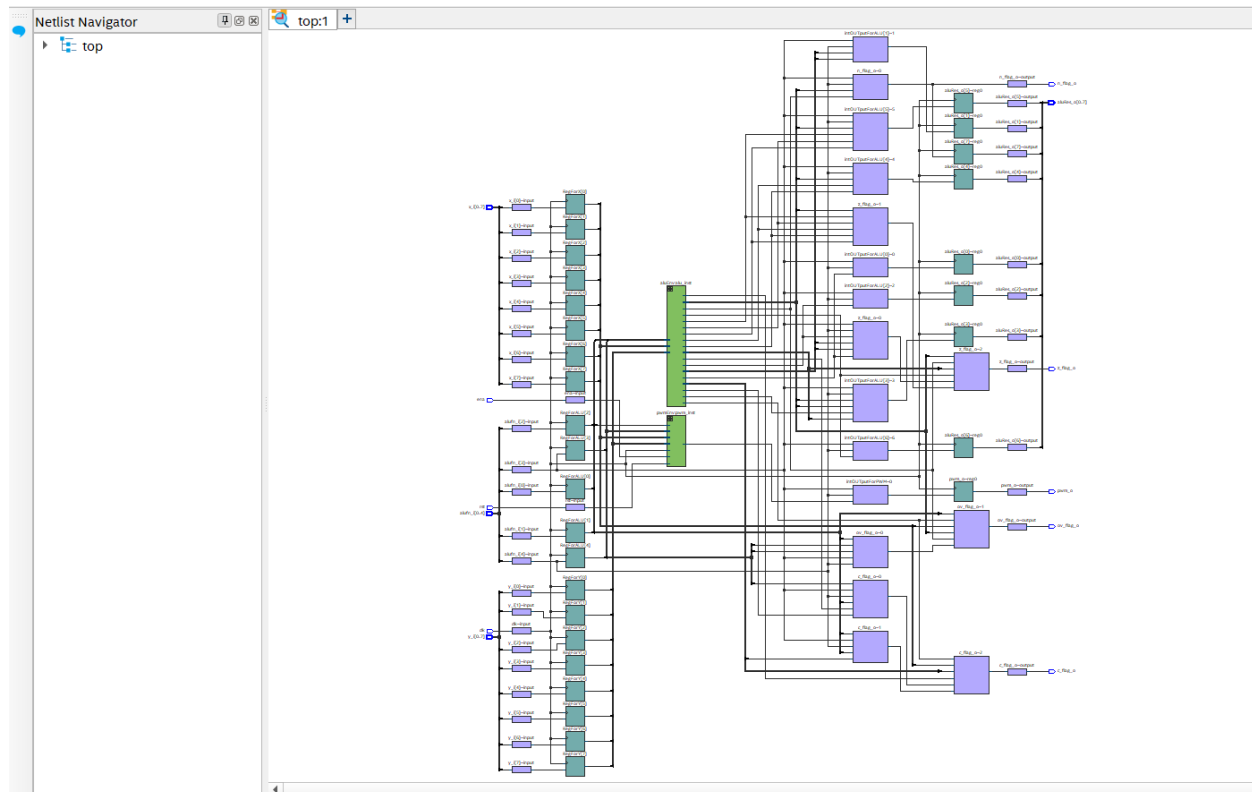
All <<Filter>> Find... Find Next

Type	ID	Message
i	12128	Elaborating entity "aluEnv" for hierarchy "aluEnv:alu_inst"
i	12128	Elaborating entity "AdderSub" for hierarchy "aluEnv:alu_inst AdderSub:AddSub_inst"
i	12128	Elaborating entity "FA" for hierarchy "aluEnv:alu_inst AdderSub:AddSub_inst FA:FA_inst"
i	12128	Elaborating entity "shifter" for hierarchy "aluEnv:alu_inst shifter:Shift_inst"
i	12128	Elaborating entity "LOGIC" for hierarchy "aluEnv:alu_inst LOGIC:Boolean_inst"
i	12128	Elaborating entity "pwmEnv" for hierarchy "pwmEnv:pwm_inst"
w	10540	VHDL Signal Declaration warning at PWMEnv.vhd(18): used explicit default value
i	12128	Elaborating entity "pwm" for hierarchy "pwmEnv:pwm_inst pwm:pwm_inst"
i	286030	Timing-Driven Synthesis is running
i	16010	Generating hard_block partition "hard_block:auto_generated_inst"
i	21057	Implemented 182 device resources after synthesis - the final resource count might change
i		Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings

איור 2 : תיאור מעבר סינטזה תקין של המערכת.



איור 3 : תיאור RTL VIEW



איור 4 : תיאור נוסף של RTL

Quartus Prime Lite Edition - C:/Users/elado/Desktop/vhdl_lab/CPUArchitecture-VHDL/LAB4FPGAQuartusMemo...

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

top

Project Navigator

Files

- SDC1_LAB4.sdc
- ../DUT/top.vhd
- ../DUT/Shifter.vhd
- ../DUT/PWMenv.vhd
- ../DUT/PWM.vhd
- ../DUT/Logic.vhd
- ../DUT/FA.vhd
- ../DUT/counter.vhd
- ../DUT/aux_package.vhd
- ../DUT/ALUenv.vhd
- ../DUT/AdderSub.vhd

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer

Compilation Report - top

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- Flow Summary
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Flow Summary

<<Filter>>

Flow Status	Successful - 1
Quartus Prime Version	21.1.0 Build 1
Revision Name	top
Top-level Entity Name	top
Family	Cyclone V
Device	5CSXFC6D6F
Timing Models	Final
Logic utilization (in ALMs)	83 / 41,910 (0 %)
Total registers	39
Total pins	37 / 499 (7 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

Messages

All

<<Filter>>

Find... Find Next

Type	ID	Message
Information		Quartus Prime Timing Analyzer was successful. 0 errors, 1 warning
Information		*****
Information		Running Quartus Prime EDA Netlist Writer
Information		Command: quartus_eda --read_settings_files=off --write_settings_files=off LAB4_
Warning	18236	Number of processors has not been specified which may cause overloading on shar
Information	204019	Generated file top.vho in folder "C:/Users/elado/Desktop/vhdl_lab/CPUArchitectu
Information		Quartus Prime EDA Netlist Writer was successful. 0 errors, 1 warning
Information	293000	Quartus Prime Full Compilation was successful. 0 errors, 9 warnings

System Processing (132)

100% 00:01:00

איור 5 : תיאור נוסף עם SDC

Compilation Report - top X

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- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
 - Summary
 - Parallel Compilation
 - SDC File List
 - Clocks
 - Slow 1100mV 85C Model
 - Fmax Summary**
 - Timing Closure Reco
 - Setup Summary
 - Hold Summary
 - Recovery Summary
 - Removal Summary
 - Minimum Pulse Width
 - Metastability Summa
 - Slow 1100mV 0C Model
 - Fmax Summary
 - Setup Summary

Slow 1100mV 85C Model Fmax Summary

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	Fmax	Restricted Fmax	Clock Na
1	167.62 MHz	167.62 MHz	clk

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for

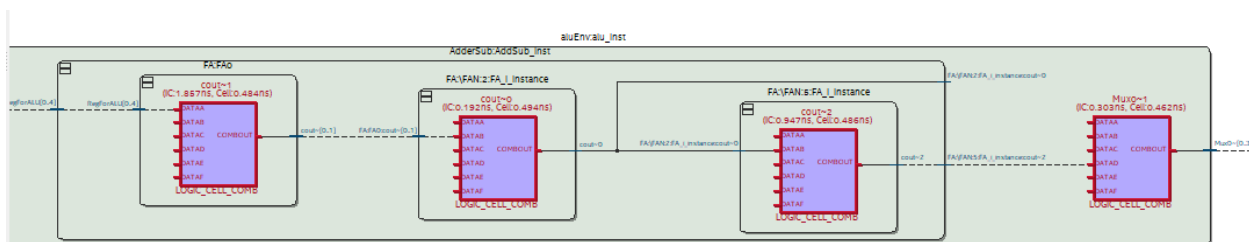
איור 6 : תיאור של ניתוח זמנים ופירוט FMAX

▼ Combinational ALUT usage for logic	124	
-- 7 input functions	0	
-- 6 input functions	55	
-- 5 input functions	11	
-- 4 input functions	34	
-- <=3 input functions	24	
Combinational ALUT usage for route-throughs	0	
▼ Dedicated logic registers	39	
▼ -- By type:		
-- Primary logic registers	39 / 83,820	< 1 %
-- Secondary logic registers	0 / 83,820	0 %
▼ -- By function:		
-- Design implementation registers	39	
-- Routing optimization registers	0	

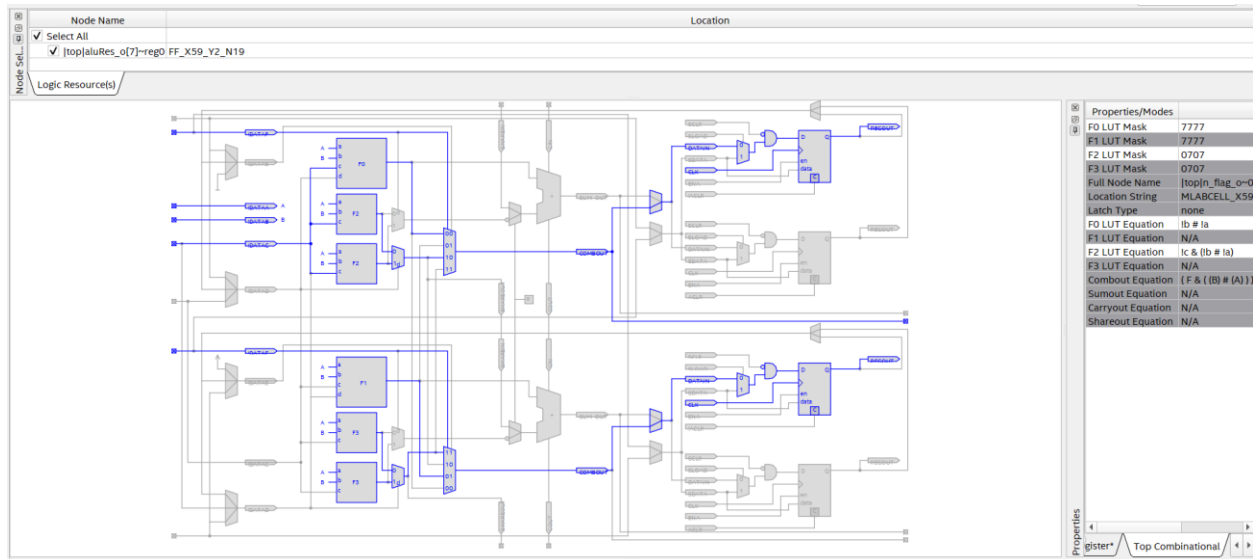
איור 7 : תיאור א של USAGE למערכת

Fitter Resource Usage Summary			
<<Filter>>			
	Resource	Usage	%
1	Logic utilization (ALMs needed / total ALMs on device)	83 / 41,910	< 1 %
2	▼ ALMs needed [=A-B+C]	83	
1	▼ [A] ALMs used in final placement [=a+b+c+d]	85 / 41,910	< 1 %
1	[a] ALMs used for LUT logic and registers	13	
2	[b] ALMs used for LUT logic	65	
3	[c] ALMs used for registers	7	
4	[d] ALMs used for memory (up to half of total ALMs)	0	
2	[B] Estimate of ALMs recoverable by dense packing	2 / 41,910	< 1 %
3	▼ [C] Estimate of ALMs unavailable [=a+b+c+d]	0 / 41,910	0 %
1	[a] Due to location constrained logic	0	
2	[b] Due to LAB-wide signal conflicts	0	
3	[c] Due to LAB input limits	0	
4	[d] Due to virtual I/Os	0	
3			
4	Difficulty packing design	Low	
5			
6	▼ Total LABs: partially or completely used	13 / 4,191	< 1 %
1	-- Logic LABs	13	
2	-- Memory LABs (up to half of total LABs)	0	
7			
8	▼ Combinational ALUT usage for logic	124	

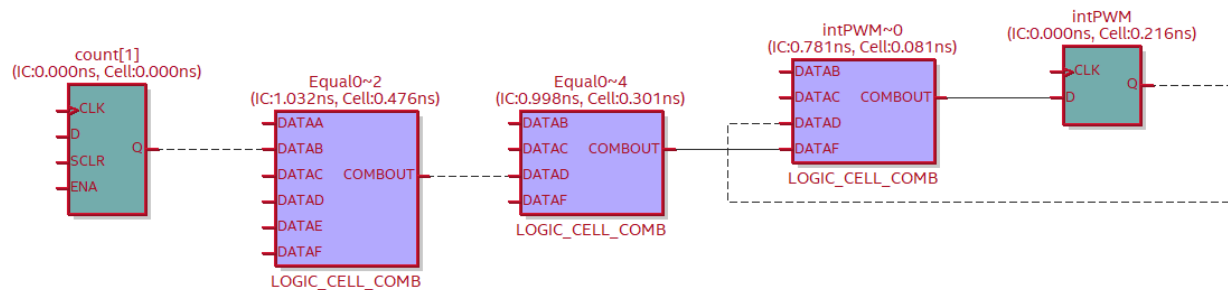
איור 8: תיאור ב ל USAGE למערכת



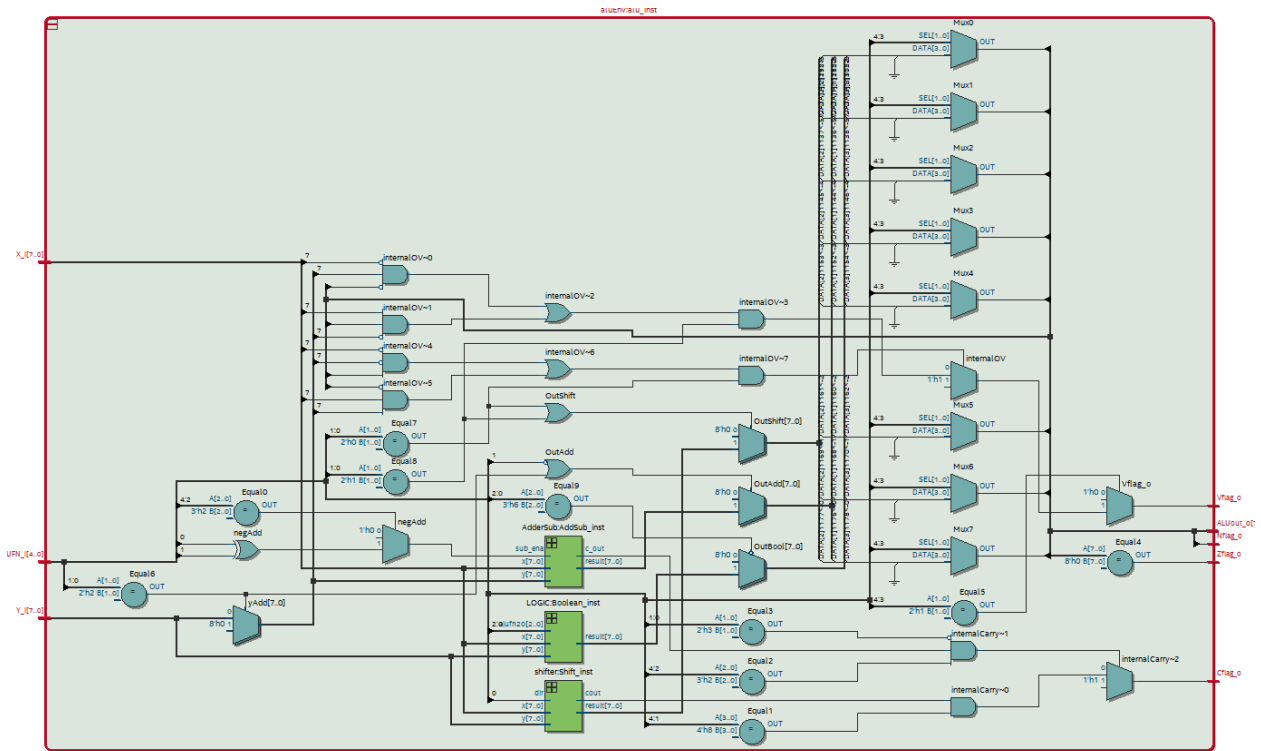
איור 9: תיאור כללי למערכת ל CRITICAL PATH ע"י VIEWER



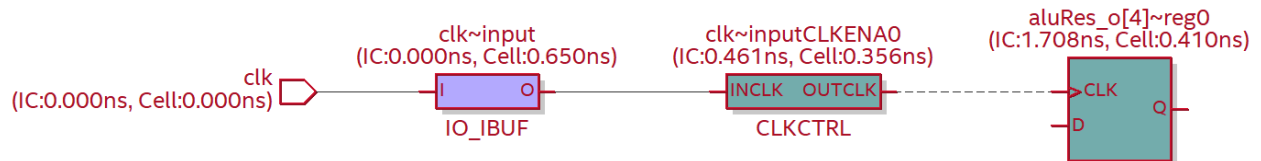
איור 10 : תיאור כללי למערכת ל CRITICAL PATH בצורה נוספת



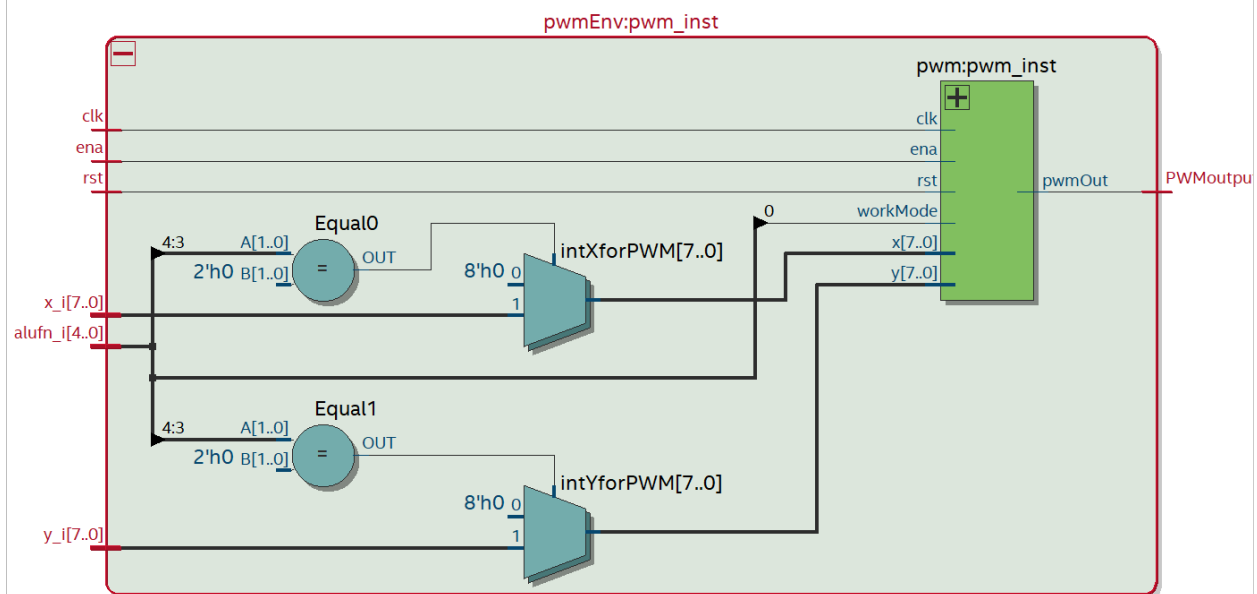
איור 11 : תיאור של CRITICAL PATH PWM



איור 12 : תיאור של ALU ע"י RTL



איור 13 : דרך נוספת להציג CRITICAL PATH



איור 14 : הצגת PWM ע"י RTL

כעת ביצענו שינויים בקוד לטובת התאמה ל FPGA , עטפנו את הקוד בצורה כזו שתתאים לבניסות היציאות של הFPGA לפי הדרישה מטה בעבודה :

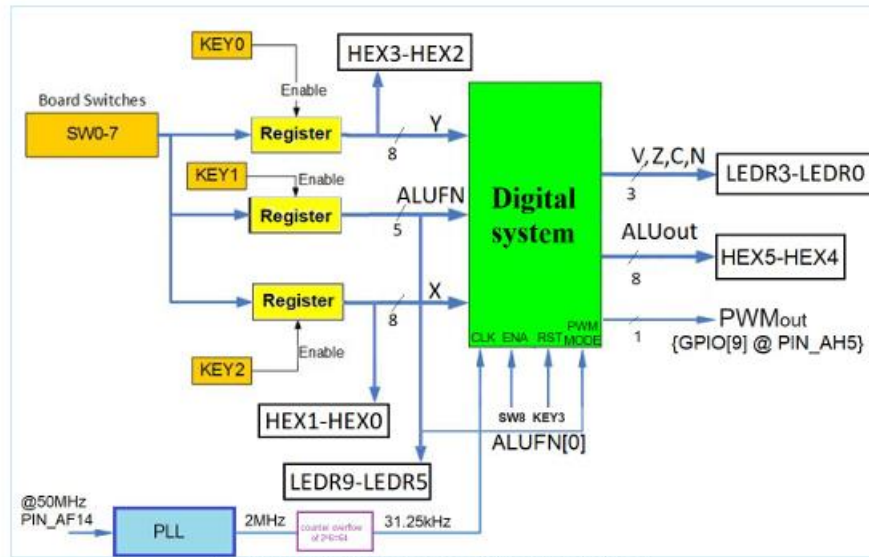
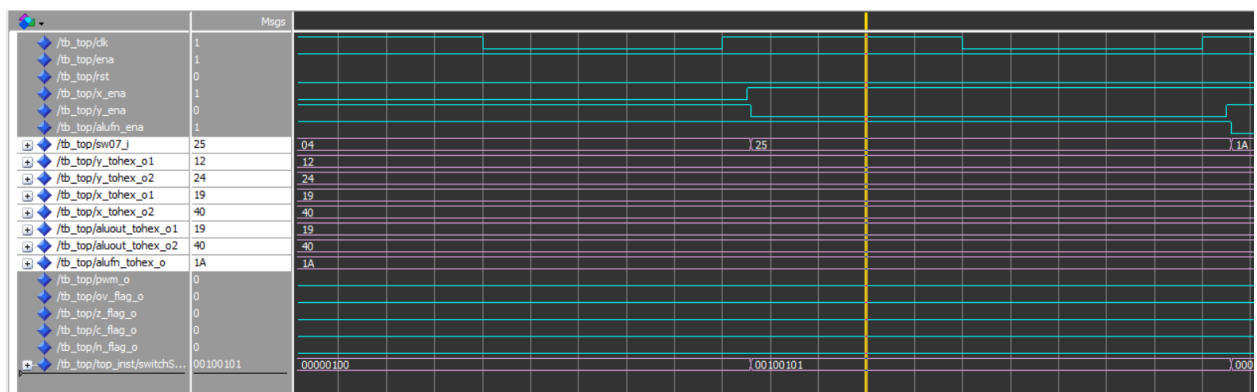
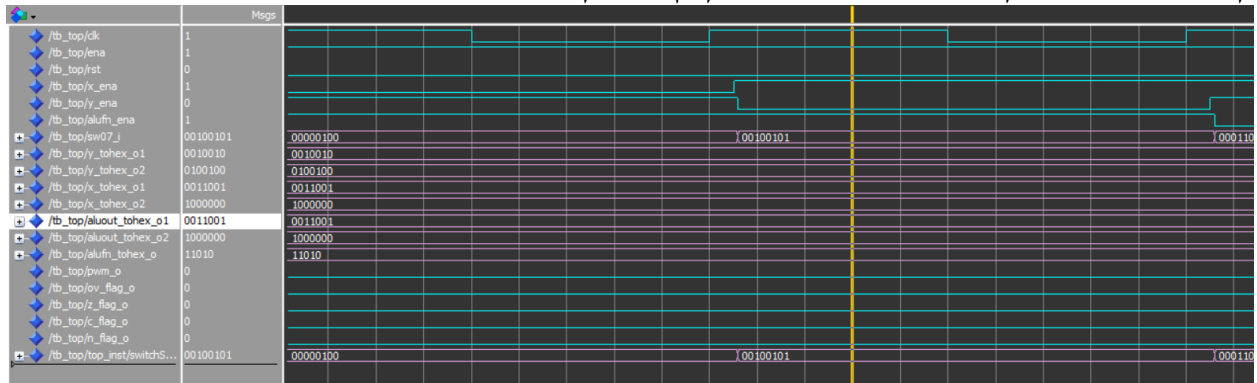


Figure 3: Digital system with I/O interface

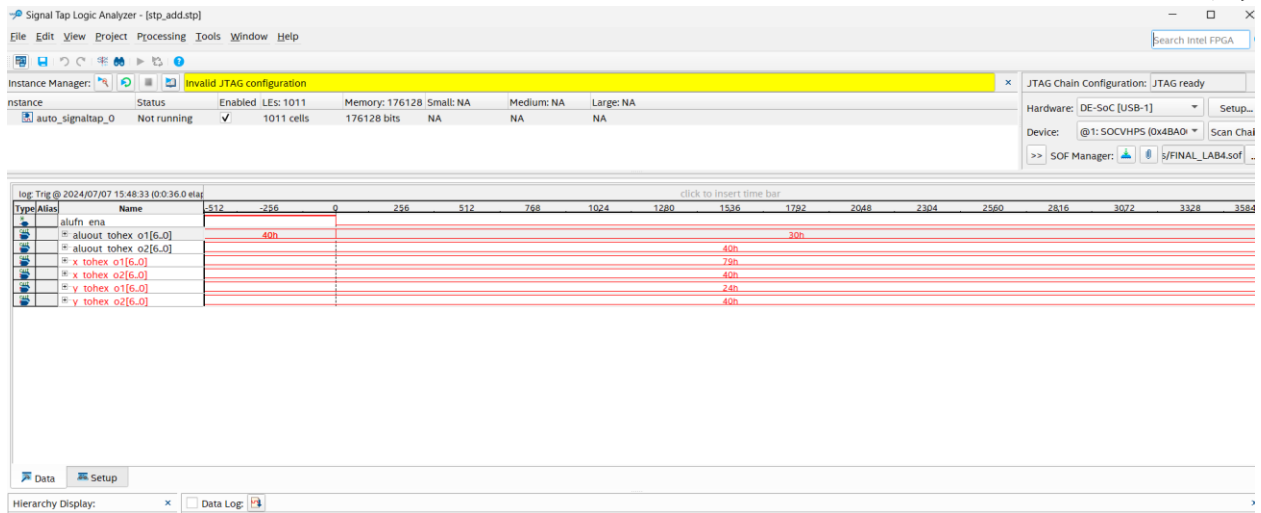
קימפלנו וביצענו בדיקות ב MODELSIM עי"י קובץ TB וקיבלנו את התוצאות הנ"ל:



כאן ניתן לראות את תוצאת AND עי"י ה ALU במערכת התוצאת מוצגת ב aluout_tohex

עבור בדיקה של הקוד שלנו על ה FPGA קיבלנו 2 קבצי STP עבור ADD ו SHIFT ,

עבור ADD



עבור SHIFT :

