

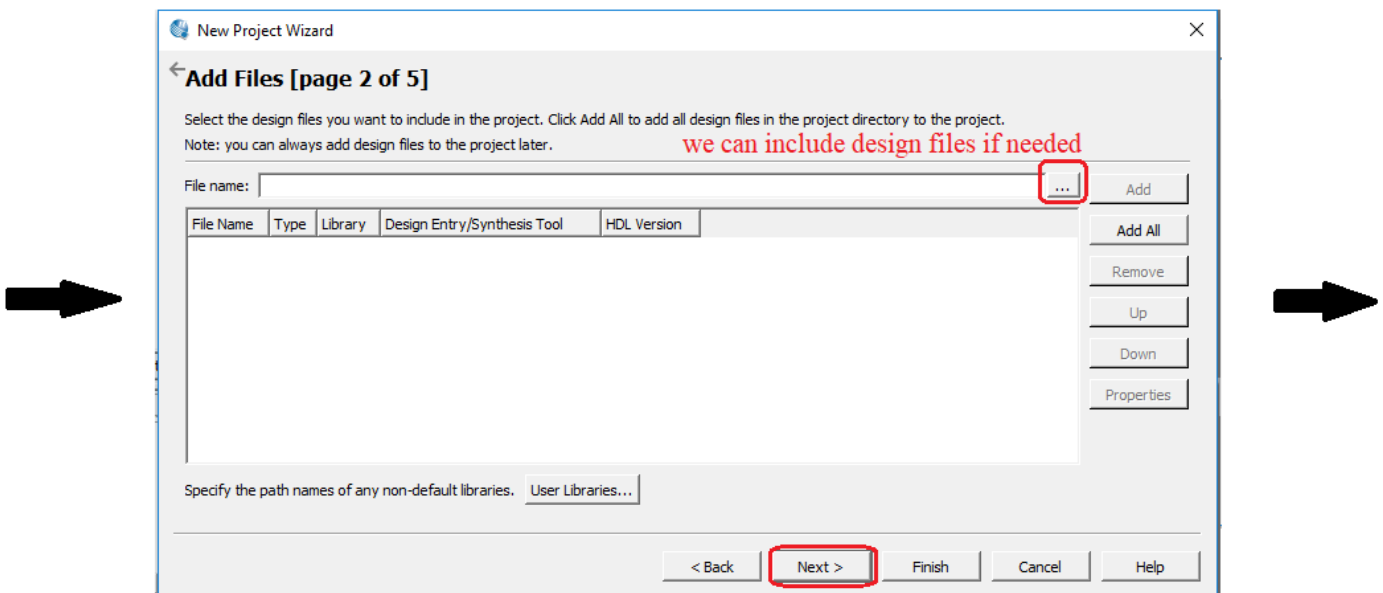
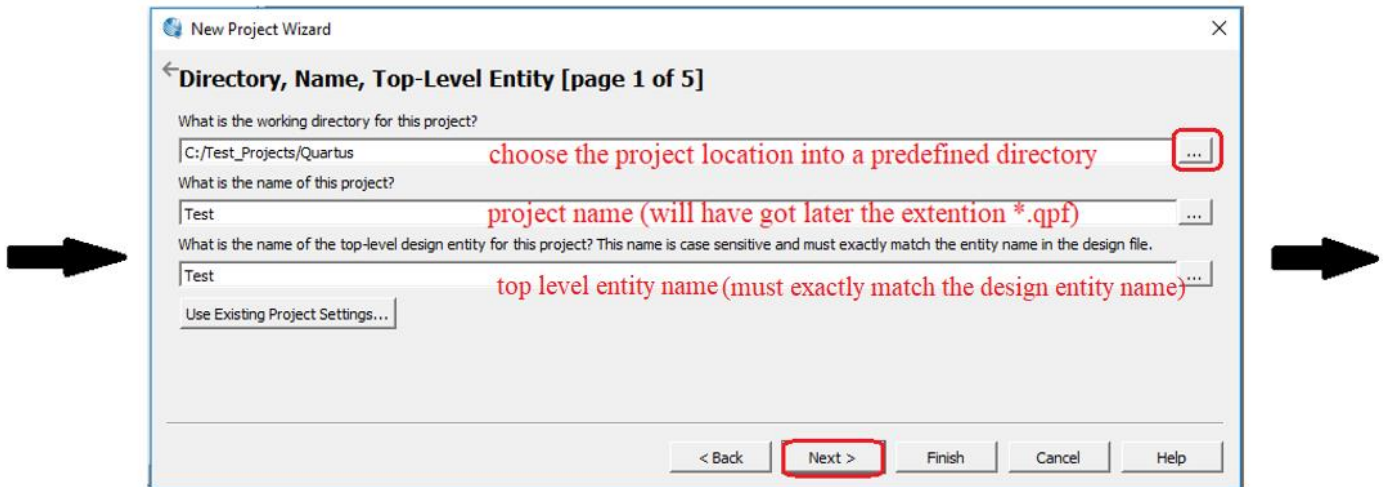
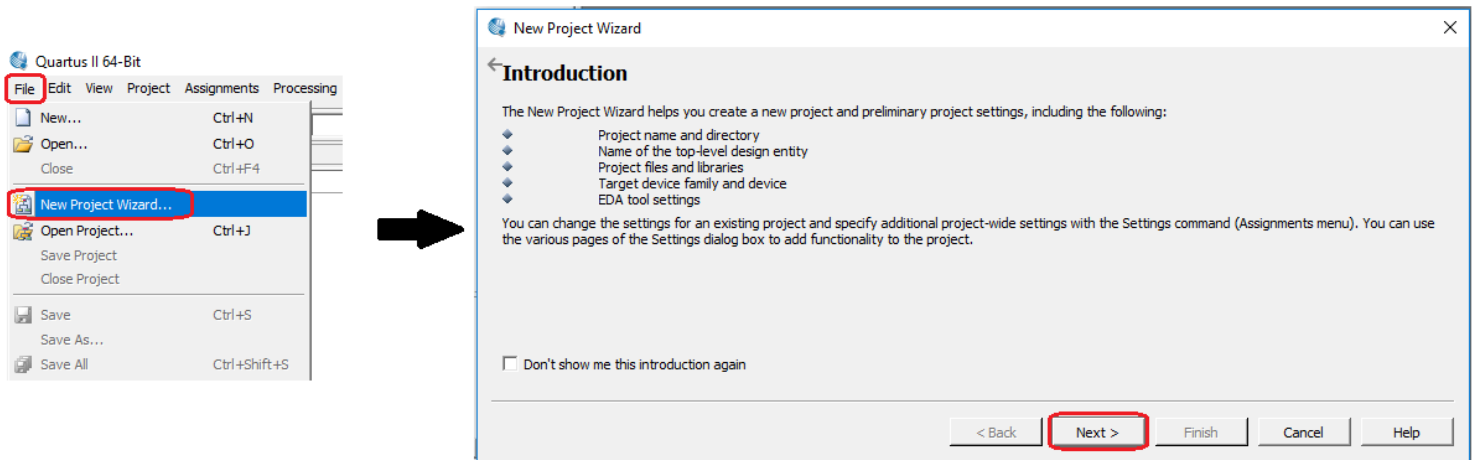
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Quartus - Create or Open a Project

A. Create a New Project:

1. Step 1 – create a new project and add VHDL files:



New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Core speed grade: Any

Name filter:

☒ Show advanced devices

Device and Pin Options...

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	PCIe Hard IP Blocks	Memory Controllers	Memory Bits
5CSXFC6C6U23I7ES	1.1V	41910	342	314	6	6	1	2	5662720
5CSXFC6C6U23I7L	1.1V	41910	342	314	6	6	1	2	5662720
5CSXFC6D6F31A7	1.1V	41910	499	457	9	9	2	2	5662720
5CSXFC6D6F31C6	1.1V	41910	499	457	9	9	2	2	5662720
5CSXFC6D6F31C7	1.1V	41910	499	457	9	9	2	2	5662720
5CSXFC6D6F31C8	1.1V	41910	499	457	9	9	2	2	5662720
5CSXFC6D6F31C8ES	1.1V	41910	499	457	9	9	2	2	5662720
5CSXFC6D6F31I7	1.1V	41910	499	457	9	9	2	2	5662720
5CSXFC6D6F31I7ES	1.1V	41910	499	457	9	9	2	2	5662720
5CEBA5F23C7	1.1V	29080	240	240	0	0	0	0	4567040
5CFRA5F23C8	1.1V	29080	240	240	0	0	0	0	4567040

< Back Next > Finish Cancel Help

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel Help

New Project Wizard

Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory: C:/Test_Projects/Quartus

Project name: Test

Top-level design entity: Test

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: Cyclone II

Device: EP2C20F484C7

EDA tools:

Design entry/synthesis: <None> (<None>)

Simulation: ModelSim-Altera (VHDL)

Timing analysis: 0

Operating conditions:

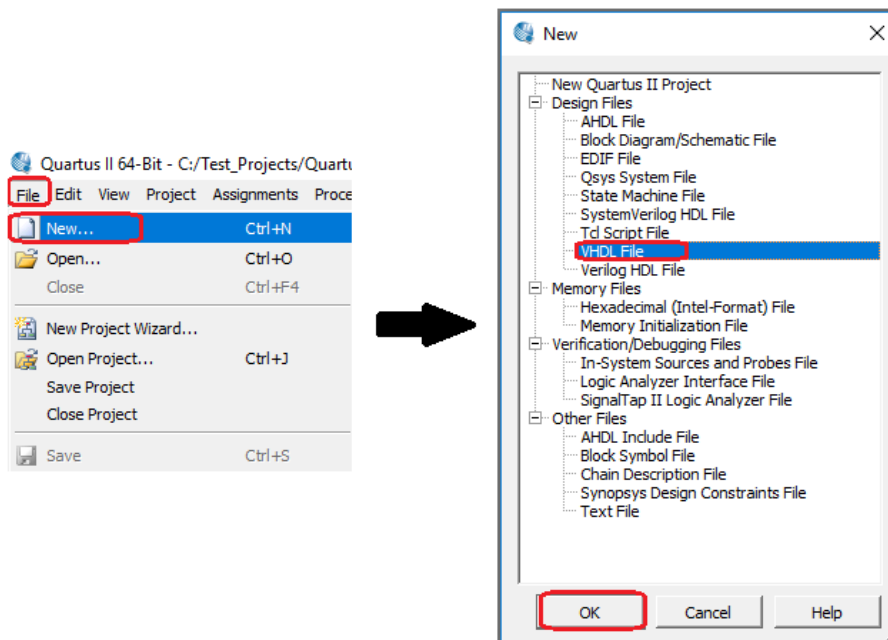
Core voltage: 1.2V

Junction temperature range: 0-85 °C

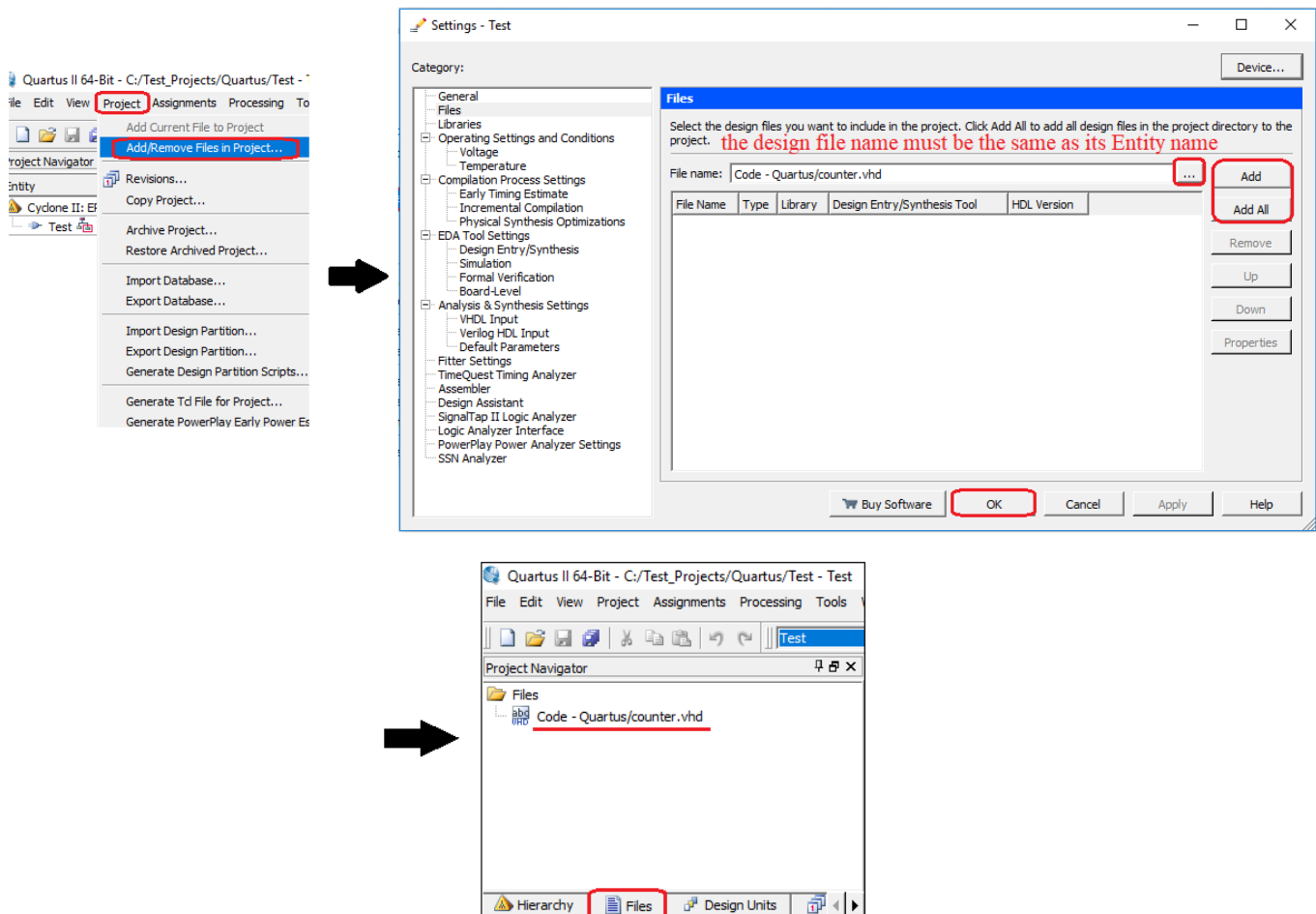
< Back Next > Finish Cancel Help

2. Step 2 – Add project files:

- a. In order to open VHDL blank file use the next step (if you're using VHDL existing files, copy these files into project folder and skip to clause b):

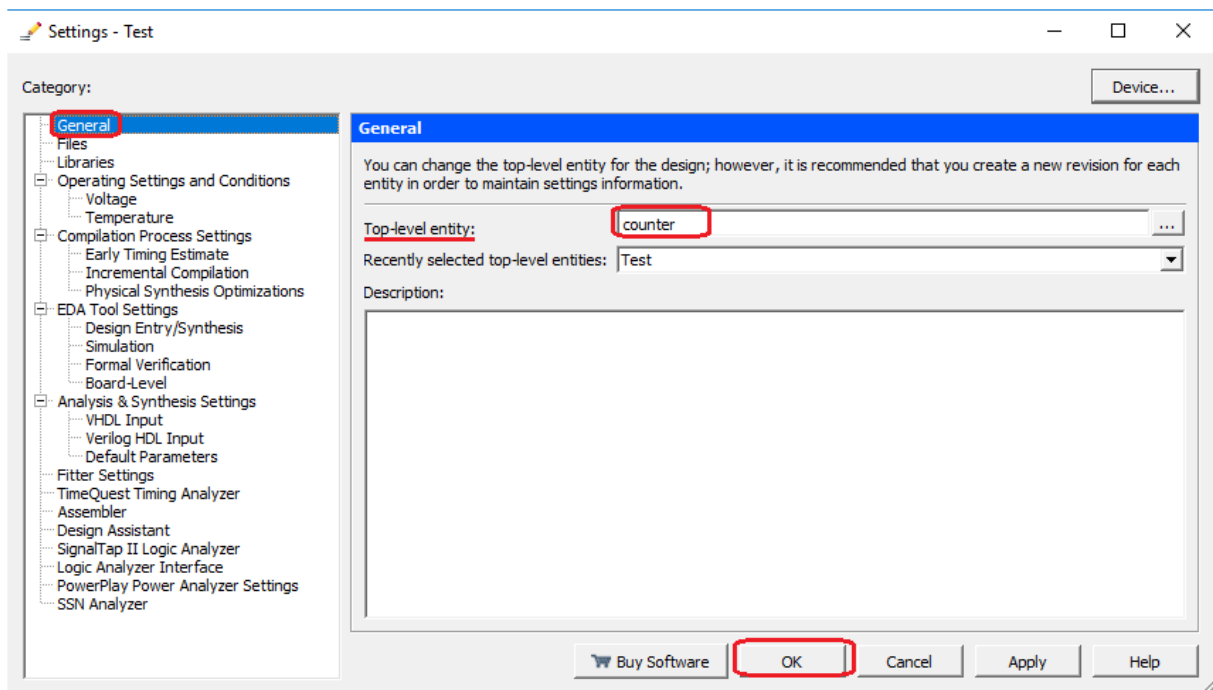
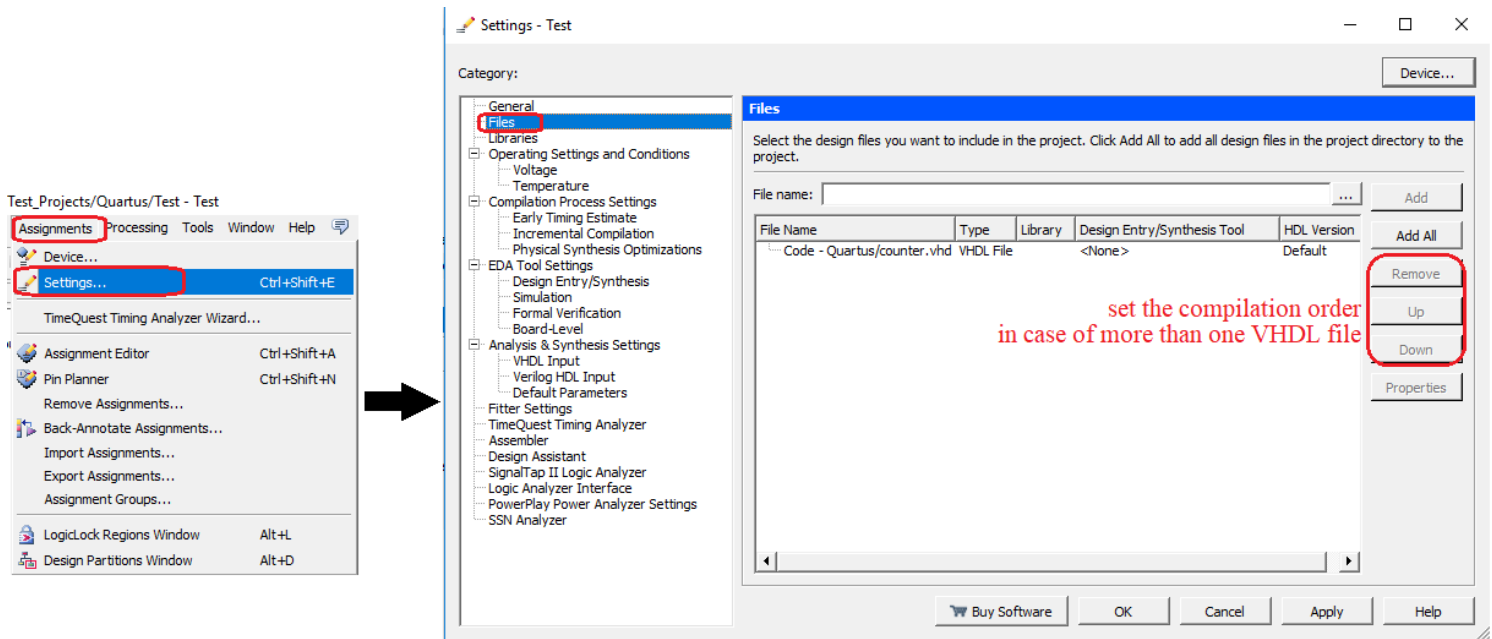


- b. Add the project VHDL existing files:



3. Step 3 – Code compilation:

a. Set the compilation order and top level entity:



counter.vhd

```
library ieee;
use ieee.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity counter is port (
    clk,enable : in std_logic;
    q          : out std_logic_vector (7 downto 0));
end counter;

architecture rtl of counter is
    signal q_int : std_logic_vector (31 downto 0) :=x"00000000";
begin
    process (clk)
    begin
        if (rising_edge(clk)) then
            if enable = '1' then
                q_int <= q_int + 1;
            end if;
        end if;
    end process;
    q <= q_int(31 downto 24); -- Output only 8MSB
end rtl;
```

Example application:

- 32bit behavioral counter with enable
- 8-bit MSB of counter output are connected to red LEDs (LEDR7-LEDR0)
- Enable connected to switch SW0
- 50MHz on board clock named CLOCK_50

b. Code compilation:

Quartus II 64-bit - C:/Test_Projects/Quartus/Test - Test

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Files

- Code - Quartus/counter.vhd

Tasks

Flow: Compilation Customize...

Task	Status
Compile Design	00
Analysis & Synthesis	00
Fitter (Place & Route)	00
Assembler (Generate programming files)	00
TimeQuest Timing Analysis	00
EDA Netlist Writer	00
Program Device (Open Programmer)	

Compilation Report - Test

Flow Summary

Flow Status: Successful - Tue Mar 26 15:04:19 2019

Quartus II 64-bit Version: 12.1 Build 177 11/07/2012 SJ Web Edition

Revision Name: Test

Top-level Entity Name: counter

Family: Cyclone II

Device: EP2C20F484C7

Timing Models: Final

Total logic elements: 32 / 18,752 (< 1 %)

Total combinational functions: 32 / 18,752 (< 1 %)

Dedicated logic registers: 32 / 18,752 (< 1 %)

Total registers: 32

Total pins: 10 / 315 (3 %)

Total virtual pins: 0

Total memory bits: 0 / 239,616 (0 %)

Embedded Multiplier 9-bit elements: 0 / 52 (0 %)

Total PLLs: 0 / 4 (0 %)

Quartus II

Full Compilation was successful (11 warnings)

OK

c. Start analysis and synthesis:

File Edit View Project Assignments Processing Tools Window Help

Compilation Report - Test

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis

Flow Summary

Flow Status: Successful - Tue Mar 26 15:13:14 2019

Quartus II 64-bit Version: 12.1 Build 177 11/07/2012 SJ Web Edition

Revision Name: Test

Top-level Entity Name: counter

Family: Cyclone II

Device: EP2C20F484C7

Timing Models: Final

Total logic elements: 32

Total combinational functions: 32

Dedicated logic registers: 32

Total registers: 32

Total pins: 10

Total virtual pins: 0

Total memory bits: 0

Embedded Multiplier 9-bit elements: 0

Total PLLs: 0

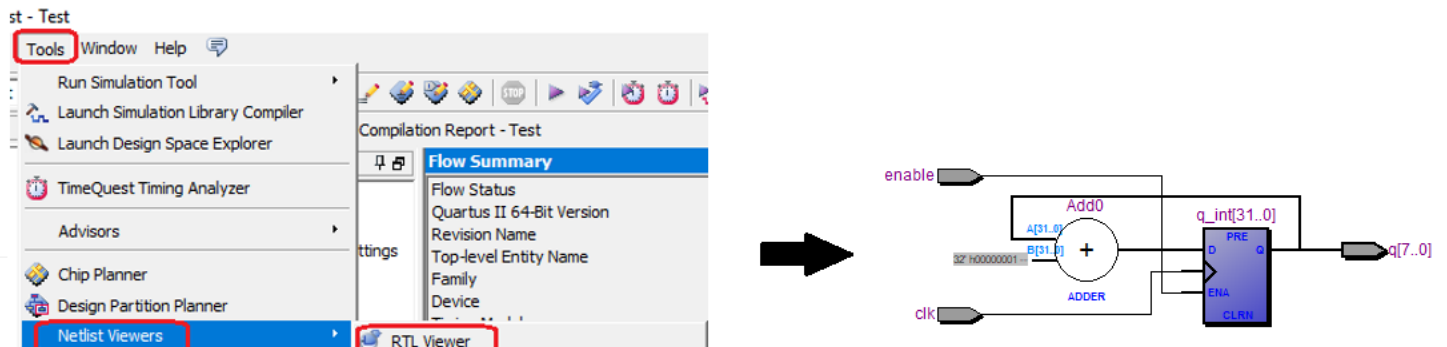
Quartus II

Analysis & Synthesis was successful (1 warning)

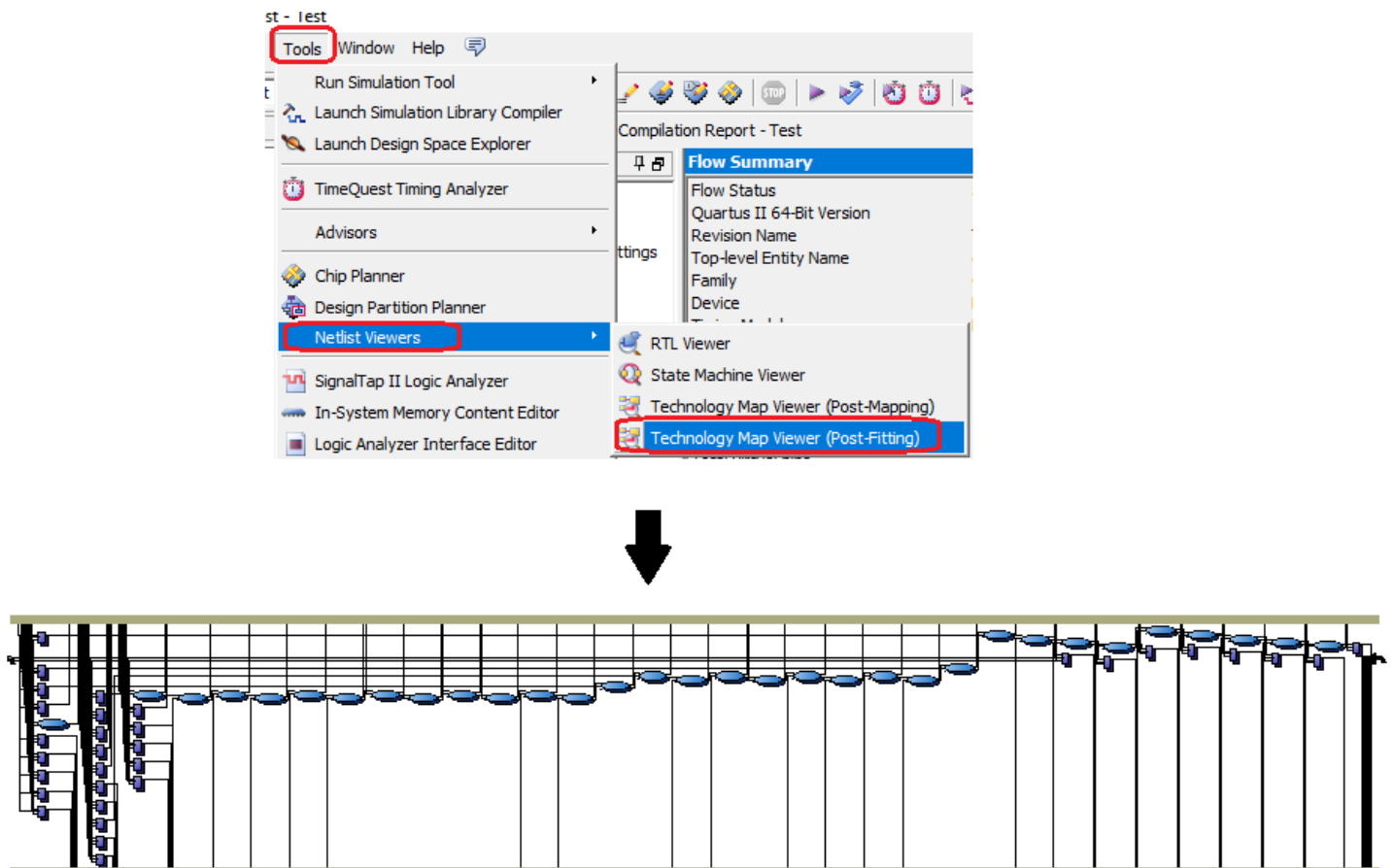
OK

4. Step 4 – Synthesis results:

a. Synthesis RTL viewer:

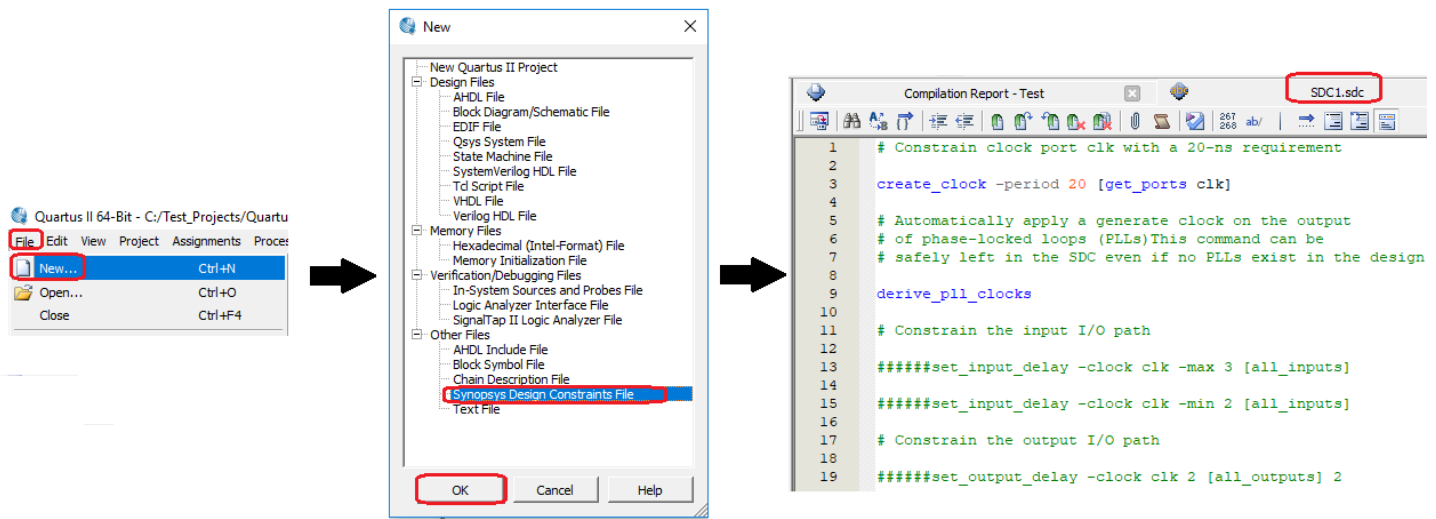


b. Synthesis Map (Post-Fitting) viewer (LEs and FFs combination):

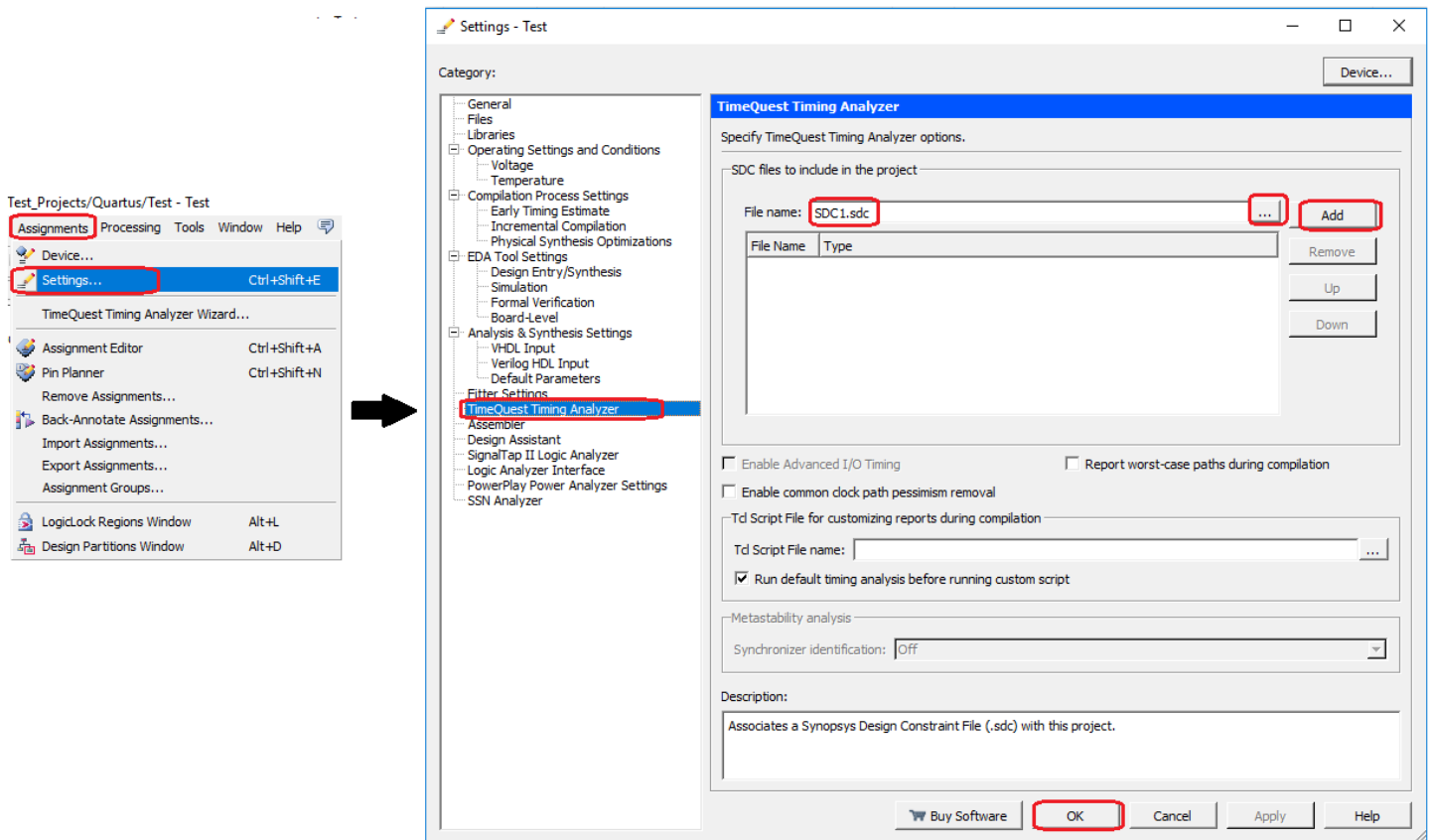


5. Step 5 – Setting system constraints:

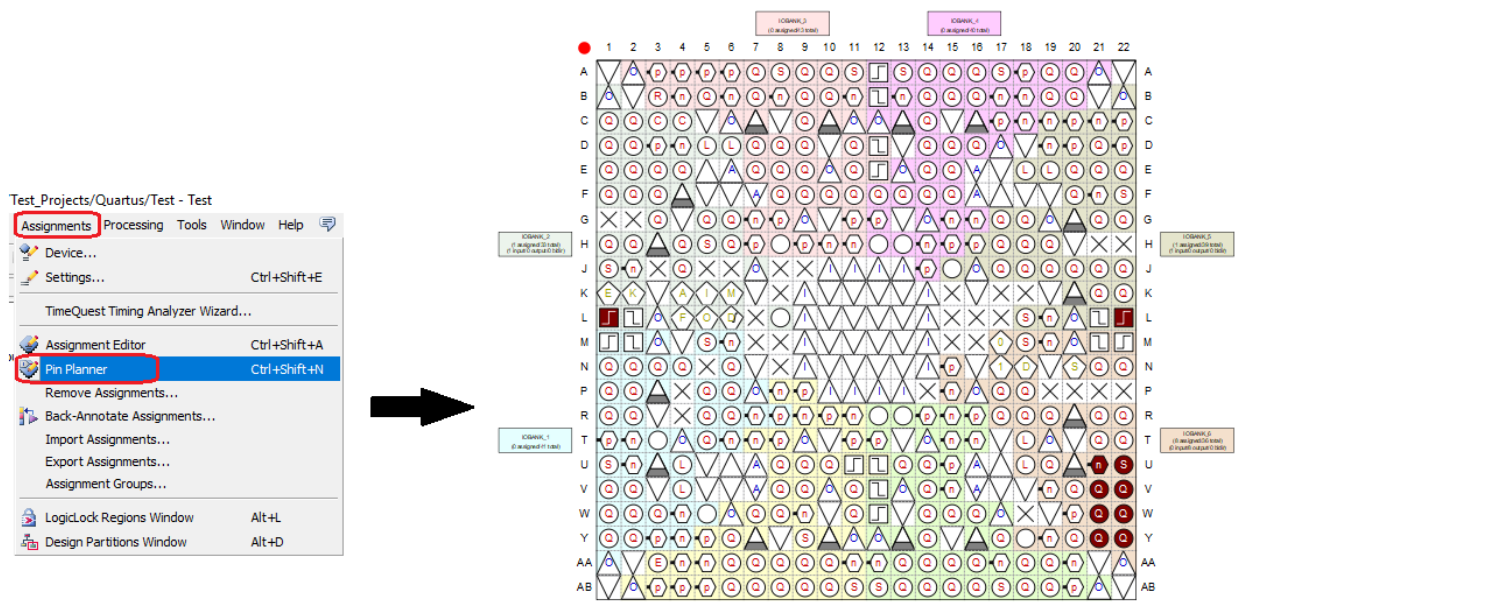
a. Create the system constraints *.sdc file:



b. Add the *.sdc file to the project:



6. Step 6 – Pin Planner Layout (See DE1-Standard user manual on pages 24-26):



Test_Projects/Quartus/Test - Test

Assignments Processing Tools Window Help

Device... Ctrl+Shift+E

Settings... Ctrl+Shift+E

TimeQuest Timing Analyzer Wizard...

Assignment Editor Ctrl+Shift+A

Pin Planner Ctrl+Shift+N

Remove Assignments...

Back-Annotate Assignments...

Import Assignments...

Export Assignments...

Assignment Groups...

LogicLock Regions Window Alt+L

Design Partitions Window Alt+D

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate
clk	Input	PIN_AF14	3B	B3B_N0	PIN_Y27	2.5 V (default)		12mA (default)	
enable	Input	PIN_AB30	5B	B5B_N0	PIN_AE26	2.5 V (default)		12mA (default)	
q[7]	Output	PIN_AF24	4A	B4A_N0	PIN_AB26	2.5 V (default)		12mA (default)	1 (default)
q[6]	Output	PIN_AE24	4A	B4A_N0	PIN_AJ29	2.5 V (default)		12mA (default)	1 (default)
q[5]	Output	PIN_AF25	4A	B4A_N0	PIN_AD27	2.5 V (default)		12mA (default)	1 (default)
q[4]	Output	PIN_AG25	4A	B4A_N0	PIN_Y21	2.5 V (default)		12mA (default)	1 (default)
q[3]	Output	PIN_AD24	4A	B4A_N0	PIN_W21	2.5 V (default)		12mA (default)	1 (default)
q[2]	Output	PIN_AC23	4A	B4A_N0	PIN_W22	2.5 V (default)		12mA (default)	1 (default)
q[1]	Output	PIN_AB23	5A	B5A_N0	PIN_W20	2.5 V (default)		12mA (default)	1 (default)
q[0]	Output	PIN_AA24	5A	B5A_N0	PIN_AH29	2.5 V (default)		12mA (default)	1 (default)

Pin Planner - C:/Test_Projects/Quartus/Test - Test

File Edit View Processing Tools Window Help

Groups

Named: *

Start I/O Assignment Analysis

Enable Live I/O Check

Quartus II

I/O Assignment Analysis was successful (3 warnings)

OK

Table 3-5 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
CLOCK_50	PIN_AF14	50 MHz clock input	3.3V

Table 3-6 Pin Assignment of Slide Switches

Signal Name	FPGA Pin No.	Description	I/O Standard
SW[0]	PIN_AB30	Slide Switch[0]	Depend on JP3

Table 3-8 Pin Assignment of LEDs

Signal Name	FPGA Pin No.	Description	I/O Standard
LEDR[0]	PIN_AA24	LED [0]	3.3V
LEDR[1]	PIN_AB23	LED [1]	3.3V
LEDR[2]	PIN_AC23	LED [2]	3.3V
LEDR[3]	PIN_AD24	LED [3]	3.3V
LEDR[4]	PIN_AG25	LED [4]	3.3V
LEDR[5]	PIN_AF25	LED [5]	3.3V
LEDR[6]	PIN_AE24	LED [6]	3.3V
LEDR[7]	PIN_AF24	LED [7]	3.3V

7. Step 7 – Full compilation (finding of f_{max}):

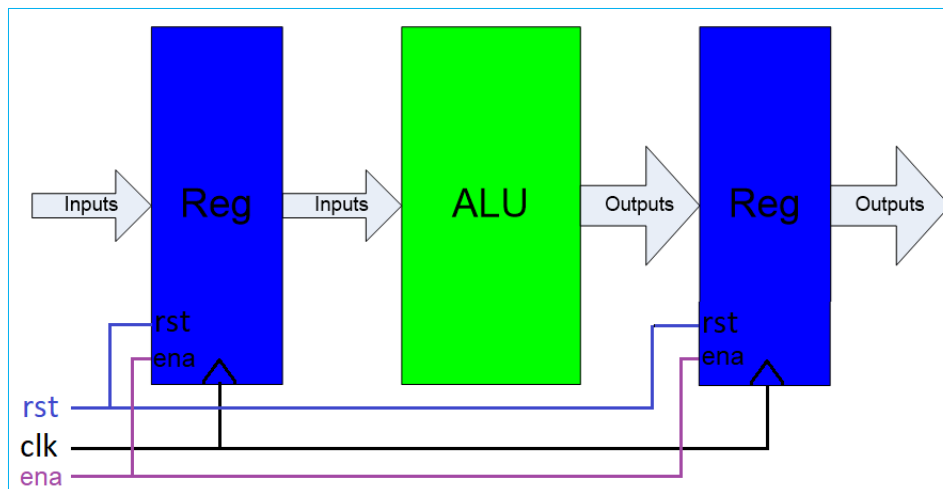
Compilation Report - Test SDC1.sdc

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- TimeQuest Timing Analyzer**
- Summary
- Parallel Compilation
- SDC File List
- Clocks
- Slow Model**
- Fmax Summary**
- Setup Summary
- Hold Summary
- Recovery Summary
- Removal Summary
- Minimum Pulse Width Summ
- Worst-Case Timing Paths
- Datasheet Report
- Fast Model
- Multicorner Timing Analysis Sun
- Multicorner Datasheet Report !
- Clock Transfers
- Report TCCS
- Report RSKM
- Unconstrained Paths
- Messages
- EDA Netlist Writer

Slow Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	221.29 MHz	221.29 MHz	clk	



Explanation: In order Quartus IDE can calculate f_{max} the logic design parts must be wrapped by registers

8. Step 8 – Finding Critical Path Location:

The screenshot illustrates the steps to generate a timing report in the TimeQuest Timing Analyzer. On the left, a secondary window shows the 'Tools' menu with 'TimeQuest Timing Analyzer' highlighted. A large black arrow points to the main application window. In the main window, the 'Tasks' pane on the left lists various reports, with 'Report Timing...' selected and a red box around it. A red text label 'Mouse right click' points to this item. A context menu is open over 'Report Timing...', showing 'Start' and 'Start Again' options, with 'Start' highlighted by a red box. The 'Report' pane at the top shows 'Report not available'. The right side of the window displays a 'Getting Started' welcome screen. The bottom console window shows the following text:

```
assumed to be external and are run using Tcl's "exec"
command.
- Type "exit" to exit.
- Type "help" to view a list of Quartus II Tcl packages.
- Type "help <package name>" to view a list of Tcl commands
available for the specified Quartus II Tcl package.
- Type "help -tcl" to get an overview on Quartus II Tcl usages.
*****
tcl> project_open -force "C:/Test_Projects/Quartus/Test.qpf" -revision T
tcl>
```

Report Timing

Clocks
 From clock:
 To clock:

Targets
 From:
 Through:
 To:

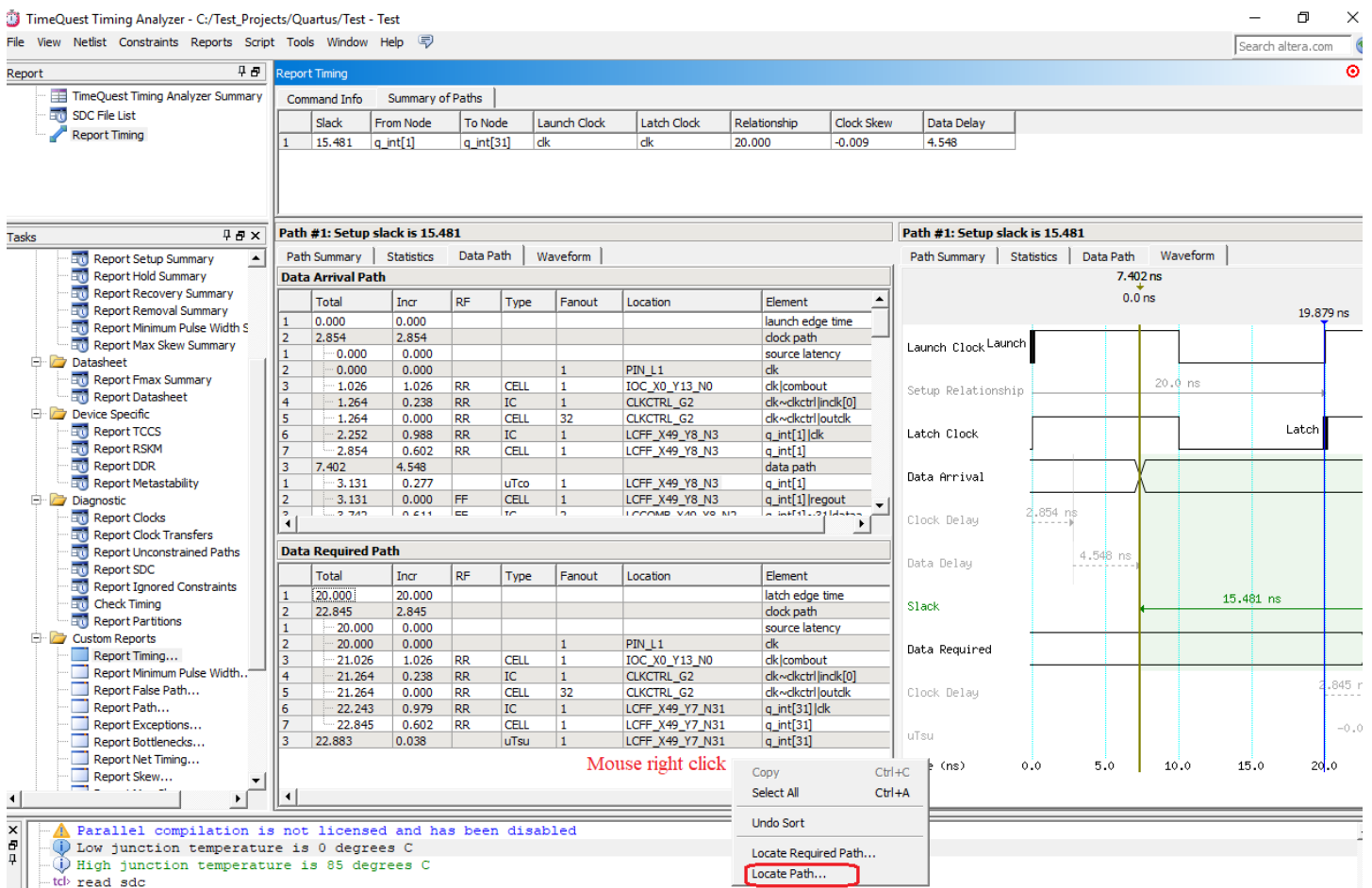
Analysis type
☒ Setup
☐ Hold
☐ Recovery
☐ Removal

Paths
 Report number of paths: 1
 Maximum number of paths per endpoint:
 Maximum slack limit: ns
☐ Pairs only

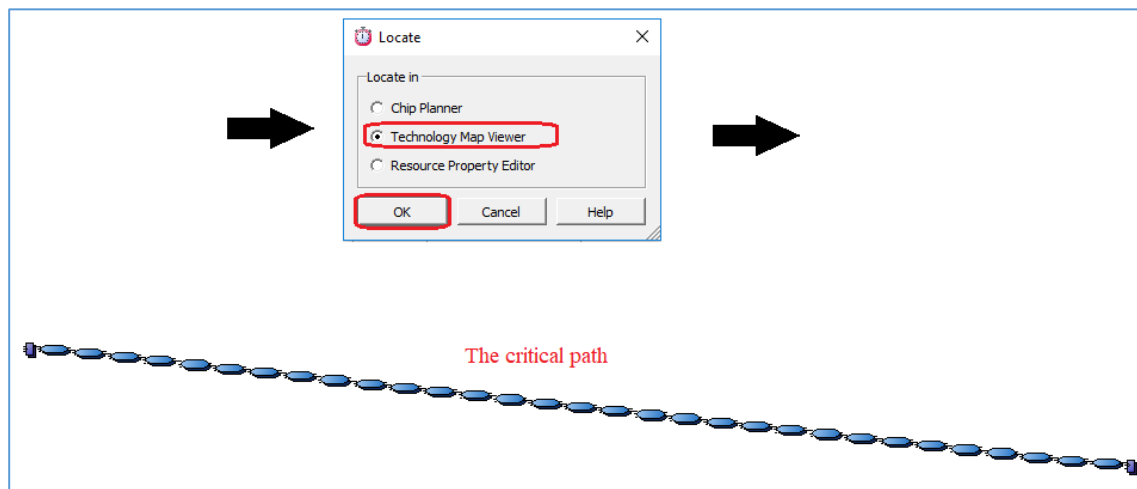
Output
 Detail level: Full path Set Default
☐ Show routing
☒ Report panel name: Report Timing
☐ File name:
 File options
☒ Overwrite ☐ Append Open
☐ Console

Td command: report_timing -setup -npaths 1 -detail full_path -panel_name {Report Timing}

Report Timing Close Help



i. Technology Map Viewer:



ii. Resource Property Editor:

The diagram illustrates the process of editing resource properties in the Resource Property Editor. It shows a 'Locate' dialog box with 'Resource Property Editor' selected. Below the dialog, the Resource Property Editor window is shown, displaying the properties of a selected LUT (LUT6).

Resource Property Editor - C:/Test_Projects/Quartus/Test - Test

Node Name: **counter[qa_int[10]~49]** Location: **LCCOMB_X49_Y8_N20**

Properties/Modes Values

Sum LUT Mask	SA5F
Carry LUT Mask	SF5F
Operation Mode	arithmetic
Latch Type	none
Sum Equation	A & IC # 1A & (C # 1D)
Carry Equation	1C # 1A

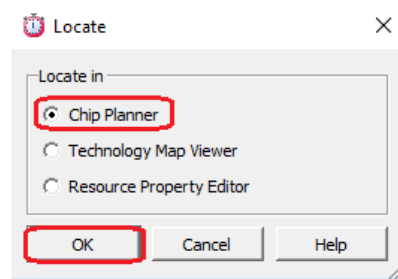
Input Port Name Signal Name Inverted

Register		
EN	counter[enab]	False
SCLR	<Disconnected>	False
IACLR	<Disconnected>	False
SDATA	<Disconnected>	False
DATAIN	counter[qa_int[10]~49]	False
SLOAD	<Disconnected>	False
CLK	counter[clk~clkctrl]	False
Combinational		
DATAA	<Disconnected>	False
DATAB	<Disconnected>	False
DATAD	VCC	False
CTN	counter[qa_int[9]~48]	False

Output Port Name Signal Name

Register	
REGOUT	counter[qa_int[10]
Combinational	
COUT	counter[qa_int[10]~50]
COMBOUT	counter[qa_int[10]~49]

iii. Chip Planner:



Coordinate: Editing Mode: ECO - EP2C20F484C7

Layers Settings

Basic

- ☒ Background
 - ☐ None
 - ☒ Block Utilization
 - ☐ Design Partition P...
- ☒ LogicLock Regions
 - ☒ User-assigned Lo...
 - ☒ Fitter-placed Logi...
- ☐ Clock Regions
 - ☐ Global Clock Region
 - ☐ Local Clock Region
 - ☐ LVDS Clock Region
 - ☐ Regional Clock R...
 - ☐ Periphery Clock ...
- ☒ Overlay Objects
 - ☒ Connection Lines
 - ☐ Labels
 - ☒ Differential Pin P...
 - ☒ Report Overlay

Layers Settings Color Legend

Properties

Selected elements:

General

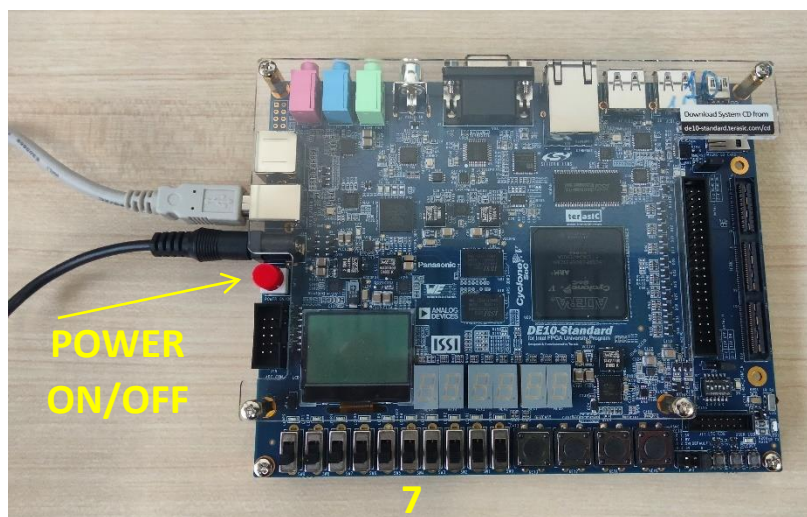
Timing

Located Objects

Located 1 paths

Time	Object
15.481	q_int[1] -> q_int[31]
1.026ns	clk -> q_int[1]
0.238ns	clk -> clk~clkctrl
0.000ns	clk~clkctrl -> clk~clkctrl
0.988ns	clk~clkctrl -> q_int[1]
0.602ns	q_int[1] -> q_int[1]
Arrival Data	q_int[1] -> q_int[31]
(Required Clock)	clk -> q_int[31]

9. Step 9 – Code Programming:



After compiling and verifying your design you are ready to program the FPGA on the development board. You download the SOF you just created into the FPGA using the USB – BlasterII circuitry on the board. Set up your hardware for programming using the following steps:

The image shows the Intel Quartus Programmer interface. The **Tools** menu is open, with **Programmer** selected. The **Programmer** window is open, showing the hardware setup as **DE-SoC [USB-1]** and the mode as **JTAG**. The **Auto Detect** button is highlighted. A red text annotation says: *Click Auto Detect to detect all the device s on the JTAG chain*. Below the **Auto Detect** button, a diagram shows a JTAG chain with a device labeled **5CSXFC6D6F31**. The **Select Device** dialog is open, showing a list of devices found with a shared JTAG ID. The device **5CSXFC6D6** is selected. A red text annotation says: *Select 5CSXFC6D6 and click OK*. The **OK** button is highlighted.

Tools Window Help

- Run Simulation Tool
- Launch Simulation Library Compiler
- Launch Design Space Explorer II
- Timing Analyzer
- Advisors
- Chip Planner
- Design Partition Planner
- Netlist Viewers
- Signal Tap Logic Analyzer
- In-System Memory Content Editor
- Logic Analyzer Interface Editor
- In-System Sources and Probes Editor
- Signal Probe Pins...
- Programmer**
- JTAG Chain Debugger
- Fault Injection Debugger
- System Debugging Tools

Programmer - C:/TestPrograms/Quartus21_1/Test - Test - [Test.cdf]

File Edit View Processing Tools Window Help

Hardware Setup... DE-SoC [USB-1] Mode: JTAG Progress:

☐ Enable real-time ISP to allow background programming when available

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	Reactions	ISP CLAMP	SFI	PF
output_files/Test.sof	5CSXFC6D6F31	00AF9471	00AF9471	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Auto Detect Click Auto Detect to detect all the device s on the JTAG chain

TDI →

← TDO

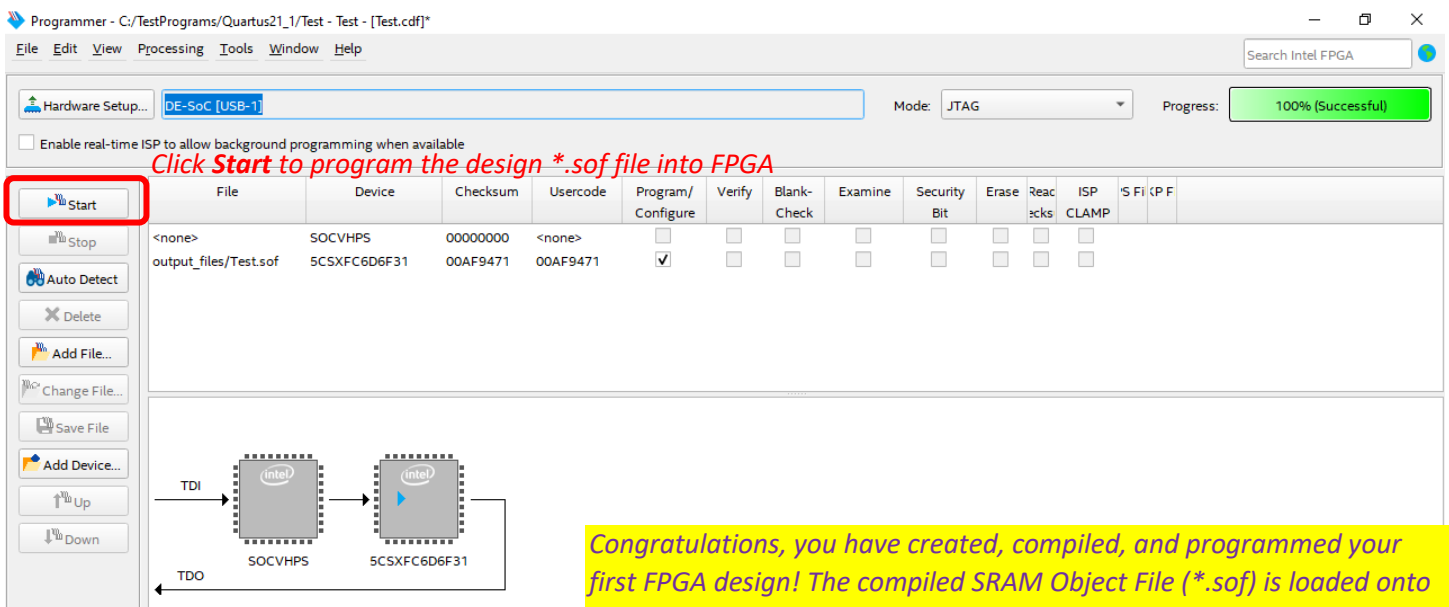
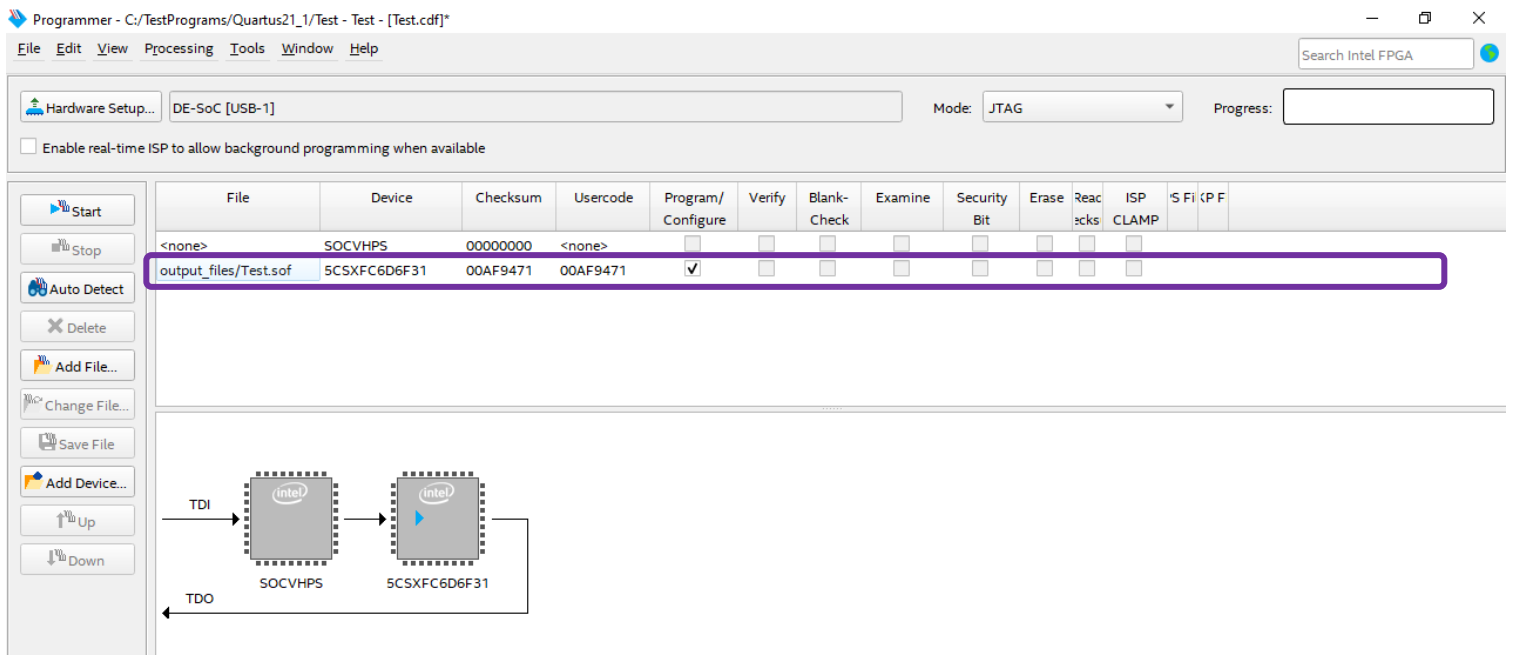
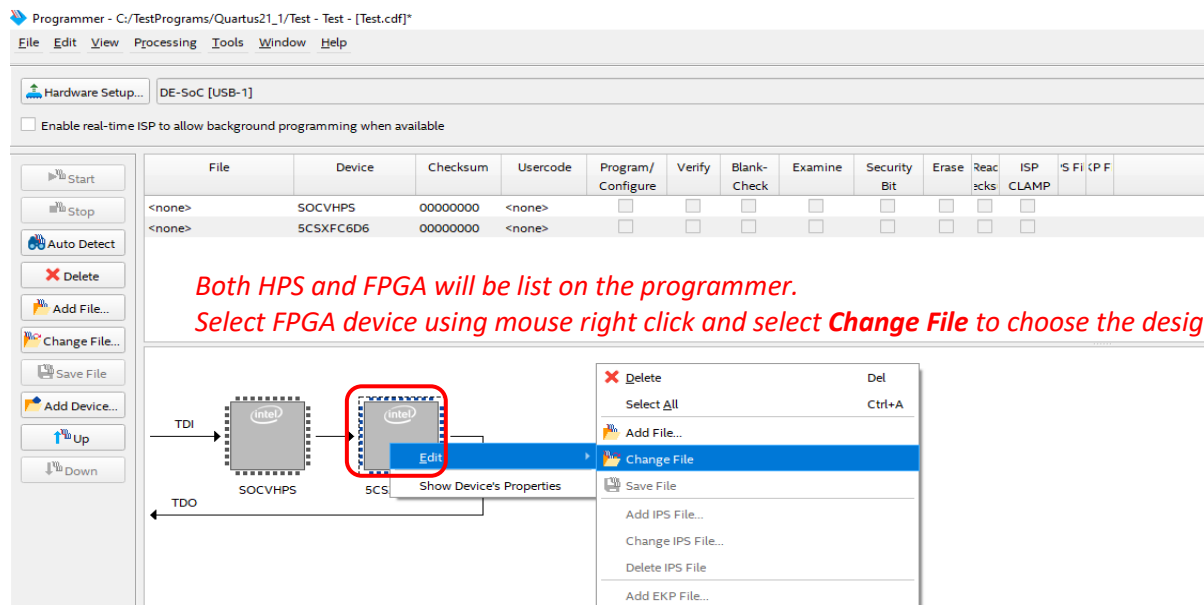
5CSXFC6D6F31

Select Device

Found devices with shared JTAG ID for device 2. Please select your device.

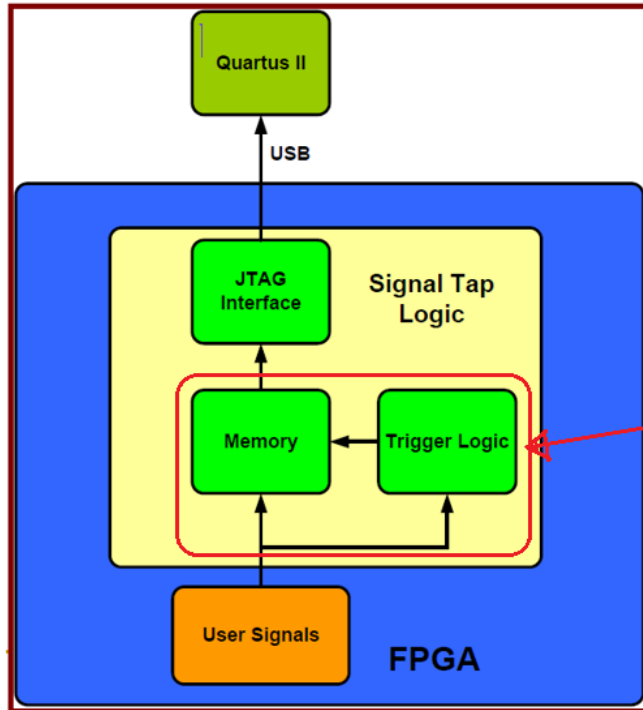
- ☐ 5CSEBA6
- ☐ 5CSEBA6ES
- ☐ 5CSEMA6
- ☐ 5CSTFD6D5
- ☐ 5CSXFC6C6
- ☐ 5CSXFC6C6ES
- ☒ **5CSXFC6D6** Select 5CSXFC6D6 and click OK
- ☐ 5CSXFC6D6ES

OK



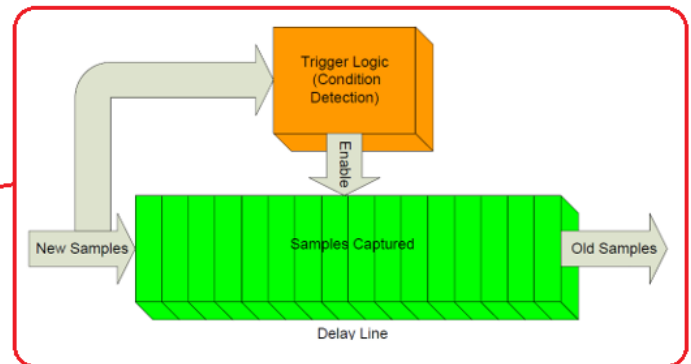
B. Verification – Using Signal TAP:

1. Block Diagram:



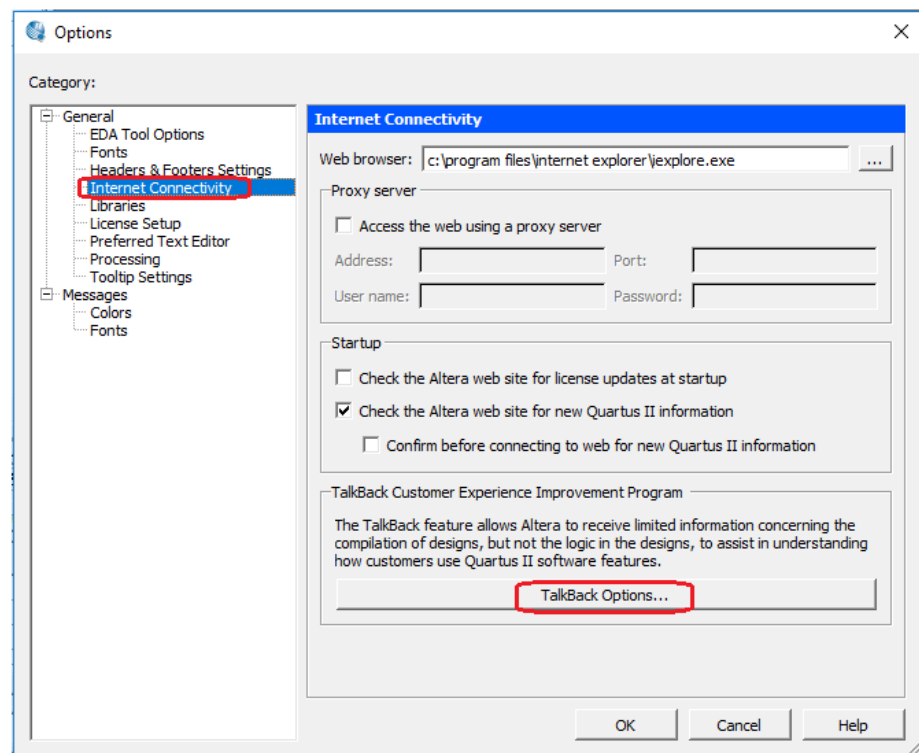
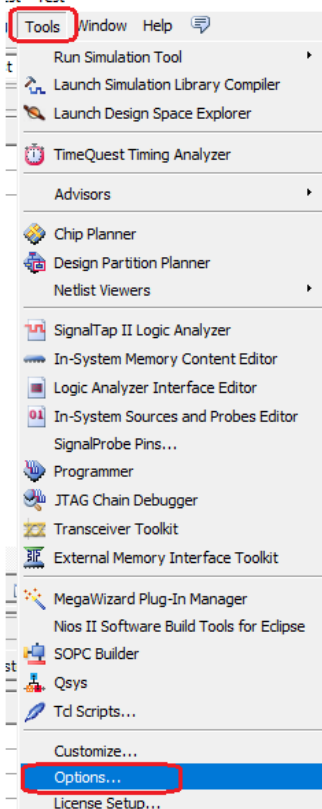
Signal TAP Pros & Cons:

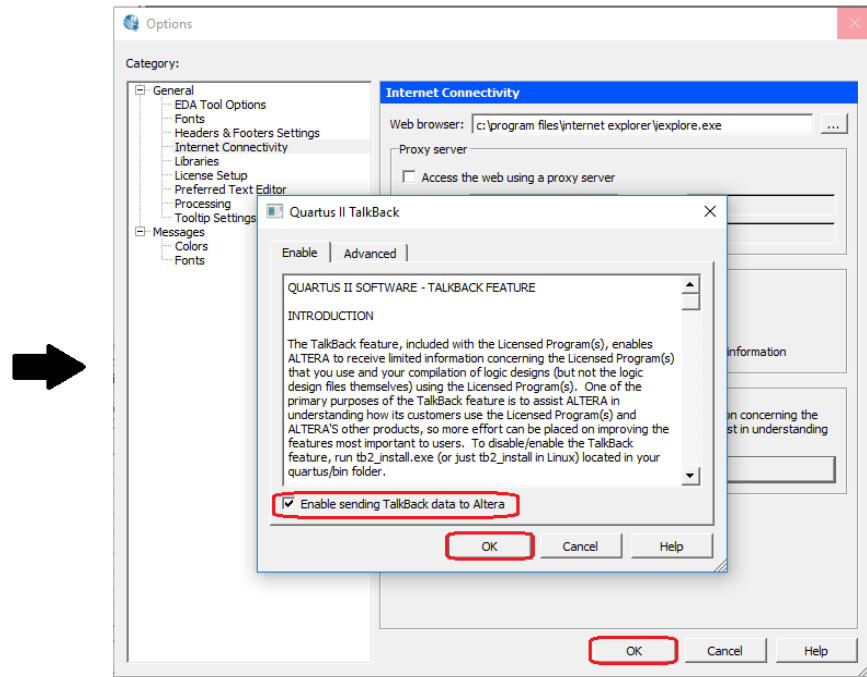
- Captures real time state of FPGA internal signals and pins (up to 200MHz)
- Connects to Quartus II through JTAG
- Do not require huge and expensive equipment
- Uses internal FPGA resources
 - Memory Blocks
 - Logic Elements
- Each time the captured signals list change the design must be recompiled



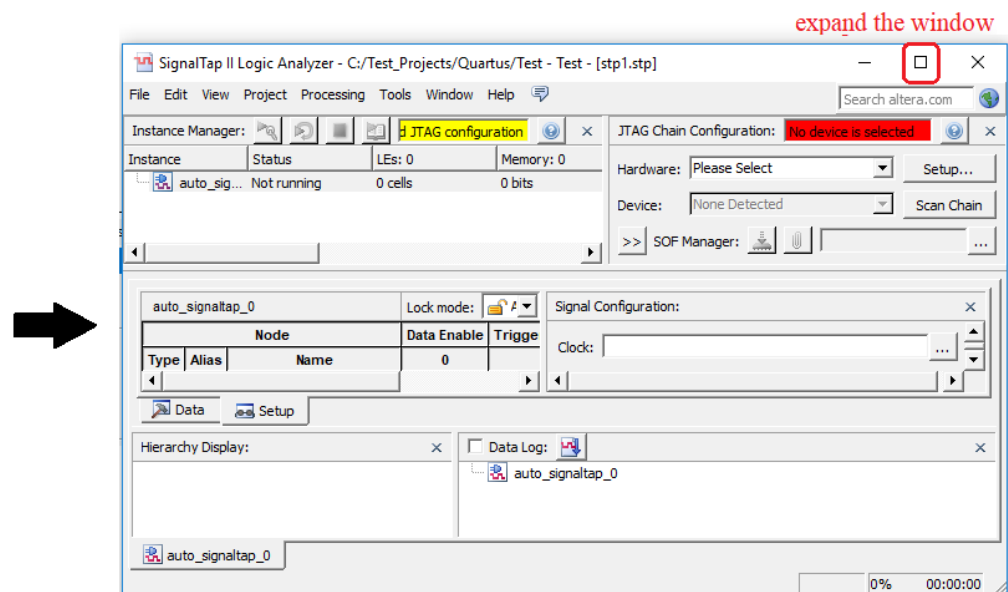
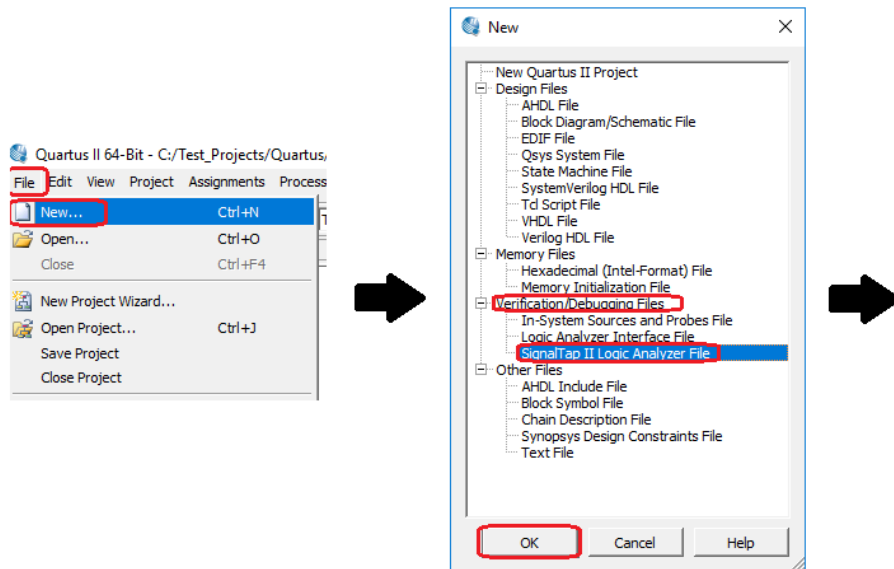
Signal TAP Features:

- Up to 1024 Data Channels
- Multiple Analyzers in One Device
 - Supports Analysis of Multiple Clock Domains
 - Each Analyzer Can Run Simultaneously
- Multiple Analyzers in One Device
- Up to 10 Trigger Levels Per Channel





3. Create a new STP file:



4. Configurations (after expansion of the previous window):

The image displays a sequence of screenshots from the Quartus II software interface, illustrating the configuration process for a signal tap.

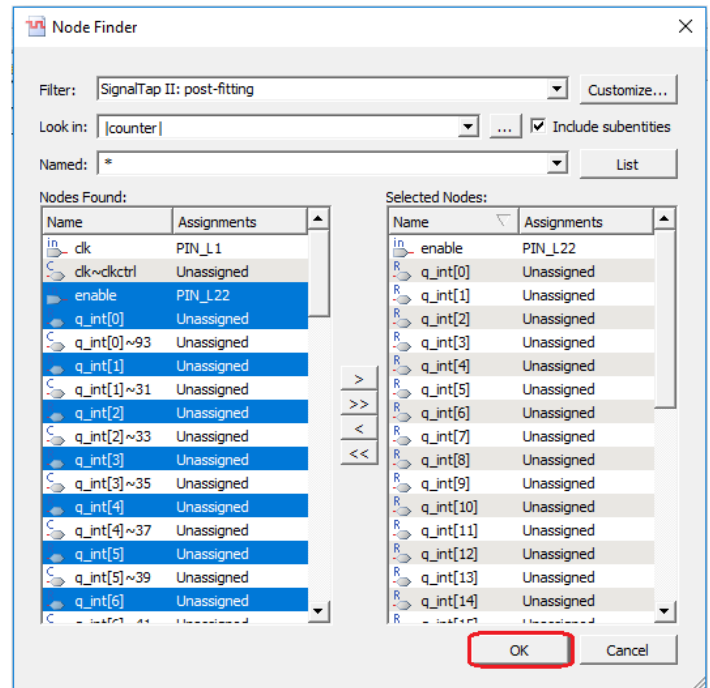
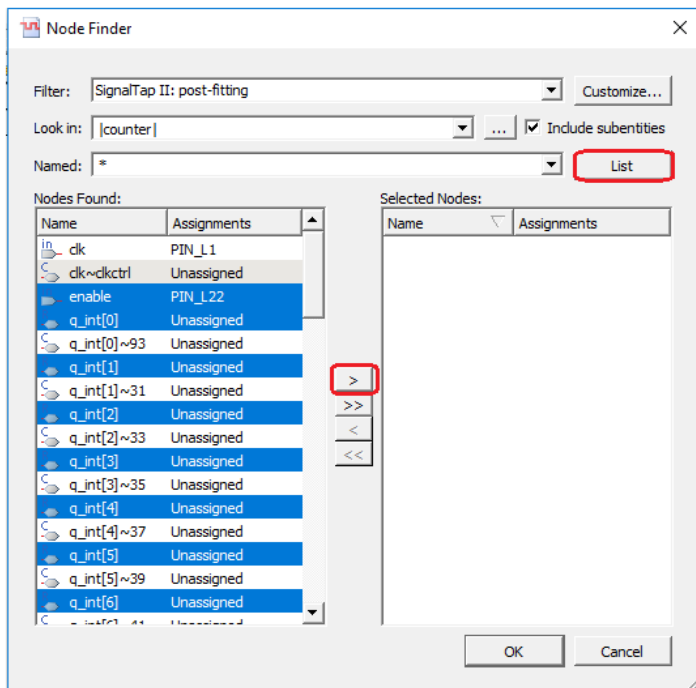
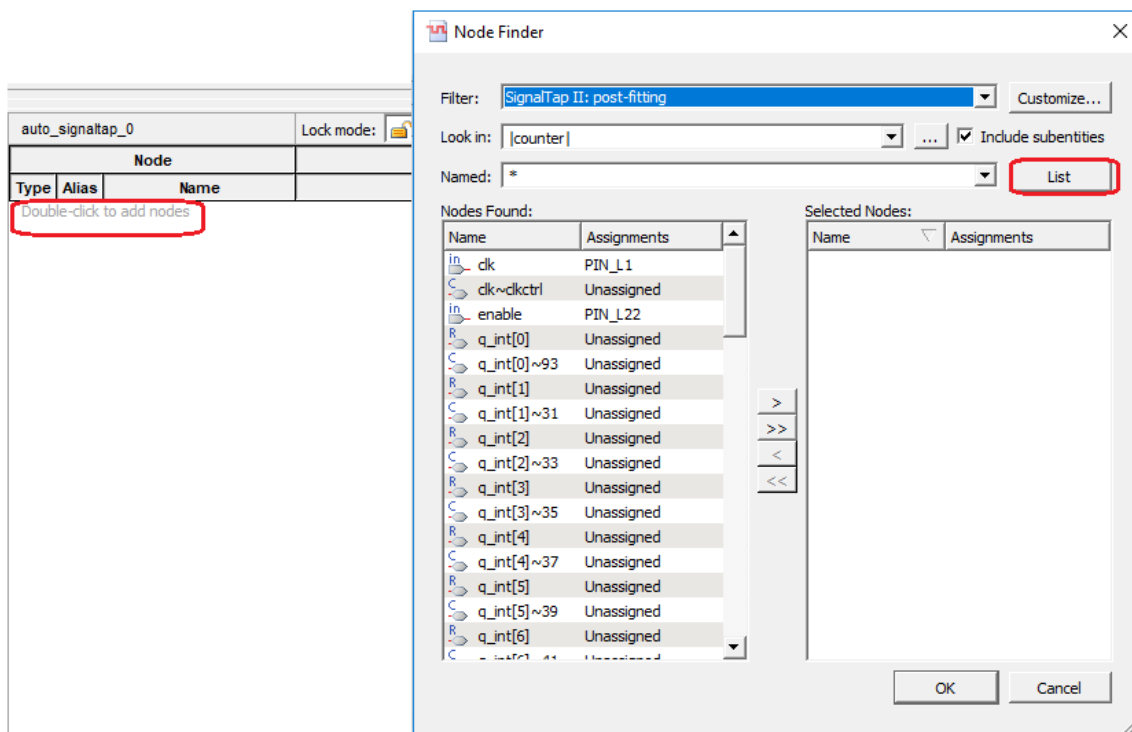
Top Row:

- Node Finder:** The 'Filter' is set to 'SignalTap II: post-fitting'. The 'Look in' dropdown shows 'counter'. The 'List' button is highlighted. The 'Nodes Found' table lists various signals, with 'clk' (PIN_L1) selected. The 'Selected Nodes' table shows 'clk' (PIN_L1) is now selected.
- JTAG Chain Configuration:** The 'Hardware' dropdown is set to 'Please Select'. The 'Device' dropdown is set to 'None Detected'. The 'SOF Manager' button is highlighted.
- Signal Configuration:** The 'Clock' is set to 'clk'. The 'Sample depth' is set to '4 K'. The 'RAM type' is set to 'Auto'. The 'Type' is set to 'Continuous'. The 'Trigger flow control' is set to 'Sequential'. The 'Trigger position' is set to 'Pre trigger position'. The 'Trigger conditions' are set to '1'.

Bottom Row:

- Select Programming File:** The 'Look in' dropdown shows 'C:\Test_Projects\Quartus'. The 'Files of type' is set to 'SRAM Object Files (*.sof)'. The 'output_files' folder is selected.
- Select Programming File:** The 'Look in' dropdown shows 'C:\Test_Projects\Quartus\output_files'. The 'Test.sof' file is selected. The 'Open' button is highlighted.
- JTAG Chain Configuration:** The 'Hardware' dropdown is set to 'USB-Blaster [USB-0]'. The 'Device' dropdown is set to 'None Detected'. The 'SOF Manager' button is highlighted.
- Signal Configuration:** The 'Clock' is set to 'clk'. The 'Sample depth' is set to '4 K'. The 'RAM type' is set to 'Auto'. The 'Type' is set to 'Continuous'. The 'Trigger flow control' is set to 'Sequential'. The 'Trigger position' is set to 'Pre trigger position'. The 'Trigger conditions' are set to '1'.

Red boxes and arrows indicate the flow of the configuration process, highlighting key settings and file selections.



In case of more than one Trigger condition columns:
 1) **Between lines in the same column** the operation is **AND**.
 2) **Between columns** the operation is **OR**.



auto_singaltap_0 Lock mode: Allow all changes

Type	Alias	Name	Data Enable	Trigger Enable	Trigger Conditions
In		enable	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	1 Basic
R		q_int[0]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[1]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[2]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[3]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[4]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[5]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[6]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[7]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[8]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[9]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[10]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[11]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[12]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[13]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[14]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[15]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[16]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[17]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[18]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[19]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[20]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[21]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[22]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[23]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[24]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[25]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
R		q_int[26]	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

Signal Configuration:

Clock: clk

Data

Sample depth: 4 K

☐ Segmented: 2 2

Storage qualifier:

Type: Con

Input port:

☒ Record data disc

☐ Disable storage q

Trigger

Trigger flow control: S

Trigger position:

Trigger conditions: 1

☐ Trigger in

Source: auto_stp_

Pattern: Don't C

☐ Trigger out

Target:

Level: Active

Latency delay:

Data
 Setup

mouse right click

Don't Care
 Low
 Falling Edge
 Rising Edge
 High
 Either Edge



SignalTap II Logic Analyzer - C:/Test_Projec

File Edit View Project Processing Tools W

New File Ctrl+N

Close

Save Ctrl+S

Save As...

Export...

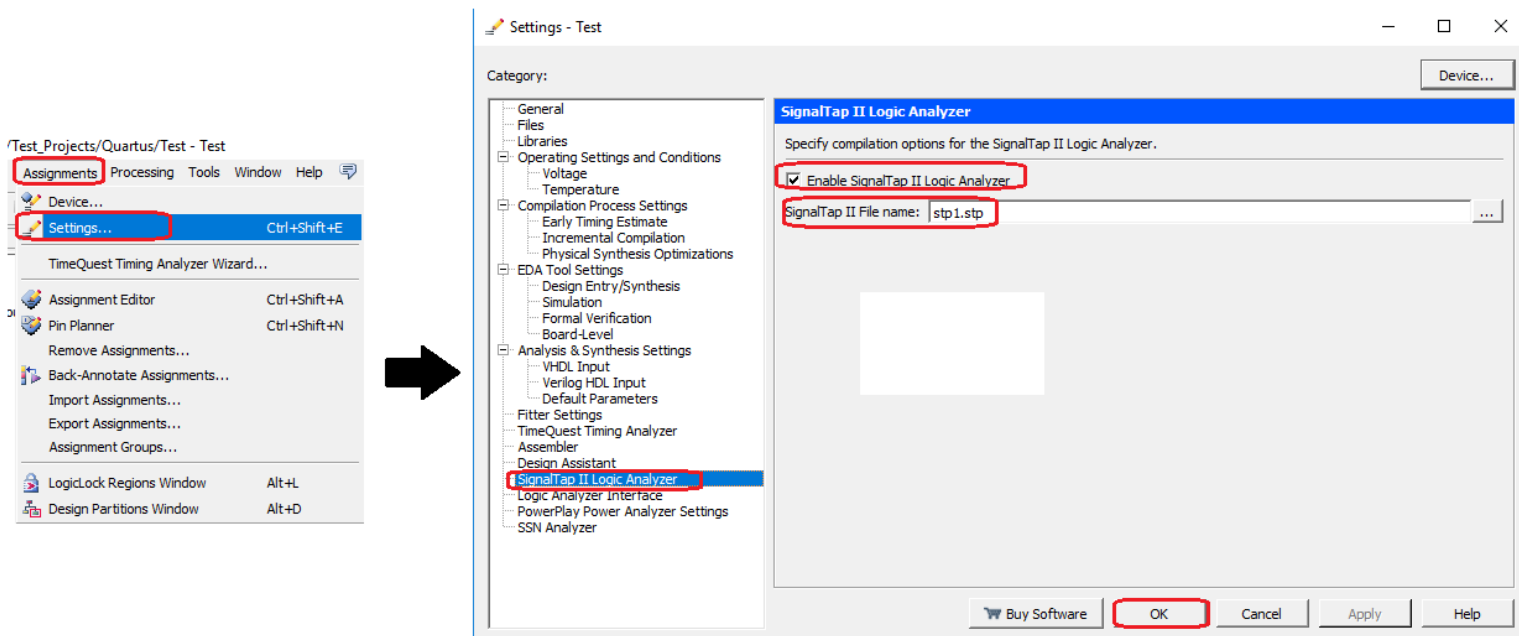
Page Setup...

Print Preview

Print... Ctrl+P

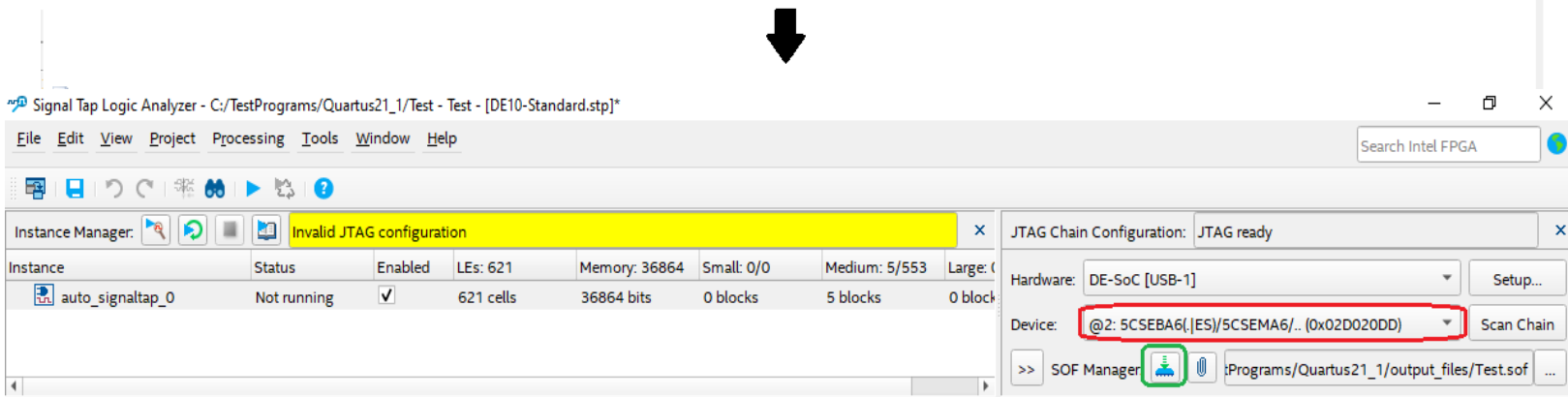
Type	Alias	Name
In		enable
R		q_int[0]

5. Project Compilation and Programming (an eventually the Signals results):

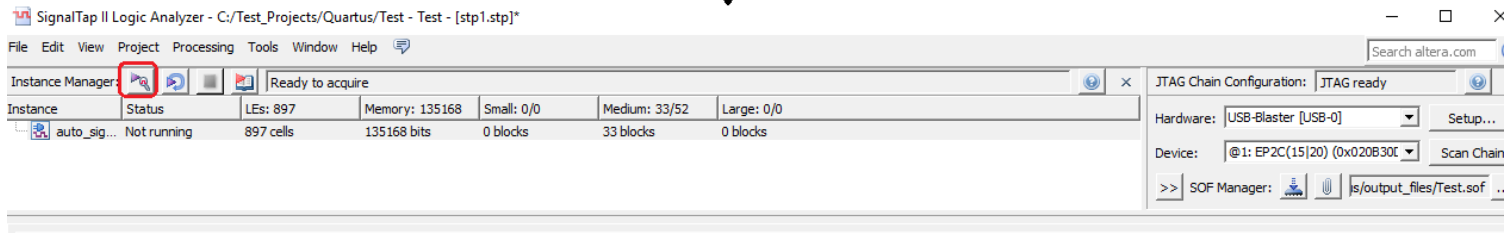


Turn ON the DE1 Board power

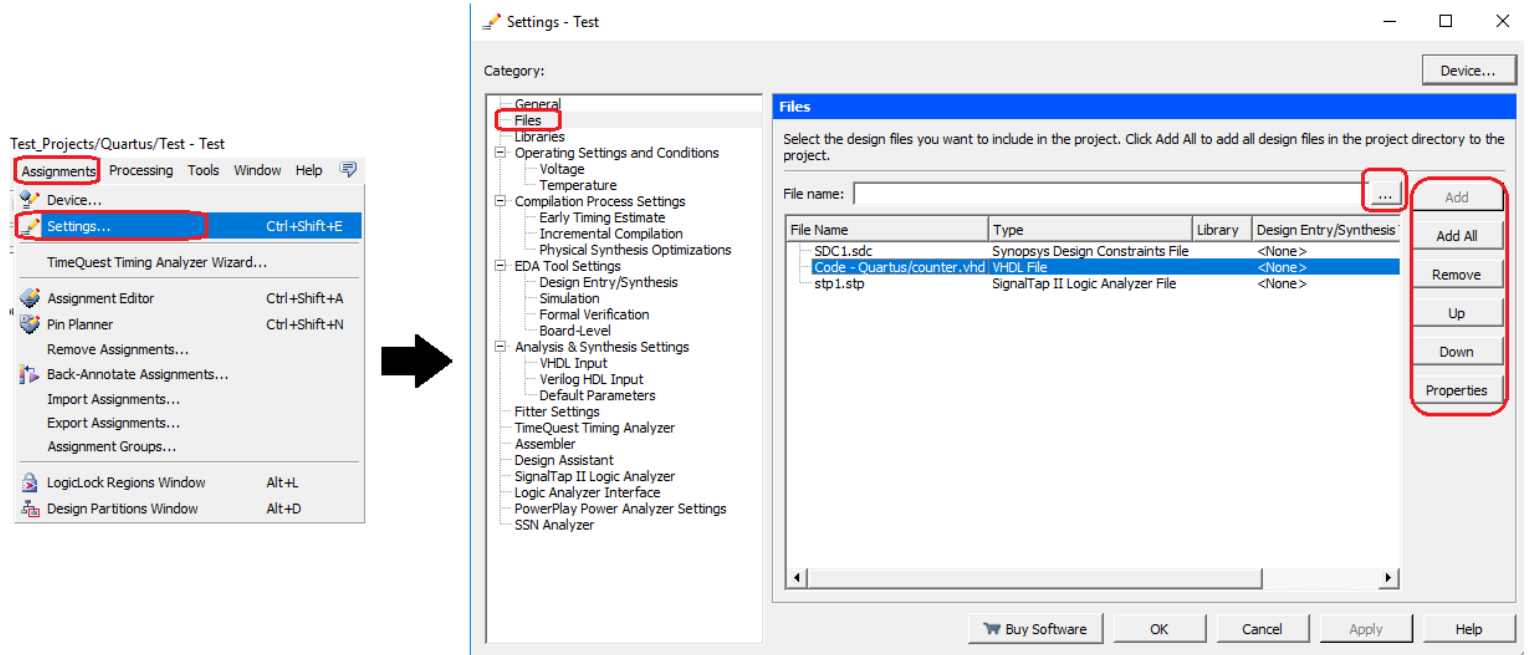
Open the STP file



Device programming



C. Changing the VHDL source files of the project:



D. Open Existing Project:

