- **Organization . . .**
  1048576 x 16 Bits x 4 Banks
  2097152 x 8 Bits x 4 Banks
  4194304 x 4 Bits x 4 Banks
- **3.3-V Power Supply (±10% Tolerance)**
- **Four Banks for On-Chip Interleaving for x8/x16 (Gapless Access) Depending on Organizations**
- **High Bandwidth – Up to 125-MHz Data Rates**
- **Burst Length Programmable to 1, 2, 4, 8**
- **Programmable Output Sequence – Serial or Interleave**
- **Chip-Select and Clock-Enable for Enhanced-System Interfacing**
- **Cycle-by-Cycle DQ Bus Mask Capability**
- **Only x16 SDRAM Configuration Supports Upper-/Lower-Byte Masking Control**
- **Programmable CAS Latency From Column Address**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYLE TIME		ACCESS TIME CLOCK TO OUTPUT		REFRESH INTERVAL
	t_{CK3}	t_{CK2}	t_{AC3}	t_{AC2}	t_{REF}
’664xx4-8	8 ns	10 ns	6 ns	6 ns	64 ms
’664xx4-8A	8 ns	15 ns	6 ns	7.5 ns	64 ms
’664xx4-10	10 ns	15 ns	7.5 ns	7.5 ns	64 ms

- **Pipeline Architecture (Single-Cycle Architecture)**
- **Single Write/Read Burst**
- **Self-Refresh Capability (Every 16 μs)**
- **Low-Noise, Low-Voltage Transistor-Transistor Logic (LVTTL) Interface**
- **Power-Down Mode**
- **Compatible With JEDEC Standards**
- **16K RAS-Only Refresh (Total for All Banks)**
- **4K Auto Refresh (Total for All Banks)/64 ms**
- **Automatic Precharge and Controlled Precharge**
- **Burst Interruptions Supported:**
  - **Read Interruption**
  - **Write Interruption**
  - **Precharge Interruption**
- **Support Clock-Suspend Operation (Hold Command)**
- **Intel PC100 Compliant (-8 and -8A parts)**

description

The TMS664xx4 series are 67108864-bit synchronous dynamic random-access memory (SDRAM) devices which are organized as follow:

- Four banks of 1 048 576 words with 16 bits per word
- Four banks of 2097152 words with 8 bits per word
- Four banks of 4194304 words with 4 bits per word

All inputs and outputs of the TMS664xx4 series are compatible with the LVTTL interface.

The SDRAM employs state-of-the-art technology for high-performance, reliability, and low power. All inputs and outputs are synchronized with the CLK input to simplify system design and to enhance use with high-speed microprocessors and caches.

The TMS664xx4 SDRAM is available in a 400-mil, 54-pin surface-mount thin small-outline package (TSOP) (DGE suffix).

TMS664xx4 (LVTTL)
DGE PACKAGE
(TOP VIEW)

4M x 16	8M x 8	16M x 4						
V_{CC}	V_{CC}	V_{CC}	1		54	V_{SS}	V_{SS}	V_{SS}
DQ0	DQ0	NC	2		53	NC	DQ7	DQ15
V_{CCQ}	V_{CCQ}	V_{CCQ}	3		52	V_{SSQ}	V_{SSQ}	V_{SSQ}
DQ1	NC	NC	4		51	NC	NC	DQ14
DQ2	DQ1	DQ0	5		50	DQ3	DQ6	DQ13
V_{SSQ}	V_{SSQ}	V_{SSQ}	6		49	V_{CCQ}	V_{CCQ}	V_{CCQ}
DQ3	NC	NC	7		48	NC	NC	DQ12
DQ4	DQ2	NC	8		47	NC	DQ5	DQ11
V_{CCQ}	V_{CCQ}	V_{CCQ}	9		46	V_{SSQ}	V_{SSQ}	V_{SSQ}
DQ5	NC	NC	10		45	NC	NC	DQ10
DQ6	DQ3	DQ1	11	54-Pin	44	DQ2	DQ4	DQ9
V_{SSQ}	V_{SSQ}	V_{SSQ}	12	Plastic	43	V_{CCQ}	V_{CCQ}	V_{CCQ}
DQ7	NC	NC	13	TSOP–II	42	NC	NC	DQ8
V_{CC}	V_{CC}	V_{CC}	14	(Pitch = 0.8 mm)	41	V_{SS}	V_{SS}	V_{SS}
DQML	NC	NC	15		40	NC	NC	NC
$\overline{W}$	$\overline{W}$	$\overline{W}$	16		39	DQM	DQM	DQMU
$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	17		38	CLK	CLK	CLK
$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	18		37	CKE	CKE	CKE
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	19		36	NC	NC	NC
A13, BS0	A13, BS0	A13, BS0	20		35	A11	A11	A11
A12, BS1	A12, BS1	A12, BS1	21		34	A9	A9	A9
A10, AP	A10, AP	A10, AP	22		33	A8	A8	A8
A0	A0	A0	23		32	A7	A7	A7
A1	A1	A1	24		31	A6	A6	A6
A2	A2	A2	25		30	A5	A5	A5
A3	A3	A3	26		29	A4	A4	A4
V_{CC}	V_{CC}	V_{CC}	27		28	V_{SS}	V_{SS}	V_{SS}

	ROW ADDR	COL ADDR
x4	A0–A13	A0–A9
x8	A0–A13	A0–A8
x16	A0–A13	A0–A7

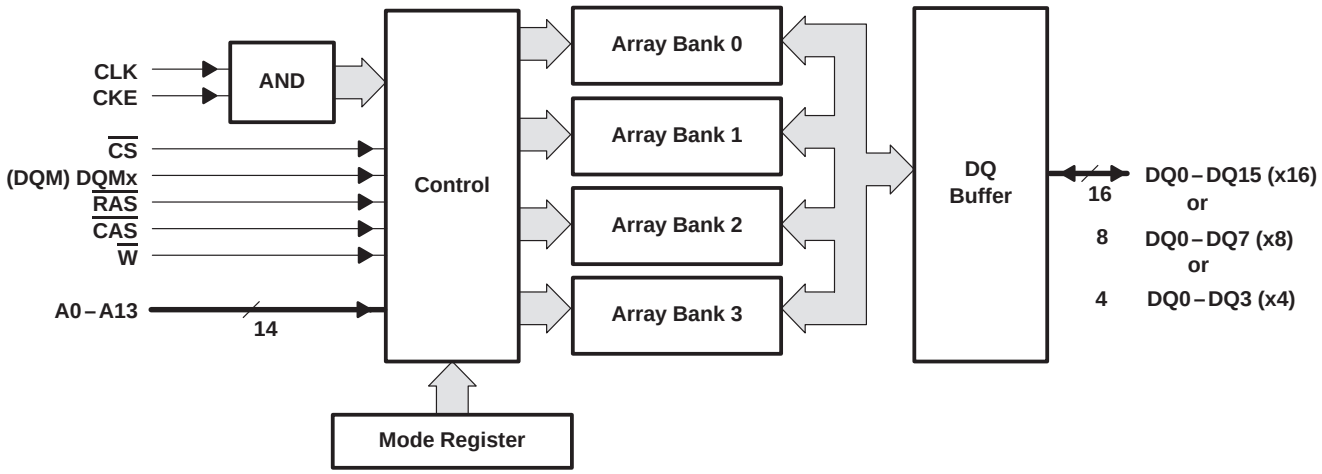
A10	Auto Precharge

BANKS	BANK-SELECT ADDRESS
4	A13–A12

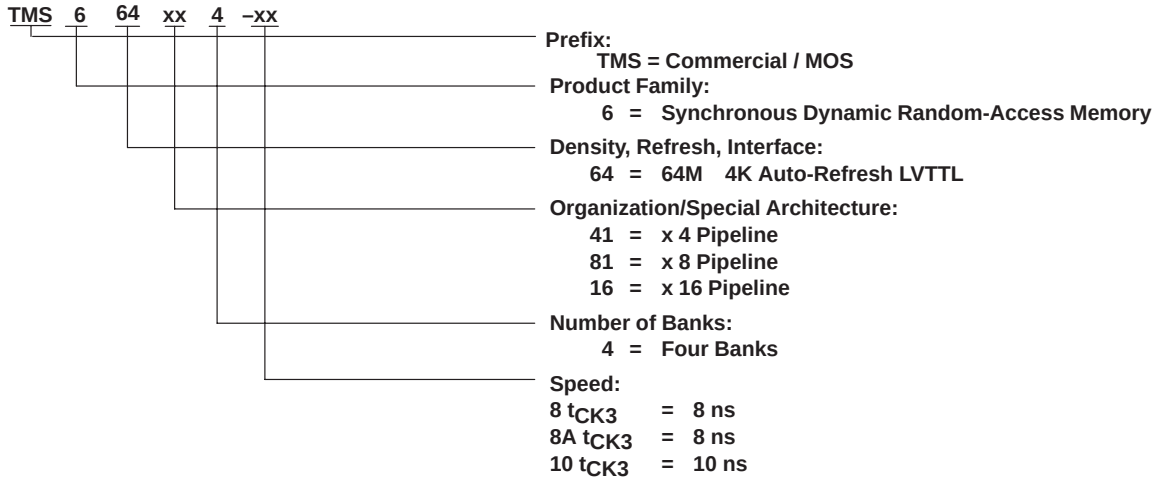
PIN NOMENCLATURE

A[0:13]	Address Inputs Four Banks Column A0 –A9 Column Addr (x4) A0 –A8 Column Addr (x8) A0 –A7 Column Addr (x16) A10 Auto Precharge A12 – A13 Bank-Select Row A0 – A11 Row Addrs A12 – A13 Bank-Select
$\overline{W}$	Write Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{CAS}$	Column-Address Strobe
CKE	Clock-Enable
CLK	System Clock
$\overline{CS}$	Chip-Select
DQ[0:3]	SDRAM Data Input/Data Output (x4)
DQ[0:7]	SDRAM Data Input/Data Output (x8)
DQ[0:15]	SDRAM Data Input/Data Output (x16)
DQMU/DQML	Data/Output Mask Enables for x16
DQM	Data/Output Mask Enables for x8/x4
NC	No External Connect
V_{CC}	Power Supply (3.3 V Typical)
V_{CCQ}	Power Supply for Output Drivers (3.3 V Typical)
V_{SS}	Ground
V_{SSQ}	Ground for Output Drivers

functional block diagram (four banks)



device numbering conventions (SDRAM family nomenclature)



operation

All inputs to the ’664xx4 SDRAM are latched on the rising edge of the system (synchronous) clock. The outputs (DQ0–DQ3 for x4, DQ0–DQ7 for x8, and DQ0–DQ15 for x16) are also referenced to the rising edge of CLK. The ’664xx4 has four banks that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh all banks alternately.

Five basic commands or functions control most operations of the ’664xx4:

- Bank activate/row-address entry
- Column-address entry/write operation
- Column-address entry/read operation
- Bank deactivate
- Auto-refresh/self-refresh entry

Additionally, operations can be controlled by three methods: using chip select ($\overline{CS}$) to select/deselect the devices, using DQMx to enable/mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation.

Table 1 through Table 3 show the various operations that are available on the ’664xx4. These truth tables identify the command and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

operation (continued)

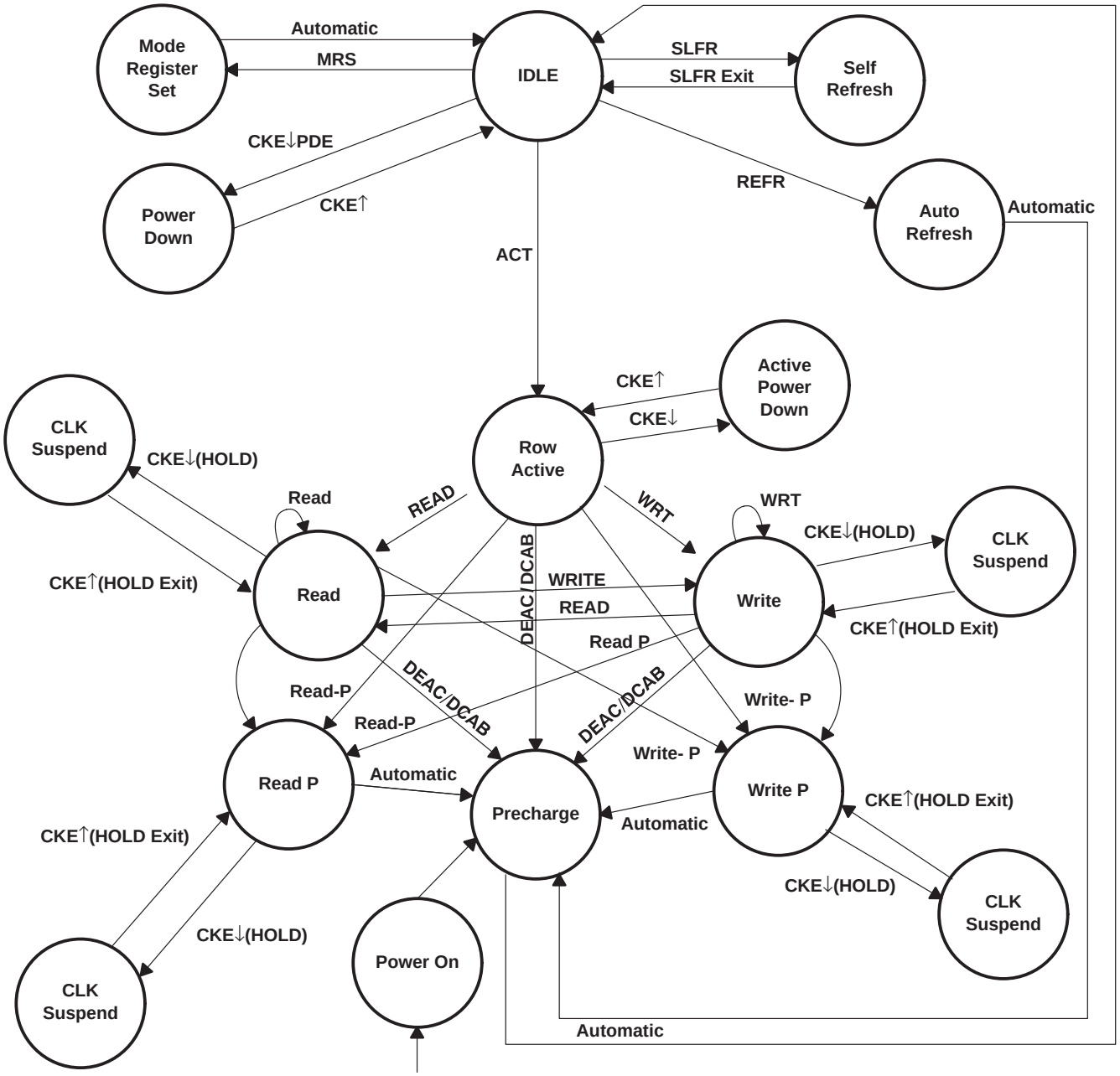


Figure 1. State Diagram

operation (continued)

Table 1. Basic Command Truth Table†‡

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A13	A12	A11	A10	A9 – A0	MNEMONIC
Mode register set	All Banks = deac	L	L	L	L	X	X	X	X	A9 = V, A8 = 0, A7 = 0, A6 – A0 = V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	BS	X	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	X	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	BS	V	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	BS	X	L	A0 – A7 = V, A8 – A9 = X, for x16 A0 – A8 = V, A9 = X, for x8 A0 – A9 = V, for x4	WRT
Column-address entry/write operation with auto-deactivate	SB = actv	L	H	L	L	BS	BS	X	H	A0 – A7 = V, A8 – A9 = X, for x16 A0 – A8 = V, A9 = X, for x8 A0 – A9 = V, for x4	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	BS	X	L	A0 – A7 = V, A8 – A9 = X, for x16 A0 – A8 = V, A9 = X, for x8 A0 – A9 = V, for x4	READ
Column-address entry/read operation with auto-deactivate	SB = actv	L	H	L	H	BS	BS	X	H	A0 – A7 = V, A8 – A9 = X, for x16 A0 – A8 = V, A9 = X, for x8 A0 – A9 = V, for x4	READ-P
No operation	X	L	H	H	H	X	X	X	X	X	NOOP
Control-input inhibit/no operation	X	H	X	X	X	X	X	X	X	X	DESL
Auto refresh§	All banks= deac	L	L	L	H	X	X	X	X	X	REFR

† For execution of these commands on cycle n, CKE must satisfy requirements for one of the following:
- CKE (n – 1) must be high
- t_{CESP} from power-down exit (PDE)
- t_{IS} and n_{CLE} from clock-suspend (HOLD) exit
- t_{CESP} and t_{RC} from self-refresh (SLFR) exit.

‡ DQMx (n) is a don't care

§ Auto-refresh or self-refresh entry requires that all banks be deactivated or be in an idle state prior to the command entry. An REFR command turns on four rows (one from each bank; therefore, 4096 REFR commands fully refresh the memory).

Legend:

n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care (either logic high or logic low)
V = Valid
actv = Activated
deac = Deactivated
BS = Logic:
(A12 = 0, A13 = 0) select bank 0
(A12 = 1, A13 = 0) select bank 1
(A12 = 0, A13 = 1) select bank 2
(A12 = 1, A13 = 1) select bank 3
SB = Select bank by A12 – A13 at cycle n

operation (continued)

Table 2. Clock-Enable (CKE) Command Truth Table†

COMMAND	STATE OF BANK(S)	CKE (n–1)	CKE (n)	$\overline{CS}$ (n)	$\overline{RAS}$ (n)	$\overline{CAS}$ (n)	$\overline{W}$ (n)	MNEMONIC
Self-refresh entry	All banks = deac	H	L	L	L	L	H	SLFR
Power-down entry at n + 1‡	All banks = no access operation§	H	L	X	X	X	X	PDE
Self-refresh exit	All banks = self-refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit¶	All banks = power down	L	H	X	X	X	X	—
CLK suspend at n+1	All banks = access operation§	H	L	X	X	X	X	HOLD
CLK suspend exit at n+1	All banks = access operation§	L	H	X	X	X	X	—

† For execution of these commands, A0–A13 (n) and DQMx (n) are don't care entries.
‡ On cycle n, the device executes the respective command (listed in Table 1). On cycle (n+1), the device enters the power-down mode.
§ A bank is no longer in an access operation one cycle after the last data-out cycle of a READ (READ-P) operation, and two cycles after the last data-in cycle of a WRT (WRT-P) operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a WRT (WRT-P) operation.
¶ If setup time from CKE high to the next CLK high satisfies t_{CESP}, the device executes the respective command (listed in Table 1). Otherwise, either the DESL or NOOP command must be applied before any other command.

Legend:
n = CLK cycle number
L = Logic low
H = Logic high
X = Don't care (either logic high or logic low)
deac = Deactivated

operation (continued)

Table 3. Data/Output Mask Enable (DQM) Command Truth Table†‡

COMMAND	STATE OF BANK(S)	DQM (DQML/DQMU)§ (n)	D0–D3 (x4) D0–D7 (x8) D0–D15 (x16) (n)	Q0–Q3 (x4) Q0–Q7 (x8) Q0–Q15 (x16) (n+2)	MNEMONIC
—	Any bank = deac	X	N/A	Hi-Z	—
—	Any bank = actv (no access operation)¶	X	N/A	Hi-Z	—
Data-in enable	Any bank = write	L	V	N/A	ENBL
Data-in mask	Any bank = write	H	M	N/A	MASK
Data-out enable	Any bank = read	L	N/A	V	ENBL
Data-out mask	Any bank = read	H	N/A	Hi-Z	MASK

† For execution of these commands on cycle n, one of the following must be true:
— CKE (n–1) must be high
— t_{CESP} from power-down exit (PDE)
— n_{CLE} from clock-suspend (HOLD) exit
— t_{CESP} and t_{RC} from self-refresh (SLFR) exit

‡ $\overline{CS}$ (n), $\overline{RAS}$ (n), $\overline{CAS}$ (n), $\overline{W}$ (n), and A0–A13 (n) are don't care entries.

§ DQM is used for x4/x8 (no byte control). DQM (n) operations correspond to D0–D7 and Q0–Q7 events. DQML/DQMU are used for x16 (for byte-control). DQML (n) operations correspond to D0–D7 and Q0–Q7 events, while DQMU (n) operations correspond to D8–D15 and Q8–Q15 events.

¶ A bank is no longer in an access operation one cycle after the last data-out cycle of a READ (READ-P) operation, and two cycles after the last data-in cycle of a WRT (WRT-P) operation. Neither the PDE nor the HOLD command is allowed on the cycle immediately following the last data-in cycle of a WRT (WRT-P) operation.

Legend:

n	=	CLK cycle number	actv	=	Activated
L	=	Logic low	deac	=	Deactivated
H	=	Logic high	write	=	Activated and accepting data in on cycle n
X	=	Don't care (either logic high or logic low)	read	=	Activated and delivering data out on cycle n + 2
V	=	Valid			
M	=	Masked input data			
N/A	=	Not applicable			
Hi-Z	=	High impedance			

burst sequence

All data for the ’664xx4 is written or read in a *burst* fashion, that is, a single starting address is entered into the device and then the ’664xx4 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first one can be at preceding, as well as succeeding, column addresses depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Table 4 through Table 6). The length of the burst sequence can be user-programmed to be 1, 2, 4, or 8. After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated.

Table 4. 2-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

Table 5. 4-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A1 – A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00

burst sequence (continued)

Table 6. 8-Bit Burst Sequences

	INTERNAL COLUMN ADDRESS A2 – A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

latency

The beginning data-output cycle of a read burst can be programmed to occur two or three CLK cycles after the READ command (see Figure 2 on how to set the mode register.) This feature allows adjustment of the ’664xx4 to operate in accordance with the system’s capability to latch the data output from the ’664xx4. The delay between the READ command and the beginning of the output burst is known as CAS latency (also known as read latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum CAS latencies is restricted, based on the particular maximum frequency rating of the ’664xx4. Once the mode register has been set (see the section on setting the mode register), subsequent changes to the CAS latency are prohibited.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK as the WRT command. The write latency is fixed and is not determined by the mode-register contents.

four-bank operation

The ’664xx4 contains four independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank then must be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding $\overline{RAS}$ low, $\overline{CAS}$ high, $\overline{W}$ high, and A12 – A13 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ (READ-P) or a WRT (WRT-P) command, or by using the bank-deactivate (DEAC) command. All banks can be deactivated at once by using the DCAB command (see Table 1 for a description of the bank-deactivation, and Figure 25 and Figure 26 for examples of the operation).

four-bank row-access operation

One of the features of the four-bank operation is access to information on random rows at a higher rate of operation than is possible with a standard DRAM. This is accomplished by activating one of the banks with a row address and, while the data stream is being accessed to/from that bank, activating one of the other banks with other row addresses. When the data stream to/from the first activated bank is complete, the data stream to/from the second activated bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses or the entry of new row addresses for other banks which currently are deactivated. In this manner, operation can continue in an interleaved fashion. Figure 29A is an example of four-bank, row-interleaving, read bursts with automatic deactivate with a CAS latency of 3 and a burst length of 8. Figure 29B is an example of four-bank, row-interleaving, read bursts with automatic deactivate with a CAS latency of 3 and a burst length of 4.

four-bank column-access operation

The availability of four banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A12–A13 for the four-bank column-access operation can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 30 is an example of four-bank, column-interleaving, read bursts with a CAS latency of 3 and a burst length of 2.

bank deactivation (precharge)

All banks can be deactivated simultaneously (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A12–A13 select the bank to be precharged (see Table 1; Figure 27 and Figure 31 provide examples). A bank can also be deactivated automatically by using A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank, selected by A12–A13, is automatically deactivated upon completion of the access burst. If A10 is held low during READ- or WRT-command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted as READ-P and WRT-P. See Figure 29A and Figure 29B for examples.

chip-select

$\overline{CS}$ (chip-select) can be used to select or deselect the ’664xx4 for command entries, which might be required for multiple-memory-device decoding. If $\overline{CS}$ is held high on the rising edge of CLK (DESL command), the device does not respond to $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ until the device is selected again by holding $\overline{CS}$ low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Table 1 and Table 2). Using $\overline{CS}$ does not affect an access burst that is in progress; the DESL command can restrict only $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ inputs to the ’664xx4.

data/output mask

Masking of individual data cycles within a burst sequence can be accomplished by using the MASK command (see Table 3). If DQM (or DQML/DQMU of x16) is held high on the rising edge of CLK during a write burst, the incident data word (referenced to the same rising edge of CLK) on DQ0–DQ7 [or (DQ0–DQ7)/(DQ8–DQ15) of x16] is ignored. If DQM (or DQML/DQMU of x16) is held high on the rising edge of CLK for a read burst, DQ0–DQ7 [or (DQ0–DQ7)/(DQ8–DQ15) of x16], referenced to the second rising edge of CLK, are in the high-impedance state. The application of DQM (DQML/DQMU) to data-output cycles (READ burst) involves a latency of two CLK cycles, but the application of DQM to data-in cycles (WRITE burst) has no latency. The MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read-burst or a write-burst sequence. Figure 14, Figure 38 and Figure 39 show examples of data/output masking.

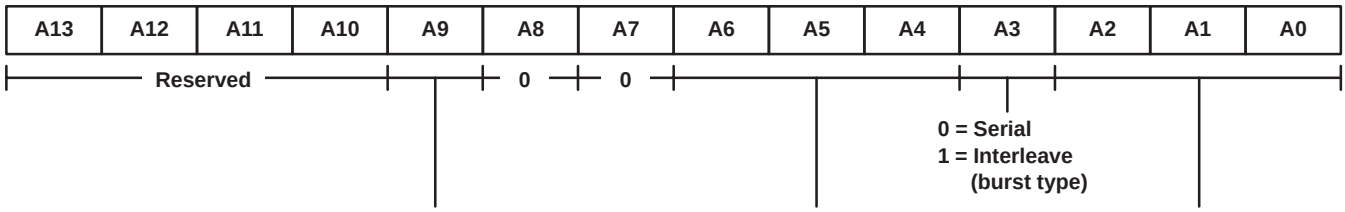
CLK-suspend/power-down mode

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus occurring at the immediate next rising edge of CLK is frozen at its current state and no further inputs are accepted until CKE is returned high. This is known as a CLK-suspend operation and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE is returned high. See Figure 42 and Figure 43 for examples.

If CKE is brought low when no READ (READ-P) or WRT (WRT-P) command is in progress, the device enters power-down mode. If all banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or auto-refresh periods to reduce input-buffer power. After power-down mode has been entered, no further inputs are accepted until CKE returns high. To ensure that data in the device remains valid during the power-down mode, the self-refresh command (SLRF) must be executed concurrently with the power-down entry (PDE) command. When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time (t_{CESP}) is satisfied. Table 2 shows the command configuration for a CLK-suspend/power-down operation; Figure 18 and Figure 19 show examples of the procedure.

setting the mode register

The ’664xx4 contains a mode register that must be user-programmed with the CAS latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information entered on address lines A0–A9. A logic 0 must be entered on A7 and A8, but A10–A13 are “don’t care” entries for the ’664xx4. When A9 = 1, the write burst length is always 1. When A9 = 0, the write burst length is defined by A2–A0. Figure 2 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ low and the input-mode word valid on A0–A9 on the rising edge of CLK (see Table 1). The MRS command can be executed only when all banks are deactivated and may not be executed while a burst is active. See Figure 24 and Figure 35 for examples.



REGISTER BIT A9	WRITE BURST LENGTH
0	A2–A0
1	1

REGISTER BITS†			CAS LATENCY‡§
A6	A5	A4	
0	0	0	Reserved
0	0	1	2
0	1	0	Reserved
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

REGISTER BITS†			BURST LENGTH
A2	A1	A0	
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

† All other combinations are reserved.
‡ Refer to timing requirements for minimum valid read latencies based on maximum frequency rating.
§ Once the mode register has been set, subsequent changes to the CAS latency is prohibited.

Figure 2. Mode-Register Programming

refresh

The ’664xx4 must be refreshed at intervals not exceeding t_{REF} (see timing requirements) or data cannot be retained. Refresh is accomplished by performing one of the following:

- An ACTV command ($\overline{RAS}$-only refresh) to every row in all banks
- 4096 auto-refresh (REFR) commands
- Putting the device in self-refresh mode

Regardless of the method used, refresh must be accomplished before t_{REF} has expired. See Figure 34 for an example.

auto refresh

Before performing an auto refresh, all banks must be deactivated (placed in precharge). To enter a REFR command, $\overline{RAS}$ and $\overline{CAS}$ must be low and $\overline{W}$ must be high during the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, all banks of the ’664xx4 are refreshed. The external address and bank-select A12–A13 are ignored. The execution of a REFR command automatically deactivates all banks upon completion of the internal auto-refresh cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before t_{REF} expires.

self-refresh mode

To enter self-refresh mode, all banks of the ’664xx4 must be deactivated first and an SLFR command must be executed (see Table 2). The SLFR command is identical to the REFR command except that CKE is low. For proper entry of the SLFR command, CKE is brought low for the same rising edge of CLK when $\overline{RAS}$ and $\overline{CAS}$ are low and $\overline{W}$ is high. CKE must be held low to stay in self-refresh mode. In the self-refresh mode, refreshing signals are generated internally for all banks with all external signals (except CKE) being ignored. Data can be retained by the device automatically for an indefinite period when power is maintained (consumption is reduced to a minimum). To exit self-refresh mode, CKE must be brought high. New commands are issued after t_{RC} has expired. If CLK is made inactive during self-refresh, it must be returned to an active and stable condition before CKE is brought high to exit self-refresh mode (see Figure 19).

Prior to entering and upon exiting self-refresh mode, 4096 REFR commands are recommended before continuing with normal device operations. This ensures that the SDRAM is fully refreshed.

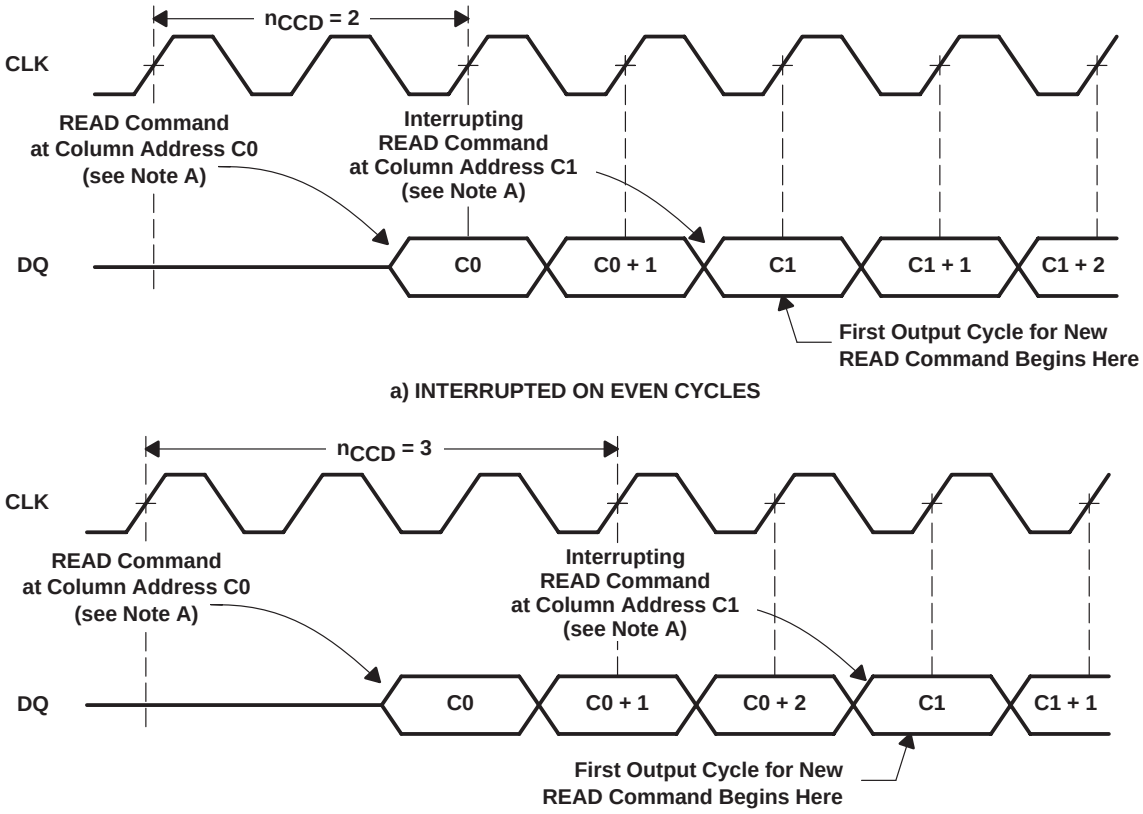
interrupted bursts

A read or write can be interrupted before the burst sequence is complete with no adverse effects to the operation. This is accomplished by entering certain superseding commands as listed in Table 7 and Table 8, provided that all timing requirements are met. The interruption of READ-P and WRT-P operations is not supported.

Table 7. Read-Burst Interruption

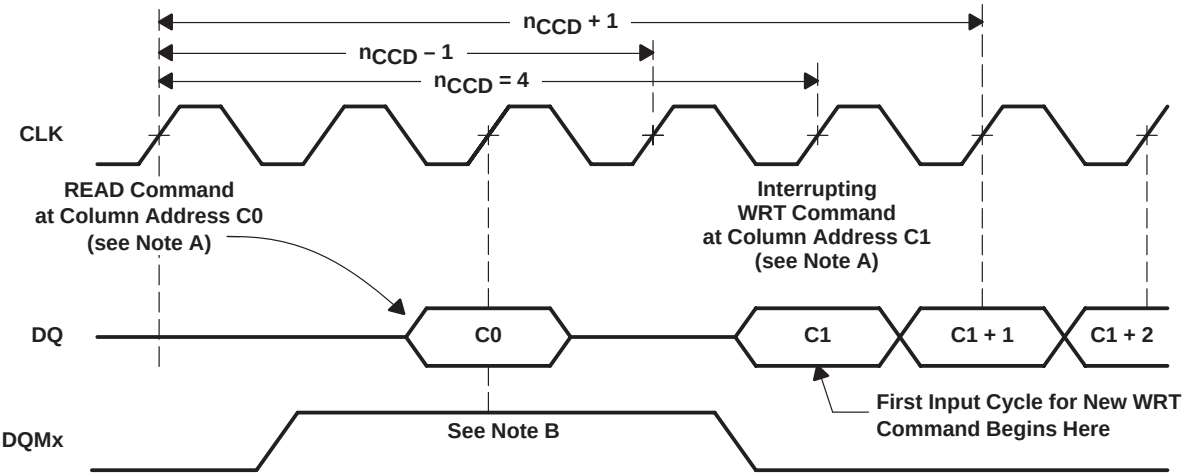
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met and new output cycles begin (see Figure 3).
WRT, WRT-P	The WRT (WRT-P) command immediately supersedes the read burst in progress. To avoid data contention, DQMx must be high before the WRT (WRT-P) command to mask output of the read burst on cycles (n_{CCD}–1), n_{CCD}, and (n_{CCD}+1), assuming there is any output on these cycles (see Figure 4).
DEAC, DCAB	The DQ bus is in the high-impedance state when n_{HZP} cycles are satisfied or upon completion of the read burst, whichever occurs first (see Figure 5 and Figure 22).

interrupted bursts (continued)



NOTE A: For this example, assume CAS latency = 2 and burst length > 2.

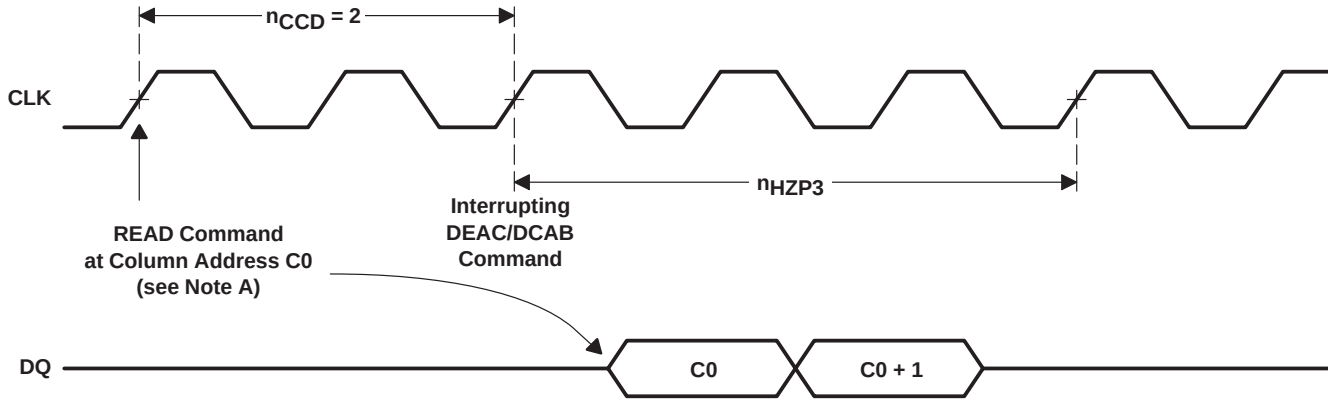
Figure 3. Read Burst Interrupted by Read Command



NOTES: A. For this example, read latency = 2 and burst length > 2.
B. DQMx must be high to mask output of the read burst on cycles (n_{CCD}–1), (n_{CCD}), and (n_{CCD}+1).

Figure 4. Read Burst Interrupted by Write Command

interrupted bursts (continued)



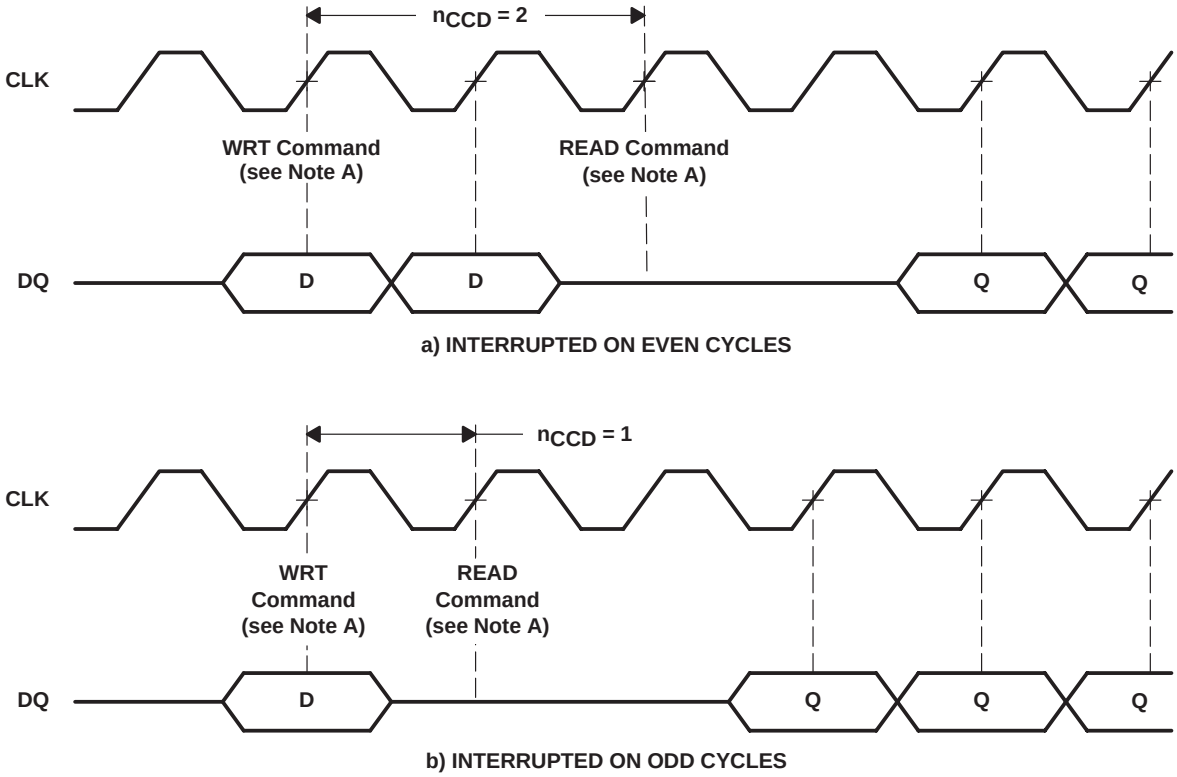
NOTE A: For this example, assume CAS latency = 3 and burst length > 2.

Figure 5. Read Burst Interrupted by DEAC Command

Table 8. Write-Burst Interruption

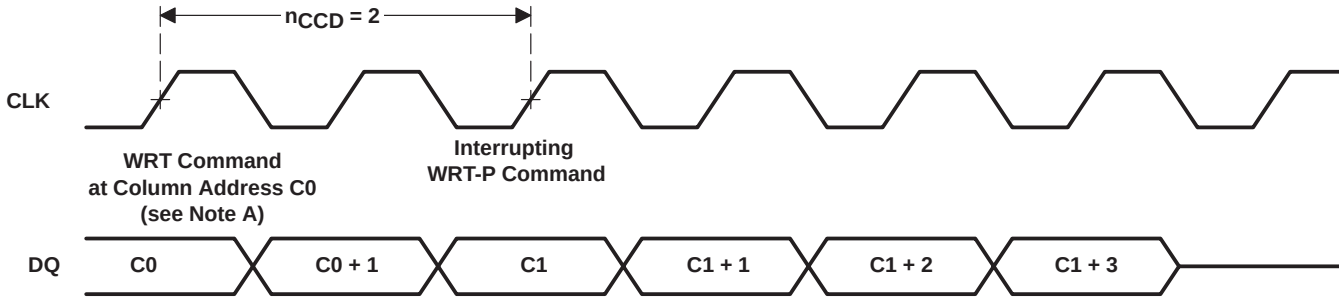
INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
READ, READ-P	Data that was input on the previous cycle is written and no further data inputs are accepted (see Figure 6).
WRT, WRT-P	The new WRT (WRT-P) command and data-in immediately supersede the write burst in progress (see Figure 7).
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQMx must be used to mask the DQ bus such that the write recovery specification (n_{WR}) is not violated by the interrupt (see Figure 8).

interrupted bursts (continued)



NOTE A: For this example, assume CAS latency = 2, burst length > 2.

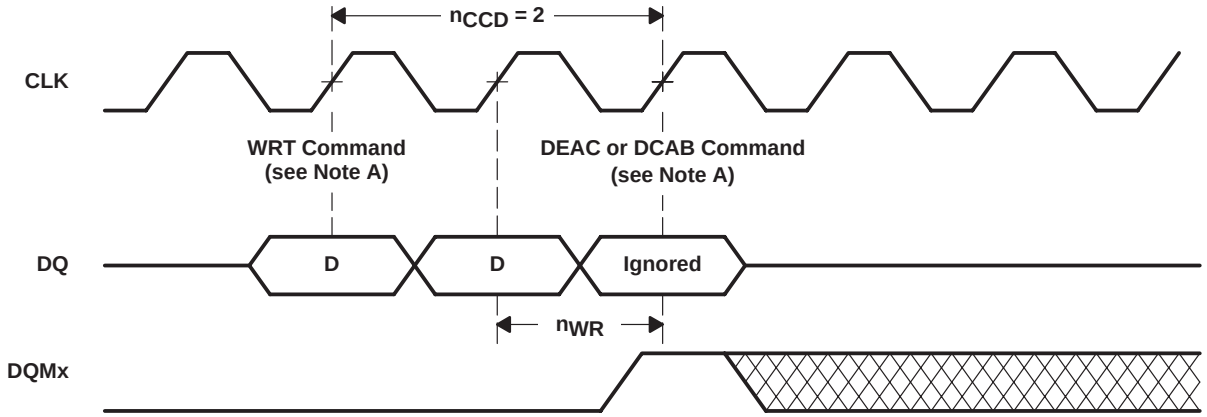
Figure 6. Write Burst Interrupted by Read Command



NOTE A: For this example, burst length > 2.

Figure 7. Write Burst Interrupted by Write Command

interrupted bursts (continued)



NOTE A: For the purposes of this example, CAS latency = 2 and burst length > 2.

Figure 8. Write Burst Interrupted by DEAC/DCAB Command

power up

Device initialization should be performed after a power up to the full V_{CC} level. After power is established, a 200-µs interval is required (with no inputs other than CLK). After this interval, all banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization. See Figure 24.

absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 0.5 V to 4.6 V
Supply voltage range for output drivers, V_{CCQ} . . . . . – 0.5 V to 4.6 V
Voltage range on any input pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Voltage range on any output pin (see Note 1) . . . . . – 0.5 V to V_{CC} + 0.5 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{CCQ}	Supply voltage for output drivers‡	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{SSQ}	Supply voltage for output drivers		0		V
V_{IH}	High-level input voltage	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	– 0.3		0.8	V
T_A	Operating ambient temperature	0		70	°C

‡ $V_{CCQ} \leq V_{CC} + 0.3$ V

electrical characteristics over recommended ranges of supply voltage and operating ambient temperature (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS		- 8 (x8/x4)		- 8 (x16)		- 8A (x8/x4)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –2 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CCQ} Output disabled			±10		±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, t_{RC} ≥ t_{RC} MIN, I_{OH}/I_{OL} = 0 mA (see Notes 3, 4, and 5)	CAS latency = 2		115		125		95	mA
			CAS latency = 3		125		135		125	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 6)			1		1		1	mA
I_{CC2PS}		CKE and CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 7)			1		1		1	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 6)			40		40		40	mA
I_{CC2NS}		t_{CK} =∞ (see Note 7)			5		5		5	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Notes 3 and 6)			8		8		8	mA
I_{CC3PS}		CKE and CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 3 and 7)			8		8		8	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Notes 3 and 6)			50		55		50	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 3 and 7)			15		15		15	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, (see Notes 8, 9, and 10)	CAS latency = 2		165		165		120	mA
			CAS latency = 3		225		245		165	mA
I_{CC5}	Auto-refresh current	t_{RC} ≥ t_{RC} MIN (see Notes 4 and 7)	CAS latency = 2		150		150		150	mA
			CAS latency = 3		150		150		150	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			1		1		1	mA

NOTES:
2. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
3. Only one bank is activated.
4. t_{RC} ≥ t_{RC} MIN
5. Control, DQ, and address inputs change state twice during t_{RC}.
6. Control, DQ, and address inputs change state once every 30 ns.
7. Control, DQ, and address inputs do not change state (stable).
8. 4-bank ping-pong, burst length = 4, n_{CCD} = 4 cycles, data pattern 0011.
9. Column address and bank address increment every 4 cycles.
10. A t_{CK} of 10 ns is used to obtain I_{CC4} for CL3 of the -8A speed grade.

electrical characteristics over recommended ranges of supply voltage and operating ambient temperature (unless otherwise noted) (see Note 2) (continued)

PARAMETER		TEST CONDITIONS		– 8A (x16)		– 10 (x8/x4)		– 10 (x16)		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = –2 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	0 V ≤ V_I ≤ V_{CC} + 0.3 V, All other pins = 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	0 V ≤ V_O ≤ V_{CCQ} Output disabled			±10		±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, t_{RC} ≥ t_{RC} MIN, I_{OH}/I_{OL} = 0 mA (see Notes 3, 4, and 5)	CAS latency = 2		105		95		105	mA
			CAS latency = 3		135		105		115	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 6)			1		1		1	mA
I_{CC2PS}		CKE and CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 7)			1		1		1	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 6)			40		40		40	mA
I_{CC2NS}		t_{CK} =∞ (see Note 7)			5		5		5	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Notes 3 and 6)			8		8		8	mA
I_{CC3PS}		CKE and CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 3 and 7)			8		8		8	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Notes 3 and 6)			55		55		60	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CLK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 3 and 7)			15		15		15	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, (see Notes 8, 9, and 10)	CAS latency = 2		140		120		140	mA
			CAS latency = 3		165		175		200	mA
I_{CC5}	Auto-refresh current	t_{RC} ≥ t_{RC} MIN (see Notes 4 and 7)	CAS latency = 2		150		150		150	mA
			CAS latency = 3		150		150		150	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			1		2		2	mA

NOTES: 2. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
3. Only one bank is activated.
4. t_{RC} ≥ t_{RC} MIN
5. Control, DQ, and address inputs change state twice during t_{RC}.
6. Control, DQ, and address inputs change state once every 30 ns.
7. Control, DQ, and address inputs do not change state (stable).
8. 4-bank ping-pong, burst length = 4, n_{CCD} = 4 cycles, data pattern 0011.
9. Column address and bank address increment every 4 cycles.
10. A t_{CK} of 10 ns is used to obtain I_{CC4} for CL3 of the -8A speed grade.

capacitance over recommended ranges of supply voltage and operating ambient temperature f = 1 MHz (see Note 11)

PARAMETER		MIN	MAX	UNIT
$C_{i(S)}$	Input capacitance, CLK input	2.5	4	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A13, $\overline{CS}$, DQMx, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	2.5	5	pF
$C_{i(E)}$	Input capacitance, CKE input		5	pF
C_o	Output capacitance	4	6.5	pF

NOTE 11: V_{CC} = 3.3 ± 0.3 V and bias on pins under test is 0 V.

ac timing requirements† ‡

			’664xx4-8		’664xx4-8A		’664xx4-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CK2}	Cycle time, CLK	CAS latency = 2	10		15		15		ns
t_{CK3}	Cycle time, CLK	CAS latency = 3	8		8		10		ns
t_{CH}	Pulse duration, CLK high		3		3		3		ns
t_{CL}	Pulse duration, CLK low		3		3		3		ns
t_{AC2}	Access time, CLK high to data out (see Note 12)	CAS latency = 2		6		7.5		7.5	ns
t_{AC3}	Access time, CLK high to data out (see Note 12)	CAS latency = 3		6		6		7.5	ns
t_{OH2}	Hold time, CLK high to data out with 50-pF load	CAS latency = 2	3		3		3		ns
t_{OH3}	Hold time, CLK high to data out with 50-pF load	CAS latency = 3	3		3		3		ns
t_{LZ}	Delay time, CLK high to DQ in low-impedance state (see Note 13)		1		1		2		ns
t_{HZ}	Delay time, CLK high to DQ in high-impedance state (see Note 14)			8		8		10	ns
t_{IS}	Setup time, address, control, and data input		2		2		2		ns
t_{IH}	Hold time, address, control, and data input		1		1		1		ns
t_{CESP}	Power down/self-refresh exit time (see Note 15)		8		8		10		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command		48	100000	48	100000	50	100000	ns
t_{RC}	Delay time, ACTV, REFR, or SLFR command to ACTV, MRS, REFR, or SLFR command		68		68		80		ns
t_{RCD}	Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 16)		20		20		30		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command		20		20		30		ns
t_{RRD}	Delay time, ACTV command in one bank to ACTV command in the other bank		16		16		20		ns
t_{RSA}	Delay time, MRS command to ACTV, MRS, REFR, or SLFR command		16		16		20		ns

† See Parameter Measurement Information for load circuits (see Figure 9).
‡ All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 12. t_{AC} is referenced from the rising transition of CLK that precedes the data-out cycle. For example, the first data-out t_{AC} is referenced from the rising transition of CLK that is CAS latency – one cycle after the READ command. An access time is measured at output reference level 1.5 V.
13. t_{LZ} is measured from the rising transition of CLK that is CAS latency – one cycle after the READ command.
14. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
15. See Figure 18 and Figure 19.
16. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

ac timing requirements†‡ (continued)

			’664xx4-8		’664xx4-8A		’664xx4-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{APR}	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command		$t_{RP} – (CL –1) * t_{CK}$						ns
t_{APW}	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command		$t_{RP} + 1\ t_{CK}$						ns
t_T	Transition time		1	5	1	5	1	5	ns
t_{REF}	Refresh interval			64		64		64	ms
n_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command		1		1		1		cycle
n_{CCD}	Delay time, READ or WRT command to an interrupting command		1		1		1		cycle
n_{CDD}	Delay time, $\overline{CS}$ low or high to input enabled or inhibited		0	0	0	0	0	0	cycle
n_{CLE}	Delay time, CKE high or low to CLK enabled or disabled		1	1	1	1	1	1	cycle
n_{CWL}	Delay time, final data in of WRT command to READ, READ-P, WRT, or WRT-P command		1		1		1		cycle
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in		0	0	0	0	0	0	cycle
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out		2	2	2	2	2	2	cycle
n_{HZP2}	Delay time, DEAC or DCAB command to DQ in high-impedance state	CAS latency = 2		2		2		2	cycle
n_{HZP3}	Delay time, DEAC or DCAB command to DQ in high-impedance state	CAS latency = 3		3		3		3	cycle
n_{WCD}	Delay time, WRT command to first data in		0	0	0	0	0	0	cycle

† See Parameter Measurement Information for load circuits (see Figure 9).
‡ All references are made to the rising transition of CLK, unless otherwise noted.

PARAMETER MEASUREMENT INFORMATION

general information for ac timing measurements

The ac timing measurements are based on signal rise and fall times equal to 1 ns (t_T = 1 ns) and a midpoint reference level of 1.5 V (INPUT = 2.8 V, 0 V) for LVTTL. For signal rise and fall times greater than 1 ns, the reference level should be changed to V_{IH} MIN and V_{IL} MAX instead of the midpoint level. All specifications referring to READ commands are valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.

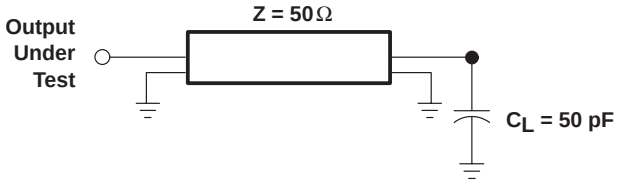


Figure 9. ac Load Circuit

PARAMETER MEASUREMENT INFORMATION

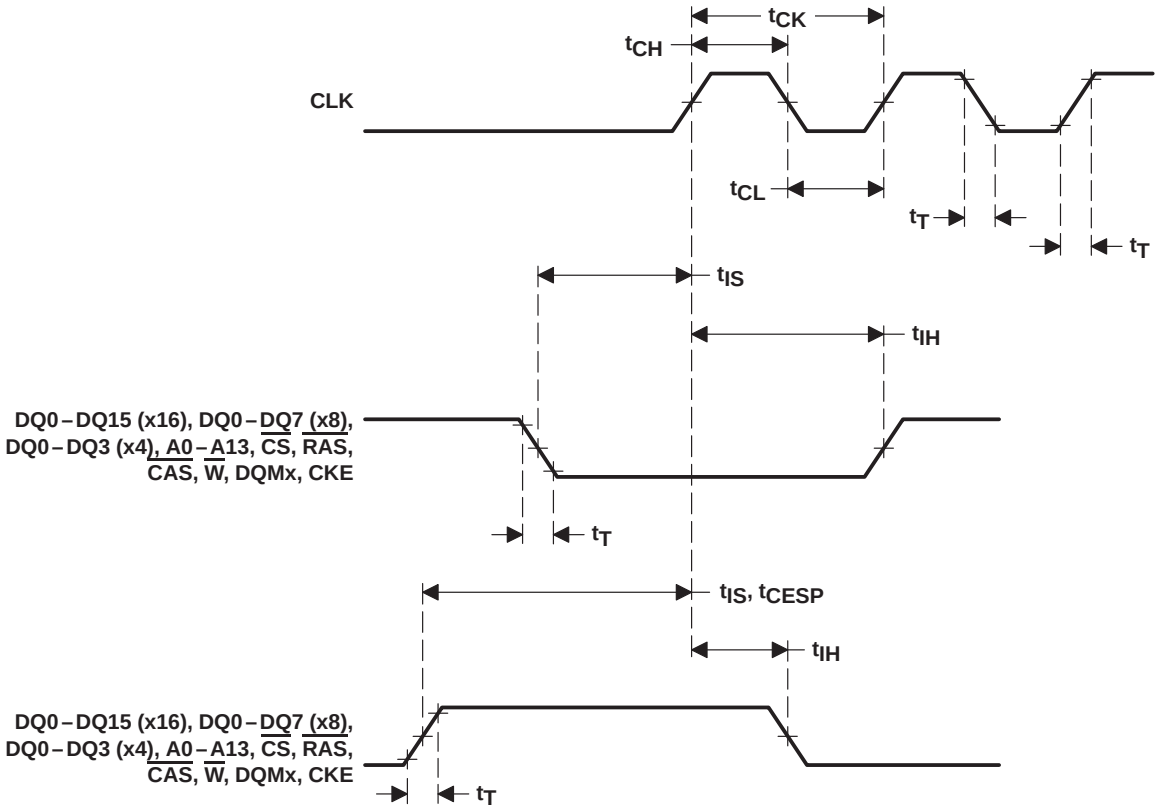


Figure 10. Input-Attribute Parameters

PARAMETER MEASUREMENT INFORMATION

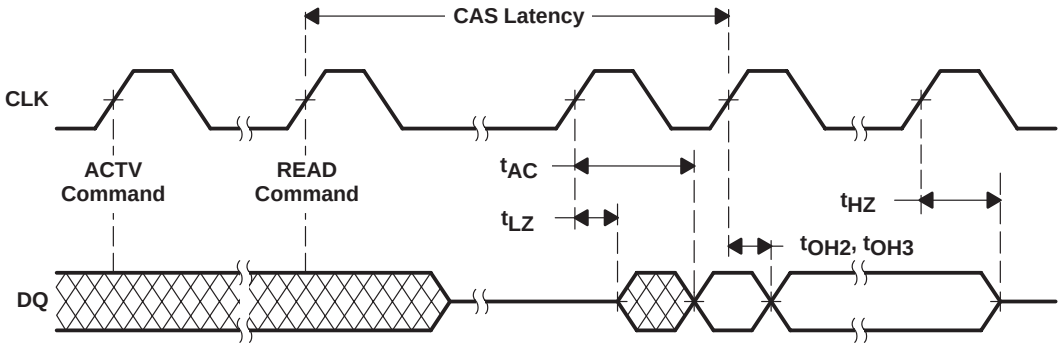
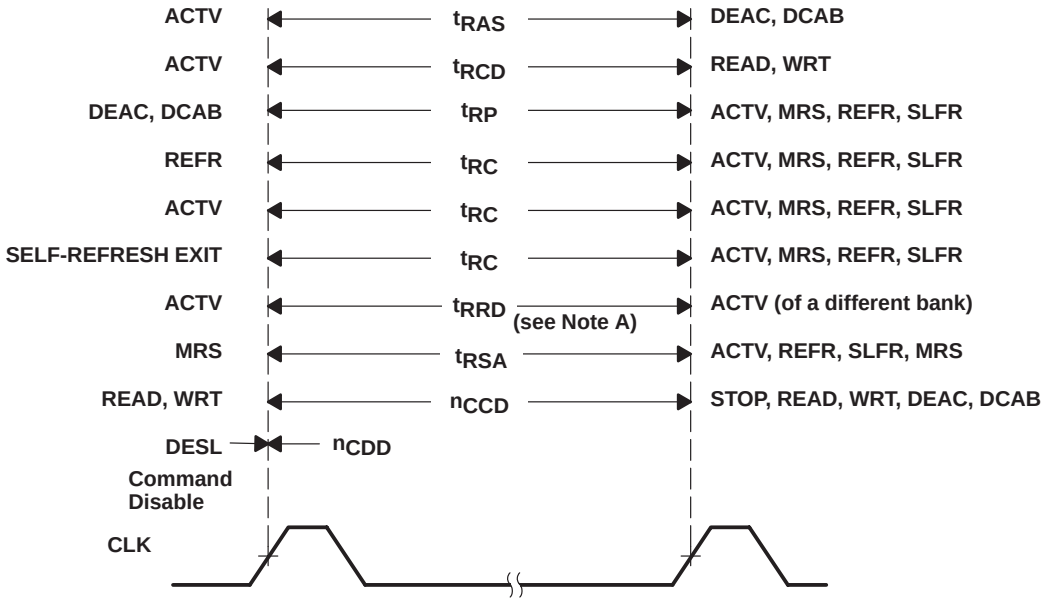


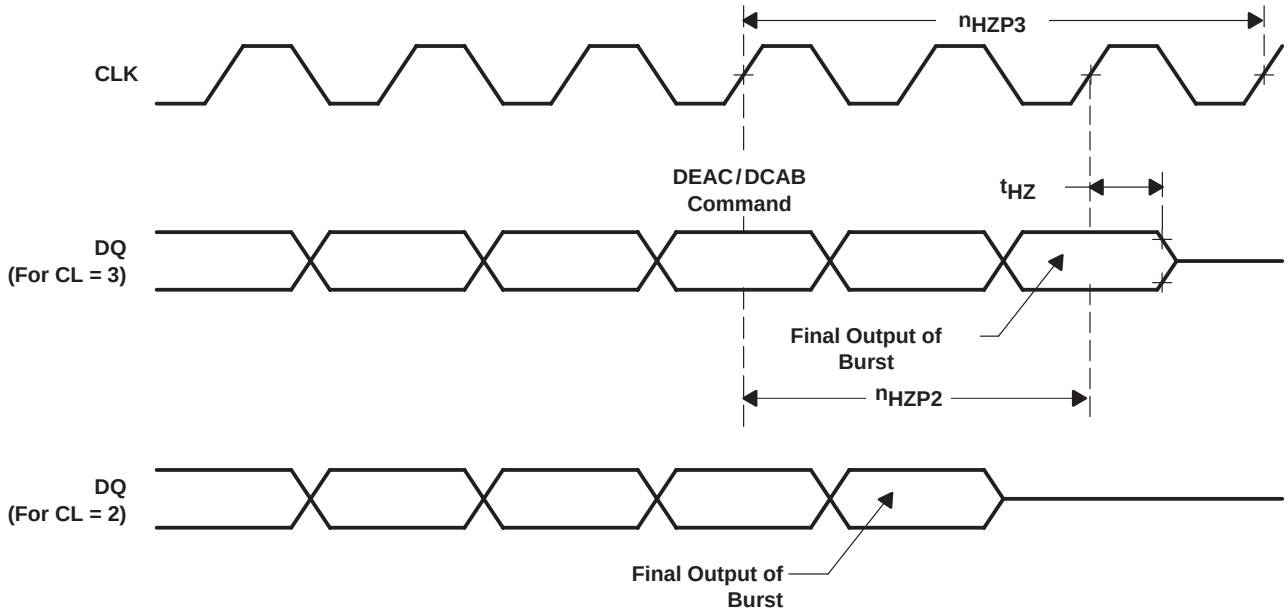
Figure 11. Output Parameters



NOTE A: t_{RRD} is specified for command execution in one bank to command execution in another bank.

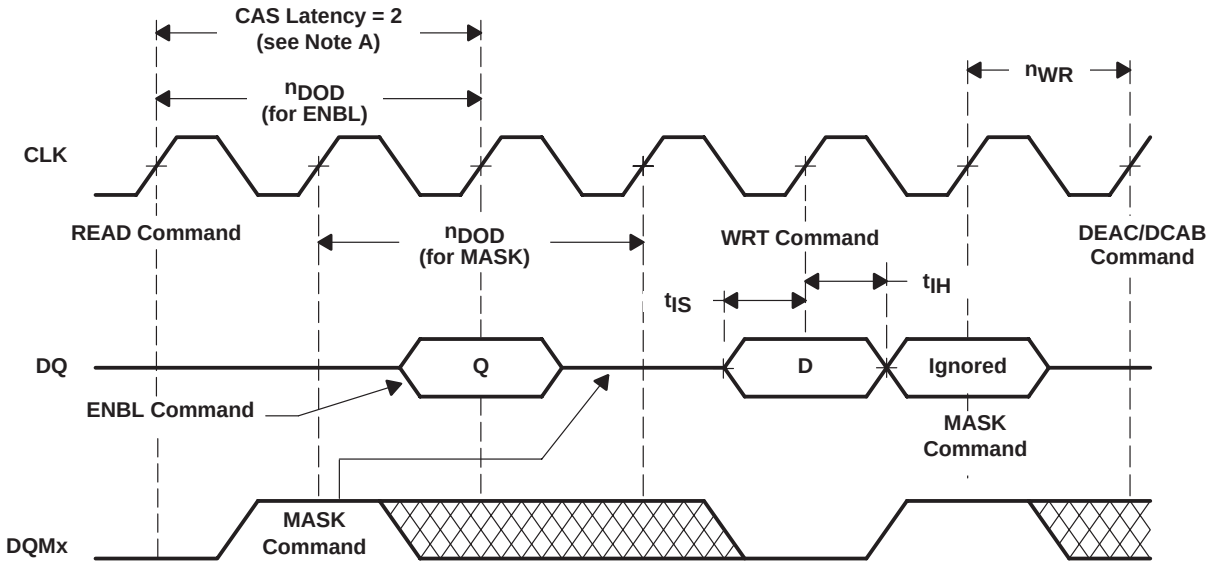
Figure 12. Command-to-Command Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume CAS latency = 2, 3 and burst length > 1.

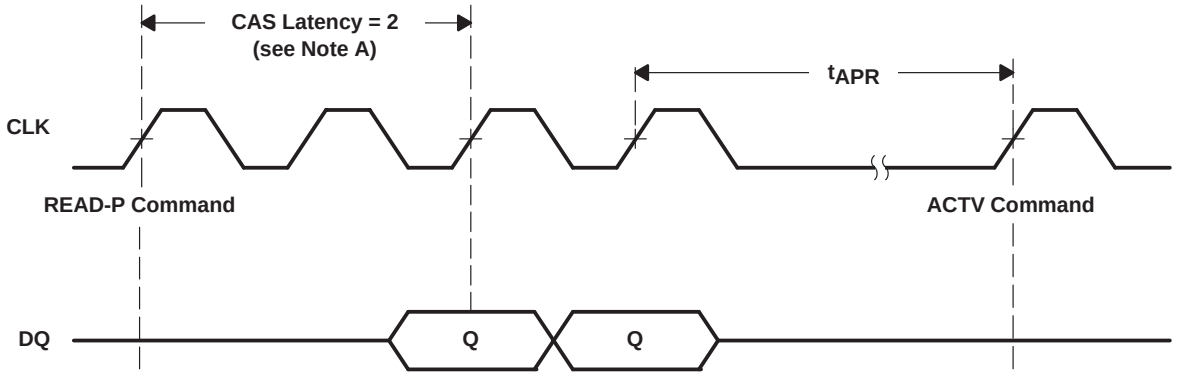
Figure 13. Final Data Output to DEAC or DCAB Command for CAS Latency = 2, 3



NOTE A: For this example, assume CAS latency = 2 and burst length = 2.

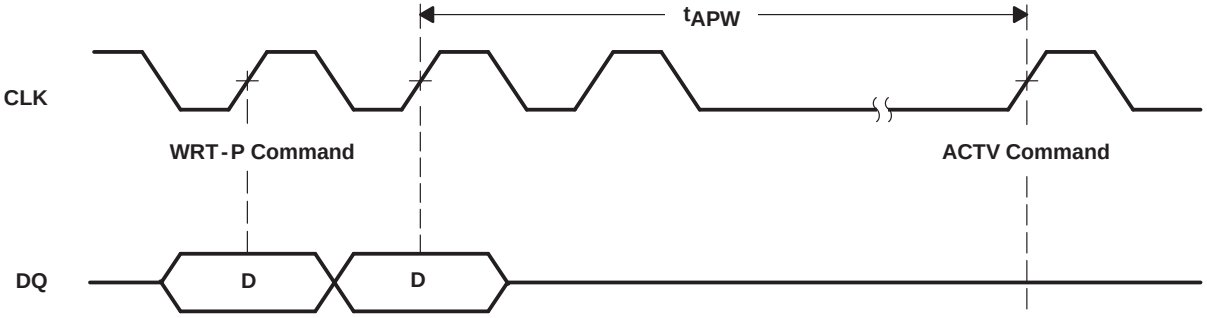
Figure 14. DQ Masking

PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume CAS latency = 2 and burst length = 2.

Figure 15. Read Automatic-Deactivate (Autoprecharge)



NOTE A: For this example, the burst length = 2.

Figure 16. Write Automatic-Deactivate (Autoprecharge)

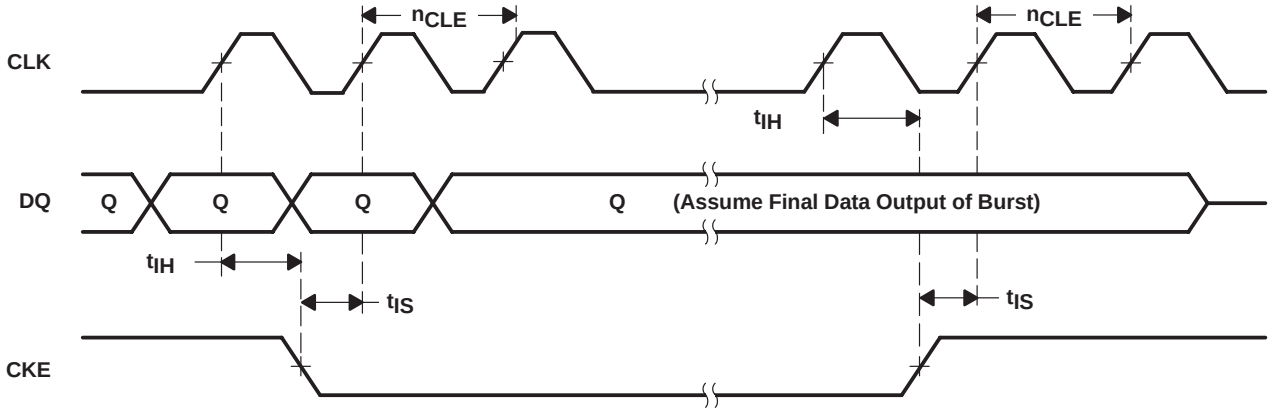


Figure 17. CLK-Suspend Operation (Assume Burst Length = 4)

PARAMETER MEASUREMENT INFORMATION

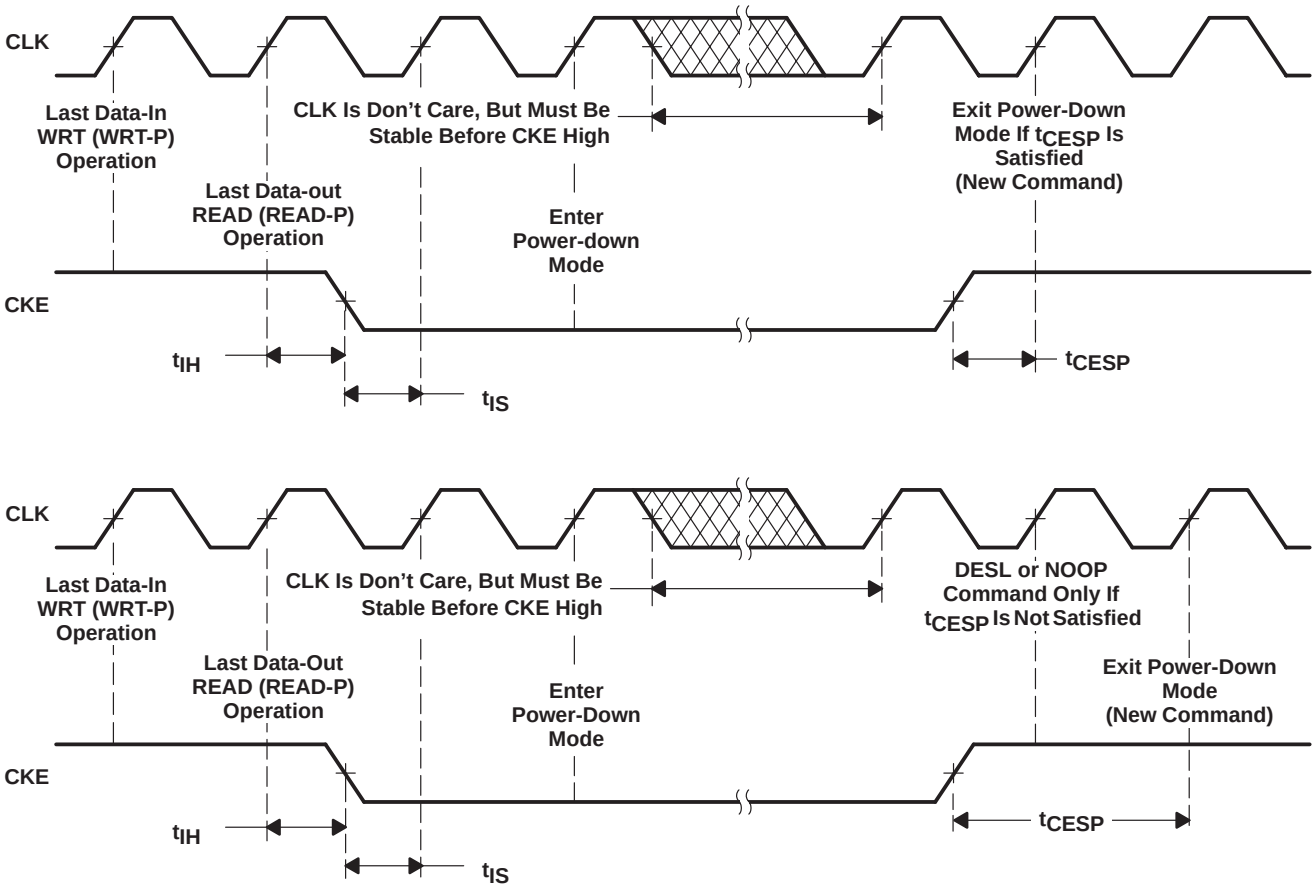
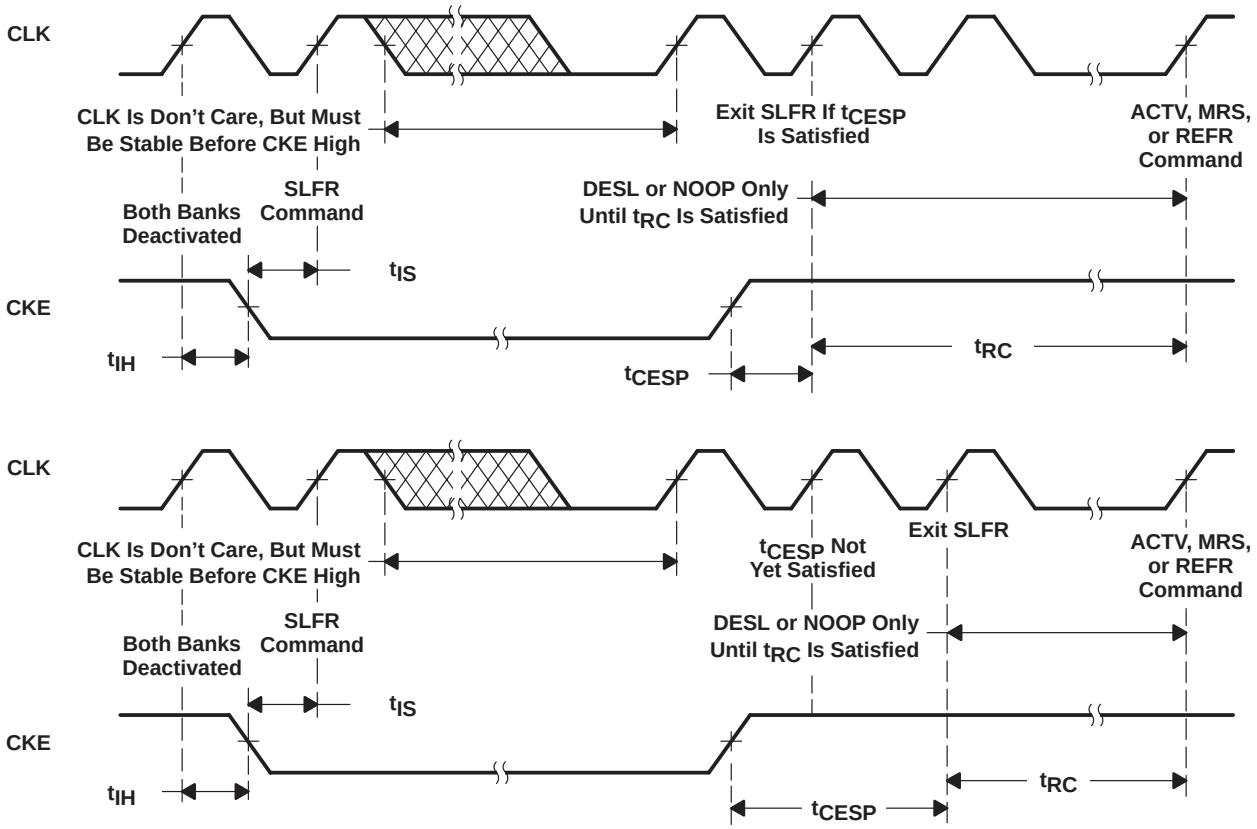


Figure 18. Power-Down Operation

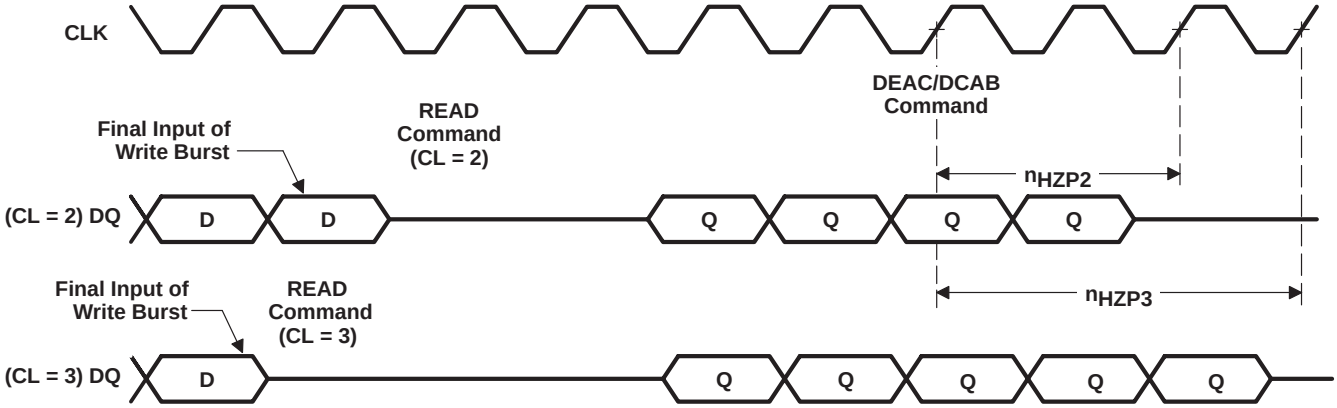
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Assume both banks are deactivated before the execution of SLFR.
B. Before/after self-refresh mode, 4K burst auto-refresh cycles are recommended to ensure that the SDRAM is fully refreshed.

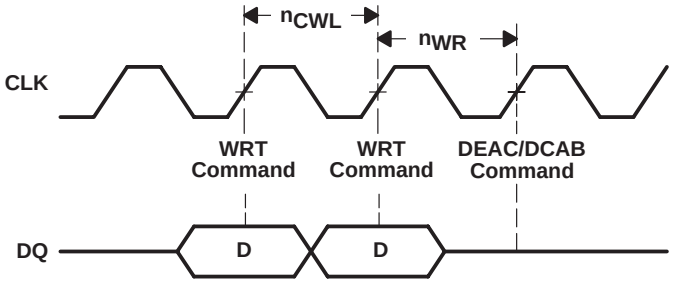
Figure 19. Self-Refresh Entry/Exit

PARAMETER MEASUREMENT INFORMATION



NOTE A: Assume burst length = 8.

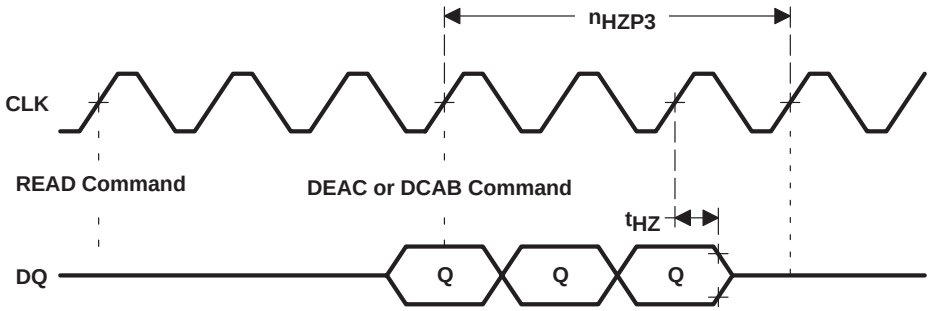
Figure 20. Write Burst Followed by DEAC/DCAB-Interrupted Read



NOTE A: For this example, assume burst length = 1.

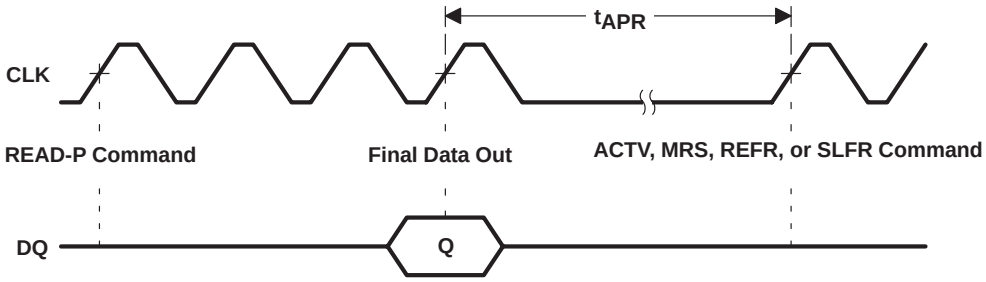
Figure 21. Write Followed by Deactivate

PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume CAS latency = 3, and burst length = 4.

Figure 22. Read Followed by Deactivate



NOTE A: For this example, assume CAS latency = 3, and burst length = 1.

Figure 23. Read With Auto-Deactivate

PARAMETER MEASUREMENT INFORMATION

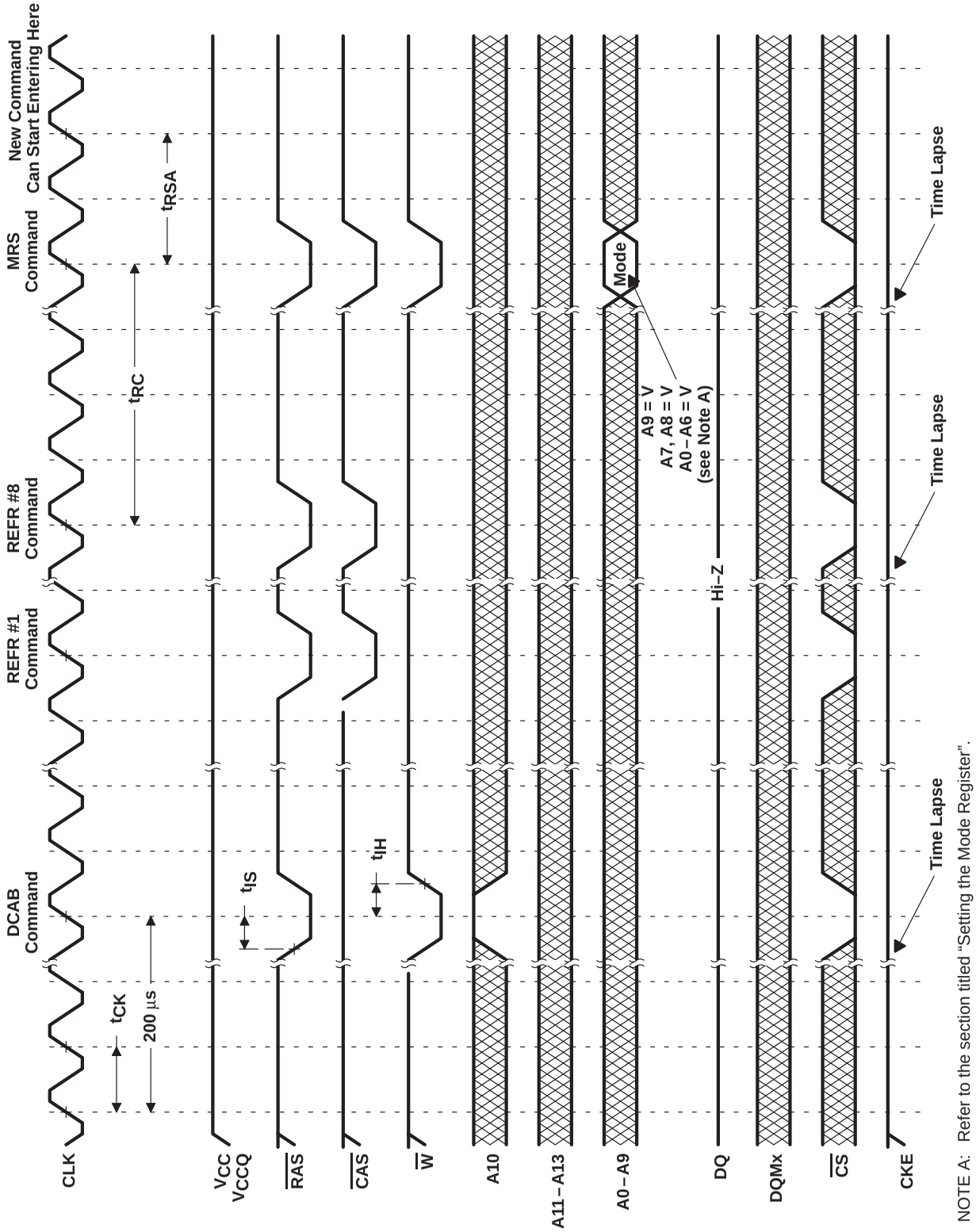
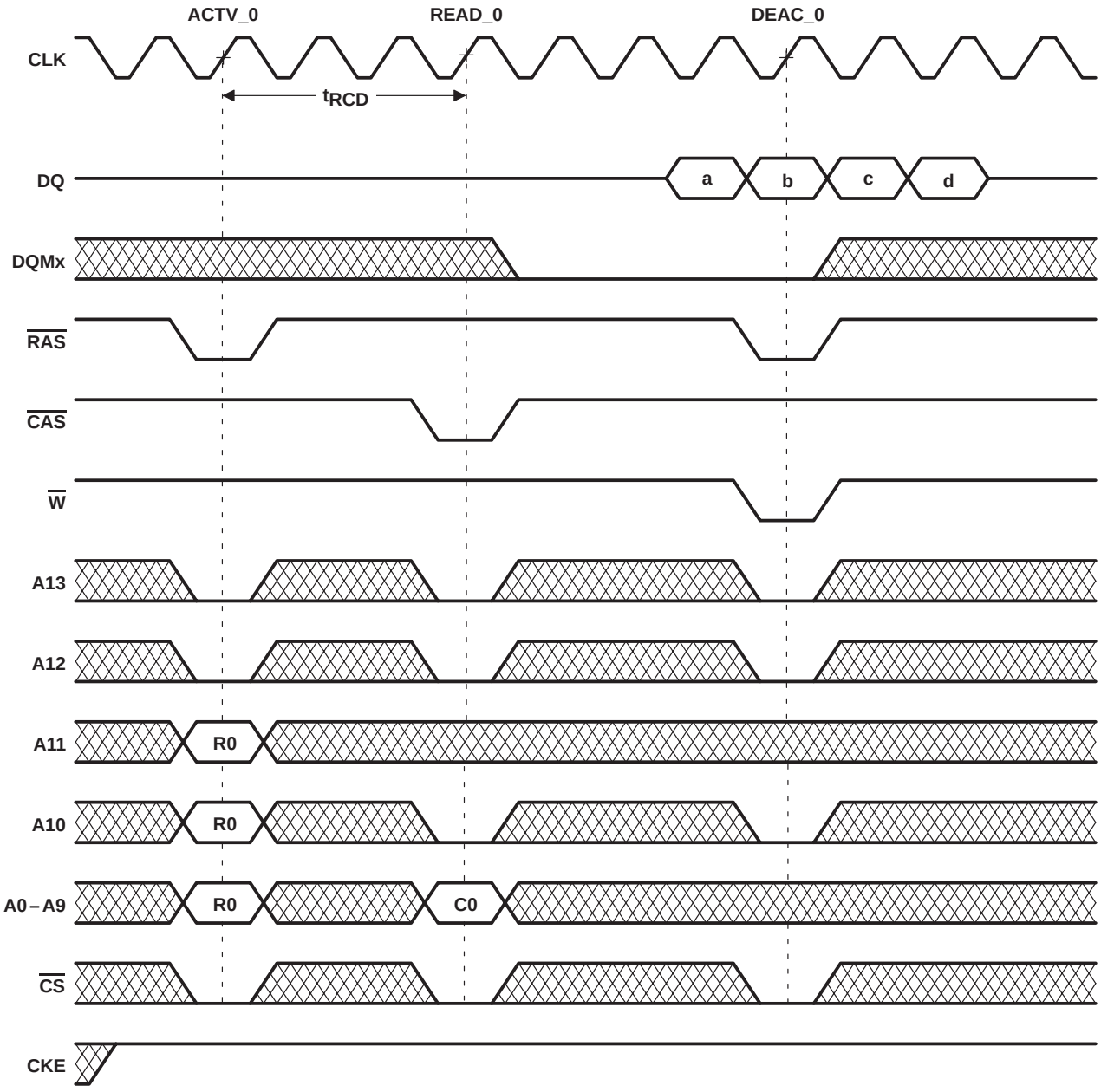


Figure 24. Power-Up Sequence

NOTE A: Refer to the section titled "Setting the Mode Register".

PARAMETER MEASUREMENT INFORMATION

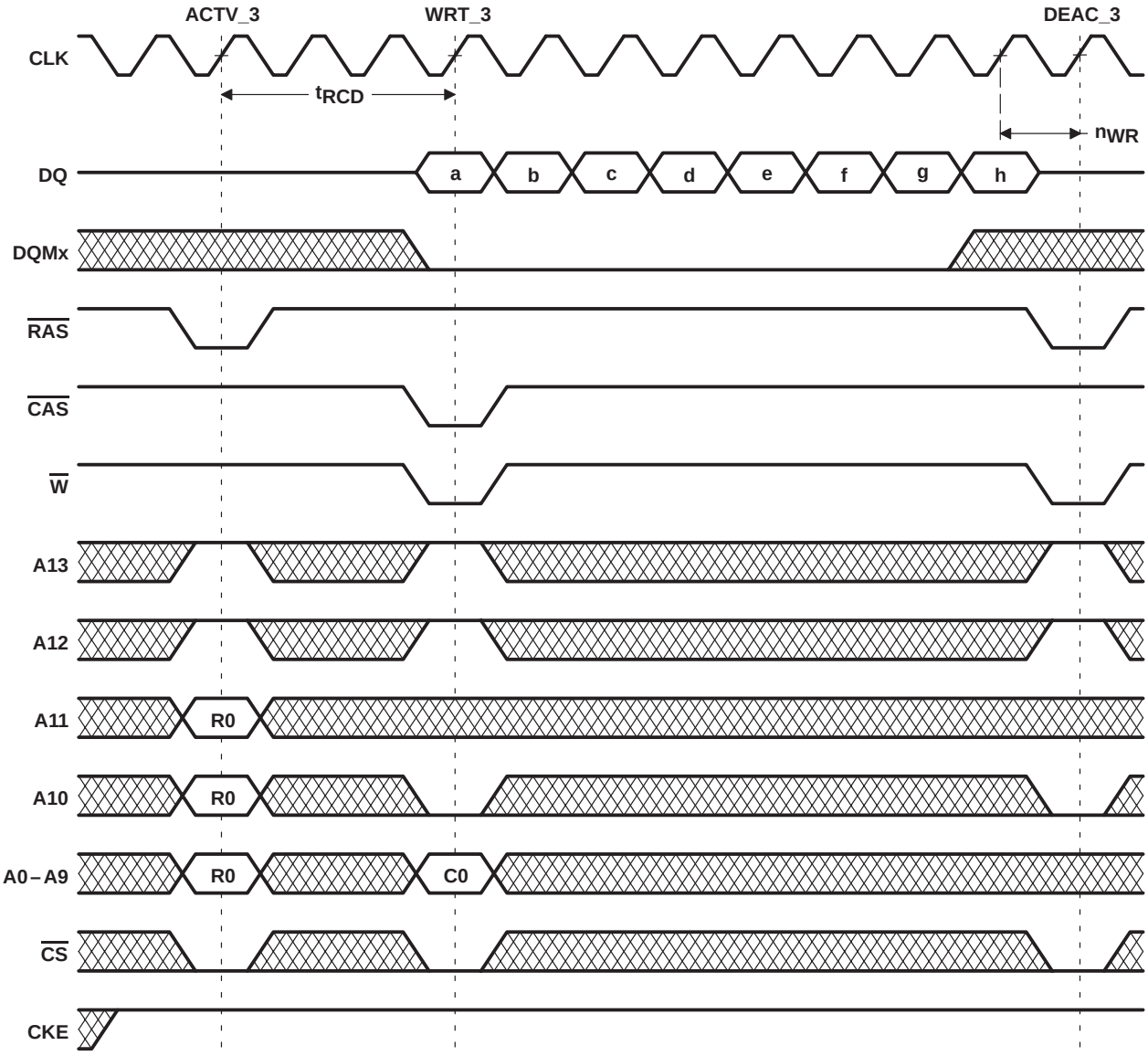


BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(0 – 3)	ADDR	a	b	c	d
Q	0	R0	C0†	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting address C0 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 125 MHz.

Figure 25. Read Burst (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



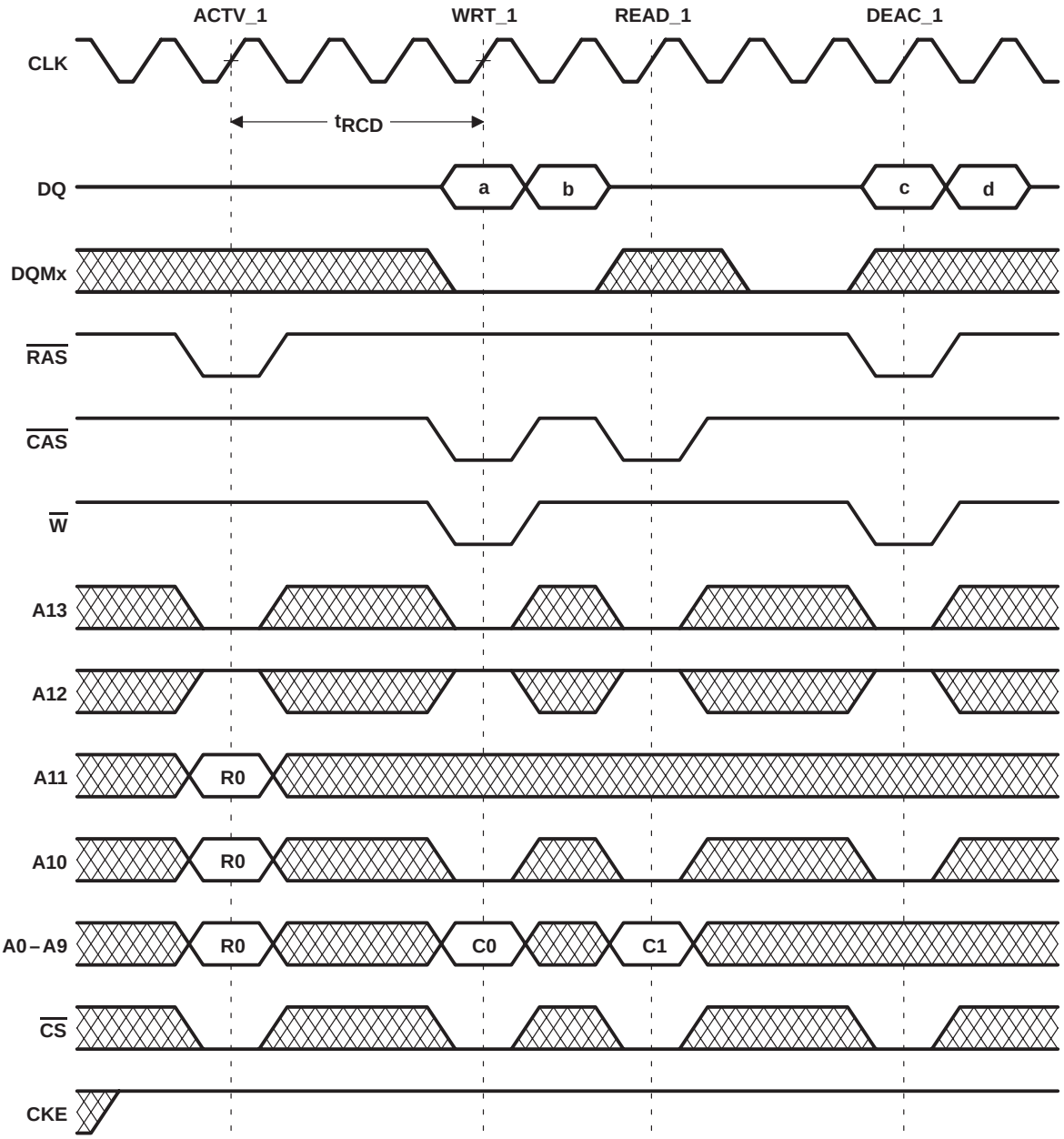
BURST TYPE (D/Q)	BANK (0 – 3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	3	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and starting address C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} and n_{WR} for the ’664xx4 at 125 MHz.

Figure 26. Write Burst (burst length = 8)

PARAMETER MEASUREMENT INFORMATION

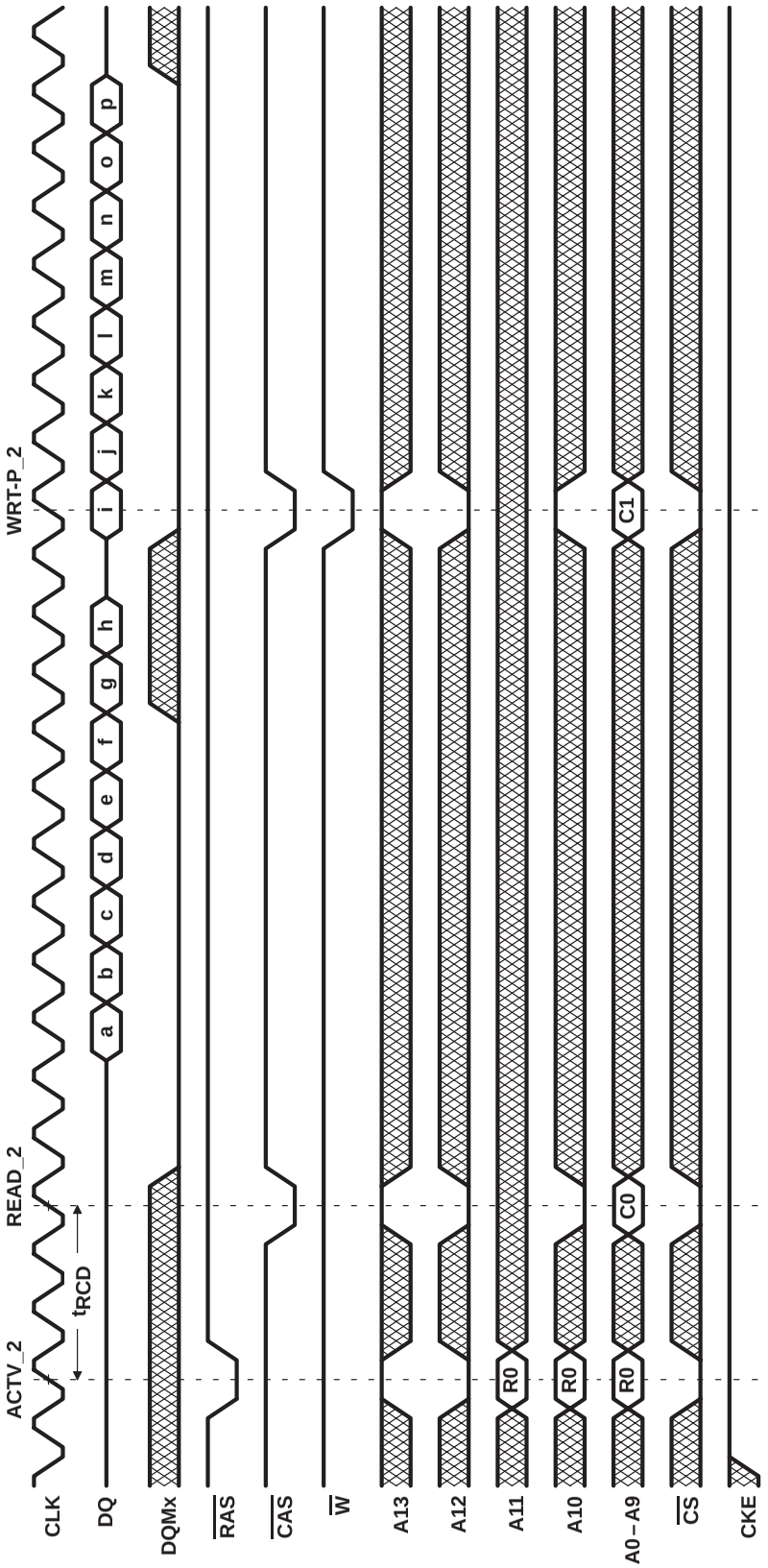


BURST TYPE (D/Q)	BANK (0 – 3)	ROW ADDR	BURST CYCLE a	b	c	d
D	1	R0	C0†	C0 + 1		
Q	1	R0			C1	C1 + 1

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} for the ’664xx4 at 125 MHz.

Figure 27. Write-Read Burst (CAS latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



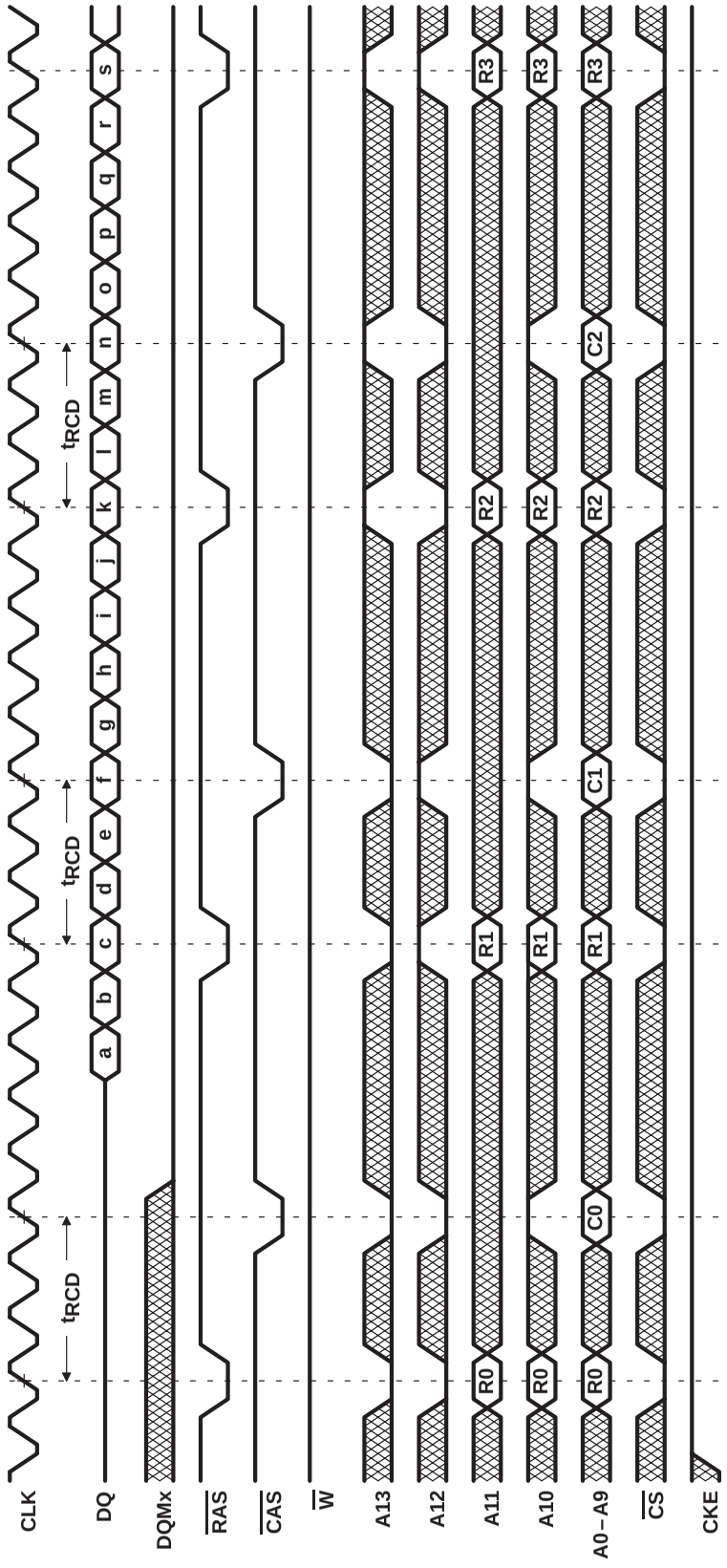
BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
Q	2	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7								
D	2	R0									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7

† Column-address sequence depends on programmed burst type and starting address C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 125 MHz.

Figure 28. Read-Write Burst With Automatic Deactivate (CAS latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



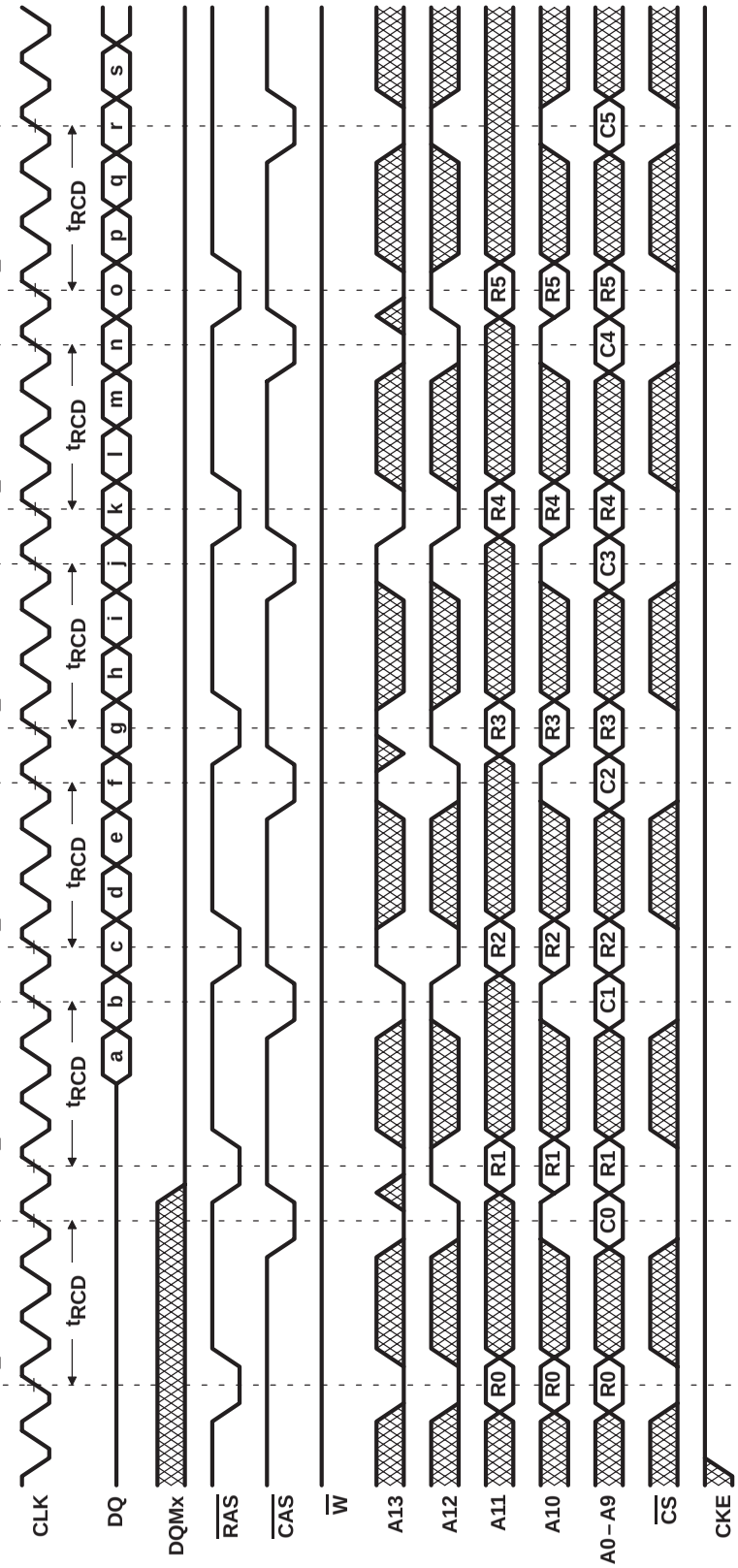
BURST TYPE	BANK	ROW	BURST CYCLE																		
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s
Q	0	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7											
Q	1	R1									C1	C1+1	C1+2	C1+3	C1+4	C1+5	C1+6	C1+7			
Q	2	R2																	C2	C2+1	C2+2

† Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 125 MHz.

Figure 29. *[A]* Four-Bank Row-Interleaving Burst Length of 8 With Automatic Deactivate (CAS latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



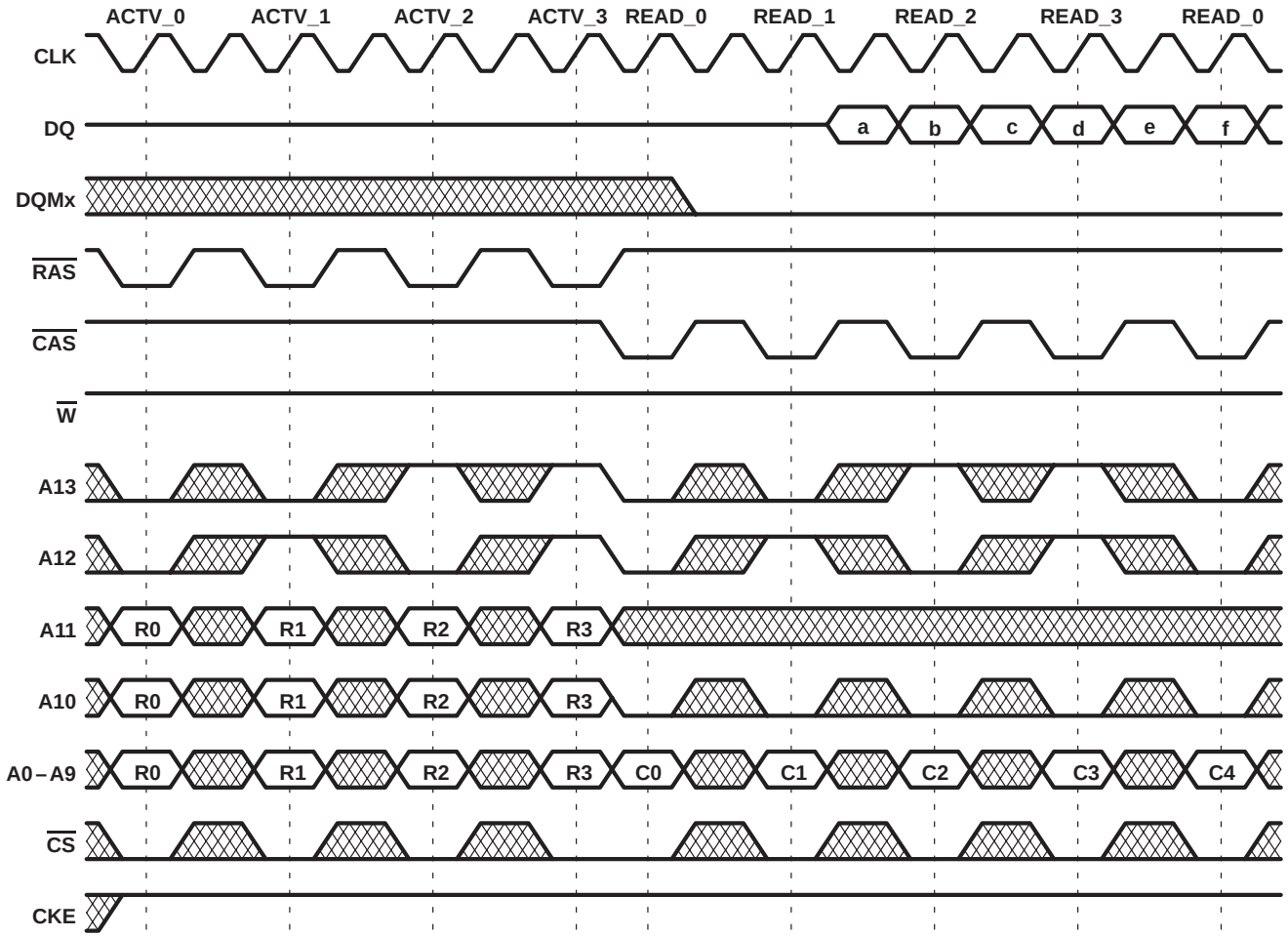
BURST TYPE	BANK	ROW	BURST CYCLE																	
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	. . .
Q	0	R0	C0†	C0+1	C0+2	C0+3																
Q	1	R1					C1	C1+1	C1+2	C1+3												
Q	2	R2									C2	C2+1	C2+2	C2+3								
Q	3	R3													C3	C3+1	C3+2	C3+3				
Q	0	R4																	C4	C4+1	C4+2	. . .

† Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 125 MHz.

Figure 29. *[B]* Four-Bank Row-Interleaving Burst Length of 4 With Automatic Deactivate (CAS latency = 3, burst length = 4) (Cont'd)

PARAMETER MEASUREMENT INFORMATION

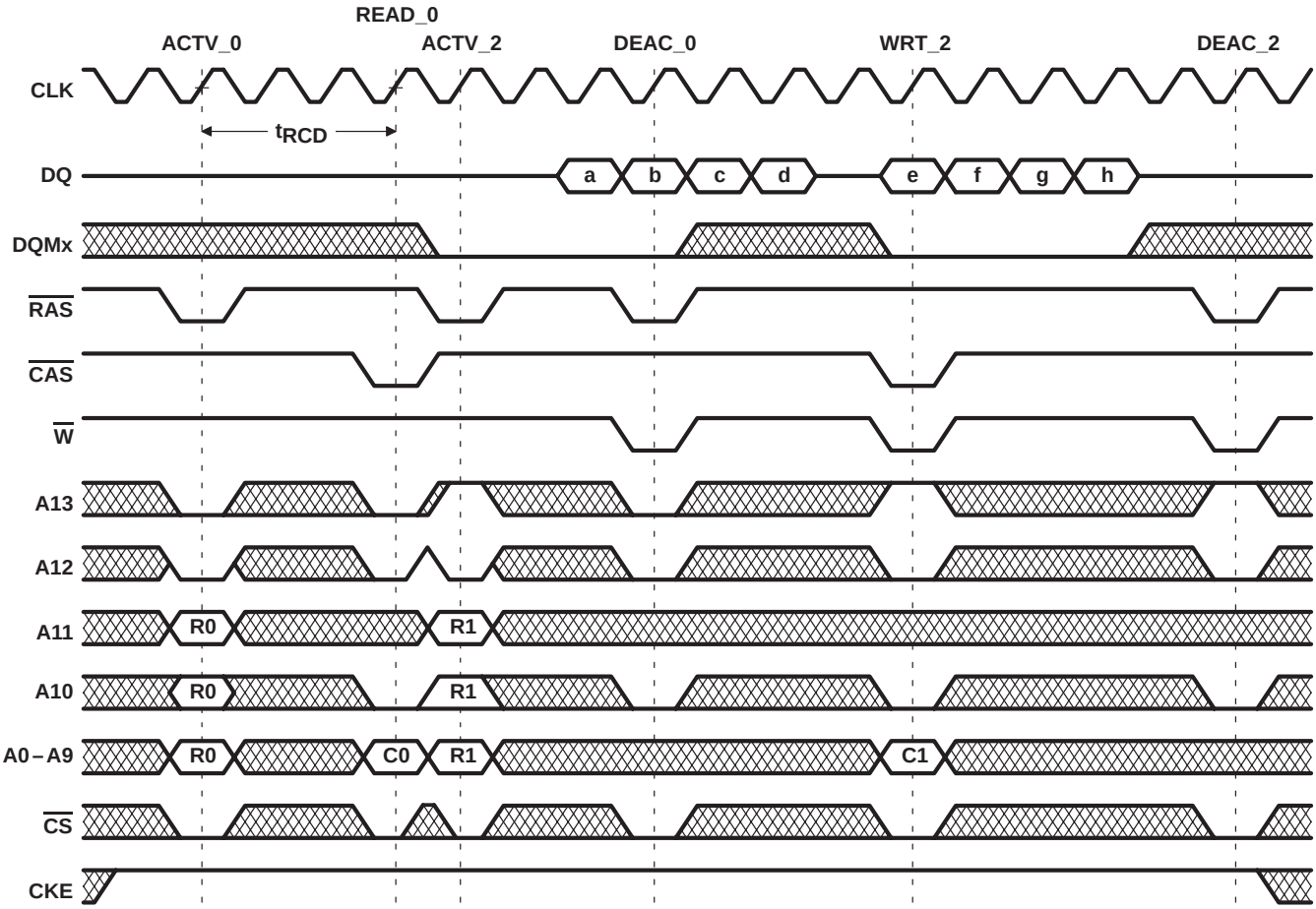


BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	. . .	. . .
Q	0	R0	C0†	C0+1								
Q	1	R1			C1	C1+1						
Q	2	R2					C2	C2+1				
Q	3	R3							C3	C3+1		
. . .	. . .	. . .									. . .	. . .

† Column-address sequence depends on programmed burst type and starting addresses C0, C1, and C2 (see Table 4).

Figure 30. Four-Bank Column-Interleaving Read Bursts (CAS latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION

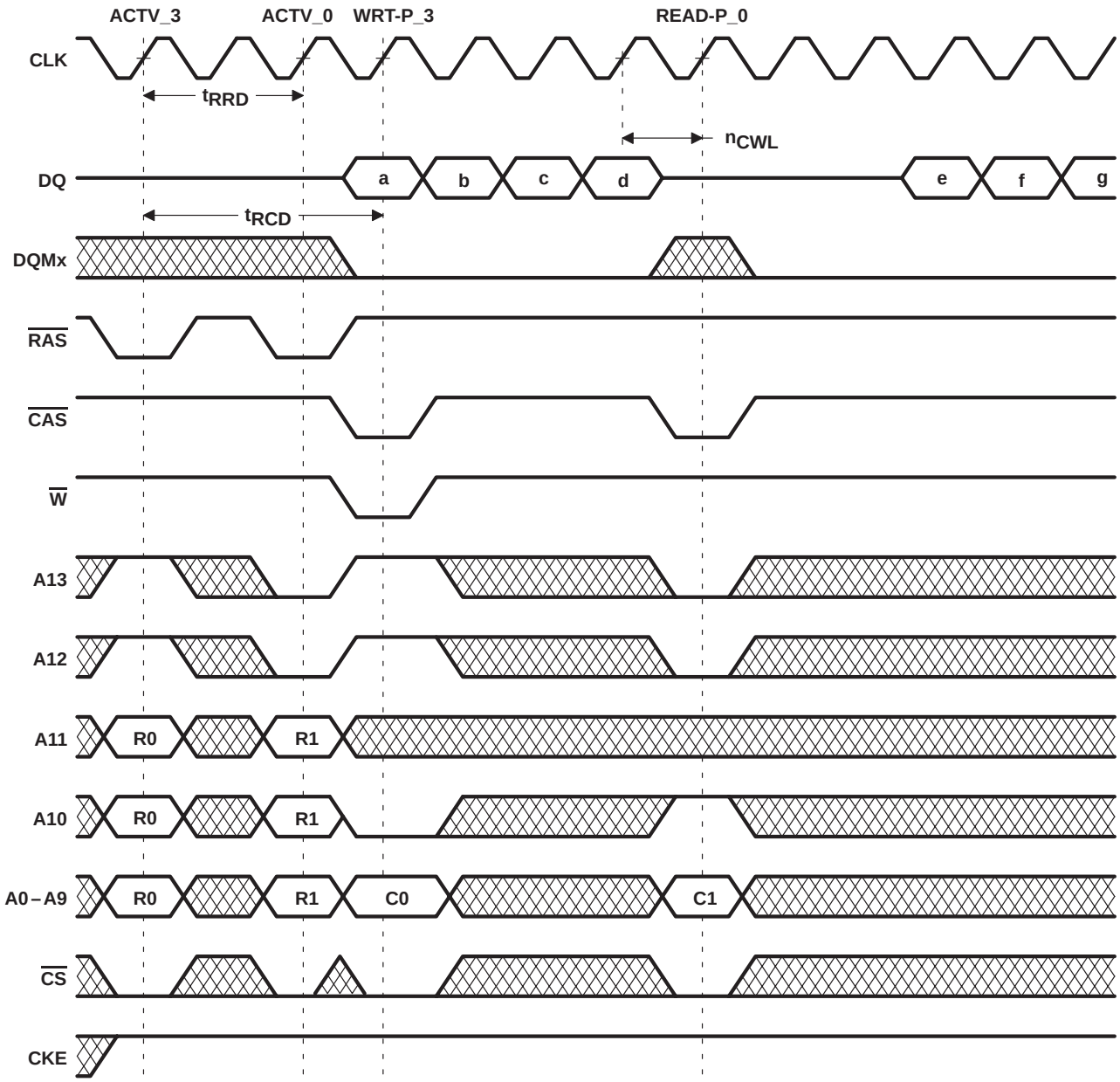


BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	0	R0	C0†	C0+1	C0+2	C0+3				
D	2	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the ’664xx4 at 125 MHz.

Figure 31. Read-Burst Bank 0, Write-Burst Bank 1 (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

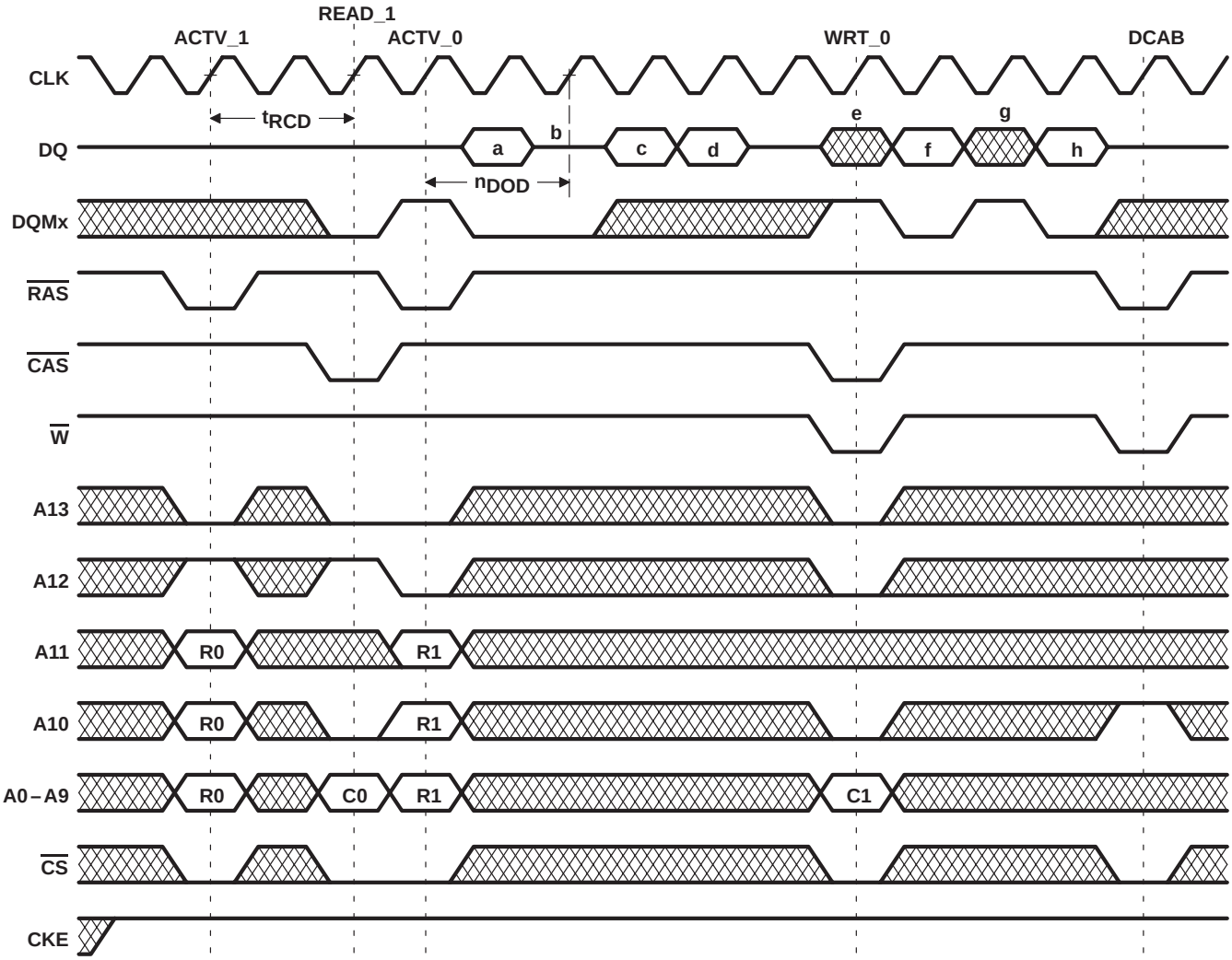


BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
D	3	R0	C0†	C0+1	C0+2	C0+3				
Q	0	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum n_{CWL}, t_{RRD}, and t_{RCD} for the '664xx4 at 125 MHz.

Figure 32. Write-Burst Bank 3, Read-Burst Bank 0 With Automatic Deactivate (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

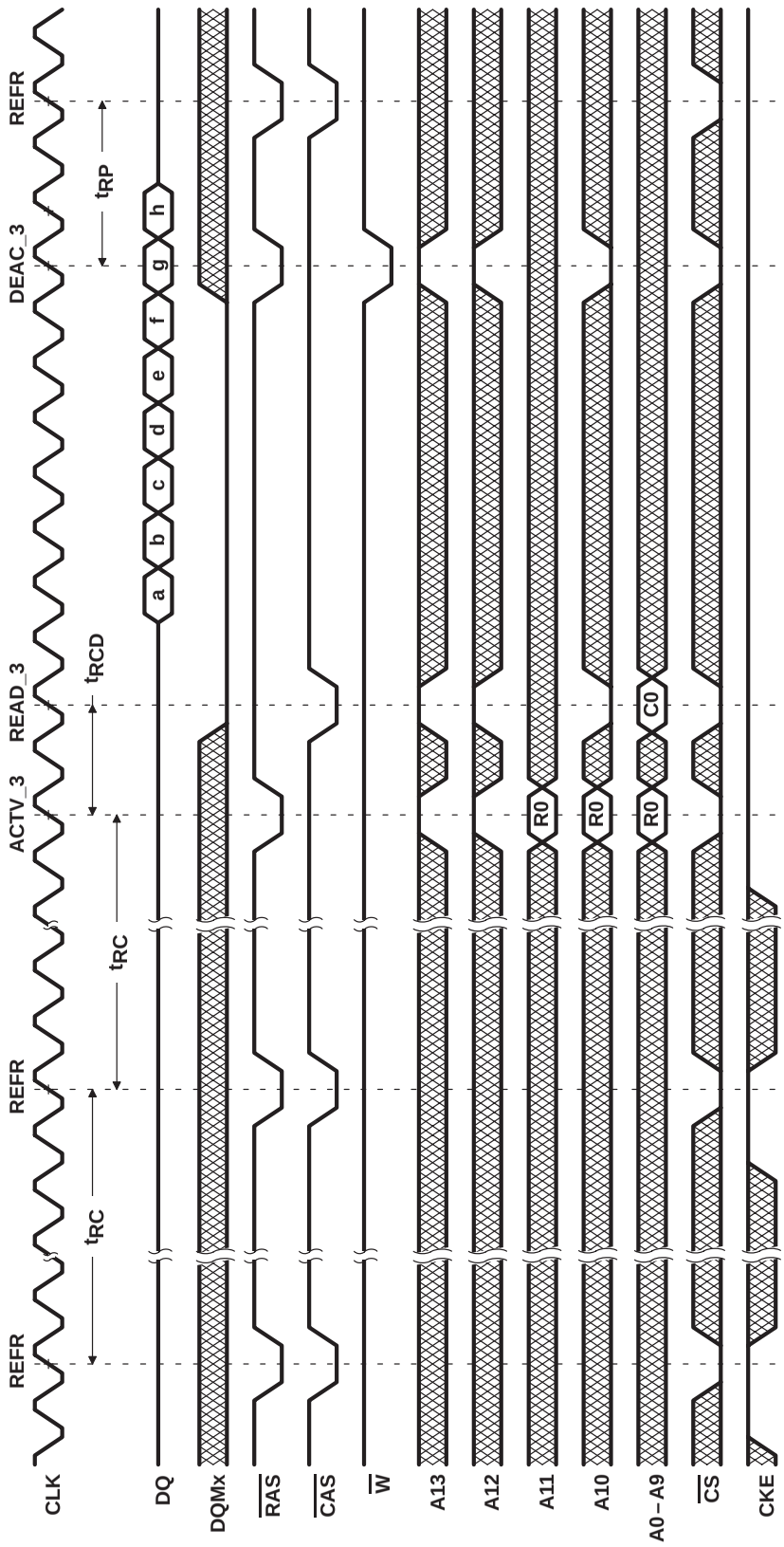


BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	1	R0	C0†	C0+1	C0+2	C0+3				
D	0	R1					C1	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} for the ’664xx4 at 100 MHz.

Figure 33. Use of DQM for Output and Data-In Cycle Masking (Read-Burst Bank 1, Write-Burst Bank 0, Deactivate All Banks) (CAS latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



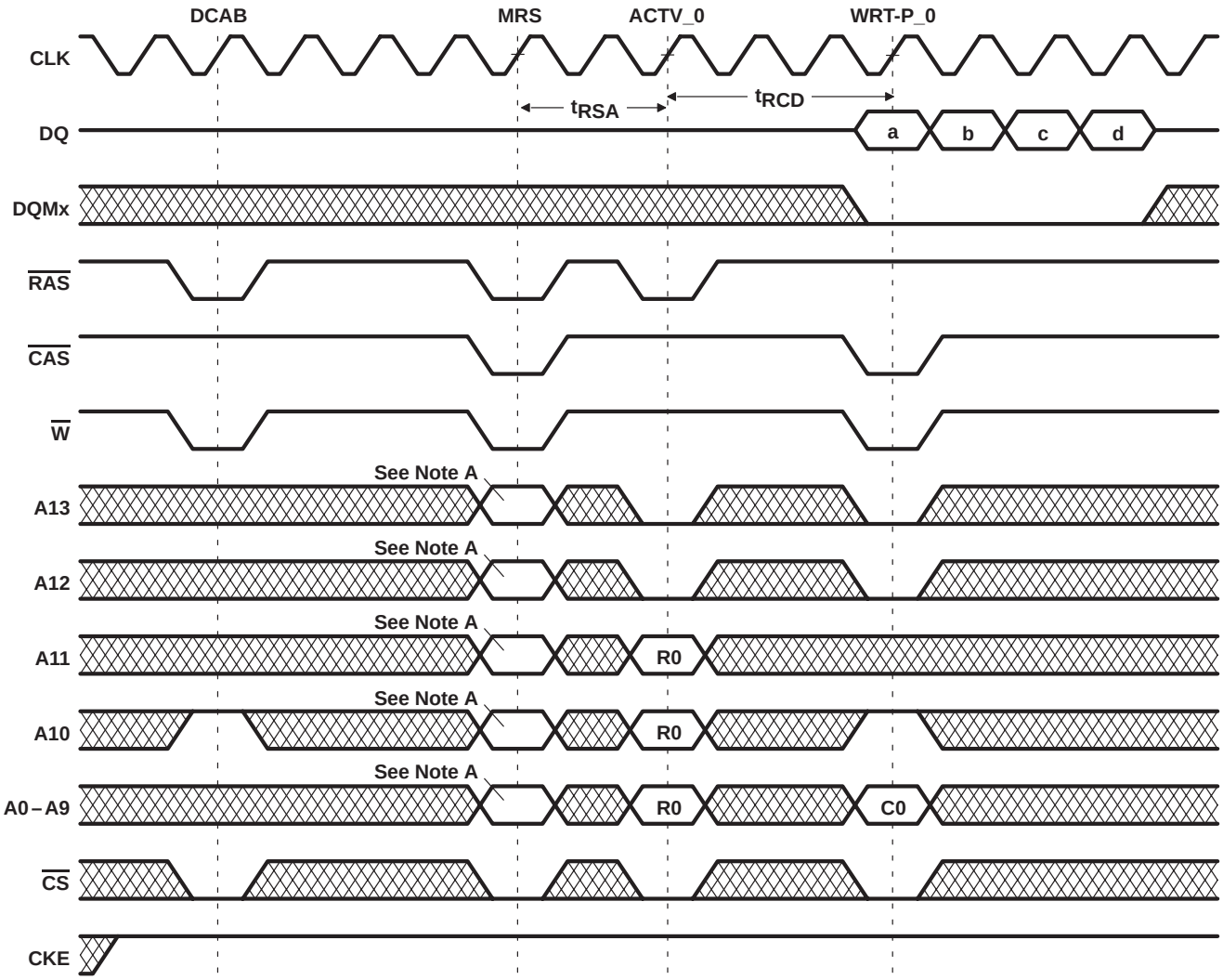
BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h
Q	3	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and starting address C0 (see Table 6).

NOTE A: This example illustrates minimum t_{RC}, t_{RCD}, and t_{RP} for the '664xx4 at 100 MHz.

Figure 34. Refresh Cycles (Refreshes Followed by Read Burst, Followed by Refresh)
(CAS latency = 2, burst length = 8)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d
D	0	R0	C0†	C0+1	C0+2	C0+3

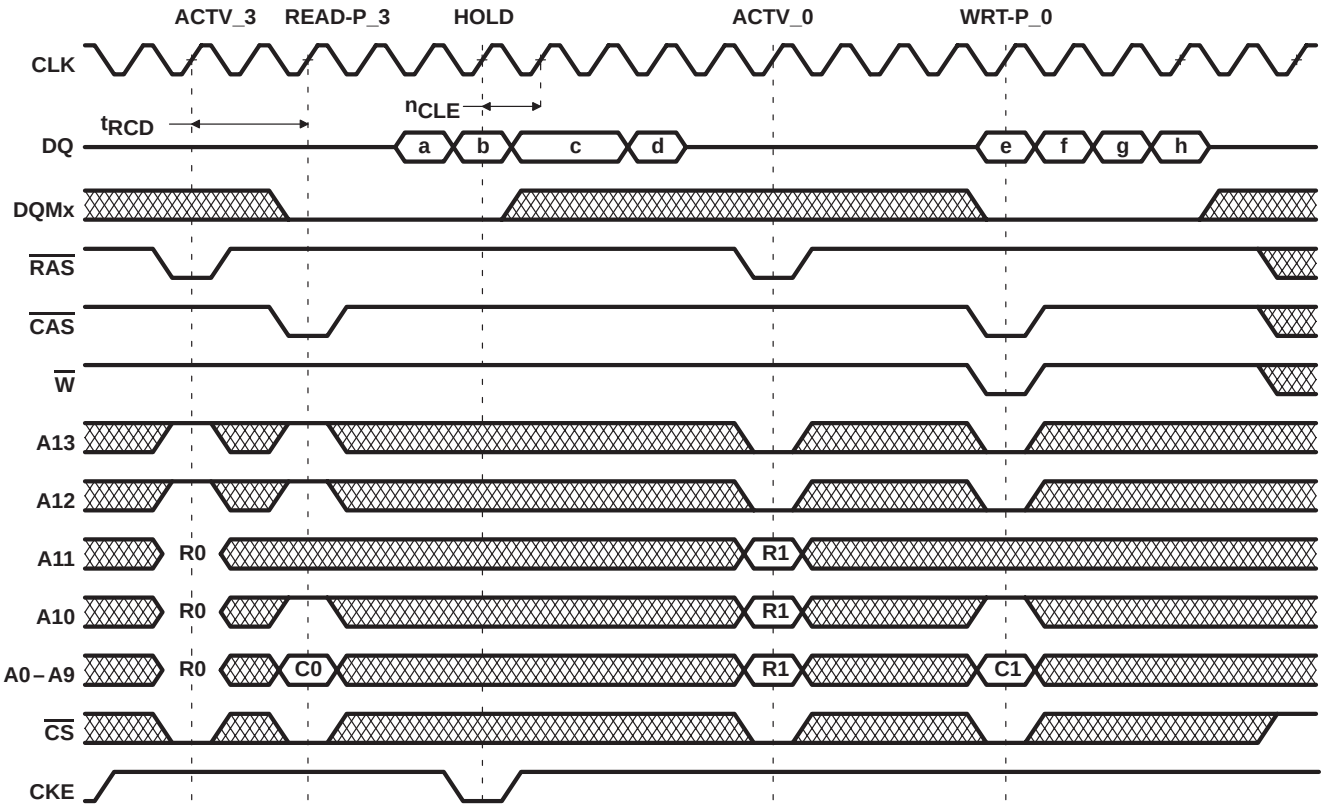
† Column-address sequence depends on programmed burst type and starting address C0 (see Table 5).

NOTES: A. Refer to Figure 2 (for setting mode registers)

B. This example illustrates minimum t_{RCD} and t_{RSA} for the ’664xx4 at 125 MHz.

Figure 35. Mode-Register Programming
(Deactivate All, Mode Program, Write Burst With Automatic Deactivate)
(CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(0–3)	ADDR	a	b	c	d	e	f	g	h
Q	3	R0	C0†	C0+1	C0+2	C0+3				
D	0	R1					C1†	C1+1	C1+2	C1+3

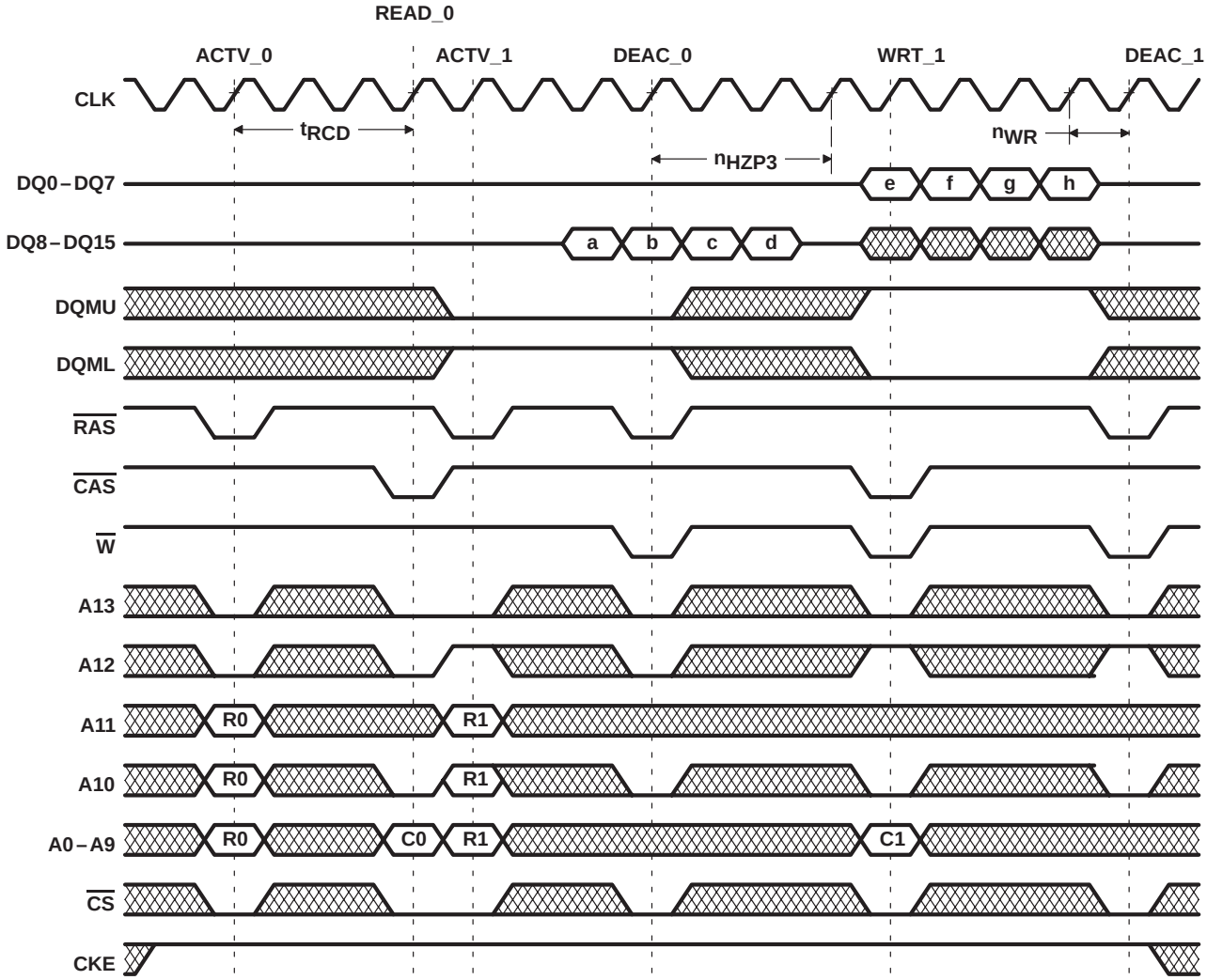
† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTES: A. This example illustrates minimum t_{RCD} and t_{APW} for the ’664xx4 at 100 MHz.

B. If entering the PDE command with violation of short t_{APW}, the device is still entering the power-down mode and then both banks are deactivated (still in power-down mode).

Figure 36. Use of CKE for Clock Gating (Hold) and Standby Mode (Read-Burst Bank 3 With Hold, Write-Burst Bank 0, Standby Mode) (CAS latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



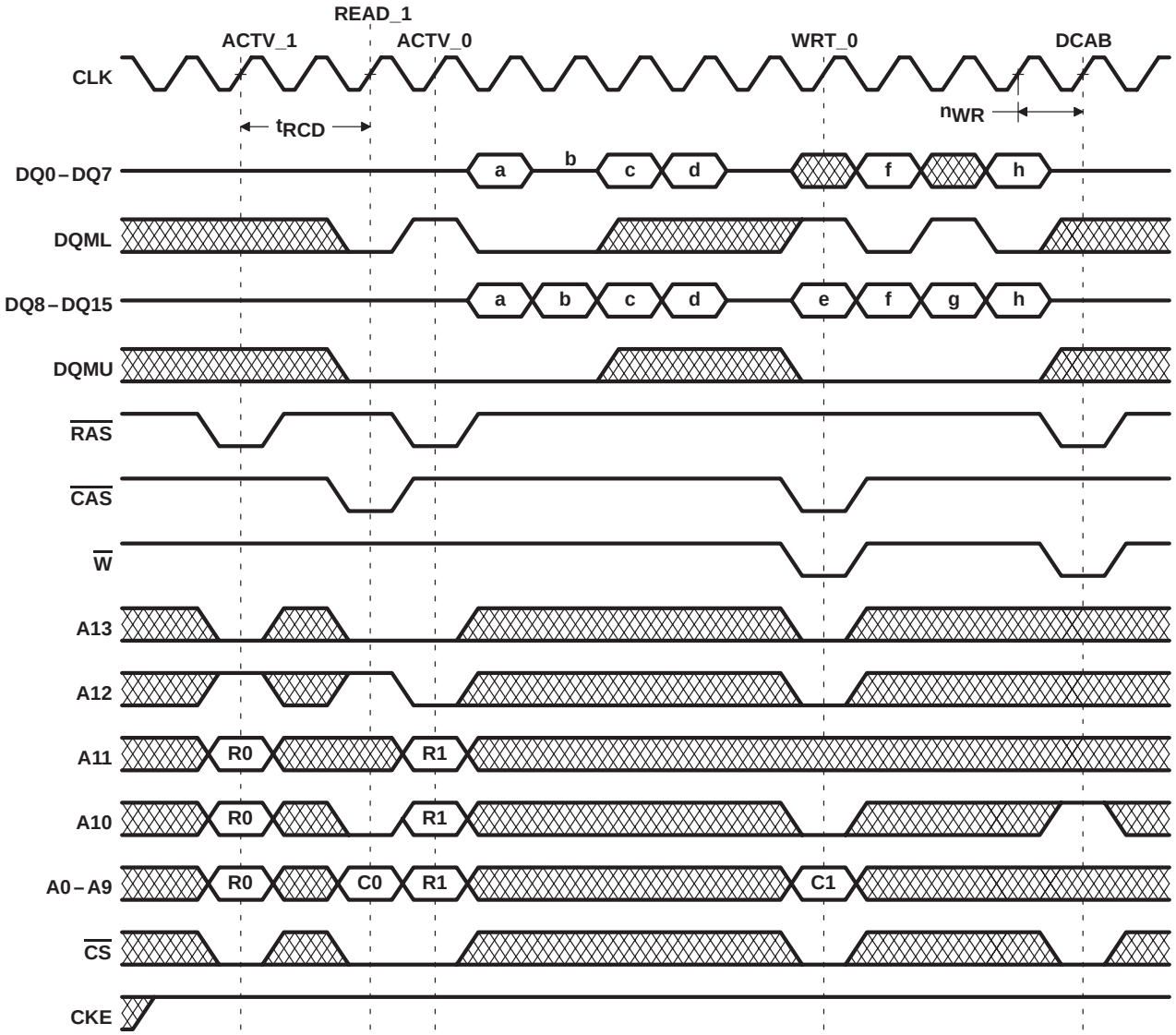
BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	0	R0	C0†	C0+1	C0+2	C0+3				
D	1	R1					C1†	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTE A: This example illustrates minimum t_{RCD} read burst, and a minimum n_{WR} write burst for the ’664xx4 at 125 MHz.

Figure 37. Read-Burst Bank 0, Write-Burst Bank 1 (With Lower Bytes Masked Out During the READ Cycles and Upper Bytes Masked Out During the WRITE Cycles) (Only for x16) (CAS latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

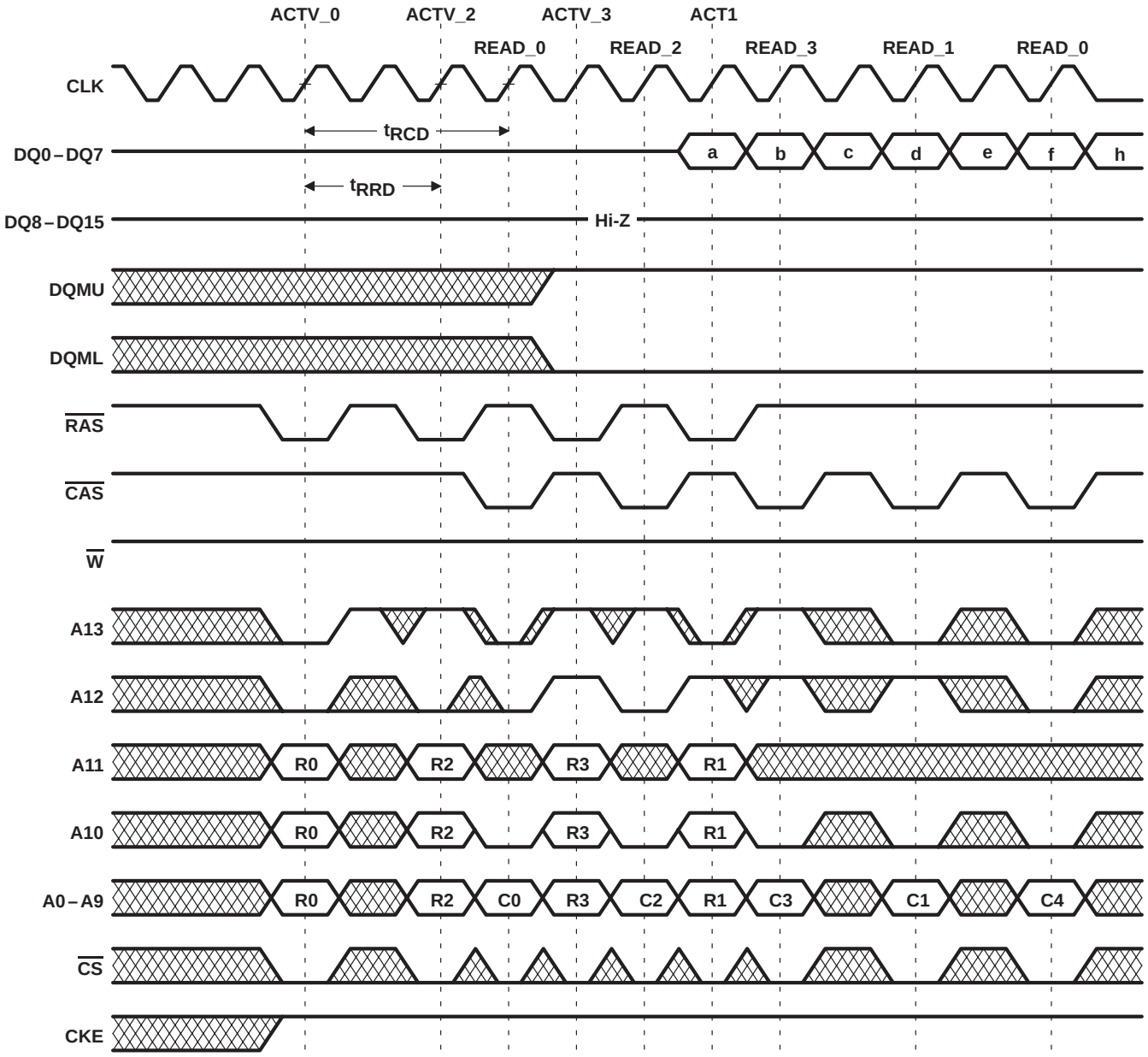


BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	1	R0	C0†	C0+1	C0+2	C0+3				
D	0	R1					C1†	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).
NOTE A: This example illustrates minimum t_{RCD} and a minimum n_{WR} write burst for the ’664xx4 at 100 MHz.

Figure 38. Use of DQM for Output and Data-In Cycle Masking (Read-Burst Bank 1, Write-Burst Bank 0, Deactivate All Banks) [Only Masked Out the Lower Bytes (Random Bits)] for x16 (CAS latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

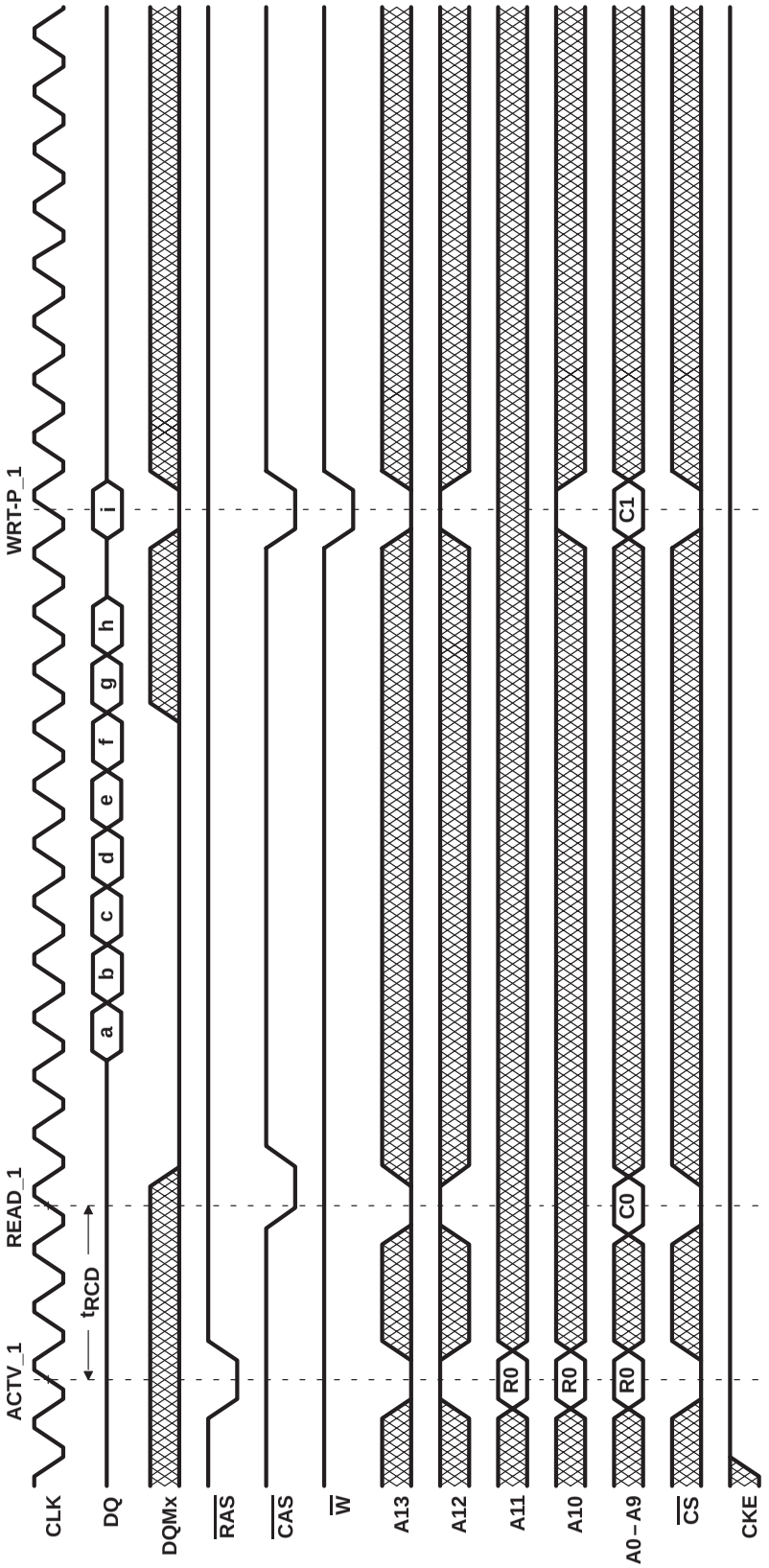


BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	0	R0	C0†	C0+1						
Q	2	R2			C2	C2+1				
Q	3	R3					C3	C3+1		
Q	1	R1							C1	C1+1

† Column-address sequence depends on programmed burst type and starting addresses C0, C1, C2, and C3 (see Table 4).
NOTE A: This example illustrates minimum t_{RCD} and minimum t_{RRD} for the '664xx4 at 125 MHz.

Figure 39. Four-Bank Column-Interleaving Read Bursts (With Upper Bytes to be Masked) (Only for x16) (CAS latency = 3, burst length = 2)

PARAMETER MEASUREMENT INFORMATION



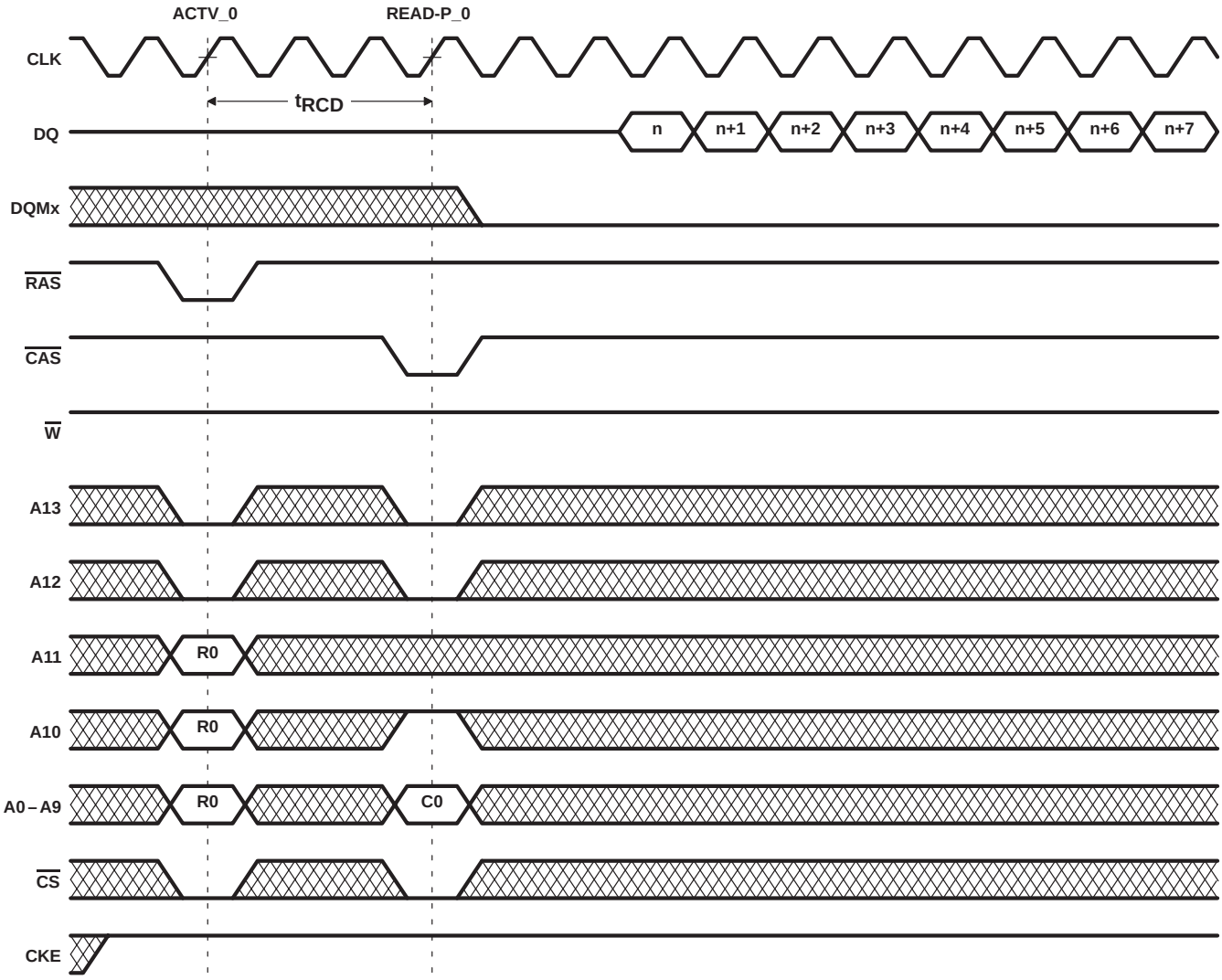
BURST TYPE (D/Q)	BANK (0–3)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h	i
Q	1	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7	
D	1	R0									C1

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 6).

NOTE A: This example illustrates minimum t_{RCD} for the '664xx4 at 125 MHz.

Figure 40. Read Burst — Single Write With Automatic Deactivate (CAS latency = 3, burst length = 8)

PARAMETER MEASUREMENT INFORMATION

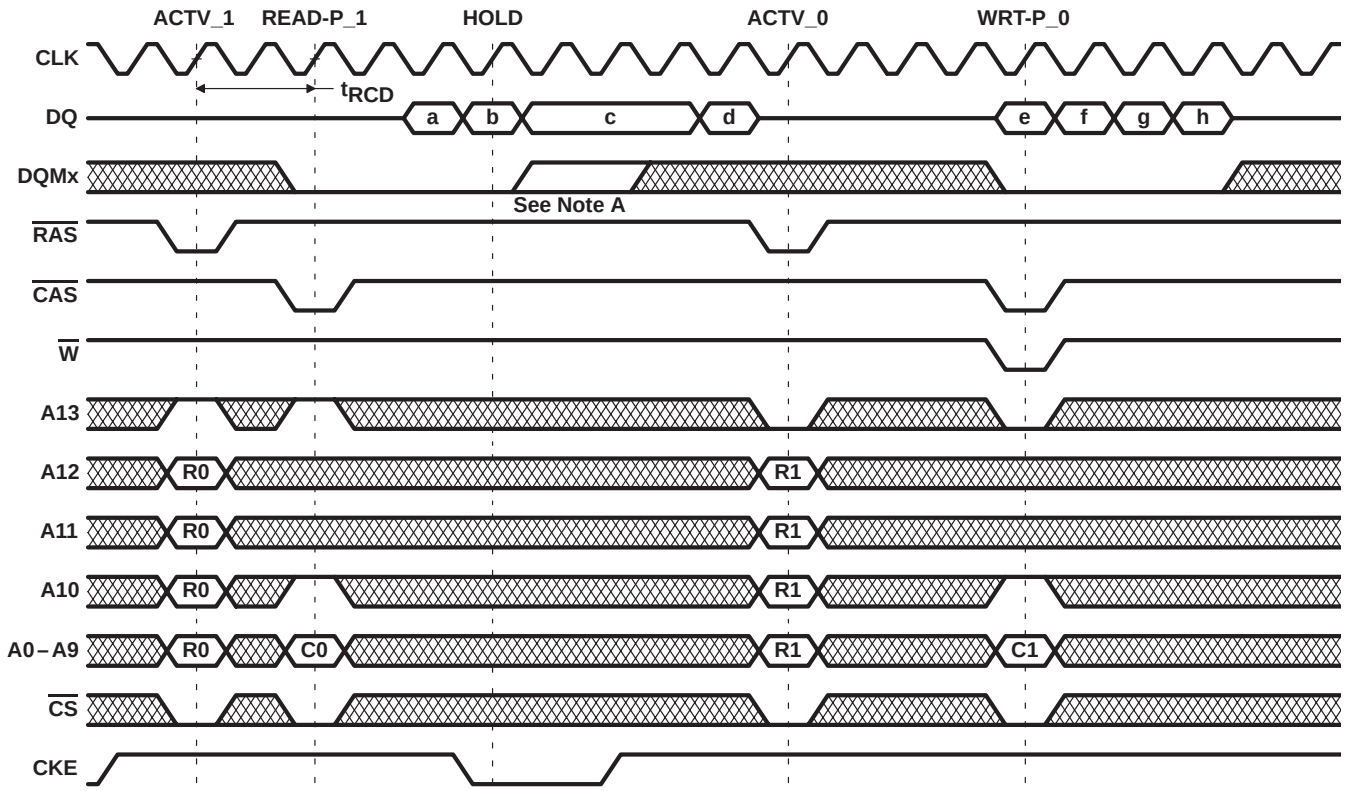


BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(0 – 3)	ADDR	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
Q	0	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 6).
NOTE A: This example illustrates minimum t_{RCD} for the ’664xx4 at 125 MHz.

Figure 41. Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8) (for x16)

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (0 – 1)	ROW ADDR	BURST CYCLE a	b	c	d	e	f	g	h
Q	1	R0	C0†	C0 + 1	C0 + 2	C0 + 3				
D	0	R1					C1	C1 + 1	C1 + 2	C1 + 3

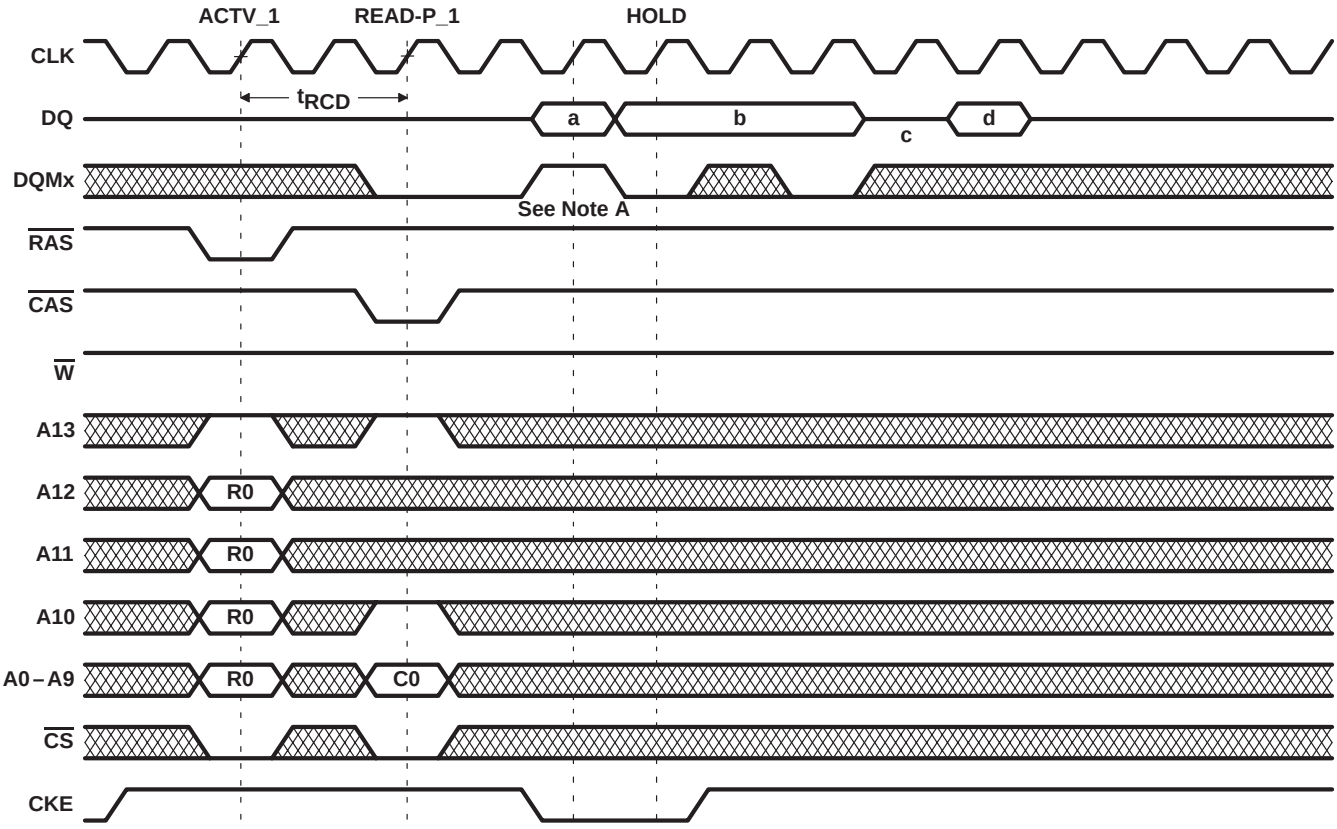
† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTES: A. These rising clocks during output “c” with DQMx = Hi do not mask out the output “d” due to CKE inserted low to suspend those rising clocks at cycle DQMx = Hi.

B. This example illustrates minimum t_{RCD} for the ’664xx4 at 100 MHz.

Figure 42. Use of CKE for Clock Gating (Hold/Suspend) and DQM = Hi Showed No Effect (CAS latency = 2, burst length = 4, two banks)

PARAMETER MEASUREMENT INFORMATION



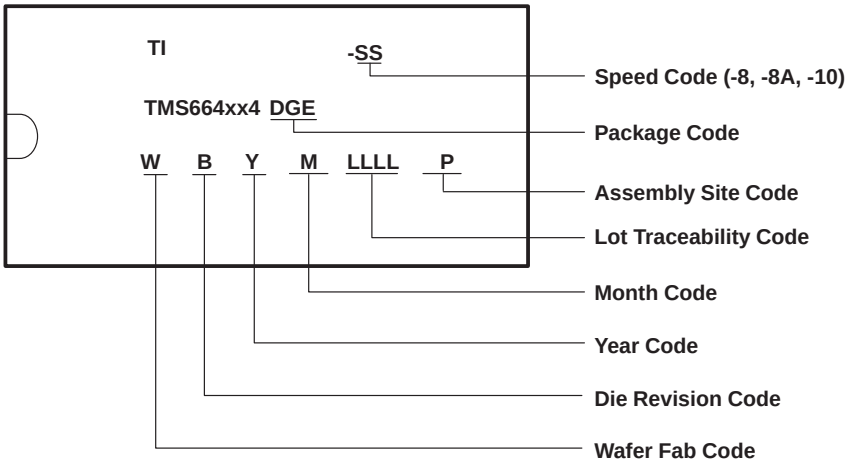
BURST TYPE (D/Q)	BANK (0 – 1)	ROW ADDR	BURST CYCLE a	b	c	d
Q	1	R0	C0†	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and starting addresses C0 and C1 (see Table 5).

NOTES: A. This example illustrates that the DQM mask is also delayed when a HOLD/Suspend is in progress.
B. This example illustrates minimum t_{RCD} for the '664xx4 at 100 MHz.

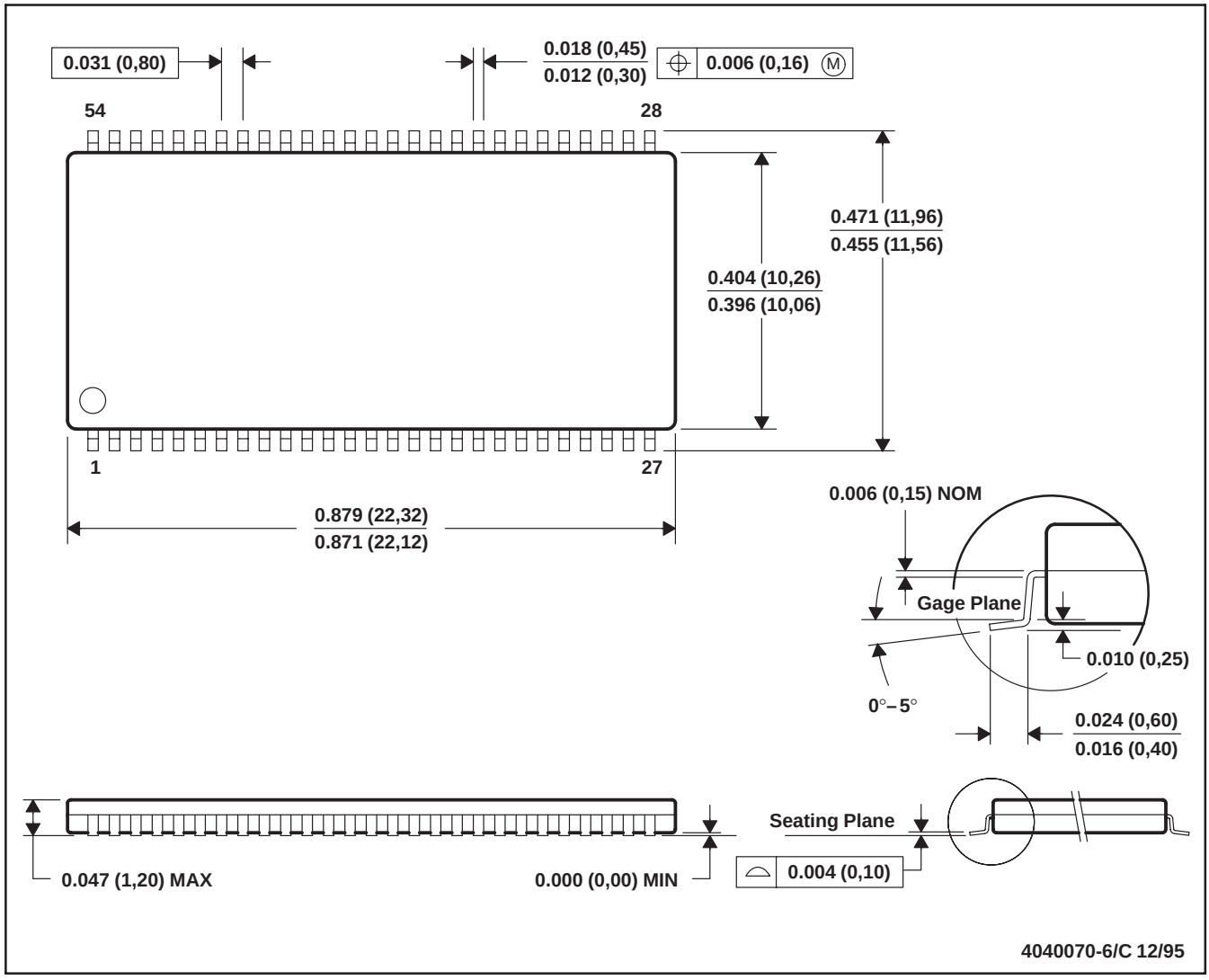
Figure 43. DQMx Mask Delay As the Hold/Suspend In Progress (CAS latency = 2, burst length = 4)

device symbolization



MECHANICAL DATA

DGE (R-PDSO-G54) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

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TMS664414 - http://www.ti.com/product/tms664414?HQS=TI-null-null-dscatalog-df-pf-null-wwe

TMS6641648A - http://www.ti.com/product/tms6641648a?HQS=TI-null-null-dscatalog-df-pf-null-wwe

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