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ECEN 3002

8 October 2020

Project 1 Phase 1 Write Up

For the most part, the project is going well, however, I am unable to properly test the project on my monitor as it is not compatible with the VGA signal coming from the DE10. Initially, I thought it was an error with my code, but eventually found out it was simply my monitor due to the code working on my partner’s older monitor and the lack of a boot up image on my monitor when the board is turned on.

Nonetheless, I was able to confirm functionality of the project through Modelsim. I’m able to see all the signals acting as expected, more specifically am able to see the roll over of the vertical counter from 524 to 0, which then initiates the expected VS pulse. This simulation proves the VTC file is implemented correctly. A header file was created for the VTC file in order to easily change resolutions for future applications.

In addition, my partner and I were able to get a moving red block image to appear on his monitor. The block could’ve been any color by changing the various values in the R, G, and B registers, but the focus was on creating a simple display to prove operation. However, we did have issues trying to create other images, for example two moving blocks, but decided to turn in as is.

The implementation of signal tap also worked very well. It was cool to learn how to use the on board Logic Analyzer as it will be surely a useful skill for analyzing signals from more complex FPGA designs.

Overall, I am very happy with the progress made in phase one. Although it is slightly less exciting due to the lack of implementing the application on my own monitor, its still rewarding to see the design function on my partner’s. This project provided a great learning experience as I have never previously designed a video signal nor have I utilized a PLL. I am looking forward to expanding on more complex graphics and designs in the future.